A 0.7-V 17.4-μW 3-Lead Wireless ECG SoC

Mahmood Khayatzadeh, *Student Member, IEEE*, Xiaoyang Zhang, *Student Member, IEEE*, Jun Tan, *Member, IEEE*, Wen-Sin Liew, *Member, IEEE*, and Yong Lian, *Fellow, IEEE*

***Abstract*—This paper presents a fully integrated sub-1 V 3-lead wireless ECG System-on-Chip (SoC) for wireless body sensor network applications. The SoC includes a two-channel ECG front-end with a driven-right-leg circuit, an 8-bit SAR ADC, a custom-designed 16-bit microcontroller, two banks of 16 kb SRAM, and a MICS band transceiver. The microcontroller and SRAM blocks are able to operate at sub-/near-threshold regime for the best energy consumption. The proposed SoC has been implemented in a standard 0.13-μm CMOS process. Measurement results show the microcontroller consumes only 2.62 pJ per instruction at 0.35 V. Both microcontroller and memory blocks are functional down to 0.25 V. The entire SoC is capable of working at single 0.7-V supply. At the best case, it consumes 17.4 μW in heart rate detection mode and 74.8 μW in raw data acquisition mode under sampling rate of 500 Hz. This makes it one of the best ECG SoCs among state-of-the-art biomedical chips.**

***Index Terms*—Electrocardiograph (ECG), microcontroller, sub-threshold, system-on-chip, ultra-low-power, wireless.**

I. Introduction

PERVASIVE, predictive, preventive, and personalized healthcare is envisaged being the future of medicine. This paradigm shift requires the support of innovative sensor technologies, especially wireless body sensor networks (WBSN) formed with various wearable biomedical sensors. This type of sensors has very stringent power requirement due to constraints on battery life and form factor. Therefore, ultra-low power design is essential in the development of these sensors in addition to low cost. SoC implementation is an attractive option in terms of cost, size, and performance.

Cardiac arrhythmias and coronary heart disease constitute significant public health burdens. Atrial fibrillation, a common arrhythmia, afflicts nearly 9% of persons over 80 years old, and is associated with increased stroke risk [1]. Early diagnosis presents an opportunity for preventive treatment. However, many patients with cardiac arrhythmia or silent myocardial ischemia remain undiagnosed and untreated, because abnormal ECG episodes often occur sporadically and are easily missed. Hence, there is a need for low cost and easy to use wearable wireless ECG sensors.

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The authors are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117583, Singapore (e-mail: mahmood@nus.edu.sg; xz@nus.edu.sg; eletj@nus.edu.sg; elelws@nus.edu.sg; eleliany@nus.edu.sg).

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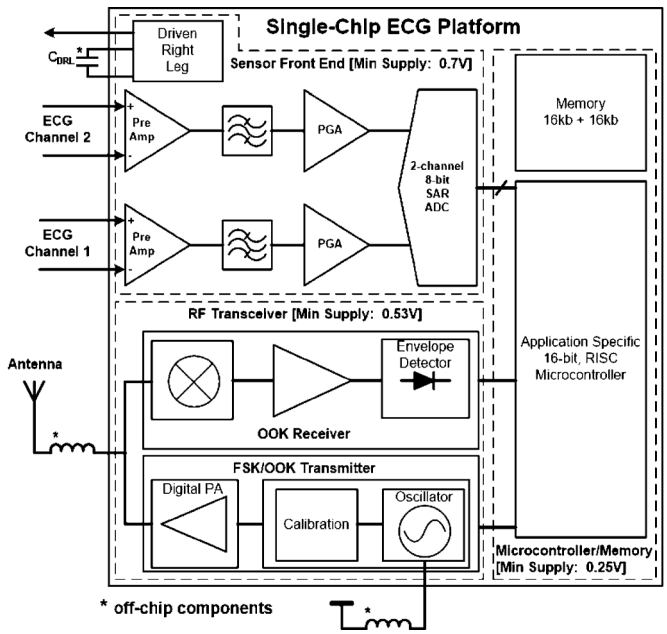

Fig. 1. Block diagram of the proposed single-chip ECG platform.

The development of ECG SoC has attracted much attention in recent years [2]–[8]. Some of ECG SoCs [3]–[6] integrate microcontroller or microprocessor on the chip to conduct pre-processing in order to minimize the wireless transmission of raw data. Commercial low-power microcontrollers, e.g., PIC and MSP430, and ultra-low-power implementations in [3], [9] are not power-efficient choices for the target application as they need abundant clock cycles to implement a common task like filtering. On the other hand, more powerful DSPs [10] are too power hungry and thus not suitable for power-limited biomedical SoC. As a result, a low-power microcontroller core with a few carefully-selected DSP features is a more appropriate choice for wireless biomedical sensors. In addition, biomedical sensors often demand a large block of memory to facilitate burst mode wireless transmission. In some of previous works [3], [6], the memory is placed in a separate and higher voltage domain, which increases power consumption and requires additional supply. In this paper, we present an ultra-low power ECG SoC that addresses issues in existing solutions.

This paper is organized as follows. In Section II, the architecture of the proposed wireless ECG SoC is presented, followed by the description of each sub-block in Section III. Section IV shows chip implementation details and discusses measurement results. Conclusion is drawn in Section V.

II. Programmable Wireless Biomedical Platform

The block diagram of the proposed wireless ECG platform is shown in Fig. 1. The system front-end has two fully-dif-

ferential channels for a typical 3-lead ECG recording, which performs signal filtering and amplification for ECG inputs before the quantization. A driven-right-leg (DRL) circuit is implemented to reduce common-mode interferences, especially from 50-Hz or 60-Hz power-line noises. A 2-channel 8-bit SAR ADC provides simultaneous sampling for both channels but quantizes them sequentially. Multiplexing after quantization removes any cross-talk between two channels. Simultaneous sampling is necessary to construct the third lead ECG signal based on the signals from other two leads. The output of the ADC is connected to a novel 16-bit RISC microcontroller customized to meet the special requirements of biomedical signal processing. The proposed instruction set improves computational efficiency for signal processing. To facilitate an effective communication between ADC and microcontroller, an interrupt port is dedicated to indicate the end of AD conversion. Two banks of 16 kb ultra-low-power sub-threshold SRAM are implemented for both program code storage and ECG signals buffering. They facilitate feature extraction and lossless data compression before transmitting via RF link, leading to significant reduction in the amount of transmitted raw data. In addition, duty cycling of the RF link is implemented to further optimize power consumption of the entire system. The proposed SRAM is working at the same voltage as the rest of the digital core e.g., 0.7-V, which eliminates the high supply voltage and level shifters at interfaces.

The microcontroller is connected to a Medical Implantation Communication Service (MICS) band transmitter via a configurable serial port to send raw or processed ECG data to a gateway. The serial port allows both synchronous and asynchronous transmissions. The transmitter needs only two off-chip inductors, which minimize the cost of external components. Furthermore, the SoC also integrates a receiver to ensure a reliable communication between sensor and gateway via RF link. As the amount of data in the transmit path is much higher than the receive path, a high-data rate FSK transmitter is used at the transmitter while a low-data rate OOK receiver is implemented in the receiving path.

To achieve ultra-low power, the proposed SoC is designed to operate at low voltage. For single-supply operation, the SoC can work under a 0.7-V supply. Digital sub-systems, i.e., microcontroller and SRAMs, are fully functional with a supply as low as 0.25 V. The RF transceiver is functional at 0.53 V.

III. Circuit Implementation

A. Sensor Front-End

A 2-channel fully integrated analog front-end is designed for the system, as shown in Fig. 2. Each ECG channel consists of an instrumentation amplifier (IA) and a programmable-gain amplifier (PGA) [2].

The IA uses capacitive-coupled input structure for its low-power dissipation and simplicity. To filter out low-frequency baseline fluctuations and ECG electrodes offsets under 0.67 Hz [11], high impedance pseudo-resistors are required. Conventional nominal-V_t pseudo resistors can only provide up to GΩ resistance due to the increasing leakage current under

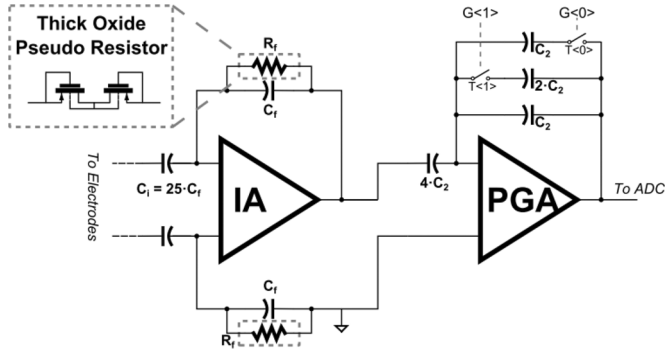

Fig. 2. Analog front-end amplifier circuit.

0.13-μm CMOS process. In this scenario, about 100 pF capacitance is required for C_f to achieve sub-0.67 Hz high-pass cut-off frequency, which is difficult and wasteful for on-chip implementation. To solve this problem, our design uses two high-V_t thick-oxide PMOS transistors for the pseudo-resistor. Post-layout simulation shows the resistance is boosted from 4.9 GΩ to 583.1 GΩ by changing the thin-oxide PMOS transistors to thick-oxide ones. As a result, capacitor C_f with several pF is sufficient to meet the high-pass requirement.

The DRL circuit suppresses the common-mode noise using negative feedback. It compares the 3-lead common-mode signal with the AC ground $V_{\rm CM}$ and drives the body through the right-leg electrode. For maximum noise reduction, the DRL gain is tunable through an external capacitor $C_{\rm DRL}$ shown in Fig. 1. The total power consumption is less than 0.7 μW.

The digital multiplexing scheme [12] is modified to facilitate simultaneous AD conversion of 2 ECG channels. Fig. 4(a) and (b) show the schematic and timing diagram of the 2-channel 8-bit SAR ADC. Independent S/H stages are employed for each channel and multiplexing is performed in the digital domain, thus avoid the use of the analog multiplexer. Furthermore, channel crosstalk is avoided because every channel is now independent of each other and the multiplexing happens only after quantization. In this work, the SAR logic is reconfigured so that signal sampling for all channels are performed simultaneously while quantization is performed on each channel in sequential order. A complete AD conversion takes 40 clock cycles as shown in Fig. 3(b). The first 10 clock cycles are for simultaneous signal sampling. Quantization takes place after another 10 clock cycles and lasts for 20 clock cycles for two channels. The additional 10 clock cycles between sampling and quantization are to misalign the two phases and also allow the DAC array to be reset.

Since signal sampling is performed simultaneously, the sampled signals have to be hold until AD conversions in both channels are completed. As technology scales down, the leakage current at the sampling switch and the input gate of the comparator becomes an issue when the holding time is much longer due to slow target conversion rate (<1 kS/s for the ECG application). Although an increased ADC clock frequency helps to shorten the holding time, it dissipates more power in the clock generation which is undesirable in the low-power design. Although the use of high-V_t device can minimize the leakage current but it will demand larger device size in order to achieve the same

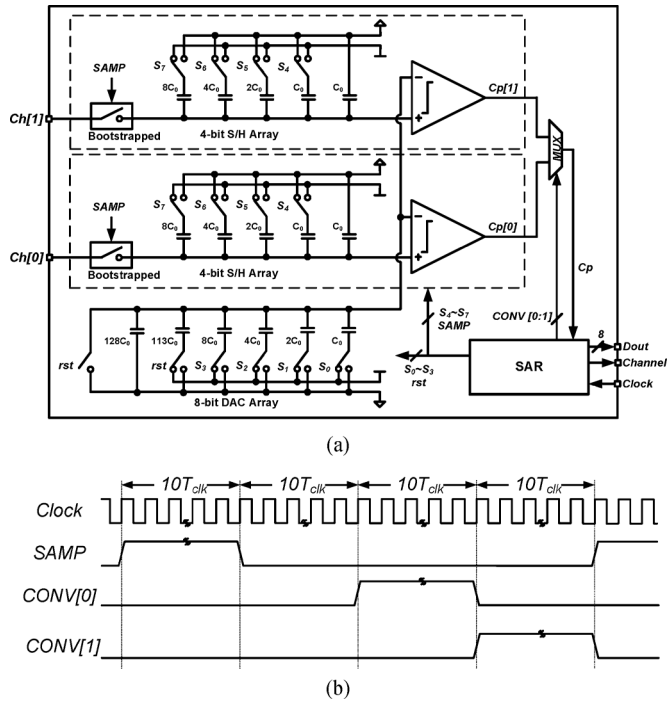

Fig. 3. (a) Simplified schematic and (b) timing diagram of the 2-channel SAR ADC based on the digital multiplexing scheme.

$R_{\rm on}$ for the sampling switch and same accuracy (i.e., speed and resolution) for the comparator. Consequently, this will result in larger parasitic capacitance associated with the capacitor array and thus non-linearity in the ADC. On the other hand, the sampling switch with boosted turn-off [13] can be used to suppress the leakage current in the sampling switch. However, this technique requires a twin-well process which is unavailable in the target technology. Therefore, the leakage current has to be carefully considered during design. The change in the sampled voltage due to leakage over holding time must be less than 1/2 LSB, which is given by

$$\Delta V_{\rm sampled} = \frac{i_{\rm leakage}}{C_{S/H}} \cdot t_{\rm holding} < \frac{1}{2}{\rm LSB} \qquad (1)$$

where $i_{\rm leakage}$ is the total leakage current from the common node of the sampling capacitor, $C_{S/H}$ is the total capacitance of S/H array, and $t_{\rm holding}$ is the worst-case holding time for the sampled voltage. Equation (1) implies that $C_{S/H}$ has to be large enough to sustain the leakage throughout holding time. The use of high-density capacitor option, which provides higher capacitance value with smaller area, proved to be more advantageous in this case as compared to low-density capacitor option. Furthermore, overdesign of the sampling switch and comparator must be avoided to keep $i_{\rm leakage}$ as small as possible.

B. Sub-Threshold Application Specific 16-Bit RISC Microcontroller

A new 16-bit sub-threshold application-specific microcon troller has been proposed and integrated into the system. The novelties include a low power sub-threshold SRAM cell,

TABLE I
INSTRUCTION SET AND ADDRESSING MODES OF THE PROPOSED BIOMEDICAL MICROCONTROLLER CORE

Instruction set		Addressing Modes
Arithmetic	ADD, ADDC, SUB, SUBC, CMP, MUL, MAC	Register (R1, R2, R3) Immediate Direct Indirect Indirect-Auto-Increment Indirect-Auto-Decrement
Logical	AND, OR, XOR, INV, RRA, RRC, RLA, RLC, TEST	
Load and Store	MOV, LOADL, LOADH, LOAD, IN, OUT, PUSH, POP	
Branch	CALL, RET, RETI, JMP, JZ, JC, JP, JV	
Special	SLEEP	

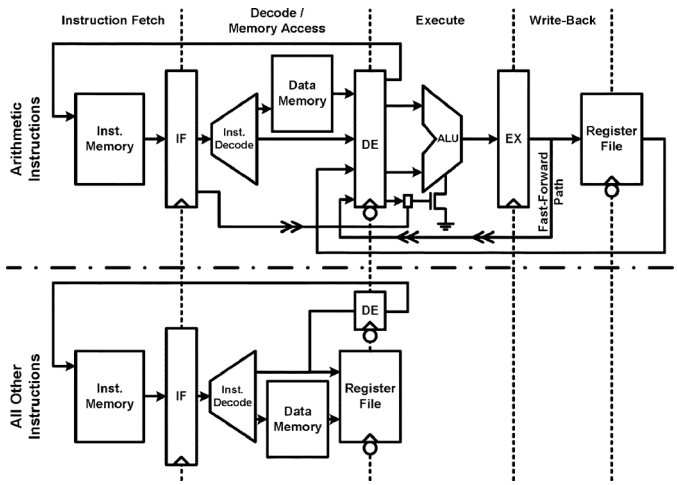

Fig. 4. Microarchitecture of the proposed microcontroller core.

the new biomedical microcontroller architecture which includes DSP-like instruction sets such as multiply-accumulate, and DSP-like addressing modes such as auto-increment and auto-decrement. The proposed architecture allows efficient implementation of biosignal processing algorithms including filter, data compression, and more. The architecture is kept concise and efficient in order to reduce power for power-limited sensor applications. The proposed core has a RISC instruction set which includes 33 instructions and 6 different addressing modes as summarizes in Table I. All instructions are 16-bit wide and executed every one clock cycle i.e., average clock-per-instruction (CPI) is 1. The microcontroller has three general purpose and one indirect addressing registers. All internal registers and data paths are 16 bits and ALU operations are performed on 16-bit data.

The core features Harvard architecture and a carefully designed 4-stage pipeline as shown in the microarchitecture diagram in Fig. 4. This microarchitecture is designed in such a way that it prevents any hazard or stall in the pipeline and executes all branches, call, and interrupt in one cycle. The number of stages in the pipeline depends on the type of instruction. All arithmetic operations will go through instruction fetch (IF), decode (DE) and data memory access, execute (EX), and write-back (WB) stages. Every stage is completed within half clock cycle. The custom-designed asynchronous SRAM allows data access during half period of the clock. If the result of one arithmetic operation is going to be used in the next instruction,

a fast-forward path bypasses the write-back stage and transfers the result of the previous instruction directly to the decode stage of the next instruction. All other instructions need only the first two stages to be executed as can be seen from the lower section of Fig. 4. This flexible configuration allows saving power during operation modes like transferring blocks of data, by turning off whole ALU via a power switch.

The proposed instruction set architecture (ISA) has been evaluated by comparing its performance against widely-used ultra-low-power architectures like PICmicro from Microchip [14] and MSP430 from Texas Instruments [15]. PICmicro has 8-bit RISC architecture with 49 instructions and 3 addressing modes while MSP430 features a 16-bit RISC architecture with 27 instructions and 7 addressing modes. For the purpose of this comparison, various biomedical applications were reviewed and three commonly-used tasks in the digital back-end of such applications were selected. The first selected task was filtering. Filters are used to smooth the signal, select or reject specific frequency band [16], or as matched-filter to detect a pattern [17]. In this comparison, a 16-tap finite impulse response (FIR) filter was implemented in each microcontroller. Power calculation was selected as the second task. Calculating average power of the signal over a window is required in various feature extraction algorithms [16]. Therefore, an average power calculation routine over a 16-sample window was implemented in each microcontroller family. Finally, error-detection is required during transmission of the signal from the sensor node to the base station. Therefore cyclic redundancy check (CRC), as an effective error detection algorithm, was selected as the third task. The 5-bit CRC which is used in radio frequency identification (RFID) systems [18] was implemented as it is intended for very-low-power applications. These three routines are a fair representation of the whole digital back-end link from pre-processing and feature extraction to signal transmission.

All tasks were implemented in the PICmicro, MSP430 and the proposed ISA. 12-bit signed data was considered for all tasks as it is a common and acceptable bit size for biomedical applications. The implemented routines were examined for the code size and the number of clock cycles required to execute the task. As the instruction width is different among these microcontrollers, the code size in terms of the number of bits was used in the comparison. Smaller code size implies that a smaller code memory can be used in the system which translates to less leakage and active power in the memory. Fig. 5(a) shows the comparison of the code size of the implemented tasks in three microcontrollers. As can be seen, the proposed instruction set considerably improves the code size in computational intensive tasks like filtering and power calculation.

Next, the number of clock cycles required to complete one iteration of a task was evaluated for each routine. For example, in the FIR filter, filtering one sample, i.e., performing all 16 multiplications and additions for a 16-tap filter, was considered as one iteration. Fig. 5(b) shows the number of clock cycles for each task across three microcontrollers. According to this graph, the proposed architecture substantially reduces the number of clock cycles in each task. Given a fixed operating frequency for three microcontrollers, the fastest execution time is achieved by the proposed architecture. This reduction in the number of

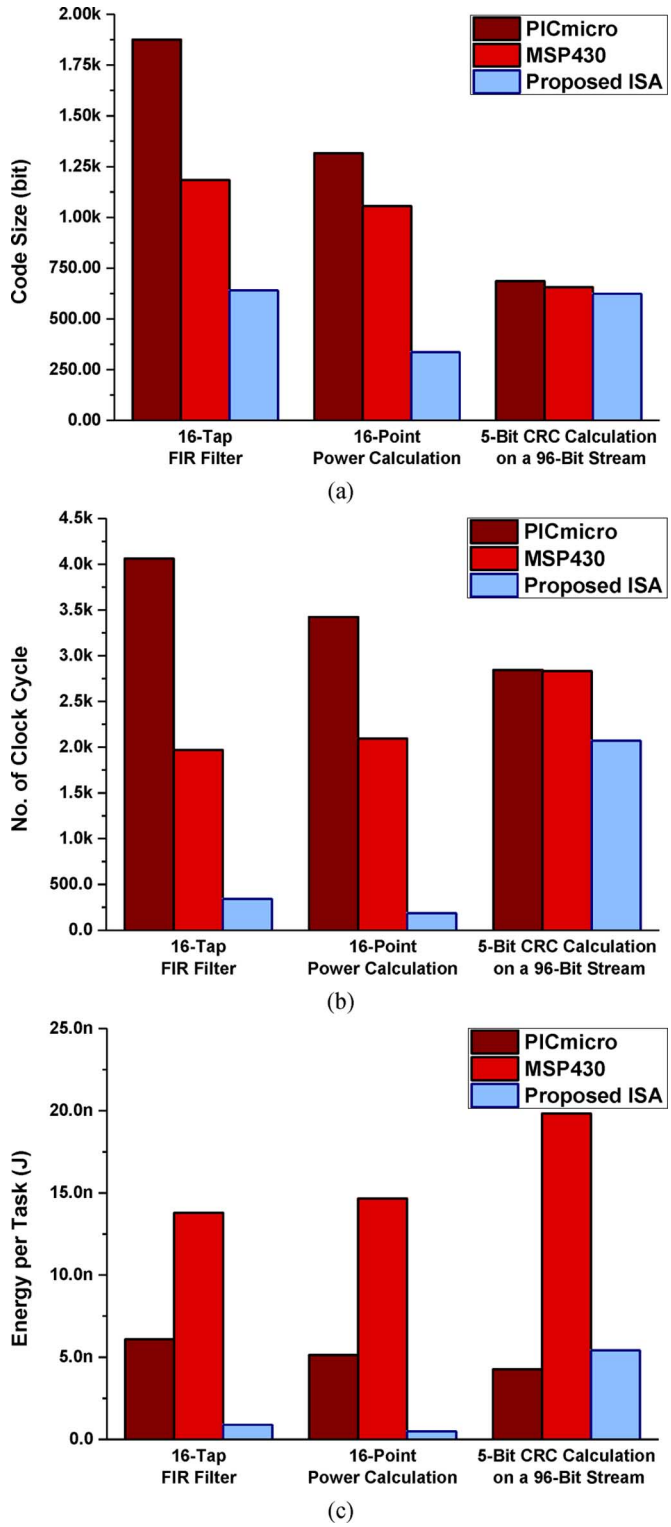

Fig. 5. Comparison of (a) code size, (b) number of clock cycles, and (c) energy per task of three different tasks, implemented using PICmicro, MSP430, and the proposed microcontroller architecture.

clock cycles and code size is due to adding DSP features into the proposed architecture. To better examine the efficiency of the execution of given tasks, the required energy for each task should be compared. This comparison will reveal any overhead due to complicated instructions or addressing modes. Since the proposed microcontroller operates in the sub-threshold regime,

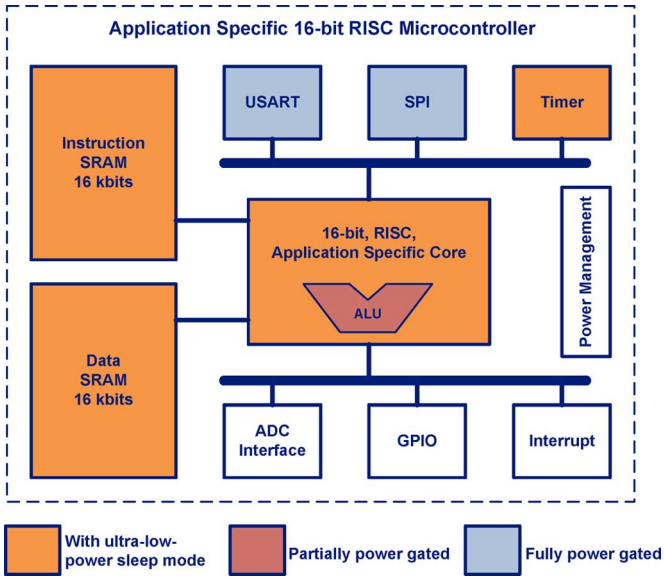

Fig. 6. Block diagram of the proposed application-specific biomedical microcontroller.

for a fair comparison, two sub-threshold implementations of PICmicro [3] and MSP430 [9] were selected. The minimum energy per cycle was used to calculate energy per each task. Fig. 5(c) shows energy consumption during executing each task for three microcontrollers. As can be seen from this graph, while introducing complicated instructions in the proposed architecture helps greatly in reducing clock per task, the instruction set is sufficiently concise to allow very low energy per instruction. As a result, the proposed instruction set architecture allows implementing computationally expensive tasks like filtering and power calculation with 6.8–28 times less energy compared to other microcontroller families. For less computational tasks like CRC calculation, the performance of the proposed microcontroller is comparable to the performance of the minimal 8-bit microcontroller i.e., the added overhead is negligible.

The microcontroller is designed for sub/near-threshold operation to provide the best energy efficiency. To prevent any hold violations in the presence of high variations in the sub-threshold regime, a dual-edge pipelining was implemented in which two consecutive stages are working with two opposite edges of the clock.

Fig. 6 shows the peripheral blocks implemented in the microcontroller. Two 16 kb custom-designed asynchronous SRAMs have been implemented to store code and data information. The memory blocks are capable of working at the sub-threshold regime down to 0.25 V. To have an efficient data transmission via RF link, a universal synchronous/asynchronous serial port (USART) is incorporated to generate serial data with adjustable data rate which is useful in various communication protocols. Other peripherals like timer, general purpose IO, and SPI are also included.

As the power consumption of sensor nodes is of main concern, extensive power and clock gatings are inserted in the microcontroller. First, larger peripherals like USART and SPI are power gated allowing complete shutdown while the system is in the standby mode or they are not being used. The ALU is also

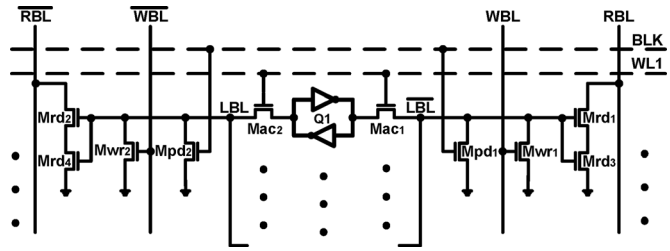

Fig. 7. Architecture of the SRAM block for sub-threshold operation [19].

power gated for lowering power consumption while the microcontroller is idle or just transferring blocks of data. Second, a sleep mode, via a SLEEP command, is designed for the core and memory blocks. Under this mode, the whole core is clock gated and both memories are put into an ultra-low-power mode without losing their data.

C. Sub-Threshold Average-8T SRAM

The power and speed of the code and data memory blocks are very important in the system as their power sets the minimum power level for the digital block and their speed limits the maximum operating frequency and the minimum energy-per-operation. These memory blocks are designed to work at the same voltage as the digital core, i.e., down to 0.25 V, to have the best power performance. To obtain high-speed performance and area efficiency at the sub-threshold regime, a novel low-power average-8T SRAM architecture [19] is proposed, as shown in Fig. 7. In this architecture, local bitlines are decoupled from both read and write global bitlines via read and write decoupling transistors, i.e., M_{rd} and M_{wr}. Capacitances of local bitlines are kept sufficiently low to allow reliable read and write operations at sub-threshold.

Each 16 kb memory block has 32 columns and 512 rows. A sleep mode is incorporated into the SRAM blocks to achieve substantial reduction in the leakage power during the sleep mode of the system while maintaining their data. In this mode all local and global bitlines are placed in the high impedance mode.

D. RF Transceiver

The transceiver is designed at MICS band which has lower body absorption rate and allows for low-power implementation [20], [21]. The communication for the ECG sensor is asymmetric in terms of data-rates. BFSK modulation with data-rate up to 150 kbps is chosen for the uplink communication and OOK modulation with data-rate of 50 kbps is used for the downlink. The maximum data-rate of 150 kbps is to ensure the channel bandwidth is smaller than 300 kHz required by the MICS band communications [20], [21]. At the sensor node, it is essential to reduce the power consumption. So FSK modulation is selected due to its constant envelope that allows for high efficient nonlinear PA and simplifies the circuit implementation via directly modulating the oscillator [20]. OOK signals can be demodulated through envelope detection, which helps to reduce the power consumption of the receiver. The transceiver works in half duplex mode, avoiding the transmitter leakage problem.

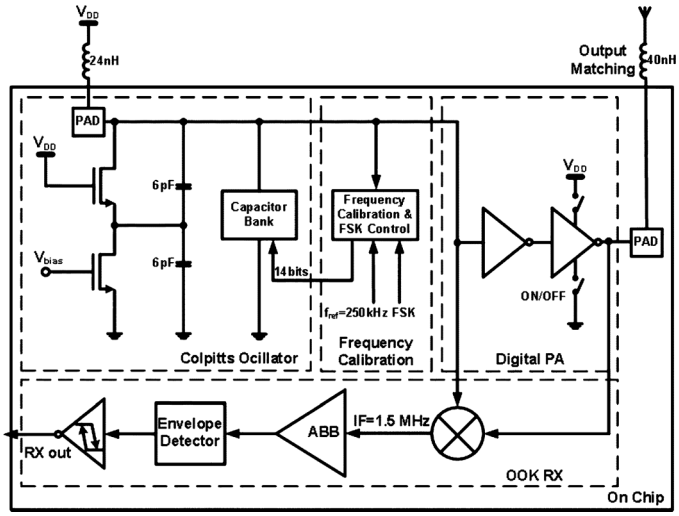

Fig. 8. Block diagram of the RF Transceiver.

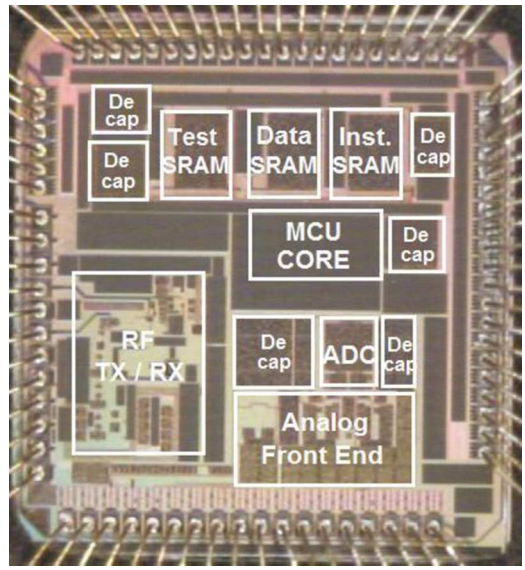

Fig. 9. Die photo of the fabricated ECG platform.

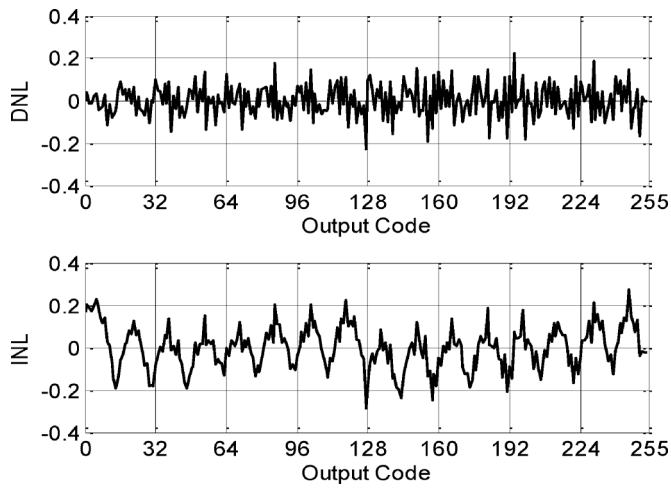

Fig. 10. Measured DNL and INL of the ADC.

The transceiver block diagram is shown in Fig. 8. A single-ended Colpitts oscillator is used to generate the local oscillation (LO) signal. To implement the LC-tank of the oscillator, a low-cost off-chip inductor of 24 nH is used to save the silicon area and the capacitor is integrated on-chip. The frequency control is realized through a 14-bit digitally switched capacitor bank with a fine tuning step of 5 kHz. The LO frequency is divided by 4 and then drives the frequency calibration block. The frequency calibration is implemented by simple counters and SAR logic. The reference clock for frequency calibration is 250 kHz. After generating the desired frequency control bits, BFSK is realized by directly changing the frequency control bits of the oscillator. In this design, the frequency deviation for BFSK modulation is 50 kHz. Simple inverters are used as digital PA. The PA can be turned off during the receiver mode. An off-chip inductor of 40 nH is used for impedance matching.

The OOK receiver is based on envelope detection. The received OOK signal is firstly down-converted to an intermediate frequency (IF) of 1.5 MHz. The LO signal is generated by the same oscillator used in the transmitter. The analog baseband of the receiver reduces the noise bandwidth through band-pass filtering centered at the IF frequency, and it also provides a gain of about 40 dB. The final bit stream is generated by an envelope detector followed by a Schmitt trigger.

IV. Chip Implementation and Measurement Results

A prototype of the proposed wireless ECG SoC has been fabricated in a standard 0.13-μm bulk CMOS process. Fig. 9 shows the die photo and floorplan of the chip. The total area of the chip is 2.4 mm $\times$ 2.5 mm, which is pad-limited.

A. Sensor Front-End

The system gain is tunable from 36 dB to 44 dB with low-pass cut-off at about 64 Hz. The low-frequency high-pass corner is less than 0.1 Hz, thanks to the thick-oxide pseudo-resistor configuration. The input-referred noise, integrated from 0.5 Hz to 250 Hz, is 6.9 $\mu\mathrm{V_{rms}}$. The Front-end power-supply rejection ratio (PSRR) is 70 dB, and the common-mode rejection ratio (CMRR) is 59 dB. Both are measured without enabling DRL. The front-end functions correctly under 0.45 V to 1.0 V power supply. The power consumption under 0.7 V supply is 0.45 μW for each ECG channel.

The ADC is characterized at 1-kHz sampling rate. The measured ADC DNL and INL with respect to the output code are shown in Fig. 10. The measured DNL is in the range of $-0.23/+0.22$ LSB, while the measured INL is in the range of $-0.29/+0.27$ LSB. Fig. 11 shows the measured 8192-point ADC output PSD with a rail-to-rail 16-Hz sinusoidal input. The measured SNDR and SFDR are 45.63 dB and 53.83 dB, respectively. The calculated effective number of bits (ENOB) is 7.29 bits.

B. Digital Back-End

The microcontroller and memories are fully functional down to 0.25 V supply voltage on average and 0.22 V in the best case as illustrated in the distribution of the minimum operating voltage in Fig. 12. In the current version of the system, a programmer writes the code into the code memory of the system

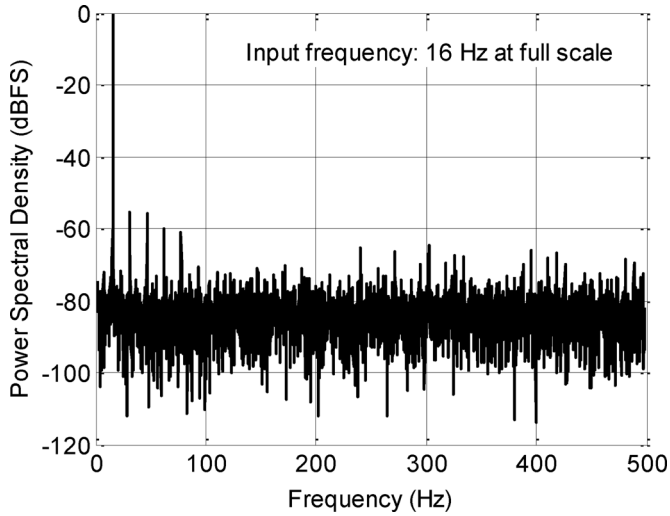

Fig. 11. Measured output PSD of the ADC with 16-Hz sinusoidal input.

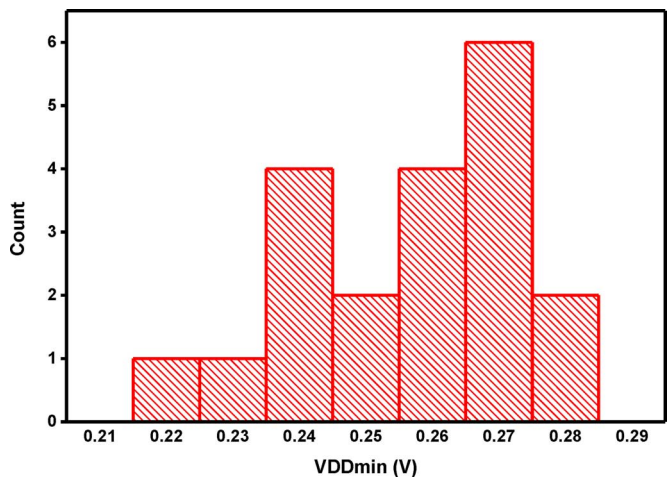

Fig. 12. The distribution of the minimum operating supply voltage for 20 chips.

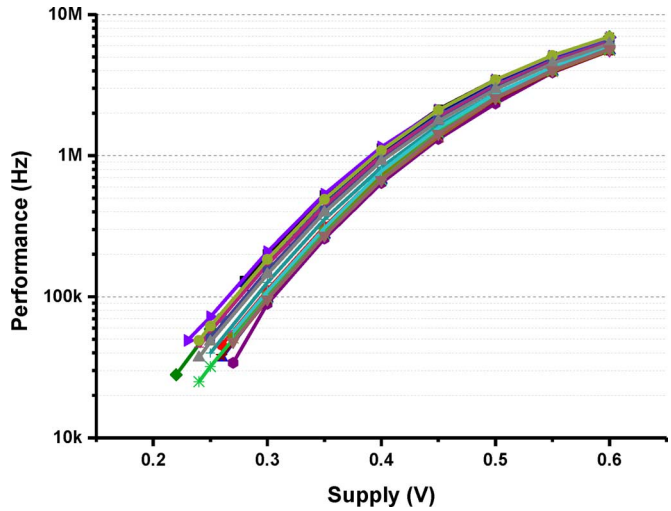

Fig. 13. Performance of the digital back-end across various supply voltages, measured for 20 chips.

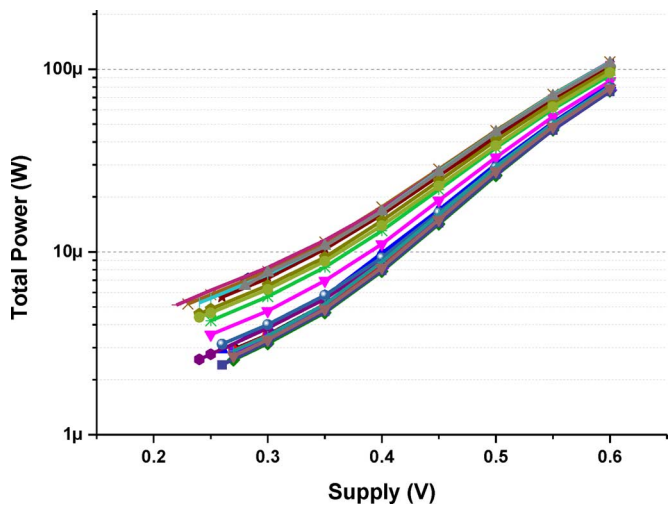

Fig. 14. Total power consumption of the digital back-end at full speed across various supply voltages, measured for 20 chips.

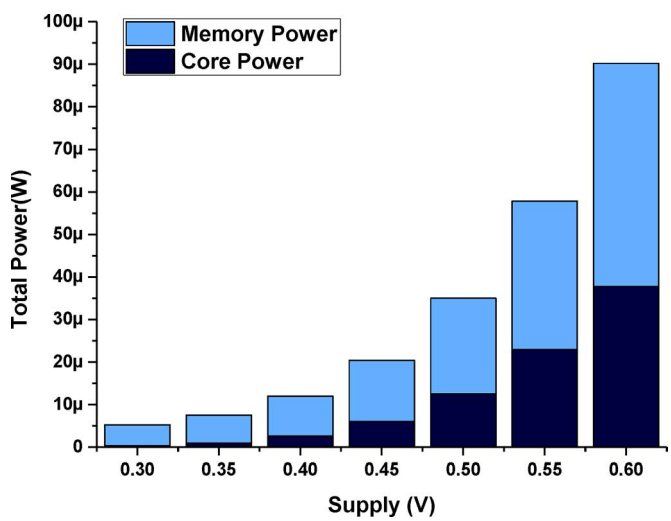

Fig. 15. The breakdown of the total power consumption in terms of memory and core power consumption across various supply voltages.

via a parallel port at the first power-up. The average of the minimum supply voltage is 0.256 V with 17 mV standard deviation. All chips are fully functional at 0.28 V. Fig. 13 shows the maximum operating frequency of the microcontroller at various supply voltages for 20 chips. As can be seen, the microcontroller is working from 52 kHz at 0.25 V to 6.1 MHz at 0.6 V. At the full speed, it consumes from 4.5 μW at 0.25 V to 90.2 μW at 0.6 V as shown in Fig. 14. These power consumption values include the instruction and data SRAM power. The contributions of the SRAM and microcontroller core to the total power are depicted in Fig. 15. At higher supply voltages, like 0.6 V, around 60% of the total power is consumed by the SRAM blocks while at voltages below threshold, like 0.3 V, almost all power is consumed by the leakage power of the SRAM while the core power is negligible. This phenomenon would be worst in more advanced technologies in which their leakage current is much higher. This graph clearly shows the importance of designing ultra-low-power low-leakage SRAM in power-sensitive applications.

The leakage power of the digital back-end and its variation is depicted in Fig. 16. As expected, high variations in the

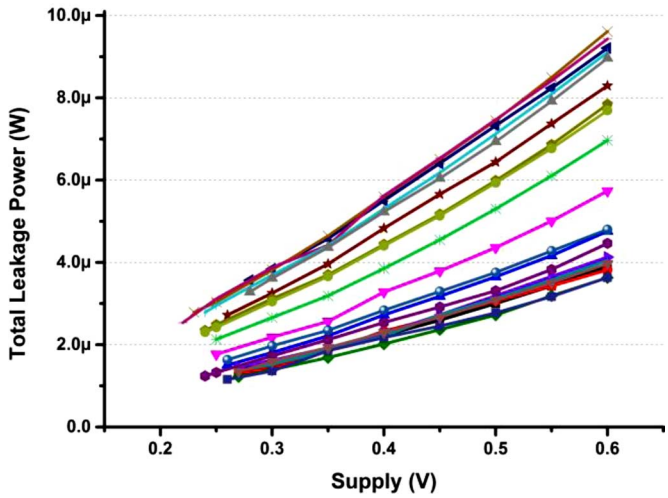

Fig. 16. Total leakage power of the digital back-end across various supply voltages, measured for 20 chips.

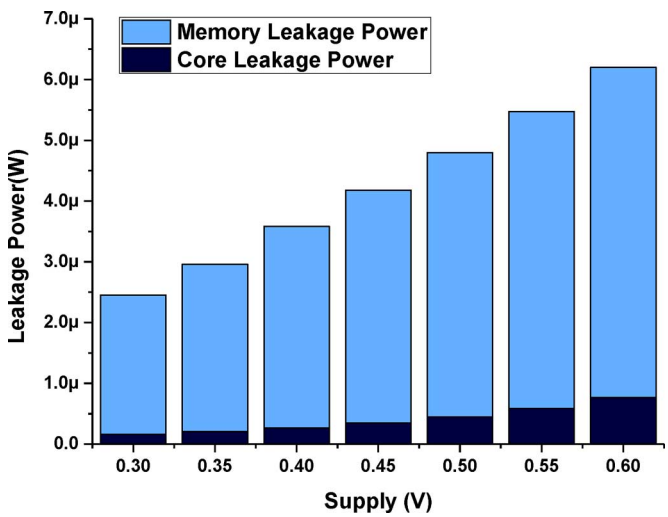

Fig. 17. The breakdown of the total leakage power in terms of memory and core leakage power across various supply voltages.

sub-/near-threshold regime causes around 3x variation in the leakage power. In terms of leakage breakdown, most of the leakage power is consumed by the SRAM blocks as shown in Fig. 17.

Fig. 18 shows the average energy-per-instruction for the microcontroller core. At the minimum-energy point, the microcontroller consumes only 2.62 pJ per instruction on average. As predicted, this point is located near-threshold, i.e., 0.35 V. Considering the 16-bit core and complicated instructions like multiply and multiply-accumulate, this core shows interesting energy consumption per instruction. Table II summarizes the specifications and performance of the digital back-end of the fabricated SoC and compares it with recent state-of-the-art works. It should be noted that the values in this table are the average performance of 20 chips. This work achieves the lowest operating voltage and the fastest performance while gives promising average energy-per-instruction.

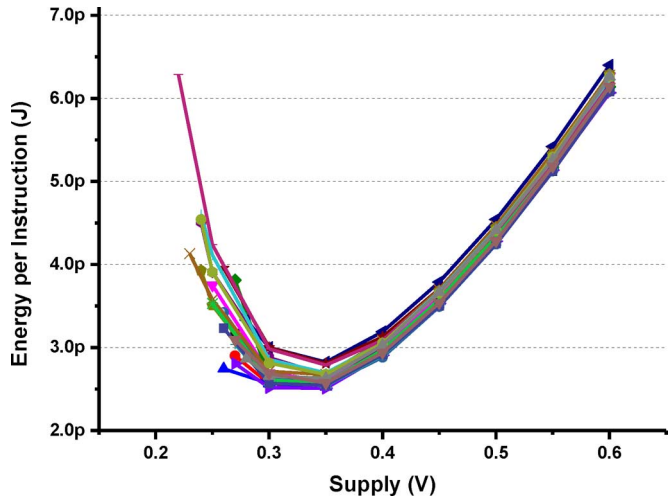

Fig. 18. Average energy-per-instruction of the microcontroller core across various supply voltages, measured for 20 chips.

TABLE II
SPECIFICATIONS AND PERFORMANCE SUMMARY AND COMPARISON OF THE DIGITAL CORE

	[4]	[5]	[9]	This work
Technology	0.18 µm	0.13 µm	65 nm	0.13 µm
Min Supply	1.2 V	0.3 V	0.3 V	0.25 V
Memory size	5 kB + 4 kB + 32 kB	5.5 kB	128 kb	16 kb + 16 kb
Microcontroller Architecture	32-bit, SIMD, Cus-tom-designed	8-bit, RISC, PIC micro	16-bit, RISC, MSP430	16-bit, RISC, Custom-designed
Energy/Inst.	N.A.	1.5 pJ @ 0.5 V	~7 pJ @ 0.5 V	2.62 pJ @ 0.35 V
Operating Frequency	1 MHz @ 1.2 V	2 kHz @ 0.3 V 1.7 MHz @ 0.6 V	8.7 kHz @ 0.3 V 1 MHz @ 0.6 V	52 kHz @ 0.25 V 6.1 MHz @ 0.6 V
Total Power consumption (Core + SRAM)	~12 µW	2.1 µW	~11.8 µW @ 0.5 V	4.5 µW @ 0.25 V 90.2 µW @ 0.6 V
Leakage power (Core + SRAM)	N.A.	N.A.	1 µW @ 0.3 V	2.3 µW @ 0.25 V 6.2 µW @ 0.6 V

C. RF Transceiver

The measured minimum supply voltage of the RF transceiver is 0.53 V, which is slightly higher than 0.5 V in the simulation. This is because the minimum supply voltage of the frequency divider is 0.53 V. The FSK transmitter consumes 1.14 mA current while delivering −18 dBm output power. The OOK receiver consumes 1.07 mA current while achieving a sensitivity of −63 dBm at 50 kbps data-rate which is sufficient for short-distance communications within 1–2 m. The oscillator dominates the power consumption of the transceiver. Under 0.5-V supply voltage, the simulated current consumption of the oscillator is about 800 μA. The PA draws 200 μA while delivering −16 dBm output power. The measured FSK output spectrum while sending a pseudo-random sequence at 150 kbps data-rate is shown in Fig. 19. It can be seen that the occupied 20 dB bandwidth is less than 300 kHz, which satisfies the MICS channel bandwidth. The OOK receiver excluding the oscillator consumes 120 μA. The auxiliary biasing circuitry draws about 20 μA.

D. Overall System

Fig. 20 shows a real 3-lead ECG signal recording on a volunteer and compares it with a measurement from a commercial de-

Fig. 19. BFSK spectrum of the transmitter while sending a pseudo-random sequence at 150 kbps.

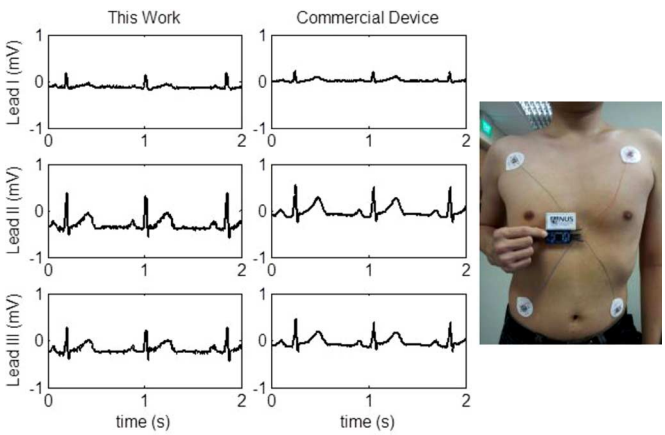

Fig. 20. Real 3-Lead ECG recording with no post-processing compared with a measurement from a commercial device.

vice. In this recording, Leads I and III were recorded while Lead II was derived accordingly. For the best energy efficiency, each block was working at its minimum supply voltage which can give the required performance. Therefore the digital back-end was working at 0.4 V and around 1 MHz, analog front-end and RF transceiver was working at 0.53 V and ADC was working at 0.7 V. The result shows good recording quality. During the recording, the whole system consumes 74.8 μW in the raw data transmission mode in which the data is stored in the on-chip memory for 2 seconds (500 Hz sampling rate for both channels) and sent at the maximum bit-rate in a burst mode which gives less than 10% duty cycle for the RF transmission. In this mode, more than 80% of the power is consumed by the RF transceiver and around 18% is consumed by the digital back-end. In the heart rate detection mode, the amount of transmitted data is much less than the raw data transmission mode. By transmitting heart rate information in every 5 seconds, this mode allows 0.5% duty cycling of the RF transmission which leads to 17.4 μW power consumption of the system. In this mode 77% of the power is consumed by the digital back-end and only around 17% is consumed by the RF transceiver. Table III summarizes specifications of the fabricated wireless ECG SoC and compares it with recent state-of-the-art works.

TABLE III
SYSTEM-LEVEL SPECIFICATIONS AND COMPARISON

	[4]	[5]	This work
Technology	0.18 μm	0.13 μm	0.13 μm
Area	5 mm × 4.7 mm	N.A.	2.4 mm × 2.5 mm
ECG Channels	3	4	2 (3 Leads)
Driven-Right-Leg	No	No	Yes
RF Transmitter	No	Yes	Yes
RF Receiver	No	No	Yes
Supply Voltages	1.2 V	0.3, 0.5, 1, 1.2 V (Harvesting)	Single: 0.7 V Multiple: 0.25, 0.5, 0.7 V
Total Power (Raw Data)	38 μW (No RF)	397 μW	74.8 μW
Total Power (Heart Rate)	31.1 μW (No RF)	19 μW	17.4 μW

V. CONCLUSION

We have presented a 0.7-V 3-lead wireless ECG SoC for wireless body sensor network applications. The fully integrated ECG chip consumes only 17.4 μW when transmitting heart rate information to a gateway. The ultra-low power is achieved through low supply voltage, the introduction of a low power sub-threshold SRAM, a power efficient microcontroller, and an asymmetrical RF transceiver.

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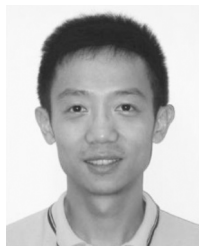
Mahmood Khayatzadeh (S'09) received the B.S. and M.S. degrees in electrical engineering and electronics from the Amirkabir University of Technology, Tehran, Iran, in 2000 and 2002, respectively.

In 2000, he joined the Emad Semiconductor Company, Tehran, Iran. From 2006 to 2008, he was with the KavoshCom R&D Group, Tehran, Iran, working on the UHF RFID reader. In 2008, he was with Delphi Automotive Systems, Singapore Design Engineering Center, Singapore. Since 2009, he has been with the National University of Singapore, working toward the Ph.D. degree. His research focuses on ultra-low-power and low-voltage VLSI circuits and systems.

Xiaoyang Zhang (S'09) received the B.Sc. degree in microelectronics from Peking University, Beijing, China, in 2009.

Currently, he is working toward the Ph.D. degree in electrical engineering at the National University of Singapore. His research interests include low-power biomedical sensors and wearable computing.



Jun Tan (S'07–M'12) received the B.Sc. and M.Sc. degrees in electrical engineering from Fudan University, Shanghai, China, in 2001 and 2004, respectively, and the Ph.D. degree from the National University of Singapore in 2012.

He was with Intel Products, Shanghai, China, in 2004. He worked at Agilent Technology, Shanghai, China, from 2005 to 2006. He has been with the National University of Singapore since 2006. His research interests include analog and RF circuit design for low-power wireless communications.

Wen-Sin Liew (S'08–M'13) received the B.Eng. and Ph.D. degrees in electrical engineering from the National University of Singapore (NUS) in 2007 and 2013, respectively.

Currently, he is a Research Fellow with the Bioelectronics Laboratory, NUS. His research interests include analog-to-digital converters, mixed-signal circuits, and biomedical sensor interfaces.

Mr. Liew was the winner of 2010 DAC/ISSCC Student Design Contest Award.

Yong Lian (M'90–SM'99–F'09) received the B.Sc. degree from the College of Economics and Management, Shanghai Jiao Tong University, Shanghai, China, in 1984, and the Ph.D. degree from the Department of Electrical Engineering, National University of Singapore, Singapore, in 1994.

He worked in industry for nine years and joined the National University of Singapore in 1996, where he is the Provost's Chair Professor with the Department of Electrical and Computer Engineering. He teaches VLSI diigital circuit design, integrated digital design, and emerging technologies in electrical engineering. He is the author or coauthor of more than 190 scientific publications in peer-reviewed journals and conference proceedings. His current research interests include biomedical circuits and systems and signal processing. He is the Founder of ClearBridge VitalSigns Pte. Ltd., a startup for wireless wearable biomedical devices.

Dr. Lian was a recipient of the 1996 IEEE CAS Society's Guillemin–Cauer Award for the best paper published in the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II, the 2008 Multimedia Communications Best Paper Award from the IEEE Communications Society for the paper published in the IEEE TRANSACTIONS ON MULTIMEDIA, winner of the 47th DAC/ISSCC Student Design Contest (as a Ph.D. Advisor), the Best Student Paper Award in the ICME in 2007 (as a M.Eng. Advisor), and the 2011 IES Prestigious Engineering Achievement Award. For his teaching, he received the University Annual Teaching Excellent Award in 2009 and 2010, respectively. He is the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS, a Vice President for Publications of the IEEE Circuits and Systems Society, Steering Committee Member of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, the Past Chair of DSP Technical Committee of the IEEE Circuits and Systems (CAS) Society. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS, IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and *Journal of Circuits Systems Signal Processing* in the past 10 years, and was the Guest Editor for seven special issues in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and *Journal of Circuits, Systems and Signal Processing*. He was the Vice President of the Asia Pacific Region of the IEEE CAS Society from 2007 to 2008, AdComm Member of the IEEE Biometrics Council from 2008 to 2009, CAS Society Representative to the BioTechnology Council from 2007 to 2009, Chair of the BioCAS Technical Committee of the IEEE CAS Society from 2007 to 2009, Member of the IEEE Medal for Innovations in Healthcare Technology Committee from 2010 to 2012, and a Distinguished Lecturer of the IEEE CAS Society from 2004 to 2005. He is the Founder of the International Conference on Green Circuits and Systems, the Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, and the IEEE Biomedical Circuits and Systems Conference. He is a Fellow of the Academy of Engineering Singapore.