# SDRdrum

## Arty Shield

| File Name | Page | Description |
|---|---|---|
| **Title.SchDoc** | 1 | Fancy title sheet |
| **Inputs.SchDoc** | 2 | Input amplification and filtering |
| **Outputs.SchDoc** | 3 | Output amplification and filtering |
| **ADCs.SchDoc** | 4 | ADCs |
| **DACs.SchDoc** | 5 | DACs and current-to-voltage converters |
| **Power.SchDoc** | 6 | Power supplies |
| **Connectors and Mechanical.SchDoc** | 7 | Arty FPGA board connector and mechanical components |

| Revision | Date | Remarks |
|---|---|---|
| A | 2017-01-08 | Initial revision |
| B | 2018-03-20 | Fix input gain adjustment, add output reconstruction filter, switch to BNCs |

| **Title Page** | |
|---|---|
| **SDRdrum Arty Shield** | Revision: B |
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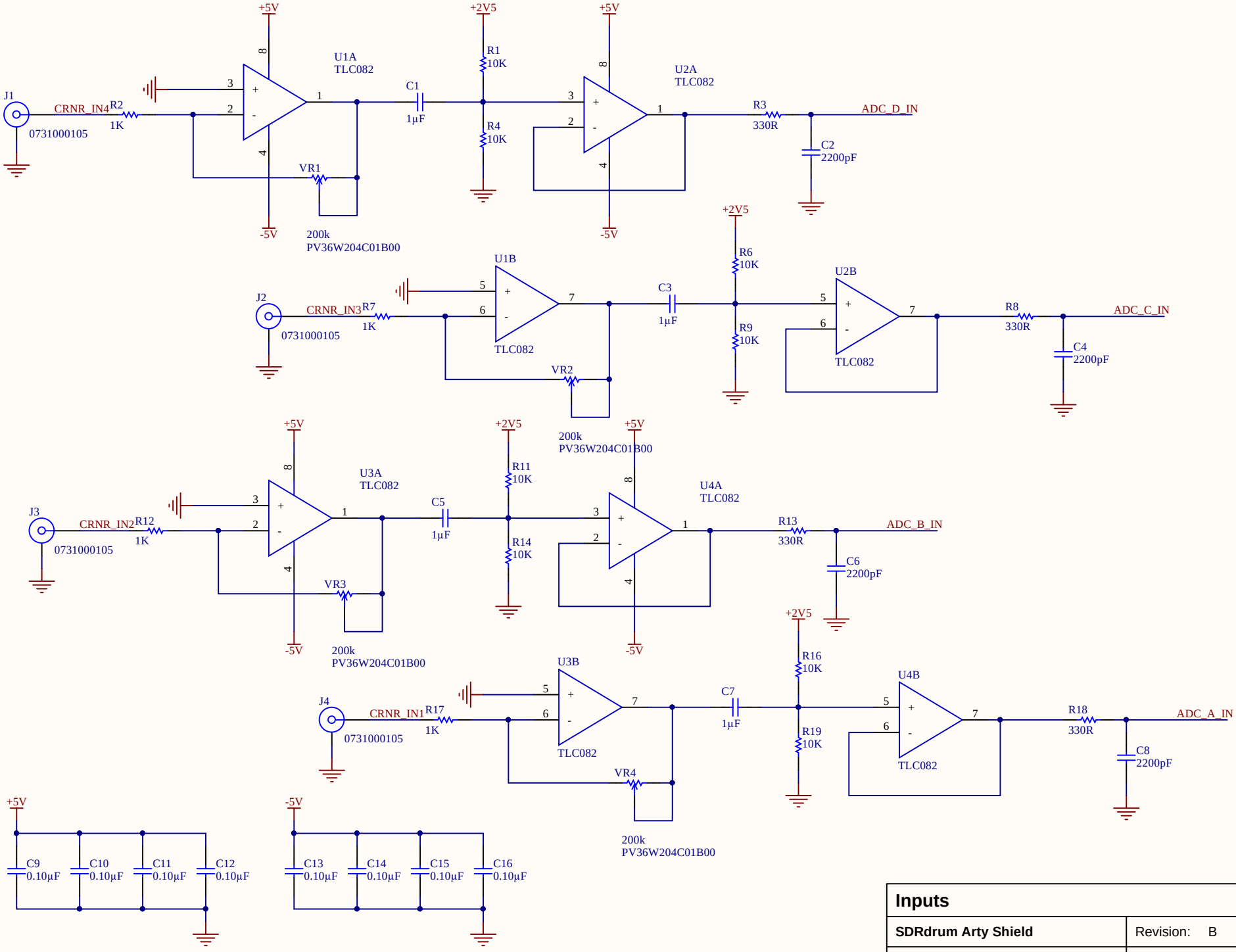
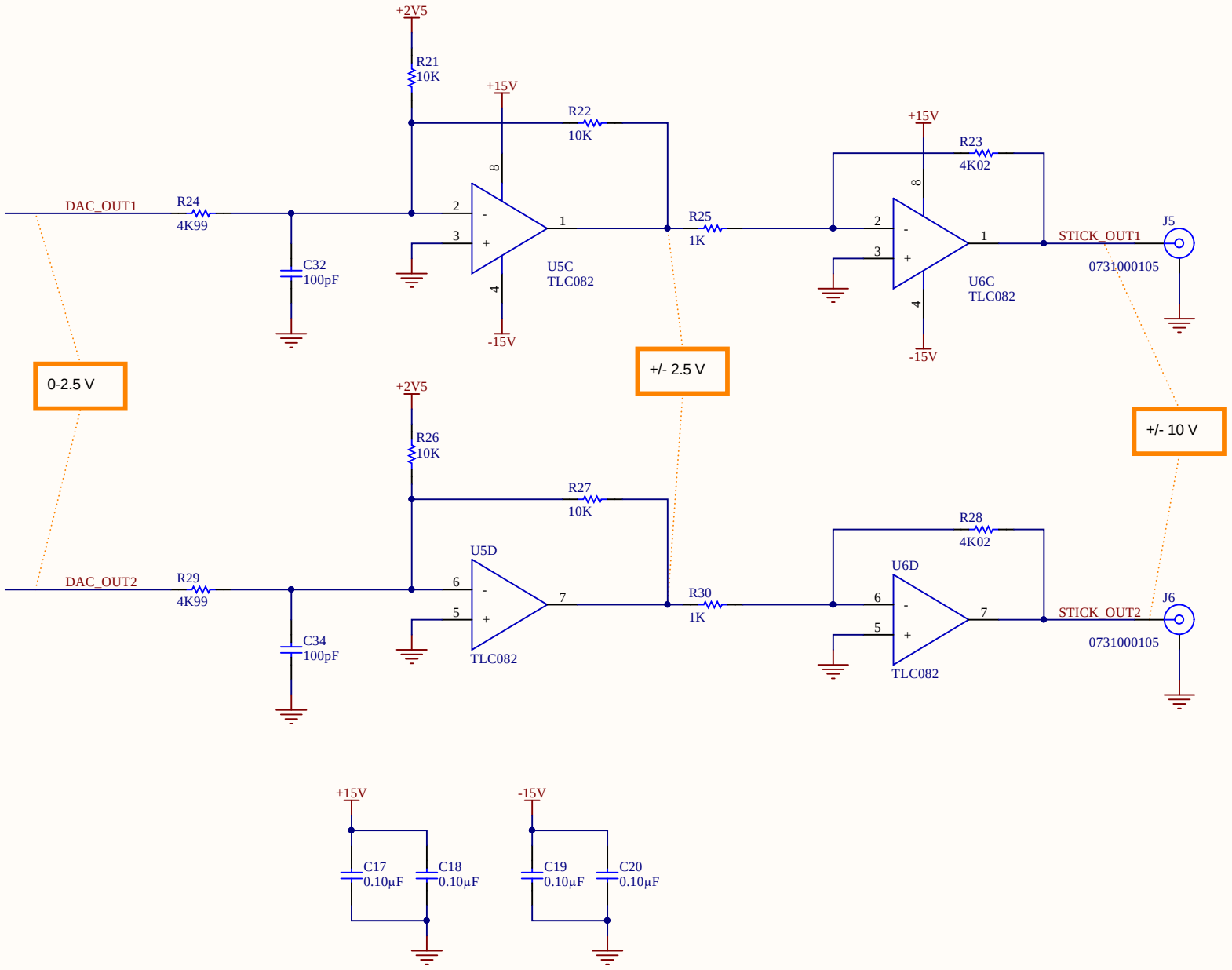



| Inputs | |
|---|---|
| **SDRdrum Arty Shield** | Revision: B |
| Date: 2019-Jan-27 | Sheet: 2 / 7 |




| Outputs | |
|---|---|
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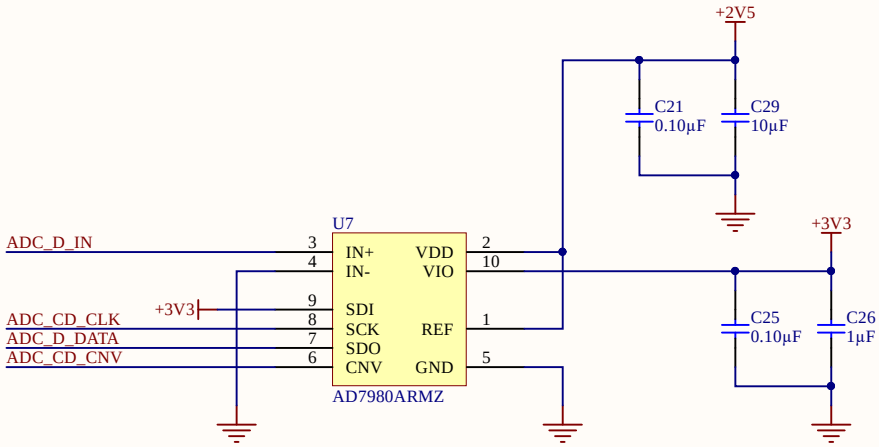
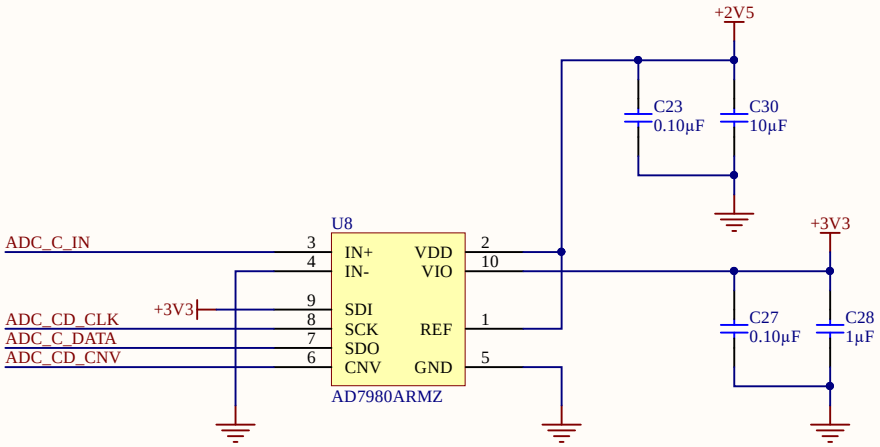
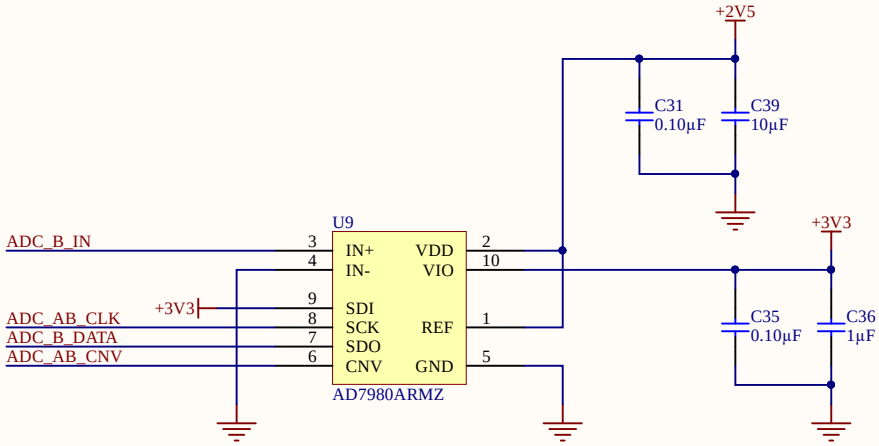
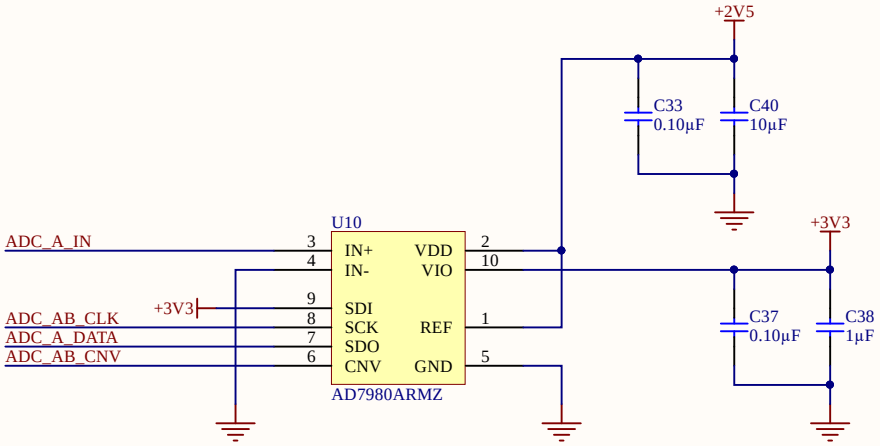
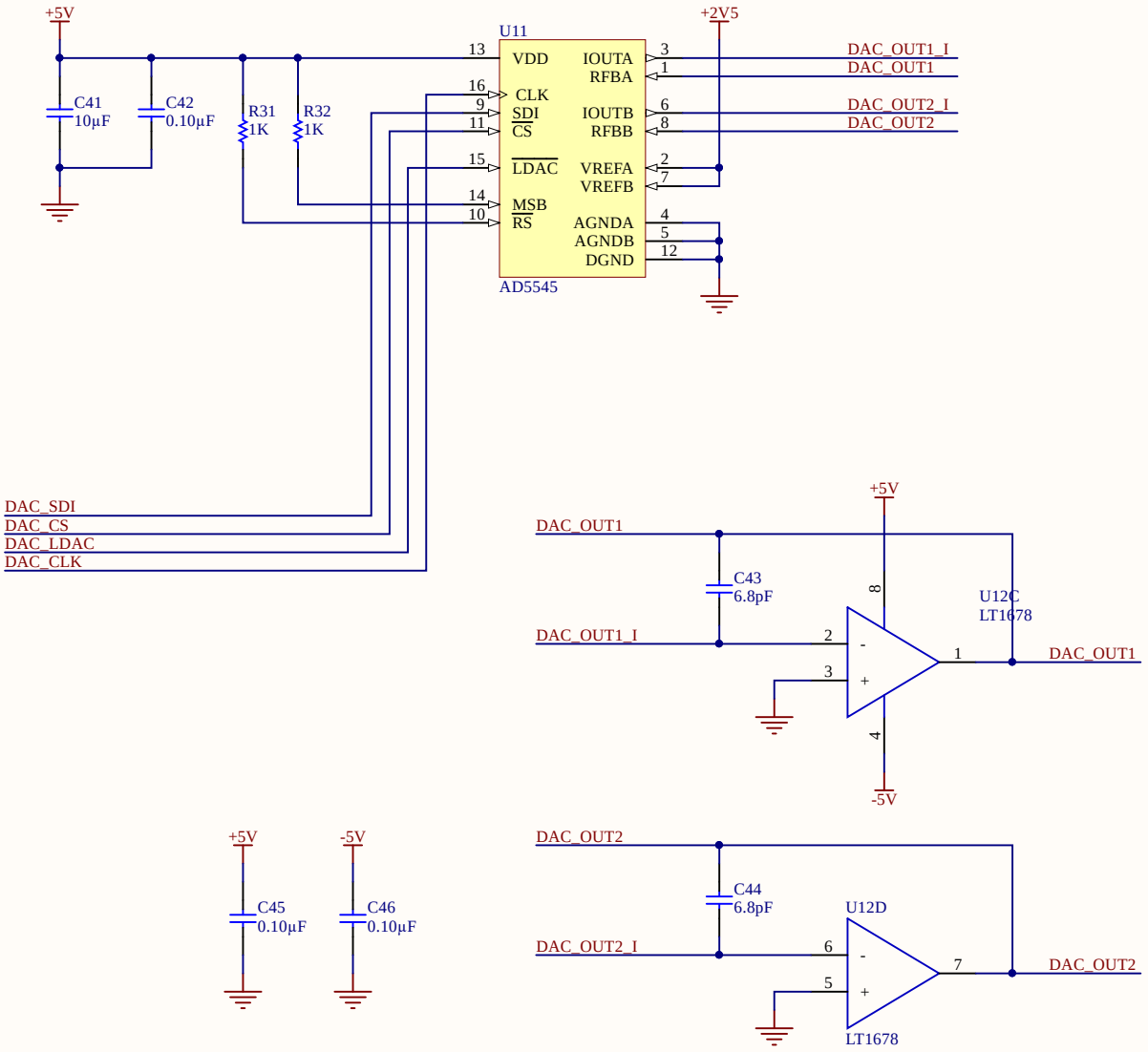



| ADCs | |
|---|---|
| **SDRdrum Arty Shield** | Revision: B |
| Date: 2019-Jan-27 | Sheet: 4 / 7 |




| DACs | |
|---|---|
| **SDRdrum Arty Shield** | Revision: B |
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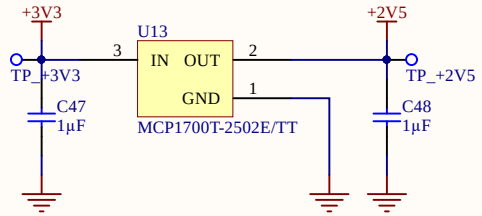
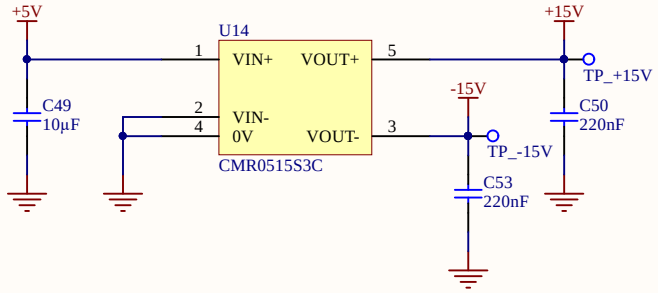
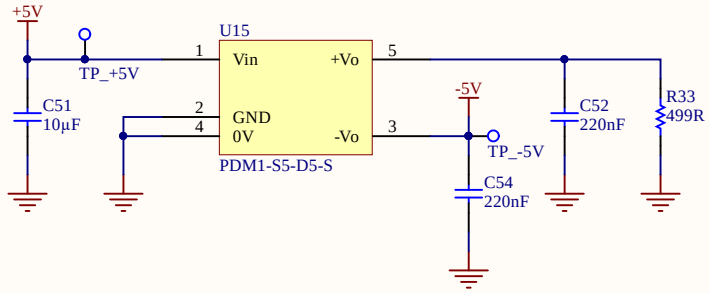



DESIGN NOTE:
PDM1-S5-D5-S requires a minimum load of 10 mA per channel. R? provides this minimum load on the unused 5 V output.




| Power Supplies | |
|---|---|
| **SDRdrum Arty Shield** | Revision: B |
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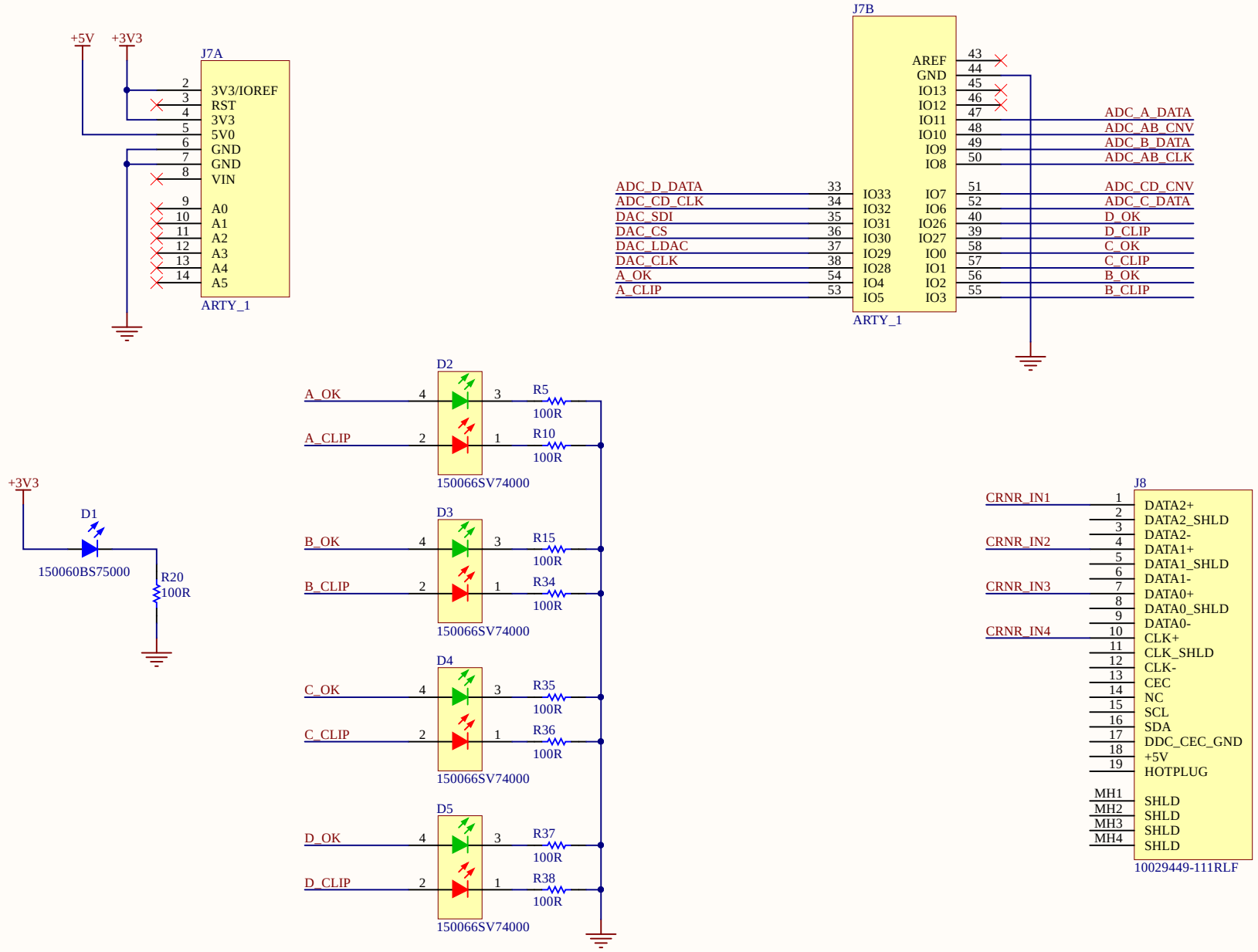


| Connectors and Mechanical | |
|---|---|
| **SDRdrum Arty Shield** | Revision: B |
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