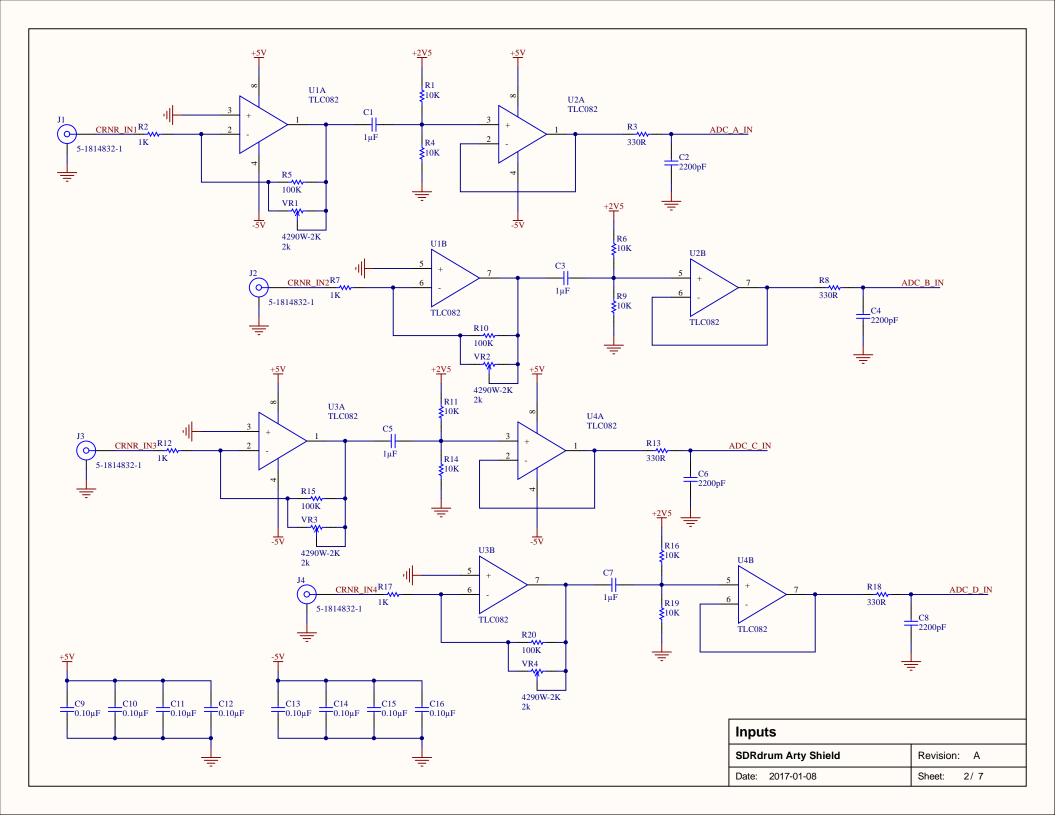
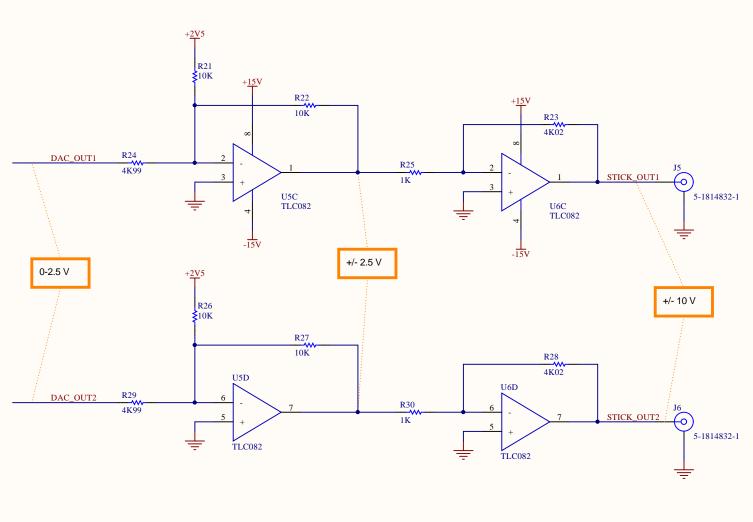
## SDRdrum Arty Shield

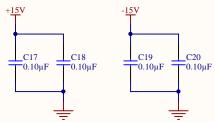
File Name	Page	Description
Title.SchDoc	4	Consultitle cheet
Title.SchDoc	ı	Fancy title sheet
Inputs.SchDoc	2	Input amplification and filtering
Outputs.SchDoc	3	Output amplification and filtering
ADCs.SchDoc	4	ADCs
DACs.SchDoc	5	DACs and current-to-voltage converters
Power.SchDoc	6	Power supplies
Connectors and Mechanical.SchDoc	7	Arty FPGA board connector and mechanical components

Revision	Date	Remarks
А	2017-01-08	Initial revision

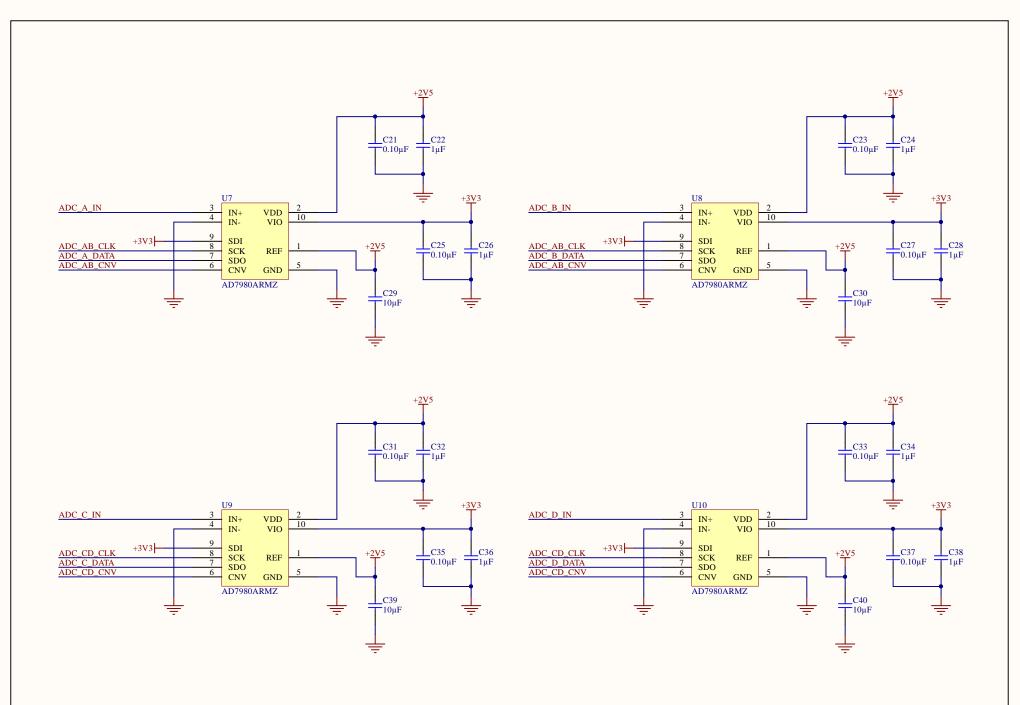
Title Page		
SDRdrum Arty Shield	Revision: A	
Date: 2017-01-08	Sheet: 1/7	



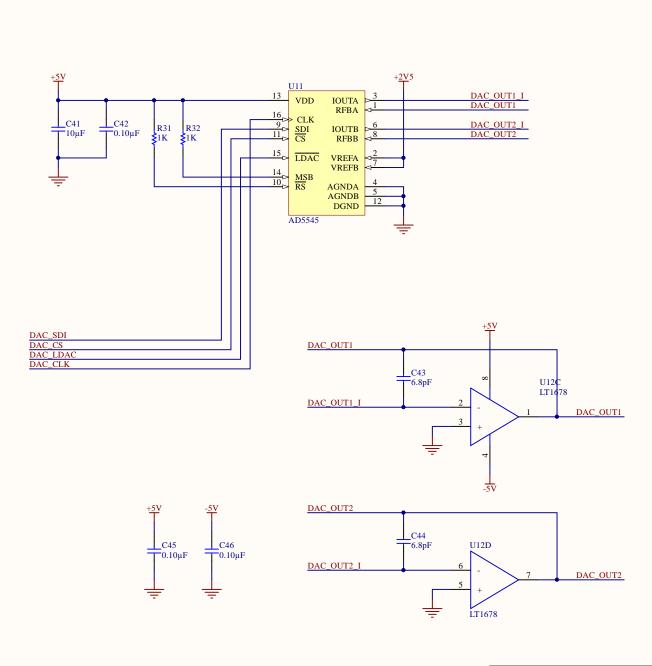




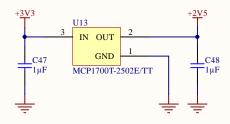
Outputs		
SDRdrum Arty Shield	Revision: A	
Date: 2017-01-08	Sheet: 3/7	



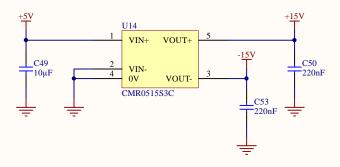
ADCs	
SDRdrum Arty Shield	Revision: A
Date: 2017-01-08	Sheet: 4/7

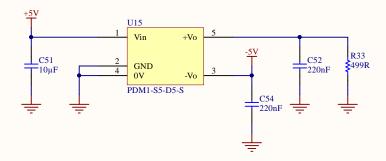


DACs		
SDRdrum Arty Shield	Revision: A	
Date: 2016-07-01	Sheet: 5/7	

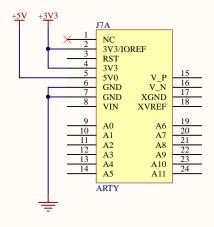


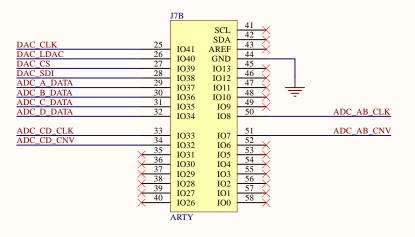
DESIGN NOTE:
PDM1-S5-D5-S requires a minimum load of 10 mA per
channel. R? provides this minimum load on the unused
5 V output.





Power Supplies		
SDRdrum Arty Shield	Revision: A	
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Connectors and Mechanical	
SDRdrum Arty Shield	Revision: A
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