

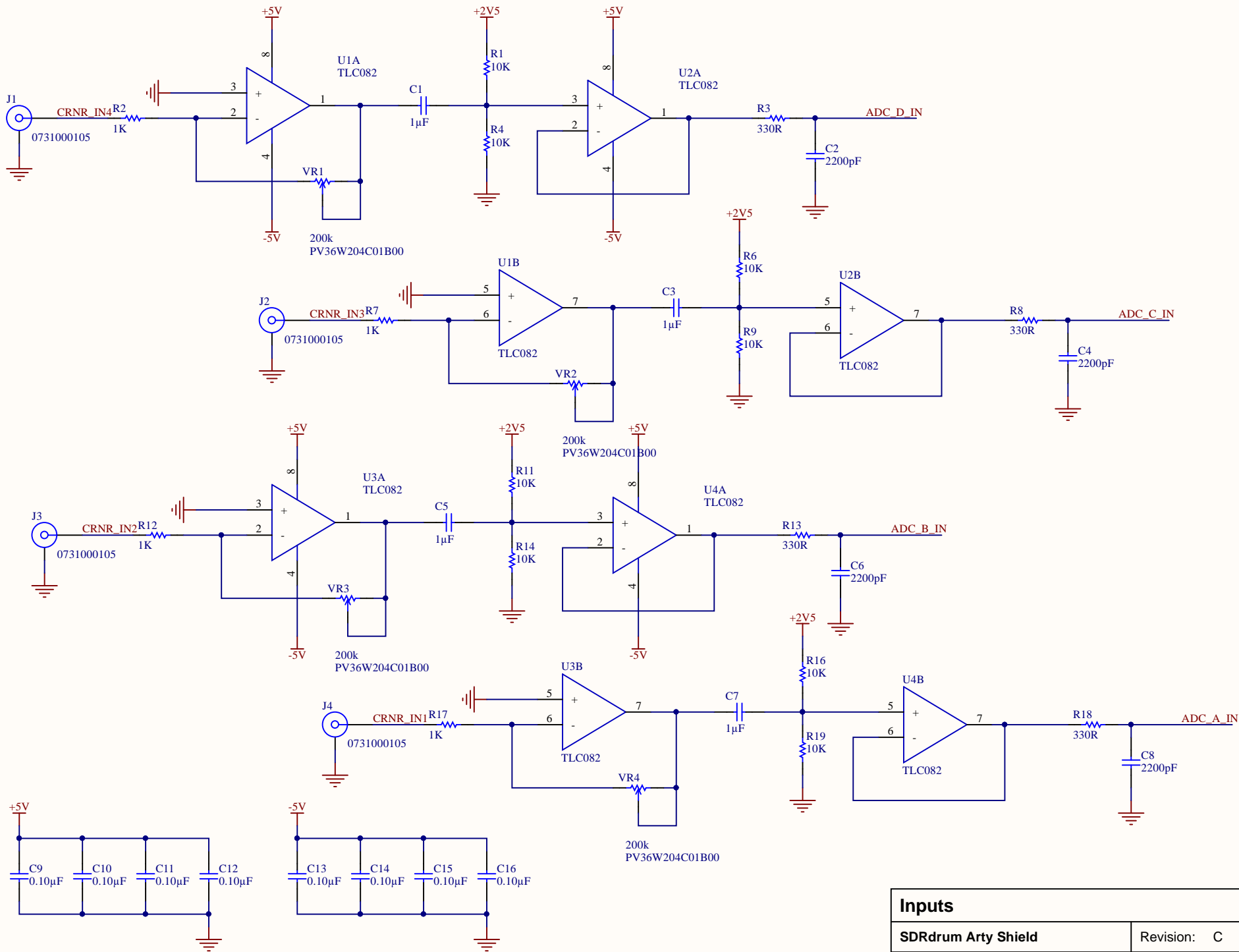
SDRdrum

Arty Shield - Rev C

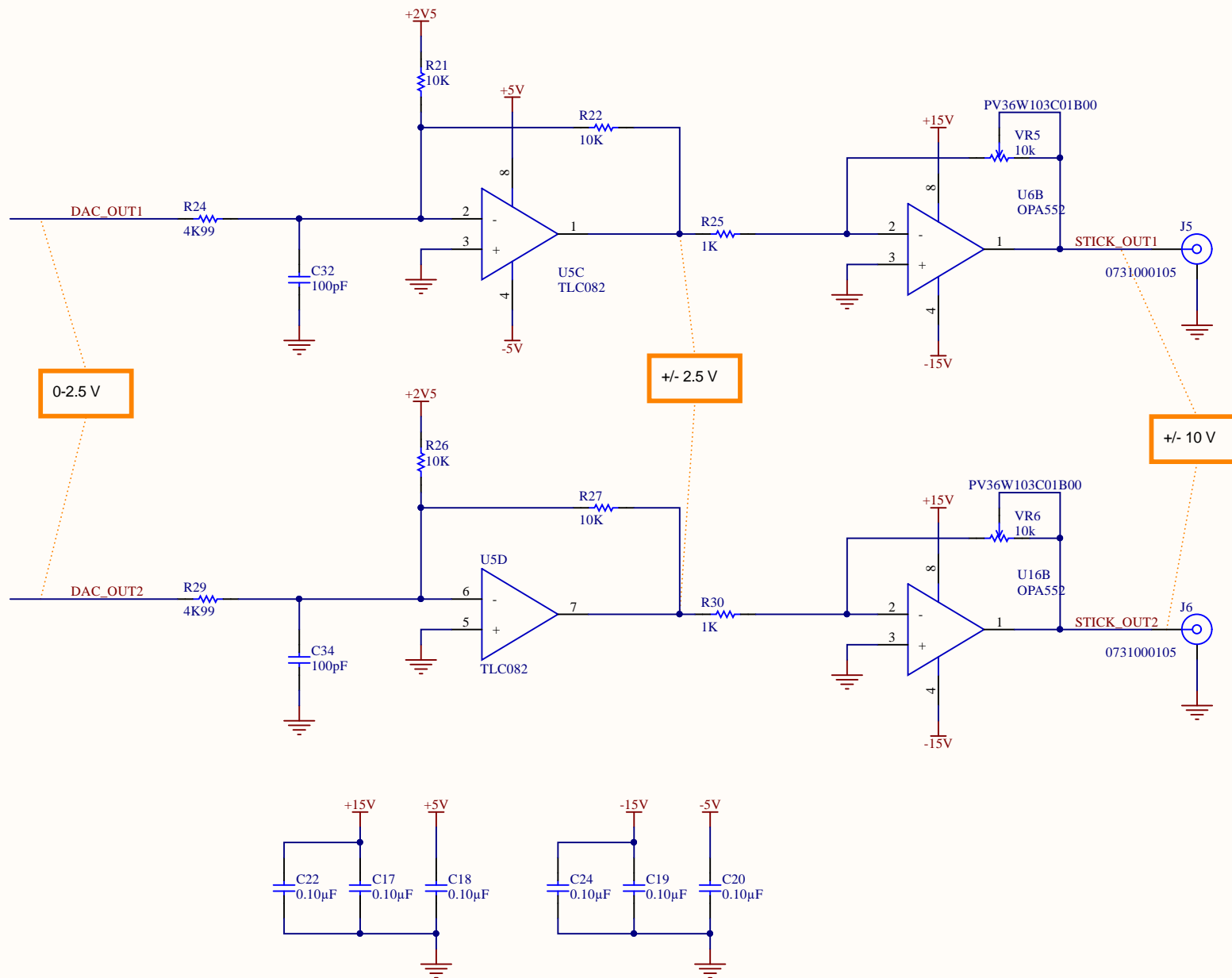
File Name	Page	Description
Title.SchDoc	1	Fancy title sheet
Inputs.SchDoc	2	Input amplification and filtering
Outputs.SchDoc	3	Output amplification and filtering
ADCs.SchDoc	4	ADCs
DACs.SchDoc	5	DACs and current-to-voltage converters
Power.SchDoc	6	Power supplies
Connectors and Mechanical.SchDoc	7	Arty FPGA board connector and mechanical components

Revision	Date	Remarks
A	2017-01-08	Initial revision
B	2019-07-18	Fixed input gain adjustment, added DAC reconstruction filter capacitors, fixed PCB bugs
C	2019-01-29	Switch to BNC and HDMI connectors, add status LEDs, redo PCB layout

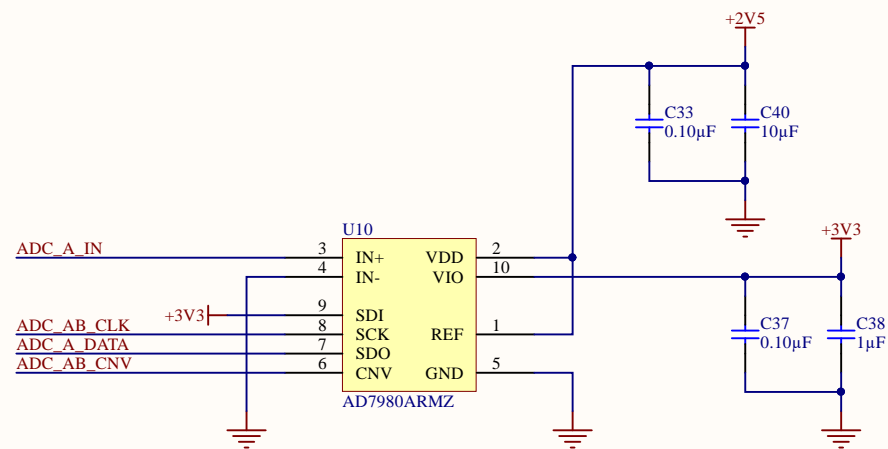
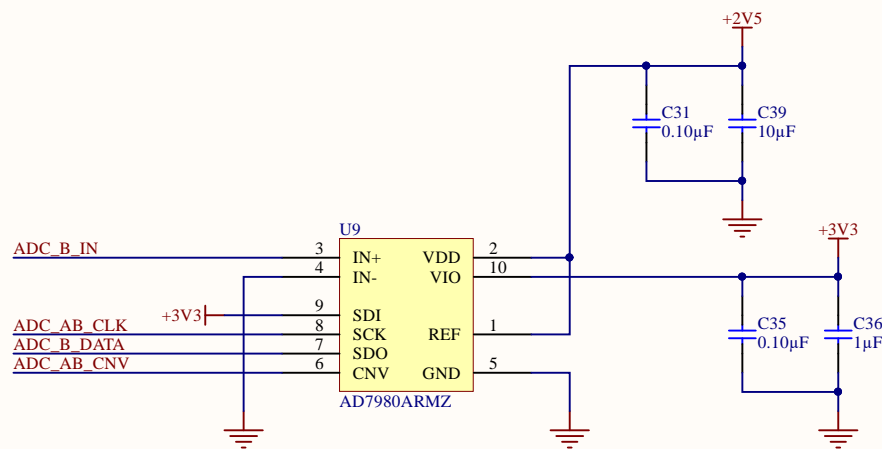
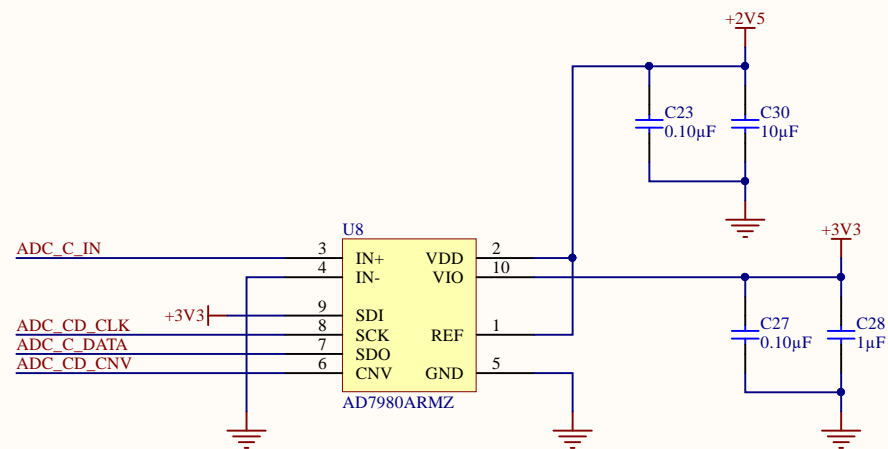
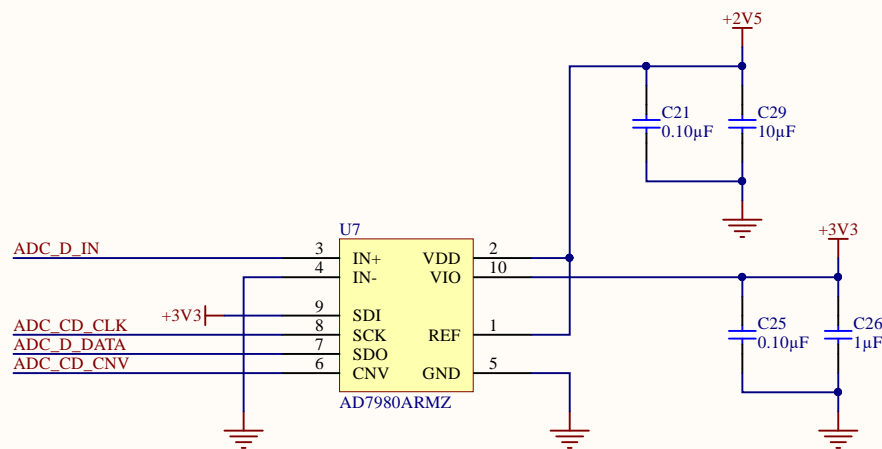
Title Page	
SDRdrum Arty Shield	Revision: C
Date: 2019-01-27	Sheet: 1/ 7



Inputs	
SDRdrum Arty Shield	Revision: C
Date: 2019-01-27	Sheet: 2 / 7



Outputs	
SDRdrum Arty Shield	Revision: C
Date: 2019-01-27	Sheet: 3 / 7



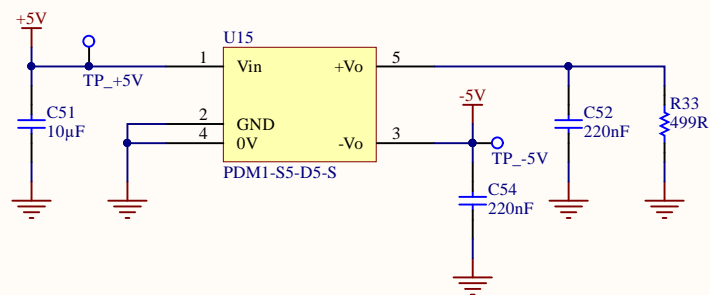
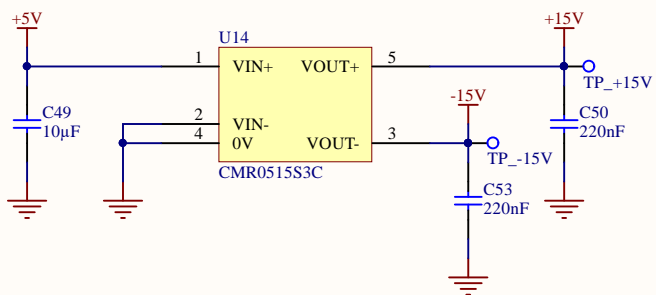
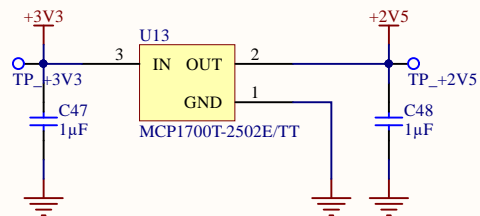
ADCs

SDRdrum Arty Shield

Revision: C

Date: 2019-01-27

Sheet: 4/ 7



DESIGN NOTE:
PDM1-S5-D5-S requires a minimum load of 10 mA per channel. R? provides this minimum load on the unused 5 V output.

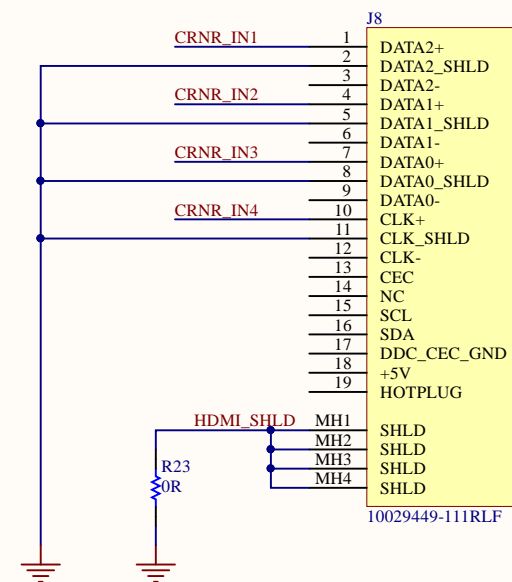
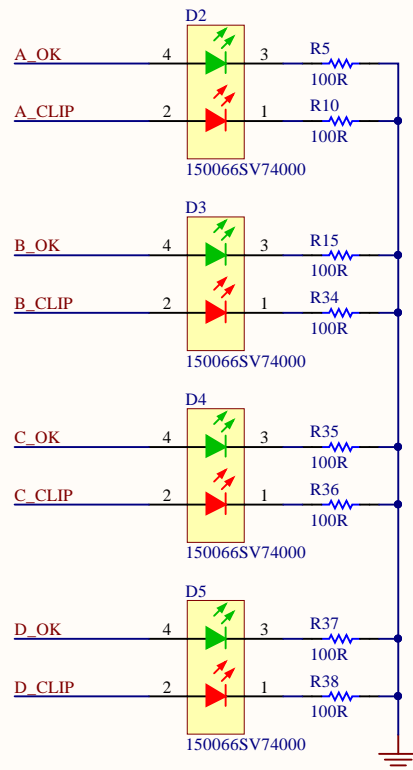
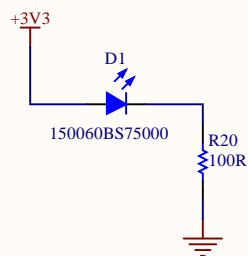
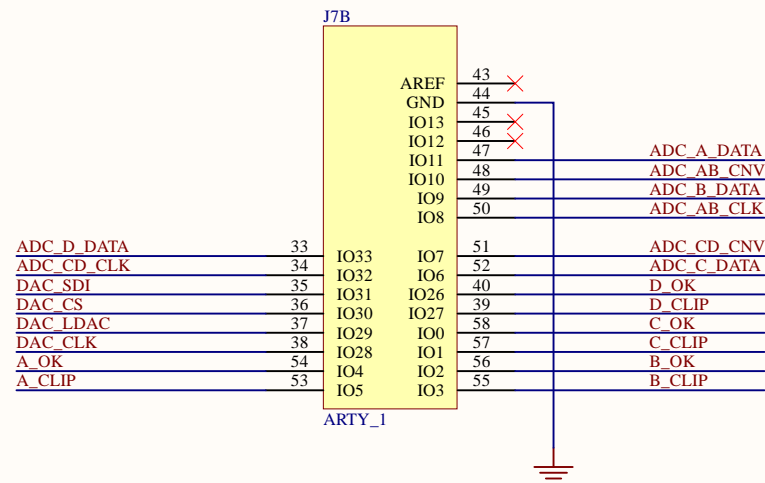
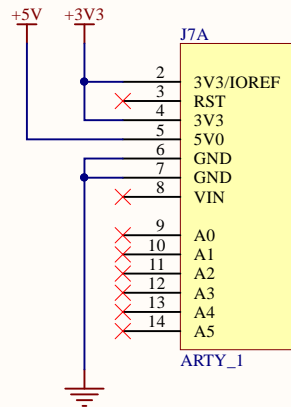
Power Supplies

SDRdrum Arty Shield

Revision: C

Date: 2019-01-27

Sheet: 6 / 7



Connectors and Mechanical

SDRdrum Arty Shield

Revision: C

Date: 2019-01-27

Sheet: 7 / 7