The Cray XC30 "Darter" System

Daniel Lucio

The Darter Supercomputer

The Darter Supercomputer

- Funded by the University of Tennessee to study cutting edge computing technologies
- Available since April 2013
- Next generation network interconnect (developed by DARPA HPCS program)
- 250 TFlops of peak performance
- Uses Intel technology
- Native shared library support

Darter Specs

- Cray XC30 (Cascade)
- Cray Linux Environment 5.0 upo3
- 4 compute racks
- 23,936 compute cores w/hyper threading
- 24 TB of compute memory
- 334TB Sonexion parallel file system
- 748 compute nodes
- Cray Aries Interconnect

Each compute node has:

- Two 2.6 GHz eight-core Intel SandyBridge (Xeon E5-2670) processors
- 16 physical cores (32 w/hyper-threading)
- 32 GB of memoryCray Aries interconnect with 8GB/sec bandwidth

Darter features?

- Home areas are the same across all NICS resources
- Latest software development tools available
- Native Shared libraries support
- Hyper-Threading is off by default. Need to use aprun option '-j 2' to turn it on
- No GSI access support.
- No PGI Compiler available
- Software tree is smaller, but you can do requests

http://www.nics.tennessee.edu/request-software-installation-nics

Darter Allocations

- Time available through JICS/NICS Discretionary Allocations.
- Access to UT academic community, Regional Education Partners and Industrial Partners.

	Research Allocation	**Pilot Allocation**	**EOT Allocation per event**
Darter (core hours)	500K-1M	200K	5K

http://www.nics.tennessee.edu/darter-allocations

Darter vs Kraken facts

	Darter	Kraken
Allocations	NICS/JICS	XSEDE/NICS
Processor	Intel Xeon	AMD Istanbul
Interconnect	Cray SeaStar	Cray Aries
Network Topology	3D-torus	Dragongfly
Shared Library support	YES!	no
HPSS access	no	yes
Software Tree status	Updated	Frozen
Default compiler	Cray CCE	PGI

Darter vs Kraken facts

	Darter	Kraken
Memory per node	32	16
#Cores per node	16 (32)	12
Hyper-threading	YES	N/A
Size for Node allocation	32	12

The size of allocation need to be a multiple of 32. This is because PBS expects the number of logical cores to use, and there are 32 logical cores per node.

Naming conventions

Cray modules now start with ‘’ cray-’

cray-ga/5.1.0.2(default)
cray-hdf5/1.8.11(default)
cray-hdf5-parallel/1.8.11(default)
cray-lgdb/2.2.1
cray-libsci/12.1.01
cray-mpich/6.1.0
cray-mpich2/6.1.0
cray-netcdf/4.3.0(default)
cray-netcdf-hdf5parallel/4.3.0(default)
cray-parallel-netcdf/1.3.1.1(default)
cray-petsc/3.4.2.0
cray-petsc-complex/3.4.2.0
cray-shmem/6.1.0
cray-tpsl/1.3.04(default)
cray-trilinos/11.4.1.0

Note: FFTW library still called ‘fftw’

Going from PGI to Intel

PGI	Intel	Description
`-fast`	`-fast -no-ipo`	Standard optimization
`-mp= nonuma`	`-openmp`	Enable OpenMP support
`-Mfixed`	`-fixed`	Fortran fixed format support
`-Mfree`	`-free`	Fortran free format support
`-byteswapio`	`-convert big_endian`	Read and write Fortran unformatted data files as big endian.
	`-mkl`	Link to Intel MKL
`-V`	`--version`	Show compiler version

Support for CAF and UPC

The Cray compiler compiler provides native support for Coarray Fortran and Unified Parallel C:

CAF example:

```
ftn -h caf -o CAFhello CAFhello.f90
```

UPC example:

```
cc -h upc -o UPCProg UPCProg.c
```

Compiler options

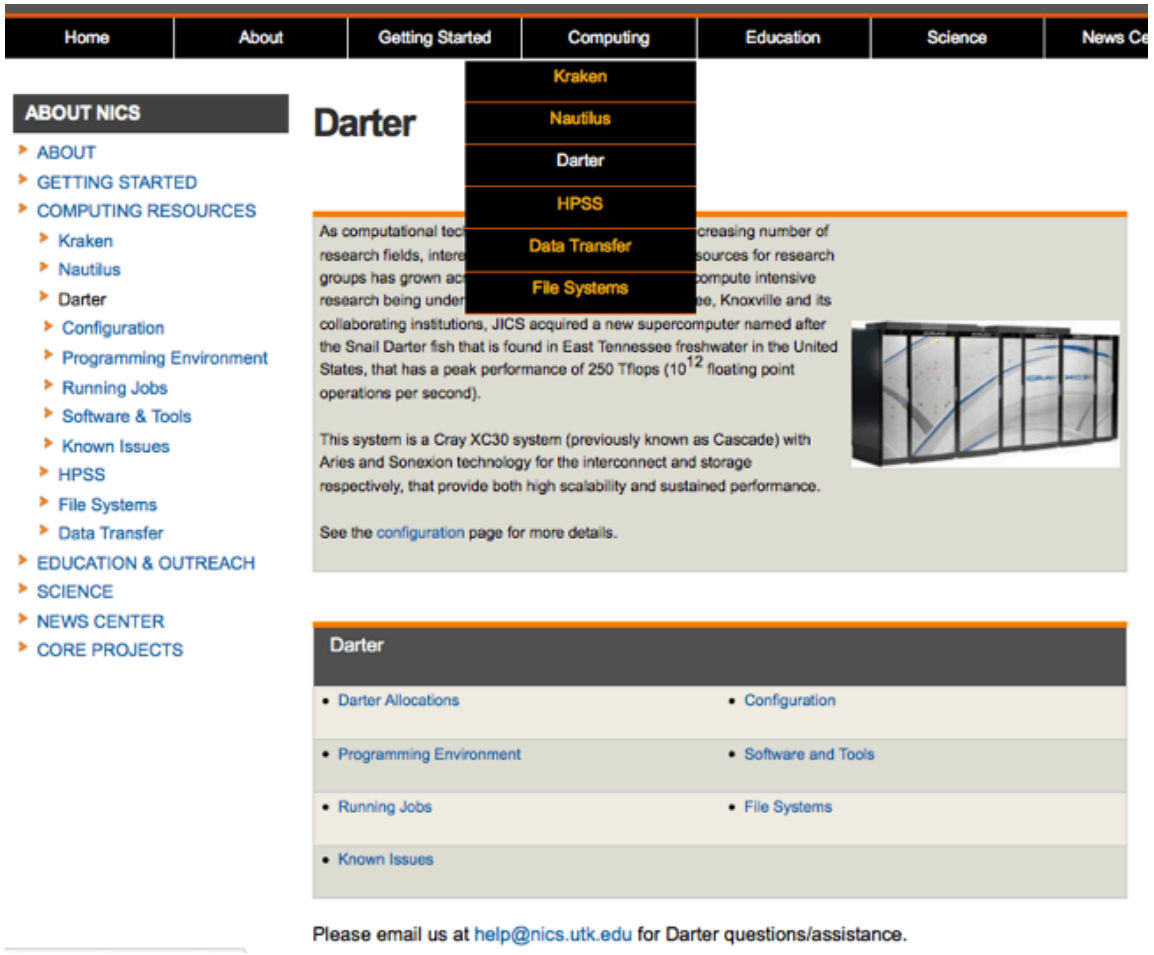
Recommended standard optimization arguments:

- **Cray**: *none, it does automatically*
- **Intel**: `-fast -no-ipo`
- **Gnu**: `-O3 -ffast-math`

When using the Intel compiler, you need to use option '`-mkl`' as a flag at link time to compile against the Intel MKL library.

Darter Documentation

http://www.nics.tennessee.edu/computing-resources/darter



Where to go for help?

help@nics.utk.edu

External links:

http://www.cray.com/Products/Computing/XC/Resources.aspx

https://www.olcf.ornl.gov/support/system-user-guides/eos-user-guide/

http://www.nersc.gov/users/computational-systems/edison/

http://user.cscs.ch/hardware/piz_daint_cray_xc30/index.html