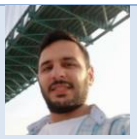
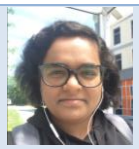
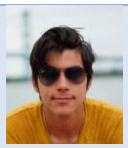
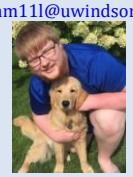
School of Computer Science
Faculty of Science

COMP-2650: Computer Architecture I: Digital Design
Fall 2020

Laboratory Guide v1.0	
Description[1]	This laboratory guide is intended for the student who takes *COMP2650: Computer Architecture I: Digital Design* course at the School of Computer Science. It includes 10 laboratory tutorials. Each laboratory covers design and analysis practices tightly connected to the course lectures, so the attendance at the lectures is highly encouraged for a better understanding of the treated subjects. The student is encouraged to go through the guide in the presented order, since each laboratory may contain elements studied, designed, and analyzed in the previous ones. Each chapter of this laboratory guide may start with a short presentation of the necessary theoretical concepts, followed by design and analysis practices to improve the problem-solving ability of the students. The weekly laboratory assignments that a student must do are found at the end of each chapter. The student is encouraged to carefully read all the laboratory material before attending the laboratory session to be familiar with the tasks that must be designed and/or analyzed throughout the laboratory.
Co-requisite	COMP2650: Computer Architecture I: Digital Design
Homepage	blackboard.uwindsor.ca→COMP2650-1-R-2020F-a: Computer Architecture I: Digital Design→ Labs
Lab Sections	blackboard.uwindsor.ca→COMP2650-1-R-2020F-a: Computer Architecture I: Digital Design→ Labroom Lab Instructor (GA): Saiteja Danda (saiteja@uwindsor.ca)[2] Lab Moderator (GA): Ala Alam Falaki (alamfal@uwindsor.ca) Lab Assistant (TA): Ariya Rasekh (rasekh@uwindsor.ca) Lab Assistant (TA): Section: 51, Mondays 11:30AM - 12:50PM, Blackboard Collaborate Ultra Section: 53, Mondays 01:00PM - 02:20PM, Blackboard Collaborate Ultra Section: 55, Tuesdays 11:30AM - 12:50PM, Blackboard Collaborate Ultra Lab Instructor (GA): Ala Alam Falaki (alamfal@uwindsor.ca) Lab Moderator (GA): Saiteja Danda (saiteja@uwindsor.ca) Lab Assistant (TA): Shivani Pansara (pansara@uwindsor.ca) Lab Assistant (TA): Husin Sarhill (sarhilla@uwindsor.ca) Section: 52, Wednesdays 11:30AM - 12:50PM, Blackboard Collaborate Ultra Section: 54, Wednesdays 01:00PM - 02:20PM, Blackboard Collaborate Ultra Section: 55, Tuesdays 11:30AM - 12:50PM, Blackboard Collaborate Ultra
Lab Instructors (GA) **Lab Assistants (TA)**	 Ala Alam Falaki (GA) alamfal@uwindsor.ca  Saiteja Danda (GA) saiteja@uwindsor.ca  Shivani Pansara (TA) pansara@uwindsor.ca  Ariya Rasekh (TA) rasekh@uwindsor.ca  Phillip Pham (TA) pham11l@uwindsor.ca  Husin Sarhill (GA) sarhilla@uwindsor.ca  Mohamad Farhat farha116@uwindsor.ca  Sean Janssens janssen1@uwindsor.ca

[1] This course is based on schematic design only and Hardware Description Language (HDL) is not covered.

[2] Wishing to contact the lab instructors or assistants, please use [uwinid]@uwindsor.ca and indicate full name, studentid, the course title.

# Labs	10	
Submission Due Date	Next Week Wednesdays Midnight Anywhere on Earth (AoE)	
Grade Release Date	1 Week after Submission Due Date	
Marking Scheme	10 Lab Assignments × 2% Each = 20%	
Attendance	Encouraged but not mandatory due to time zone accommodation in the COVID-19 era.	
Office Hours	N/A.	
Schedule[3,4]	**L01: Meet & Greet, Number Systems I** Binary, Octal, and Hexa Numbers. Number-base Conversions.	Sep. 21-23
	L02: Number Systems II Complements of Numbers. Signed Numbers. Binary Codes.	Sep. 28-30
	L03: Boolean Algebra and Logic Gates Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Digital Logic Gates.	Oct. 05-07
	Reading Week No Laboratory	Oct. 10-18
	L04: Gate-Level Minimization I The Map Method. Four-Variable K-Map. Product-of-Sums Simplification.	Oct. 19-21
	L05: Gate-Level Minimization II Don't-Care Conditions. NAND, NOR, XOR, Wired AND, Wired OR.	Oct. 26-28
	L06: Combinational Logic I & II Adders. Subtractors. Multipliers. Decoders. Encoders. Multiplexers. Demultiplexers.	Nov. 02-04
	L07: Synchronous Sequential Logic I Sequential Circuits. Latches. Flip-Flops.	Nov. 09-11
	L08: Synchronous Sequential Logic II Analysis of Clocked Sequential Circuits. State Reduction and Assignment.	Nov. 16-18
	L09: Synchronous Sequential Logic III Registers and Counters. Shift Registers.	Nov. 23-25
	L10: Synchronous Sequential Logic IV Ripple Counters. Synchronous Counters.	Nov. 30-Dec 02

Notes to Students:

1. **Equity, Diversity, and Inclusiveness (EDI):** Lab sections along with all its components are, without question, safe places for students of all races, genders, sexes, ages, sexual orientations, religions, disabilities, and socioeconomic statuses. Disrespectful attitude, sarcastic comments, offensive language, or language that could be translated as offensive and/or marginalize anyone are absolutely unacceptable. Immediate actions must be taken by the lab instructor to protect the safety and comfort of the students. Ethnically rich and diverse, multi-cultural world should be celebrated in the labs. The instructor, too, must treat every student equally and with the respect and compassion that all students deserve.
2. **Lab Assignment:** Lab assignments are expected to be submitted on the assigned due date and time. Late submission is not accepted and receive zero unless a verifiable reason with appropriate documentation is provided. The students should follow the submission procedure for each assignment. Failure to follow the procedure (e.g., incorrect, unreadable, and/or missing file attachments as instructed) heavily penalizes the assignment. Each assignment must be done *individually*.
3. **Accommodation for Religious or Spiritual Observance:** Requests for accommodation of specific religious or spiritual observance must be presented to the instructor no later than 2 weeks prior to the conflict in question. In extenuating circumstances, this deadline may be extended. If the dates are not known well in advance because they are linked to other conditions, requests should be submitted as soon as possible in advance of the required observance. Timely requests will prevent difficulties in arranging constructive accommodations.

[3] This is a preliminary schedule. The material and depth and order of presentation are subject to change at the discretion of the instructor and student pace.

[4] There is no lab session in the first and last weeks of the course as well as reading week.

4. **Academic Accommodation:** A student who has 3 or more major in-term evaluations scheduled or due within 24 hours may apply, no later than the end of the first quarter of classes, to seek an appropriate accommodation such as a due date extension and alternative assignment.
5. **Appeal:** Students have the right to review the assignments marking within 1 week of their release.
6. **Policies, Bylaws, and Procedures:** Students are required to adhere to all relevant policies, bylaws, and procedures at the University of Windsor including, but not limited to, the student code of conduct, academic integrity, student academic and non-academic conduct. Failure to follow the policies, bylaws, and procedures are subject to disciplinary procedures as set out under, but not limited to, the Senate Bylaw 31: Academic Integrity and Procedures for Addressing Student Non-Academic Misconduct. Regarding the plagiarism, the Blackboard's SafeAssign will be used for some or all student assignments or equivalent at the instructor's discretion. Plagiarized submissions, i.e., submissions with the same or minor modifications, receive zero. Should you need to record the lectures, please follow the Senate Policy on Recording Lectures.
7. **Communication (Student-Lab Instructor-Lab Assistant):** Students are required to obtain and maintain a University of Windsor e-mail account, [uwindid]@uwindsor.ca, for timely communications with the instructor. The course homepage on the Blackboard, *COMP2650-1-R-2020F-a: Computer Architecture I: Digital Design*, is the main notification center for the lab announcements and repository for the lab material and resources. Blackboard Collaborate Ultra at *COMP2650-1-R-2020F-a: Computer Architecture I: Digital Design → Labroom → Lab Section* is the official place for the lab sections. In Microsoft Teams, the team *SCS - COMP2650 - Fall2020* with channels for each lab section is provided for emergency cases and backup plans only.
8. **Office Hour:** There is no office hour dedicated to assistants in meeting with students. Assistants, however, are accessible on an ad-hoc basis throughout the week via email, discussion board, or teams.
9. **Change Notification:** Any changes in the lab outline, due dates, marking, or evaluation will be discussed in class at least 2 weeks prior to being implemented.
10. **Student Evaluation of Lab Instructor:** The student evaluation of the lab instructor will be conducted during the last weeks of the classes.
11. **Online Experience:** Participants in online lectures and lab sections include an instructor, a moderator, and students. Students are able to share camera or send messages but cannot share audio unless they Raise Hand, and the moderator or the instructor allows them. The moderator also supervises private messages. Students are encouraged to let the moderator and/or the instructor know of any connection issues asap regarding the quality of presentation in terms of audio and video (e.g., slides).
12. **Feeling Overwhelmed?** Should face obstacles and experience difficulties that affect her academic performance, students can reach out to the following service centers as well as other on- and off-campus resources listed at www.uwindsor.ca/wellness:
    - Student Health Services
    - Student Counselling Centre
    - Peer Support Centre

Lab#	Title	Due Date	Grade Release Date
Lab 01	**L01: Meet & Greet, Number Systems I** Binary, Octal, and Hexa Numbers. Number-base Conversions.	Sept. 30, 2020 Wednesday Midnight AoE	Oct. 07, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 02	**L02: Number Systems II** Complements of Numbers. Signed Numbers. Binary Codes.	Oct. 07, 2020 Wednesday Midnight AoE	Oct. 14, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 03	**L03: Boolean Algebra and Logic Gates** Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Digital Logic Gates.	Oct. 14, 2020 Wednesday Midnight AoE	Oct. 21, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 04	**L04: Gate-Level Minimization I** The Map Method. Four-Variable K-Map. Product-of-Sums Simplification.	Oct. 28, 2020 Wednesday Midnight AoE	Nov. 04, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 05	**L05: Gate-Level Minimization II** Don't-Care Conditions. NAND, NOR, XOR, Wired AND, Wired OR.	Nov. 04, 2020 Wednesday Midnight AoE	Nov. 11, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 06	**L06: Combinational Logic I & II** Adders. Subtractors. Multipliers. Decoders. Encoders. Multiplexers. Demultiplexers.	Nov. 11, 2020 Wednesday Midnight AoE	Nov. 18, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 07	**L07: Synchronous Sequential Logic I** Sequential Circuits. Latches. Flip-Flops.	Nov. 18, 2020 Wednesday Midnight AoE	Nov. 25, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 08	**L08: Synchronous Sequential Logic II** Analysis of Clocked Sequential Circuits. State Reduction and Assignment.	Nov. 25, 2020 Wednesday Midnight AoE	Dec. 02, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 09	**L09: Synchronous Sequential Logic III** Registers and Counters. Shift Registers.	Dec. 02, 2020 Wednesday Midnight AoE	Dec. 09, 2020

Lab#	Title	Due Date	Grade Release Date
Lab 10	**L10: Synchronous Sequential Logic IV** Ripple Counters. Synchronous Counters.	Dec. 09, 2020 Wednesday Midnight AoE	Dec. 13, 2020