PGP PPI For The RCE Generation 3 Platform Design Document

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1 PGP PPI Modules

1.1 PGP PPI Top Level

1.1.1 Top Level Interfaces

The generic ports for the top level module are shown in table 1. The exact values may expand or change depending on the implementation decisions of the designer. This table is meant as a guide to indicate what type of top level configurations may be required to meet the system requirements.

Value	Type	Default	Description
TPD_G	time	1 ns	Synchronous signal delay value for simulation.
LANE_COUNT_G	positive	12	Generic to determine how many lanes are implemented. One per Lane.
LANEn_RATE_G	TBD	TBD	Generics to configure the line rate of each lane. One per Lane.
LANEn_WIDTH_G	TBD	TBD	Generics to configure the interface width of each lane. One per Lane.
LANEn_SYNC_G	boolean	false	Generics to configure enable synchronous mode for each lane. One per Lane.
LANEn_VER_G	positive	2	Generics to determine the PGP version for each lane. One per Lane.
LANEn_REFSEL_G	TBD	TBD	Generics to determine the reference for each lane. One per Lane.

Table 1: Top Level Generics

The proposed signal ports for the top level module are shown in table 2.

Signal	Type	Width	Direction	Description
sysClk200	Logic	1	In	External 200Mhz system clock. Used as the clock for the PPI interface.
sysClk200Rst	Logic	1	In	Reset for external 200Mhz system clock.
locRefClk	Logic	2	In	Reference clocks from local DPM oscillators.
extRefClk	Logic	3	In	Reference clocks from DTM.
sysClk	Logic	1	In	System clock used by synchronous lanes.
sysCode	Logic	8	In	8-Bit system code which is forwarded by lanes running in synchronous mode. Sampled when SysCodeEn is high.
sysCodeEn	Logic	1	In	Enable for 8-bit system code.
obPpiClk	Logic	1	Out	Outbound PPI clock input
obPpiToFifo	ObPpiToFifoType	1	Out	Outbound PPI input signals
obPpiFromFifo	ObPpiFromFifoType	1	In	Outbound PPI output signals
ibPpiClk	Logic	1	Out	Outbound PPI clock input
ibPpiToFifo	IbPpiToFifoType	1	Out	Inbound PPI input signals
ibPpiFromFifo	IbPpiFromFifoType	1	In	Inbound PPI output signals
pgpRxP	Logic	LANE_COUNT_G	In	PGP serial RX positive
pgpRxM	Logic	LANE_COUNT_G	In	PGP serial RX negative
pgpTxP	Logic	LANE_COUNT_G	Out	PGP serial TX positive
pgpTxM	Logic	LANE_COUNT_G	Out	PGP serial TX negative

Table 2: ArmRceG3Top Signals

1.1.2 Top Level Block Diagram

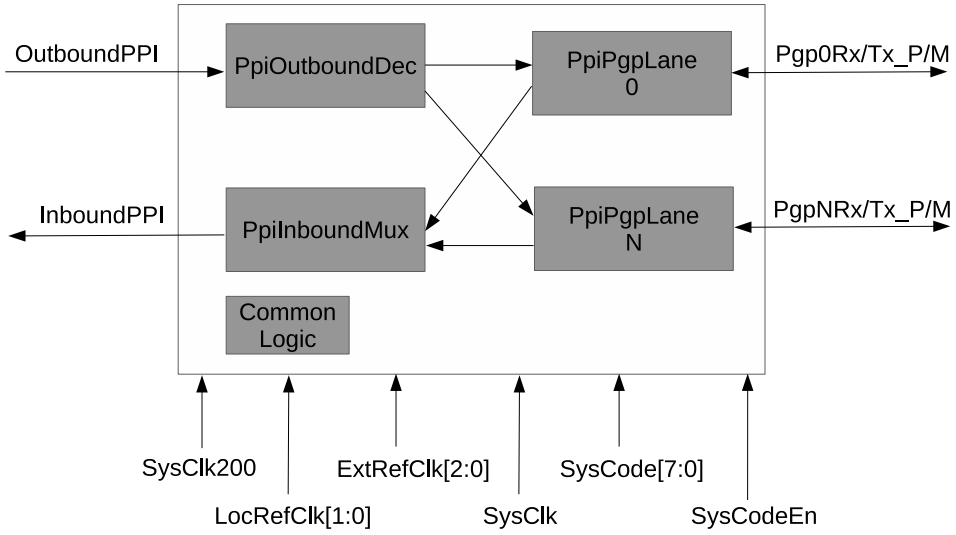

Figure 1: Top Level Block Diagram

The PGP PPI block supports up to 12 PGP lanes. The 11 lanes operate independently, each having it's own width, speed, clocking mode and version as configured through a set of generics.

1.2 PPI Outbound Decoder

The outbound decoder block serves as the interface between the single outbound PPI interface and the numerous PPG lane blocks. This block is implemented as a generic block which may be reused in many PPI implementations.

1.2.1 PPI Outbound Decoder Interfaces

The generic ports for the PPI outbound decoder module are shown in table 3. The exact values may expand or change depending on the implementation decisions of the designer.

Value	Type	Default	Description
TPD_G	time	1 ns	Synchronous signal delay value for simulation.
DEC_COUNT_G	positive	12	Generic to determine how many decoded interfaces are implemented.

Table 3: PPI Outbound Decoder Generics

The proposed signal ports for the PPI outbound decoder module are shown in table 4.

Signal	Type	Width	Direction	Description
obPpiClk	Logic	1	In	Outbound PPI clock input
obPpiToFifo	ObPpiToFifoType	1	Out	Outbound PPI input signals
obPpiFromFifo	ObPpiFromFifoType	1	In	Outbound PPI output signals
obDecPpiToFifo	ObPpiToFifoType	DEC_COUNT_G	Out	Decoded Outbound PPI input signals
obDecPpiFromFifo	ObPpiFromFifoType	DEC_COUNT_G	In	Decoded Outbound PPI output signals

Table 4: PPI Outbound Decoder Signals

1.2.2 PPI Outbound Decoder Block Diagram

The outbound decoder block is fully synchronous to sysClk200 and does not contain any FIFOs. The flow control state of the destination lane determines if the frame can be read from the outbound PPI interface.

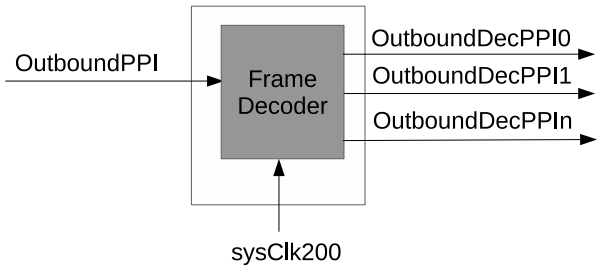

Figure 2: PPI Outbound Decoder Block Diagram

1.2.3 PPI Outbound Frame Format

The following diagram shows the outbound PPI frame and the location of the field which the outbound decoder uses to direct the frame. The least significant byte of the first quad word transfered contains the 8-bit destination ID.

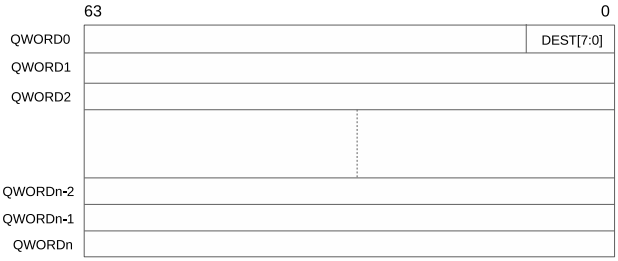

Figure 3: PPI Outbound Decoder Frame Fields

1.3 PPI Inbound Multiplexer

The PPI inbound multiplexer moves a frame at time from one of a number of PGP lane modules to the inbound PPI interface and is is fully synchronous to the sysClk200 system clock. Arbitration logic chooses which lane module to accept data from while the multiplexer moves the frame frame from the selected interface. The frame encoder updates the inbound frame indicating the source address of the frame. This block is implemented as a generic block which may be reused in many PPI implementations.

1.3.1 PPI Inbound Multiplexer Interfaces

The generic ports for the PPI inbound multiplexer module are shown in table 5. The exact values may expand or change depending on the implementation decisions of the designer.

Value	Type	Default	Description
TPD_G	time	1 ns	Synchronous signal delay value for simulation.
MUX_COUNT_G	positive	12	Generic to determine how many muliplexed interfaces are implemented.

Table 5: PPI Inbound Multiplexer Generics

The proposed signal ports for the PPI inbound multiplexer module are shown in table 6.

Signal	Type	Width	Direction	Description
ibPpiClk	Logic	1	In	Inbound PPI clock input
ibPpiToFifo	ObPpiToFifoType	1	Out	Inbound PPI input signals
ibPpiFromFifo	ObPpiFromFifoType	1	In	Inbound PPI output signals
ibMuxPpiToFifo	ObPpiToFifoType	MUX_COUNT_G	Out	Multiplexed Inbound PPI input signals
ibMuxPpiFromFifo	ObPpiFromFifoType	MUX_COUNT_G	In	Multiplexed Inbound PPI output signals
laneReq	Logic	MUX_COUNT_G	In	Lane frame request.
laneGnt	Logic	MUX_COUNT_G	Out	Lane frame grane.

Table 6: PPI Inbound Multiplexer Signals

1.3.2 PPI Inbound Multiplexer Block Diagram

The inbound multiplexer block is fully synchronous to sysClk200 and does not contain any FIFOs.

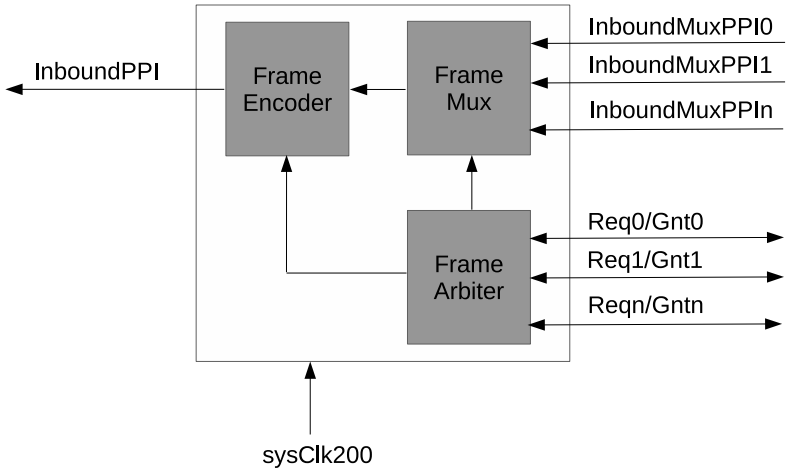

Figure 4: PPI Inbound Multiplexer Block Diagram

1.3.3 PPI Inbound Frame Format

The following diagram shows the inbound PPI frame and the location of the field into which the frame source is encoded. The least significant byte of the first quad word transfered contains the 8-bit source ID.

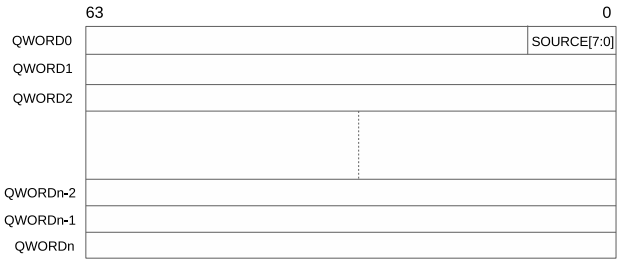

Figure 5: PPI Inbound Multiplexer Frame Fields

1.4 PPI PGP Lane Module

The PGP lane module contains the logic required to interface a single PGP lane with the inbound and outbound PPI interfaces. This module is designed to be generic with numerous variations supporting configurable modes and versions of the PGP cores.

1.4.1 PPI PGP Lane Interfaces

The generic ports for the PPI PGP lane module are shown in table 7. The exact values may expand or change depending on the implementation decisions of the designer.

Value	Type	Default	Description
TPD_G	time	1 ns	Synchronous signal delay value for simulation.
LANE_RATE_G	TBD	TBD	Generics to configure the line rate of the lane.
LANE_WIDTH_G	TBD	TBD	Generics to configure the interface width of the lane.
LANE_SYNC_G	boolean	false	Generics to configure enable synchronous mode for the lane.
LANE_VER_G	positive	2	Generics to determine the PGP version for the lane.
LANE_REFSEL_G	TBD	TBD	Generics to determine the reference for the lane.

Table 7: PPI PGP Lane Generics

The proposed signal ports for the PPI PGP Lane module are shown in table 8.

Signal	Type	Width	Direction	Description
sysClk200	Logic	1	In	External 200Mhz system clock. Used as the clock for the PPI interface.
sysClk200Rst	Logic	1	In	Reset for external 200Mhz system clock.
locRefClk	Logic	2	In	Reference clocks from local DPM oscillators.
extRefClk	Logic	3	In	Reference clocks from DTM.
sysClk	Logic	1	In	System clock used by synchronous lanes.
sysCode	Logic	8	In	8-Bit system code which is forwarded by lane when running in synchronous mode. Sampled when SysCodeEn is high.
sysCodeEn	Logic	1	In	Enable for 8-bit system code.
obPpiToFifo	ObPpiToFifoType	1	Out	Outbound PPI input signals
obPpiFromFifo	ObPpiFromFifoType	1	In	Outbound PPI output signals
ibPpiToFifo	IbPpiToFifoType	1	Out	Inbound PPI input signals
ibPpiFromFifo	IbPpiFromFifoType	1	In	Inbound PPI output signals
laneReq	Logic	1	Out	Lane frame request.
laneGnt	Logic	1	In	Lane frame grane.
pgpRxP	Logic	1	In	PGP serial RX positive
pgpRxM	Logic	1	In	PGP serial RX negative
pgpTxP	Logic	1	Out	PGP serial TX positive
pgpTxM	Logic	1	Out	PGP serial TX negative

Table 8: PPI PGP Lane Signals

1.4.2 PPI PGP Lane Block Diagram

The proposed block diagram for the PPI PGP Lane module is shown below. The logic is separated into blocks which are each described in detail in the following text. The PPI PGP lane module has a number of input clocks to support a wide variety of operating modes. The inbound and outbound PPI interfaces are synchronous to sysClk200 One of the other inputs clocks is chosen to be the reference clock for the PGP module depending on the chosen operating mode. SysClk, sysCode and sysCodeEn are utilized for the PGP module operating in synchronous mode while the remaining reference clocks are available when operating in asynchronous mode.

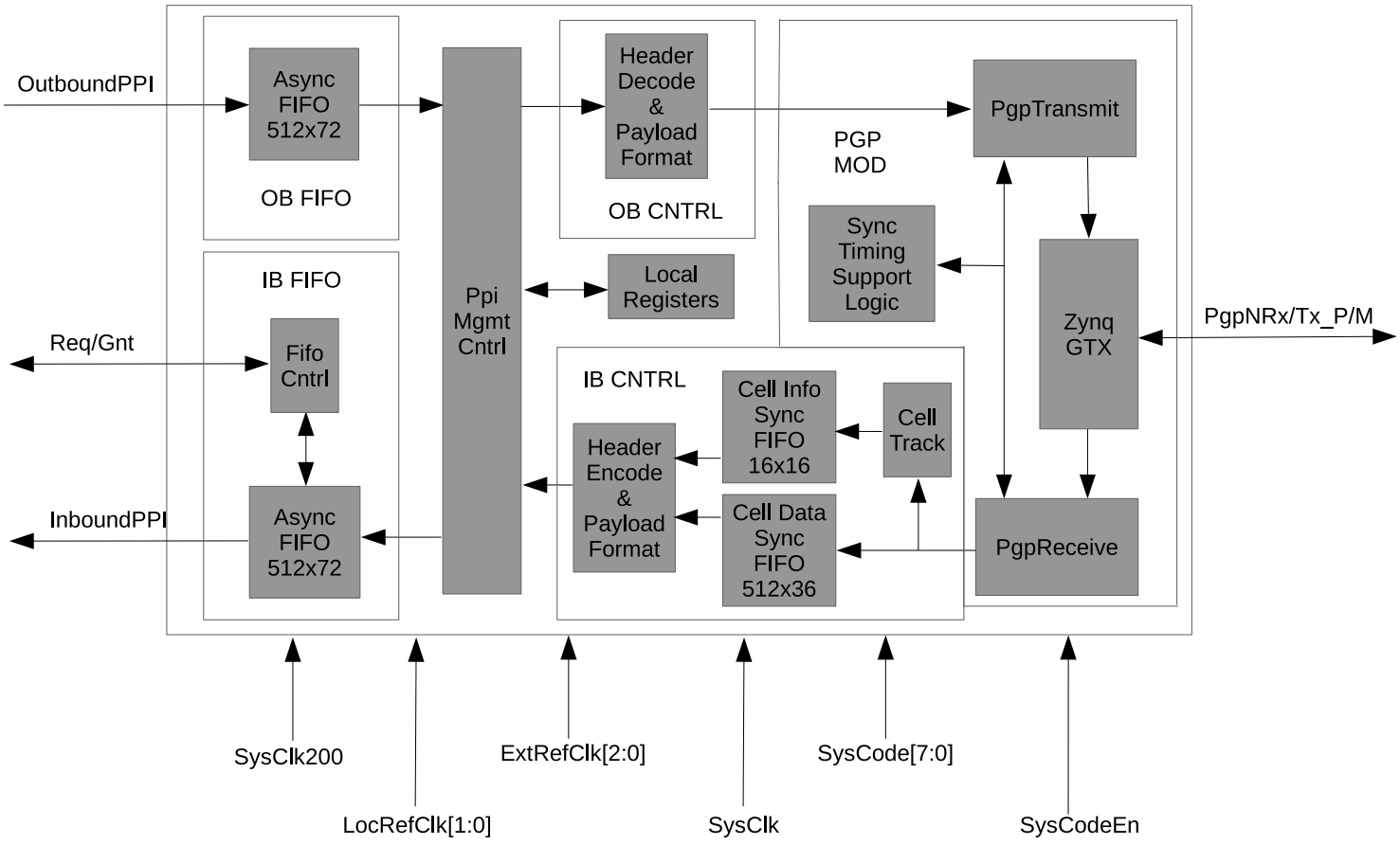

Figure 6: PPI PGP Lane Block Diagram

1.4.3 Outbound FIFO Block

The outbound FIFO block (OB FIFO) receives outbound PPI frames from the outbound PPI decoder module. Data is buffered in an asynchronous 72-bit x 512 entry FIFO with the PPI side being synchronous to SysClk200 and the PGP side being synchronous to the configured PGP transmit clock. The output of this FIFO is passed to the PPI management control module.

1.4.4 PPI Management Control

The PPI management control module (see section 1.5) sits in both the outbound and inbound data paths. This module intercepts and processes management frames that are received at the outbound PPI interface.

1.4.5 Outbound Control

The outbound control block (OB CNTRL) receives the PPI frame, decodes the header and passes the payload to the appropriate PGP virtual channel. The 64-bit words received from the PPI interface are passed to the PGP transmit core in smaller units containing 16-bits or 32-bits of data as determined by the native width of the configure PGP transmit core with the lower bits being transmitted first. The EOF and size fields of the outbound PPI frame indicate the end of the transmitted cell.

This module monitors the flow control signals for the selected virtual channel, pausing data transmission as necessary.

All of the logic in the outbound control block is synchronous to the PGP transmit clock.

The following diagram shows the proposed format for the outbound PGP frame. The first 64-bit quad word forms the header and contains control information for the outbound frame.

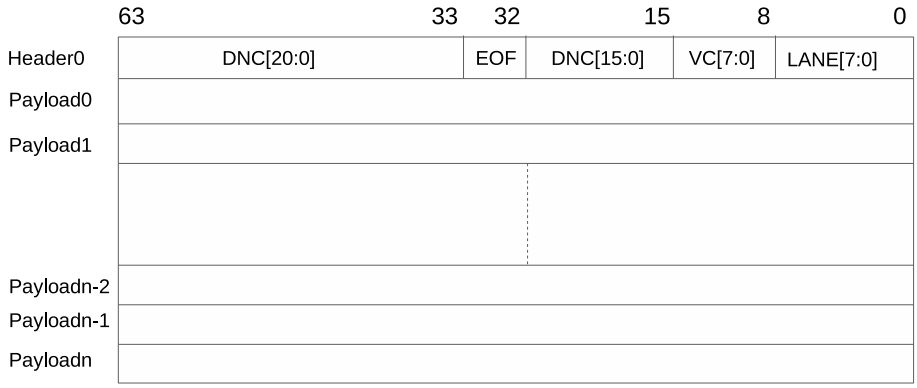

Figure 7: PPI PGP Outbound Frame Format

The following fields are found in the outbound PPI header word:

- Lane[7:0]: Identifies the destination lane for the outbound frame. (ignored by this block)
- VC[7:0]: Identifies the destination virtual channel for the outbound frame.
- EOF: Indicates if this cell is the last in a frame.

1.4.6 PGP Module

The PGP module (PGP MOD) contains the generic PGP core and it's support logic. This block of logic is implemented using one of the PGP modules provided by the PGP support library. This block contains the receive and transmit PGP cores, the Zynq GTX module and additional logic required to support synchronous clocking. The details of this module are described in a separate document.

The interface to PGP module will include a number of configuration and status vectors which must be supported by the local register logic.

1.4.7 Inbound Control

The inbound controller (IB CNTRL) will receive partial frames from the PGP receive core. Each of these partial frames contains a a single PGP cell worth of data. The boundary between receive cells is indicated when the valid signal is de-asserted by the PGP receive core. All of the logic in the inbound control block is synchronous to the PGP receive clock.

Received cell data is passed directly to the cell data buffer which is implemented in a 36-bit by 512 entry FIFO. This FIFO is 36-bits wide in order to support future versions of the PGP core which will utilize a 32-bit wide interface. The upper half of this FIFO is not be utilized when interfacing to the current 16-bit PGP cores.

When the end of the cell is received the cell tracking logic will add a single 16-bit entry to the cell information buffer. This buffer is implemented in a synchronous distributed ram 16-bit x 16-entry FIFO. This buffer stores information about the length, virtual channel and control signals (EOF and EOFE) of the received cell.

The header encode and payload format block of firmware will pull entries from the cell information and cell data FIFOs. The entries from these two FIFOs are used to form the inbound PPI frame as shown in the following diagram. The frame is then passed through the PpiMgmtCntrl block and on to the inbound PPI FIFO control block. This block forms the received 16-bit (or 32-bit) PGP data into 64-bit quad words for the PPI inbound interface. The lower 16-bits of the 64-bit quad word are filled first. The EOF bit and

size field of the inbound PPI interface are updated accordingly and a single idle cycle is inserted between each inbound PPI frame.

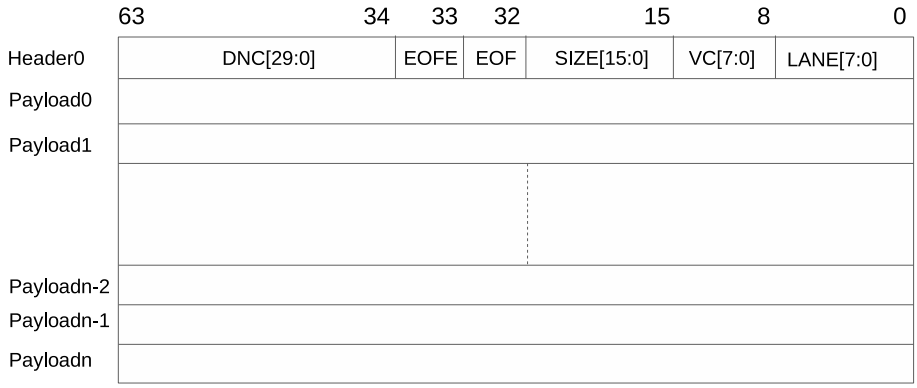

Figure 8: PPI PGP Inbound Frame Format

The following fields are found in the inbound PPI header word:

- Lane[7:0]: Identifies the source lane for the outbound frame. (set to zero by this block)
- VC[7:0]: Identifies the source virtual channel for the outbound frame.
- Size[15:0]: Indicates the size of the received cell in bytes.
- EOF: Indicates that the cell received is the last in a PGP frame.
- EOFE: Indicates that the frame contained errors (coincident with EOF).

The inbound control block will assert flow control to the PGP core based upon the fill level of the cell information and cell data FIFOs.

1.4.8 Inbound PPI FIFO

The inbound PPI FIFO logic (IB FIFO) accepts inbound cell frame from the inbound controller as well as management response frames generated in the PPI management control module. Inbound PPI frames are buffered in an asynchronous 72-bit x 512 entry FIFO. The PGP side of this FIFO is synchronous to the PGP receive clock while the PPI side of this FIFO is synchronous to SysClk200.

The FIFO control logic contained within this block keeps track of the number of PPI frames stored in the asynchronous FIFO. If at least one frame exists in this FIFO it will assert the request line to the inbound PPI multiplexer logic. When the incoming grant line is asserted, a single frame of data will be read out of the FIFO to the inbound PPI multiplexer. The request line is de-asserted between each frame to allow for re-arbitration.

1.5 PPI Management Module

The PPI management module is designed to interface with both the receive and transmit data paths. This module intercepts management frames sourced from the outbound PPI interface and converts them into local register read and write transactions. In the inbound direction response frames are inserted into the inbound data paths when gaps permit. The PPI management block supports three separate clock domains, one for the outbound data path, one for the inbound data path and the last for the local register bus.

This module is designed to be generic and used in a number of PPI implementations.

1.5.1 PPI Management Interfaces

The generic ports for the PPI management module are shown in table 9. The exact values may expand or change depending on the implementation decisions of the designer.

Value	Type	Default	Description
TPD_G	time	1 ns	Synchronous signal delay value for simulation.

Table 9: PPI Management Generics

The proposed signal ports for the PPI management module are shown in table 10.

Signal	Type	Width	Direction	Description
obPpiClock	Logic	1	In	Outbound PPI clock
obPpiToFifo	ObPpiToFifoType	1	Out	Outbound PPI input signals
obPpiFromFifo	ObPpiFromFifoType	1	In	Outbound PPI output signals
obLocPpiToFifo	ObPpiToFifoType	1	In	Local Outbound PPI input signals
obLocPpiFromFifo	ObPpiFromFifoType	1	Out	Local Outbound PPI output signals
ibPpiClock	Logic	1	In	Inbound PPI clock
ibPpiToFifo	IbPpiToFifoType	1	Out	Inbound PPI input signals
ibPpiFromFifo	IbPpiFromFifoType	1	In	Inbound PPI output signals
ibLocPpiToFifo	IbPpiToFifoType	1	In	Local Inbound PPI input signals
ibLocPpiFromFifo	IbPpiFromFifoType	1	Out	Local Inbound PPI output signals
regClock	Logic	1	In	Local register space clock
regAddr	Logic	16	Out	Local register address bus
regWriteEnable	Logic	1	Out	Local register write enable signal
regWriteData	Logic	32	Out	Local register write data bus
regReadEnable	Logic	1	Out	Local register read enable signal
regReadValid	Logic	1	In	Local register read data valid signal
regReadData	Logic	32	In	Local register read data bus

Table 10: PPI Management Signals

1.5.2 PPI Management Block Diagram

The following block diagram shows the internal structure of the PPI management block. Two asynchronous FIFOs of undetermined size are used to buffer incoming requests and outgoing responses.

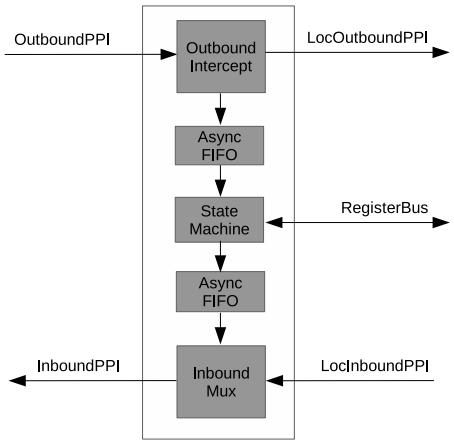

Figure 9: PPI Management Block Diagram

1.5.3 PPI Management Frames

The following figure shows the format for an outbound management frame. This frame contains a single 64-bit quad word header containing the lane number (updated and decoded by external blocks), a write enable bit, a 16-bit address and 32-bit data.

Read requests have the write bit set to zero and an empty data field. Once the read transaction has completed the frame will be sent back to the PPI software with the data field containing the resulting read data.

Write requests will have the write bit set to one and contain the write data. The write transaction is processed without a response?

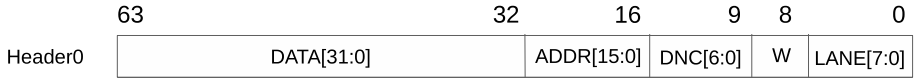

Figure 10: PPI PGP Management Frame

1.5.4 Local Register Bus

An example write transaction is shown in the following figure. The address, write enable and write data are presented for a single clock period.

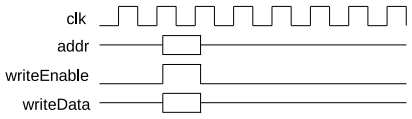

Figure 11: PPI PGP Management Write

An example read transaction is shown in the following figure. The address and read enable signal are asserted for a single clock period. The state machine then waits for the local bus client to return the read data on the readData vector coincident with the assertion of the readValid signal. The state machine will wait for up to 256 clock cycles for the local bus slave to complete the read transaction. If the local bus slave does not respond within this period of time the transaction will be terminated and the read data returned will be 0xdeadbeef.

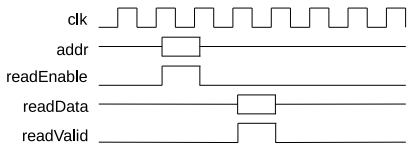

Figure 12: PPI PGP Management Read