Cryo Detector Frequency Tracking Algorithm (FTA)

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# Registers

The Cryo Mux Processor presently contains up to 2048 “Configuration” registers which the app can read and write, and up to 2048 “Status” registers which are read-only to the app. All registers are 32-bits wide. Registers are defined below; more registers will be defined eventually.

### Configuration Registers

The Configuration Registers are used by the app to configure and operate the FPGA PLL. Configuration Registers are write-only to the high-level app.

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| --- | --- | --- | --- |
| **Configuration Registers (R/W)** | | | |
| **AXI addr** | **Word** | **Function** | **Comments** |
| 0x800 | 0 | Control Register | See bit-by-bit definition below |
| 0x804 | 1 | Feedback enable | Set bit 0 to 1 to enable overall feedbacks  (each channel must be individually enabled as well) |
| 0x808 | 2 | Feedback gain | unsigned 16\_12 e.g 0x1000 = nominal gain  min nonzero gain = 1/4096, max gain = 16 |
| 0x80c | 3 | Reference delay | Compensates delay of up/down converter and cryo,  8 bits in steps of 5.4 ns, range 0 to 1.378 s |
| 0x810 | 4 | Output amplitudes | A0 (31:16) amplitude of central lines 0xffff=full scale  A1 (15:0) relative amplitudes of sidebands 0xffff=1.0  Both are unsigned 16\_16 |
| 0x814 | 5 | FB limit  Fsideband | (31:16) max frequency excursion for FB  Sideband offset frequency 185MHz/216 =2.8125 kHz per LSB |
| 0x818 | 6 | Bandwidth | Bandwidth assumed for each notch. 16 bits in increments of 185MHz/216 ~= 2.8 kHz  (functionally another feedback gain) |
| 0x81c | 7 | Synch threshold | Signed 16\_15 threshold on ADC 1 for signaling flux ramp synch when using function generator |
| 0x820 | 8 | Phase ref lowpass control  Freq Error lowpass control | wPhiRef (15:0) unsigned 16\_16  wdPhi (31:16) 1.0🡺no filtering (see Note 1 below) |
| 0x824 –0x8f8 | 9 -62 | unused |  |
| 0x8fc | 63 | Command Reg | Set bit 0 to reset algorithm |
| 0x900 –0x93C | 64-95 | Enable FBi  Initial Fi | Fi [24]: FBeni enable ith feedback (1=ena,0=disa)  Fi [23:0] Initial frequency of ith line, unsigned 24 bits, units of 307.2MHz/224 ~= 18.31 Hz per LSB |
| 0x940 –0x9FC |  | Unused/Reserved |  |
| 0xA00 –0xA7C | 96-127 | eta I&Q channel calibration constants | 32b Floating point value  Addr, Addr+4: Chan(n) I, Chan(n) Q |
| 0xA80 -- 0xAFC |  | Unused/Reserved |  |
| 0XB00 –0xB3C | 128-143 | DAC IF Band Frequency shift LO tune word | Sets the tuning frequency of the DAC output to match the band of the DAC unconverter |
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#### Control Register Bit Definition

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| --- | --- | --- |
| **bit** | **function** | **comment** |
| 0 | RF output enable | 0 🡺 off | 1 🡺 RF output enabled |
| 1 | Reference source | 0 🡺 use ADC ref input | 1 🡺 use internal reference (not implemented, always uses internal reference) |
| 2 | Notch simulator enable | 1 🡺 enable internal notch simulator (not yet implemented) |
| 3 | White noise | 1 🡺 generate white noise in band around each output line (not yet implemented) |
| 4 | Feedback polarity | 0 🡺 normal polarity | 1 🡺 inverted |
| 5-7 | unused |  |
| 8-15 | Status mux | Selects a resonance line for which status regs 0-7 provide debug information |
| 16-23 | Debug mux setting | Selects which data sources are sent to debug streams  High 4 bits select mode:  0 🡺 f , df  1 🡺f, synch count  2 🡺 df, synch count  Low 4 bits: if <12 which resonance line  If = 15 interleave all 12 lines (low 4 bits of f, df contain channel number) |
| 24 | Ch0 band A I/Q swap | Swap I/Q datapaths on incoming 32b data stream  0: I=Din[15:0], Q=Din[31;16]  1: Q=Din[15:0], I=Din[31;16] |
| 24-31 | unused | unused |
|  |  |  |

Notes:

1. Low pass filter parameters (Config\_08):

The 32-bit register Config\_08 contains two 16-bit words which set the corner frequencies for single-pole low pass filters on two internal variables:

1.  the “frequency error calibration constant” which is generated from the S21 measured at the sideband frequencies, and must be averaged to get adequate S/N so that its noise doesn’t dominate the measurment of the line center frequency.
2. f, the frequency error as exported to the status ports, which should be low-pass filtered to prevent aliasing when being read in decimated readout.

They are both expressed as 16-bit fractions, e.g. R = 0xffff = 1.0 or R = 0x0001 = 2-16 . Each low pass filter is characterized by a time constant  = ts/R. where for f, the frequency error estimate, ts = 144/185MHz = 778 ns, while for  the sideband calibration constant ts = 8\*144/185MHz = 6.2 s.

Reasonable values are:

R = 0x0100 = 1/256 🡺 = 256\*6.2s = 1.6 ms

R = 144/decimation hence if the readout decimation rate is 1152 (~160ksps readout rate)  
then R = 1/16 and  = 256\*778ns = 12.5s .

### Status Registers

Status registers, read-only to high-level apps, provide status info from the Laser Locker module.

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| **Status Registers (Read-only)** | | | | |
| **AXI addr** | **Word** | **Function** | **Comments** | |
| 0x000 | 0 | Freq | Debug :  Select Ith line via Config 0 bits 8-15 | Frequency of 32 bits, 185MHz/231 ~11.6LSB/Hz |
| 0x004 | 1 | delta F | Freq error (32 bits, ~23LSB/Hz) |
| 0x008 | 2 | Signal amplitude | Amplitudes, 18 bits, 0x3FFFF 🡺 full scale |
| 0x00C | 3 | Reference amplitude |
| 0x010 | 4 | Minus sideband amplitude |
| 0x014 | 5 | Minus sideband reference |
| 0x018 | 6 | Plus sideband amplitude |
| 0x01C | 7 | Plus sideband reference |
| 0x020 | 8 | Im(eta) | Signed 32\_14 |
| 0x024 | 9 | Re(eta) |
| 0x028 | 10 | Im(eta) (lowpass) | Signed 32\_14 |
| 0x02c | 11 | Re(eta) (lowpass) |
| 0x030 | 12 | Synch min, max | 16 bits each | |
| 0x034-0x0ff | 13-63 | unused |  | |
| 0x100-0x17C | 64-95 | Even words Fi  Odd wordsFi | Present frequency of ith line, 32bits signed, 11.6LSB/Hz  Frequency error of ith line, 32 bits signed, 23 LSB/Hz  Note: For the 16-line FTA, there are 16 pairs of these registers | |

# To Do

Add saturation status bits, div by zero bits  
Fix white noise modulator  
Add FPGA notch

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