Xray Cryo Mux Processor

Steve Smith version 0.013  
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# Version Features:

This version intended for new RF board, ADC at 2.5 GSPS, 16 channels of processing, phi0 rate of ~1 MHz.

# Registers

The Cryo Mux Processor presently contains up to 2048 “Configuration” registers which the app can read and write, and up to 2048 “Status” registers which are read-only to the app. All registers are 32-bits wide. Registers are defined below; more registers will be defined eventually.

### Configuration Registers

The Configuration Registers are used by the app to configure and operate the FPGA. Configuration Registers are write-only to the high-level app.

|  |  |  |  |
| --- | --- | --- | --- |
| **Configuration Registers (R/W)** | | | |
| **AXI addr** | **Word** | **Function** | **Comments** |
| 0x800 | 0 | Control Register | See bit-by-bit definition below |
| 0x804 | 1 | Feedback enable | Set bit 0 to 1 to enable overall feedbacks  (each channel must be individually enabled as well) |
| 0x808 | 2 | Feedback gain | unsigned 16\_12 e.g 0x1000 = nominal gain  min nonzero gain = 1/4096, max gain = 16 |
| 0x80c | 3 | Reference delay | Compensates delay of up/down converter and cryo,  8 bits in steps of 5.4 ns, range 0 to 1.378 s |
| 0x810 | 4 | Output amplitudes | A0 (31:16) amplitude of central lines 0xffff=full scale  A1 (15:0) relative amplitudes of sidebands 0xffff=1.0  Sidebands not used for Xray det  unsigned 16\_16 |
| 0x814 | 5 | FB limit  Fsideband | (31:16) max frequency excursion for FB  Sideband offset frequency 185MHz/216 =2.8125 kHz  Sidebands not used for Xray det  per LSB |
| 0x818 | 6 | Bandwidth | Bandwidth assumed for each notch. 16 bits in increments of 185MHz/216 ~= 2.8 kHz  (functionally another feedback gain) |
| 0x81c | 7 | Synch threshold | Signed 16\_15 threshold on ADC 1 for signaling flux ramp synch when using function generator |
| 0x820 | 8 | Phase ref lowpass control  Freq Error lowpass control | wPhiRef (15:0) unsigned 16\_16  wdPhi (31:16) 1.0🡺no filtering (see Note 1 below) |
| 0x824 | 9 | MFR | MFR (15:0) #samples per Flux Ramp  @ 185MSPS/12 = 15.4 MSPS  Currently (17/Aug2017) only low 12 bits used |
| 0x828 | 10 | FeedForward Gain | unsigned 16\_4 e.g 0x10 = nominal gain  min nonzero gain = 1/16, max gain = 4095 |
| 0x82C | 11 | Flux Ramp Feedforward  Quadrature delay | Low 4 bits: Number of samples of F to delay to estimate quadrature component of Flux Ramp Phase signal. 1 LSB = 16 ticks of FPGA clock. |
| 0x830 | 12 | Sync delay | # ticks delay to synchronize to flux ramp generator  Where a tick is 12/185MHz = 64.9 ns.  IF FPGA generates synch, then synch delay is round trip time for reset to appear after demodulation  (still fuzzy concept) |
| 0x834 | 13 | Flux Ramp Phase Null | Angle of null flux ramp phase  Signed 16\_15 range +-1  Probably just latency \* frequency  0 🡺 0x0000, -pi 🡺 0xFFFF, +pi 🡺 0x7FFF |
| 0x838–0x87C | 14-31 | unused |  |
| 0x880-0x8BC | 32-47 | Upconvert freq shift for each DDC block | Unsigned 16 bit fraction of FPGA clock rate (307.2 MHz) (set to 0 for sim, set to compensated for ADC/DDC freq shift in real operation) |
| 0x8C0-0x8F8 | 48-62 | unused |  |
| 0x8FC | 63 | Command Reg | Set bit 0 to reset algorithm |
| 0x900 0x93C | 64-79 | Enable FBi  Initial Fi | Bit 24: FBeni enable ith feedback  Fi (23:0) Initial frequency of ith line, unsigned 24 bits, units of 185MHz/224 ~= 11.03 Hz per LSB |
| 0xA00 -0xA3C | 128- 143 | AFM | Amplitude of Frequency Modulation U24\_0  185MSPS/224 ~11 Hz per LSB  🡺 FM deviation of 1 MHz 🡺 ~90e3 |
| 0xB00 -0xB3C | 196-211 | Φ0 Rate | Cycles of Φ0 per sample, unsigned 16\_16 per 12/185MHz =15.4MSPS  1 MHz phi0 rate ~1/15.4 =~0.649 = 0x10A0 0000 0000 0000 |
| 0xC00 -0xC3C | 256-271 | Re(η’) | Each (I,Q) component is Fix\_32\_14  η’ is the complex number by which one multiplies Sig\*conj(Ref) and take the real part to estimate frequency error, expressed as a fraction of the FPGA clock. |
| 0xD00 -0xD3C | 320-335 | Im(η’) |
| 0xE00 -0xFFB | 384-510 | unused |  |
| 0xFFC | 511 | scratchpad | 32 bits |

#### Control Register Bit Definition

|  |  |  |
| --- | --- | --- |
| **bit** | **function** | **comment** |
| 0 | RF output enable | 0 🡺 off | 1 🡺 RF output enabled |
| 1 | Reference source | 0 🡺 use ADC ref input | 1 🡺 use internal reference (not implemented, always uses internal reference) |
| 2 | Notch simulator enable | 1 🡺 enable internal notch simulator (not yet implemented) |
| 3 | White noise | 1 🡺 generate white noise in band around each output line (not yet implemented) |
| 4 | Feedback polarity | 0 🡺 normal polarity | 1 🡺 inverted |
| 5-7 | unused |  |
| 8-15 | Status mux | Selects a resonance line for which status registers 0-15 provide debug information |
| 16-23 | Debug mux setting | Selects which data sources are sent to debug port  Bits [3:0] select resonance line to send to debug port  Bit [4] single/multiple lines to debug port:  0🡺single line to debug port  1🡺all lines mux’d to debug port (low 4 bits of f, df indicate channel number)  Bits [6:5] select mode:  0 🡺 f , df  1 🡺f, synch count  2 🡺 df, synch count |
| 24-31 | unused | unused |

Notes:

1. Low pass filter parameters (Config\_08): TO BE REVISED FOR HIGHSPEED XRAY

The 32-bit register Config\_08 contains two 16-bit words which set the corner frequencies for single-pole low pass filters on two internal variables:

1.  the “frequency error calibration constant” which is generated from the S21 measured at the sideband frequencies, and must be averaged to get adequate S/N so that its noise doesn’t dominate the measurement of the line center frequency.
2. f, the frequency error as exported to the status ports, which should be low-pass filtered to prevent aliasing when being read in decimated readout.

They are both expressed as 16-bit fractions, e.g. R = 0xffff = 1.0 or R = 0x0001 = 2-16 .

To be updated: Each low pass filter is characterized by a time constant  = ts/R. where for f, the frequency error estimate, ts = 144/185MHz = 778 ns, while for  the sideband calibration constant ts = 8\*144/185MHz = 6.2 s.

Reasonable values are:

R = 0x0100 = 1/256 🡺 = 256\*6.2s = 1.6 ms

R = 144/decimation hence if the readout decimation rate is 1152 (~160ksps readout rate)  
then R = 1/16 and  = 256\*778ns = 12.5s .

### Status Registers

Status registers, read-only to high-level apps, provide status info from the Laser Locker module.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Status Registers (Read-only)** | | | | |
| **AXI addr** | **Word** | **Function** | **Comments** | |
| 0x000 | 0 | Freq | Debug :  Select Ith line via Config 0 bits 8-15 | Frequency of 32 bits, 185MHz/231 ~11.6LSB/Hz |
| 0x004 | 1 | delta F | Freq error (32 bits, ~23LSB/Hz) |
| 0x008 | 2 | Signal amplitude | Amplitudes, 18 bits, 0x3FFFF 🡺 full scale  (no sidebands for high bandwidth feedforward case) |
| 0x00C | 3 | Reference amplitude |
| 0x010 | 4 | Minus sideband amplitude |
| 0x014 | 5 | Minus sideband reference |
| 0x018 | 6 | Plus sideband amplitude |
| 0x01C | 7 | Plus sideband reference |
| 0x020 | 8 | Im(eta) | Signed 32\_14 (eta is input for no sideband case) |
| 0x024 | 9 | Re(eta) |
| 0x028 | 10 | Im(eta) (lowpass) | Signed 32\_14 |
| 0x02c | 11 | Re(eta) (lowpass) |
| 0x030 | 12 | Im(S21) | S21 full rate | Signed 32\_31 |
| 0x034 | 13 | Re(S21) |
| 0x038 | 14 | Im(S21) (lowpass) | S21 lowpass | Signed 32\_31 |
| 0x03c | 15 | Re(S21) (lowpass) |
| 0x040 | 16 | Synch min, max |  | 16 bits each |
|  |  |  |  |  |
| 0x044-0x0ff | 17-63 | unused |  | |
| 0x100-0x | 64-85 | Even words Fi  Odd wordsFi | Present frequency of ith line, 32bits signed, 11.6LSB/Hz  Frequency error of ith line, 32 bits signed, 23 LSB/Hz | |
| 0x200-0x | 128-160 | Even words φ  Odd wordsδφ | Flux ramp phase shift (physics signal)  Instantaneous estimate of error of flux ramp phase shift | |
|  |  |  |  | |

# Operation:

Calibration

Flux ramp off

Identify line centers

Record S21 at line center, +- sideband offset frequency

Optional: sweep frequency and plot complex S21

Calculate η offline

Load η config register for each line

Turn flux ramp ON

Estimate phi0 frequency for each line in this flux ramp configuration