

Title **TinySDR**

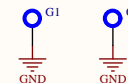
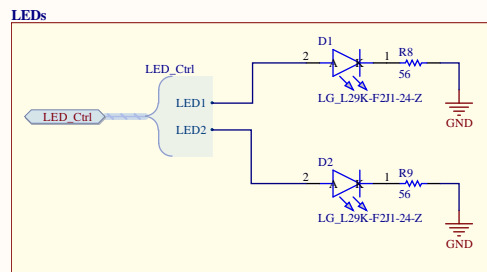
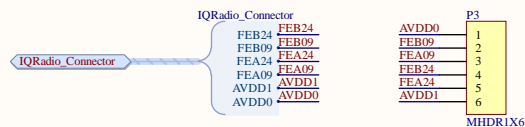
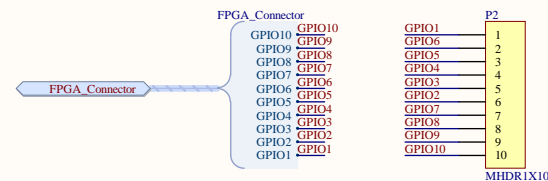
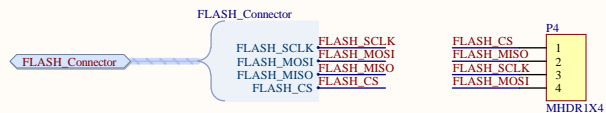
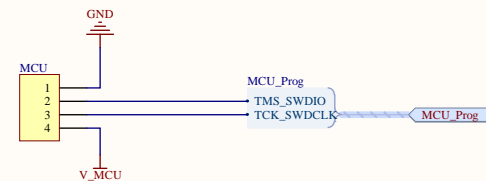
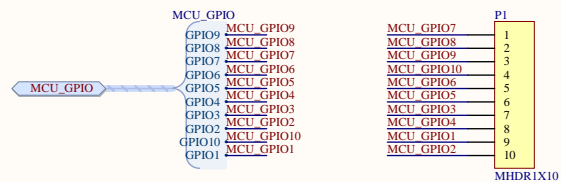
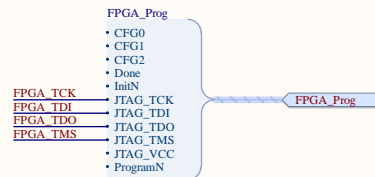
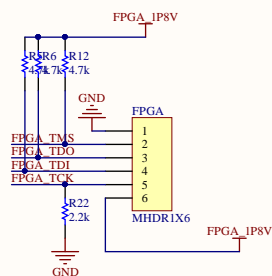
Revision: V1

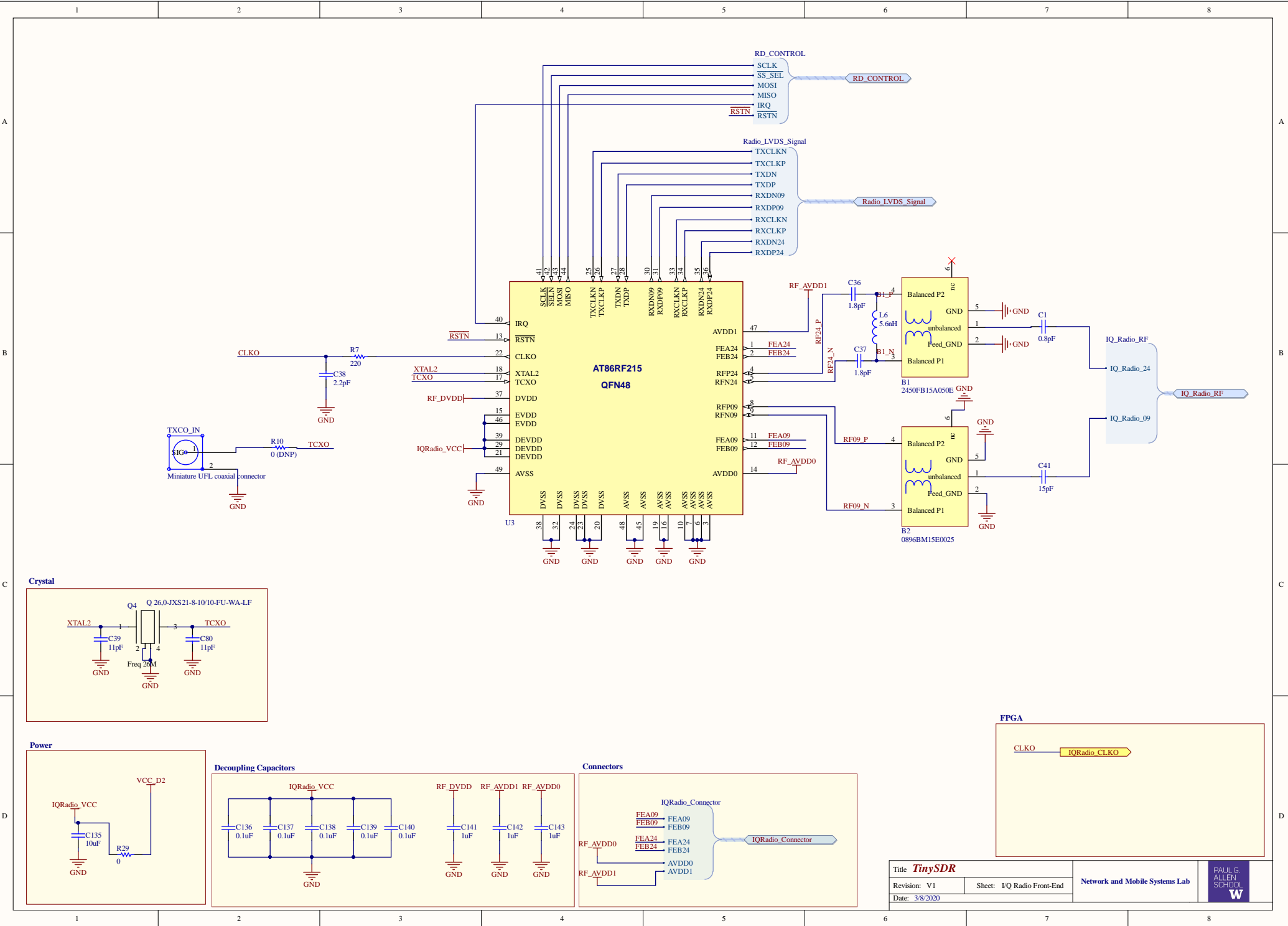
Sheet: TopLevel

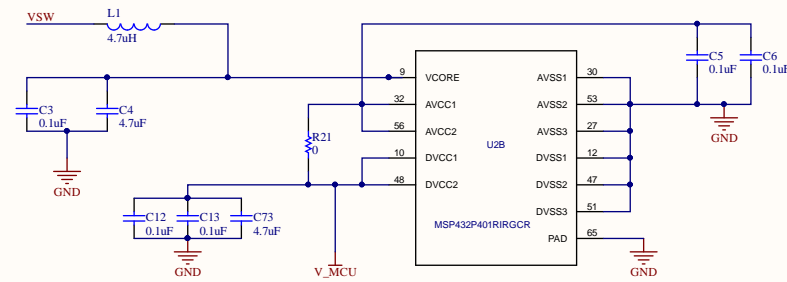
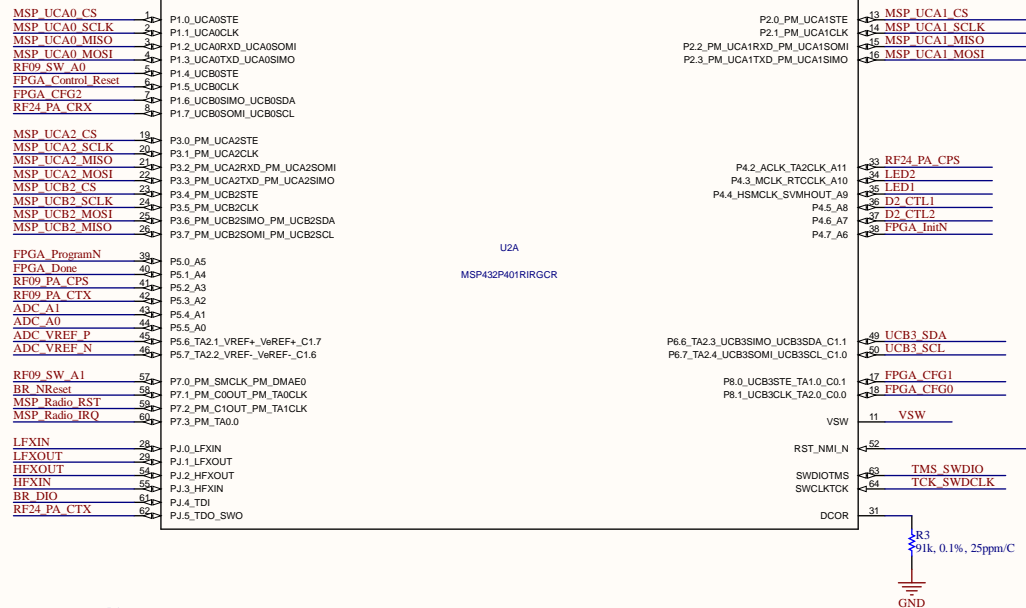
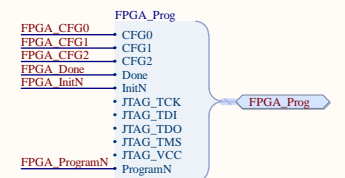
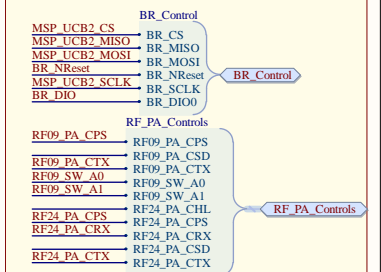
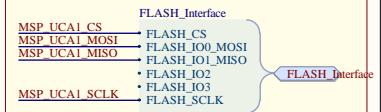
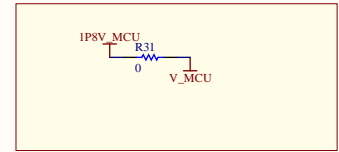
Date: 3/8/2020

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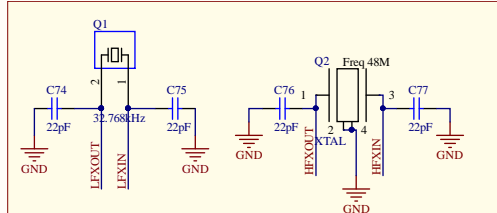
PAUL G.  
ALLEN  
SCHOOL  
W



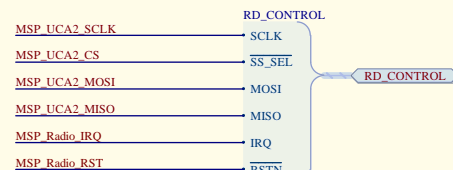




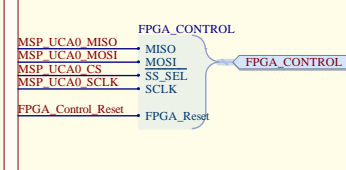
## Oscillators



## IQ\_Radio



## FPGA



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Revision: V1	Sheet: MCU		
Date: 3/8/2020			

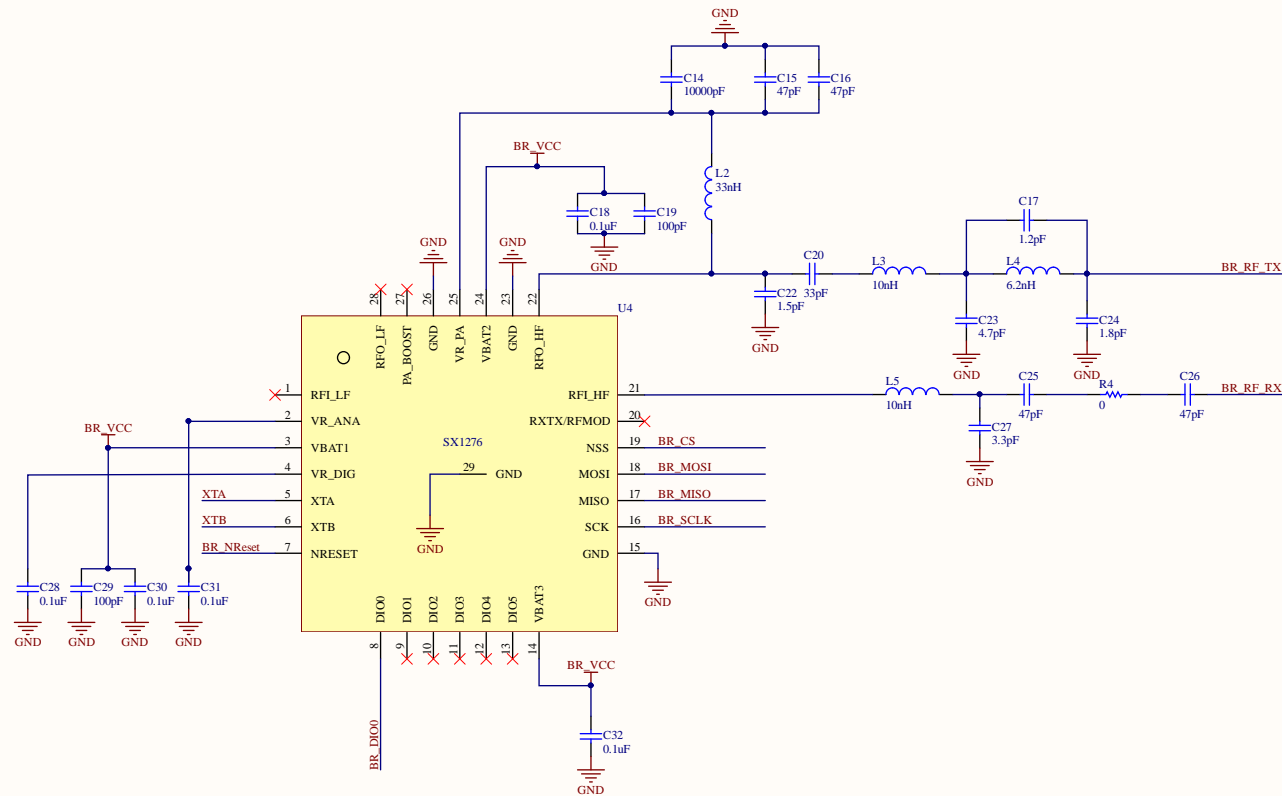
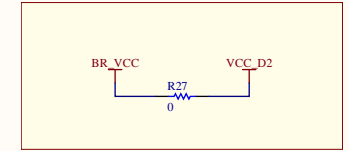


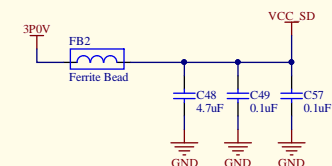
Diagram illustrating the connection of BR signals to the BR\_Control block:

- BR\_NReset
- BR\_CS
- BR\_MOSI
- BR\_MISO
- BR\_SCLK
- BR\_DIO0

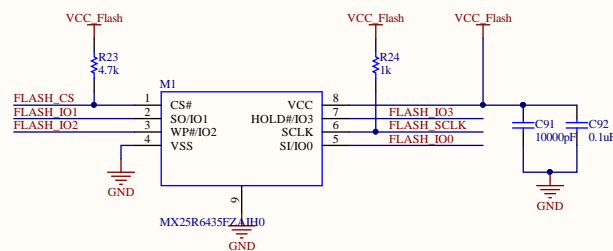
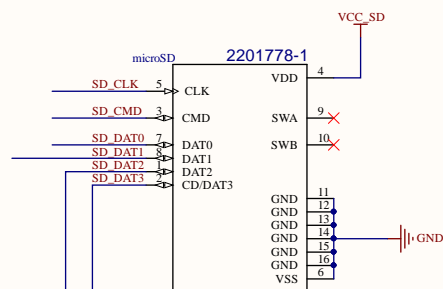
These signals are connected to the BR\_Control block, which is represented by a light blue rounded rectangle. A bracket on the right side of the diagram groups these signals under the label BR\_Control.

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## Power



VCC\_Flash  
1P8V



FLASH\_Interface  
FLASH\_CS  
FLASH\_SCLK

FLASH\_IO0  
FLASH\_IO1  
FLASH\_IO2  
FLASH\_IO3

FLASH\_Interface

SDCard\_Interface

SD\_DAT0  
SD\_DAT1  
SD\_DAT2  
SD\_DAT3  
SD\_CMD  
SD\_CLK

SDCard\_Interface

Title **TinySDR**

Revision: V1

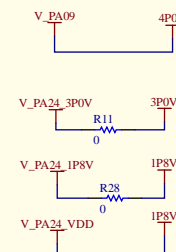
Sheet: Memories

Date: 3/8/2020

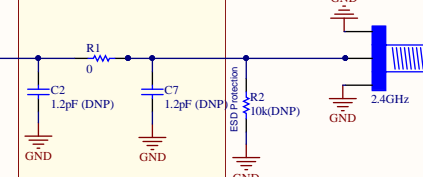
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ALLEN  
SCHOOL  
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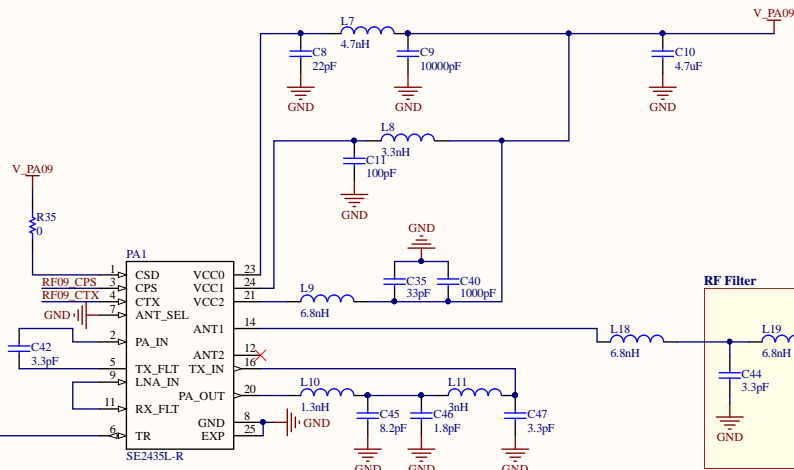
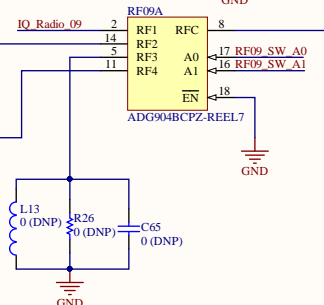
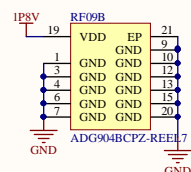
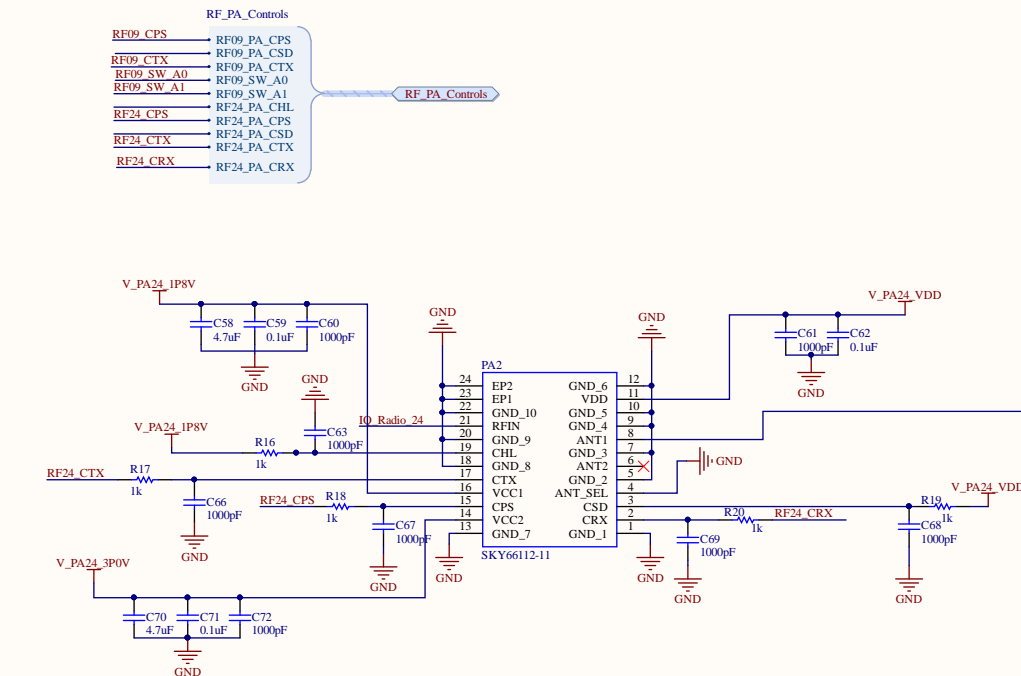
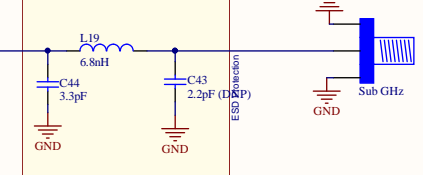
# Power

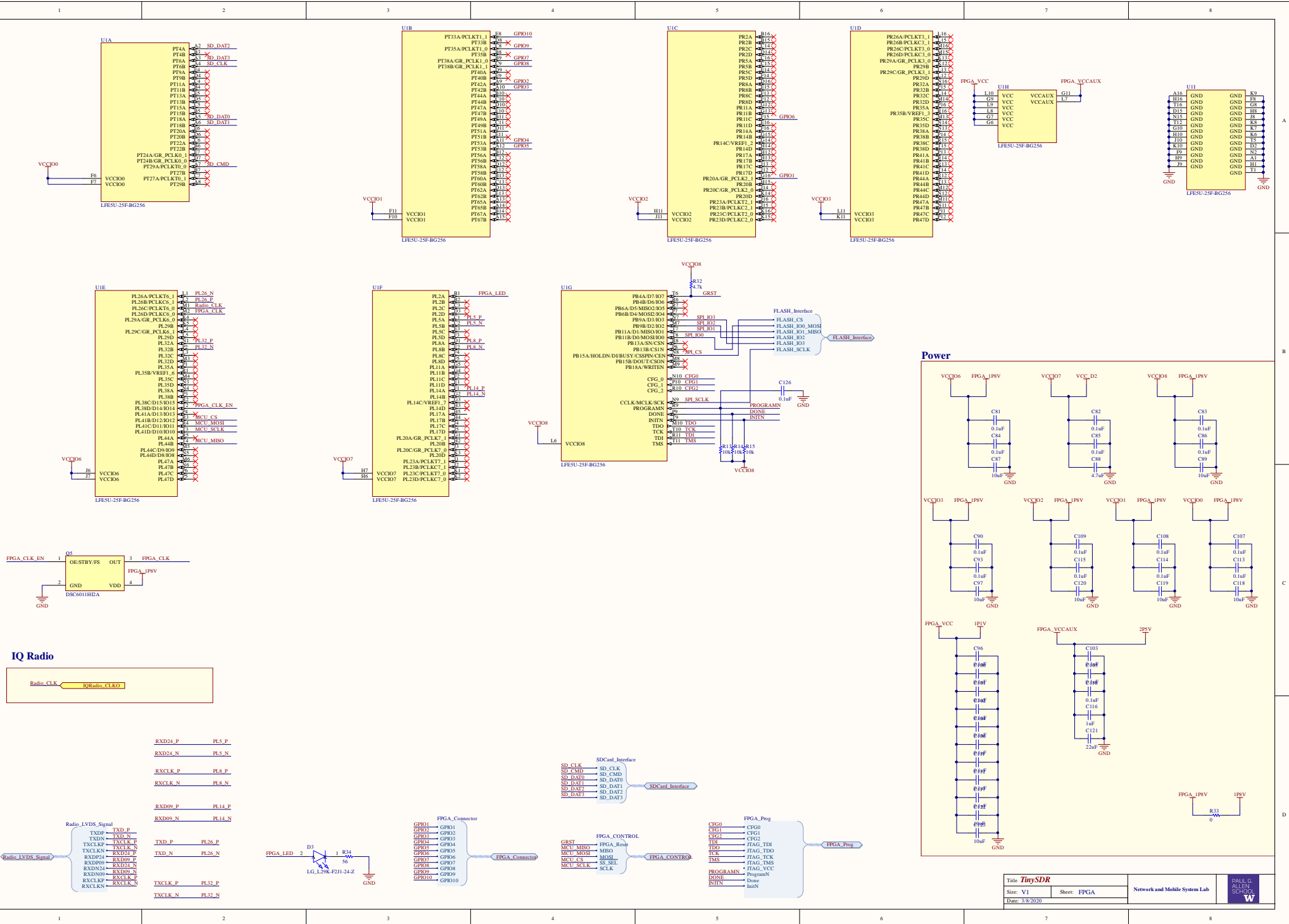


# RF Filter



# RF Filter







# Power Input

