CHAPTER 7

PROGRAMMABLE RELOAD TIMERS (PRTS)

7.1 INTRODUCTION

The Z80185 contains a two channel 16-bit Programmable Reload Timer (PRT). Each PRT channel contains a 16-bit down counter and a 16-bit reload register. The down counter can be directly read and written, and a down counter overflow interrupt can be programmably enabled or disabled. Also, if bit 3 of the IAR1B register is 1, the T_{OUT}/DREQ pin has the T_{OUT} function, and can be set high, low, or toggled when PRT channel 1 counts down to zero. Thus, PRT1 can perform programmable output waveform generation.

7.2 PRT BLOCK DIAGRAM

The PRT block diagram is shown in Figure 7-1. The two channels have separate timer data and reload registers and a common status/control register. The PRT input clock for both channels is equal to the system clock divided by 20.

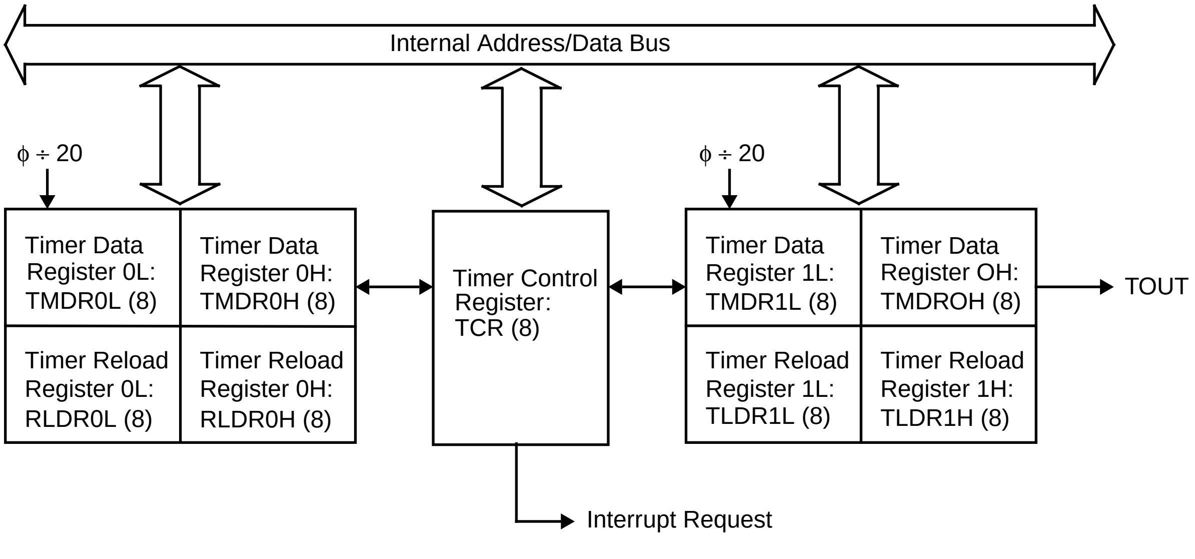
Internal Address/Data Bus
ϕ ÷ 20
ϕ ÷ 20
Timer Data Register 0L: TMDR0L (8)
Timer Data Register 0H: TMDR0H (8)
Timer Reload Register 0L: RLDR0L (8)
Timer Reload Register 0H: RLDR0H (8)
Timer Control Register: TCR (8)
Timer Data Register 1L: TMDR1L (8)
Timer Data Register OH: TMDROH (8)
Timer Reload Register 1L: TLDR1L (8)
Timer Reload Register 1H: TLDR1H (8)
TOUT
Interrupt Request

Figure 7-1. Programmable Reload Timer (PRT) Block Diagram

7.3 PRT REGISTER DESCRIPTION

7.3.1 Timer Data Register

(TMDR: I/O Address - CH0, 0DH, 0CH, CH1: 15H, 14H). PRT0 and PRT1 each have 16-bit Timer Data Registers (TMDR). TMDR0 and TMDR1 are each accessed as low and high byte registers (TMDR0H, TMDR0L and TMDR1H, TMDR1L). During RESET, TMDR0 and TMDR1 are set to FFFFH.

TMDR is decremented once every twenty clocks. When TMDR counts down to 0, it is automatically reloaded with the value contained in the Reload Register (RLDR).

TMDR is read and written by software using the following procedures. The read procedure uses a PRT internal temporary storage register to return accurate data without requiring the timer to be stopped. The write procedure requires the PRT to be stopped.

For reading (without stopping the timer), TMDR should be read in the order of lower byte - higher byte (TMDRnL, TMDRnH). The lower byte read (TMDRnL) stores the higher byte value in an internal register. The following higher byte read (TMDRnH) accesses this internal register. This procedure ensures timer data validity by eliminating the problem of potential 16-bit timer updating between the two 8-bit read. Specifically, reading TMDR in higher byte - lower byte order may result in invalid data. Note the implications of TMDR higher byte internal storage for applications which may read only the lower and/or higher bytes. In normal operation, all TMDR read routines should access both the lower and higher bytes, in that order. For writing, the TMDR down counting must be inhibited using the TDE (Timer Down Count Enable) bits in the TCR (Timer Control Register). Then, any or both higher and lower bytes or TMDR can be freely written (and read) in any order.

7.3.2 Timer Reload Register

(RLDR: I/O Address = CH0, OEH, OFH, CH1: 16H, 17H). PRT0 and PRT1 each have 16-bit Timer Reload Registers (RLDR). RLDR0 and RLDR1 are each accessed as low and high byte registers (RLDR0H, RLDR0L and RLDR1H, RLDR1L). During RESET, RLDR0 and RLDR1 are set to FFFFH.

When the TMDR counts down to 0, it is automatically reloaded with the contents of RLDR.

7.3.3 Timer Control Register (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts..

Bit	7	6	5	4	3	2	1	0
	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Figure 7-2. Timer Control Register (TCR: I/O Address = 10H)

TIF1: Timer Interrupt Flag 1 (bit 7). When TMDR1 decrements to 0, TIF1 is set to 1. This generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when the TCR is read when either byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIF0: Timer Interrupt Flag 0 (bit 6). When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read when either byte of TMDR0 is read. During RESET TIF0 is cleared to 0.

TIE1: Timer Interrupt Enable 1 (bit 5). When TIE1 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE1 is reset to 0, the interrupt request is inhibited. During RESET, TIE1 is cleared to 0.

TIE0: Timer Interrupt Enable 0 (bit 4). When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

TOC1, 0: Timer Output Control (bits 3, 2). TOC1 and TOC0 control the output of PRT1 using the multiplexed T_{OUT}/DREQ pin as shown in Table 7-1. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the T_{OUT} function is selected. By programming

TOC1 and TOC0, the T_{OUT}/DREQ pin can be forced high, low, or toggled when TMDR1 decrements to 0.

Table 7-1. Timer Output Control

TOC1	TOC0	Output	
0	0	Inhibited	The T_{OUT}/DREQ pin is not affected by the PRT.
0	1	Toggled	If bit 3 of IAR1B is 1, the T_{OUT}/DREQ pin is toggled or set low or high as indicated.
1	0	0	
1	1	1	

TDE1, 0: Timer Down Count Enable (bits 1, 0). TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0, 1) is set to 1, down counting is stopped and TMDRn can be freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn will not decrement until TDEn is set to 1.

7.4 PRT TIMING

Figure 7-3 shows timer initialization, count down, and reload timing. Figure 7-3 shows timer output (T_{OUT}/DREQ) timing.

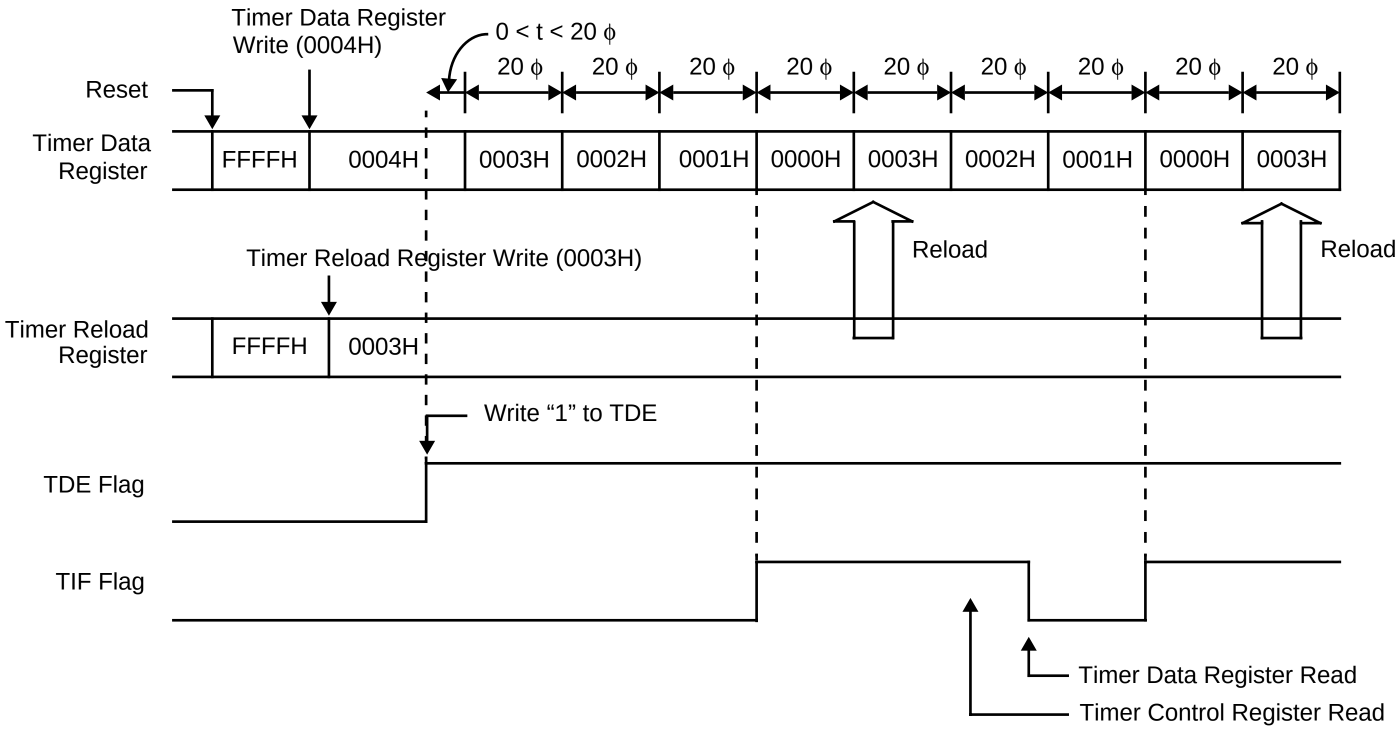

Figure 7-3. Timer Initialization, Count Down, and Reload Timing

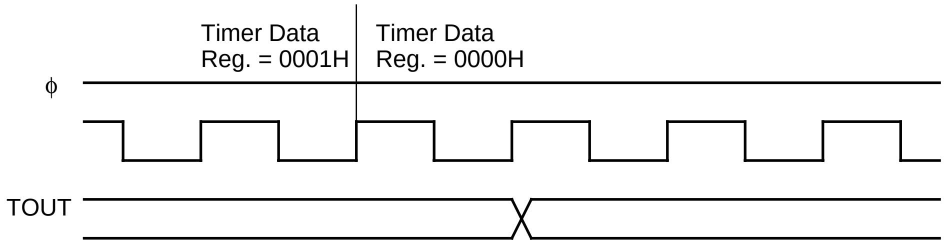

Figure 7-4. Timer Output Timing

7.5 PRT INTERRUPTS

The PRT interrupt request circuit is shown in Figure 7-5.

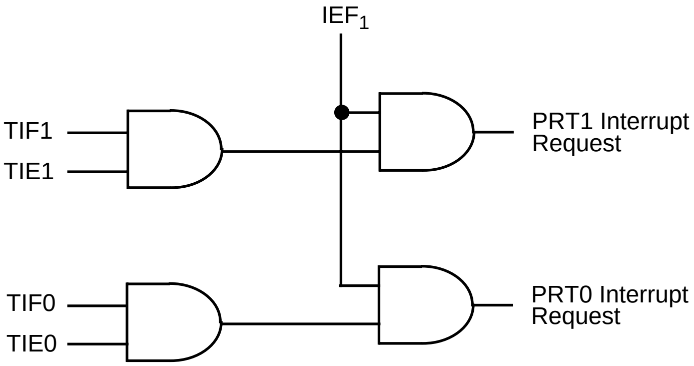

Figure 7-5. PRT Interrupt Request Generation

7.6 PRT AND RESET

During RESET, the bits in TCR are initialized as defined in the TCR register description. Down counting is stopped and the TMDR and RLDR registers are initialized to FFFFH.

7.7 PRT OPERATION NOTES

1. TMDR data can be accurately read without stopping down counting, by reading the lower (TMDRnL*) and higher (TMDRnH*) bytes in that order. Also, TMDR can be freely read or written by stopping the down counting.
2. Care should be taken to ensure that a timer reload does not occur during or between lower (RLDRnL*) and higher (RLDRnH*) byte writes. This may be guaranteed by system design/timing or by stopping down counting (with TMDR containing a non-zero value) during the RLDR updating. Similiarly, in applications in which TMDR is written at each TMDR overflow, the system/software design should guarantee that RLDR can be updated before the next overflow occurs. Otherwise, time base inaccuracy will occur.

Note: *n = 0, 1

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