
# SD UHSII PHY IP

## PCS Family Datasheet

SLDE-DS-0059 Rev. 1.8

Sep. 13, 2013

# TABLE OF CONTENTS

# FIGURES

# 1 INTRODUCTION

SD UHS-II PCS Family is SLI's Physical Coding Sublayer (PCS) IP for SD 4.0 UHS-II HOST and DEVICE. This IP is a synthesizable digital part. SLI provides this IP and Physical Media Attachment blocks (PMA) which is hard macro optimized for UHS-II HOST or DEVICE.

It supports the speed from 390Mbps to 1.56Gbps for the data rate per lane and both Full Duplex/Half Duplex modes for its operation mode. This document describes the basic specification of PCS part.

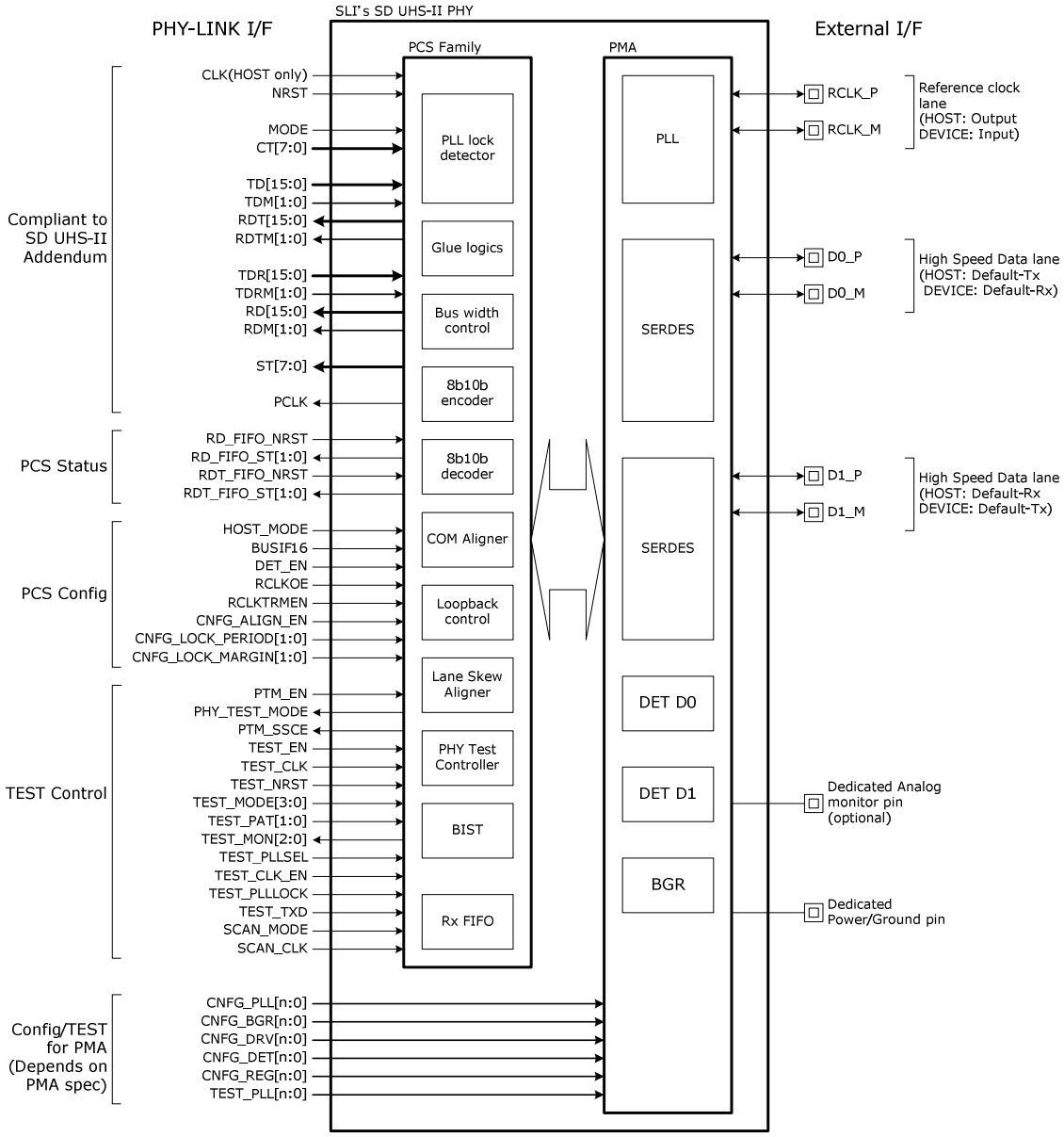


**Figure 1 Block Diagram of SD UHS-II PHY**

# 2 Features

- SD UHS-II compliant Physical Coding Sublayer for host and device
  - Compliant to the following specifications
    - “SD Specifications Part 1 Physical Layer Specification Version 4.10”
    - “SD Specifications Part 1 UHS-II Addendum Version 1.01”
- Fully-synthesizable part (Verilog HDL)
- Supports both 16bit and 8bit interface to Link layer
- Supports both Full Duplex mode and Half Duplex mode
- Power saving mode
- Various test modes (BIST, loopback, etc)
- Corresponds to all of SLI’s PMA variation

# 3 PIN DESCRIPTIONS

## 3.1 Link Interface Signals

**Table 1 Link Interface Signals**

| Pin name | Direction | Sync/ Async | Active | At Reset | Descriptions |
|---|---|---|---|---|---|
| PCLK | output | - | | | System clock for PHY-LINK I/F. |
| CLK | input | - | | | PLL reference clock (26 to 52MHz) for UHS-II HOST mode. This is used only SD UHS-II HOST with PMA for HOST. Fix to 0 while this IP works as UHS-II DEVICE with PMA for DEVICE. |
| NRST | input | Async | 0 | | System reset for PHY. |
| TD[15:0] | input | PCLK | | | TX data input for default-Tx lane. Only TD[7:0] is valid when BUSIF16=0. |
| TDM[1:0] | input | | | | TX K-line inputs for default-Tx lane. Only TDM[0] is valid when BUSIF16=0. |
| TDR[15:0] | input | | | | TX data input for default-Rx lane. Only TDR[7:0] is valid when BUSIF16=0. |
| TDRM[1:0] | input | | | | TX K-line inputs for default-Rx lane. Only TDRM[0] is valid when BUSIF16=0. |
| CT[7:0] | input | | | | PHY control signal.<br>Bit[3:0]: PINIT/PCMD(depending on MODE)<br>[When MODE=0]<br>PHY Initialization parameter in Dormant state.(PINIT)<br>bit[1:0]: Selected PHY Major Revision<br>-Reserved(set 00b for UHS156)<br>bit[3:2]: Selected Transmission Speed Range<br>00: Range A<br>(390-780 Mbps per Lane at UHS156)<br>01: Range B<br>(780-1,560 Mbps per Lane at UHS156)<br>others: Reserved<br>[When MODE=1]<br>PHY Command(PCMD)<br>0000: No Command Operation<br>0001: Enter to Loopback mode for DB Streaming<br>0011: Exit from Loopback mode for DB Streaming<br>0101: Enter to (2L-)HDIN mode(Default Tx->Rx)<br>0110: Enter to (2L-)HDOUT mode (Default Rx->Tx)<br>0111: Exit from (2L-)HD mode<br>11XX: Reserved for Vendor Unique Command<br>(Not support) |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | others: Reserved<br>Bit[5:4]: TDS[1:0]<br>state control for default-Tx lane.<br>2'b00: EIDL<br>2'b01: OFF<br>2'b10: STB<br>2'b11: VLD<br>Bit[7:6]: TDRS[1:0]<br>state control for default-Rx lane<br>2'b00: EIDL<br>2'b01: OFF<br>2'b10: STB<br>2'b11: VLD |
| MODE | input | | | | PHY power mode<br>1: Active<br>0: Dormant |
| RCLKOE | input | PCLK | 1 | | RCLK output enable<br>1: RCLK active (while PLL is locked)<br>0: RCLK is stopped (EIDL) |
| RDT[15:0] | output | PCLK | | 16'h0000 | RX data outputs for default-Tx lane.<br>Only RDT[7:0] is valid when BUSIF16=0. |
| RDTM[1:0] | output | | | 2'b00 | RX k-line outputs for default-Tx lane.<br>Only RDTM[0] is valid when BUSIF16=0. |
| RD[15:0] | output | | | 16'h0000 | RX data outputs for default-Rx lane.<br>Only RD[7:0] is valid when BUSIF16=0. |
| RDM[1:0] | output | | | 2'b00 | RX k-line outputs for default-Rx lane.<br>Only RDM[0] is valid when BUSIF16=0. |
| ST[7:0] | output | | | 8'h40 | PHY Status.<br>Bit[0]: DET<br>Amplitude detector output (asynchronous).<br>1: Differential amplitude is detected on default-Rx lane.<br>0: No differential amplitude is detected on default-Rx lane.<br>Bit[1]: LOCK<br>PLL lock status<br>1: Locked<br>0: Unlocked<br>Bit[2]: PACK<br>Acknowledge for PCMD<br>1: Ack<br>0: Not acknowledge<br>Bit[3]: ERR<br>Receive error status<br>1: Error occurs at least one lane<br>0: No error<br>Bit[5:4]: RDS[1:0]<br>RD status<br>00: EIDL<br>01: OFF<br>10: STB<br>11: VLD<br>Bit[7:6]: RDTS[1:0]<br>RDT status<br>00: EIDL<br>01: OFF<br>10: STB<br>11: VLD |

## 3.2 PCS Configuration Signals

**Table 2 Configuration Signals**

| Pin name | Direction | Sync/ Async | Active | At Reset | Descriptions |
|---|---|---|---|---|---|
| BUSIF16 | input | PCLK | 1 | | LINK-PHY Bus width select<br>1:Bus width=16bit (Recommended)<br>0:Bus width=8bit<br>This signal should be fixed at PHY startup sequence. |
| HOST_MODE | input | | 1 | | Mode select for PHY digital<br>1: PHY digital works as UHS-II HOST<br>-RCLK lane is handled as output port by this IP.<br>-D0 lane is handled as default-Tx lane by this IP<br>-D1 lane is handled as default-Rx lane by this IP<br>0: PHY digital works as UHS-II DEVICE<br>-RCLK lane is handled as input port by this IP<br>-D1 lane is handled as default-Tx lane by this IP<br>-D0 lane is handled as default-Rx lane by this IP<br>This pin shall be fixed to dedicated level on PHY TOP module provided by SLI. |
| DET_EN | input | Async | 1 | | Controls Amplitude detector on default-Rx lane<br>1: Enable<br>0: Disable(Power down)<br>LINK can set this pin to 0 for reduction of power consumption of PHY only while dormant of UHS-II HOST as required. |
| RCLKTRMEN | input | | 1 | | Controls Termination resistor on RCLK lane<br>1: Enable<br>0: Disable(Make hi-z)<br>When the card controller does not select UHS-II I/F, this signal is used for RCLK lane becomes to high impedance by LINK or upper layer. |
| CNFG_LOCK_PERIOD[1:0] | input | | | | Configuration of sampling duration for PLL lock detector.<br>2'b00 :103us@26MHz / 51.5us@52MHz<br>2'b01 :256us@26MHz / 128us@52MHz<br>2'b10 :502us@26MHz / 251us@52MHz<br>2'b11 :1004us@26MHz / 502us@52MHz<br>Note that these durations are made by frequency of CLK. |
| CNFG_LOCK_MARGIN[1:0] | input | | | | Configuration of permissible error range for PLL lock detector.<br>2'b00 :+/- 1CLK<br>2'b01 :+/- 4CLK<br>2'b10 :+/- 8CLK<br>2'b11 :+/- 15CLK |
| CNFG_ALIGN_EN | input | PCLK | 1 | | Enables Lane Skew Aligner.<br>1: Enable(Normal)<br>0: Disable |

## 3.3 Test Control Signals

**Table 3 TEST Control Signals (1/2)**

| Pin name | Direction | Sync/ Async | Active | At Reset | Descriptions |
|---|---|---|---|---|---|
| SCAN_CLK | input | - | | | SCAN shift clock input for SCAN test mode. This clock drive all F/Fs in this IP during the SCAN_MODE is 1. |
| SCAN_MODE | input | Async | 1 | | Controls SCAN Test mode of PCS.<br>1: SCAN Test enable<br>0: Normal operation |
| TEST_NRST | input | Async | | | System reset for TEST mode. |
| TEST_CLK | input | - | | | PLL reference clock for TEST mode.<br>Supply constant clock (26 to 52MHz) for using each TEST mode. |
| TEST_CLK_EN | input | Async | 1 | | Enables TEST_CLK |
| TEST_EN | input | Async | 1 | | Enables each test mode selected by TEST_MODE[3:0]. |
| TEST_PLLSEL | input | PCLK | 1 | | PLL multiplication factor select in test mode.<br>0: x15<br>1: x30 |
| TEST_PAT[1:0] | input | | | | BIST data pattern select<br>2'b00: PRBS with 8B10B coding<br>2'b01: Fixed K28.5<br>2'b10: Fixed D10.2<br>2'b11: Repeated "LIDL0" (K28.5+K28.3) |
| TEST_MODE[3:0] | input | | | | Test mode select.<br>4'b0000: Dormant Supply Current Test<br>4'b0001: Normal Supply Current Test<br>4'b0010: Differential Voltage "H" Test<br>4'b0011: Differential Voltage "L" Test<br>4'b0100: Tx Terminator Resistance Test<br>4'b0101: Rx Terminator Resistance Test<br>4'b0110: Detector Function Test<br>4'b0111: Reserved (Do not use)<br>4'b1000: Forward SERDES Loopback BIST<br>4'b1001: Backward SERDES Loopback BIST<br>4'b1010: Forward Driver Loopback BIST<br>4'b1011: Backward Driver Loopback BIST<br>4'b1100: Forward Loopback Test<br>4'b1101: Backward Loopback Test<br>4'b1110: Forward Receiver Loopback Test<br>4'b1111: Backward Receiver Loopback Test<br>For more details, see chapter 5.8. |
| TEST_PLLLOCK | input | Async | 1 | | Make LOCK signal H for test.<br>Fix to 0 while normal operation. |
| TEST_TRM_OFF | input | Async | 1 | | Disables terminator of all lanes to make high impedance state. |
| TEST_MON[2:0] | output | Async | | 2'b00 | Indicates result of the test. |
| TEST_TXD | input | PCLK | 1 | | Controls TX serial data format (for debug purpose).<br>1: MSB first<br>0: LSB first<br>Fix to 0 this signal for conforming to SD UHS-II specification. |

**Table 4 TEST Control Signals (2/2)**

| Pin name | Direction | Sync/ Async | Active | At Reset | Descriptions |
|---|---|---|---|---|---|
| PTM_EN | input | | 1 | | Enables to enter to PHY Test Mode compliant to SD UHS-II Addendum.<br>When this pin is set to 1 while HOST_MODE=0, PHY enters to the PHY Test Mode when it detects the dedicated packet automatically.<br>When this pin is set to 1 while HOST_MODE=1, PHY enters to "Slave Mode" described in SD UHS-II Addendum. |
| PHY_TEST_MODE | output | | 1 | 0 | Indicates that PHY enters to PHY Test Mode. During PHY Test Mode, this IP asserts this signal to 1. |
| PTM_SSCE | output | | 1 | 0 | Indicates that SSC enable bit which is set by TMD2[6] while PHY Test Mode.. |

## 3.4 Misc Signals

**Table 5 Misc Signals**

| Pin name | Direction | Sync/ Async | Active | At Reset | Descriptions |
|---|---|---|---|---|---|
| RD_FIFO_NRST | input | Async | 0 | | Rx FIFO reset for default-Rx lane.<br>1: Normal<br>0: Reset FIFO status and read/write pointers. |
| RDT_FIFO_NRST | input | | 0 | | Rx FIFO reset for default-Tx lane.<br>1: Normal<br>0: Reset FIFO status and read/write pointers. |
| RD_FIFO_ST[1:0] | output | PCLK | | 2'b00 | Rx FIFO status for default-Rx lane.<br>00: Normal<br>01: Almost full or empty<br>10: FIFO Overflow<br>11: FIFO Underflow |
| RDT_FIFO_ST[1:0] | output | | | 2'b00 | Rx FIFO status for default-Tx lane.<br>00: Normal<br>01: Almost full or empty<br>10: FIFO Overflow<br>11: FIFO Underflow |

## 3.5 PMA Interface Signals

**Table 6 PMA Interface Signals**

| Pin name | Direction | Sync/ Async | Active | Descriptions |
|---|---|---|---|---|
| PHY_PCLK | input | | | This is the symbol interval clock. |
| PHY_PLL_FBCK | input | | | This is the feedback clock from PLL which is used for PLL lock detection. |
| PHY_RXC | input | | | This is the reference clock for PLL from RCLK receiver. |
| PHY_RX_CLK0 | input | | | This is synchronous clock for D0 receive data from CDR. |
| PHY_RX_CLK1 | input | | | This is synchronous clock for D1 receive data from CDR. |
| PHY_TRMCAL_TRG | output | Async | 0 | Trigger of calibration for termination resistors. |
| PHY_NSLP_REG | output | | | Sleep control signal for regulator. |
| PHY_NSLP_BGR | output | | | Sleep control signal for BGR. |
| PHY_NSLP_VCO | output | | | Sleep control signal for VCO. |
| PHY_NSLP_PLL | output | | | Sleep control signal for PLL. |
| PHY_NSLP_PLLCLK | output | | | Sleep control signal for clock driver of PLL. |
| PHY_NSLP_TXC | output | | | Sleep control signal for RCLK driver. This is used for only UHS-II HOST mode. |
| PHY_NSLP_RXC | output | | | Sleep control signal for RCLK receiver. |
| PHY_NSLP_TXD0 | output | | | Sleep control signal for D0 driver. |
| PHY_NSLP_TXD1 | output | | | Sleep control signal for D1 driver. |
| PHY_NSLP_RXD0 | output | | | Sleep control signal for D0 receiver. |
| PHY_NSLP_RXD1 | output | | | Sleep control signal for D1 receiver. |
| PHY_NSLP_DET0 | output | | | Sleep control signal for D0 amplitude detector. |
| PHY_NSLP_DET1 | output | | | Sleep control signal for D1 amplitude detector. |
| PHY_TRMEN_TXC | output | | 1 | Termination resistor enable signal for RCLK driver. This is used for only UHS-II HOST mode. |
| PHY_TRMEN_RXC | output | | | Termination resistor enable signal for RCLK receiver. |
| PHY_TRMEN_TXD0 | output | | | Termination resistor enable signal for D0 driver. |
| PHY_TRMEN_TXD1 | output | | | Termination resistor enable signal for D1 driver. |
| PHY_TRMEN_RXD0 | output | | | Termination resistor enable signal for D0 receiver. |
| PHY_TRMEN_RXD1 | output | | | Termination resistor enable signal for D1 receiver. |
| PHY_TX_EIDL0 | output | PHY_PCLK | 1 | Driver output disable for D0. |
| PHY_TX_EIDL1 | output | | | Driver output disable for D1. |
| PHY_RX_EIDL0 | input | Async | 1 | Status of differential signal for D0. |
| PHY_RX_EIDL1 | input | | | Status of differential signal for D1. |
| PHY_TX_STBL1 | output | | 1 | Driver control signal for D1. |
| PHY_PLLSEL | output | | | Controls PLL multiplication ratio. |
| PHY_TX_D0[9:0] | output | PHY_PCLK | | D0 transmit data |
| PHY_TX_D1[9:0] | output | | | D1 transmit data |
| PHY_RX_D0[9:0] | input | PHY_RX_CLK0 | | D0 receive data |
| PHY_RX_D1[9:0] | input | PHY_RX_CLK1 | | D1 receive data |
| PHY_TEST_LB[1:0] | output | Async | | Test control signal for PHY internal loopback. |

# 4 Block Diagram

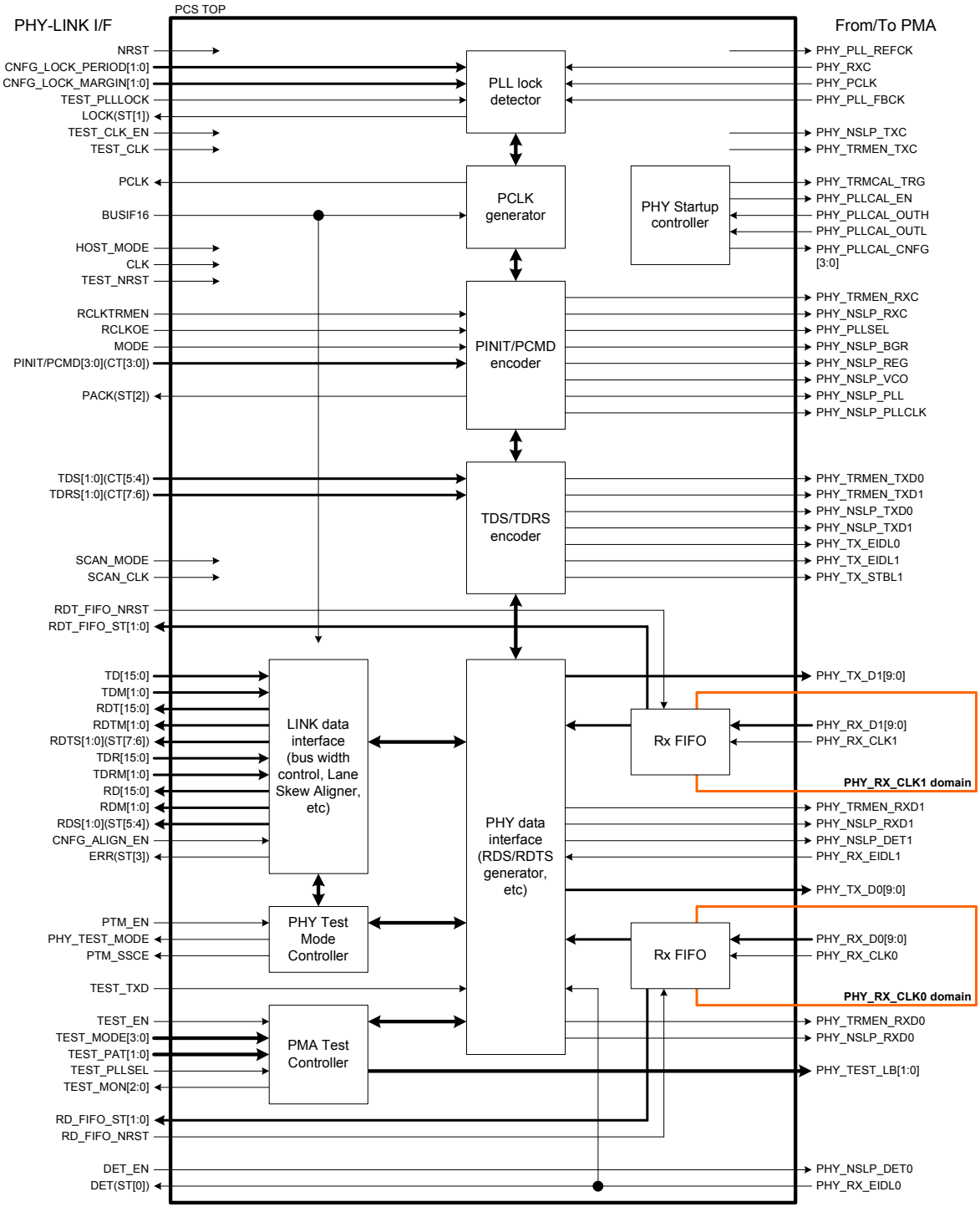


**Figure 2 PCS Block Diagram**

# 5 Functional Description

## 5.1 High Speed Data Lane (D0, D1)

This IP handles each high speed data lanes (D0 and D1) as the default-Tx/Rx lane according to the HOST_MODE pin as shown below.

**Table 7 Truth Table of Data Lane Handling**

| HOST_MODE | PCS mode | Declaration of data lane |
|---|---|---|
| 0 | UHS-II DEVICE | D0: Default-Rx lane<br>D1: Default-Tx lane |
| 1 | UHS-II HOST | D0: Default-Tx lane<br>D1: Default-Rx lane |

In both case, this IP connects following signals of PHY-LINK interface to default-Tx lane.

-TD[15:0]

-TDM[1:0]

-TDS[1:0](CT[5:4])

-RDT[15:0]

-RDTM[1:0]

-RDTS[1:0](ST[7:6])

-RDT_FIFO_NRST

-RDT_FIFO_ST[1:0]

-TEST_RDT_TRM_OFF

Similarly, this IP connects following signals of PHY-LINK interface to default-Rx lane.

-TDR[15:0]

-TDRM[1:0]

-TDRS[1:0](CT[7:6])

-RD[15:0]

-RDM[1:0]

-RDS[1:0](ST[5:4])

-RD_FIFO_NRST

-RD_FIFO_ST[1:0]

-TEST_RD_TRM_OFF

Each data lane supports half duplex (2L-HD) mode.

For more details, see chapter 5.4.

## 5.2 Reference Clock Lane (RCLK)

### 5.2.1 Overview

This IP handles RCLK lane as the input/output port according to the HOST_MODE pin as shown below.

**Table 8 Truth Table of RCLK Lane Handling**

| HOST_MODE | PCS mode | Direction of RCLK lane |
|---|---|---|
| 0 | UHS-II DEVICE | Input<br>(RCLK is supplied by RCLK receiver in PMA to this IP. The RCLK is used for generating PCLK.) |
| 1 | UHS-II HOST | Output<br>(This IP supplies PLL reference clock from CLK pin on PHY-LINK interface to PMA. The CLK is used for generating PCLK.) |

### 5.2.2 RCLK Driver/Terminator Control for UHS-II HOST

This IP controls RCLK driver and terminator while UHS-II HOST mode as following.

**Table 9 Truth Table of RCLK Driver Status**

| RCLKTRMEN | ST[1] (LOCK) | RCLKOE | Status of RCLK lane |
|---|---|---|---|
| 0 | X | X | Driver is inactivated<br>(RCLK lane is high impedance) |
| 1 | 0 | X | Driver is inactivated<br>(RCLK lane is EIDL) |
| | 1 | 0 | |
| | | 1 | Driver is activated<br>(RCLK is running) |

### 5.2.3 RCLK Receiver/Terminator Control for UHS-II DEVICE

This IP controls RCLK receiver and terminator while UHS-II DEVICE mode as following.

**Table 10 Truth Table of RCLK Receiver Status**

| NRST | RCLKTRMEN | ST[0](DET) | Status of RCLK lane |
|---|---|---|---|
| 0 | 0 | X | Receiver is inactivated<br>(RCLK lane is high impedance) |
| | 1 | X | Receiver is inactivated<br>(RCLK lane is EIDL) |
| 1 | 0 | X | Receiver is inactivated<br>(RCLK lane is high impedance) |
| | 1 | 0 | Receiver is inactivated<br>(RCLK lane is EIDL) |
| | | 1 | Receiver is activated<br>(RCLK is running) |

Note that ST[0] is asserted by receiving STB.L on D0 lane.

## 5.3 Symbol Coding

This IP includes an 8b/10b symbol coder and decoder which comply with ANSI X3.230-1994, clause 11 and also IEEE 802.3z, 36.2.4.

For more details about coding rule, refer to SD UHS-II Addendum.

## 5.4 PHY-LINK Interface

### 5.4.1 MODE and Power Consumption of PHY

MODE is used for controlling power consumption of PHY.

When MODE is turn to “L”, all of components in PHY analog is inactive except DET. Also DET can be inactive by DET_EN pin as needed in only UHS-II HOST mode.

**Table 11 Truth Table of PHY Power Mode**

| Components of PHY Analog | Dormant (MODE=0) | Active (MODE=1) | Note |
|---|---|---|---|
| Regulator | Inactive | Active | |
| BGR | | | |
| VCO | | | |
| PLL | | | |
| RCLK Driver/Receiver | Inactive (until DET=1) | | |
| Receiver for default-Rx lane | Inactive | Depends on RDS | |
| Receiver Terminator for default-Rx lane | Depends on RDS | | |
| Amplitude Detector for default-Rx lane | DET_EN=1:Active DET_EN=0:Inactive | | While UHS-II DEVICE mode (HOST_MODE=0), DET_EN should be set to 1 even if PHY enters to Dormant. |
| Driver sleep for default-Rx lane | Inactive | Active | |
| Driver output enable for default-Rx lane | Disable | Depends on TDRS | |
| Driver Terminator for default-Rx lane | Depends on TDRS | | |
| Receiver for default-Tx lane | Inactive | Depends on RDTS | |
| Receiver Terminator for default-Tx lane | Depends on RDTS | | |
| Amplitude Detector for default-Tx lane | Inactive | | |
| Driver sleep for default-Tx lane | Inactive | Active | |
| Driver output enable for default-Tx lane | Disable | Depends on TDS | |
| Driver Terminator for default-Tx lane | Depends on TDS | | |

When MODE is turned to 1, common components in PHY analog are active, but components of related each data lane are depends on the state of data lane..

### 5.4.2 PCLK

PCLK is used for synchronous clock of PHY-LINK interface.

The frequency of PCLK depends on PLL status and/or bus width setting as shown below.

**Table 12 Truth Table of PCLK**

| Status/setting | PLLLOCK | BUSIF16 | PCLK |
|---|---|---|---|
| PLL is unlocked | 0 | x | RCLK or CLK (Depends on HOST_MODE) |
| PLL is locked<br>Bus width = 16-bit | 1 | 1 | 1/20 * data rate (78MHz max.) |
| PLL is locked<br>Bus width = 8-bit | | 0 | 1/10 * data rate (156MHz max.) |

### 5.4.3 PINIT/PCMD/PACK

PINIT is used for selecting transmission speed range during Dormant state (MODE=0).

This IP supports only Range A and Range B.

PACK is used for acknowledge of PCMD. When PHY completes switching internal circuit after PCMD input from LINK, PHY asserts PACK. PCMD should keep the command until PACK is asserted from PHY.

PCMD is used for selecting PHY command operation during PHY is activated (MODE=1).

This IP supports following commands.

**Table 13 Supported PCMDs**

| PCMD[3:0] | Description |
|---|---|
| 4'b0000 | No Command Operation |
| 4'b0001 | Enter to Loopback mode for DB streaming<br>(PHY guarantees disparity continuity of stream) |
| 4'b0011 | Exit from Loopback mode for DB streaming<br>(PHY guarantees disparity continuity of stream) |
| 4'b0101 | Enter to 2L-HDIN mode |
| 4'b0110 | Enter to 2L-HDOUT mode |
| 4'b0111 | Exit from 2L-HD mode |

Other commands are not supported in this IP, so, when PHY received these command, PHY works as "No Command Operation" and does not assert PACK.

### 5.4.4 TD/TDM/TDS

TD/TDM/TDS are used for controlling the transmitting data and driver of default-Tx lane.

The default-Tx lane is controlled by Link via these signals according to the following table.

**Table 14 Truth Table of Default-Tx Lane**

| NRST | TDS[1:0] | TD[15:0] | TDM[1:0] | Line State | Driver / Serializer | Driver Output | Driver Terminator |
|---|---|---|---|---|---|---|---|
| 0 | Any | Any | Any | EIDL (DIF_PD) | Inactive | Disable | Enable |
| 1 | 2'b00 | Any | Any | EIDL (DIF-PD) | Active | Disable | Enable |
| | 2'b10 | bit[0]=0, bit[15:1]: Any | Any | STB.L (DIF-L) | | Enable | |
| | | bit[0]=1, bit[15:1]: Any | | STB.H (DIF-H) | | Enable | |
| | 2'b11 | Any | Any | VLD (depends on TD/TDM) | | Disable | |
| | 2'b01 | Any | Any | OFF (DIF-Z) | | Disable | Disable |

### 5.4.5 RDT/RDTM/RDTS

RDT and RDTM are used for receiving the data. RDTS indicates the PHY receiver status of default-Tx lane as shown below.

**Table 15 Details of RDTS**

| NRST | Line State | RDTS [1:0] | RDT [15:0] | RDTM [1:0] | ERR | Receiver / CDR | Receiver Terminator | Amplitude Detector |
|---|---|---|---|---|---|---|---|---|
| 0 | Any | 2'b01 | 00H | 2'b00 | 0 | Inactive | Disable | Inactive |
| 1 | OFF (FD) | 2'b01 | 00H | 2'b00 | 0 | | | |
| | EIDL | 2'b00 | 00H | 2'b00 | 0 | | Enable | Active |
| | STB.L | 2'b10 | 00H | 2'b00 | 0 | Active | | |
| | STB.H | | 01H | 2'b00 | 0 | | | |
| | -8B10B decode error happens before VLD state after STB.L. or -8B10B decode error happens at VLD state (See Note 1) | | Note-2 | | 1 | | | |
| | VLD (RDT/RDTM are depend on receiving data.) | 2'b11 | 8B10B decoded symbol | | 0 | | | Inactive |
| | Disparity error happens during VLD state. (RDT/RDTM are depend on decoded result.) | | | | 1 | | | |

Note 1)When 8B10B decode error happens at VLD state, RDTS is turned to STB and ERR is asserted until symbol re-lock. When PHY detects symbol re-lock, RTDS is turned to VLD and ERR is negated.

Note 2) When PHY detects 8B10B decode error, RDT indicates 00H, and RDTM indicates 1'b0.

For example, when 8B10B decode error happens at receiving MSB symbol of 16-bit lane, and LSB symbol is correct, RDT/RDTM indicates each symbol as following;

RDT = 16'h00xx , RDTM = 2'b0x ("x": depends on decoded result)

Conditions of RDTS transition are shown below.

**Table 16 State Transition of RDTS**

| Current state | Next State | | | |
|---|---|---|---|---|
| | **EIDL** | **OFF** | **STB** | **VLD** |
| **EIDL** | - | PACK for Exit from HDIN | Detects STB.L | Never |
| **OFF** | Never | - | PACK for Enter to HDIN | Never |
| **STB** | End of STB.H receiving | Never | - | Symbol (re)lock |
| **VLD** | Never | Never | 8B10B decode error / STB.H | - |

### 5.4.6 TDR/TDRM/TDRS

These signals are used for controlling the transmitting data and driver of default-Rx lane.

The default-Rx lane is controlled by Link via these signals according to the following table.

**Table 17 Truth Table for Default-Rx Lane (Driver)**

| NRST | TDRS [1:0] | TDR [15:0] | TDRM [1:0] | Line State | Driver / Serializer | Driver Output | Driver Terminator |
|---|---|---|---|---|---|---|---|
| 0 | Any | Any | Any | OFF (DIF-Z) | Inactive | Disable | Disable |
| 1 | 2'b00 | Any | Any | EIDL (DIF-PD) | Active | Disable | Enable |
| | 2'b10 | bit[0]=0, bit[15:1]: Any | Any | STB.L (DIF-L) | | Enable | |
| | | bit[0]=1, bit[15:1]: Any | | STB.H (DIF-H) | | Enable | |
| | 2'b11 | Any | Any | VLD (depends on TD/TDM) | | Disable | |
| | 2'b01 | Any | Any | OFF (DIF-Z) | | Disable | Disable |

### 5.4.7 RD/RDM/RDS

RD and RDM are used for receiving the data. RDS indicates the PHY receiver status of default-Rx lane as shown below.

**Table 18 Details of RDS**

| NRST | Line State | RDS [1:0] | RD [15:0] | RDM [1:0] | ERR | Receiver / CDR | Receiver Terminator | Amplitude Detector |
|---|---|---|---|---|---|---|---|---|
| 0 | Any | 2'b01 | 00H | 2'b00 | 0 | Inactive | Enable | Active (Note-3) |
| 1 | OFF (2L-HDOUT) | 2'b01 | 00H | 2'b00 | 0 | | Disable | Inactive |
| | EIDL | 2'b00 | 00H | 2'b00 | 0 | | Enable | Active (Note-3) |
| | STB.L | 2'b10 | 00H | 2'b00 | 0 | Active | | |
| | STB.H | | 01H | 2'b00 | 0 | | | |
| | -8B10B decode error happens before VLD state after STB.L. or -8B10B decode error happens at VLD state (See Note 1) | | Note-2 | | 1 | | | |
| | VLD (RDT/RDTM are depend on receiving data.) | 2'b11 | 8B10B decoded symbol | | 0 | | | Inactive |
| | Disparity error happens during VLD state. (RDT/RDTM are depend on decoded result.) | | | | 1 | | | |

Note 1)When 8B10B decode error happens at VLD state, RDS is turned to STB and ERR is asserted until symbol re-lock. When PHY detects symbol re-lock, RDS is turned to VLD and ERR is negated.

Note 2) When PHY detects 8B10B decode error, RD indicates 00H, and RDM indicates 1'b0.

For example, when 8B10B decode error happens at receiving MSB symbol of 16-bit lane, and LSB symbol is correct, RD/RDM indicates each symbol as following;

RD = 16'h00xx , RDM = 2'b0x ("x" : depends on decoded result)

Note-3) Only while dormant of UHS-II HOST, the amplitude detector can be inactivated by setting DET_EN to 0 as required. But in other case, LINK always shall set DET_EN to 1.

Conditions of RDS transition are shown below.

**Table 19 State Transition of RDS**

| Current state | Next State | | | |
|---|---|---|---|---|
| | **EIDL** | **OFF** | **STB** | **VLD** |
| **EIDL** | - | PACK for Enter to HDOUT | Detects STB.L | Never |
| **OFF** | Never | - | PACK for Exit from HDOUT | Never |
| **STB** | End of STB.H receiving | Never | - | Symbol (re)lock |
| **VLD** | Never | Never | 8B10B decode error STB.H | - |

### 5.4.8 Error Handling

Basically, PHY-LINK interface of this IP is compliant with SD UHS-II Addendum Appendix-F.

And when PHY receives the packet which violates to the spec from HOST as shown below, this IP handles it as follows.

**Table 20 Error Handling Table**

| Item | Definition By Spec | Handling by this IP | Note |
|---|---|---|---|
| STB.H duration (T_EIDL_ENTRY) | Fixed 4SI | -When this IP receives STB.H at least 2SI, this IP converts STB.H status as 4SI period.<br>-When this IP receives STB.H longer than 5SI, this IP converts STB.H status as 4SI period. | |

# 5.5 Lane Skew Aligner for 2L-HDIN

## 5.5.1 Overview

This IP includes lane skew aligner for 2L-HDIN mode. This function guarantees synchronism of the packet from SDB to EDB between RD/RDM and RDT/RDTM, even if skew occurs between D0 and D1 lane by input data jitter, etc.

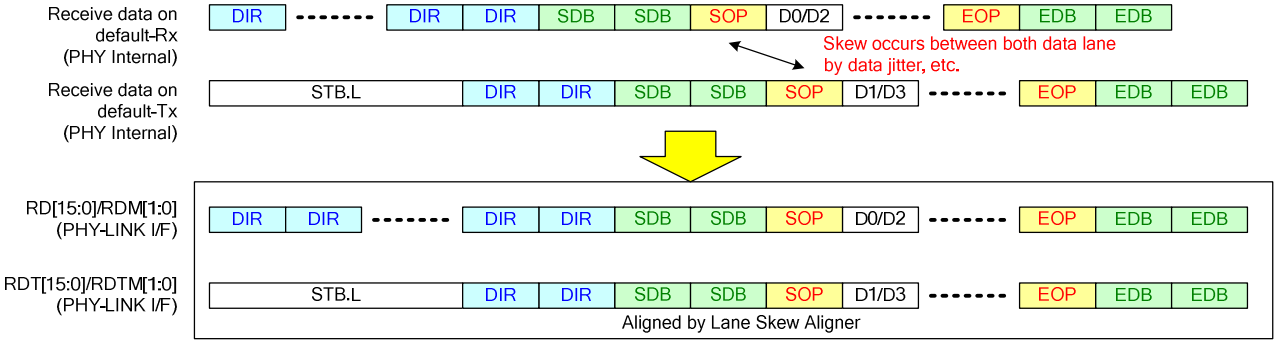


**Figure 3 Functional Overview of Lane Skew Aligner**

## 5.5.2 Related Pins

Related pins of this function are shown below.

-CNFG_ALIGN_EN: Configuration of bypassing lane skew aligner.

This is used for debug purpose, fix to 1 while using PHY.

### 5.5.3 Block Diagram

Block diagram of this component is shown below.

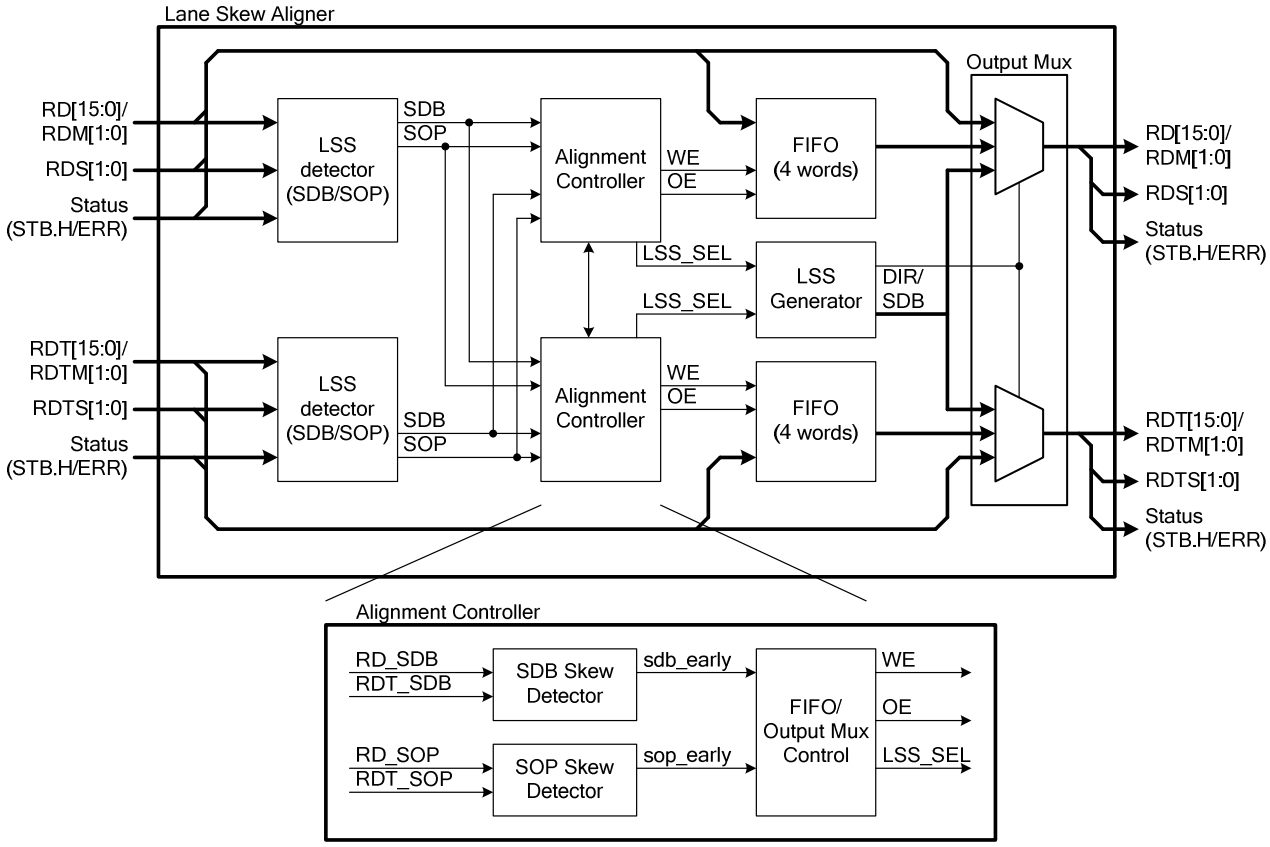


**Figure 4 Block Diagram of Lane Skew Aligner**

This module monitors SDB/SOP LSS on each data lane during 2L-HDIN mode.

When skew of LSS on between both lanes is detected, this module stores the packet which is started from SDB/SOP on faster lane into the buffer until SDB/SOP is received on another lane, and inserts DIR/SDB LSS onto faster lane as output data.

When SDB/SOP is detected on later lane, this module outputs stored packet from the buffer.

### 5.5.4 Error Handling

Regarding SD4.0 UHS-II spec, LINK shall handles following packet as the “No error” at 2L-HDIN.

-Includes at least one SDB

-Includes one SOP

Therefore, this module aligns all of “No error” packets even if corrupted symbols are included in received packet.

When receiving packet has corrupted symbols, lane skew aligner output the packet according to following table.

**Table 21 Error Handling Table for Lane Skew Aligner**

| Lane | 1’st SDB | 2’nd SDB | SOP | Result |
|---|---|---|---|---|
| D0 | **Any** | **Any** | **SOP** | Aligned |
| D1 | **Any** | **Any** | **SOP** | |
| | | | | |
| D0 | **SDB** | **Any** | **Any** | Aligned |
| D1 | **SDB** | **Any** | **Any** | |
| | | | | |
| D0 | !SDB | Any | !SOP | Not aligned<br>(This case is handled as the error by LINK) |
| D1 | Any | Any | Any | |
| | | | | |
| D0 | Any | Any | Any | Not aligned<br>(This case is handled as the error by LINK) |
| D1 | !SDB | Any | !SOP | |

1) “!SOP” and “!SDB” indicates corrupted symbols.

### 5.5.5 Example Timing Diagram

Example timing diagrams are shown below.

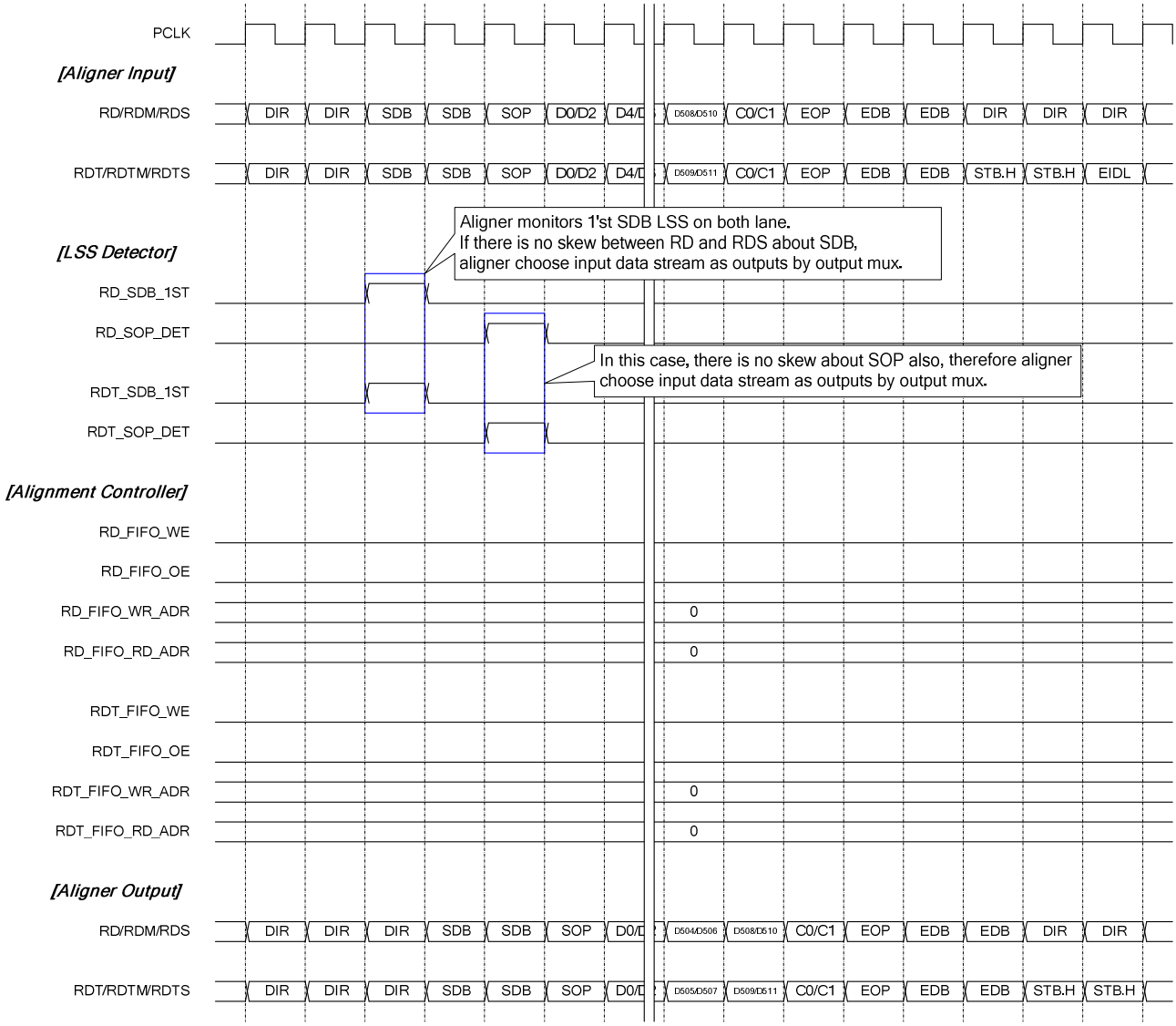


**Figure 5 Example Timing (No Skew)**

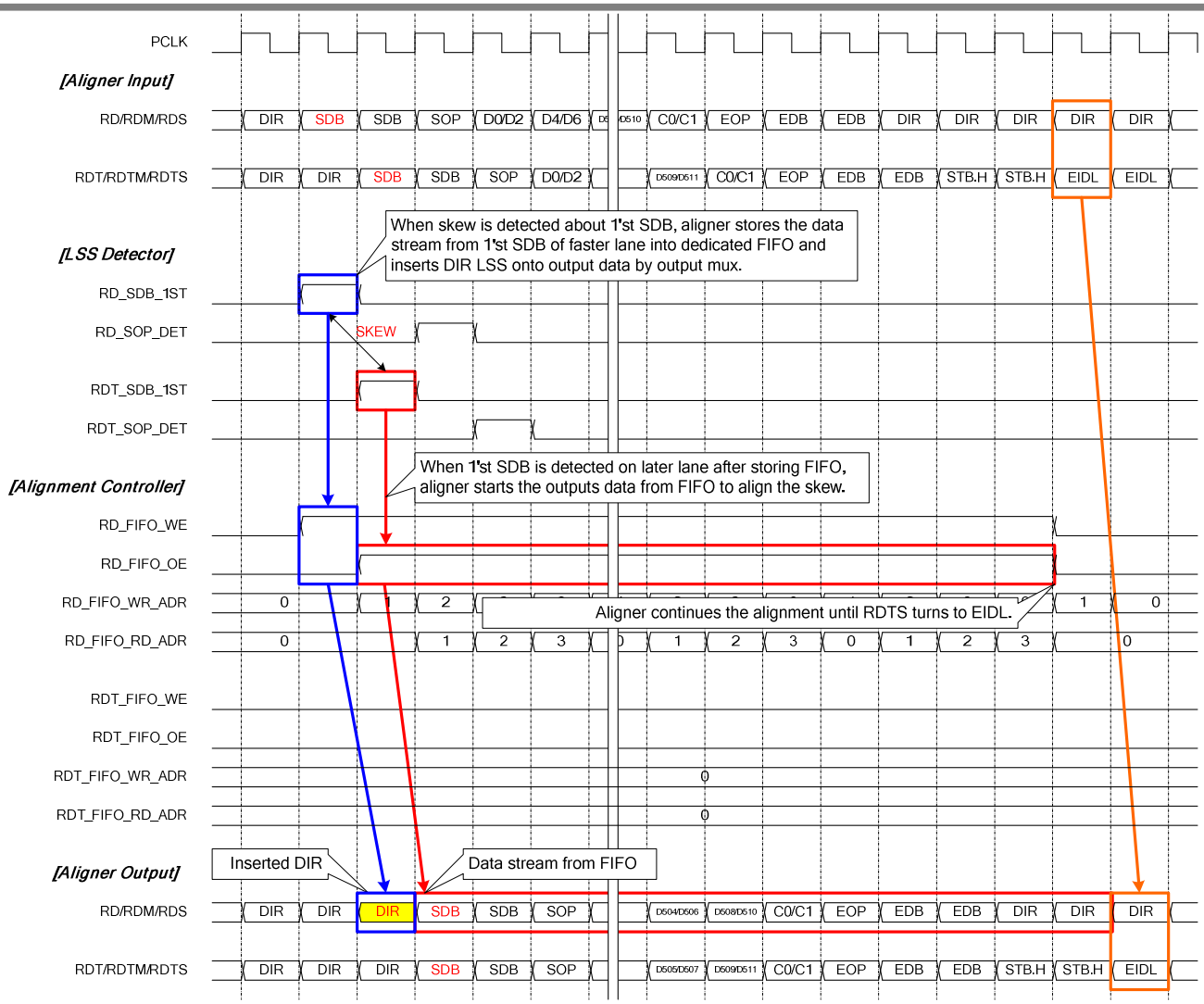


**Figure 6 Example Timing (with Skew)**

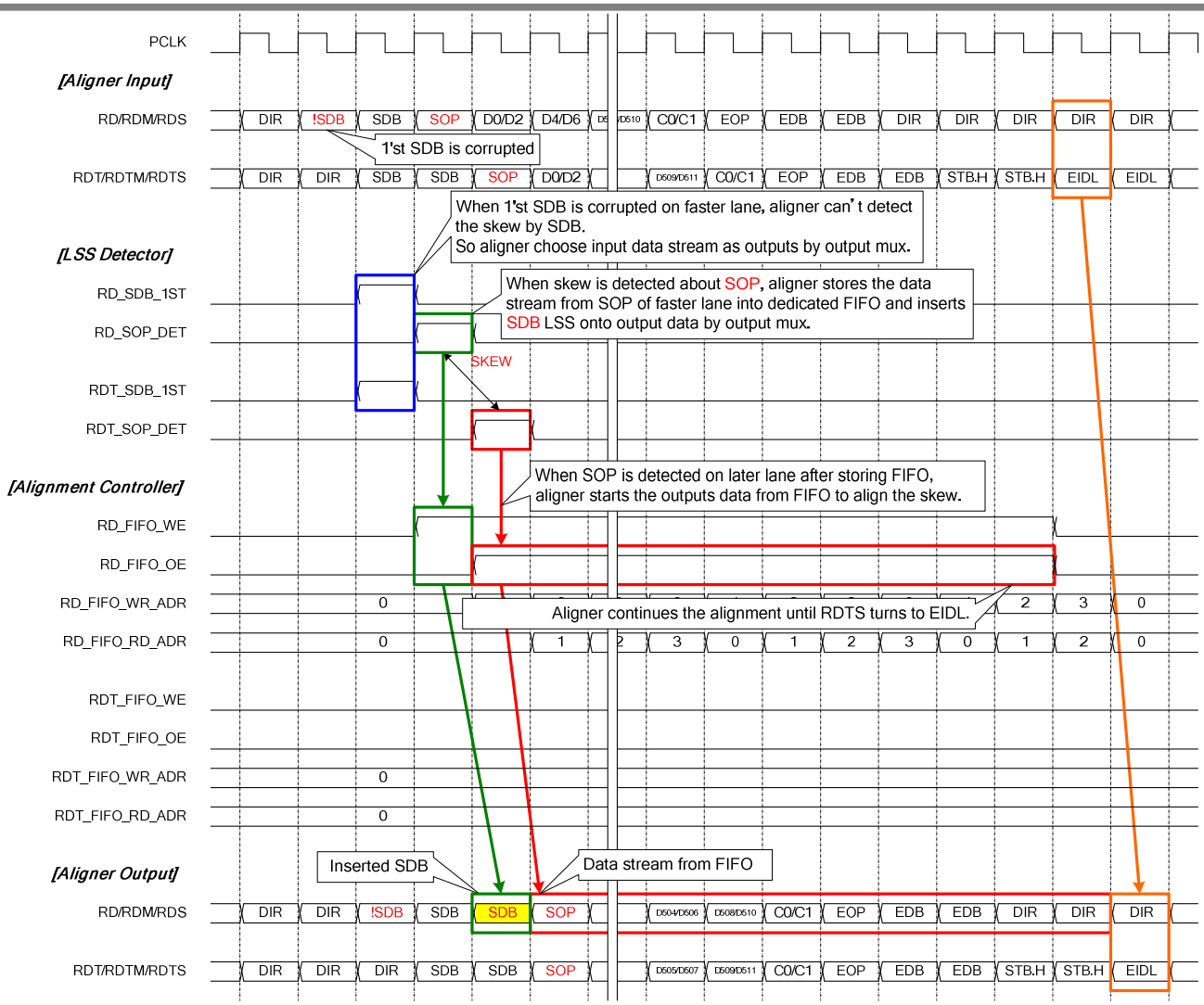


**Figure 7 Example Timing (with Skew, 1'st SDB is corrupted on faster lane)**

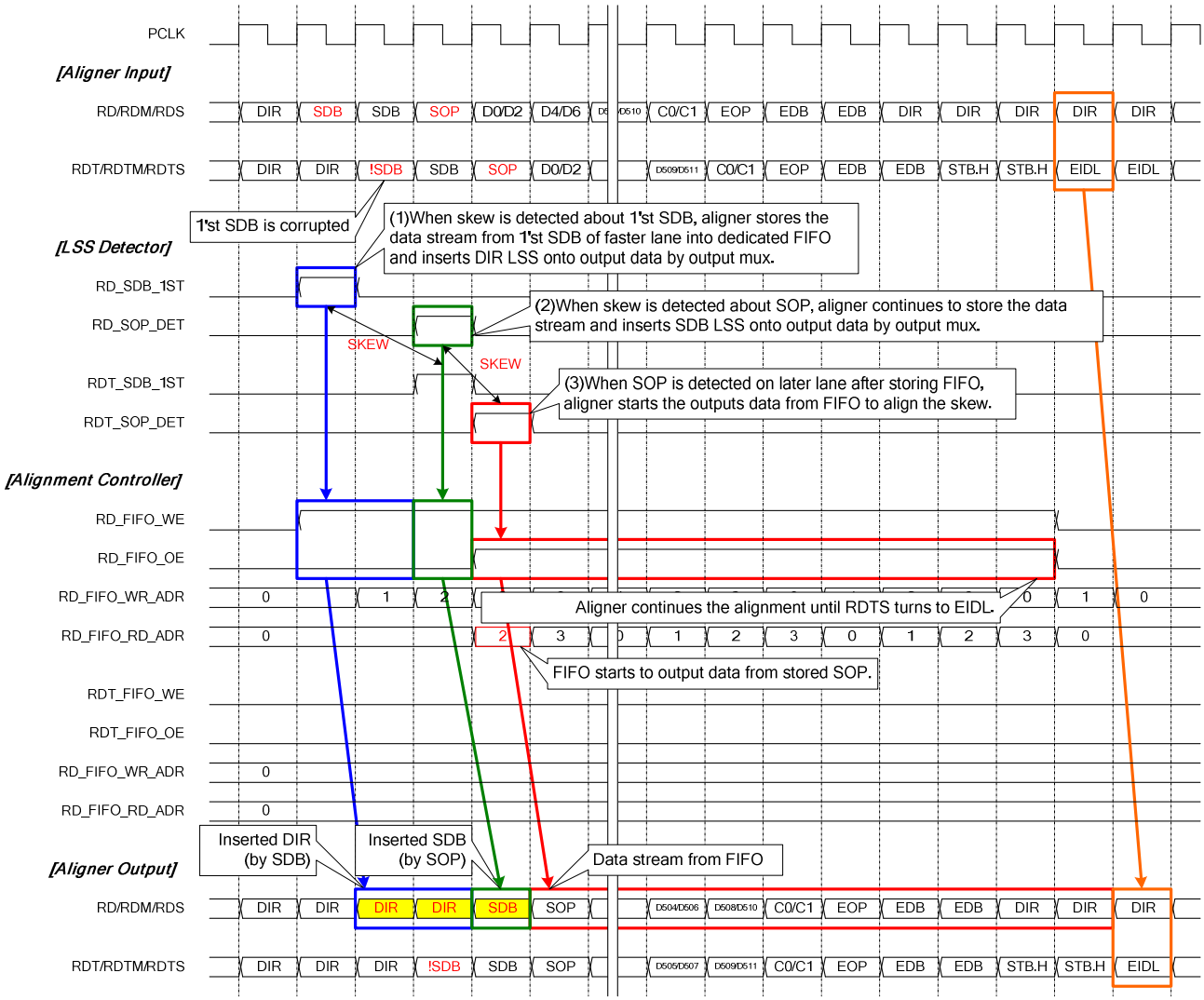


**Figure 8 Example Timing (with Skew, 1'st SDB is corrupted on later lane)**

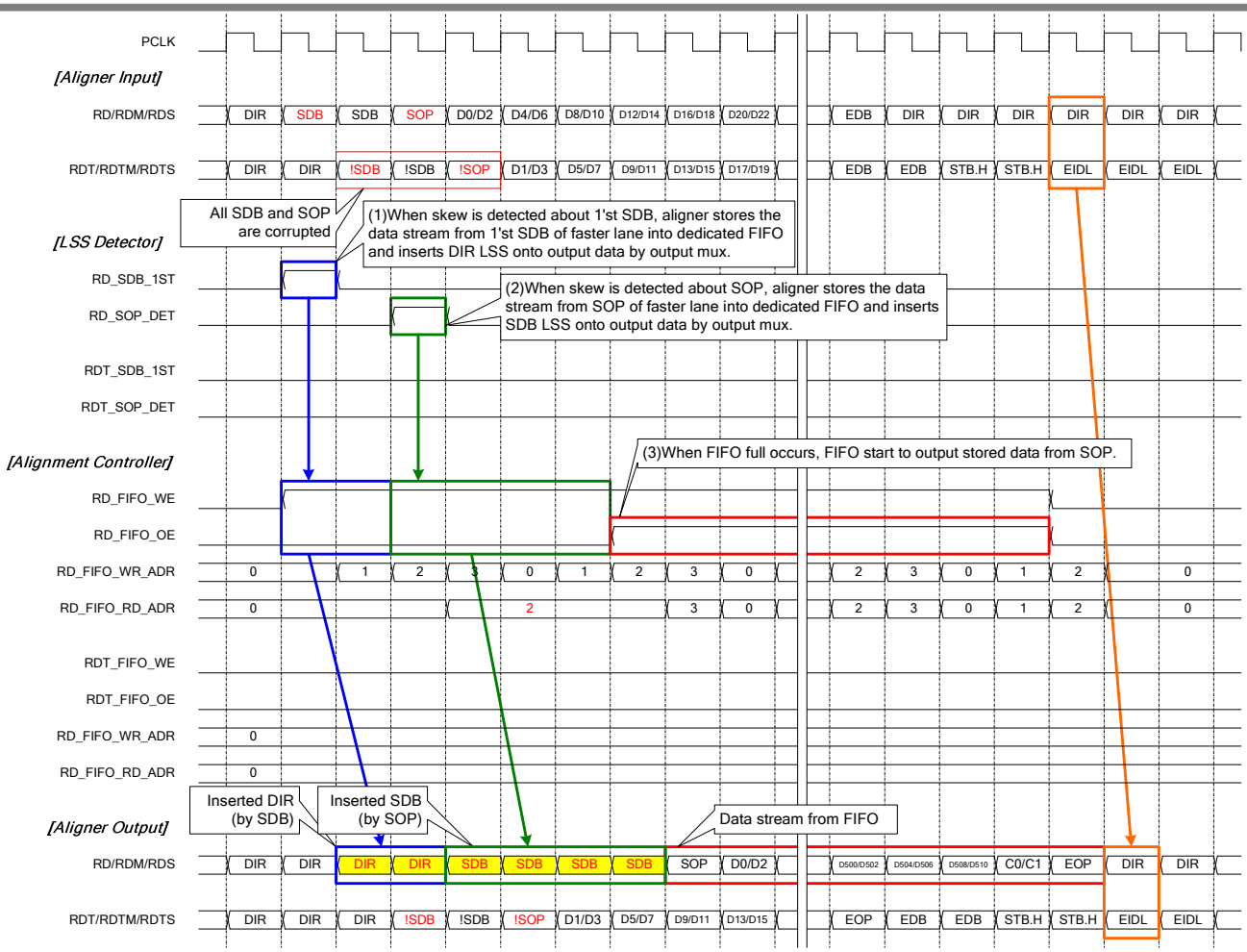


**Figure 9 Example Timing (with Skew, All LSSes are corrupted on later lane)**

In this case, the packet has no SOP and SDB. Therefore aligner does not align the packet because this packet is handled by LINK as the error.

## 5.6 PLL Lock Detector

### 5.6.1 Overview

This IP includes PLL lock detector. This function provides lock status of PLL to LINK layer.

This block monitors frequency of PHY_PLL_FBCK while PHY is activated (MODE=1), and it asserts LOCK signal (ST[1]) when both frequency will be same between PHY_PLL_FBCK and PLL reference clock (CLK or RCLK).

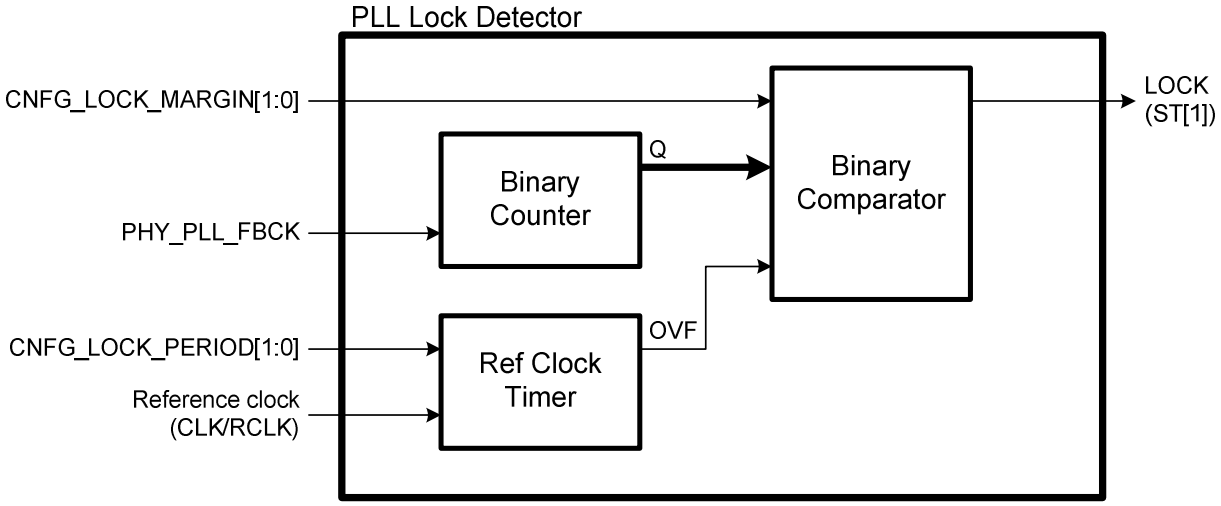


**Figure 10 Block Diagram**

### 5.6.2 Related Pins

Related pins of this function are shown below.

**Table 22 Description of Related Pins**

| Name | Description |
|---|---|
| CNFG_LOCK_PERIOD[1:0] | Configuration of sampling duration for PLL lock detector.<br>2'b00 :103us@26MHz / 51.5us@52MHz<br>2'b01 :256us@26MHz / 128us@52MHz<br>2'b10 :502us@26MHz / 251us@52MHz<br>2'b11 :1004us@26MHz / 502us@52MHz<br>Note that these durations are made by frequency of CLK. |
| CNFG_LOCK_MARGIN[1:0] | Configuration of permissible error range for PLL lock detector.<br>2'b00 :+/- 1CLK<br>2'b01 :+/- 4CLK<br>2'b10 :+/- 8CLK<br>2'b11 :+/- 15CLK |

### 5.6.3 Functional Description

The lock detector monitors the counter value of PHY_PLL_FBCK at the overflow of reference clock timer.

If the difference of counter and timer is within the permissible error range which is given by CNFG_LOCK_MARGIN[1:0], lock detector asserts LOCK status(ST[1]).

Otherwise, detector will negates LOCK status.

Following figure shows example timing of lock detector.

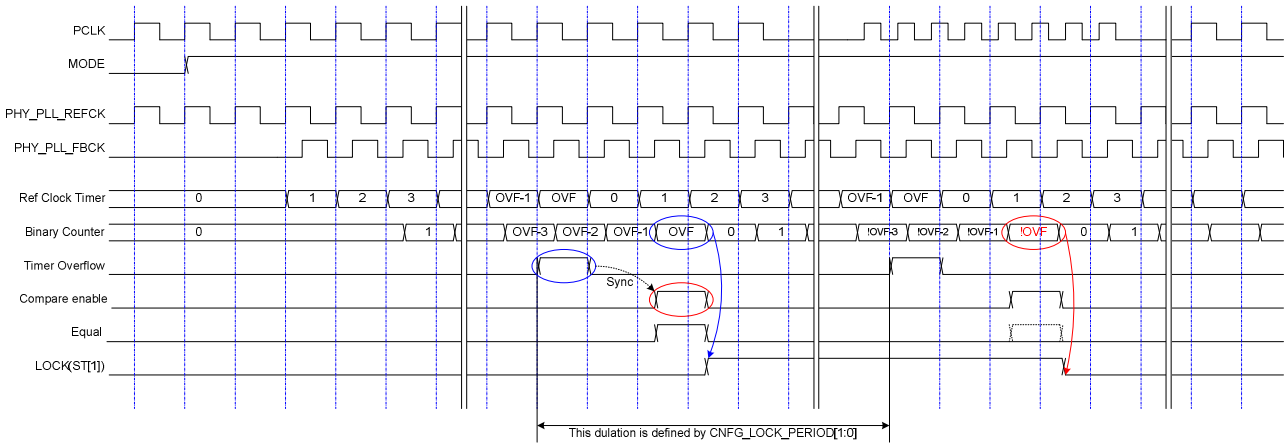


**Figure 11 Example Timing Diagram**

# 5.7 Rx FIFO

## 5.7.1 Overview

This IP includes two FIFO buffers on both Rx data paths for re-timing receive data from CDR in PHY mixed.

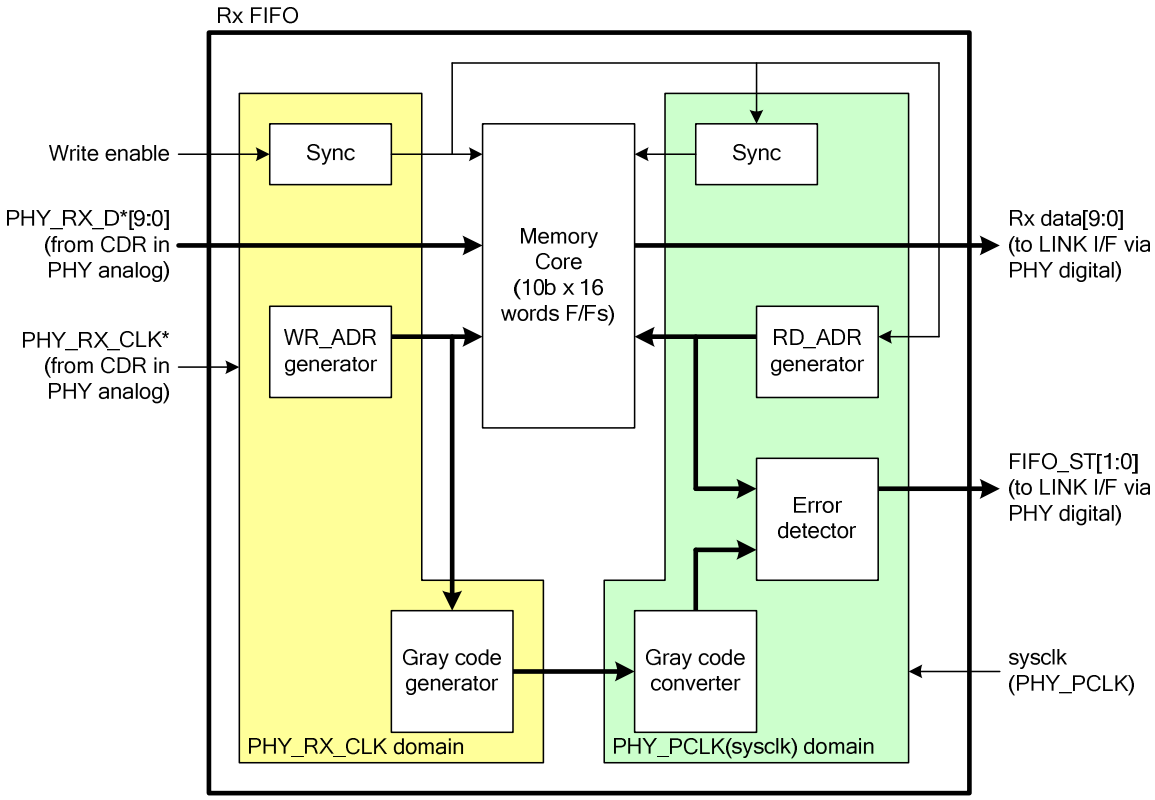


**Figure 12 Block Diagram of Rx FIFO**

When PHY receives the data, CDR recovers data and clock (PHY_RX_CLK) which is synchronized to the data. Rx FIFO uses this clock to store the received data into itself. Then Rx FIFO outputs the stored data which is synchronized to system clock of PHY digital (sysclk: symbol interval clock (same as PHY_PCLK)).

### 5.7.2 Related Pins

The related pins of Rx FIFO are shown below.

**Table 23 Description of Related Pins**

| Name | Description |
|---|---|
| RDT_FIFO_NRST | This is used as partial reset signal for Rx FIFO on default-Tx lane. When this signal is asserted, the status (RDT_FIFO_ST[1:0]) and internal pointers of Rx FIFO are cleared.<br>When the RDT_FIFO_ST[1:0] indicates the status except "Normal", LINK can clear the status by asserting this signal during RDTS=OFF. |
| RD_FIFO_NRST | This is used as partial reset signal for Rx FIFO on default-Rx lane. When this signal is asserted, the status (RD_FIFO_ST[1:0]) and internal pointers of Rx FIFO are cleared.<br>When the RD_FIFO_ST[1:0] indicates the status except "Normal", LINK can clear the status by asserting this signal during RDS=EIDL or OFF. |
| RDT_FIFO_ST[1:0] | PHY indicates the status of Rx FIFO on default-Tx lane via these pins.<br>Each status are shown below;<br>-2'b00: Normal (default)<br>-2'b01: Almost full or empty.<br>-2'b10: FIFO Overflow.<br>-2'b11: FIFO Underflow. |
| RD_FIFO_ST[1:0] | PHY indicates the status of Rx FIFO on default-Rx lane via these pins.<br>Each status are shown below;<br>-2'b00: Normal (default)<br>-2'b01: Almost full or empty.<br>-2'b10: FIFO Overflow.<br>-2'b11: FIFO Underflow. |

### 5.7.3 Functional Description

As mention above, this FIFO generates some error status.

The mechanism of error detection is shown below.

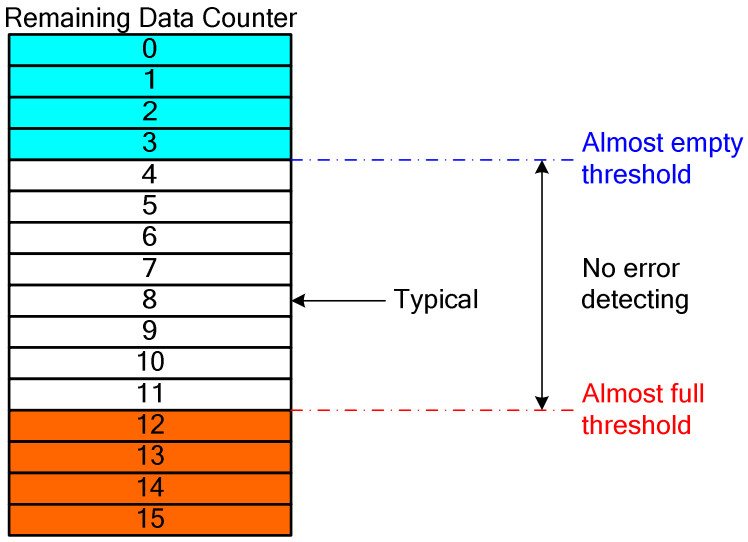


**Figure 13 Thresholds for Error Detecting**

#### 5.7.3.1 Normal Operation

When PHY starts the data receiving on each lane, Rx FIFO starts to store the data into itself. Then, when the remaining (stored) data counter reaches to 8, FIFO starts to output stored data and starts detecting errors. Typically, the frequency of both reading and writing clock are same, so the remaining data will be always 8 and FIFO does not assert the error status.

#### 5.7.3.2 Error Handling

When PHY receives the data which is injected very large jitter, the frequency of the clock from CDR is skewed by jittered data. In such case, frequency will be differ between reading and writing clocks, so remaining data counter might be moves from typical location to each error thresholds.

When the counter reaches to either error thresholds, FIFO detects it and changes RD(T)_FIFO_ST[1:0] to 2'b01. Then in the next cycle, FIFO changes RD(T)_FIFO_ST[1:0] to 2'b10 or 2'b11 depends on the previous status. For example, if the counter reached to "Almost empty threshold" when RD(T)_FIFO_ST[1:0] indicated 2'b01, FIFO changes to 2'b11. Afterward, FIFO resets the internal pointer and stops storing the received data.

After the reset, FIFO starts storing the data same as the normal operation.

## 5.8 PCS Manufacturing Test

This IP supports SCAN test for manufacturing test.

### 5.8.1 Related Pins

Related pins about SCAN test are shown below.

**Table 24 Description of Related Pins for SCAN Test**

| Name | I/O | Description |
|---|---|---|
| NRST | Input | System reset for PCS. |
| SCAN_CLK | Input | SCAN shift clock input for SCAN test mode.<br>This clock drive all F/Fs in this IP during the SCAN_MODE is 1. |
| SCAN_MODE | Input | Controls SCAN Test mode of PCS.<br>1: SCAN Test enable<br>0: Normal operation |

To start SCAN test, assert SCAN_MODE pin.

All SCAN F/Fs are driven by SCAN_CLK (positive edge), and reset by NRST while SCAN_MODE = 1.

For more details, see the SoC Design Guideline for each IP.

## 5.9 PMA Manufacturing Test

This IP provides various test methods for manufacturing test of PHY.

In these test modes, this IP controls driver, receiver, and terminator automatically according to direction of each differential lane.

### 5.9.1 Test Item List

Following list shows the supported test items by this IP.

**Table 25 Test Item List**

| Test No. | Major Category | Minor Category | Measurement Pins | Measurement Item | Unit | Notes |
|---|---|---|---|---|---|---|
| 1 | Supply Current | Dormant | Analog VDD | I | [uA] | IP Spec |
| 2 | Pin Leakage | | D0_P/M, D1_P/M, RCLK_P/M | I | [uA] | UHS-II Spec |
| 3 | Supply Current | Normal Operation | Analog VDD | I | [mA] | IP Spec |
| 4 | VCO Gain | Min/Max | TEST_MON[1] | Freq. | [MHz] | |
| 5 | PLL Frequency Acquisition | Min/Max | TEST_MON[0] | Level | | |
| 6 | Driver | Diff "H" Voltage | D0_P/M, D1_P/M, RCLK_P/M (Note-1) | V | [mV] | UHS-II Spec |
| 7 | | Diff "L" Voltage | D0_P/M, D1_P/M, RCLK_P/M (Note-1) | V | [mV] | UHS-II Spec |
| 8 | Terminator Resistance | Tx | D0_P/M, D1_P/M, RCLK_P/M (Note-1) | I | [mA] | UHS-II Spec |
| 9 | Terminator Resistance | Rx | D0_P/M, D1_P/M, RCLK_P/M (Note-1) | I | [mA] | UHS-II Spec |
| 10 | Amplitude Detector | Detector Function | TEST_MON[2:1] | Level | | UHS-II Spec |
| 11 | SERDES | Forward SERDES Loopback | TEST_MON[1] | Level | | |
| 12 | | Backward SERDES Loopback | TEST_MON[1] | Level | | |

Note-1) When this IP is used with the PMA for UHS-II HOST, RCLK_P/M are excepted from measurement pins of test #9. Similarly, when this IP is used with the PMA for UHS-II DEVICE, RCLK_P/M are excepted from measurement pins of test #5, 6, and 7.

### 5.9.2 Related Pins

Related pins about Test Method are shown below.

Each test modes are not affected by other input pins of this IP. Therefore, user shall control only these pins for handling manufacturing test except PHY_TEST_PLL[2:0] and external pins of PMA.

**Table 26 Description of Related Pins for PMA Manufacturing Test**

| Name | I/O | Description |
|---|---|---|
| TEST_NRST | Input | System reset for PCS while test mode.<br>This pin is enabled while TEST_EN = 1. Otherwise, this pin does not affect to PHY. |
| TEST_CLK | Input | PLL reference clock for TEST mode.<br>Supply constant clock (26 to 52MHz) for using each TEST mode while HOST_MODE=1. |
| TEST_CLK_EN | Input | PLL reference clock source select.<br>0: CLK (HOST_MODE=1) / RCLK(HOST_MODE=0)<br>1: TEST_CLK |
| TEST_EN | Input | Enables manufacturing test mode. |
| TEST_PLLSEL | Input | PLL multiplication factor select in test mode.<br>0: x15 (Range-A: 390 to 780Mbps)<br>1: x30 (Range-B: 780 to 1560Mbps) |
| TEST_MODE[3:0] | Input | Test mode select.<br>4'b0000: Dormant Supply Current Test<br>4'b0001: Normal Supply Current Test<br>4'b0010: Differential Voltage "H" Test<br>4'b0011: Differential Voltage "L" Test<br>4'b0100: Tx Terminator Resistance Test<br>4'b0101: Rx Terminator Resistance Test<br>4'b0110: Detector Function Test<br>4'b0111: Reserved (Do not use)<br>4'b1000: Forward SERDES Loopback BIST<br>4'b1001: Backward SERDES Loopback BIST<br>4'b1010: Forward Driver Loopback BIST (*)<br>4'b1011: Backward Driver Loopback BIST (*)<br>4'b1100: Forward Loopback Test (*)<br>4'b1101: Backward Loopback Test (*)<br>4'b1110: Forward Receiver Loopback Test (*)<br>4'b1111: Backward Receiver Loopback Test (*)<br>Each test modes marked asterisk (*) are not used in current version of PMA test. |
| TEST_PAT[1:0] | Input | BIST data pattern select<br>2'b00: PRBS with 8B10B coding<br>2'b01: Fixed K28.5<br>2'b10: Fixed D10.2<br>2'b11: Repeated "LIDL0" (K28.5+K28.3)<br>These pins affect to only BIST modes.<br>FIx to 2'b00 except debugging purpose. |
| TEST_PLLLOCK | Input | Make LOCK signal H for test.<br>Fix to 0 while normal operation. |
| TEST_TRM_OFF | Input | Disables terminator of all lanes to make high impedance state. |
| TEST_TXD | Input | Tx Serial data format select for debug purpose.<br>Fix to 0 while all test modes. |
| TEST_MON[2:0] | Output | Indicates result/status of the test. |

### 5.9.3 Example Test Environment

Following figure shows example environment for manufacturing test of PMA.

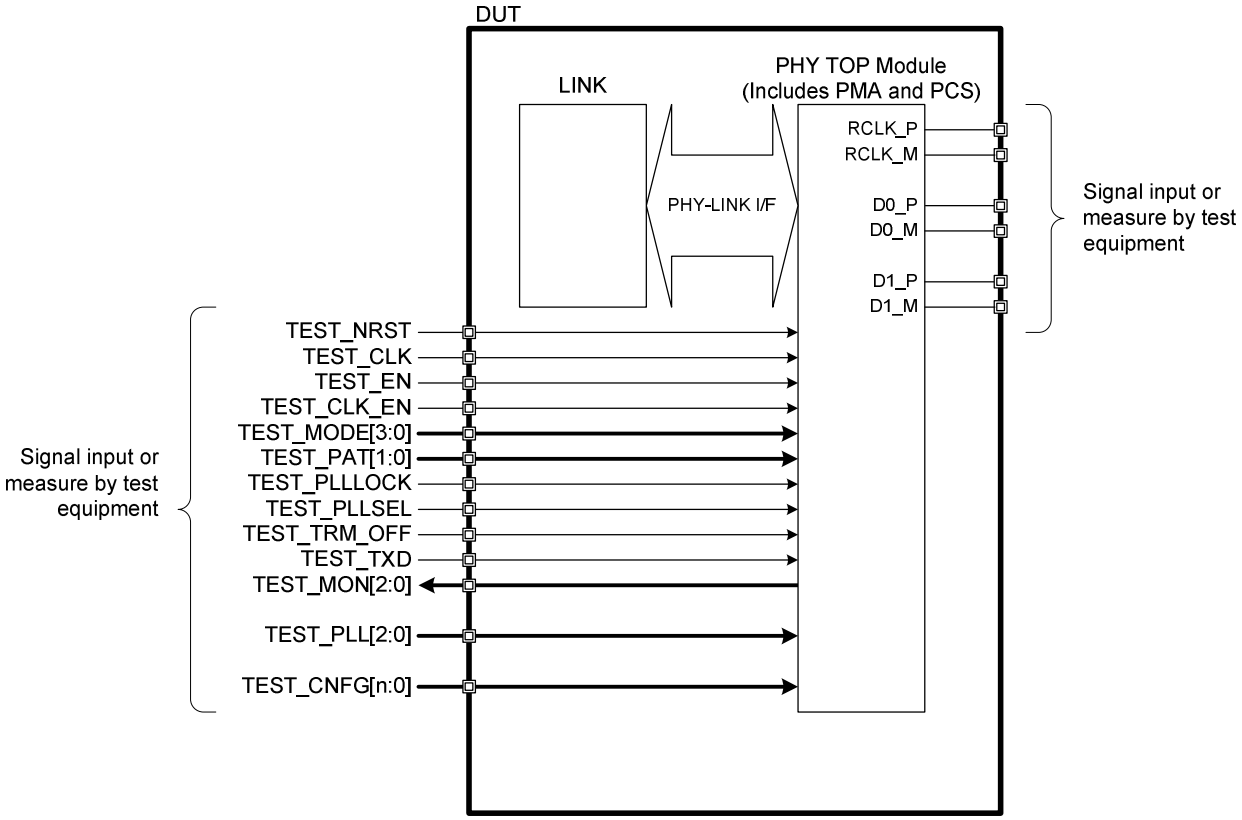


**Figure 14 Example of Test Environment**

### 5.9.4 Example Test Procedures

Procedures of each test mode are shown below.

#### 5.9.4.1 Dormant Supply Current Test

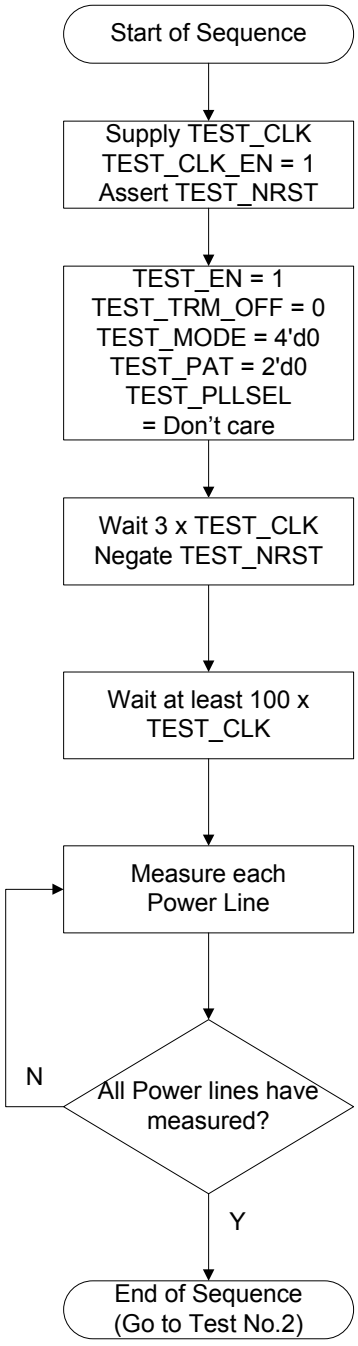


**Figure 15 Procedure of Dormant Supply Current Test**

### 5.9.4.2 Pin Leakage Current Test

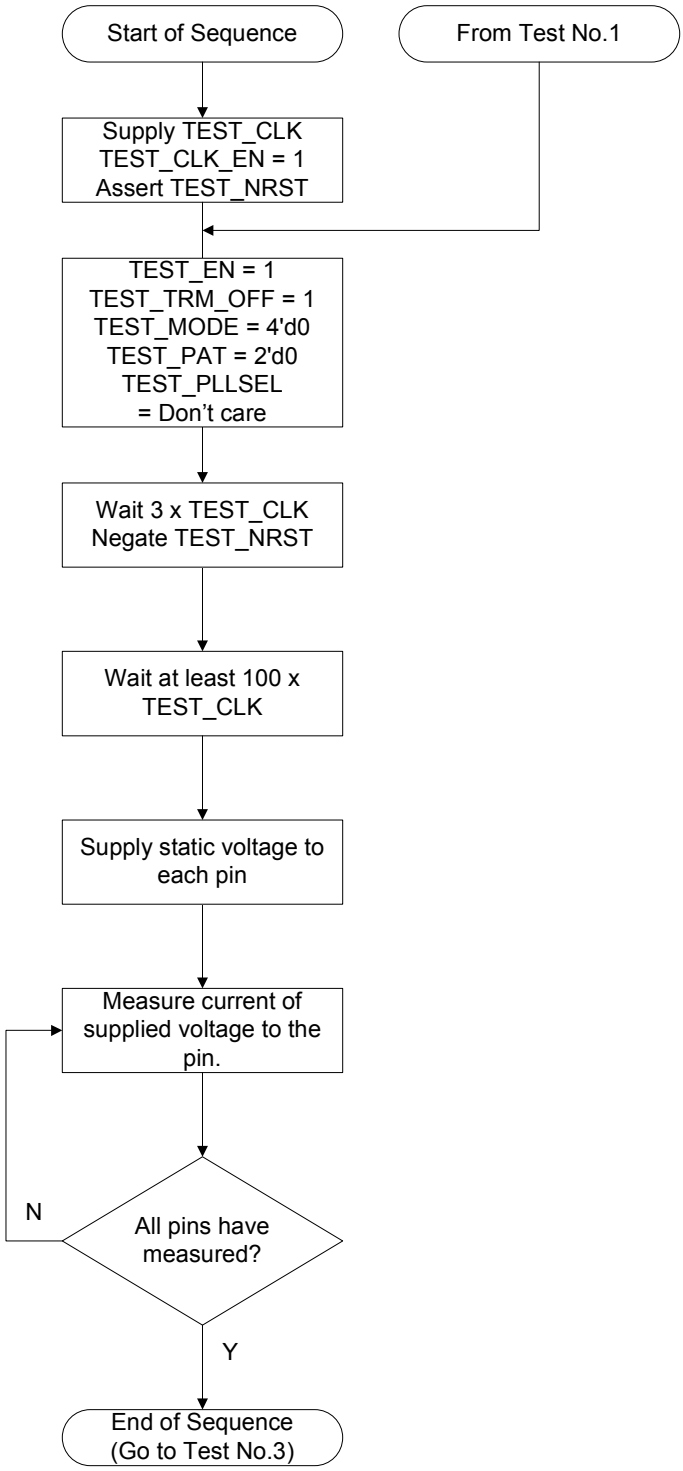


**Figure 16 Procedure of Pin Leakage Current Test**

### 5.9.4.3 Normal Supply Current Test

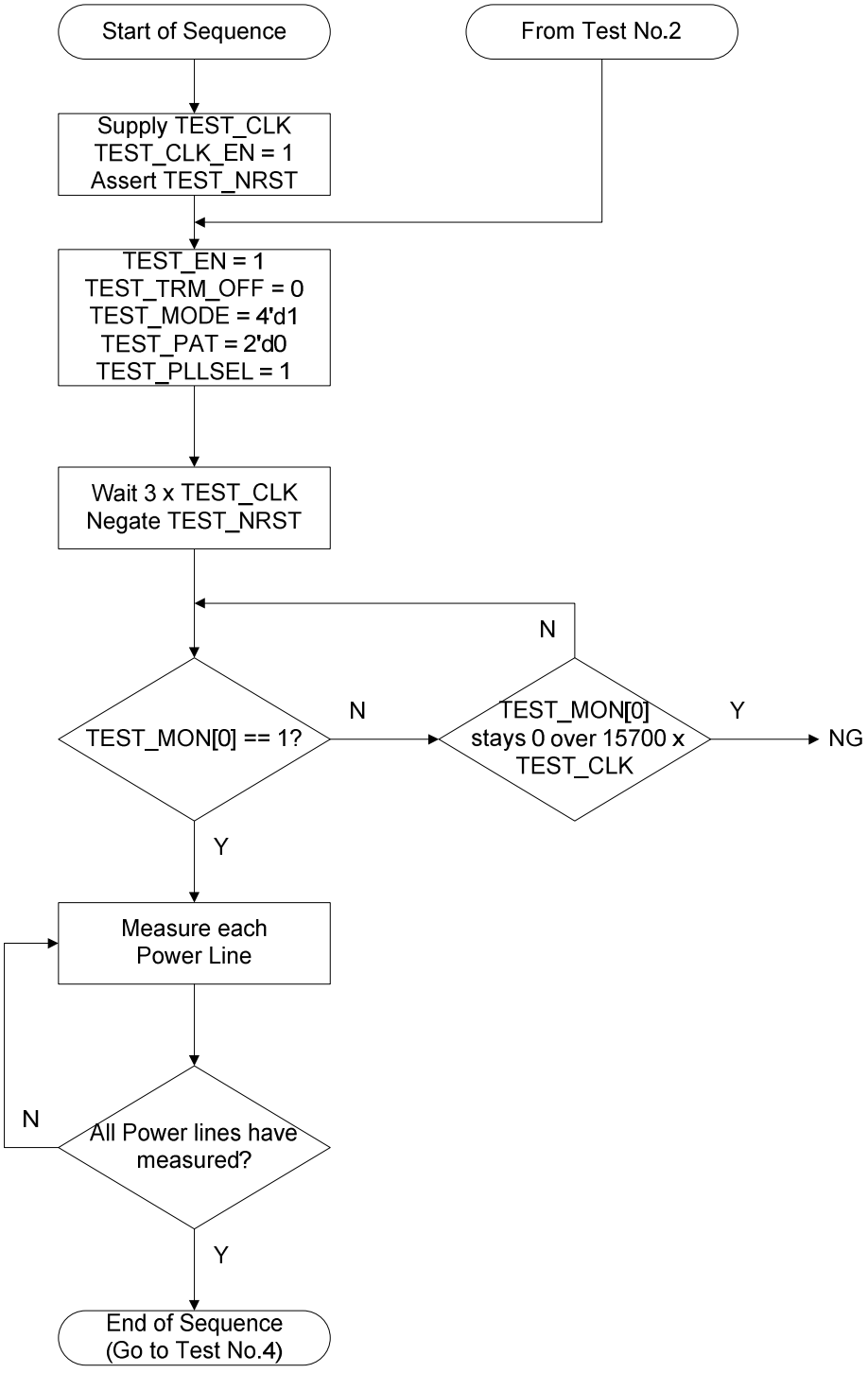


**Figure 17 Procedure of Normal Supply Current Test**

### 5.9.4.4 VCO Gain Test

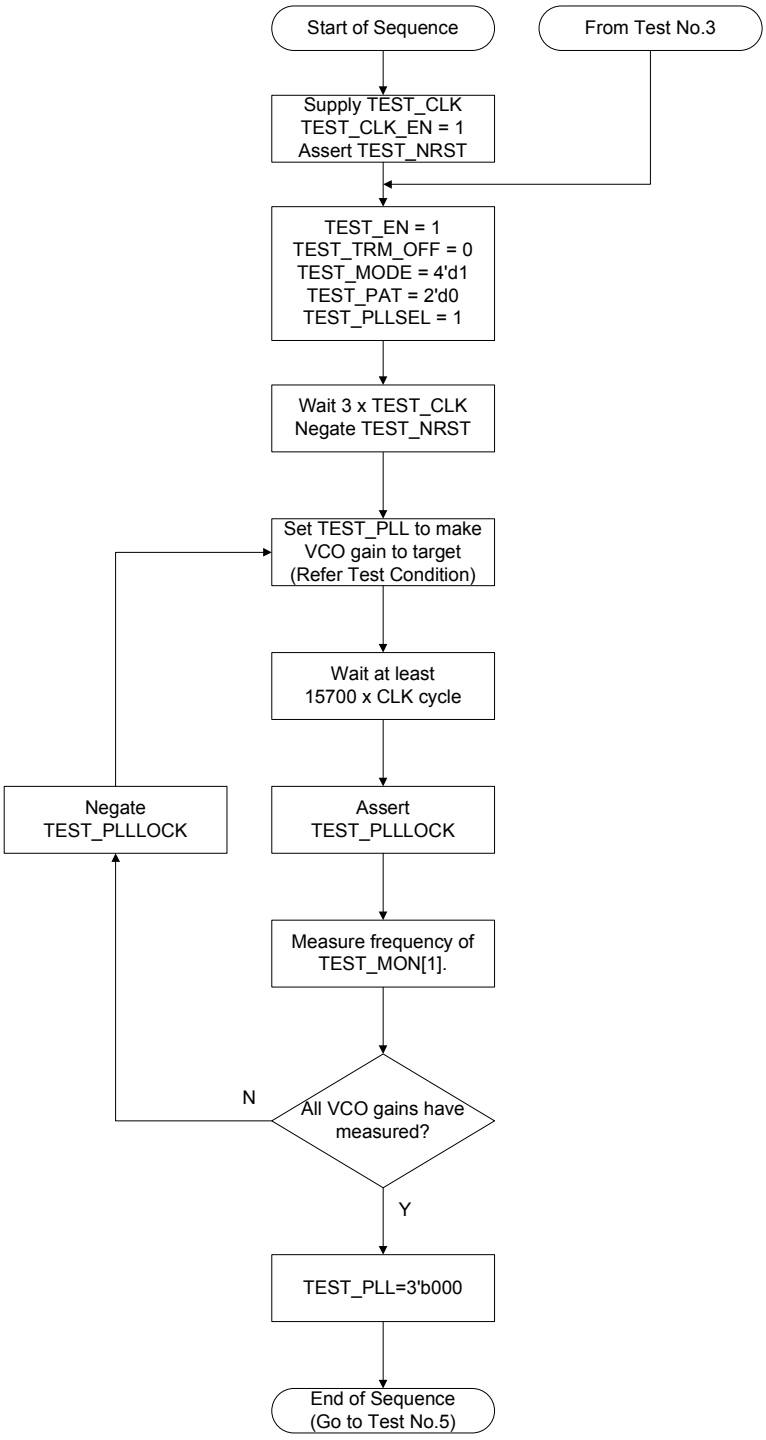


**Figure 18 Procedure of VCO Gain Test**

### 5.9.4.5 PLL Frequency Acquisition Test

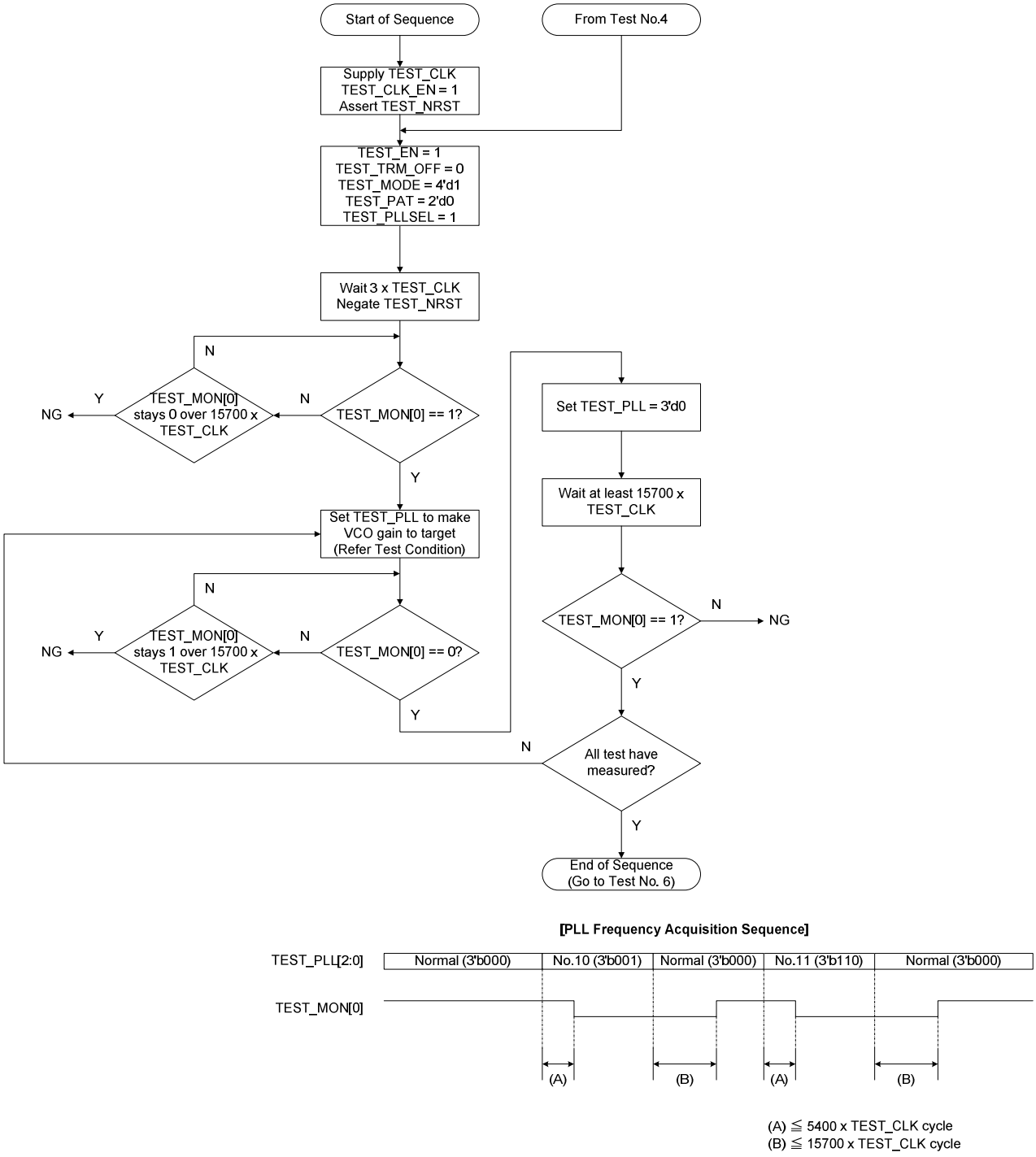


**Figure 19 Procedure of PLL Frequency Acquisition Test**

5.9.4.6 Driver Differential "H" Voltage Test

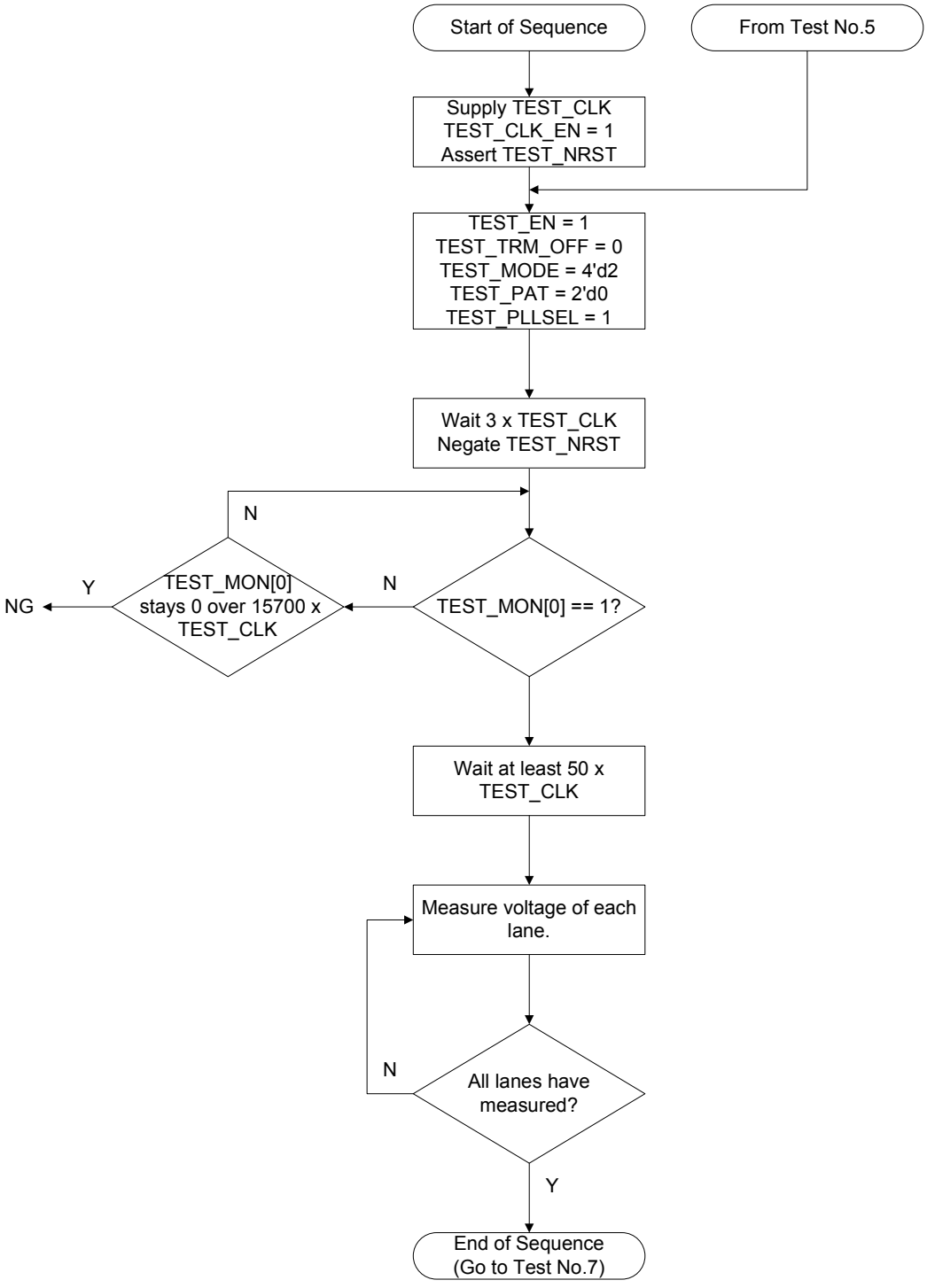


**Figure 20 Procedure of Driver Differential "H" Voltage Test**

### 5.9.4.7 Driver Differential "L" Voltage Test

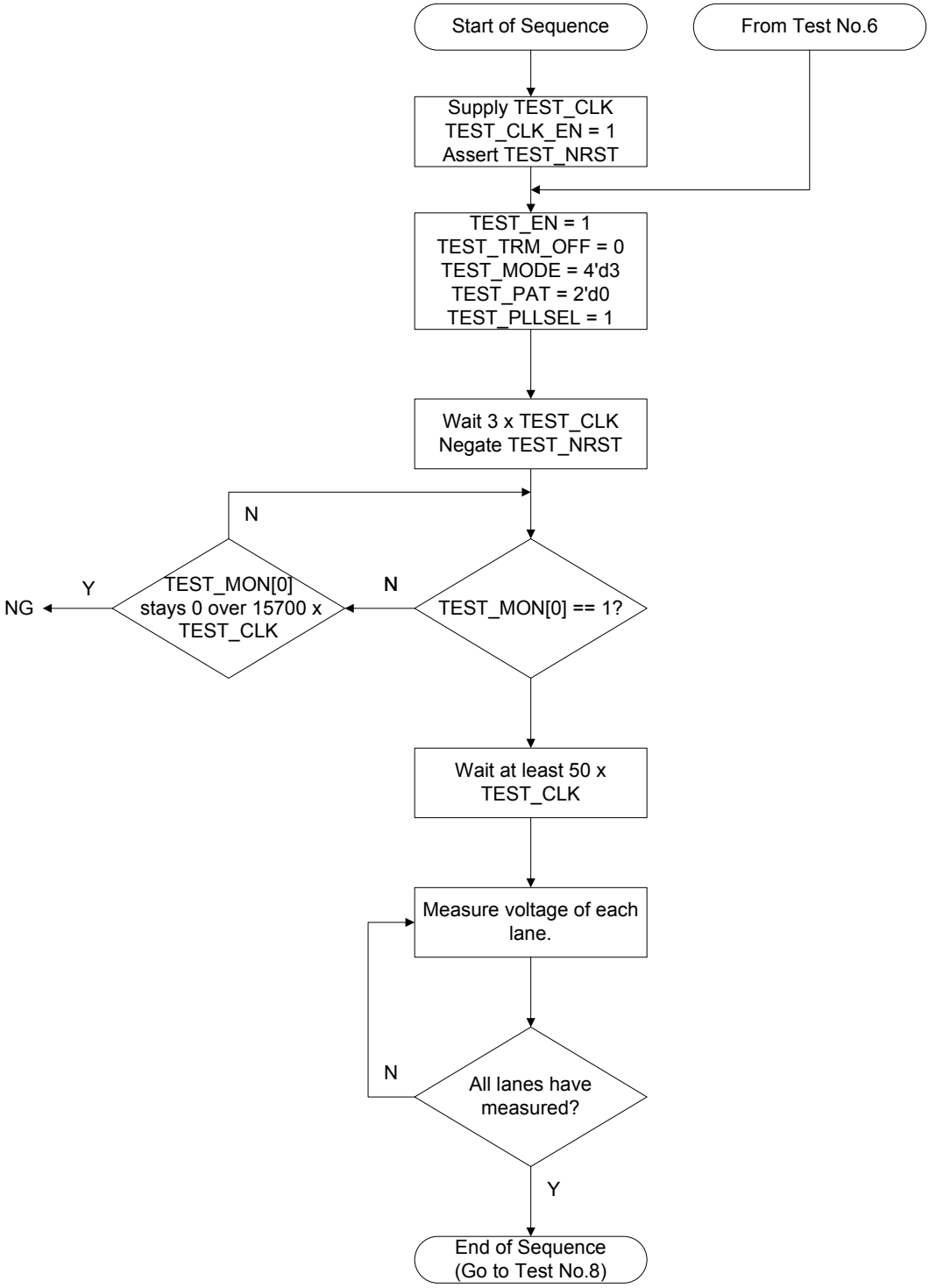


**Figure 21 Procedure of Driver Differential "L" Voltage Test**

### 5.9.4.8 Tx Terminator Resistance Test

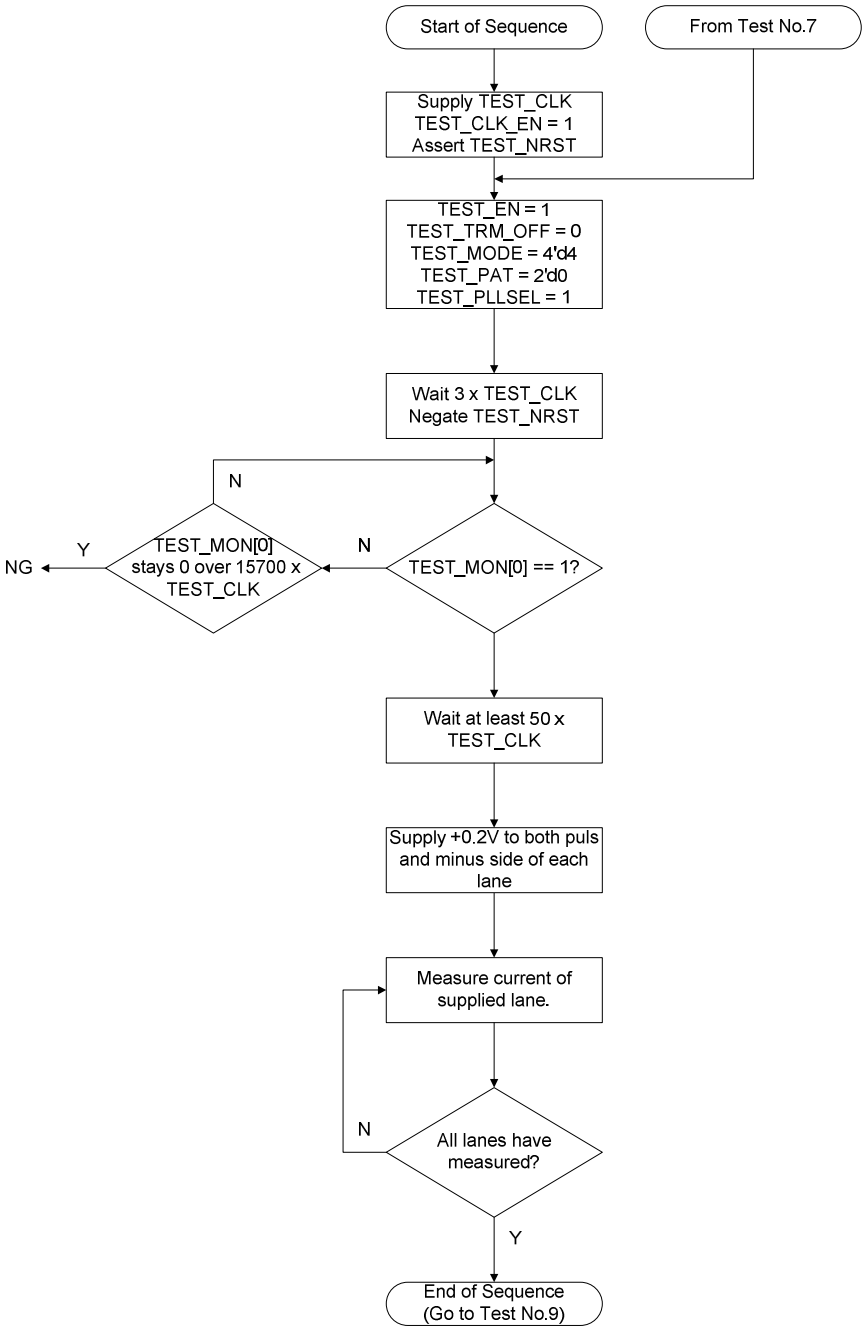


**Figure 22 Procedure of Tx Terminator Resistance Test**

### 5.9.4.9 Rx Terminator Resistance Test

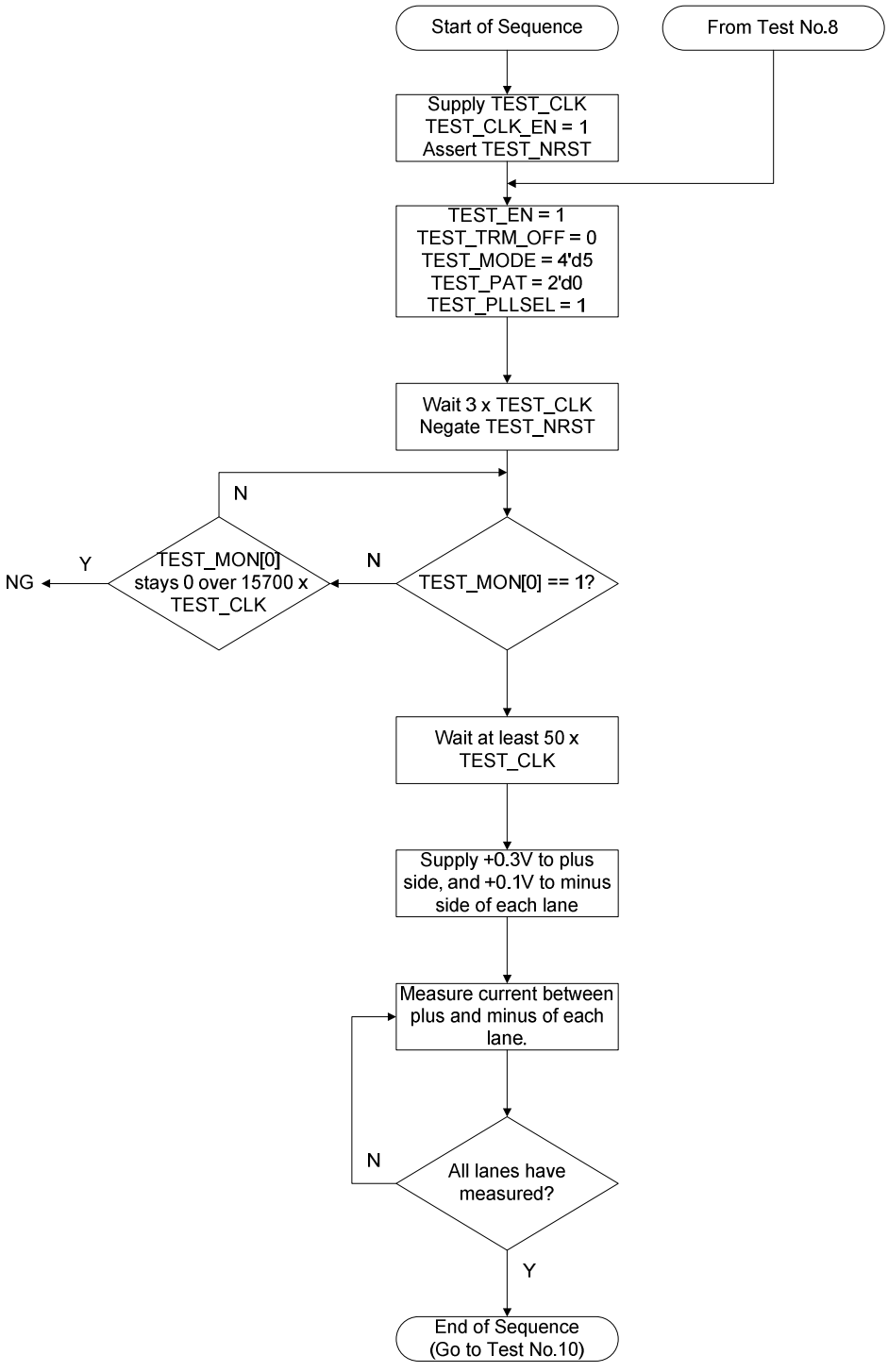


**Figure 23 Procedure of Rx Terminator Resistance Test**

### 5.9.4.10 Amplitude Detector Function Test

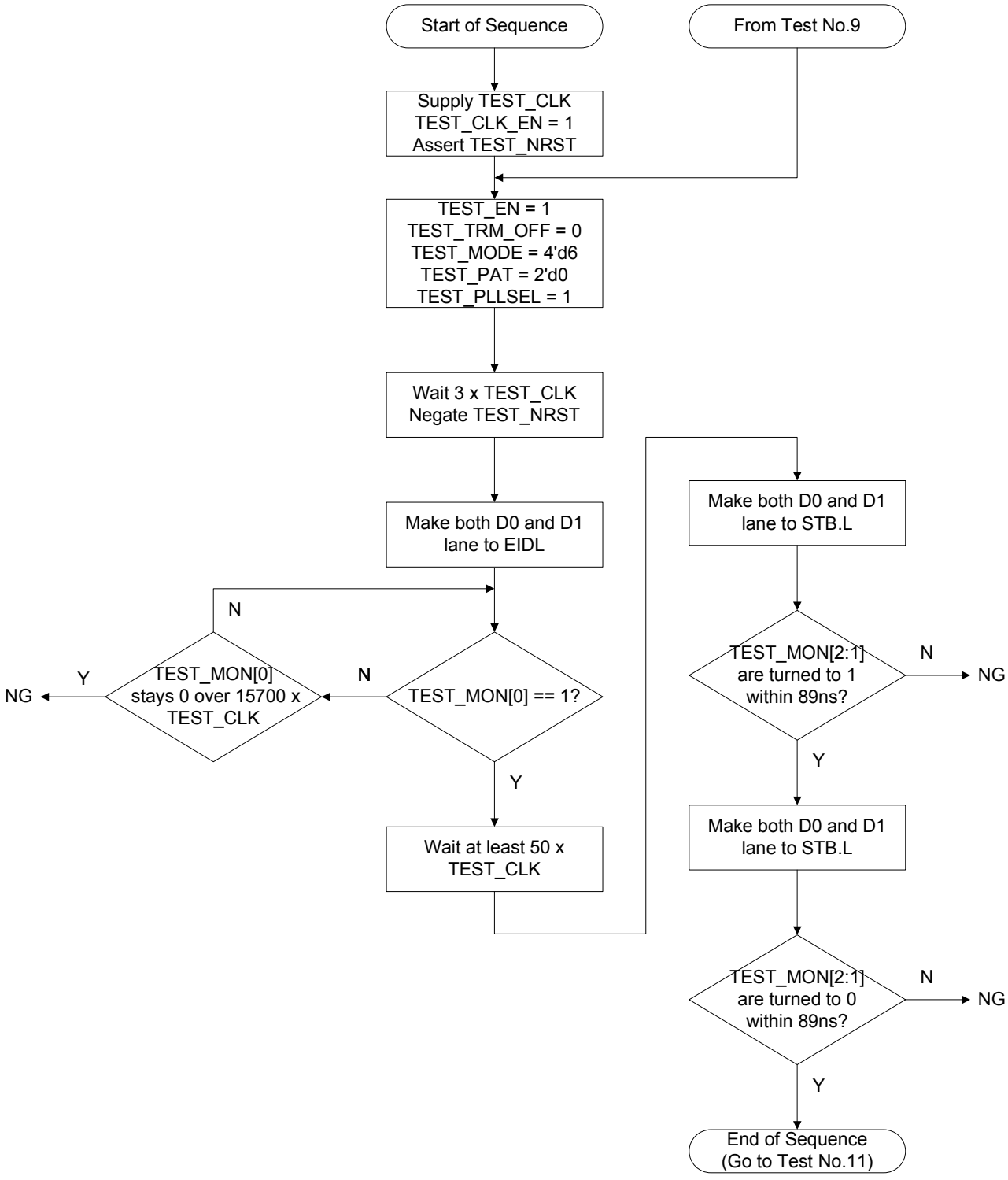


**Figure 24 Procedure of Amplitude Detector Function Test**

### 5.9.4.11 Forward SERDES Loopback BIST

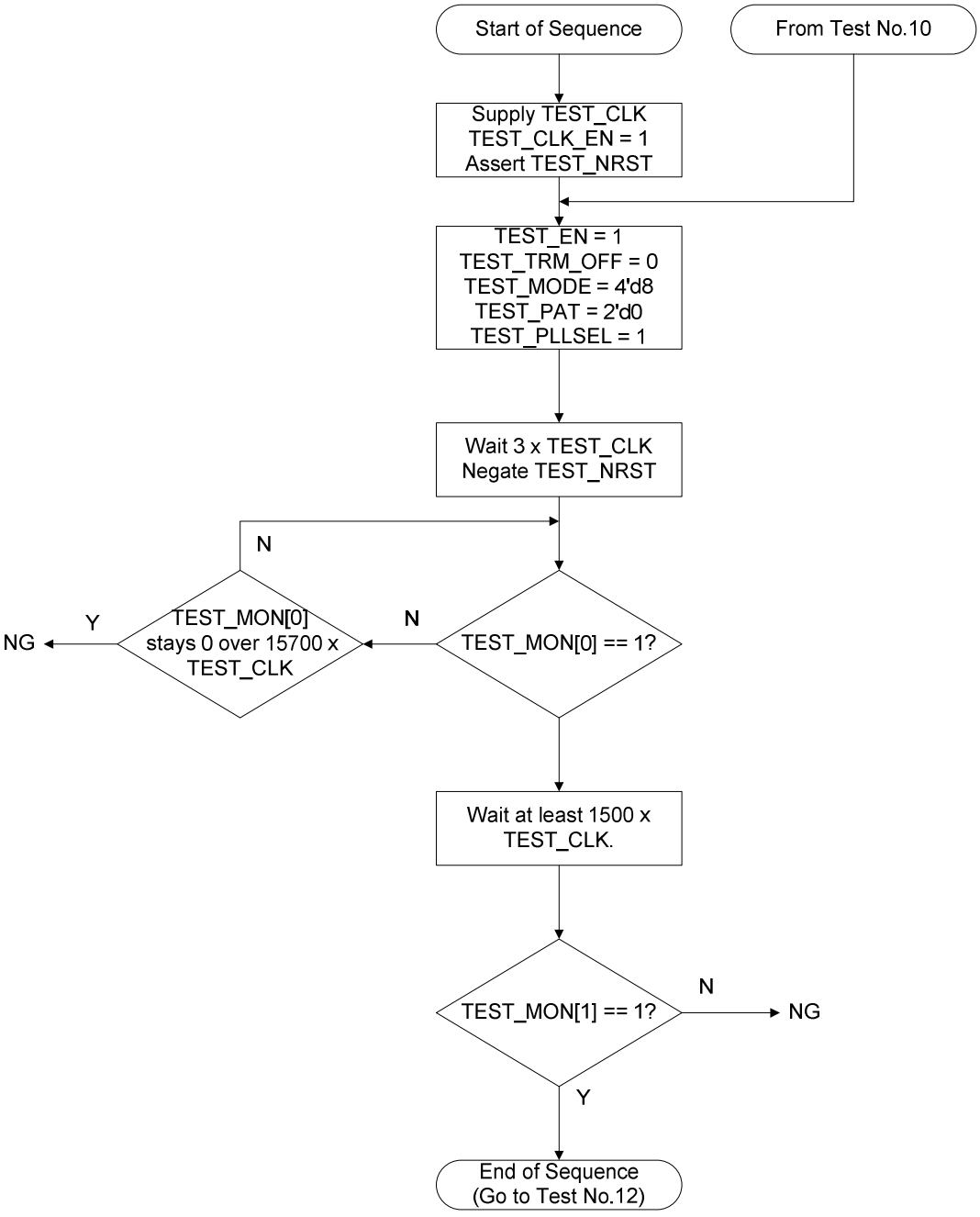


**Figure 25 Procedure of Forward SERDES Loopback BIST**

### 5.9.4.12 Backward SERDES Loopback BIST

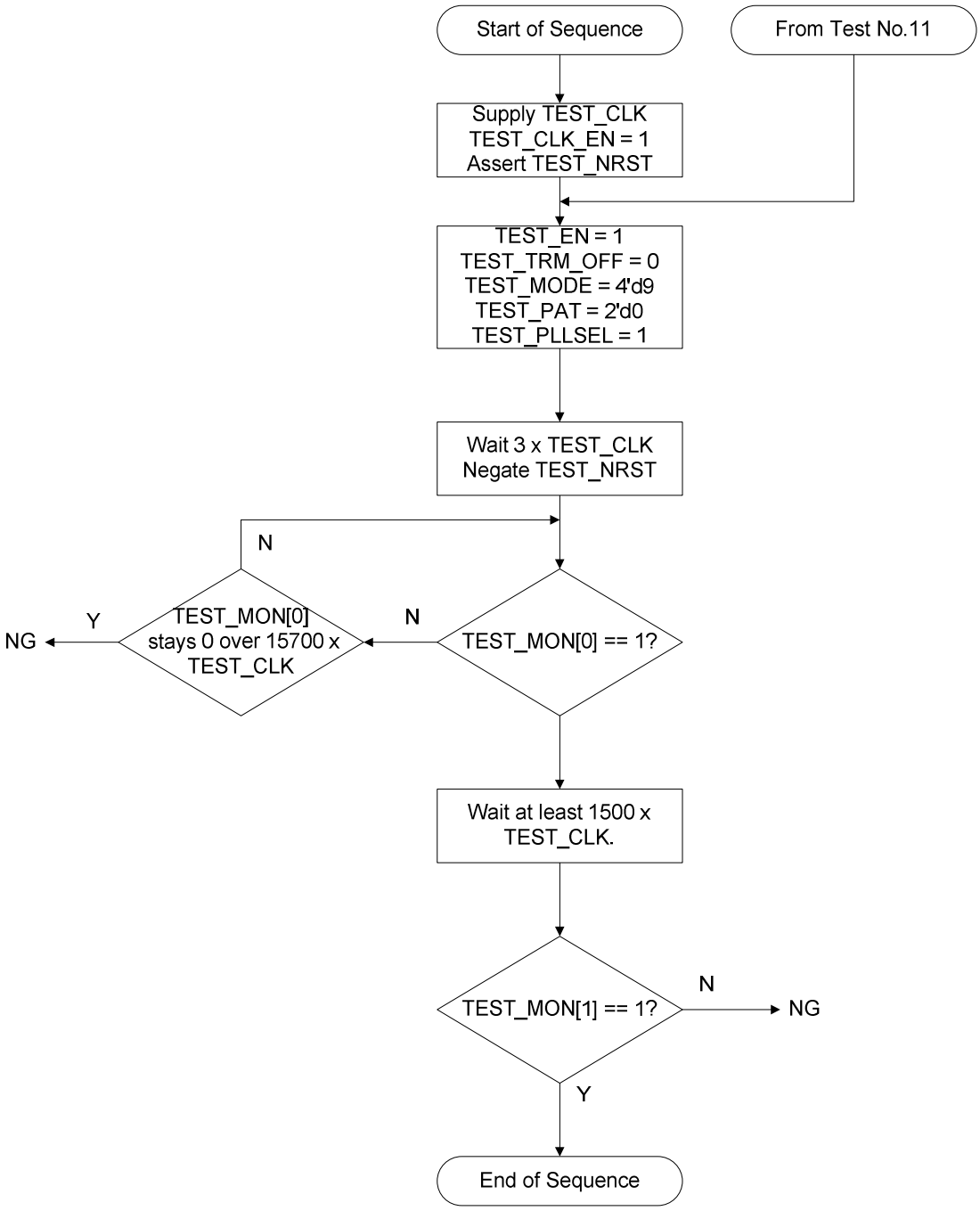


**Figure 26 Procedure of Backward SERDES Loopback BIST**

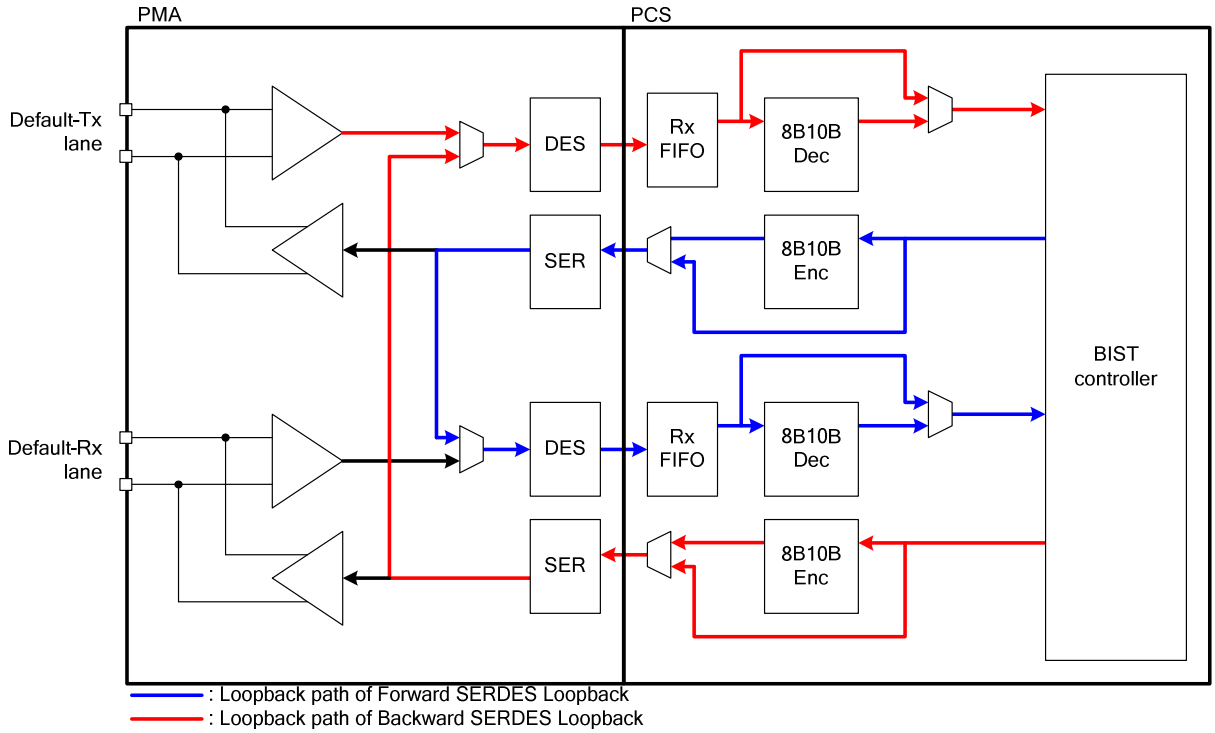


**Figure 27 Block Diagram of SERDES Loopback path for BIST**

Note that while BIST mode, both D0 and D1 lane should be floated because the direction of both D0 and D1 lanes are set as output.

### 5.9.5 Reserved Test Modes

This IP has several reserved test modes as shown below.

**Table 27 List of Reserved Test Modes**

| TEST_MODE[3:0] | Description |
|---|---|
| 4'b1010 | Forward Driver Loopback BIST |
| 4'b1011 | Backward Driver Loopback BIST |
| 4'b1100 | Forward Loopback Test |
| 4'b1101 | Backward Loopback Test |
| 4'b1110 | Forward Receiver Loopback Test |
| 4'b1111 | Backward Receiver Loopback Test |

Each modes are mentioned below.

#### 5.9.5.1 Forward/Backward Driver Loopback BIST

In this mode, PHY execute BIST via driver/receiver of each data lane as shown below.

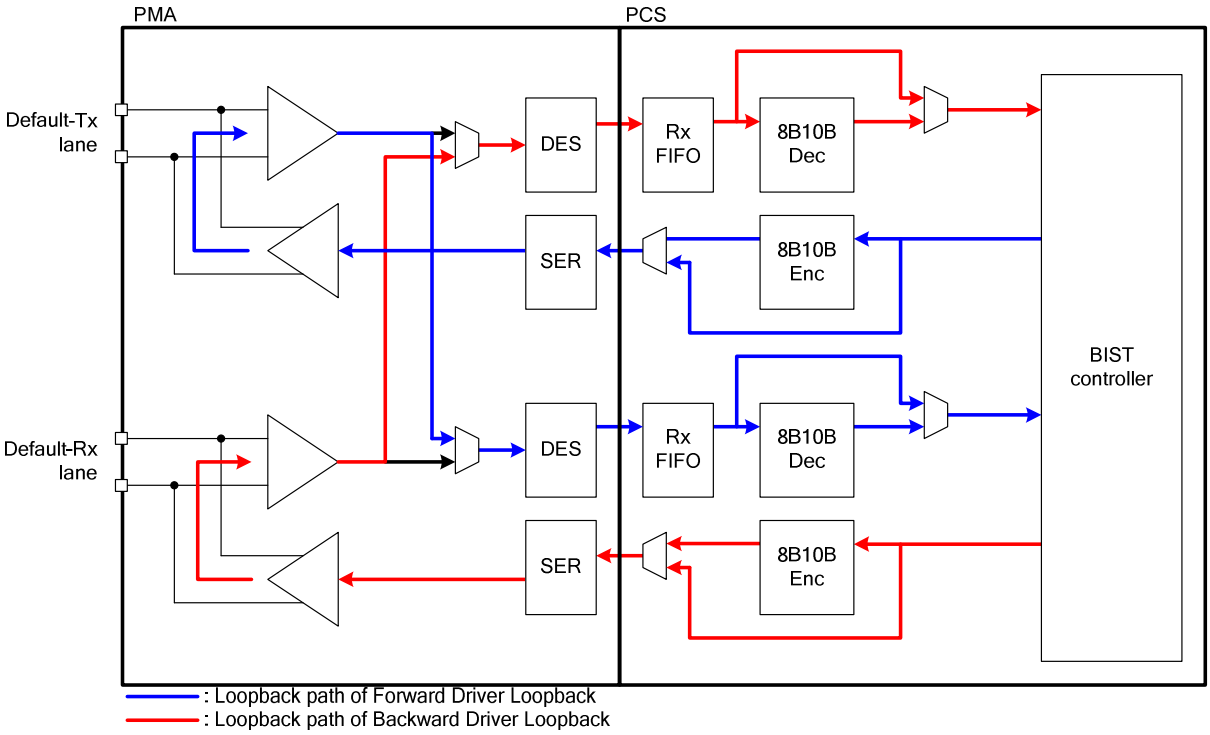


**Figure 28 Block Diagram of Driver Loopback path for BIST**

To prevent the reflection by stub on the data lanes, do not attach any loads to both D0 and D1 lane.

Otherwise, the driver loopback BIST might be failed by the reflection of data lane.

### 5.9.5.2 Forward/Backward Loopback TEST

This mode provides loopback test same as UHS-II Compliance test mentioned in section 5.10.

It is useful to enter to PHY Test Mode for UHS-II Compliance without receiving dedicated packet.

For details of loopback path, see section 5.10.1.4.

### 5.9.5.3 Forward/Backward Receiver Loopback TEST

The loopback paths of this test mode is shown below.

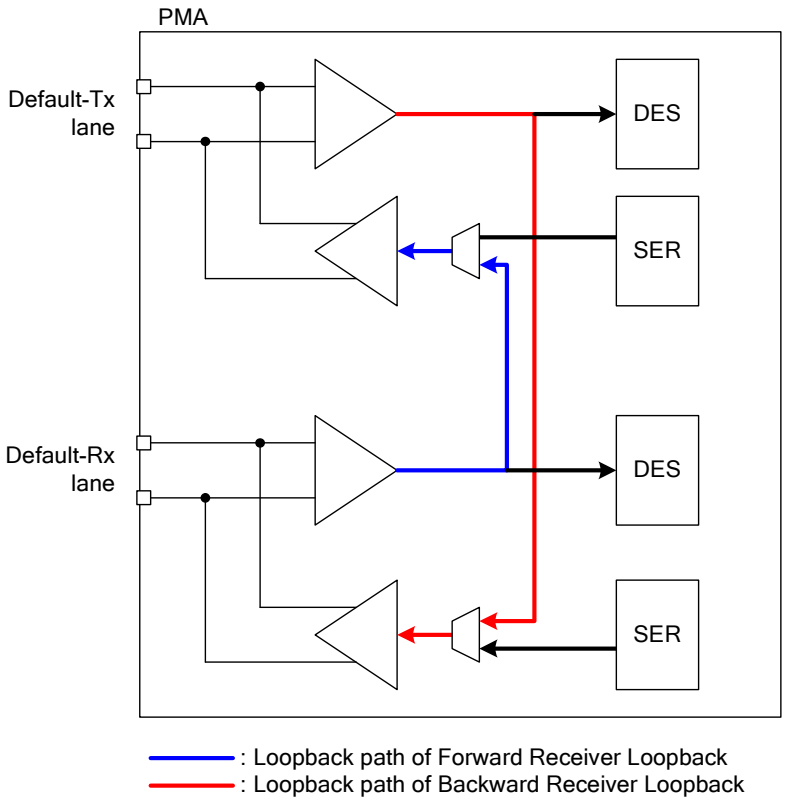


**Figure 29 Diagram of Receiver Loopback path**

This mode provides loopback function without SERDES function for debug purpose.

## 5.10 PHY Test Mode for SD UHS-II Compliance

This IP supports the PHY Test Mode described in “SD Specifications Part1 UHS-II Addendum Version 1.00 Draft 1.00”.

Basically, PHY controls internal logics automatically that depends on the TMD1 and 2 (i.e. Entering/exiting Dormant, changing loopback direction, etc) with COM and K30.7 which is included with the received packet from test equipment.

### 5.10.1.1 Related Pins

Related pins about PHY Test Mode are shown below.

**Table 28 Description of Related Pins for PHY Test Mode**

| Name | I/O | Description |
|---|---|---|
| PTM_EN | Input | This is used for enabling packet encoder which is used to enter to PHY Test Mode.<br>If this pin is set to 1 while UHS-II DEVICE mode (HOST_MODE=0), PHY enters to the PHY Test Mode when PHY detects the dedicated packet (TMDs) automatically.<br>And if this pin is set to 1 while UHS-II HOST mode (HOST_MODE=1), PHY enters to "Slave Mode" for detecting the sequence for Test Mode entry. Set to 0 this pin for normal operation of PHY while HOST_MODE=1. |
| PHY_TEST_MODE | Output | This is used to monitoring the mode of PHY.<br>0: Normal mode (except PHY Test Mode)<br>1: PHY Test Mode<br>When PHY enters to the PHY Test Mode, PHY asserts this pin and handles receiving packet for controlling the Test Mode. |
| PTM_SSCE | Output | Enables SSC generator for CLK on LINK or upper layer.<br>0: Disable<br>1: Enable<br>This signal is asserted by TMD2 bit[6] in received TEST-MODEs.<br>After reset, this pin is turned to 0. |

### 5.10.1.2 State Transition

State transition of PHY Test Mode is shown below.

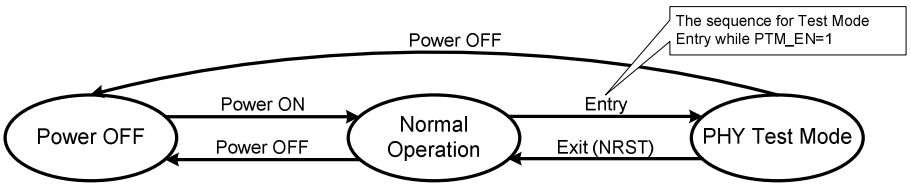


**Figure 30 State Transition of PHY Test Mode (HOST_MODE=0)**

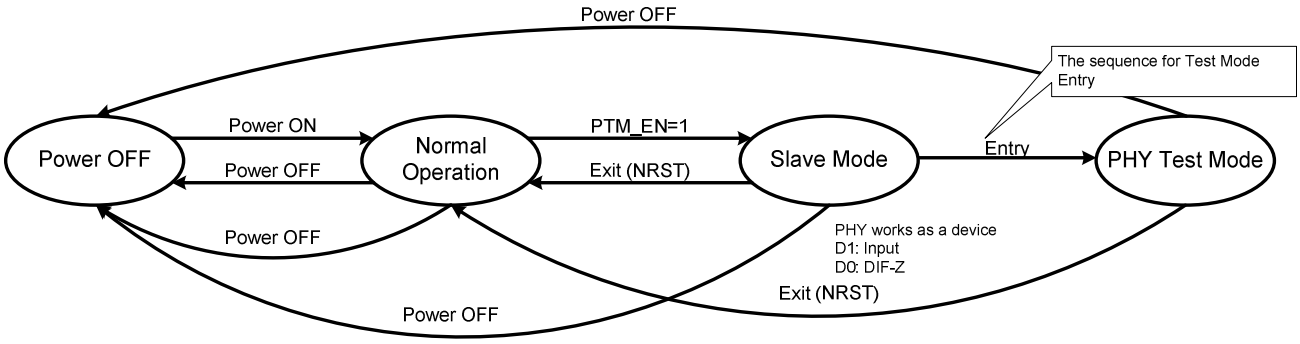


**Figure 31 State Transition of PHY Test Mode (HOST_MODE=1)**

### 5.10.1.3 Supported TMDs

Supported format of TMD1 and TMD2 are shown below.

**Table 29 TMD1 Bit Map**

| TMD1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **[7]** | **[6]** | **[5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| 0 | 0 | 0 | 0 | 0 | 0 | Dis-connect | Timing |

bit[7:2]: This IP supports only all 0 in this field.

bit[1]: This bit determines disconnect mode.

-0: Normal (Non-Disconnect)

-1: Disconnect Mode

bit[0]: This bit determines timing of test mode entry.

-0: Effective Immediately

-1: When exiting Dormant or Re-Sync state

**Table 30 TMD2 Bit Map**

| TMD2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **[7]** | **[6]** | **[5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| Loopback Direction | SSCE | 0 | 0 | 0 | PLL Multiplication Factor | | |

bit[7]: This bit determines the direction of loopback

-0: Forward Loopback

-1: Backward Loopback

bit[6]: This bit enables the SSC generator on external this IP(HOST only)

-0: Disable

-1: Enable

bit[5:3]: This IP supports only all 0 in this field.

bit[2:0]: These bits select the PLL multiplication factor.

-000: x15

-001: x30

-Others: Unsupported

When PHY detects unsupported TMDs, PHY disregards the packet and does not enter to PHY Test Mode.

### 5.10.1.4 Loopback path

The loopback path for PHY Test Mode is shown below.

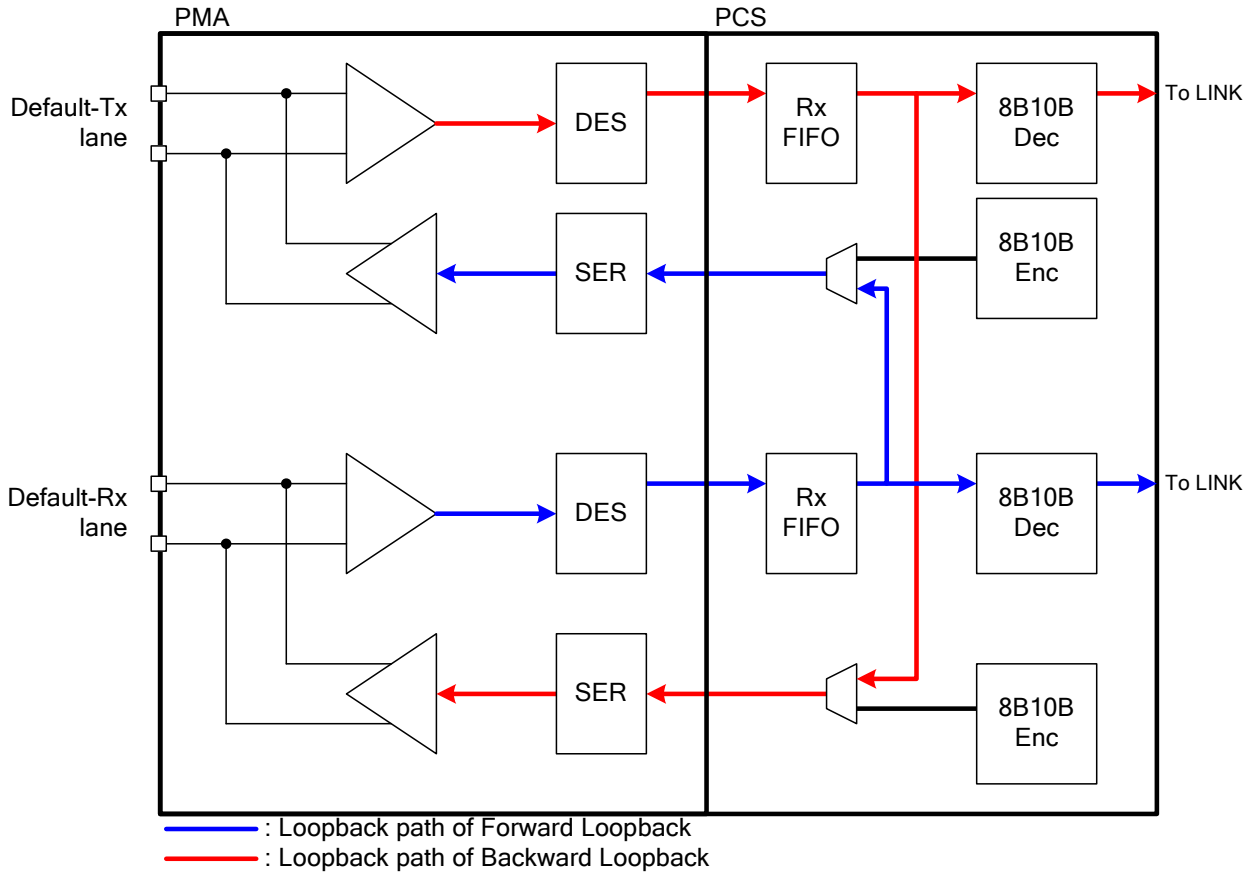


**Figure 32 Diagram of Forward/Backward Loopback path**

For more details about the sequence and procedure of PHY Test Mode, refer to chapter 8.8.

# 6 Recommended Parameters

Recommended value of each PCS configuration pins are shown below.

**Table 31 Recommended Parameters**

| Pin name | Sync/ Async | Recommended Setting |
|---|---|---|
| CNFG_LOCK_PERIOD[1:0] | Async | Duration of PLL lock sampling : Set to 2'b00 |
| CNFG_LOCK_MARGIN[1:0] | | Configuration for PLL lock detector: Set to 2'b00 |
| CNFG_FORCE_LOCK | | Set to 0 |
| CNFG_ALIGN_EN | | Set to 1 |
| CNFG_CDRCLK_SLP | PCLK | Set to 0 |
| CNFG_TX_EIDL | | Set to 0 |
| PTM_EN | | HOST_MODE=0 : Set to 1<br>HOST_MODE=1 : Set to 0 |

Note that each recommended value may be changed by evaluation result of PHY. Therefore, we recommend these configuration pins are able to control by software.

# 7 Timing Specification

**Table 32 Timing Specification of PHY**

| Item | Condition | Value[unit] | | Note |
|---|---|---|---|---|
| | | Min | Max | |
| tNRST | All | 20[ns] | | See Chapter 8.1 |
| tACT_REG | RCLK=26MHz | 10[us] | | See Chapter 8.1 |
| | RCLK=52MHz | 5[us] | | |
| tACT_PLL | RCLK=26MHz | 4[us] | | |
| | RCLK=52MHz | 2[us] | | |
| tCNFG_LOCK_PERIOD | CNFG_LOCK_PERIOD=2'b00 RCLK=26MHz | 103[us] | | |
| | CNFG_LOCK_PERIOD=2'b00 RCLK=52MHz | 51.5[us] | | |
| Teidl_stb | RCLK=26MHz | | 12[us] | Time from first STB, after EIDL, on Device Rx to STB on Device Tx. |
| | RCLK=52MHz | | 6[us] | |
| Tactivate | CNFG_LOCK_PERIOD=2'b00 RCLK=26MHz | | 750[us] | Time from first STB on Device Tx to first SYN LSS on Device Tx. |
| | CNFG_LOCK_PERIOD=2'b00 RCLK=52MHz | | 380[us] | |
| Tlidl_lidl | All | | 40[SI] | Time from LIDL on Device Rx to LIDL on Device Tx. |
| N_LSS_SYN/ N_LSS_DIR | All | 8[LSSes] | | |
| Required COMs for Symbol lock | All | 3[Symbols] | | See Chapter 8.2, 8.6.1, and 8.6.4 |
| tLB_ACK | BUSIF16=1 | | 10[SI] | See Chapter 8.3 |
| | BUSIF16=0 | | 9[SI] | |
| tDIR_SW | BUSIF16=1 | | 8[SI] | See Chapter 8.6.1, 8.6.2, 8.6.3, and 8.6.4 |
| | BUSIF16=0 | | 7[SI] | |

# 8 Timing Diagram

## 8.1 Reset and Activation (Exiting from Dormant state)

### 8.1.1 For UHS-II DEVICE (HOST_MODE=0)

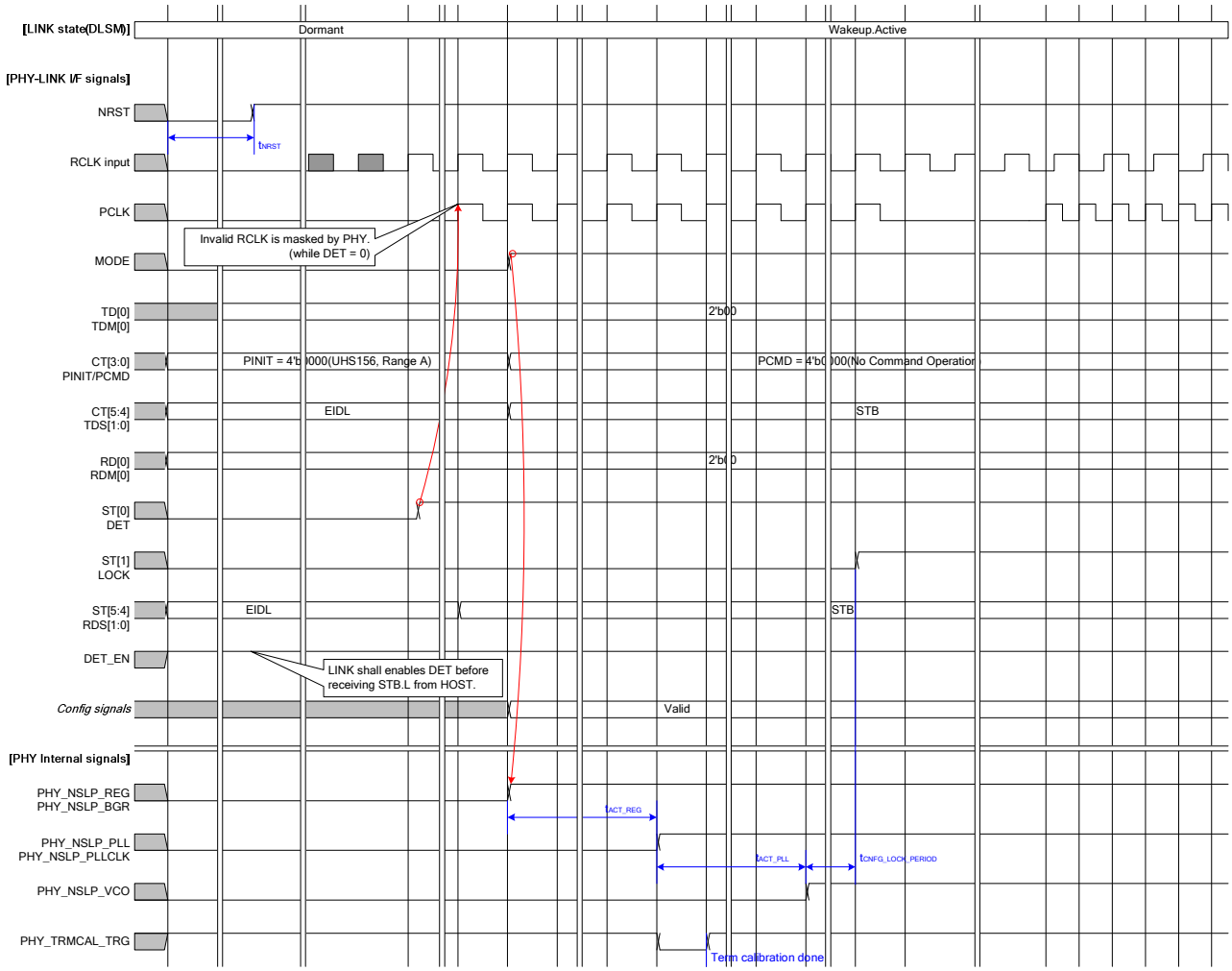


**Figure 33 Reset and Activation (HOST_MODE=0)**

### 8.1.2 For UHS-II HOST (HOST_MODE=1)

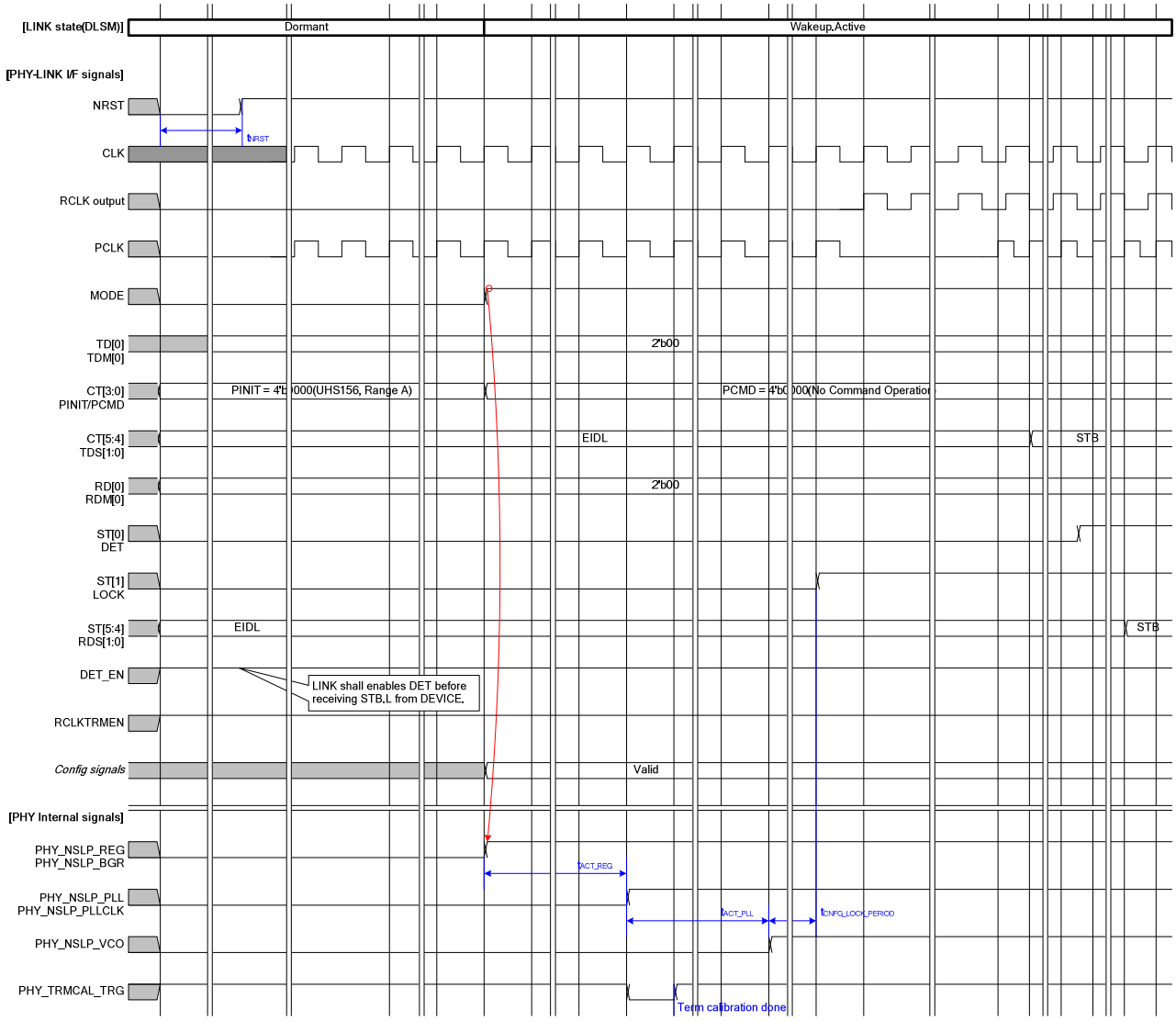


**Figure 34 Reset and Activation (HOST_MODE=1)**

## 8.2 Packet Transfer in Low Power Mode

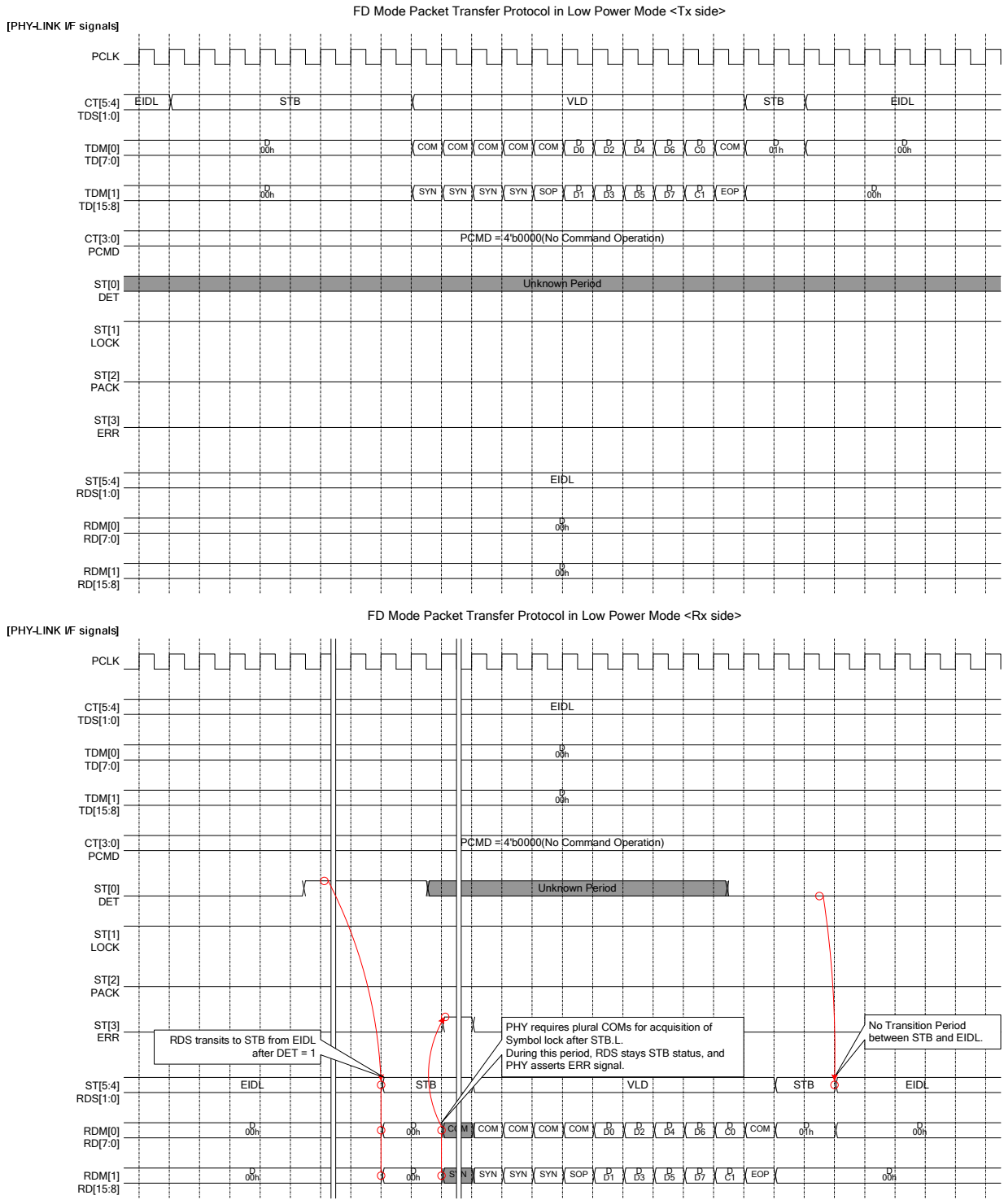


**Figure 35 Packet Transfer in Low Power Mode**

## 8.3 Loopback Control for DATA Burst Streaming

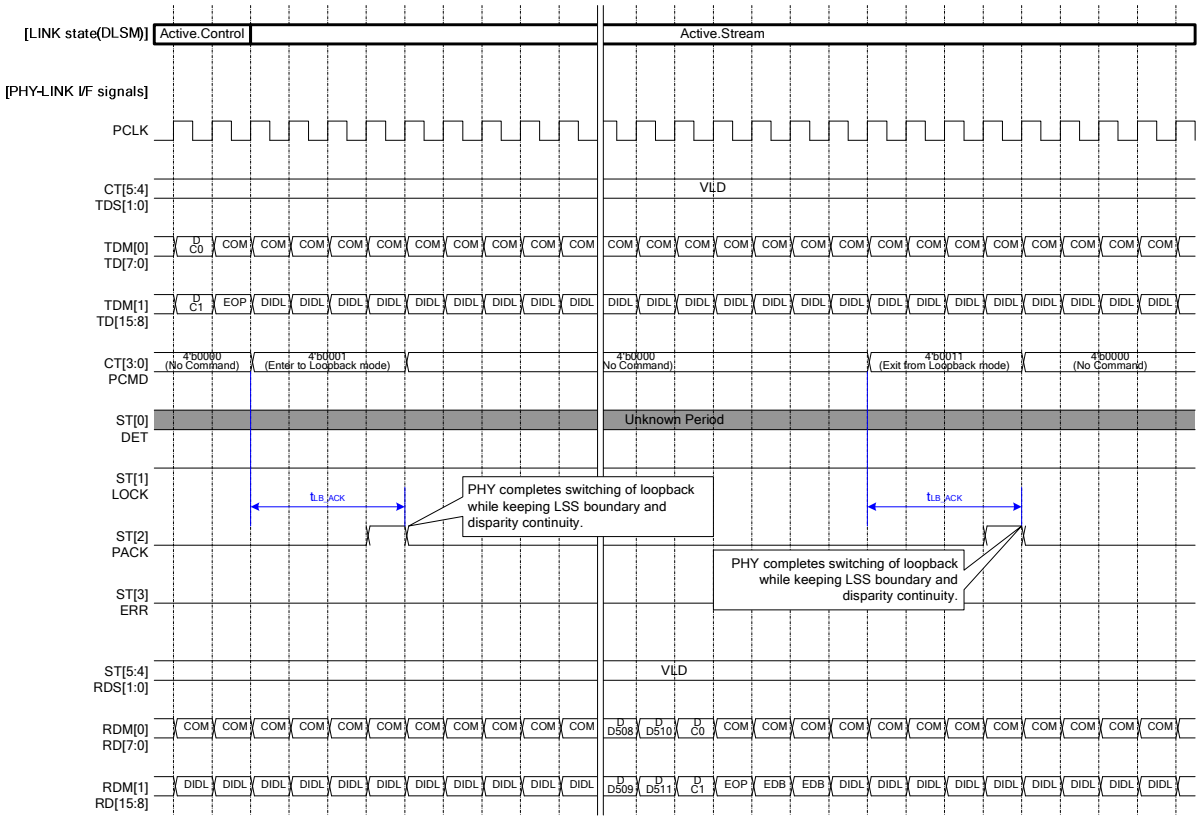


**Figure 36 Loopback Control for DATA Burst Streaming**

# 8.4 8B10B decode error Occurence during Packet Transfer

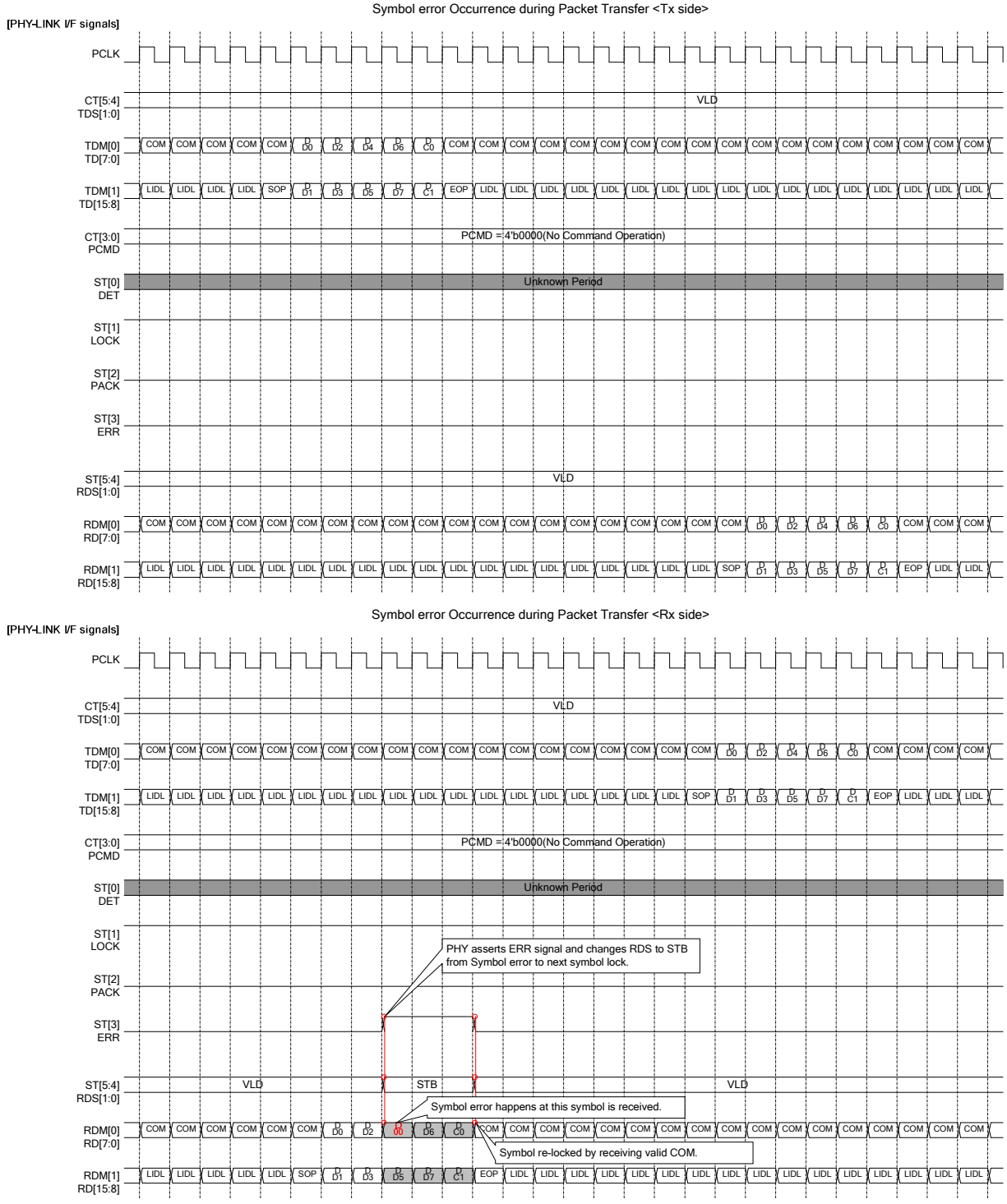


**Figure 37 Example of 8B10B decode error occurrence**

# 8.5 Disparity error Occurence during Packet Transfer

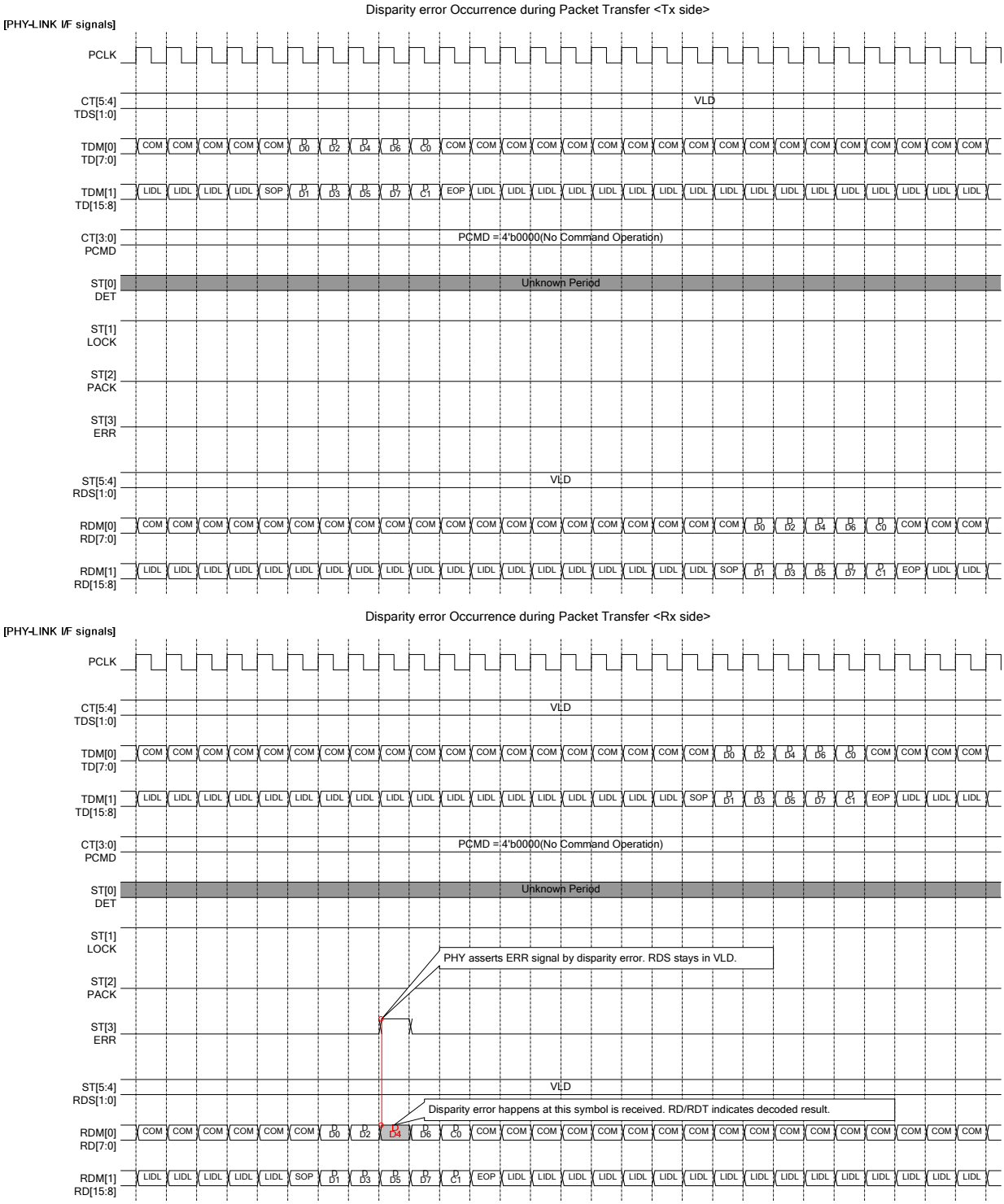


**Figure 38 Example of Disparity error occurrence**

# 8.6 Switching of Duplex Mode

## 8.6.1 Switching from FD to HDIN

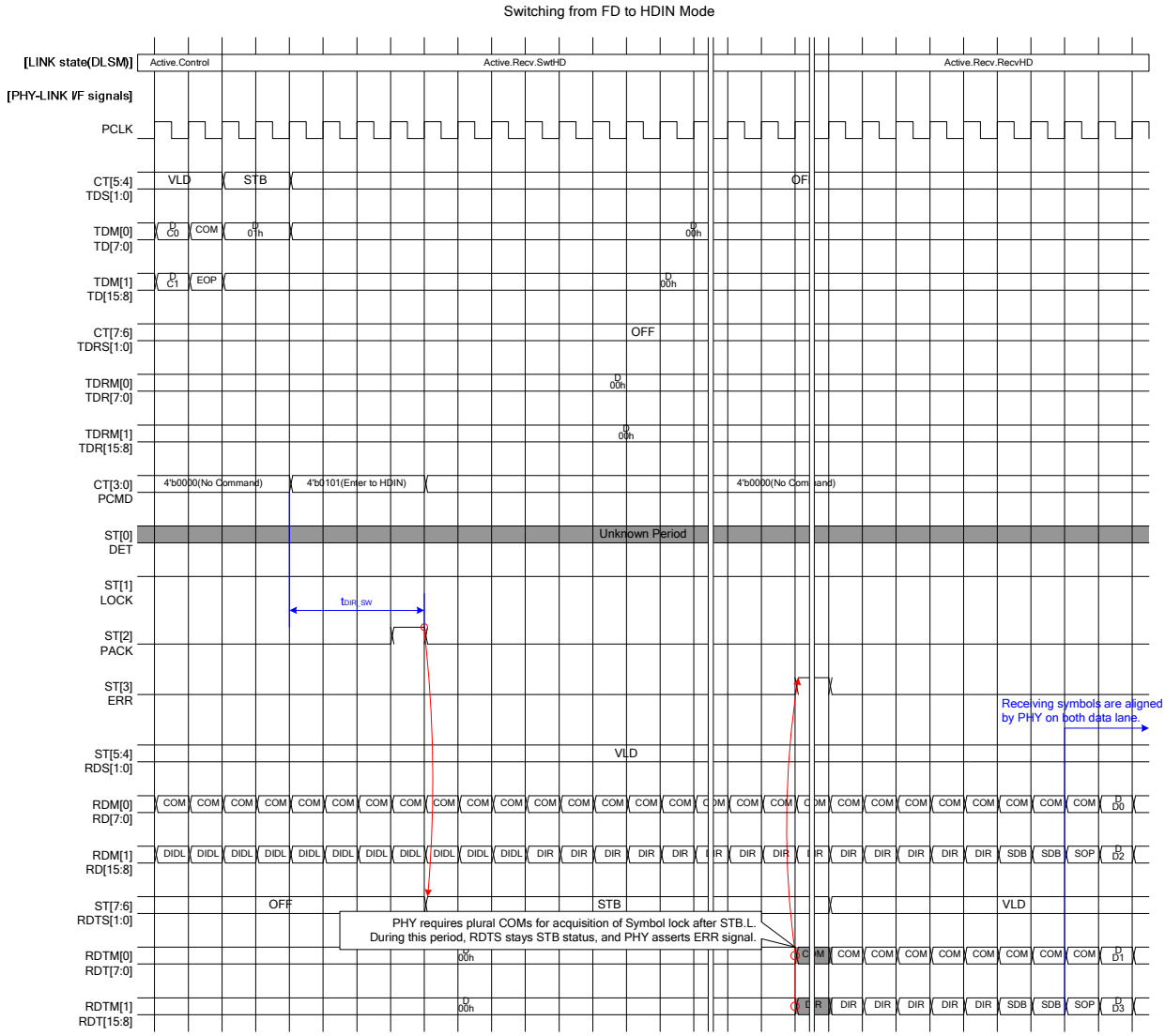


**Figure 39 Switching from FD to HDIN**

## 8.6.2 Switching from FD to HDOUT

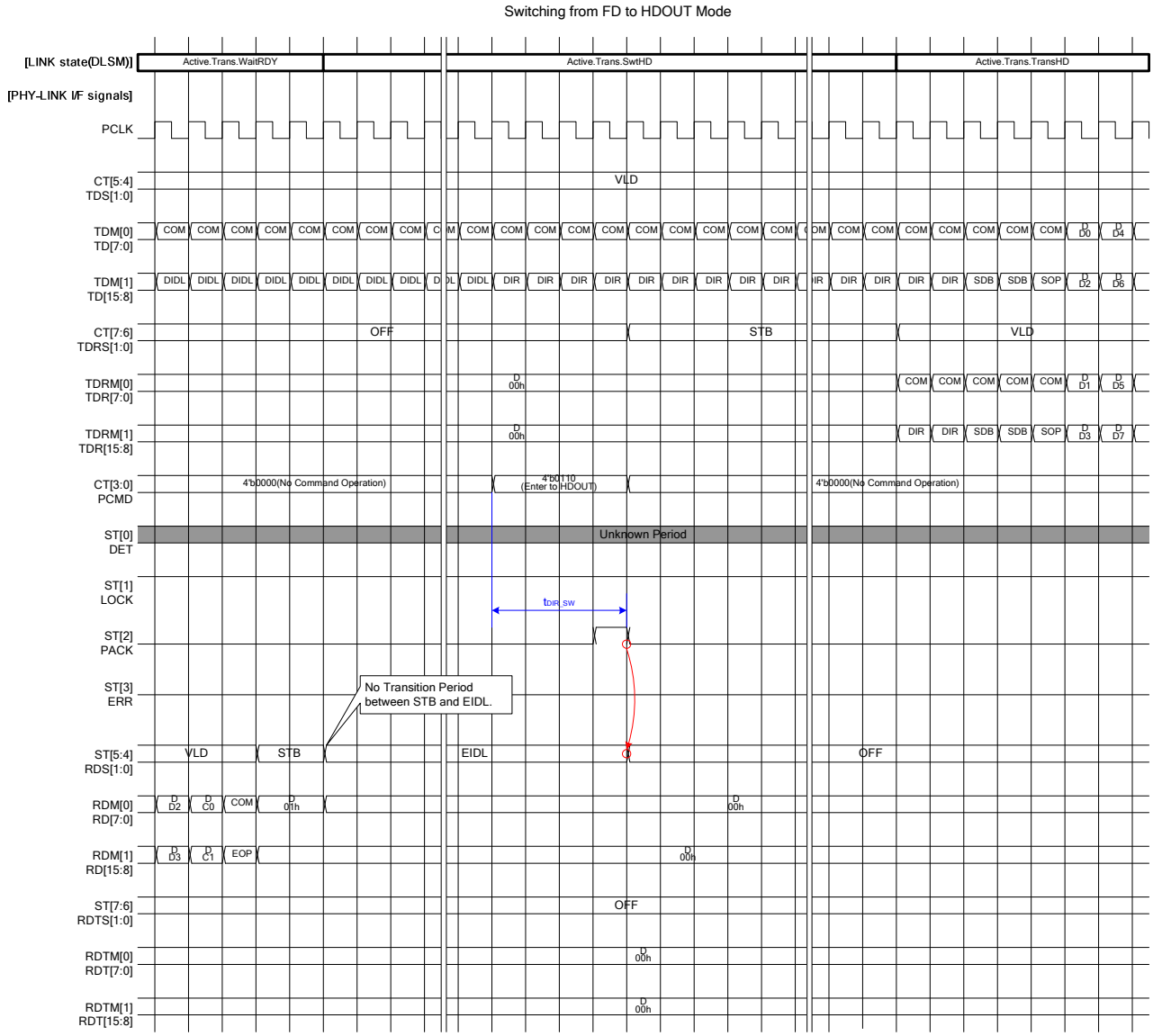


**Figure 40 Switching from FD to HDOUT**

## 8.6.3 Switching from HDIN to FD

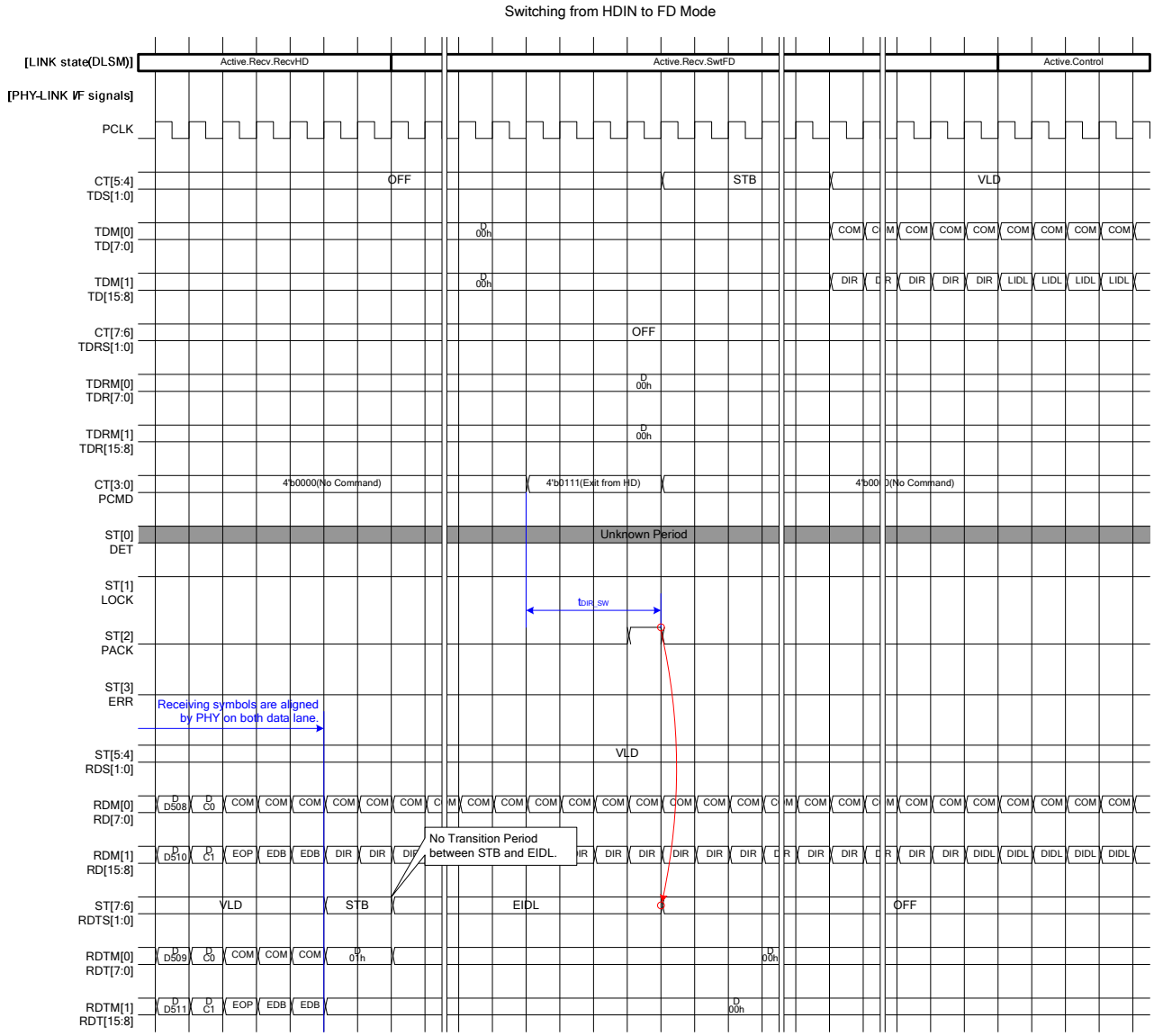


**Figure 41 Switching from HDIN to FD**

## 8.6.4 Switching from HDOUT to FD

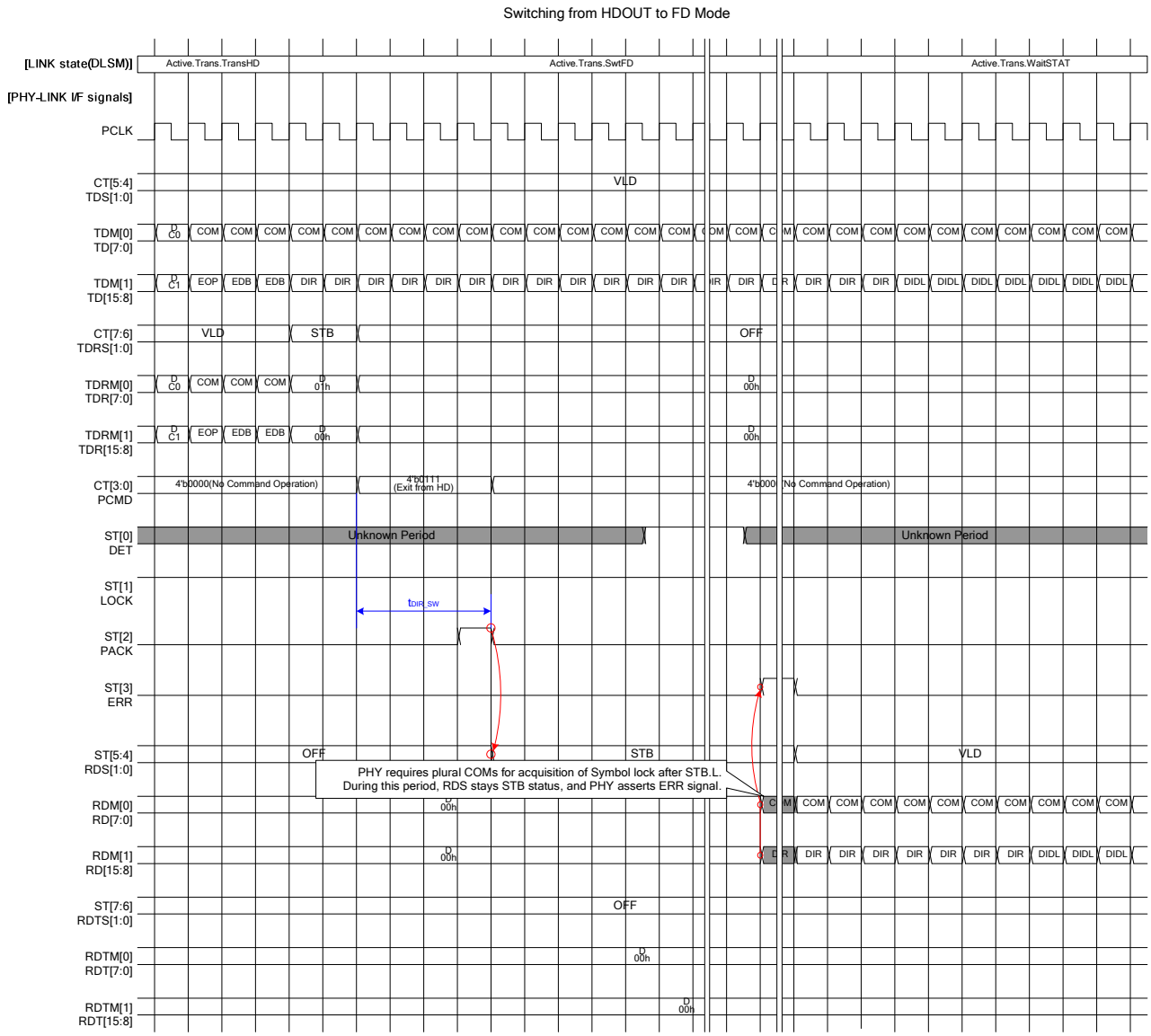


**Figure 42 Switching from HDOUT to FD**

# 8.7 Enter to Dormant

## 8.7.1 For UHS-II DEVICE (HOST_MODE=0)

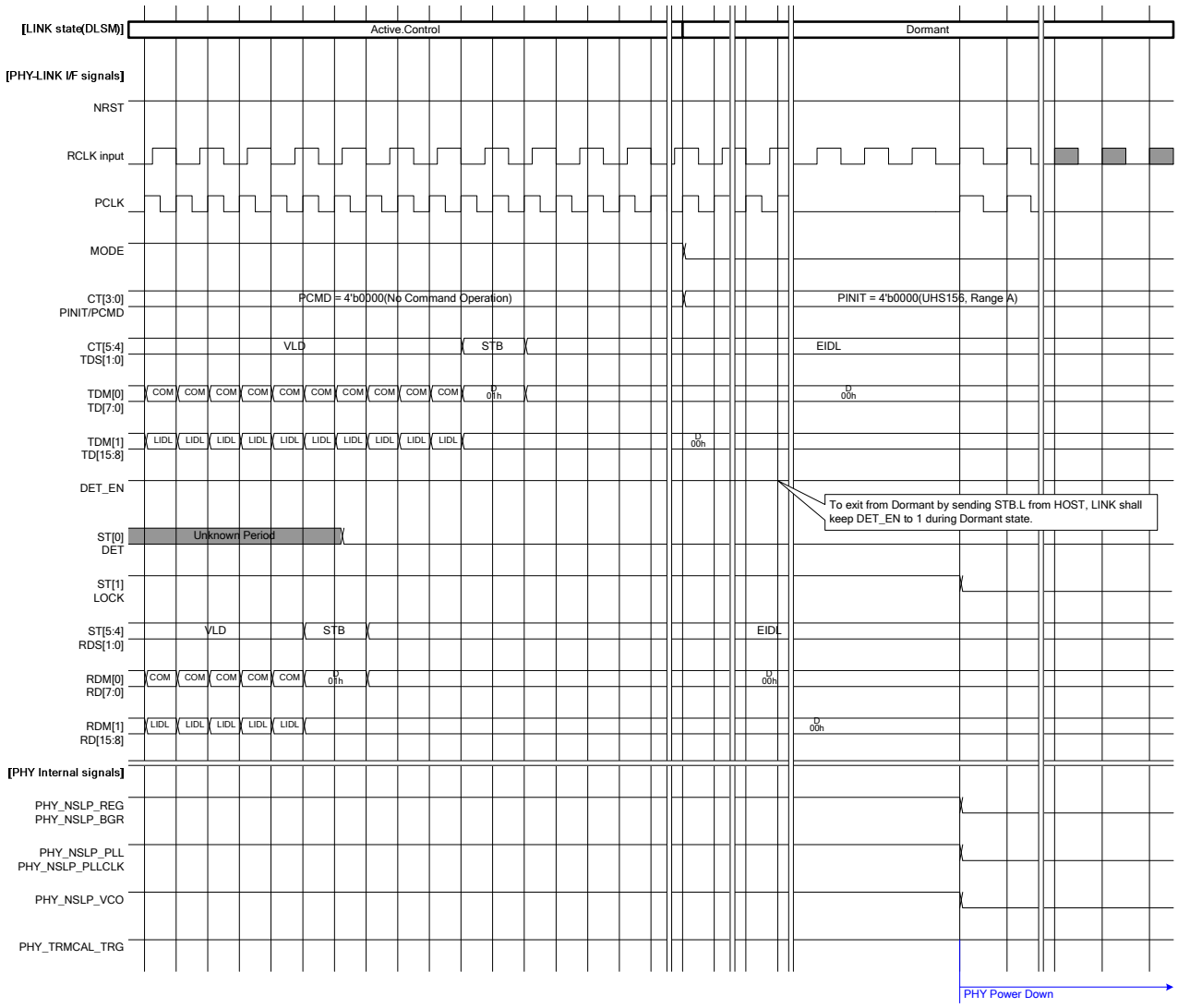


**Figure 43 Enter to Dormant (HOST_MODE=0)**

## 8.7.2 For UHS-II HOST (HOST_MODE=1)

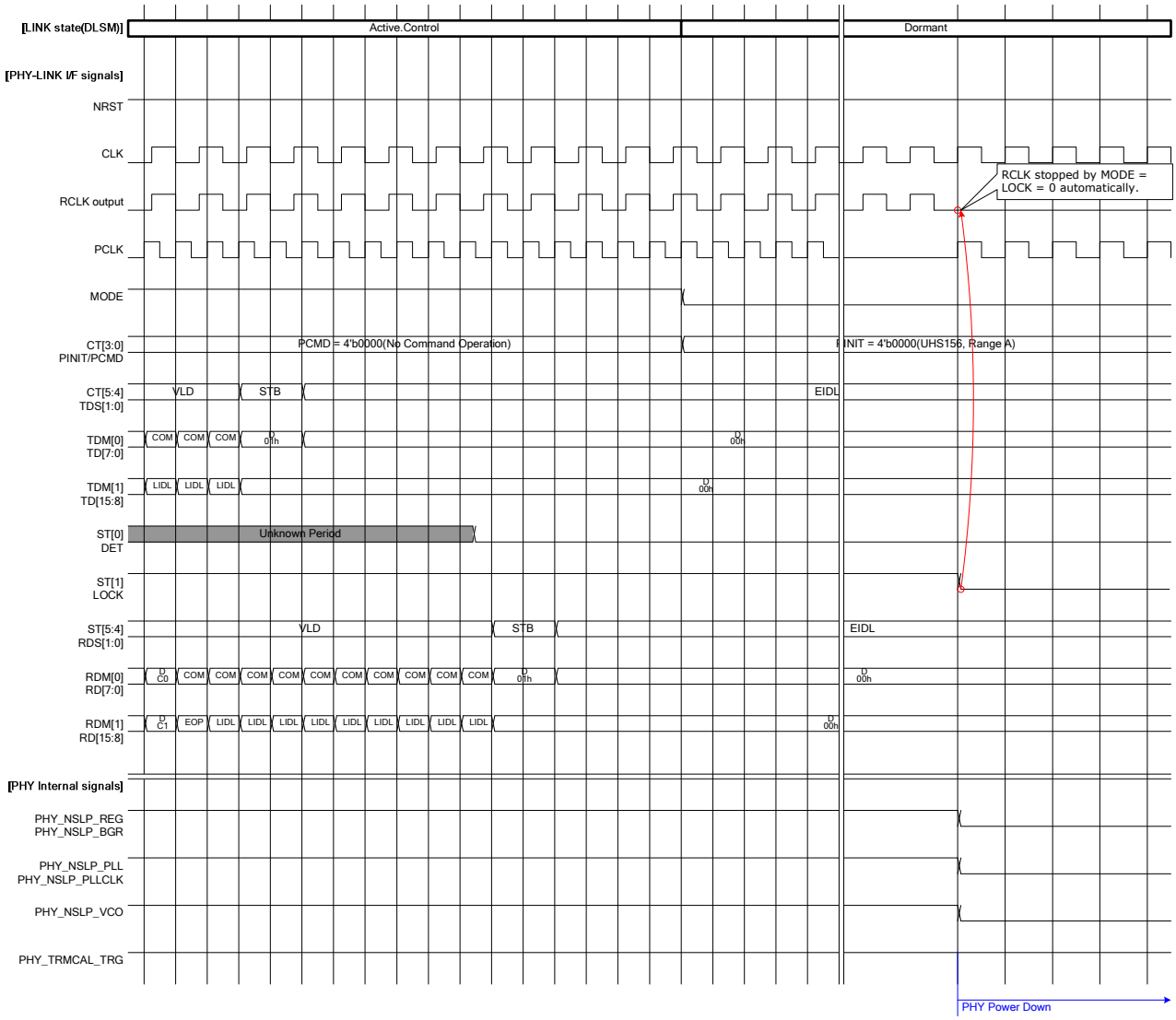


**Figure 44 Enter to Dormant (HOST_MODE=1)**

# 8.8 PHY Test Mode

During PTM_EN=1, PHY enters each test mode without controlling by LINK as following.

## 8.8.1 Disconnect Mode At Once, Backward Loopback

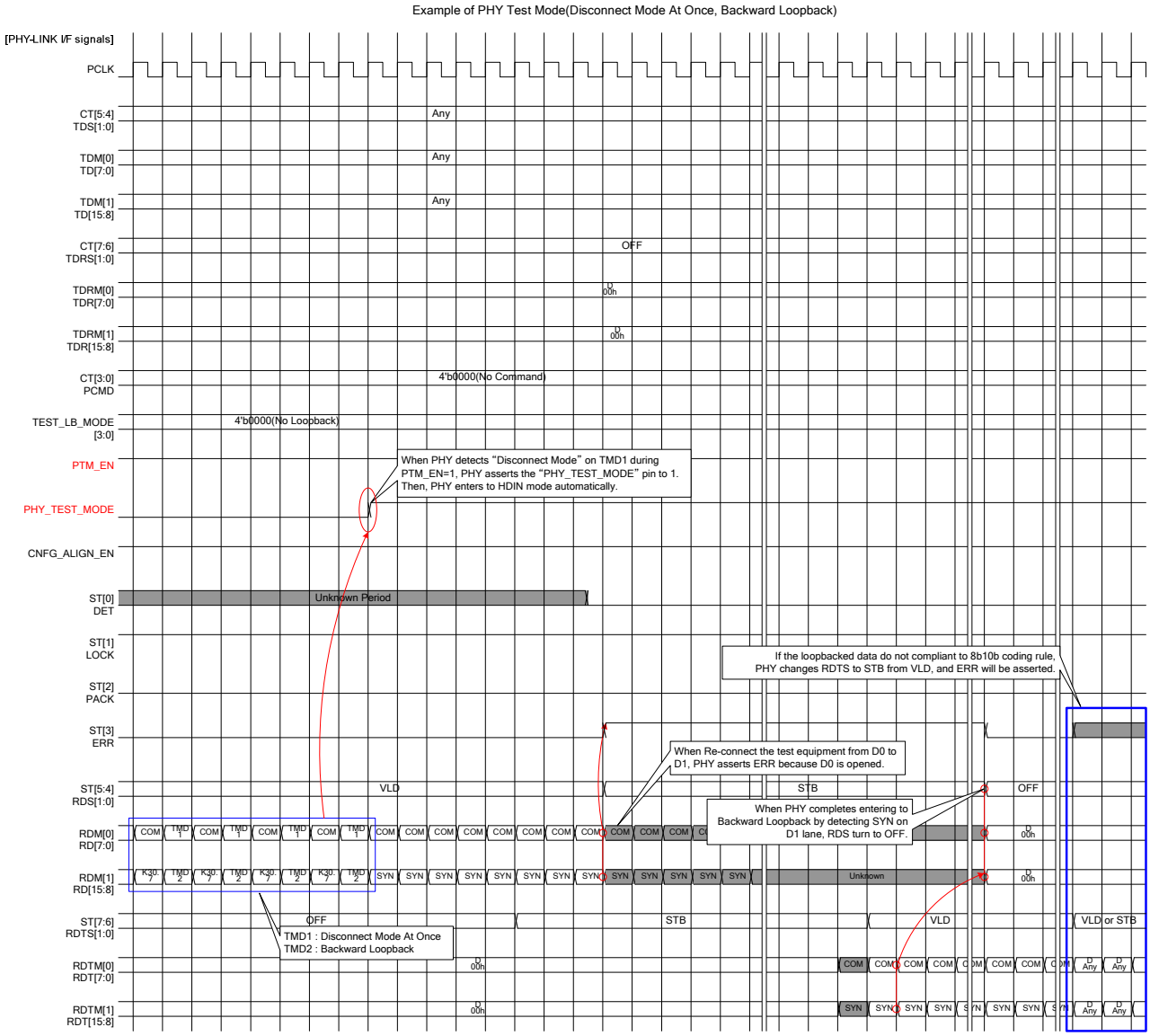


**Figure 45 Disconnect Mode At Once, Backward Loopback**

## 8.8.2 Normal Mode At Once, Forward Loopback

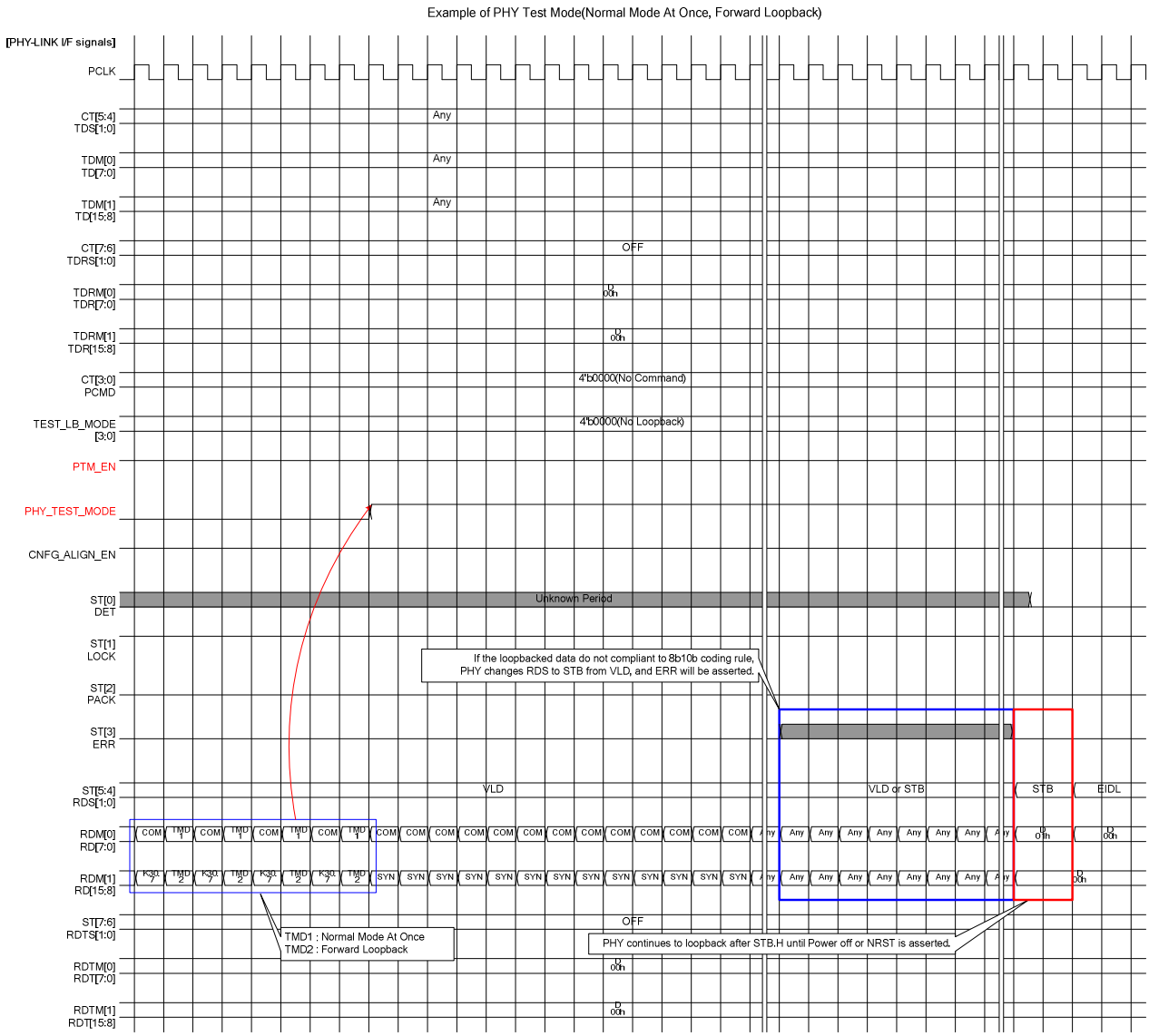


**Figure 46 Normal Mode At Once, Forward Loopback**

## 8.8.3 Disconnect Mode through Re-Sync, Backward Loopback

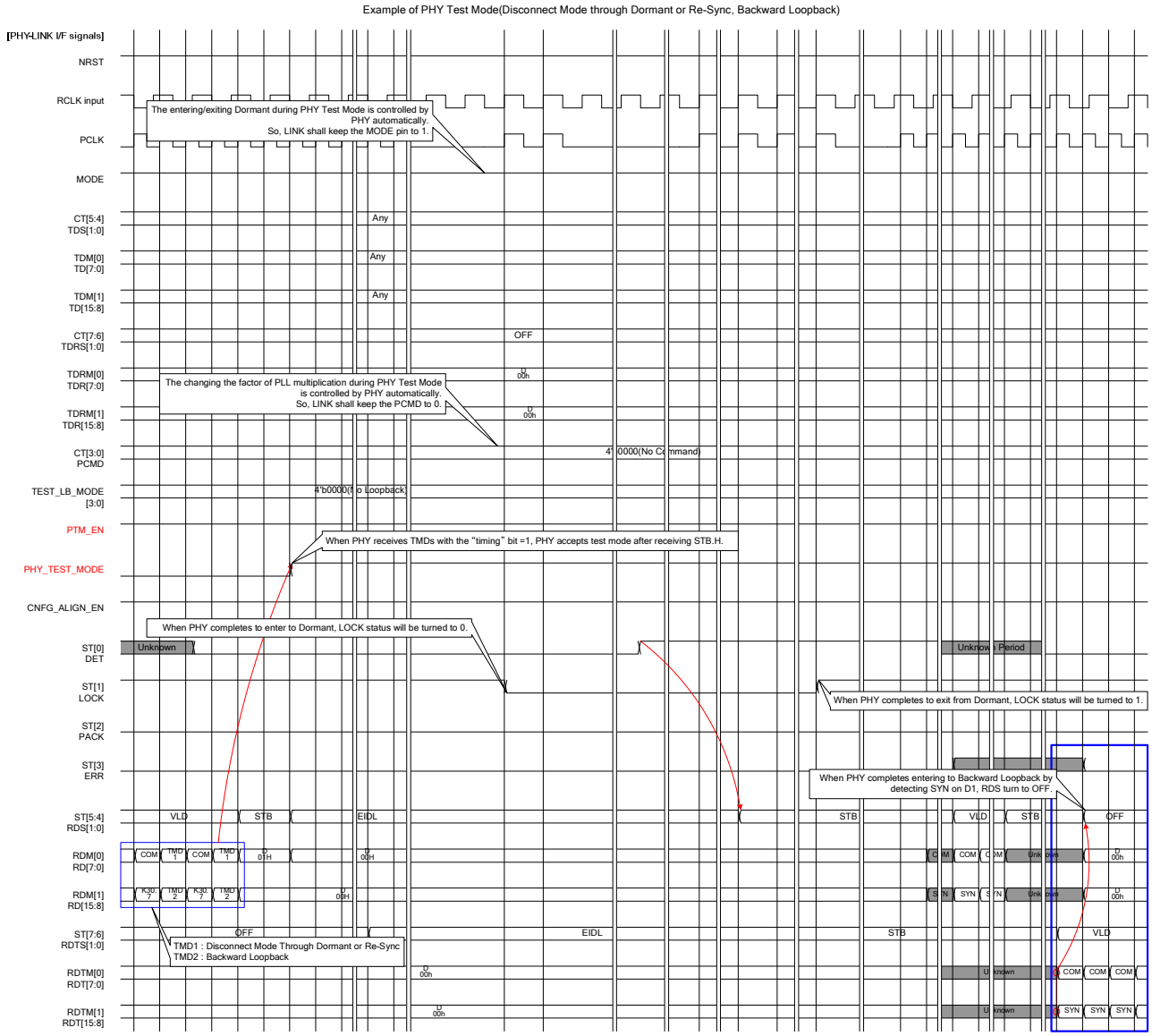


**Figure 47 Disconnect Mode through Re-Sync, Backward Loopback**

# 9 Design Information

## 9.1 Estimated Gate Count

Excluding interconnect area: T.B.D gates (SCAN synthesis is not performed)

## 9.2 Deriverables

-RTL source codes

-Liberty library (.lib/.db), LEF and Verilog simulation model for PMA part

-Example of SDC file for Synopsys Design Compiler

-Documentation (this file)

## 9.3 Required Verilog Macro

Since clock generator in this IP has the clock divider, each F/Fs in this IP use verilog macro "UD" as the delay time of sequential cells as shown below.

```
always @(posedge sysclk or negedge rst_n)begin
    if(!rst_n)begin
        xxx_reg <= #`UD 1'b0;
    end
    else begin
        xxx_reg <= #`UD xxx_in;
    end
end
```

Therefore, user shall define the value of "UD" on simulation and/or synthesis tool as follows;

[In case of NC-Verilog]

```
ncvlog xxx.v -define UD=1
```

[In case of Design Compiler]

```
analyze -f verilog -lib WORK $module_name -define {UD=1}
```

## 9.4 RTL Structure

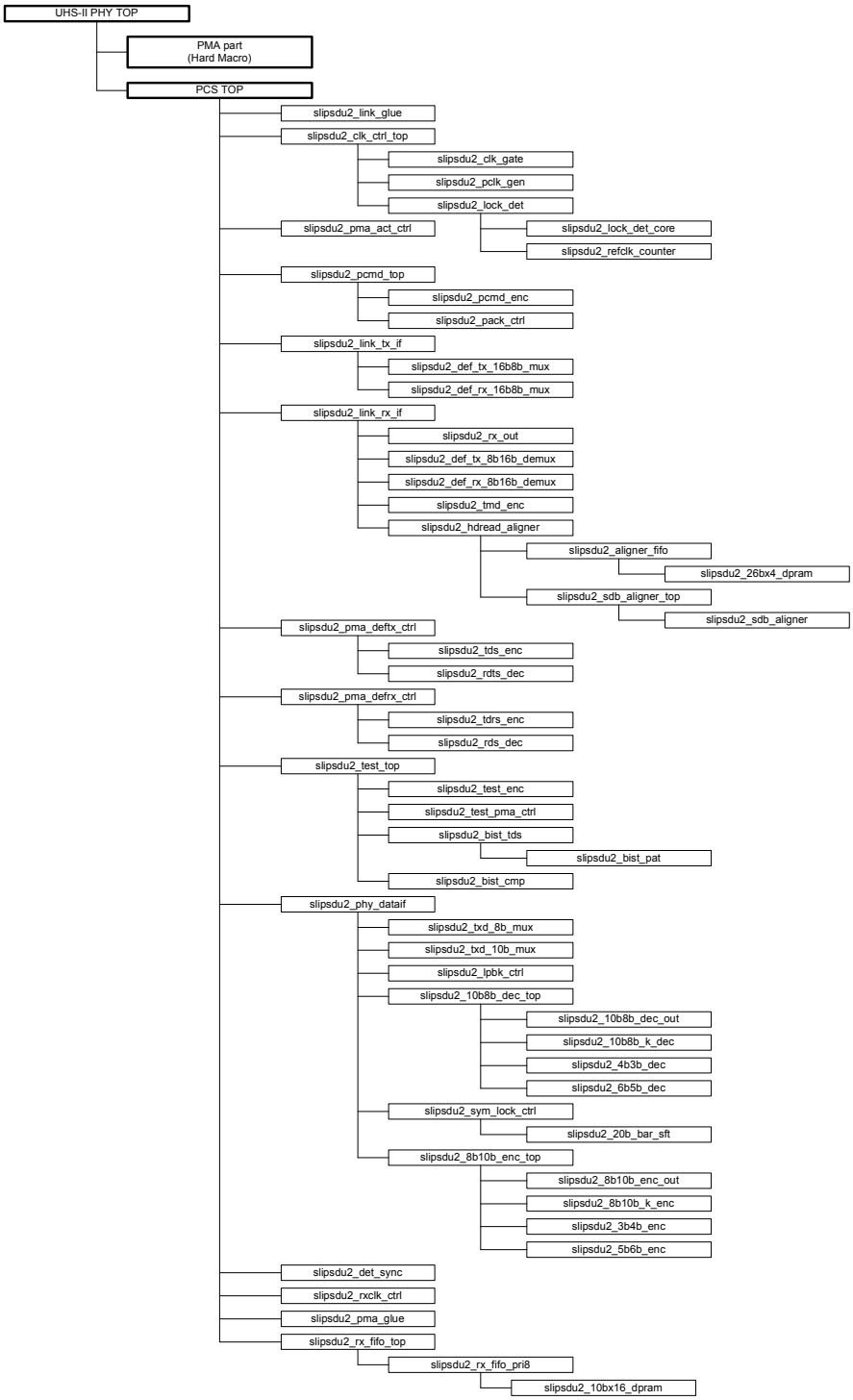


**Figure 48 RTL Hierarchy**

## 9.5 Clock Distribution

Clock distribution of this IP is shown below.

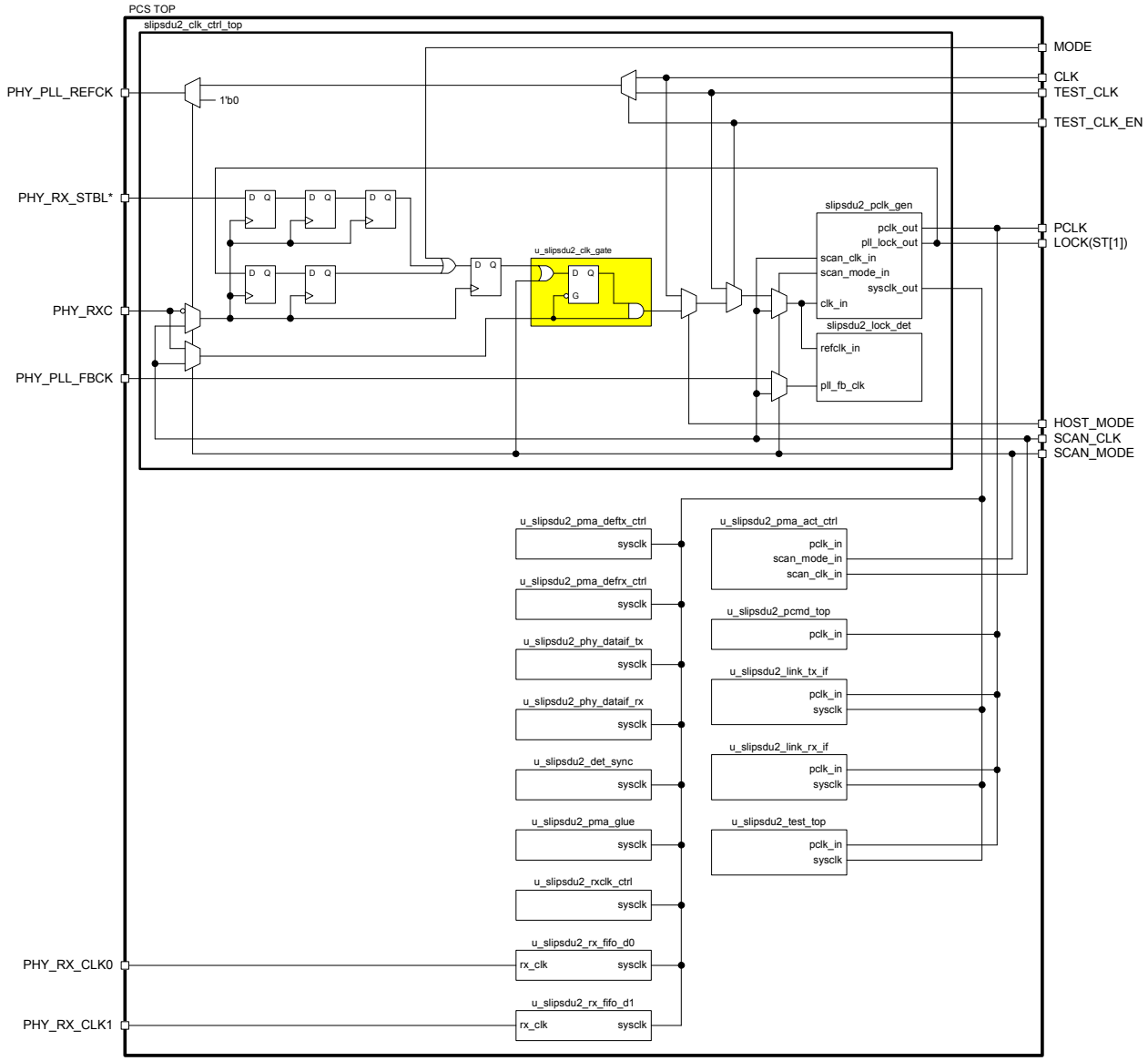


**Figure 49 Clock Diagram**

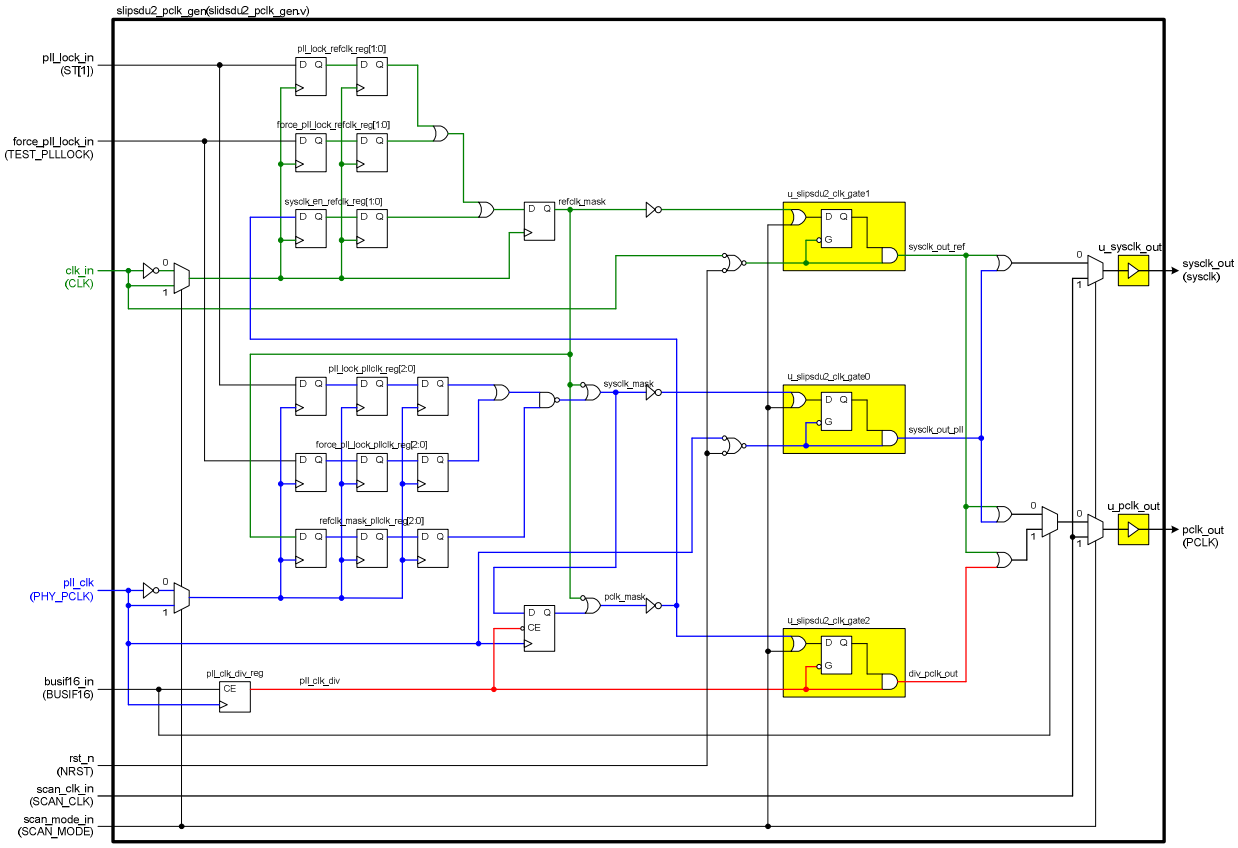


**Figure 50 Details of PCLK generator**

As shown above, there are several clocks from external pins, Analog hard macro (PMA part), or gated clock. All clocks have to be specified as “create_clock” or “create_generated_clock” at synthesis.

When SCAN mode (SCAN_MODE =1), all clock domain is driven by positive edge of the “SCAN_CLK”, so in this mode, test equipment shall supply dedicated clock to this pin.

## 9.6 Clock Table

The table of clocks which are used in this IP is shown below.

### 9.6.1 Input Clocks

**Table 33 Input Clocks**

| Clock Name | Min freq. [MHz] | Max freq. [MHz] | descriptions |
|---|---|---|---|
| PHY_PCLK | 39 | 156 | This is the symbol interval clock from PLL in PHY analog (PLL). |
| PHY_PLL_FBCK | DC | 200 | This is feedback clock from PLL which is used for detecting lock status of PLL. |
| PHY_RX_CLK0 | DC | 172 | This is the recovery clock from CDR. |
| PHY_RX_CLK1 | DC | 172 | This is the recovery clock from CDR. |
| PHY_RXC | 26 | 52 | This is the reference clock for PLL of UHS-II DEVICE. |
| CLK | 26 | 52 | This is the reference clock for PLL of UHS-II HOST. |

The constraint of timing is not required about crossing clock domain because each clocks written in this table are asynchronously.

### 9.6.2 Generated Clocks

The generated clocks by this IP are shown below.

**Table 34 Generated Clocks**

| Clock Name | Min freq. [MHz] | Max freq. [MHz] | descriptions |
|---|---|---|---|
| PCLK | 19.5 | 156 | This is the synchronous clock for PHY-LINK interface. This clock is supplied to LINK by this IP. |
| sysclk | 26 | 156 | This is the system clock for PHY digital. |

The data path between PCLK and sysclk should be synchronized each other.

The truth tables for generating each clock are shown below.

**Table 35 Truth Table for PCLK**

| Status/setting | LOCK(ST[1]) | BUSIF16 | Source clock |
|---|---|---|---|
| PLL is unlocked | 0 | x | CLK/PHY_RXC<br>(26 MHz to 52 MHz) |
| PLL is locked<br>Bus width = 16-bit | 1 | 1 | PHY_PCLK (divided by 2)<br>(19.5 MHz to 78 MHz) |
| PLL is locked<br>Bus width = 8-bit | | 0 | PHY_PCLK<br>(39 MHz to 156 MHz) |

**Table 36 Truth Table for sysclk**

| Status | LOCK(ST[1]) | Source clock |
|---|---|---|
| PLL is unlocked | 0 | CLK/PHY_RXC<br>(26 MHz to 52 MHz) |
| PLL is locked | 1 | PHY_PCLK<br>(39 MHz to 156 MHz) |

As shown above, these generated clocks require the case analysis by STA.

Required case settings for “slipsdu2_pclk_gen” are shown below.

LOCK=0 : pll_lock_in = 0, TEST_PLLLOCK = 0

LOCK=1 : pll_lock_in = 1, TEST_PLLLOCK = 0

BUSIF16 = 0

BUSIF16 = 1

## 9.7 Timing Constraints

### 9.7.1 Clock uncertainty

“set_clock_uncertainty” 0.1 is required for all clock sources.

### 9.7.2 In each clock domain

Static timing check is required in each clock domains by maximum clock frequency + 10% margin.

### 9.7.3 Output delay

There is no output delay timing requirement.

### 9.7.4 Clock skew requirement

No clock skew requirement for each clock domain.

### 9.7.5 Clock edge

In normal mode, all of modules are clocked by “positive edge” clocks except PCLK generator.

In SCAN mode, all of modules are clocked by “positive edge” of SCAN_CLK.

# 10 Limitations

No known limitations and errata.

# 11 REVISION HISTORY

| Date | Rev. | Changes Made | Section Effected |
|---|---|---|---|
| May 9, 2012 | 1.0 | Initial release | - |
| June 6, 2012 | 1.1 | Modified timing specification about “symbol re-lock” | 7 |
| August 15, 2012 | 1.2 | Modified block diagram | 1 |
| January 7, 2013 | 1.3 | Modified function title from “Symbol Alinger” to “Lane Skew Aligner” | 1, 5.4 |
| February 4, 2013 | 1.4 | Modified timing diagram of “Reset and Activation”. | 8.1 |
| July 26, 2013 | 1.5 | Added "RCLKOE" pin.<br>Added descriptions about PLL lock detector.<br>Added timing specification of Teidl_stb, Tactivate, Tlidl_lidl. | 3, 4, 5.2<br>5.6<br>7 |
| July 31, 2013 | 1.6 | Added State transition diagram of PHY Test Mode.<br>Modified recommended parameter for PTM_EN. | 5.8.1.2<br>6 |
| August 28, 2013 | 1.7 | Modified specification of Test controller.<br>Added procedures of manufacturing test for PMA. | 3.3, 5.9 |
| September 13, 2013 | 1.8 | Added design information for implementation to ASIC. | 9 |
| | | | |

# SD UHSII PHY IP PCS Family Datasheet



Silicon Library Inc.
301,Center for Collaborative Innovation and Incubation, Meiji University 2-3227,
Mita, Tama-ku, Kawasaki, Kanagawa, Japan, 214-0034
Phone: 81-50-5527-7974
Fax: 81-50-3737-7299

Silicon Library's home page can be found at:
http://www.siliconlib.com