

UHS-II Protocol & Performance Tests

Ver 0.1a

- Preliminary -

Note: This document defines the UHS-II Protocol and Performance tests to be implemented on the VTE-4100 tester.

Introduction:

The VTE-4100 Protocol / Performance tests will be executed by the TP (MBLZ) under the control of a VTE test script. The communication between the VTE and the TP will be performed via the TPCP protocol. Each test item will be given a Test Number. The test script running on the VTE-4100 application will call for individual tests to be executed by the TP (will provide required test data via TPCP). Upon completion of the test the TP will return the results to the VTE via TPCP.

UHS-II Protocol Tests

The list and description of the Protocol Tests are contained in the document SDA spec:

Part 1 UHS-II Protocol Test Guidelines Ver 1.00 Final 140714.pdf

This document organizes tests in 6 groups.

1 Systems Tests

- 1-1 Interface Speed Test (FD Mode)
- 1-3 Interface Speed Test (2L-HD mode)
- 1-5 Direction of D0 and D1
- 1-6 Direction of D0 and D1 on 2L-HD mode write
- 1-7 Direction of D0 and D1 on 2L-HD mode read
- 1-9 Block Mode and Byte Mode
- 1-11 Device operation before completing Device Initialization without Boot Code Loading
- 1-13 Device operation after completing Boot Code Loading

2 Link Layer Tests

- 2-1 Number of SYN LSS:
- 2-3 Initial Value of Node ID of Device
- 2-4 SID and DID fields in Header of Boot Device before Enumeration
-
- 2-64 Valid Transmission Gap in Active Stream

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3 CM-Tran Layer Tests

- 3-1 Packet Format of CCMD
- 3-2 Packet Format of DCMD
- 3-3 Packet Format of RES
- ...
- 3-93 Device Operation of Reserved Bits in the Packet when Handling Broadcast Packet

4 SD-Tran Tests

- 4-1 CCMD Format
- 4-2 DCMD Format
- 4-3 RES Format
- ...
- 4.43 Fractional Data Burst in LM=0 in SD-TRAN

5 2L-HD Mode Tests

- 5-1 Framed DATA Packet in Block Mode
- 5-2 Framed Data Packet in Block Mode when Payload length is $4*s+1$
- 5-3 Framed Data Packet in Block mode when Payload length is $4*s+2$
- ...
- 5-12 Duplex mode switching

6 Additional Lanes Tests

- 6-1 Configuration Number of Lanes and Functionality
- 6-2 Activating Additional Lanes through GO_DORMANT_STATE command
- 6-3 Framing Rule in 2D1U-FD and 2D2U-FD write command
- ...
- 6-8 Write transaction for 2D1U-FD or 2D2U-FD – Low Power Mode

7 Custom Tests

- 7-1 Configuration Number of Lanes and Functionality
- 7-2 Activating Additional Lanes through GO_DORMANT_STATE command

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UHS-II Test Sequence

The numbering and nomenclature used in this document should be used for reference also in the tests implemented on the VTE-4100 tester. Given that the numbering in the spec is counterintuitive it should be used in parenthesis, the actual order of the tests being determined in a logical fashion based on the typical flow of operations executed by real UHS-II devices:

1. PHY Initialization Tests:

COM + SYN Activation

COM + BSYN activation (Boot Code Loading Sequence)

2. Link Layer Tests:

Wake-Up Test

Link Layer Tests 2.1 – 2.64

3. Configuration Tests:

Device_Init test

Enumeration Test

Checking Capabilities Registers

Inquiry_Config

P2P Read CCMD

Writing Setting Registers

Set_COMMON_CONFIG

P2P Write CCMD

4. Operations in Active State:

Update Settings Registers

CM - Tran Tests (3.1-3.93)

3.22 Data Transaction

Read Performance Test

Write Performance Test

SD – Tran Tests (4.1-4.43)

CMD0/CMD8/CMD55/ACMC41

5. 2L-HD Tests

6. Additional Lanes Tests

7. Custom Tests

Note: Items in yellow were already preliminary implemented and tested
Items in green are top priority

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