TESTMETRIX

UHS-II TP / Host Interface

Ver 0.1b

- Preliminary -

Note: This document defines the interface between the UHS-II Test Processor and the Host (VTE test script running on the Host computer).

Introduction:

The VTE-4100 application program (Host) runs test scripts that communicate via USB with the Test Processor (TP) implemented in Virtex via a Microblaze (MBLZ) processor. The VTE-4100 contains a USB interface board which performs the interface between USB and Virtex.
The TP performs the communication with the Host, implements the UHS-II Transaction Layer, and interfaces with the Link layer.

The communication between the TP and the Host is implemented by means of a Host Communication I/O Module (HCIOM) implemented in Virtex, which is used as the hardware platform onto which a proprietary TE Communication Protocol (TECP) is implemented.

The TPCP on the VTE-4100 side is implemented in the form of C-functions that can be executed from VTE Test Scripts. The TPCP on the TE side needs to be implemented in MBLZ.

The TPCP for UHS-II testing should be kept as close as possible to the current TPCP employed by the VTE-4100 for UHS-I testing.

Host Communication IO Module (HCIOM)

In essence the Host Communication IO Module (HCIOM) consists of an array of 64 x 64 = 4096 selectable blocks (BS) of variable depth 8 bit arrays, with the associated decoding logic. Each BS depth is customized to the purpose it is used for.
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The TPCP on the VTE-4100 side (Host) consists of the following steps:

- Open the communication channel with the TP
- Select a specific BS
- Write / read data to/from the specific BS

Note: Up to the max number of bytes allowed for a specific BS can be written or read a time.

Similarly, the TPCP on the TP side consists of the following steps:

- Select a specific BS
- Write / read data to/from the specific BS

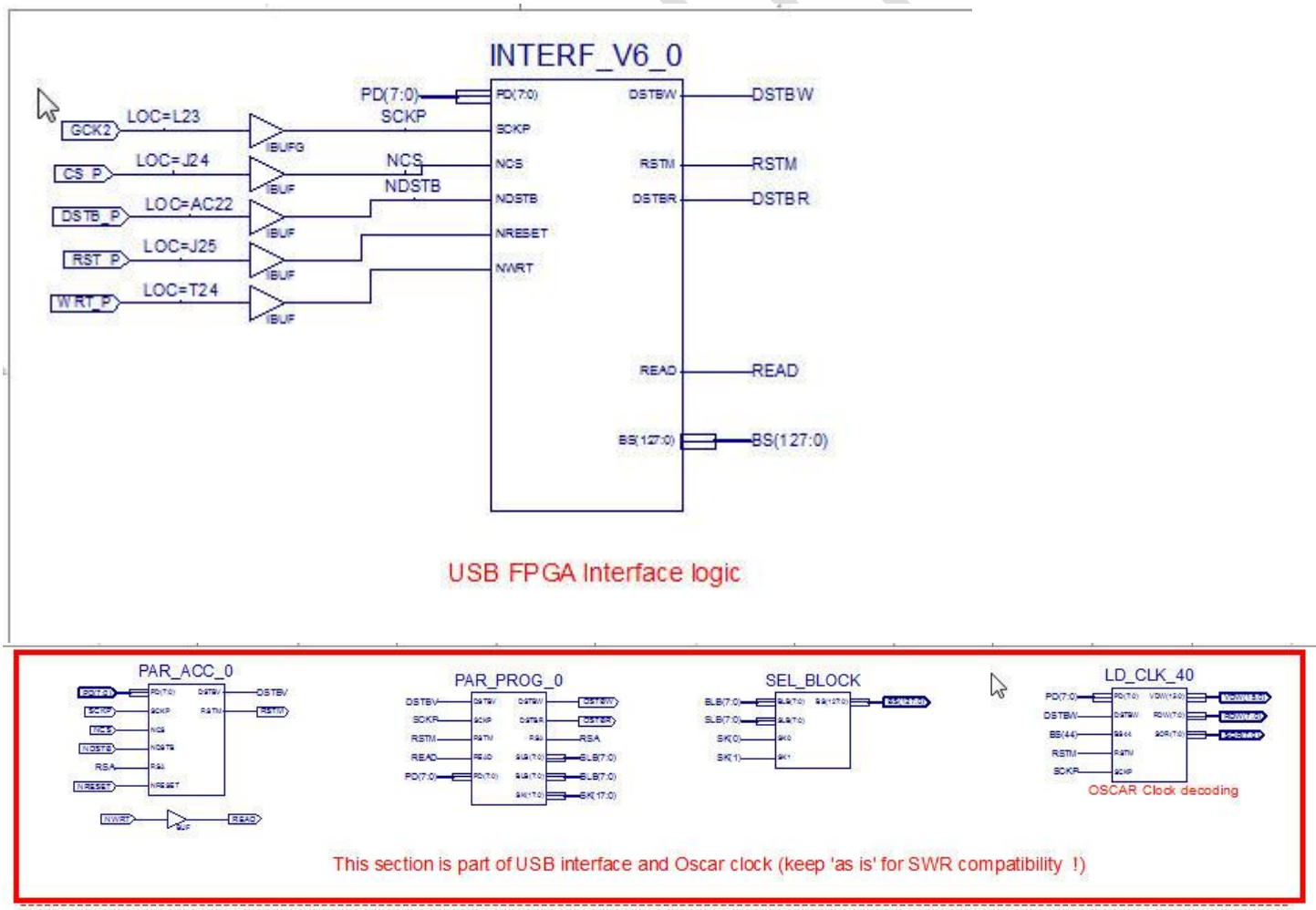
HCIOM hardware interface

Note: This section is provided for reference. Details regarding the software implementation of the BS addressing and Read/Write operation will be provided shortly

The HCIOM presented in this section is based on the UHS-I tester implementation and is not finalized yet).

The module presented below is the current implementation of the Host interface for the UHS-I tester and is to be used as starting point for the TP / Host interface:

- 8 bit bus with CS, RST, DSTB, WRT controls; EPPCK 48MHz.
- Contains additional blocks with logic to decode the USB signals and provide control signals



Signals Description:

GCK2 (SCKP) [input] Fix 48MHZ clock coming from our USB interface board
CS_P: [input] Chip select from USB (active high when the SWR is addressing the FPGA for WR/RD transfers)
RSTN_P: [input] Reset signal (active low, corresponds to RSTM output - active high)
DSTB_P: [input] Data strobe signal (active high)
WRT_P [input] Bus direction control (high=READ, low=WRITE)
PD(7:0) [input] 8 bit bus from the USB interface board PDE (7:0)
RSTM: [output] reset active high
DSTBW: [output] data strobe write (active high)
DSTBR: [output] data strobe read (active high)
BS(127:0) [output] 128 bits for block select (active high)

Notes: 1.The highlighted signals are used to select registers/Microblaze/memory blocks for Write/Read from/to the USB bus PDE (7:0)
2. BS0 is used as Command register
3. RSTM is used only for the USB interface logic reset and is not used to reset the processor or other logic. (Additional Reset signals added using registers, mapped to a particular BS block (i.e. RST bit in Command register "COMM_M2")

TP Communication Protocol (TPCP)

The array of 4096 Blocks of (BS) have dedicated purposes in the current VTE-4100 UHS-I test applications. For software compatibility purposes the allocation of the main blocks should be kept as close as possible to the current use. In rest changes should be made as needed for UHS-II testing.

The BS definitions for the UHS-II Testing configurations are:

Block#	Name	Depth	Description
BS0	TP Control Register	1 B	Control operation of TP
BS1	TP Status Register	2 B	Stores TP Status
BS2	DUT Error Register	1 B	Stores DUT Error Status
BS3	TP Execution State Reg	1 B	
BS5			
BS6	TP Code Index	6 KB	(will elaborate later)
BS7			
BS8	Watchdog Timer	5 B	Timer used for Testing

TP Control Register:

This register is written by the Host only. It is used to tell the TP what test to execute, and in general to control the operation of the TP.

The TP Status Register:

This register is written by the TP only. It is used to inform the Host about the status of a specific test execution.

Blocks (BS) for data transfer between Host and TP:

Up to 4096 BS of variable depth arrays are used for sending/receiving data between Host and TP.

Test Parameters BS:
The Test Parameters BS are written by the Host and contain parameters to be used by specific tests

Test Results BS:
The Test Results BS are written by the TP and contain data related to the execution of a specific test

TPCP Protocol Implementation:

The Host side drives the activity of the TP and communicates with the TP in the following manner:

The basic Host implementation of the TPCP:

- Check TP Status Register
- Write TP Control Register
- Loop checking the TP Status Register
- Update TP Control Register

The TP implementation of the TPCP (Main Loop):

- Check TP Control Register
- Update TP Status Register
- Execute Requested Test
- Update TP Status Register