TESTMETRIX

UHS-II Transaction Layer / Host Interface

Ver 0.1a

-Preliminary -

Note: This document defines the interface between the UHS-II Transaction layer implemented in Microblaze (MBLZ) and the Host (VTE control script running on the Host computer).

Introduction:

The communication between the Transaction Engine (TE) driving the Transaction Layer and host is implemented by means of a Communication I/O Module implemented in Virtex which is used as the hardware platform onto which a proprietary Virtex Communication Protocol (VCP) between the Host and Virtex designs is implemented.

In the Case of UHS-II testing the test processor is MBLZ. Therefore the Virtex side of the VCP needs to be implemented in MBLZ.

The VCP for UHS-II testing should be kept as close as possible to the current CTP employed by the VTE-4100 for UHS-I testing.

Communication IO Module (CIOM)

In essence the CIOM consists of an array of 64 x 64 = 4096 selectable blocks (BS) of variable depth 8 bit arrays, with the associated decoding logic. Each BS depth is customized to the purpose it is used for.

.

The Host opens the communication channel with the tester (USB based), selects a specific block, and writes or reads data to/from that block. All or a lower number of bytes than max number of the BS can be written or read a time.

The TE – Host interface implementation consists of selecting a specific BS and reading/writing data to/from the selected BS.

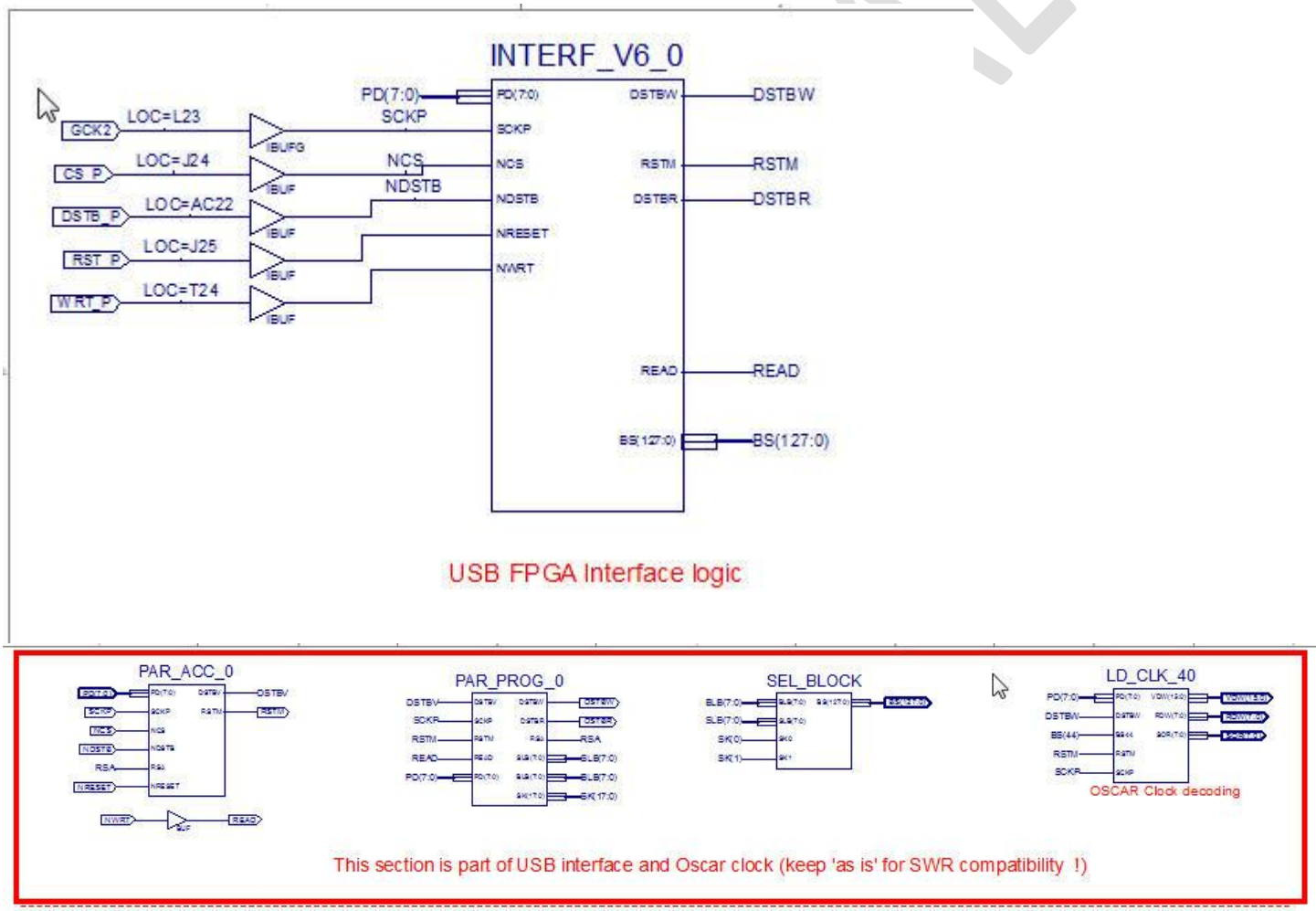
The control signals for writing / reading to/from the array of BS need to be driven by the NE to access the BS array.

CIOM hardware interface

Note: Tthis section is based on the UHS-I test implementation and is not finalized yet)

The module presented below is the current implementation of the Host interface for UHS-I testing designs and is to be used as starting point for the TE-Host interface:

- 8 bit bus with CS, RST, DSTB, WRT controls; EPPCK 48MHz.
- Contains additional blocks with logic to decode the USB signals and provide control signals



Signals Description:

GCK2 (SCKP) [input] Fix 48MHZ clock coming from our USB interface board
CS_P: [input] Chip select from USB (active high when the SWR is addressing the FPGA for WR/RD transfers)
RSTN_P: [input] Reset signal (active low, corresponds to RSTM output - active high)
DSTB_P: [input] Data strobe signal (active high)
WRT_P [input] Bus direction control (high=READ, low=WRITE)

PD(7:0) [input] 8 bit bus from the USB interface board PDE (7:0)
RSTM: [output] reset active high
DSTBW: [output] data strobe write (active high)
DSTBR: [output] data strobe read (active high)
BS(127:0) [output] 128 bits for block select (active high)

Notes:
1.The highlighted signals are used to select registers/Microblaze/memory blocks for Write/Read from/to the USB bus PDE (7:0)
2. As a general rule the BS0 is currently used as Command register
3. RSTM is used only for the USB interface logic reset and is not used to reset the processor or other logic. (Additional Reset signals added using registers, mapped to a particular BS block (i.e. RST bit in Command register "COMM_M2")

Virtex Communication Protocol (VCP)

The array of 4096 Blocks of (BS) have dedicated purposes in the current VTE-4100 UHS-I test applications. For software compatibility purposes the allocation of the main blocks should be kept as close as possible to the current use. In rest changes should be made as needed for UHS-II testing.

The main definitions for current designs are:

Block#	Name	Depth	Description
BS0	TE Command Register	1 B	Control Register for TE
BS1	TE Status Register	2 B	Status Register for TE
BS2	DUT Error Register	1 B	DUT Device Error
BS3	TE Execution State Reg	1 B	
BS5			
BS6	Code Index	6 KB	
BS7			
BS8	Watchdog	5 B	