



# **SD Specifications**

## **Part 1**

# **UHS-II Addendum**

**Version 1.02**

**May 28, 2014**

**Addendum to:**

**SD Specifications  
Part 1 Physical Layer Specification  
Version 4.00 May 30, 2011, or later**

**Technical Committee  
SD Card Association**

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## Revision History

Date	Version	Changes compared to previous issue
May 30, 2011	1.00	The first release of UHS-II Addendum
September 18, 2013	1.01	The Revised Version which includes: (1) Modifications in UHS-II 1.00 Supplementary Note Version 1.00 (2) Modifications found after the Supplementary Notes
May 28, 2014	1.02	Fixed Section number from 3.2 to 3.5 Fixed Section number from 6.2.15 to 6.3

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## Conventions Used in This Document

### Naming Conventions

- Some terms are capitalized to distinguish their definition from their common English meaning. Words not capitalized have their common English meaning.

### Numbers and Number Bases

- Hexadecimal numbers are written with a lower case "h" suffix, e.g., FFFFh and 80h.
- Binary numbers are written with a lower case "b" suffix (e.g., 10b).
- Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.
- All other numbers are decimal.

### Key Words

- May: Indicates flexibility of choice with no implied recommendation or requirement.
- Shall: Indicates a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.
- Should: Indicates a strong recommendation but not a mandatory requirement. Designers should give strong consideration to such recommendations, but there is still a choice in implementation.

### Application Notes

Some sections of this document provide guidance to the host implementers as follows:

Application Note:

This is an example of an application note.

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# 1. General

This Addendum Specification defines an additional category to the Part 1 Physical Layer Specification Version 4.00. The following sections describe additional and modified parts of the base specification for this new category.

Key background factors behind Ultra High Speed Type II (UHS-II) Specification are shown below:

- **High speed interface is required to handle large volumes of HD (High Definition) contents**

In recent years, the number of SD-applications which handle large amount of data is increasing steadily with an increase in HD (High Definition) contents (HD, Super-HD, 3D-TV, etc.). At the same time, the data size of HD contents is also increasing year by year.

UHS-II is necessary to meet the ultrahigh-speed requirement to handle HD contents and farther large-capacity contents in the future.

- **Interface should be widely available for many kinds of hosts**

It is difficult to keep signal integrity at high-speed data transfer especially for mobile devices. Generally, board design of hosts becomes more difficult with high speed interface. UHS-II should be considered both high-speed and availability for many kinds of hosts.

- **Reusability of legacy resource (IPs, software, etc.) is important for host development**

Hosts require the compatibility with legacy protocol for their efficient development.

For example, in SD protocol, preserving the SD legacy infrastructures (CMD, RES, States, Status, Errors, etc.) provides efficient development with SD hosts, and this leads to a speedy expansion of UHS-II applications.

- **Interoperability and compatibility to Legacy SD I/F is important to avoid market confusion**

Hosts and Devices require also the interoperability and compatibility with Legacy SD cards installed based to enable UHS-II specifications to be smoothly adopted by the market.

- **Low voltage, low power consumption and low EMI are needed for mobile devices**

To apply new high-speed interface to many kinds of mobile devices, it is important to realize low power consumption and low EMI.

Some low power and low EMI techniques need to be considered for UHS-II.

- **Multiple device connectivity for minimizing the number of ports and circuit size is required**

Multi device connectivity is required to reduce the number of ports and circuit size for lower developing cost.

System features of UHS-II Specification based on the background are described in the next chapter.

## 2. System Features

From background factors mentioned in Chapter 1, the features of UHS-II are defined as follows:

- (1) High speed interface up to 312MB/s
- (2) Easy implementation for whole system
- (3) Compatibility with Legacy SD interface
- (4) Ensuring effective performance of data transfer
- (5) Low voltage, low power consumption, low EMI
- (6) Multiple device connectivity

The followings are additional explanations for system features.

- Interface speed
  - (1) Full Duplex mode (abbreviated to "FD mode"): data rate from 39MB/sec to 156MB/sec in the specifications and up to double the throughput in the future.
  - (2) Half Duplex with 2 Lanes mode (abbreviated to "2L-HD mode"): data rate from 78MB/sec to 312MB/sec in the specifications and up to double the throughput in the future.
  - (3) Interface speed is continuously variable.
  - (4) Infrastructure for additional Lanes is defined as follows, allowing future bit rate expansion. (Refer to Section 3.1 for the definition of downstream or upstream.)
    - Full Duplex with 2 Downstream and 1 Upstream Lanes mode (abbreviated to "2D1U-FD mode")
    - Full Duplex with 1 Downstream and 2 Upstream Lanes mode (abbreviated to "1D2U-FD mode")
    - Full Duplex with 2 Downstream and 2 Upstream Lanes mode (abbreviated to "2D2U-FD mode")
- Layering architecture
  - (1) The system is divided into at least 4 layers, Mechanical, Physical, Link and Transaction.
  - (2) Application specific layer can be introduced as a bridge between UHS-II common Transaction layer and the application.
- Legacy SD compatibility (for Card form factor)
  - (1) Host and Device shall support Legacy SD I/F for ensuring fully backward compatibility.
  - (2) Encapsulation of Legacy SD Format for Software Compatibility.
- Easy expansion for advanced features in the future
  - (1) CMD Queuing: Another arbitrary command can be issued during some transaction.
  - (2) Relaxed Ordering: Transaction order can be rearranged with reference to priority or processing speed.
  - (3) Inter-device Communication: Some Device (called "CMD issuable Device") allows issuing commands and directly communicating to other Device.

### 3. UHS-II System Concept

In this chapter, the overall of UHS-II interface and system are described. UHS-II Card (or simply Card) denotes an SD memory card which supports UHS-II interface.

#### 3.1 Interface Speed

UHS-II interface consists of at least two Lanes based on two differential signaling lines. Each Lane provides up to 156MB/sec.

Basically, direction of both Lanes is opposite each other, that is, one is from Host to Device (downstream) and the other is from Device to Host (upstream). This mode is defined as Full Duplex mode (abbreviated to "FD mode").

It is possible that both Lanes are set to transfer data in the same directions. In that case, overall interface speed is doubled up to 312MB/sec (twice as high as FD mode). This status is defined as Half Duplex with 2 Lanes mode (abbreviated to "2L-HD mode") and is optional in this specification. It is also possible to have more than two Lanes, 3 or 4 Lanes for increasing system speed. This behavior is optional in this specification.

Figure 3-1 illustrates interface speed comparison among bus modes in Legacy SD, UHS-I and UHS-II (for UHS-II interface of 2 Lanes is assumed).

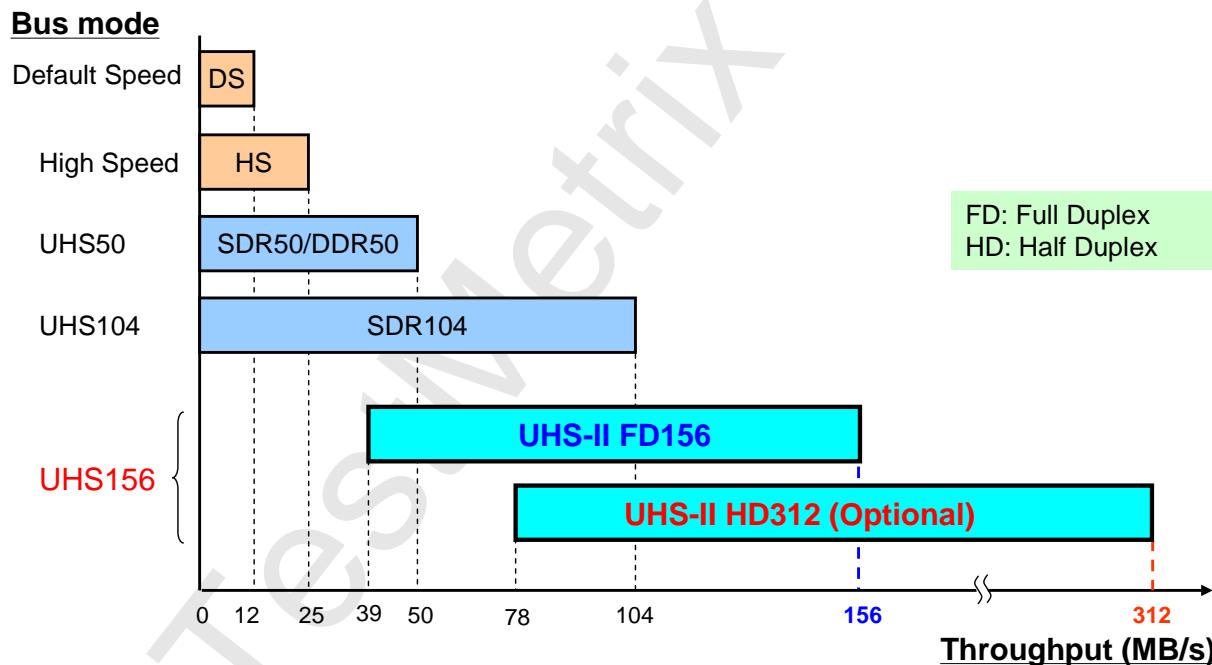


Figure 3-1 : Interface Speed Comparison

The interface speed shall be variable continuously.

## 3.2 Connection Topologies

### 3.2.1 Point to Point Connection

Minimum topology is consisting one Host and one Device is called "Point to Point" connection. Figure 3-2 shows the connection of a Host and a Device.

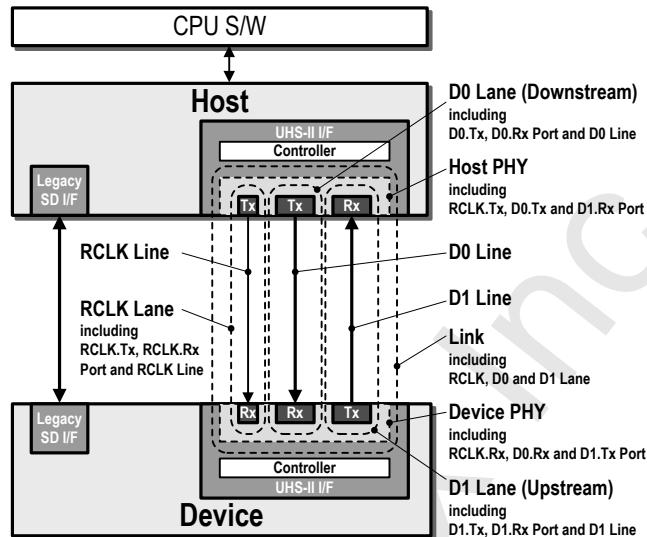


Figure 3-2 : Point to Point Topology (FD mode)

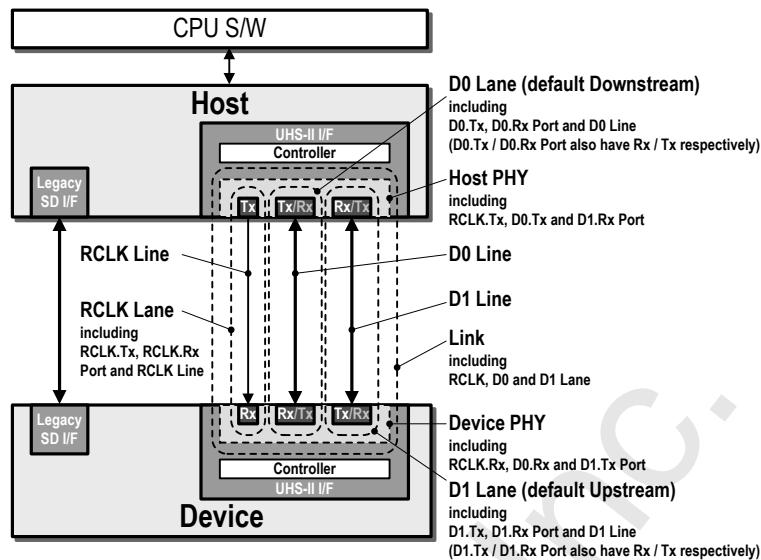
In UHS-II interface, both Host and Device have a PHY and a Controller which are responsible for performing Physical and Link / Transaction layer functions respectively. And UHS-II interface are connected by the following three Lanes.

- **RCLK:** transmits reference clock to Device from Host.
- **D0:** is a data Lane. It transmits commands, data, or other packets from Host to Device (downstream).
- **D1:** is another data Lane. It transmits responses, data, or other packets from Device to Host (upstream).

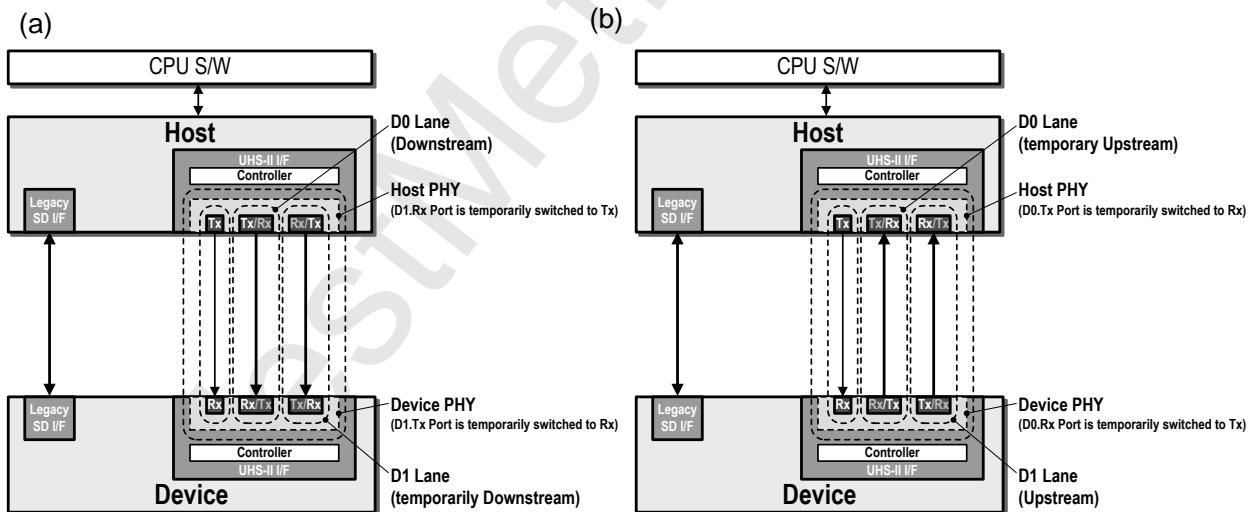
In general, each Lane consists of a Tx (Transmitter) Port and an Rx (Receiver) Port and a transmission Line between them. The notations used in this specification are used to specify each Tx or Rx Port clearly. For instance, Tx Port of RCLK Lane is described as RCLK.Tx and Rx Port of RCLK Lane is described as RCLK.Rx. The same rule is applied for other Lanes. And all Lanes are collectively called Link. Host PHY (PHY of Host) includes RCLK.Tx, D0.Tx and D1.Rx. Similarly, Device PHY (PHY of Device) includes RCLK.Rx, D0.Rx and D1.Tx.

All following descriptions relate to interface with two data Lanes. The optional case of 3 or 4 Lanes is described in Chapter 9.

Figure 3-3 shows the connection of Host and Device supporting 2L-HD mode.

**UHS-II Addendum Version 1.02****Figure 3-3 : Point to Point Topology (Supporting 2L-HD Mode)**

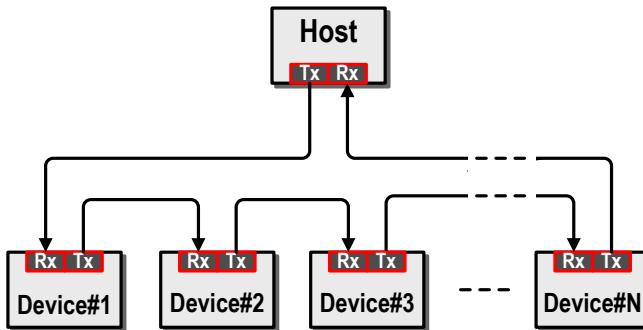
The default direction of D0 Lane is downstream, and D1 is upstream. If Host decides to send data to Device in 2L-HD mode, D1 Lane changes downstream temporarily (Figure 3-4 (a)). Similarly if Host decides to get data from Device in 2L-HD mode, D0 changes upstream (Figure 3-4 (b)). As a result, all Ports for data Lanes are necessary to have both functions of Tx and Rx.

**Figure 3-4 : Direction Changing in 2L-HD Mode****3.2.2 Multi-device Connection**

In order that Host can control or communicate with multiple Devices, UHS-II provides Multi-device connection. There are two types of topologies to realize Multi-device connection, one is Ring connection and the other is Hub connection. Ring connection is introduced to realize a cost effective topology that minimizes the total number of PHY in the embedded system. And Hub connection is introduced to realize more flexible topology compared to Ring, in terms of capability of hot insertion and removal. Note that RCLK shall be distributed individually to removable Devices, and not only UHS-II interface but also Legacy SD interface shall be connected to removable Devices.

### 3.2.2.1 Ring Connection

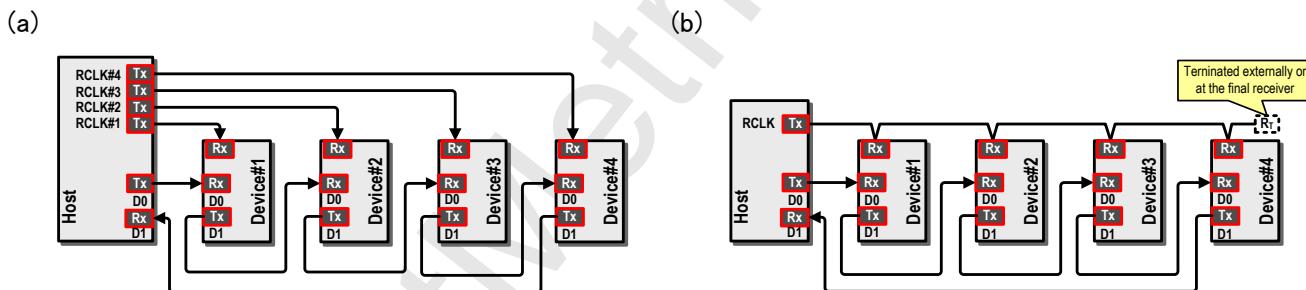
Figure 3-5 illustrates an example of Ring connection. Connection rule of data Lanes is as follows.  
(Note that 2L-HD mode is not available in Ring connection in UHS-II Addendum Version 1.00.)



**Figure 3-5 : Example of Ring Connection**

- (1) D0.Tx of Host is connected to D0.Rx of Device#1
- (2) D1.Tx of Device#1 is connected to D0.Rx of Device#2, and this operation is repeated.
- (3) D1.Tx of Device#N (final Device) is connected to D1.Rx of Host, and Ring connection completes.

Examples of RCLK distribution method are illustrated in Figure 3-6.



**Figure 3-6 : Examples of RCLK distribution method for Ring**

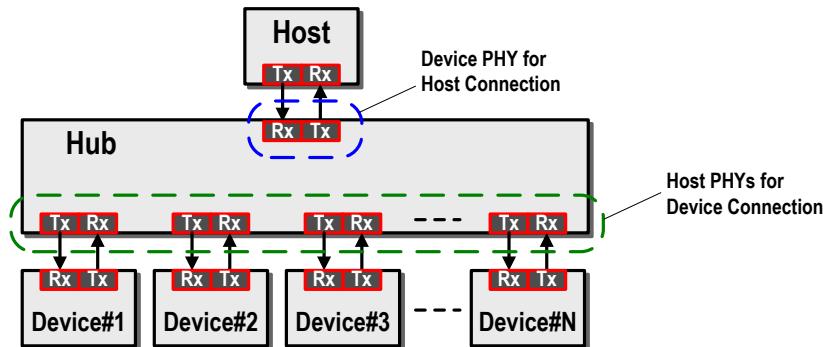
Figure 3-6 (a) shows a multiple point to point method which uses a separate RCLK driver (RCLK.Tx) for each Device. With this method, Host needs to have at least the same number of RCLK.Tx Ports as the number of connecting Devices. If Host has only one RCLK.Tx Port, multi-drop method can be applied to connect multiple Devices (Figure 3-6 (b)). With this method, RCLK bus is terminated externally or at the final receiver. In addition this method requires careful signal integrity design.

Note that Device has only one RCLK.Rx Port even in the case of Figure 3-6 (b).

### 3.2.2.2 Hub Connection

Figure 3-7 illustrates an example of Hub connection.

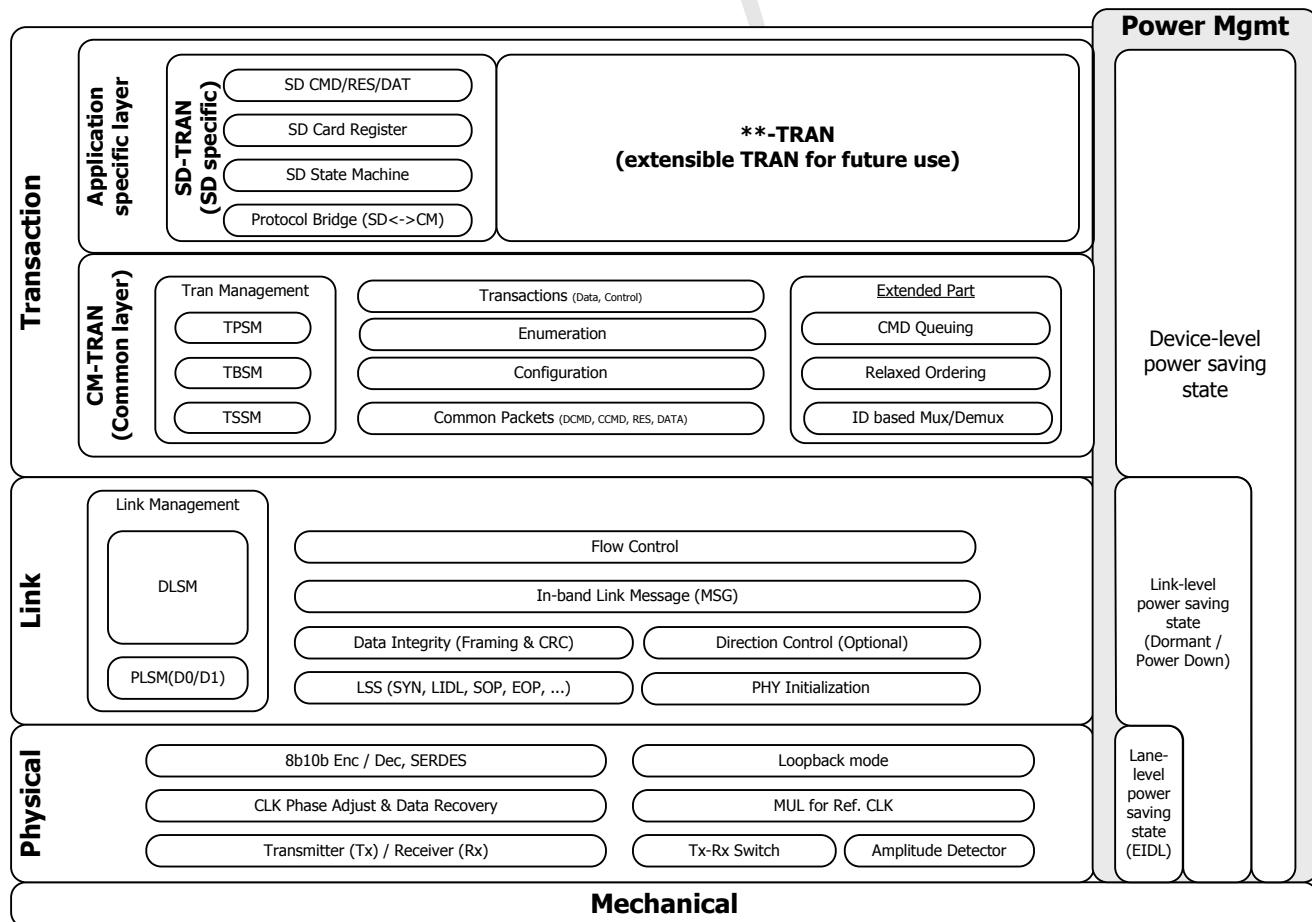
Hub shall have one Device PHY for Host connection and plural number of Host PHYs for Device connection. Hub also has functions such as transmitting signals to all connected Devices simultaneously, or selecting a packet destination according to its content.

**Figure 3-7 : Example of Hub Connection**

Note that from Device point of view behavior does not depend on UHS-II topology. Hub specification is not described in this document.

### 3.3 Layering

Figure 3-8 shows the overview of UHS-II interface layer structure.

**Figure 3-8 : Layering Overview**

Basically, UHS-II interface consists of four layers described below.

- **Mechanical layer** defines mechanical specification such as card form factor, connector pins and so on.
- **Physical layer (denoted by PHY)** defines electrical specification such as signaling architecture, and handle bit or symbol encoding and decoding.
- **Link layer (denoted by LINK)** is responsible for Link management including PHY initialization, and data integrity (packet framing / de-framing and CRC generation / checking). It is also in charge of power management and flow control.
- **Transaction layer (denoted by TRAN)** is responsible for protocol-base management including packet generation and analysis, command-response handshake, and so on.

TRAN is split into sub layers, one is a common layer called CM-TRAN and the other is an application specific layer. CM-TRAN is responsible for Basic IO or Memory transaction and control. The application specific layer bridges CM-TRAN and upper application layer in order to keep compatibility. SD-TRAN is one of the application specific layers and bridges CM-TRAN and Legacy SD applications or drivers. In this specification, SD-TRAN is also described. Other application specific layers can be defined in the future.

## 3.4 UHS-II Transaction

### 3.4.1 UHS-II Packet

The following five packet types are defined for UHS-II TRAN. UHS-II Packet other than MSG is also called Transaction Layer Packet (TLP).

- **Control command packet (denoted by CCMD)** is a command without Data packet transaction. There are two categories of CCMD, one is P2P CCMD and the other is broadcast CCMD. Refer to Section 6.2.2.3 for the details of them.
- **Data command packet (denoted by DCMD)** is a command accompanied with Data packet.
- **Response packet (denoted by RES)** is a response that Device returns to Host after receiving CCMD or DCMD.
- **Data packet (denoted by DATA)** is for transmitting data payload between Host and Device.
- **Message packet (denoted by MSG)** is for transmitting short information. Only MSG is generated or analyzed in LINK.

Basically, UHS-II packet consists the following three parts, Header, Argument, and Payload. The Header part is common for all types of packet.

TLP is basically packetized based on information provided by TRAN and depacketized in LINK. Refer to packet format described in Section 6.2.2 or Section 7.2.1 for the details of the information.

Let initiator denote a Node (Host or Device) that newly creates a packet and transmits it. The following table indicates the initiator for each packet type.

Packet Type	Initiator
CCMD/DCMD	Host (regardless of P2P CMD or broadcast CMD)
RES	Device
DATA	Node creating DATA packet (Host for write transaction, Device for read transaction)
MSG	Node creating MSG packet

Table 3-1 : Definition of Initiator

### 3.4.2 Data Transaction

Length Unit Mode is defined to specify the unit of total data transfer length (TLEN) transmitted by Data packet (DATA). Length Unit Mode has the following two modes, one is a Block Mode and the other is a Byte Mode. Note that these modes can be set as a parameter of DCMD.

- **Block Mode:** TLEN is specified by a unit of Block Length, which is a payload length for one block. Block Length is finally determined through Configuration (refer to Section 6.2.8 and 6.2.9) or settings in the application specific layers.
- **Byte Mode;** TLEN is specified by a unit of byte. TLEN shall be less than or equal to Block Length.

Also refer to Section 5.2.6 about a data framing rule of above two modes.

In addition, at most one data transaction can be executed in UHS-II Addendum Version 1.00.

### 3.4.3 CM-TRAN

As described in Figure 3-8, UHS-II transaction layer is split into common layer (CM-TRAN) and application specific layer (SD-TRAN in case of UHS-II Card).

CM-TRAN specifies the common protocol suitable for UHS-II PHY and LINK (UHS-II native protocol). CM-TRAN generates UHS-II packets and sends them in the transmitter side according to the UHS-II I/O Register, or analyzes received packets in the receiver side. UHS-II I/O register is accessed by the Application Driver (Host) or Backend (Device).

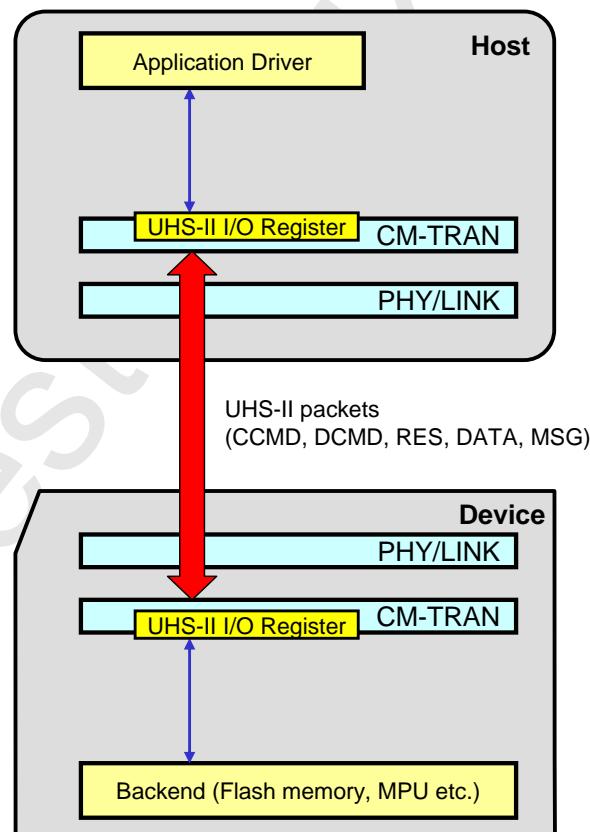


Figure 3-9 : Basic UHS-II Transaction

### 3.4.4 SD-TRAN

SD-TRAN bridges UHS-II interface (CM-TRAN) and Legacy SD IPs or software. SD-TRAN analyzes SD Host/Device Register and sets parameters to UHS-II I/O Register. In this case, CM-TRAN generates UHS-II packets which encapsulate Legacy SD command, response or data. Moreover, when CM-TRAN receives the encapsulated packets, CM-TRAN analyzes it and notifies to SD-TRAN.

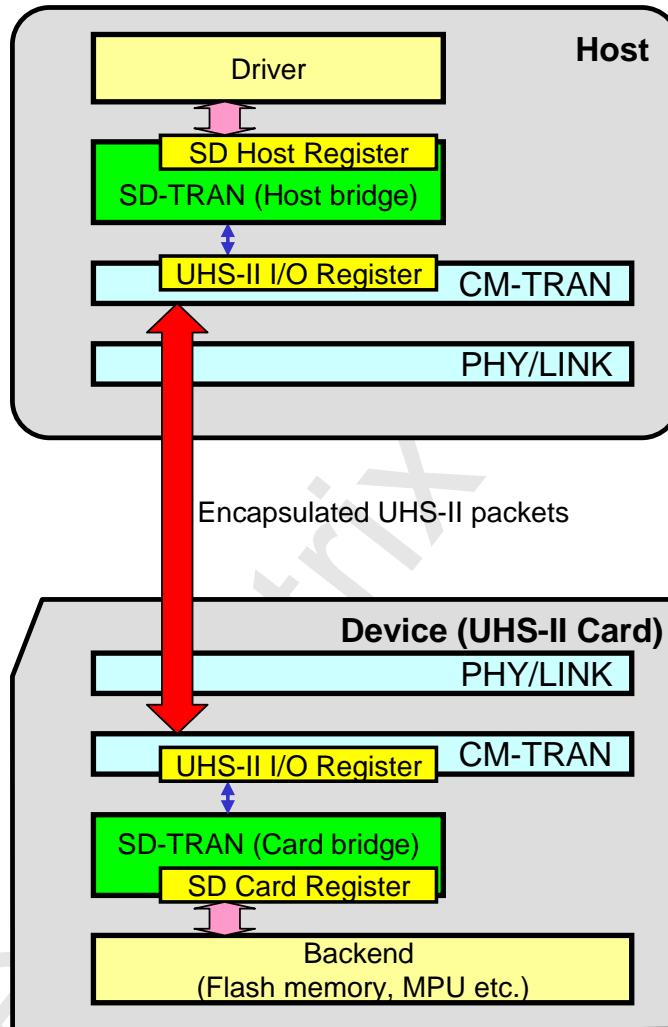


Figure 3-10 : UHS-II Transaction by SD-TRAN

### 3.4.5 Aborting Transaction

In UHS-II, TRANS\_ABORT CCMD is introduced as following purposes.

- Terminating data transmission in UHS-II native protocol. (Note that the encapsulated CMD12 shall be used instead of TRANS\_ABORT if SD-TRAN is implemented.)
- Aborting the outstanding transaction when timeout is detected.

Example sequences using TRANS\_ABORT are described in Section 6.2.14, Section 6.3.2, Section 7.2.5, and Section 7.3.2.

### 3.5 UHS-II Initialization Outline

Host shall execute UHS-II Initialization flow as described in Section 3.5.1 (in case of without Boot Code Loading) or in Section 3.5.2 (in case of with Boot Code Loading). If Host violates those rules, Device operation is not guaranteed.

#### 3.5.1 UHS-II Initialization Flow without Boot Code Loading

Figure 3-11 shows a UHS-II Initialization flow after I/F power cycle or issuing FULL\_RESET command (refer to Table 6-20 for more details). Details of state transition are defined in Section 5.2.9.

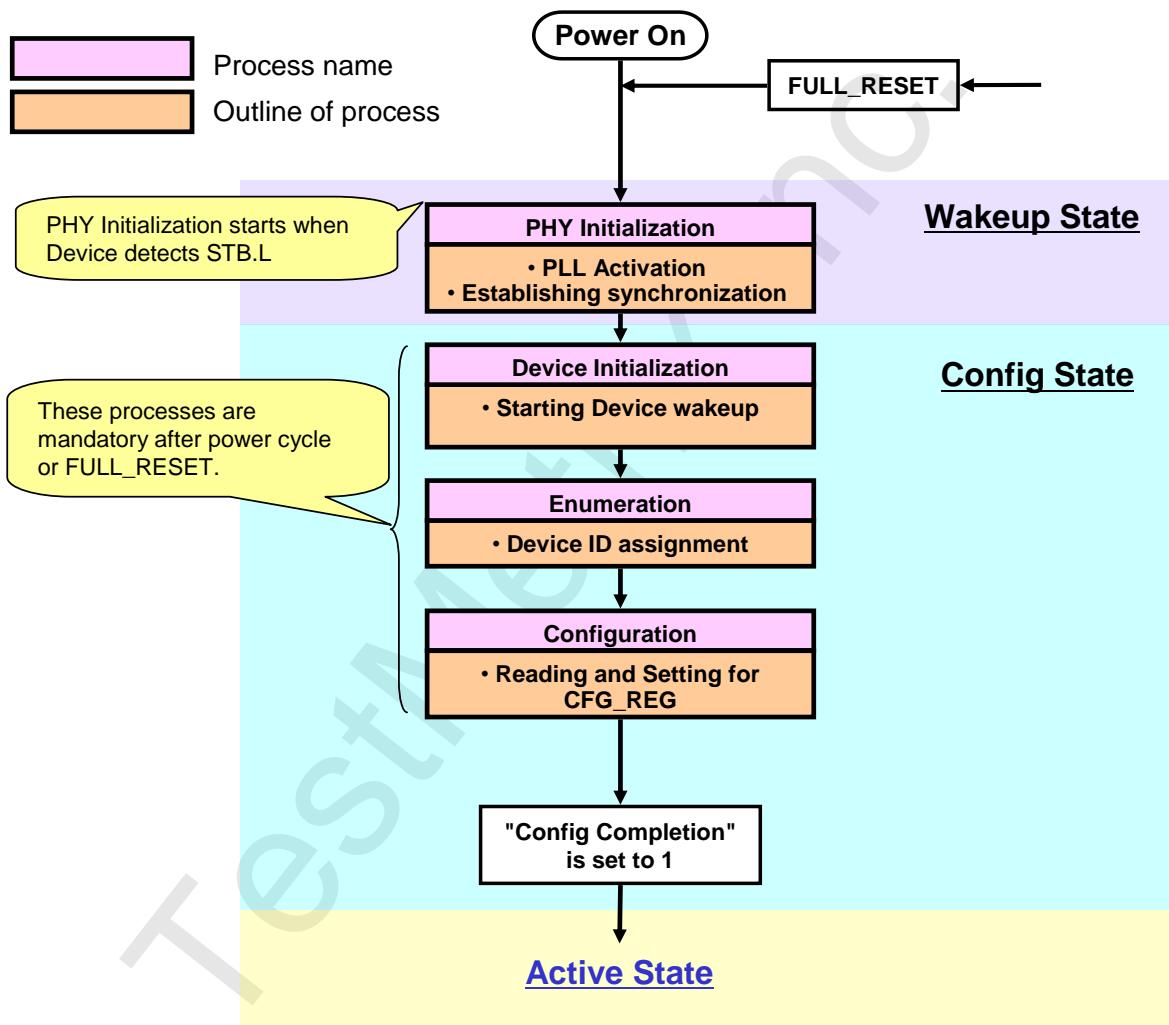


Figure 3-11 : UHS-II Initialization Flow

After I/F power cycle or FULL\_RESET, PHY Initialization process is started by Host's providing RCLK and STB.L (refer to Section 5.3 for more details).

After finishing PHY Initialization, the state transits to Config State and the following three processes take place.

- **Device Initialization:** This process is executed by DEVICE\_INIT CCMD and makes whole components in Device activated. Refer to Section 6.2.6 for more details.
- **Enumeration:** This process is executed by ENUMERATE CCMD and assigns Node IDs for each

Device uniquely. Refer to Section 6.2.7 for more details.

- **Configuration:** This process is for determination of parameters for transaction among Host and Devices. First Host reads capabilities or properties from Configuration Register (CFG\_REG) of Devices, then determines the parameters for transaction, and finally writes the parameters to the register. Refer to Section 6.2.8 and 6.2.9 for more details.

If "Config Completion" flag defined in CFG\_REG is set to 1 successfully during Configuration process, the state transits to Active State.

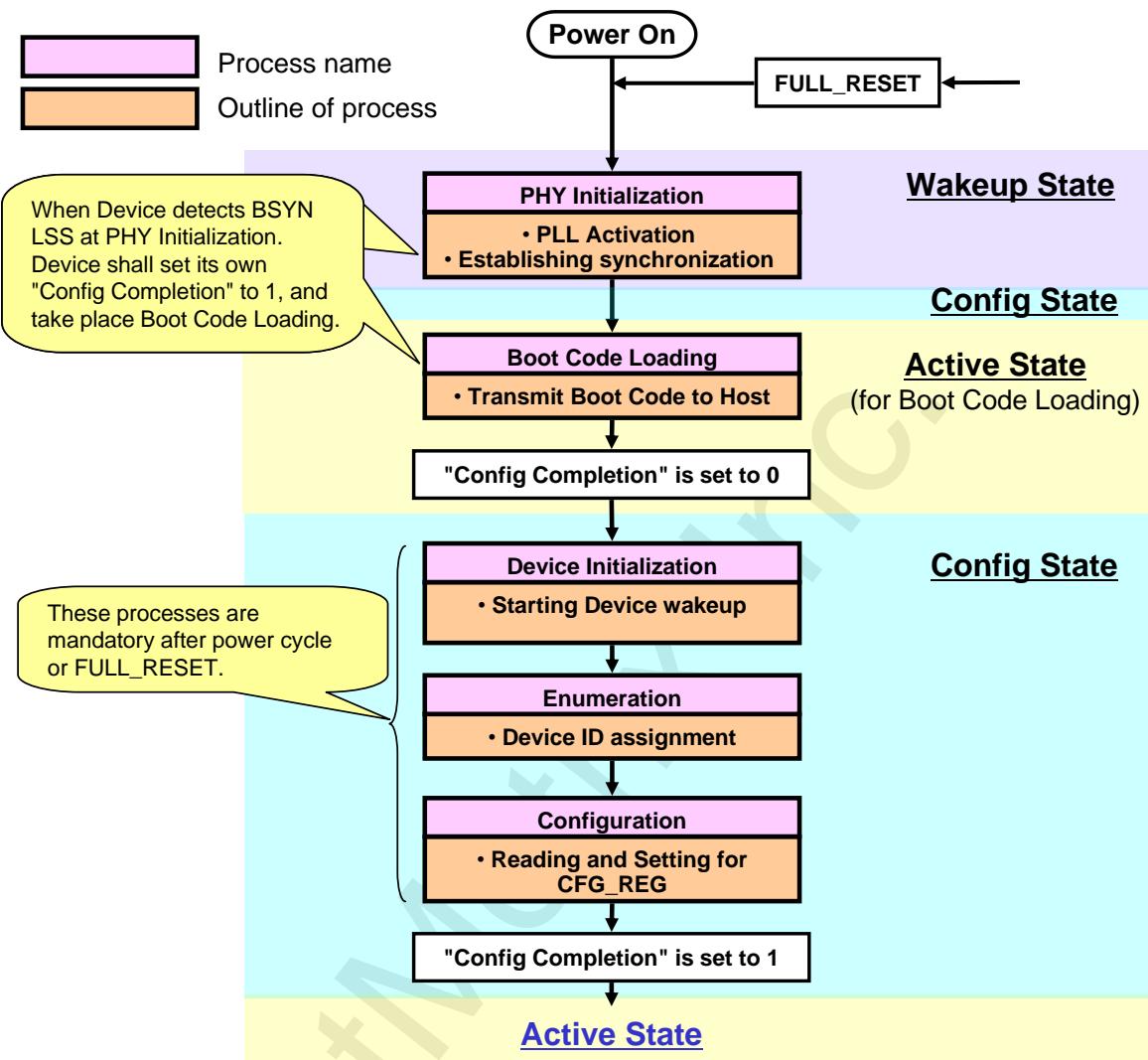
Before completing Device Initialization it shall not operate and not transmit RES or broadcast CCMD when Device receives CMD other than DEVICE\_INIT CCMD.

### **3.5.2 UHS-II Initialization Flow with Boot Code Loading**

It is possible for Host to load its Boot Code from one of connected Device, called Boot Device. Boot Device is optional in embedded system. It is required for Host to read the Boot Code as soon as possible.

Needless to say, Boot Device and Host are possible to transmit or receive Boot Code. In addition, considering the Ring connection, all other Devices also have functionality to bypass Boot Code and its related packets.

In this Section, the specification of loading Boot Code is described when the system includes Boot Device. This function is called "Boot Code Loading". Figure 3-12 shows UHS-II Initialization flow when Boot Code Loading is executed.



**Figure 3-12 : UHS-II Initialization Flow When Boot Code Loading Is Executed**

Different from Figure 3-11, Host transmits not SYN LSS but BSYN LSS in order to establish synchronization (refer to Section 5.2.2.2 and Section 5.9). At that time, all Devices shall set their own "Config Completion" to 1.

After finishing PHY Initialization, DLSM normally transits to Config state, but as "Config Completion" is equal to 1, DLSM immediately transits to Active state in order to execute Boot Code Loading.

After finishing Boot Code Loading, Host shall set "Config Completion" to 0 for all Devices before DEVICE\_INIT CCMD. Device shall accept the Broadcast Write CCMD for setting "Config Completion" to 0 even before receiving DEVICE\_INIT CCMD. Then DLSM transits to Config state. The rest of flow is same as Figure 3-11.

Details of Boot Code Loading are defined in Section 5.9.

## 4. Physical Layer Specification

The details of UHS-II Physical layer such as signaling architecture electrical specification and handle bit or symbol encoding and decoding are described in this chapter.

The UHS-II standard is targeted for mobile, portable applications and home applications. It shall be compatible to legacy SD Cards. It provides enhanced data rate, while maintaining low power and low EMI. It is recommended for short cable length, typically below 20cm.

This UHS-II specification is defined for Card and also for Embedded Device. In this specification, "Device" means both Card and Embedded Device. If some specification items or descriptions are only for Card, "Card" is used. If some specification items or descriptions are only for Embedded Device, "Embedded Device" is used.

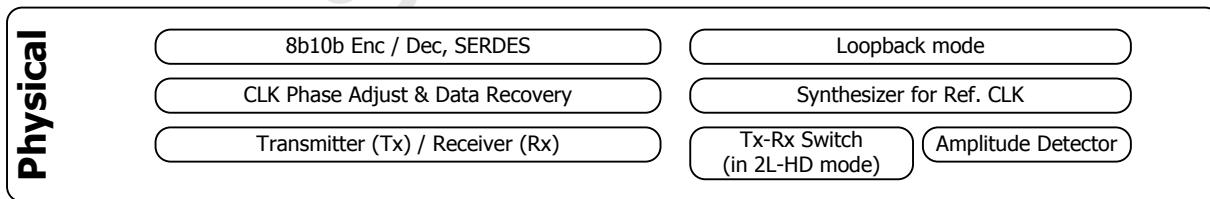
The key features of Physical Layer are defined as follows:

- Differential low voltage Signaling with DC coupling
- Flexibility of transmission rates
- Low Frequency Reference Clock (RCLK)
- Two types of duplex mode: FD mode (mandatory), 2L-HD mode (optional)
- Additional pins for High-Speed Differential transmission
- 8b/10b coding
- Enhanced power saving modes

### 4.1 Physical Layer Overview

Physical layer consists of the following functions:

- Differential Transmitter(Tx) and Receiver(Rx)
- CLK phase adjustment and Data recovery
- Serializer and De-serializer (SERDES)
- 8b/10b encoding and 10b/8b decoding
- Amplitude Detection
- Synthesizer for Reference CLK



**Figure 4-1: Physical Layer Overview**

### 4.2 Physical Layer Interface Architecture

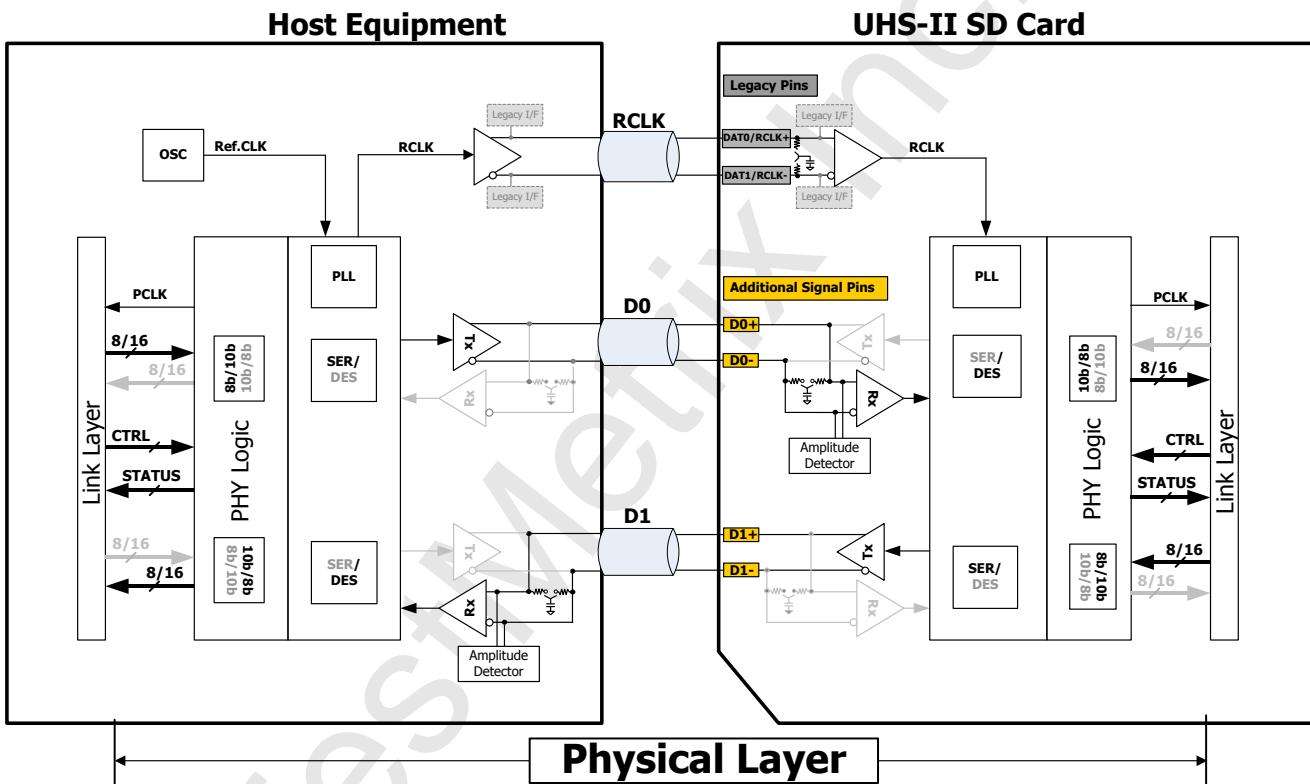
Figure 4-2 illustrates an example of the interface architecture of physical layer in case of point to point connection between Host and Card. The UHS-II interface utilizes transmission Lines (including socket and pins) and terminations which are meant to keep the impedance matching for high speed transmission. UHS-II interface introduces the additional pins for high speed data transmission.

UHS-II interface has continuous variable data rate from 39MB/sec to 156MB/sec as effective data rate. Device shall cover the whole range.

UHS-II has two data Lanes. As default, one Lane (D0) is used for downstream (from Host to Device), and another Lane (D1) is used for upstream (from Device to Host). Both data Lanes may be used for downstream Lanes or upstream Lanes at the same time by activating the 2L-HD mode (optional). The transmitted data is encoded by 8b/10b encoder.

The Differential Clock (RCLK) may be tuned in the range of 26MHz to 52MHz. Regarding Card, RCLK is sent through the legacy SD transmission lines DAT0, DAT1 and corresponding Card pins.

Amplitude Detectors, which detect the Lane's electrical level, are equipped to Host side of D1 Lane (optional) and Device side of D0 Lane (mandatory). Amplitude Detectors make the I/O circuits, such as receiver, to wake up when transmission is resumed at the Lane after Dormant state.



**Figure 4-2: Physical Layer Interface Architecture**

#### 4.2.1 Lane Definition

Host and Device are connected by 3 differential Lanes with DC coupling:

- **High speed data Lanes (D0, D1):**

D0 is used for downstream (from Host to Device), thus WRITE data and command are transferred from Host to Device on this Lane. However, when enabling the optional 2L-HD mode, it is possible to use D0 Lane as upstream (from Device to Host).

D1 is used for upstream, thus READ data and response are transferred from Device to Host on this Lane. However, when enabling the optional 2L-HD mode, it is possible to use D1 Lane as downstream.

D0 and D1 Lanes are used for differential transmission between Host and Device which are dedicated to UHS-II interface only, and are separate for signals of legacy SD interface. The D0 and D1 signals are encoded by 8b/10b code before transmission, and decoded by 10b/8b after receiving, as described in Section 4.5.

- **Reference clock Lane (RCLK):**

RCLK is transmitted from Host to Device. Whenever Host output a RCLK to the UHS-II Device, the RCLK signal frequency and phase should be stable. The RCLK shall not be stopped and its frequency shall not be changed during UHS-II transmission, even within the same range. (Refer to Section 4.2.2 for the Range definition and Section 6.2.3 for frequency change procedure).

The RCLK frequency is lower than lowest data rate. Therefore, the Device shall generate high frequency clock or multi-phase clocks internally for sampling the high-speed data. The RCLK frequency is in the range of 26MHz to 52MHz; Data rate is from 390Mbps to 1.56Gbps per Lane (Refer detail in Section 4.2.2).

Regarding Card, RCLK is sent through DAT0 and DAT1 lines of legacy SD interface. Thus, RCLK does not require additional pins. Card RCLK receiver shall be tolerant to single ended voltage range of 0V to 3.6V DC.

For power save purposes, when no data is transferred each Lane may enter EIDL state individually, or all Lanes including RCLK Lane may enter EIDL state concurrently, which is called Dormant state. During those states and mode, an Amplitude Detector of each D0, D1 Lane is active, monitoring the Line voltage and flagging wakeup notice. After detecting the wakeup notice, the detector activates PHY circuits of own port.

#### 4.2.2 Range Definition for Data Rate

In UHS-II, RCLK frequency is in the range 26MHz to 52MHz and Data rate is 390Mbps to 1.56Gbps per Lane accordingly. This range is divided to two ranges for the ease of PLL design as shown in Table 4-1. Initialization of UHS-II interface after power down shall be done with the Range A.

Device PLL acquisition time shall be at most 2ms. But only the first PLL acquisition time after power up, PLL of Host and Device shall finish locking less than 100ms. This is Tactivate. (Refer to Section 5.3 for PHY Initialization.)

	RCLK Frequency	Data Rate/channel	Ratio (Data rate / RCLK Frequency)
Range A	26MHz to 52 MHz	390Mbps to 780Mbps	x 15
Range B		780Mbps to 1.56Gbps	x 30

Note: Even if supporting SSC, the minimum RCLK frequency shall not be lower than 26MHz.

**Table 4-1: Range Definition for Data Rate**

#### 4.2.3 Power Supply Connections

Two power supply connections are needed for UHS-II interface, named VDD1 and VDD2, for powering the Device by the Host.

VDD1 is dedicated for powering the legacy SD interface, logic and the memory devices in the Device VDD2 is used for powering UHS-II interface. It should power the PHY and upper layers logic.

GND node is common to all the devices and all the circuits. It is also used as reference for the UHS-II signaling levels, thus it is recommended that both Host and Device design for minimal DC variation and AC noise on this node.

#### 4.2.4 Operating Condition

UHS-II Device shall operate with the condition shown in Table 4-2 and Table 4-3.

Operating temperature will be defined by mechanical addendum.

Item	Value				note
	Min	Typ	Max	Unit	
VDD1 Supply voltage	2.7	3.3	3.6	V	Note 1
VDD2 Supply voltage	1.7	1.8	1.95	V	Note 2

Note 1: VDD1 of 1.8V is under evaluation.

Note 2: VDD2 of 1.2V is optional for embedded Device.

**Table 4-2: Operating Voltage**

Item	Value				note
	Min	Typ	Max	Unit	
Leakage current of each UHS-II pin	-	-	10	uA	Absolute value. Note 1, 2, 3

Note 1: Refer to leakage of D0+, D0-, D1+, D1-, RCLK+ and RCLK-.

Note 2: When pin is at input state, with static valid input voltage.

Note 3: Input termination resistor is disconnected.

**Table 4-3: Leakage Current**

#### 4.2.5 Over-voltage Tolerance

When UHS-II Card is inserted to the existing multi-card socket, the differential contact pads of D0 and D1 might accidentally be in touch with the other contact terminals of the multi-card socket, which are used for the connection with the other standards removable device.

These contact terminals have a possibility to be pulled up to 3.6V via 10kohm resistor or more.

Device shall tolerate this over voltage condition. However it is not expected to function under this condition.

In addition, RCLK Rx of Card shall be tolerant to 3.6V (Refer to Section 4.2.1 "Reference Clock Lane").

## 4.2.6 Impedance and Termination Scheme

### 4.2.6.1 Impedance Definition

The performance of high-speed transmission depends on the impedance matching for all elements of the differential Lanes, such as transmission Lines on PCB, connectors and terminations.

This section specifies the impedance and termination requirements for the components of the differential Lanes.

Table 4-4 denotes the requirement of impedance characteristics for Device side. UHS-II Device shall comply with this requirement.

Item	Symbol	value				Note	
		Min	Typ	Max	Unit		
Tx Output Impedance	R <sub>SE-TX</sub>	35	50	65	ohm	Each single-ended output Impedance.	
Rx Termination Impedance	R <sub>termDIF</sub>	74	100	126	ohm	Differential mode. Measured at DC	
Input Capacitance	RCLK+, RCLK-	C <sub>RCLK</sub>	-	-	10	pF	Refer to section 6.7.1.3.3 in SD Specifications Part 1 Physical Layer Specification Ver. 4.00 or later
	D0+,D0-, D1+,D1-	C <sub>Dx</sub>	-	-	2	pF	Note 1

Note 1: This capacitance is a design guideline for the Device LSI designer. It refers to the LSI itself only, and presents the load at the end of the transmission Line, thus excludes any capacitance of the Device package.

**Table 4-4: Device Impedance Characteristics**

Table 4-5 denotes the requirement of impedance characteristics for Host. UHS-II Host shall comply with the requirement.

Item	Symbol	Value				Note
		Min	Typ	Max	Unit	
Tx Output Impedance	R <sub>SE-TX</sub>	35	50	65	Ohm	Each single-ended output Impedance.
Characteristic Impedance of differential Transmission Line	Z <sub>D</sub>	85	100	115	Ohm	Differential mode Note 1,2
Rx Termination Impedance	R <sub>termDIF</sub>	74	100	126	Ohm	Differential mode Measured at DC
Input Capacitance of D0+,D0-, D1+,D1-	C <sub>Dx</sub>	-	-	2	pF	Note 3

Note 1: Socket and cable shall also comply with this spec. But a single exception is permitted for socket: 100ohm  $\pm$ 30ohm only for 200ps duration.

Note 2: For the differential transmission Line, the difference of characteristic single-ended impedance between + and - single-ended trace (intra pair single ended impedance match) is recommended to be within  $\pm$ 5% (as informative).

Note 3: This capacitance is a design guideline for the Host LSI designer. It refers to the LSI itself only, and presents the load at the end of the transmission Line, thus excludes any capacitance of the Host LSI package.

**Table 4-5: Host Impedance Characteristics**

#### **4.2.6.2 Input Termination Scheme**

By default, the interface is set to be FD mode, where Host is Tx and Device is Rx on D0 Lane, Host is Rx and Device is Tx on D1 Lane. As the default settings, Rx of each Lane shall activate the receiver termination.

When supporting 2L-HD mode, direction of D0 and D1 Lane may be changed if required. The receiver side of each Lane shall activate the termination and transmitter side of each Lane should deactivate the termination.

For the RCLK Lane, Host always functions as transmitter and Device always functions as receiver. Thus, the Device side shall always activate the termination, and the Host side has no need for parallel termination. Multi-drop method for RCLK distribution may be applied to Embedded Devices, in that case the termination of RCLK is used in only at the last Device or the end point of RCLK Line. (Refer to Figure 3-6(b) in System and Protocol specification draft for more details).

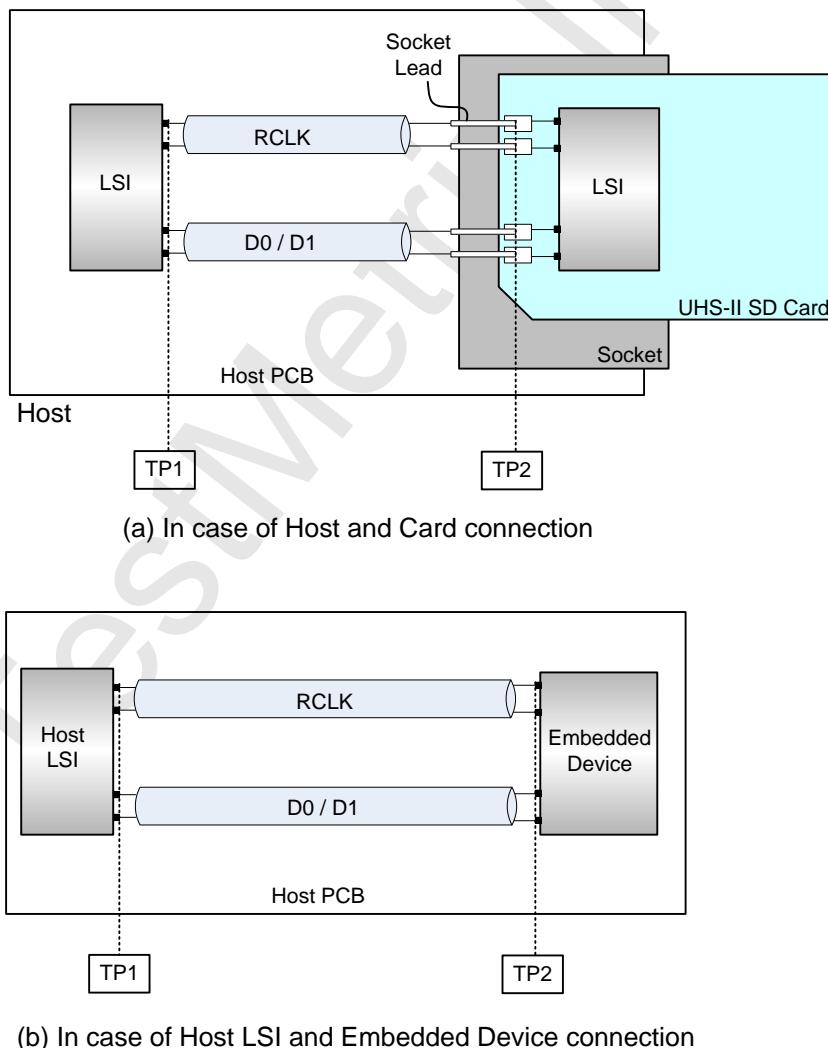
#### 4.2.7 Definition of Test Points for Host and Device

The signal test points are shown in Figure 4-3.

TP1 is the point where the Host LSI pins are connected to the PCB. The Tx and Rx electrical specifications at TP1 are described in Appendix E, while eye-mask templates at TP1 are described in Figure 4-6. All signals specifications at TP1 are for recommendation only.

In case of Host and Card connection (Figure 4-3 (a)), TP2 is the connection point between Host and Card, which are Card socket contacts. In case of Host LSI and Embedded Device connection (Figure 4-3 (b)), TP2 is the point where the Embedded Device pins are connected to the PCB.

Note: Figure 4-3 describes the conceptual location of TP1 and TP2 when Host is connected to Device. Nevertheless, all requirements that refer to TP1 and TP2 (normative and informative) in this specification are targeted to be tested for compliance in separate test fixture environments as described in Appendix E.1 (for Host) and Appendix E.2 (for Device).



**Figure 4-3: Signal Test Points**

## 4.3 Electrical Specification

### 4.3.1 Definition of Single-ended and Differential Signals

Single ended signals, representing either the positive or negative signal of a differential pair Line, are illustrated in Figure 4-4, Figure 4-5(a) as  $V_{Dp}$  and  $V_{Dn}$  respectively. The absolute value of the difference between  $V_{Dp}$  and  $V_{Dn}$  are defined as differential voltage;

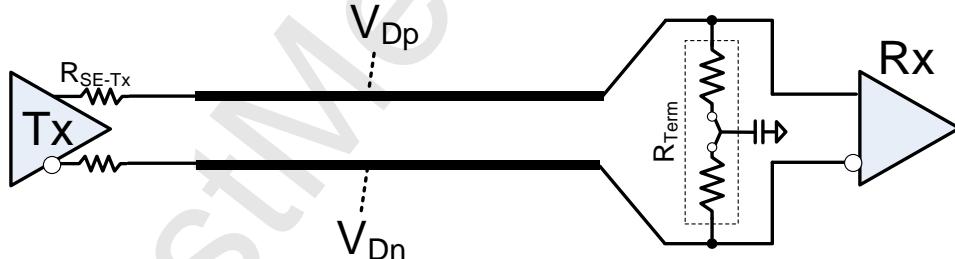
$$V_{diff} = |V_{Dp} - V_{Dn}|$$

The differential net swing is from  $-V_{diff}$  to  $+V_{diff}$  centered on 0V differential. Thus peak to peak voltage of differential signal  $V_{diff_{p-p}}$  is two times of  $V_{diff}$ ;

$$\begin{aligned} V_{diff_{p-p}} &= 2 * V_{diff} \\ &= 2 * |V_{Dp} - V_{Dn}| \end{aligned}$$

The common mode swing of differential Line ( $V_{CM}$ ) is defined as the mean value of both single ended swings  $V_{Dp}$  and  $V_{Dn}$ .

$$V_{CM} = \frac{V_{Dp} + V_{Dn}}{2}$$



**Figure 4-4: Single-ended Signal Names on Differential Line**

Note: The schematics of Tx side and Rx side in this Figure 4-4 are only example. The actual implementation may be different.

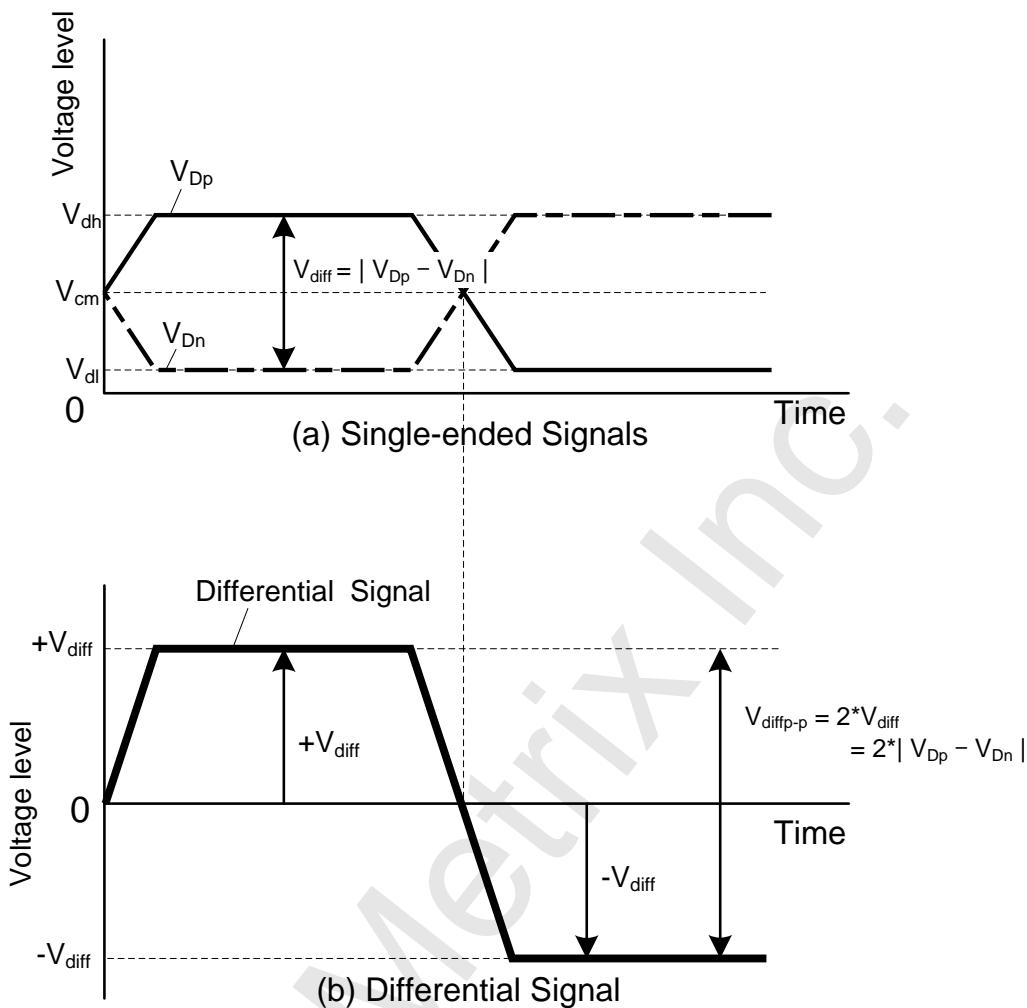


Figure 4-5: Definition of Single-ended and Differential Signals

#### 4.3.2 Specification of Transmitter and Receiver

The specifications of transmitter and receiver are detailed in this section. These specifications are defined at TP2 point.

##### 4.3.2.1 Host Transmitter Specification

When Host transmits differential signal at each differential Lane (D0 or D1), the output waveform shall meet the electrical specifications listed in Table 4-6 at TP2.

The eye-mask template for Host transmitter related to Figure 4-6 is shown in Figure 4-6 (2).

Item	Symbol	value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	125	185	280	mV	Absolute value. Note 1
Rise/Fall time of Differential signal	$T_{R,T_f}$	100	-	-	ps	From 20% to 80% of voltage swing. Note 2
Common mode voltage	$V_{CM}$	150	200	250	mV	Note 1,5
EIDL state differential voltage	$V_{diff\_PD}$	-10	0	10	mV	Note 3
EIDL state common mode voltage	$V_{CM\_PD}$	-10	0	10	mV	Note 3,5
Inter skew	$Sk_{inter}$	-	-	1.0	UI	Note 4

Note 1: With a differential termination of  $100\Omega$ .

Note 2: Designers should consider improvement of signal integrity and reduction of EMI to determine rise/fall time of Host and Device output. Use of slower rise/fall time in Range A compare with Range B is an example implementation.

Note 3: In EIDL state, both positive and negative lines of D0 Line are pulled down by Tx.

Note 4: Inter skew means the skew between D0 and D1 when both transmitters transmit from Host to Device. This is mandatory for 2L-HD mode and not applied to FD mode.

Note 5:  $V_{CM\_PD}$  and  $V_{CM}$  are measured in reference to its local GND.(more details in UHS-II PHY Test Guideline document)

**Table 4-6: D0, D1 Output Requirements for Host Transmitter at TP2**

The output waveform from Host shall meet the electrical specifications listed in Table 4-7 at TP2 for the RCLK Lane.

Item	Symbol	value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	125	185	280	mV	Absolute value. Note 1
Rise/Fall time of Differential signal	$T_{R,Tf}$	-	-	0.2	$T_{RCLK}$	From 20% to 80% of voltage swing. Refer to Section 4.11 for low EMI. Note 2
Common mode voltage	$V_{CM}$	150	200	280	mV	Note 1,3,4
Total Jitter	$T_J$	-	-	0.3	UI	Note 5,6 Refer to Section 4.3.4
Duty Cycle	$T_{CKH}$	42.5		57.5	%	Of $T_{RCLK}$

Note 1: With a differential termination of  $100\Omega$ .

Note 2:  $T_{RCLK}$  means the period time of RCLK

Note 3:  $V_{CM}$  is measured in reference to its local GND. ( more details in UHS-II PHY Test Guideline document)

Note 4: It is recommended for Host to disconnect legacy DAT0 DAT1 pull up resistors in UHS II mode.(Legacy Tx in Hi-Z )

Note 5: Total jitter is comprised of all jitter components from LSI such as deterministic jitter, random jitter etc.

Note 6: RCLK jitter for Host transmitter is measured related to itself using a 2nd order soft PLL with BW of  $2.34MHz/Sf$  inside the test equipment. Detailed measurement procedure is described in UHS-II PHY Test Guideline document. ( $S_f$  is a scaling factor. Refer to Figure 4-7 in Section 4.3.4)

**Table 4-7: RCLK Output Requirements for Host Transmitter at TP2**

#### 4.3.2.2 Device Receiver Specification

When receiving D0 signal (and D1 signal in 2L-HD mode) from Host, Device receiver shall comply with specification requirements listed in Table 4-8 at TP2 for every data rate of UHS-II.

The eye-mask template of the Device receiver related to Table 4-8 is shown in Figure 4-6 (3). Device receiver shall receive signals that comply with definition in Table 4-8 and Figure 4-6(3) correctly.

Item	Symbol	value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	95	-	-	mV	Absolute value.
Common mode voltage source	$V_{CM\_source}$	150	200	250	mV	Note 1, 3,4
EIDL state common mode voltage	$V_{CM\_PD}$	-10	0	10	mV	Note 1,2, 5

Note 1: $V_{CM\_source}$  and  $V_{CM\_PD}$  are measured in reference to its local GND.  
(more details in UHS-II PHY Test Guideline document)

Note 2: In EIDL state, both positive and negative lines of D0 Lanes are pulled down by Tx.

Note 3:  $V_{CM\_source}$  is the common-mode voltage which is transmitted by Host Tx together with diff D0/D1 signal.

Note 4: In addition to  $V_{CM\_source}$ , undefined amount of  $V_{CM\_noise}$  is expected to appear at device Rx LSI, depending on device implementation. It is recommended to follow the design guidelines at Appendix E.2.3 .

Note 5: In addition to  $V_{CM\_PD}$ , undefined amount of  $V_{CM\_noise}$  is expected to appear at device Rx LSI, depending on device implementation. It is recommended to follow the design guidelines at Appendix E.2.3 .

Note 6: Jitter tolerance specification is defined in Section 4.3.4.

Note 7: Device Receiver shall tolerate the inter skew spec defined at Table 4-6.

**Table 4-8: D0, D1 Input Requirement for Device Receiver at TP2**

Device receiver shall meet the input requirement listed in Table 4-9 for the RCLK Lane.

Item	Symbol	value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{\text{diff}}$	95	-	-	mV	Absolute value.
Common mode voltage source	$V_{\text{CM\_source}}$	150	200	280	mV	Note 1, 2,3
Total Jitter	$T_J$	-	-	0.35	UI	Refer to Section 4.3.4 Note 4
Duty Cycle	$T_{\text{CKH}}$	40		60	%	Of $T_{\text{RCLK}}$

Note 1:  $V_{\text{CM\_source}}$  is the common-mode voltage which is transmitted by Host Tx together with diff RCLK signal.

Note 2:  $V_{\text{CM\_source}}$  is measured in reference to its local GND. (more details in UHS-II PHY Test Guideline document)

Note 3: In addition to  $V_{\text{CM\_source}}$ , undefined amount of  $V_{\text{CM\_noise}}$  is expected to appear at device Rx LSI, depending on device implementation. It is recommended to follow the design guidelines at Appendix E.2.3 .

Note 4: Common-mode noise inside device may cause additional jitter on Device Rx LSI, depending on device implementation. Device designer should take this jitter into account.

**Table 4-9: RCLK Input Requirement for Device Receiver at TP2**

### 4.3.2.3 Device Transmitter Specification

When Device transmits differential signal at D1 Lane (and D0 Lane in 2L-HD mode), the output waveform shall comply with the electrical specifications listed in Table 4-10 at TP2 for every data rate of UHS-II.

The eye-mask template for Device transmitter at TP2 related to Table 4-10 is shown in Figure 4-6 (4).

Item	Symbol	Value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	140	200	280 (560)	mV	Absolute value. Note 1,2
Rise/Fall time of Differential signal	$T_{r,f}$	100	-	-	ps	From 20% to 80% of voltage swing. Note 3
Common mode voltage source	$V_{CM\_source}$	150	200	250	mV	Note 4,5,7
Common mode voltage noise	$V_{CM\_noise}$	-100		150	mV	Note 4,5,11,12
Total Common mode voltage	$V_{CM\_total}$	50	-	400	mV	Note 5,10,11,12
EIDL state differential voltage	$V_{diff\_PD}$	-10	0	10	mV	Note 8
EIDL state common mode voltage	$V_{CM\_PD}$	-10	0	10	mV	Note 4,6,8
EIDL state common mode voltage noise	$V_{CM\_PD\_noise}$	-100	0	150	mV	Note 4,6,8,11,12
EIDL state total common mode voltage	$V_{CM\_PD\_total}$	-110	0	160	mV	Note 6,8,11,12
Total Jitter	$T_J$	-	-	0.35	UI	Refer to Section 4.3.4
Inter skew	$Sk_{inter}$	-	-	0.35	UI	Note 9

Note 1: With a differential termination of  $100\Omega$ .

Note 2: The maximum differential voltage is allowed up to 560mV only when first driving STB-L just after power up.

After first STB.L driving, the following SYN symbols shall conform to the regular signaling voltage definitions (280mV maximum)

Note 3: Designers should consider improvement of signal integrity and reduction of EMI to determine rise/fall time of Host and Device output. Use of slower rise/fall time in Range A compare with Range B is an example implementation.

Note 4:  $V_{CM\_source}$  is the common-mode voltage which is transmitted by Device Tx together with diff D0/D1 signal  
 $V_{CM\_noise}$  is the common-mode voltage which is added because of Device internal activity. See Appendix E.2.3

$V_{CM\_PD}$  is the common-mode voltage which is generated by Device Tx in EIDL state.

$V_{CM\_PD\_noise}$  is the common-mode voltage which is added because of Device internal activity in EIDL state.

See Appendix E.2.3

Note 5:  $V_{CM\_total} = V_{CM\_source} + V_{CM\_noise}$ .

Note 6:  $V_{CM\_PD\_total} = V_{CM\_PD} + V_{CM\_PD\_noise}$ .

Note 7:  $V_{CM\_source}$  and  $V_{CM\_PD}$  are measured in reference to its local GND.

(more details in UHS-II PHY Test Guideline document).

Note 8: In EIDL state, both positive and negative lines of D1 Lane are pulled down by Tx.

Note 9: Inter skew means the skew between D0 and D1 when both transmitters transmit from Host to Device. This is mandatory for 2L-HD mode and not applied to FD mode.

Note 10: This parameter is valid while the Tx drives the following states: Active transfer, STB\_L, STB\_H.

Note 11: Using Section 4.3.7 – "Host Power Delivery Network Model" as device design condition

Note 12: It is recommended to follow the design guidelines at Appendix E.2.3.

**Table 4-10: D0, D1 Output Requirement at TP2 for Device Transmitter**

#### 4.3.2.4 Host Receiver Specification

When Host receives D1 signal (and D0 signal on 2L-HD mode) from Device, Host receiver shall comply with the requirement listed in Table 4-11 at TP2 at own data rate.

The eye-mask template for Host receiver at TP2 related to Table 4-11 is shown in Figure 4-6 (5). Host receiver shall be capable to receive signals that comply with requirements defined in Table 4-11 and Figure 4-6 (5).

Item	Symbol	Value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	110	-	-	mV	Absolute value.
Common mode voltage	$V_{CM}$	50	200	400	mV	Note 1
EIDL state common mode voltage	$V_{CM\_PD}$	-110	0	160	mV	Note 1,2
Total Jitter	$T_J$	-	-	0.4	UI	Refer to Section 4.3.4 Note 3

Note 1:  $V_{CM\_PD}$  and  $V_{CM}$  are measured in reference to its local GND. (more details in UHS-II PHY Test Guideline document)

Note 2: In EIDL state, both positive and negative lines of D1 Lane are pulled down by Tx.

Note 3: Host Rx data recovery function minimum BW is  $2.34MHz/S_f$ , as described on Figure 4-7(2)

Note 4: Host Receiver shall tolerate the inter skew spec defined at Table 4-10 and additional inter skew caused in Host PCB.

**Table 4-11: Input Requirement at TP2 for Host Receiver**

#### 4.3.3 Eye-mask Template

The eye-mask templates are the graphical representation of the limit for the voltage and jitter for the differential signals. The eye-mask templates of UHS-II are shown in Figure 4-6. The horizontal margin of eye-mask template is calculated as  $1 \text{ UI} - T_J$ .

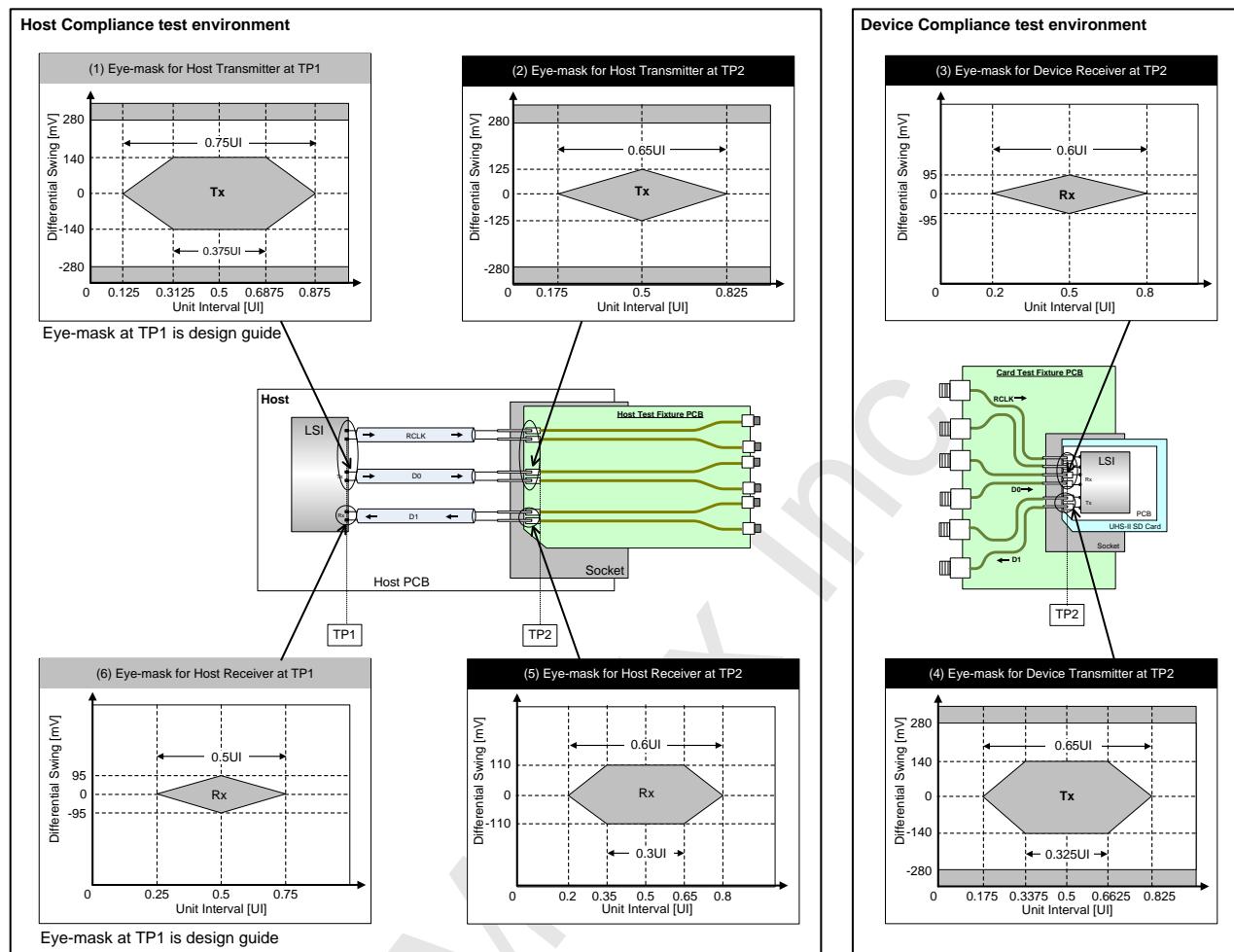
For the transmitters of Host and Device, when transmitting differential signal, these signals including over/under-shoot shall remain in the white area of each Eye-mask template (Tx) in Figure 4-6 at any time except in EIDL state.

For the receivers of Host and Device, when receiving the differential signals that have the eye-opening shown in eye-templates (Rx) in Figure 4-6, receivers shall receive these signals correctly.

The eye mask templates specified in Figure 4-6 refers to measurements at standard measurement conditions and BER of 1E-12. The standard measurement conditions are described in UHS-II PHY Test Guideline document.

Note: The Host and Device are tested separately at "ideal" compliance environment, while in real system Host and Device are connected together, so there will be some mutual effects because of this connection. The margin between (2) to (3) Eye-masks and (4) Eye-mask to (5) Eye-mask are taken because of that. The following elements are covered by this margin:

- A. Power delivery noise,
- B. Internal Device Xtalk due to other internal activity



Note 1 : In case of Host LSI and embedded device connection, the same Eye-mask templates are applied respectively.

Note 2 : For eye testing De-embedding of the test fixture should be performed. (More details in UHS-II Test Guidelines document)

Note 3 : RCLK shall be used as reference when testing downstream (host transmitter) eye diagram. Details are defined in UHS-II Test Guidelines document.

Note 4 : Eye diagram for upstream (Device transmitter) is measured related to itself using a Clock Recovery Unit (CRU) inside the test equipment. CRU bandwidth and detailed measurement procedure are described in the UHS-II Test Guidelines document.

Note 5 : D0/D1 jitter for Host Tx is measured related to RCLK using a 2nd order soft PLL with BW of  $2.34\text{MHz}/S_f$  inside the test equipment. Detailed measurement procedure is described in the UHS-II Test Guidelines document.

**Figure 4-6: Eye-mask Templates**

#### 4.3.4 Jitter

The relation between eye-opening and total jitter is defined by Eye Opening = 1UI -  $T_J$ . The more jitter, the less eye-opening. Thus, for ensuring the interconnection between Host and Device, jitter specification shall be adhered for each differential Lane: RCLK, D0 and D1.

Total Jitter  $T_J$  consists of two jitter components: deterministic peak to peak jitter  $D_J$  and random root mean square jitter  $R_{J\_rms}$ .

Total Jitter  $T_J$  is calculated by the following equation:

$$T_J = D_J + Q \cdot R_{J\_rms}$$

Where, Q factor is related to Bit error rate (BER). In UHS-II, BER performance of PHY shall be achieved by  $10^{-12}$ , when Q is 14.1.

The  $D_J$  contains two elements  $D_J(\text{ISI})$  which is the deterministic jitter caused by ISI and  $S_J$  which is a sinusoidal jitter component.

Test pattern, jitter element budgeting and jitter injection method is specified in UHS-II PHY Test Guideline document.

##### 4.3.4.1 Downstream Jitter

Generally speaking about tendency of PLL, the lower frequency the more jitter tends to go through. RCLK and D0 (also D1 when it is used as downstream) may have a lot of low frequency jitter.

But in case that Host and Device are connected as point to point topology, RCLK and D0 transmitted by the Host are coherent transfer system. In such a system both RCLK and D0 may have the same correlative jitter and no relative jitter between RCLK and D0. This correlative jitter is invisible for Device Rx data recovery function within Device Rx PLL BW.

On the other hand, in case of Ring topology (especially Device #2 or latter Device), RCLK is provided from Host directly and D0 is provided from adjacent Device in the Ring. Thus, Device receiver will see uncorrelated low frequency jitter (non-coherent transfer system).

Taking in account the two cases above, the jitter tolerance specification of a Device receiver is defined at Figure 4-7(1) as relative to RCLK. To follow the non-coherent transfer system, Device receiver shall comply with Figure 4-7(1).

This Downstream jitter specification for Device receiver is applied not only for Device D0 but also for Device D1 when it is used as Device Rx.

For the RCLK jitter specification is defined at Table 4-7, Table 4-9 and Table E-2.

Notes:

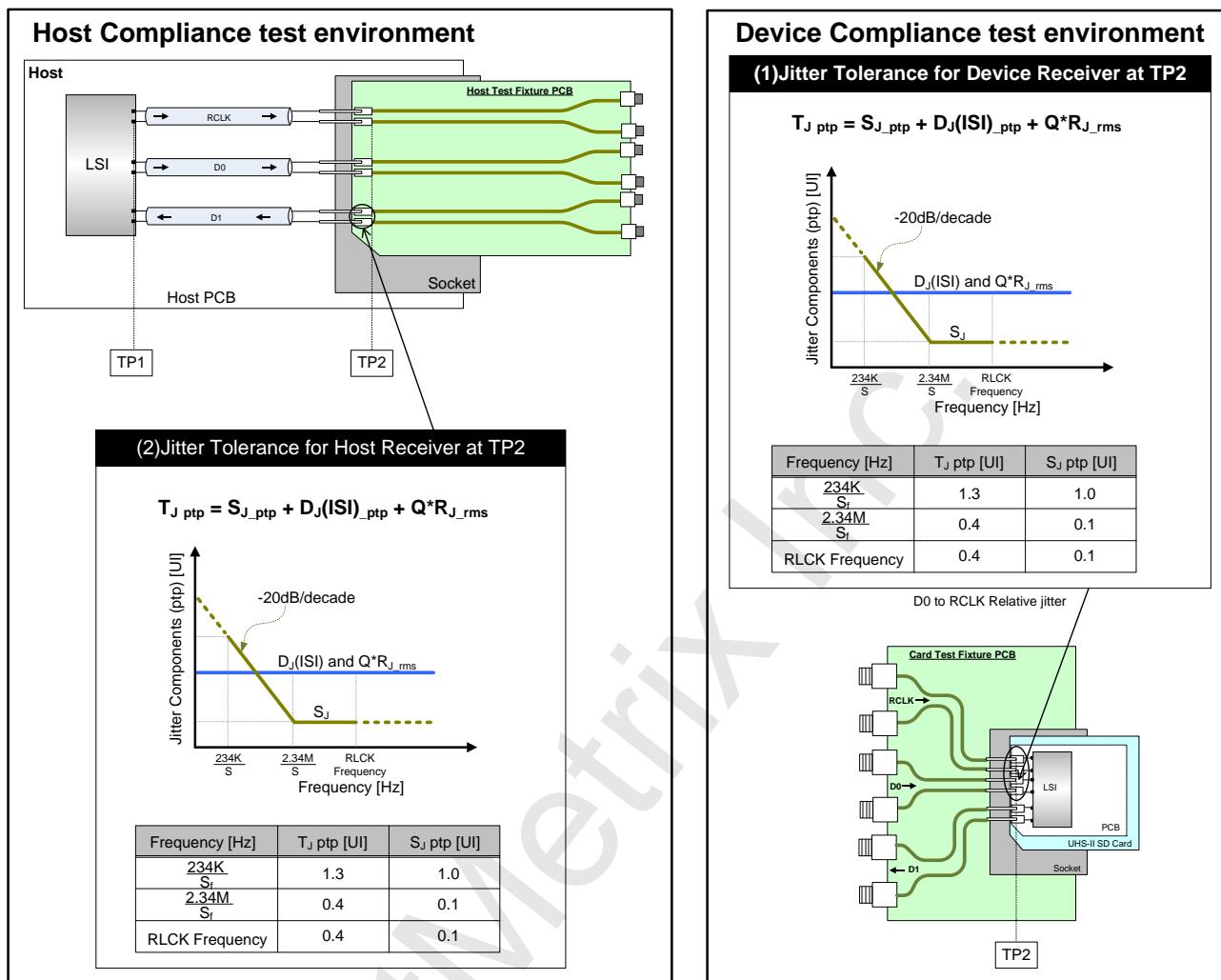
- It is recommended that Device data recovery function has wider bandwidth than Device Rx PLL.
- Device Rx PLL should be at least 2nd order.
- Effective minimum BW of Device Rx (PLL and CDR) should be 2.34MHz/S<sub>f</sub>.
- Device designer should take in account the influence of SSC on Rx PLL, data recovery function and Device Tx. For example: Certain amount of additional jitter is expected to appear on Device Rx PLL output, depending upon PLL design.

#### 4.3.4.2 Upstream Jitter

RCLK is generated by a PLL in the Host, D1 (also D0 when it is used as upstream) is generated by another PLL in a Device. Thus, a Host receiver will see the uncorrelated low frequency jitter. It is the same condition as Downstream Jitter of Ring topology above. The jitter tolerance specification of a Host receiver is defined as Figure 4-7(2). Host receiver shall comply with Figure 4-7(2).

The data recovery circuit in the Host receiver shall be designed to follow this non-coherent transfer system.

This Upstream jitter specification for Host is applied not only for Host D1 but also for Host D0 when it is used as Host Rx.



Note 1 : The graphs above shows each Jitter components for indicating the concept of Total Jitter budgeting. Refer to the UHS-II PHY Test Guidelines document for more details.

Note 2 : Scaling factor:  $S_f = \frac{1.56}{\text{actual data rate [Gbps]}}$

Note 3 : RLCK shall be used as reference when testing downstream (host transmitter) jitter. Details are defined in the UHS-II PHY Test Guidelines document.

Note 4 : In Jitter tolerance curves of (1) and (2) above, S<sub>J</sub> slope at low jitter frequencies is equal to -20dB/decade.

Note 5 : Regarding PHY testing, Rx will be tested with less jitter budget and different jitter cocktail than that of Addendum due to the test equipment's limitation. Refer to the UHS-II PHY Test Guideline document for more details.

**Figure 4-7: Jitter Tolerance Specification**

#### 4.3.5 Return Loss

The mismatch and unbalance of impedance between the components which form transmission Line causes the signal reflection. Signal reflection contributes to the degradation of signal integrity and EMI.

The return loss limits (differential return loss, common-mode return loss and common-to-differential return loss) are defined in UHS-II specification for keeping signal integrity and EMI mitigation.

Both transmitter and receiver shall comply with the return loss specification. When 2L-HD mode is supported, each port is bi-directional, thus return loss specification are applied for transmitter and receiver respectively.

The return loss is defined as the ratio of reflected power to incident power, and measured by using Test fixtures (Refer to Appendix C). The characteristic impedances of the Test Fixtures (mean differential impedance and common-mode impedance) are reference values for the return loss measurement. For Return Loss testing, De-embedding of the test fixture should be performed.

The detailed measurement method is described in UHS-II PHY Test Guideline document.

#### 4.3.5.1 Differential Mode Return Loss

The differential return loss  $RL_{DD}$  is the ratio of differential mode reflection power to differential mode incident power. It is defined as following:

$$RL_{DD} = 20 * \log_{10} |S_{DD11}|$$

Figure 4-8 is the  $RL_{DD}$  template and the detail limit level of the  $RL_{DD}$  for Device. These are applied both for transmitter and receiver of Device. The return loss of Device shall not exceed the limit.

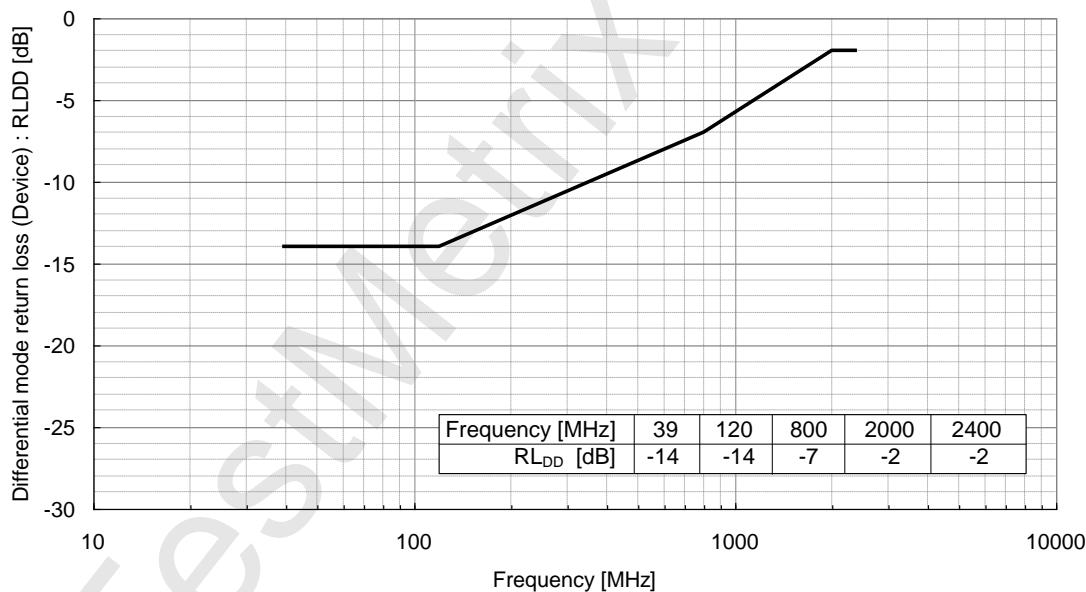
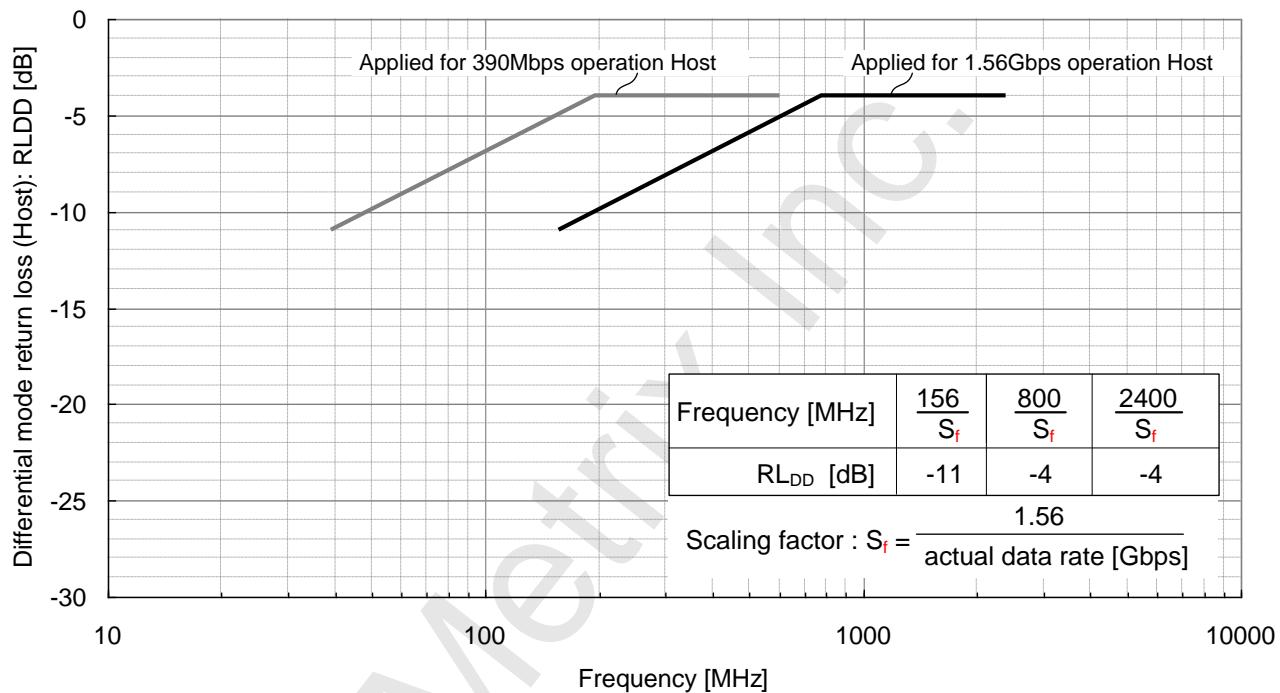


Figure 4-8: Differential Mode Return Loss ( $RL_{DD}$ ) Template for Device

Figure 4-9 is the  $RL_{DD}$  template and the detail limit level of the  $RL_{DD}$  for Host. It depends on Host's own maximum bit rate because Host may operate on specific bit rates, means it is not necessary to operate on maximum bit rate of UHS-II (1.56Gbps).

These are applied both for transmitter and receiver of Host. The return loss of Host shall not exceed the limit.



- Note 1: A specific RLDD Mask calculated using  $S_f$  scaling factor is mandatory for host to meet.  
 Note 2: For Device Receiver design, only Host RLDD mask with  $S_f=1$  shall be taken in account.

**Figure 4-9: Differential Mode Return Loss ( $RL_{DD}$ ) Template for Host**

#### 4.3.5.2 Common-mode Return Loss

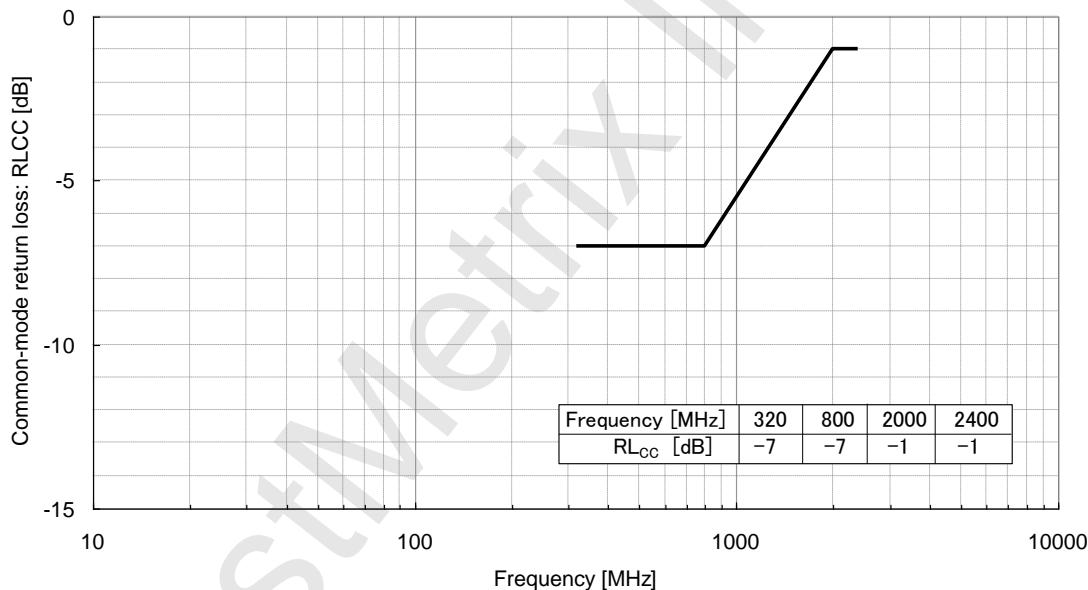
The common-mode return loss  $RL_{CC}$  is the ratio of common-mode reflection power to common-mode incident power. It is defined as following:

$$RL_{CC} = 20 * \log_{10} |S_{CC11}|$$

Figure 4-10 is the  $RL_{CC}$  template and the detail limit level of the  $RL_{CC}$ . These are applied both for transmitter and receiver. The return loss of Device and Host shall not exceed the limit.

Note: Some Hosts using common-mode filter to prevent EMI will not comply with the  $RL_{CC}$  limit level.

These Hosts shall be the only allowable exception. In this case special compliance conditions are defined. More details in UHS-II PHY Test Guideline document.



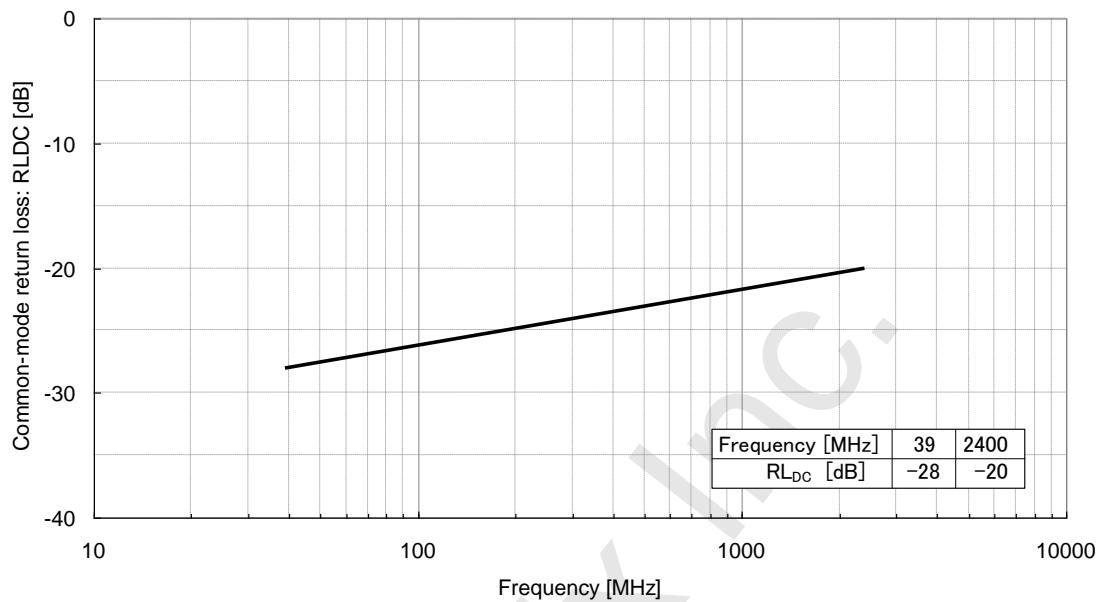
**Figure 4-10: Common-mode Return Loss ( $RL_{CC}$ ) Template**

#### 4.3.5.3 Common-to-Differential Return Loss (Impedance Balance)

The common-to-differential return loss (Impedance Balance)  $RL_{DC}$  is the ratio of common-mode incident power to differential-mode reflected power. It is defined as following:

$$RL_{DC} = 20 * \log_{10} |S_{DC11}|$$

Figure 4-11 is the  $RL_{DC}$  template the detail limit level of the  $RL_{DC}$ . These are applied both for transmitter and receiver. The return loss of Device and Host shall not exceed the limit.



**Figure 4-11: Common-to-Differential Return Loss (RL<sub>DC</sub>) Template**

#### 4.3.6 Line States

UHS-II has the following 4 Line states:

- **DIF-H** denotes differential high state. That means the positive terminal of Tx outputs is at high level, and the negative terminal of Tx outputs is low level.
- **DIF-L** denotes differential low state. That means the positive terminal of Tx outputs is at low level, and the negative terminal of Tx outputs is at high level.
- **DIF-PD** denotes Pull down state. Both single-ended voltage levels of a differential Line ( $V_{Dp}$  and  $V_{Dn}$ ) are pulled down to  $V_{CM\_PD}$  by TX.
- **DIF-Z** denotes High-Z (high impedance). Tx becomes High-Z.

Transmission Line Status	Symbol	Signal Levels	Condition of application	Remarks
Differential High	DIF-H	$V_{Dp} = V_{DH}$ $V_{Dn} = V_{DL}$	-Active-state	
Differential Low	DIF-L	$V_{Dp} = V_{DL}$ $V_{Dn} = V_{DH}$	-Active-state	
Pull down	DIF-PD	$V_{Dp} = V_{Dn} = V_{CM\_PD}$	-EIDL state	
Hi-Z	DIF-Z	Floating	-2L-HD switching	

Table 4-12: Line States

#### 4.3.7 Host Power Delivery Network Model

The Host power delivery model for VDD1 and VDD2 domains is defined in Figure 4-12.

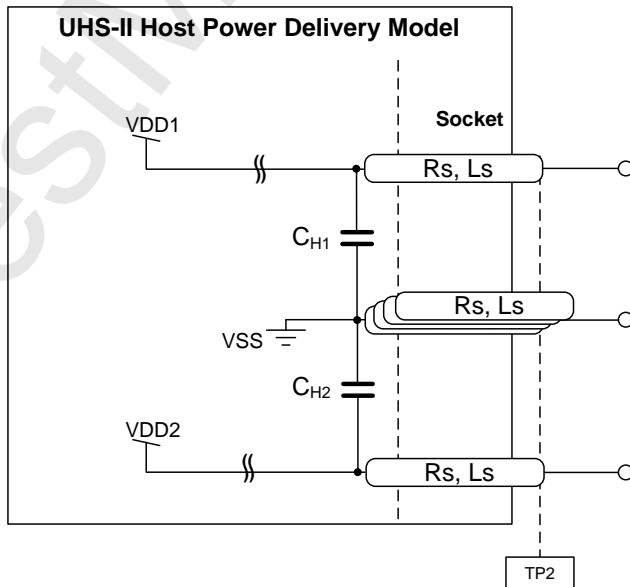


Figure 4-12: Power Delivery Network for VDD1 and VDD2 Domains

$R_s, L_s$  - Resistance/Inductance of each contact pin of the UHS-II Socket.

Refer to mechanical addendum for detailed definition.

$C_{H1}, C_{H2}$  - Decoupling capacitors adjacent to the UHS-II Socket.

Note 1: It is mandatory for Host to place  $C_{H1}$  and  $C_{H2}$  adjacent to the socket pins as shown in Figure 4-12, for each power domain (VDD1, VDD2). Otherwise Host may fail interoperability with Device. Sum of equivalent series inductance (ESL) of these capacitors and inductance of their connection to the socket should be negligible value than  $L_S$ . (Less than  $L_S/10$ )

Note 2: The Host Power Delivery Network Model described in Figure 4-12 is condition for Device Receiver and Transmitter functionality. In other conditions Device circuitry may not perform properly.

Note 3: Properties of the  $C_{H1}$  and  $C_{H2}$  Capacitors:

- Minimum value is 1[uF] (nominal value)
- Capacitor such as MLCC X5R/X7R with low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Any size of capacitor may be used (0201, 0402, 0603...), as long as it is not too big to be located very close to socket pins.
- Should be allocated adjacent to UHS-II socket.

**Application Note:**

The capacitors configuration may be improved to give better noise rejection properties per Host designer consideration. Additionally Host may choose to add more capacitors to support hot-insertion, for voltage stabilization or any other reason. Refer to Appendix E of the Physical Layer Version 4.00 for more information.

#### 4.4 EIDL State

When recovering from EIDL state, Amplitude Detector is used for detecting the voltage level of differential transmission Line, making receiver waked up and informs link layer that the differential Lane gets out of EIDL state.

Device D0 receiver, and Host D1 receiver have Amplitude Detector (mandatory for Device D0 receiver; optional for Host D1 receiver), as shown in Figure 4-2

During EIDL state, the state of the differential Line is settled to DIF-PD as shown Figure 4-13 as measured in receiver side.

During Dormant state, Host may settle the RCLK Lane to DIF-PD (Refer to the timing diagram Figure 5-23 in Protocol specification).

When getting out of EIDL state, the driver of the differential Lane (means D0 driver of Host or D1 driver of Device) shall settle the differential voltage from DIF-PD to DIF-L within 2SI, and then transmits DIF-L during 14SI for the detection by the Rx Amplitude Detector.

The minimum input differential voltage  $V_{Dn}-V_{Dp}$  is 95mV (DIF-L), the Rx Amplitude Detector shall detect the 95mV DIF-L as minimum within 14SI STB.L period (ex. 90mV as Detection threshold of Amplitude Detector is recommended, though it's implementation specific).

When the detection occurs, the high speed receivers are waked up and the link layer is being notified for EIDL recovery.

To increase the noise immunity, it is recommended to implement the Amplitude Detector with hysteresis.

When entering EIDL state, the driver of the differential Lane shall drive the differential voltage to DIF-H and then drive to DIF-PD controlled by Link layer. The Rx Amplitude Detector shall be masked before Rx transit to EIDL state (mean until the end of T\_EIDL\_GAP) and unmasked afterwards (refer to Figure 5-26 for further details).

Regarding the Power Management including EIDL state, refer to Section 5.4.

**Notes:**

1. On performing a compliance test, test equipment may have a difficulty to keep the defined timing where state transition occurs from and to EIDL state. In this case, the test equipment may provide a lane with  $V_{cm}$  level on Device test or  $V_{cm\_source}$  level on Host test, instead of DIF\_PD for EIDL.  $V_{dp}$  and  $V_{dn}$  may vary within defined  $V_{cm}$  or  $V_{cm\_source}$  variation and  $|V_{dp}-V_{dn}|$  shall be less than or equal to  $V_{diff\_PD}$ . Amplitude Detector shall function properly with defined performance when detecting the transition from  $V_{cm}$  ( $V_{cm\_source}$ ) to STB.L. This condition is only valid for compliance testing.
2. In addition to input signals complying with the specification, it should be assumed the existence of CM noise caused inside of Device depends on implementation. Since the CM noise may affect Amplitude Detector, it is recommended to follow the design guidelines in Appendix E.2.3

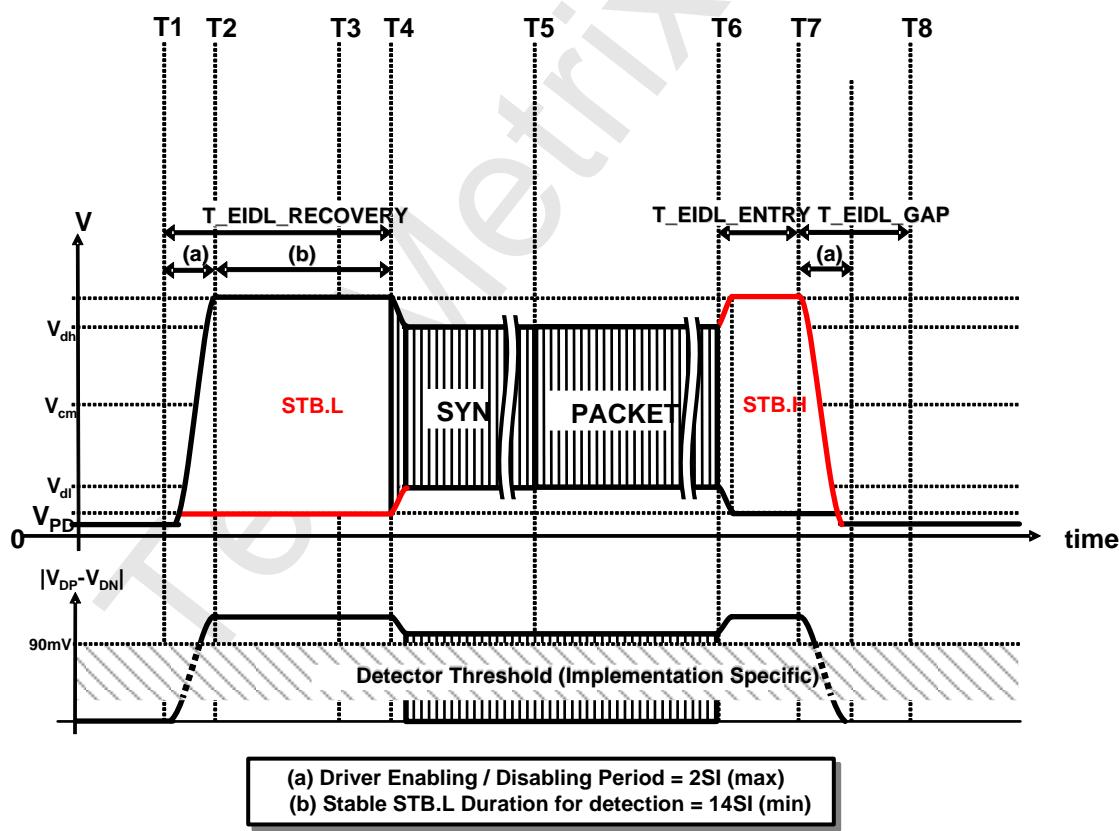


Figure 4-13: Line States and Timing in the Recovery from EIDL State and in EIDL Entry

## 4.5 Symbol Coding

UHS-II interface uses an 8b/10b transmission code in valid symbol transfer. The 8b/10b coding rule and the detail calculation method of Running Disparity (RD) refers to ANSI X3, 230-1994, clause 11 (and also IEEE 802.3z, 36.2.4)

As shown in Figure 4-14, 8-bit data characters ("HGFEDCBA") are treated as 3 bits ("HGF") and 5 bits ("EDCBA"), which are mapped onto a 4-bit code group ("jhgf") and a 6-bit code group ("iedcba"), respectively. The control bit in conjunction with the 8-bit data characters is used to indicate whether the transmission symbol is a Data symbol (D) or a Control symbol (K). After the mapping, bit "a" shall be transmitted first, followed by bits "b", "c", "d", "e", "i", "f", "g", "h" and "j" in that order. (Refer to Section 5.2.7 for related description.)

Table 4-13 to Table 4-16 show the valid translation tables between 8-bit data characters and 10-bit symbols. These tables shall be used for both 8-bit to 10-bit encoding at transmitter and 10-bit to 8-bit decoding at receiver.

The symbol K28.5 is treated as the comma (delimiter) symbol, which is used for symbol lock (or re-lock) of Deserializer for the Receiver side when symbol lock is unlocked. (Refer to Section 5.2.2.2). And also, the comma symbol is used for initialization (or re-initialization) of RD value when RD becomes incorrect value by some kind of reason.

Regarding the handling for Symbol coding errors (8b/10b decode error and 8b/10b disparity error), refer to Section 5.2.8.3.

Note: during the period of not transferring valid symbol (such as exiting EIDL state and so on), Fixed Low (continuous DIF-L), Fixed High (continuous DIF-H) and Fixed Pull-down (continuous DIF-PD) are transmitted on UHS-II interface. (Refer to Section 5.2.8.1 for more details including other Lane states)

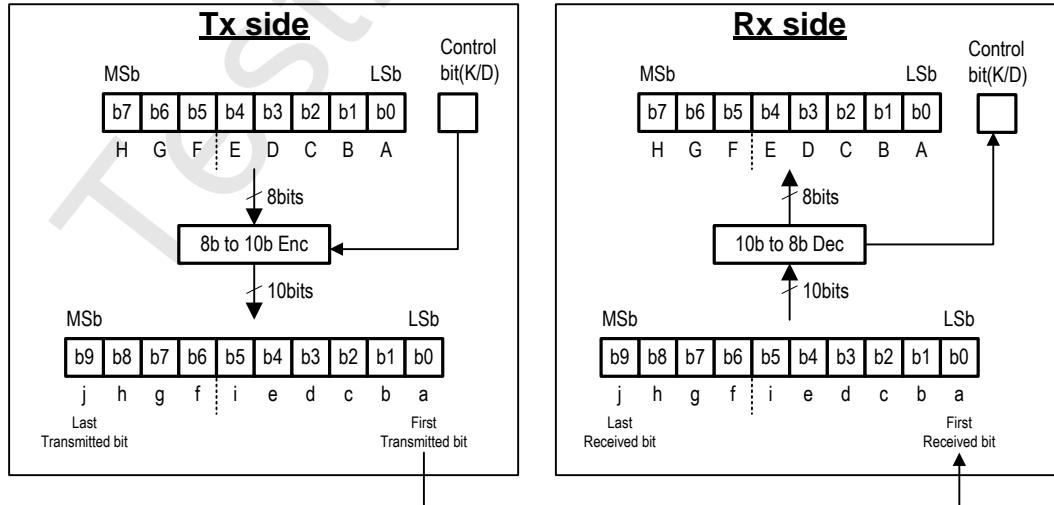


Figure 4-14: Diagram of Symbol Coding

8bit data characters		10bit data symbol		8bit data characters		10bit data symbol	
		Current RD-	Current RD+			Current RD-	Current RD+
Name	HGF EDCBA	abcdei fghj	abcdei fghj	Name	HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D16.1	001 10000	011011 1001	100100 1001
D1.0	000 00001	011101 0100	100010 1011	D17.1	001 10001	100011 1001	100011 1001
D2.0	000 00010	101101 0100	010010 1011	D18.1	001 10010	010011 1001	010011 1001
D3.0	000 00011	110001 1011	110001 0100	D19.1	001 10011	110010 1001	110010 1001
D4.0	000 00100	110101 0100	001010 1011	D20.1	001 10100	001011 1001	001011 1001
D5.0	000 00101	101001 1011	101001 0100	D21.1	001 10101	101010 1001	101010 1001
D6.0	000 00110	011001 1011	011001 0100	D22.1	001 10110	011010 1001	011010 1001
D7.0	000 00111	111000 1011	000111 0100	D23.1	001 10111	111010 1001	000101 1001
D8.0	000 01000	111001 0100	000110 1011	D24.1	001 11000	110011 1001	001100 1001
D9.0	000 01001	100101 1011	100101 0100	D25.1	001 11001	100110 1001	100110 1001
D10.0	000 01010	010101 1011	010101 0100	D26.1	001 11010	010110 1001	010110 1001
D11.0	000 01011	110100 1011	110100 0100	D27.1	001 11011	110110 1001	001001 1001
D12.0	000 01100	001101 1011	001101 0100	D28.1	001 11100	001110 1001	001110 1001
D13.0	000 01101	101100 1011	101100 0100	D29.1	001 11101	101110 1001	010001 1001
D14.0	000 01110	011100 1011	011100 0100	D30.1	001 11110	011110 1001	100001 1001
D15.0	000 01111	010111 0100	101000 1011	D31.1	001 11111	101011 1001	010100 1001
D16.0	000 10000	011011 0100	100100 1011	D0.2	010 00000	100111 0101	011000 0101
D17.0	000 10001	100011 1011	100011 0100	D1.2	010 00001	011101 0101	100010 0101
D18.0	000 10010	010011 1011	010011 0100	D2.2	010 00010	101101 0101	010010 0101
D19.0	000 10011	110010 1011	110010 0100	D3.2	010 00011	110001 0101	110001 0101
D20.0	000 10100	001011 1011	001011 0100	D4.2	010 00100	110101 0101	001010 0101
D21.0	000 10101	101010 1011	101010 0100	D5.2	010 00101	101001 0101	101001 0101
D22.0	000 10110	011010 1011	011010 0100	D6.2	010 00110	011001 0101	011001 0101
D23.0	000 10111	111010 0100	000101 1011	D7.2	010 00111	111000 0101	000111 0101
D24.0	000 11000	110011 0100	001100 1011	D8.2	010 01000	111001 0101	000110 0101
D25.0	000 11001	100110 1011	100110 0100	D9.2	010 01001	100101 0101	100101 0101
D26.0	000 11010	010110 1011	010110 0100	D10.2	010 01010	010101 0101	010101 0101
D27.0	000 11011	110110 0100	001001 1011	D11.2	010 01011	110100 0101	110100 0101
D28.0	000 11100	001110 1011	001110 0100	D12.2	010 01100	001101 0101	001101 0101
D29.0	000 11101	101110 0100	010001 1011	D13.2	010 01101	101100 0101	101100 0101
D30.0	000 11110	011110 0100	100001 1011	D14.2	010 01110	011100 0101	011100 0101
D31.0	000 11111	101011 0100	010100 1011	D15.2	010 01111	010111 0101	101000 0101
D0.1	001 00000	100111 1001	011000 1001	D16.2	010 10000	011011 0101	100100 0101
D1.1	001 00001	011101 1001	100010 1001	D17.2	010 10001	100011 0101	100011 0101
D2.1	001 00010	101101 1001	010010 1001	D18.2	010 10010	010011 0101	010011 0101
D3.1	001 00011	110001 1001	110001 1001	D19.2	010 10011	110010 0101	110010 0101
D4.1	001 00100	110101 1001	001010 1001	D20.2	010 10100	001011 0101	001011 0101
D5.1	001 00101	101001 1001	101001 1001	D21.2	010 10101	101010 0101	101010 0101
D6.1	001 00110	011001 1001	011001 1001	D22.2	010 10110	011010 0101	011010 0101
D7.1	001 00111	111000 1001	000111 1001	D23.2	010 10111	111010 0101	000101 0101
D8.1	001 01000	111001 1001	000110 1001	D24.2	010 11000	110011 0101	001100 0101
D9.1	001 01001	100101 1001	100101 1001	D25.2	010 11001	100110 0101	100110 0101
D10.1	001 01010	010101 1001	010101 1001	D26.2	010 11010	010110 0101	010110 0101
D11.1	001 01011	110100 1001	110100 1001	D27.2	010 11011	110110 0101	001001 0101
D12.1	001 01100	001101 1001	001101 1001	D28.2	010 11100	001110 0101	001110 0101
D13.1	001 01101	101100 1001	101100 1001	D29.2	010 11101	101110 0101	010001 0101
D14.1	001 01110	011100 1001	011100 1001	D30.2	010 11110	011110 0101	100001 0101
D15.1	001 01111	010111 1001	101000 1001	D31.2	010 11111	101011 0101	010100 0101

Table 4-13: Data Symbol 8b/10b Coding Table

8bit data characters		10bit data symbol		8bit data characters		10bit data symbol	
		Current RD-	Current RD+			Current RD-	Current RD+
Name	HGF EDCBA	abcdei fghj	abcdei fghj	Name	HGF EDCBA	abcdei fghj	abcdei fghj
D0.3	011 00000	100111 0011	011000 1100	D16.4	100 10000	011011 0010	100100 1101
D1.3	011 00001	011101 0011	100010 1100	D17.4	100 10001	100011 1101	100011 0010
D2.3	011 00010	101101 0011	010010 1100	D18.4	100 10010	010011 1101	010011 0010
D3.3	011 00011	110001 1100	110001 0011	D19.4	100 10011	110010 1101	110010 0010
D4.3	011 00100	110101 0011	001010 1100	D20.4	100 10100	001011 1101	001011 0010
D5.3	011 00101	101001 1100	101001 0011	D21.4	100 10101	101010 1101	101010 0010
D6.3	011 00110	011001 1100	011001 0011	D22.4	100 10110	011010 1101	011010 0010
D7.3	011 00111	111000 1100	000111 0011	D23.4	100 10111	111010 0010	000101 1101
D8.3	011 01000	111001 0011	000110 1100	D24.4	100 11000	110011 0010	001100 1101
D9.3	011 01001	100101 1100	100101 0011	D25.4	100 11001	100110 1101	100110 0010
D10.3	011 01010	010101 1100	010101 0011	D26.4	100 11010	010110 1101	010110 0010
D11.3	011 01011	110100 1100	110100 0011	D27.4	100 11011	110110 0010	001001 1101
D12.3	011 01100	001101 1100	001101 0011	D28.4	100 11100	001110 1101	001110 0010
D13.3	011 01101	101100 1100	101100 0011	D29.4	100 11101	101110 0010	010001 1101
D14.3	011 01110	011100 1100	011100 0011	D30.4	100 11110	011110 0010	100001 1101
D15.3	011 01111	010111 0011	101000 1100	D31.4	100 11111	101011 0010	010100 1101
D16.3	011 10000	011011 0011	100100 1100	D0.5	101 00000	100111 1010	011000 1010
D17.3	011 10001	100011 1100	100011 0011	D1.5	101 00001	011101 1010	100010 1010
D18.3	011 10010	010011 1100	010011 0011	D2.5	101 00010	101101 1010	010010 1010
D19.3	011 10011	110010 1100	110010 0011	D3.5	101 00011	110001 1010	110001 1010
D20.3	011 10100	001011 1100	001011 0011	D4.5	101 00100	110101 1010	001010 1010
D21.3	011 10101	101010 1100	101010 0011	D5.5	101 00101	101001 1010	101001 1010
D22.3	011 10110	011010 1100	011010 0011	D6.5	101 00110	011001 1010	011001 1010
D23.3	011 10111	111010 0011	000101 1100	D7.5	101 00111	111000 1010	000111 1010
D24.3	011 11000	110011 0011'	001100 1100	D8.5	101 01000	111001 1010	000110 1010
D25.3	011 11001	100110 1100	100110 0011	D9.5	101 01001	100101 1010	100101 1010
D26.3	011 11010	010110 1100	010110 0011	D10.5	101 01010	010101 1010	010101 1010
D27.3	011 11011	110110 0011	001001 1100	D11.5	101 01011	110100 1010	110100 1010
D28.3	011 11100	001110 1100	001110 0011	D12.5	101 01100	001101 1010	001101 1010
D29.3	011 11101	101110 0011	010001 1100	D13.5	101 01101	101100 1010	101100 1010
D30.3	011 11110	011110 0011	100001 1100	D14.5	101 01110	011100 1010	011100 1010
D31.3	011 11111	101011 0011	010100 1100	D15.5	101 01111	010111 1010	101000 1010
D0.4	100 00000	100111 0010	011000 1101	D16.5	101 10000	011011 1010	100100 1010
D1.4	100 00001	011101 0010	100010 1101	D17.5	101 10001	100011 1010	100011 1010
D2.4	100 00010	101101 0010	010010 1101	D18.5	101 10010	010011 1010	010011 1010
D3.4	100 00011	110001 1101	110001 0010	D19.5	101 10011	110010 1010	110010 1010
D4.4	100 00100	110101 0010	001010 1101	D20.5	101 10100	001011 1010	001011 1010
D5.4	100 00101	101001 1101	101001 0010	D21.5	101 10101	101010 1010	101010 1010
D6.4	100 00110	011001 1101	011001 0010	D22.5	101 10110	011010 1010	011010 1010
D7.4	100 00111	111000 1101	000111 0010	D23.5	101 10111	111010 1010	000101 1010
D8.4	100 01000	111001 0010	000110 1101	D24.5	101 11000	110011 1010	001100 1010
D9.4	100 01001	100101 1101	100101 0010	D25.5	101 11001	100110 1010	100110 1010
D10.4	100 01010	010101 1101	010101 0010	D26.5	101 11010	010110 1010	010110 1010
D11.4	100 01011	110100 1101	110100 0010	D27.5	101 11011	110110 1010	001001 1010
D12.4	100 01100	001101 1101	001101 0010	D28.5	101 11100	001110 1010	001110 1010
D13.4	100 01101	101100 1101	101100 0010	D29.5	101 11101	101110 1010	010001 1010
D14.4	100 01110	011100 1101	011100 0010	D30.5	101 11110	011110 1010	100001 1010
D15.4	100 01111	010111 0010	101000 1101	D31.5	101 11111	101011 1010	010100 1010

Table 4-14: Data Symbol 8b/10b Coding Table (cont.)

8bit data characters		10bit data symbol		8bit data characters		10bit data symbol	
		Current RD-	Current RD+			Current RD-	Current RD+
Name	HGF EDCBA	abcdei fghj	abcdei fghj	Name	HGF EDCBA	abcdei fghj	abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 4-15: Data Symbol 8b/10b Coding Table (cont.)

8bit control characters		10bit control symbol	
Name	HGF EDCBA	Current RD-	Current RD+
K28.0	000 11100	001111 0100	110000 1011
K28.1	001 11100	001111 1001	110000 0110
K28.2	010 11100	001111 0101	110000 1010
K28.3	011 11100	001111 0011	110000 1100
K28.4	100 11100	001111 0010	110000 1101
K28.5	101 11100	001111 1010	110000 0101
K28.6	110 11100	001111 0110	110000 1001
K28.7	111 11100	001111 1000	110000 0111
K23.7	111 10111	111010 1000	000101 0111
K27.7	111 11011	110110 1000	001001 0111
K29.7	111 11101	101110 1000	010001 0111
K30.7	111 11110	011110 1000	100001 0111

Table 4-16: Control Symbol 8b/10b Coding Table

## 4.6 Loopback Mode

The PHY block in the Device and Host shall have loopback path that is needed for testability purposes, and the loopback path is also used for Devices in order to perform data bypassing in ring topology (Regarding data bypassing in Ring topology, refer to Section 5.6.3 for more details). It is expected that loopback path will have the same clocking scheme as Tx and Rx lanes in FD mode, for both forward and backward loopback.

The loopback causes the data that is received at the serial input of a Lane to transmit at the serial output of another Lane after recovery. The loopback is done from the output of the de-serializer in the receiver path, to the input of the serializer of the transmitter path, by dedicated 10 bit multiplexer in the transmitter block. This loopback enables testing the PHY with any symbols including patterns which are illegal for 10b/8b decoding.

In normal condition, the loopback path in the PHY of the Host is done from the D1 receiver to the D0 transmitter, as presented in Figure 4-15. This path is named "forward loopback". For testing the other direction, which test D0 as receiver and D1 as transmitter, which are used in 2L-HD mode, there is a need for backward loopback path, as shown in Figure 4-16.

In normal condition, the loopback path in the PHY of the Device is done from the D0 receiver to the D1 transmitter, as presented in Figure 4-17. This path is named "forward loopback". For testing the other direction, which test D1 as receiver and D0 as transmitter, which are used in 2L-HD mode, there is a need for backward loopback path, as shown in Figure 4-18.

The loopback modes are controlled by the LINK layer while in normal operation, while in Test mode loopback may also be controlled internally in the PHY. Each PHY vendor may specify additional loopback modes, but it is beyond the mandatory requirements of the standard.

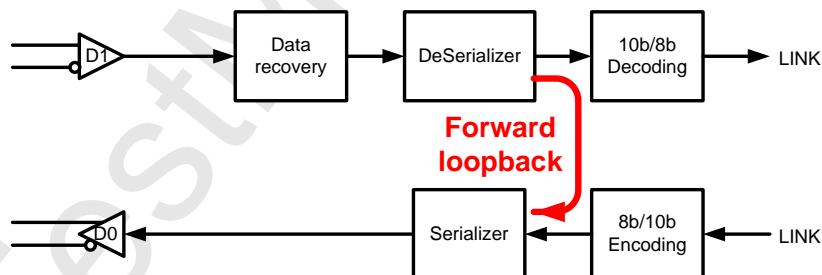


Figure 4-15: Location of Forward Loopback in PHY of the Host

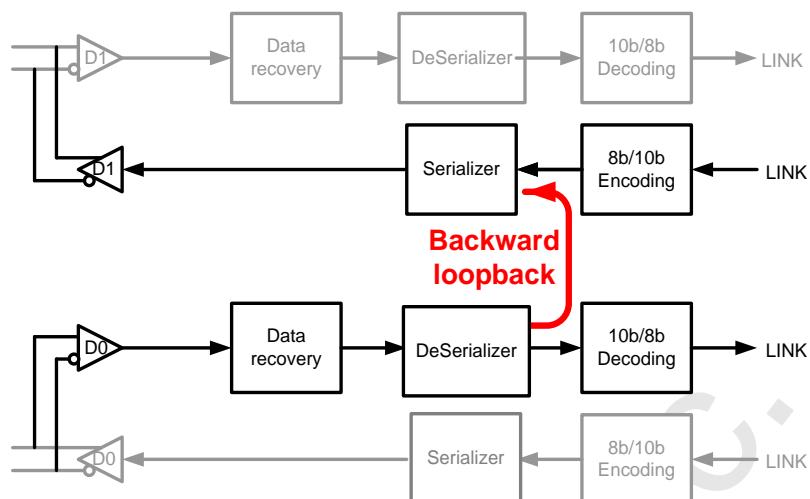


Figure 4-16: Location of Backward Loopback in PHY of the Host

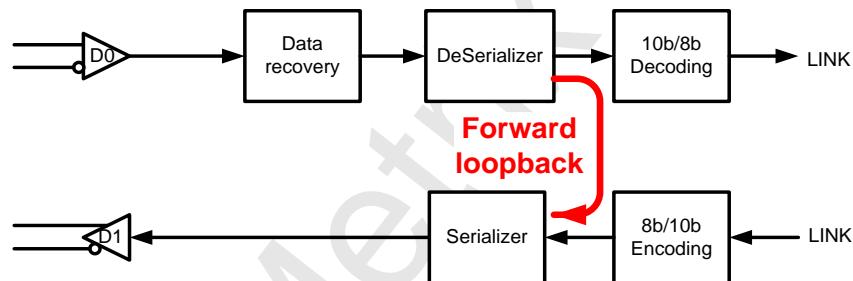


Figure 4-17: Location of Forward Loopback in PHY of the Device

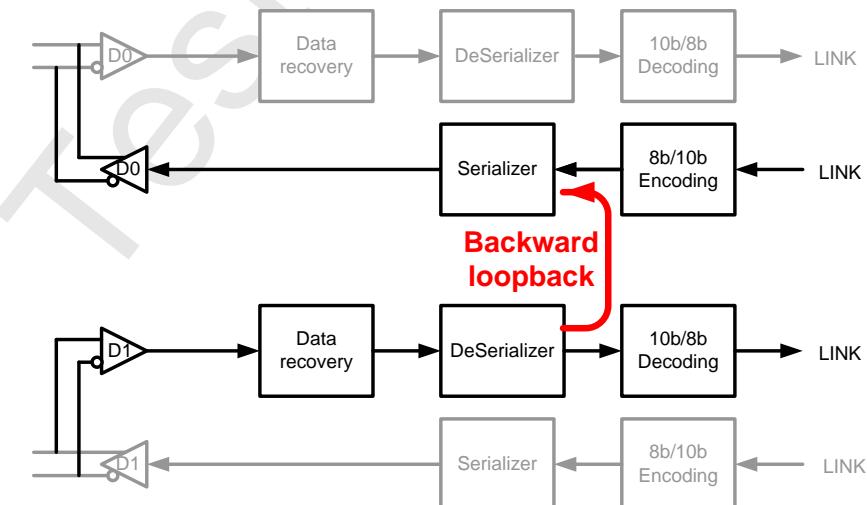


Figure 4-18: Location of Backward Loopback in PHY of the Device

## 4.7 PHY Test Mode

For the Compliance test of UHS-II PHY, Re-Sync state and following method are defined to UHS-II PHY in order to configure PHY for the specific test condition.

In PHY Test mode, Dormant state and Re-Sync state are used in case of changing PLL multiplier.

Dormant state used in PHY Test mode is the same state as in UHS-II normal operation, which is applied to the Rx which has Amplitude Detector (for example, Device D0.Rx), Therefore in the Dormant state during PHY Test mode, all PHY circuitry are powered off except Amplitude Detector. When exiting Dormant state, Amplitude Detector is used to detect STB.L.

Re-Sync state is applied to the Rx which has no Amplitude Detector (for example, Device D1.Rx). In the Re-Sync state PHY circuitry keeps power on (except for PLL while changing its multiplier) because Rx having no Amplitude Detector shall be able to receive symbols from Test equipment.

The difference between Dormant state and Re-Sync state is whether PHY is powered off or still powered on. Exiting Dormant state and Re-Sync state take the same sequences (Sequence to exit Dormant or Re-Sync; refer to Fig 4-19). When exiting these states, re-synchronization of CDR is performed.

Items to be configured in Test mode are as follows.

- Disconnect and Normal (Non-Disconnect) mode

- **Disconnect mode:**

Device and Host keep current test mode for any input levels.

That means Device and Host do not enter Dormant state even if the connection change happens between the Device/Host and test equipment. It is possible to exit Disconnect mode by using Power cycle, or transfer to Normal mode by using "Sequence to Set Test Mode".

- **Normal (Non-Disconnect) mode:**

This mode is capable to enter the Dormant state. This mode is useful to perform multiple test items automatically.

- Loop Back Direction

- **Forward Loopback:**

Default loopback direction for all Devices and Hosts.

- **Backward Loopback:**

Device and Host which support 2L-HD mode support Backward Loopback.

For Detailed Definition of Loopback modes, refer to Section 4.6 Loop Back mode.

**Notes:**

1. To enter Backward Loopback test mode, the sequence to set Test Mode (refer to Figure 4-19) shall be provided on Device D0 Rx and Host D1 Rx.
2. To enter Forward Loopback test mode retrieved from Backward Loopback test mode, the sequence to set Test Mode (refer to Figure 4-19) shall be provided on Device D1 Rx and Host D0 Rx.
3. Dormant state shall be used on Device D0 Rx (Forward Loopback) for testing an Amplitude Detector.

4. Which state Dormant or Re-sync should be used is dependent on implementation of Amplitude Detector especially on Device D1 Rx (Backward Loopback), Host D0 Rx (Backward Loopback) and Host D1 Rx (Forward Loopback).
5. Device and Host may transmit a few broken symbols instead of COM+SYN symbols expected, on switching Loopback direction.

- **PLL Multiplier factor**

PLL Multiplier factor may be set by the test mode entry method without setting configuration Register. Change of PLL Multiplier is effective only when exiting Dormant or Re-Sync state.

- **Future Test Mode Expandability**

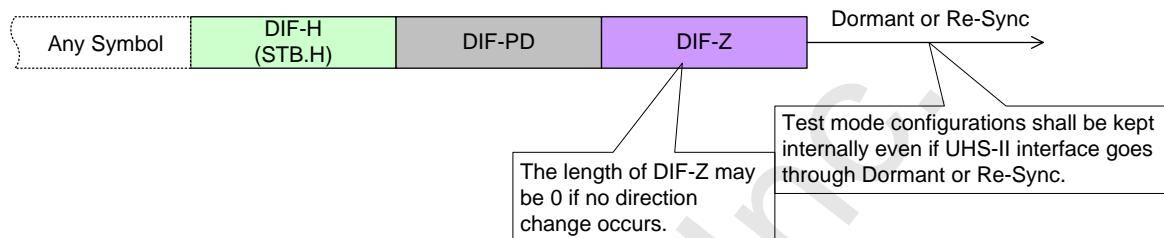
Additional vendor specific Test Modes may be defined.

#### 4.7.1 The Sequences used in PHY Test Mode

Figure 4-19 shows the sequences used in PHY Test Mode. Test mode configuration is done by setting the TMD1 and TMD2 in the symbol named "TEST-MODE" (which is constructed by COM (K28.5) + K-code (K30.7) + TMD1 + TMD2 as described in Figure 4-19). To avoid entering a test mode by mistake, TEST-MODE symbol is sent 4 times continuously.

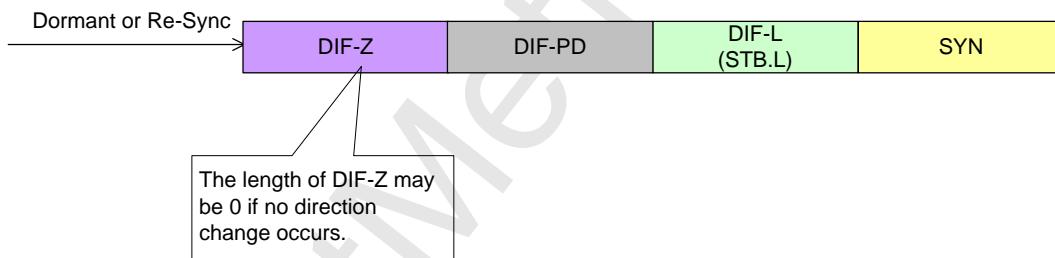
#### Sequence to Enter Dormant or Re-Sync

- When necessary to change PLL multiplier, this sequence is used



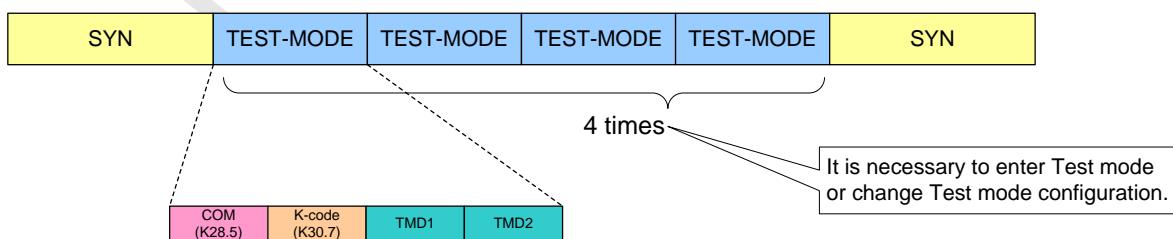
#### Sequence to Exit Dormant or Re-Sync

- When direction is switched, started by this sequence.
- When necessary to change PLL multiplier, this sequence is used



#### Sequence to Set Test Mode

- Before setting Test-Modes, re-synchronization should be performed by through Dormant or Re-Sync state. (Not necessary for every test mode setting.)



**Figure 4-19: Sequences used in PHY Test Mode**

#### 4.7.2 Definition of TMD1 and TMD2

The structure of TMD1 and TMD2 are defined as follows and in Figure 4-20. Device maintains setting of TMD1 and TMD2 during PHY test mode until Host changes setting of TMD1 and TMD2, even if going through Dormant or Re-Sync mode.

##### 4.7.2.1 TMD1

TMD1 is used for configuring Main mode and Sub mode.

Upper 4-bit is used to assign Main Mode:

- **0h** : assigned for Loop Back Test Modes
- **Fh** : assigned for vendor specific test modes (Vendor may define TMD1 and TMD2 to control vendor specific test modes)

Lower 4-bit is used to assign Sub Mode:

- **"Timing"(Sub Mode 00)**: determines the timing when Sub-Mode 03-01 is effective.
- **"Disconnect"(Sub Mode 01)**: determines whether Disconnected mode or Normal (Non-Disconnect mode).

##### 4.7.2.2 TMD2

TMD2 is specified by each Main Mode.

- **"Loop Back Direction"(07)**: determines whether Forward Loop back or Backward Loop back. When this bit is changed, the change of Loop Back Direction is done immediately.

Everytime Loopback direction is changed, both D0 and D1 are set to input at first in order to re-connect Test tool.

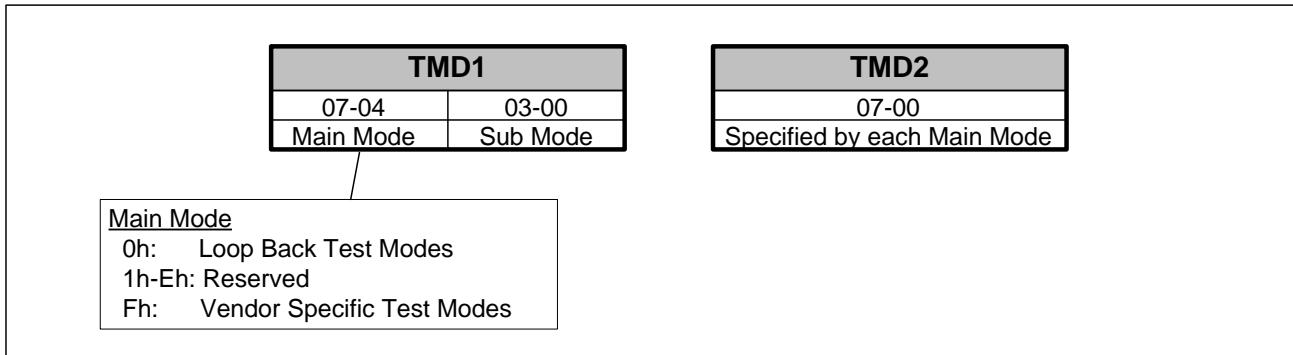
After re-connecting Test tool to Device/Host:

- <In case Loop Back Direction bit is changed 0 to 1>
  - After Device detects SYN from D1, D0 is enabled as output, and then the change of Loopback direction is done.
  - After Host detects SYN from D0, D1 is enabled as output, and then the change of Loopback direction is done.

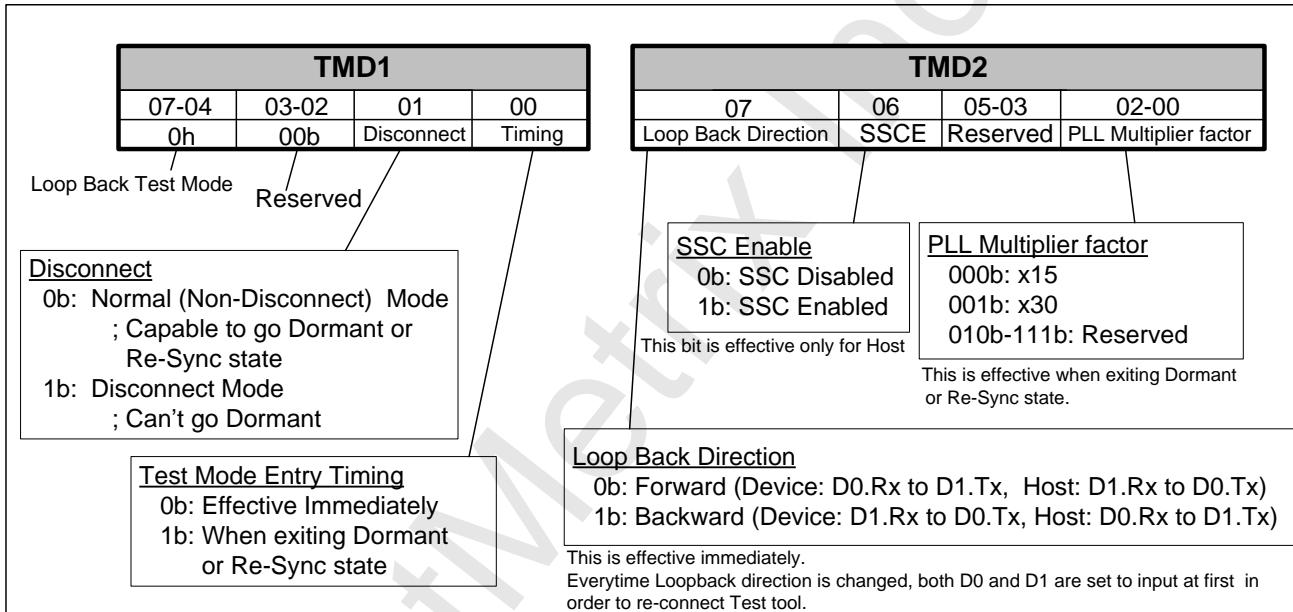
<In case Loop Back Direction bit is changed 1 to 0>

- After Device detects SYN from D0, D1 is enabled as output, and then the change of Loopback direction is done.
- After Host detects SYN from D1, D0 is enabled as output, and then the change of Loopback direction is done.

- **"SSCE"(06)**: controls Host SSC On/Off if Host supports SSC function. This bit is not effective to Device.
- **"PLL Multiplier factor"(02-00)**: determines PLL Multiplier (x15 or x30). The actual change of PLL Multiplier is done after exiting Dormant or Re-Sync state.



(a) General Definition



(b) TMD1 and TMD2 Definition in Loop Back Test Mode

Note: Symbols are described in 8-bit domain for the convenience of explanation. Actual symbols to enter and exit test mode are transferred from test equipment after 8b/10b encoding.

Figure 4-20: Structure of TMD1 and TMD2

#### 4.7.3 Test Modes

Parameters for entering each Test mode are described as follows. The sequences for entering each test mode are shown in Figure 4-21 and Figure 4-22.

##### TMD1 Modes:

- 00h: Normal Mode At Once

Setting in Sub Modes 03-01(Normal Mode) is effective immediately.  
After entering a test mode, it is possible to go back to Dormant state.

- 01h: Normal Mode Through Dormant state

Setting in Sub Modes 03-01(Normal Mode) is effective when exiting Dormant state.  
After entering a test mode, it is possible to go back to Dormant state.

- 02h: Disconnect Mode At Once

Setting in Sub Modes 03-01 (Disconnect Mode) is effective immediately.  
After entering a test mode, the Device cannot go Dormant state.

- 03h: Disconnect Mode Through Dormant state

Setting in Sub Modes 03-01 (Disconnect Mode) is effective when exiting Dormant state.  
After entering a test mode, the Device cannot go Dormant state.

##### TMD2 Modes:

###### PLL Multiplier (Bit 02-00)

- 000b: x15
- 001b:x30
- 010b-111b: Reserved

Change of this field is effective when exiting Dormant or Re-Sync state. Clock frequency may be changed only during Dormant or Re-Sync state.

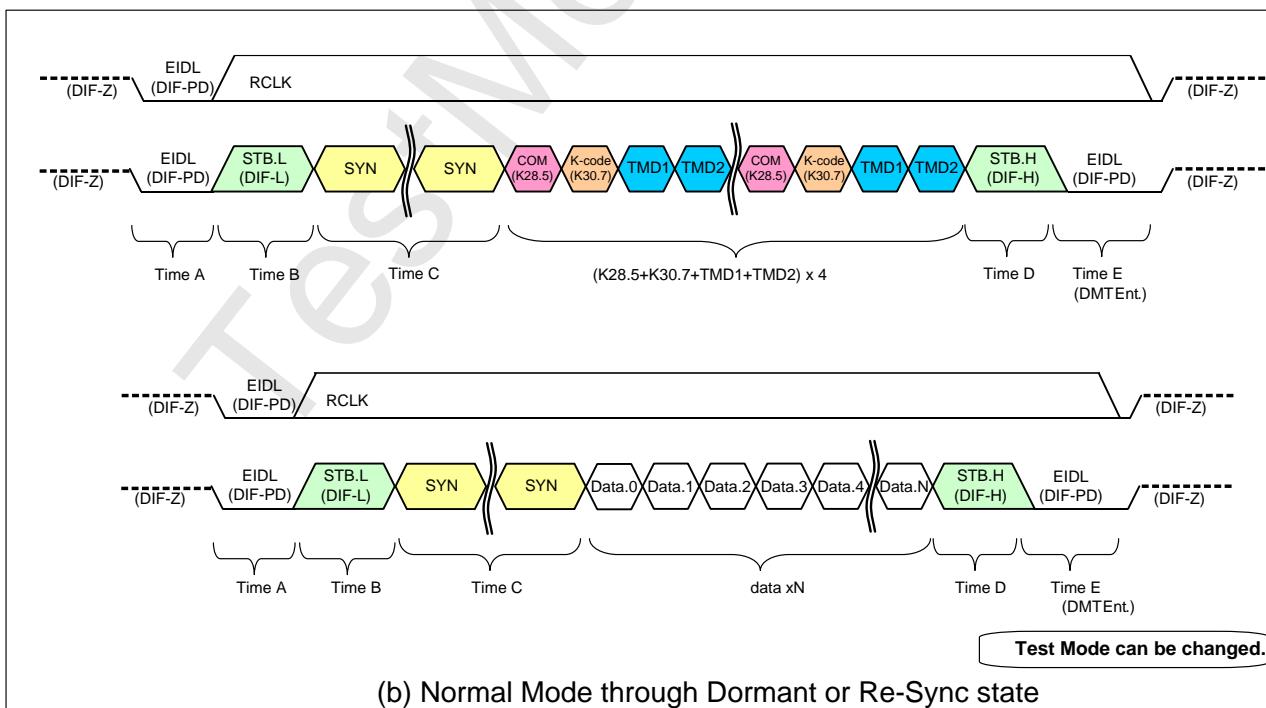
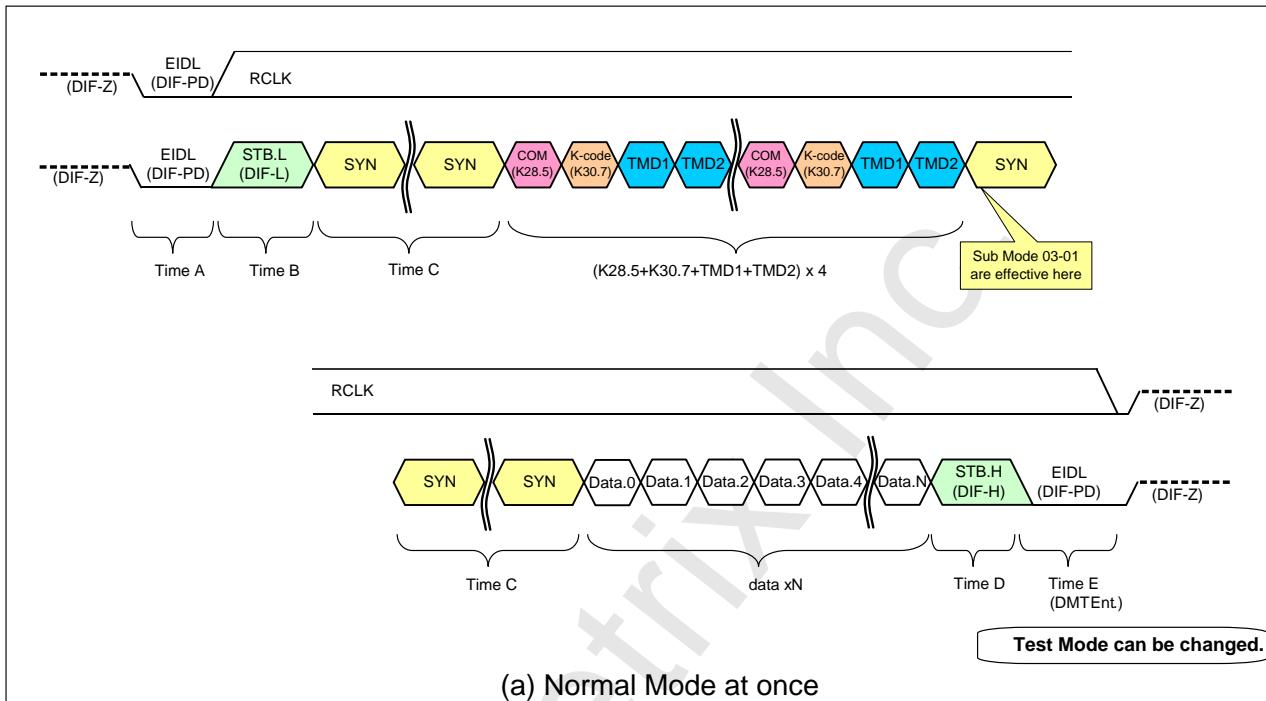
###### Loop Back Direction (Bit 07)

- 0b: Forward Loop Back (means from D0.Rx to D1.Tx)
- 1b: Backward Loop Back (means from D1.Rx to D0.Tx)

When this bit is changed, both D0 and D1 are set to input mode immediately.

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Time A	= EIDL Length	= After Power up 100ms (min.) (Manual Start) and after that 200us.
Time B	= Teidl_stb	= 200us(min.)
Time C	= Tactivate	= After Power up 100ms (min.) and after that 2ms (min.)
Time D	= T_EIDL_ENTRY	= 4SI (min.) PHY Spec. defines as fixed but test mode defines as min.
Time E	= T_DMT_ENTRY	= 750RCLK (min.)

**Figure 4-21: Normal Modes Sequence**

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Time A	= EIDL Length	= After Power up 100ms (min.) (Manual Start) and after that 200us.
Time B	= Teidl_stb	= 200us(min.)
Time C	= Tactivate	= After Power up 100ms (min.) and after that 2ms (min.)
Time D	= T_EIDL_ENTRY	= 4SI (min.) PHY Spec. defines as fixed but test mode defines as min.
Time E	= T_DMT_ENTRY	= 750RCLK (min.)

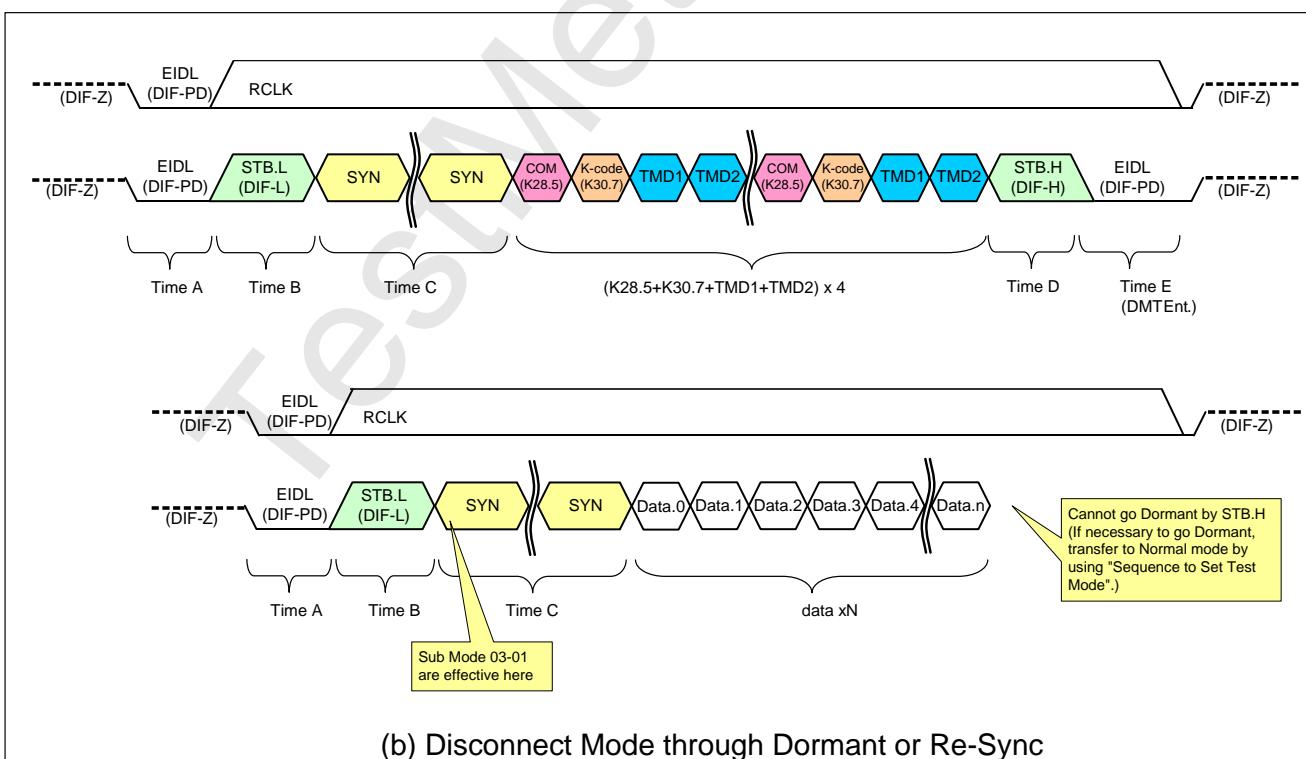
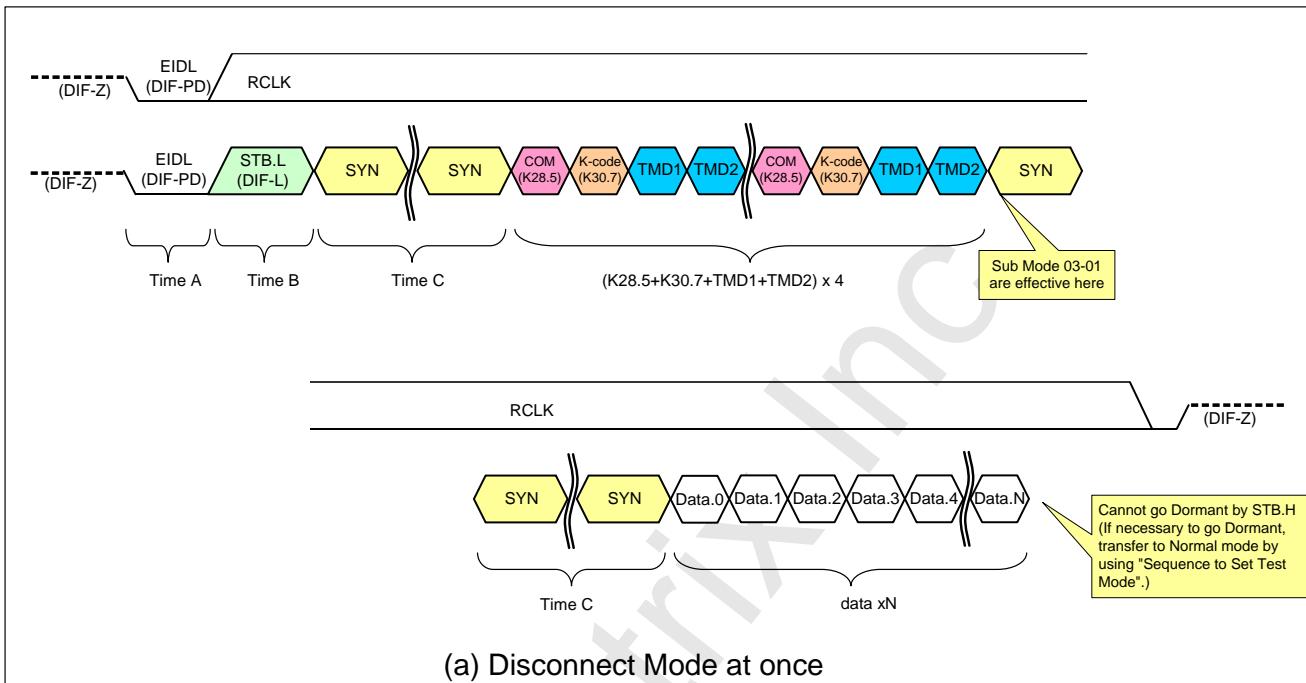


Figure 4-22: Disconnect Mode Sequence

#### 4.7.4 An Example Procedure

An example procedure for entering test mode is shown in Figure 4-23. This procedure is about Backward Loop Back test under the condition that PLL Multiplier is x30.

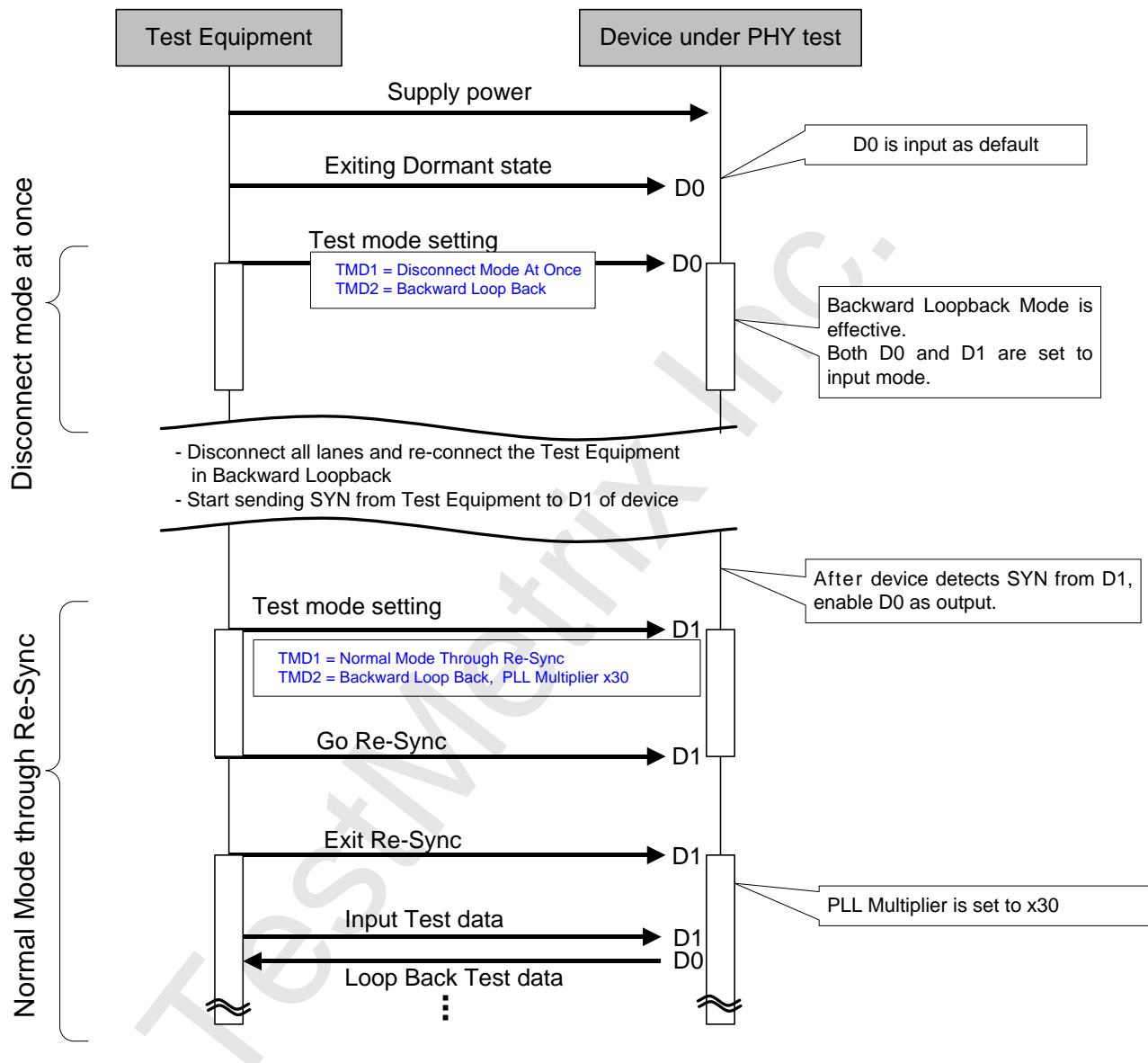
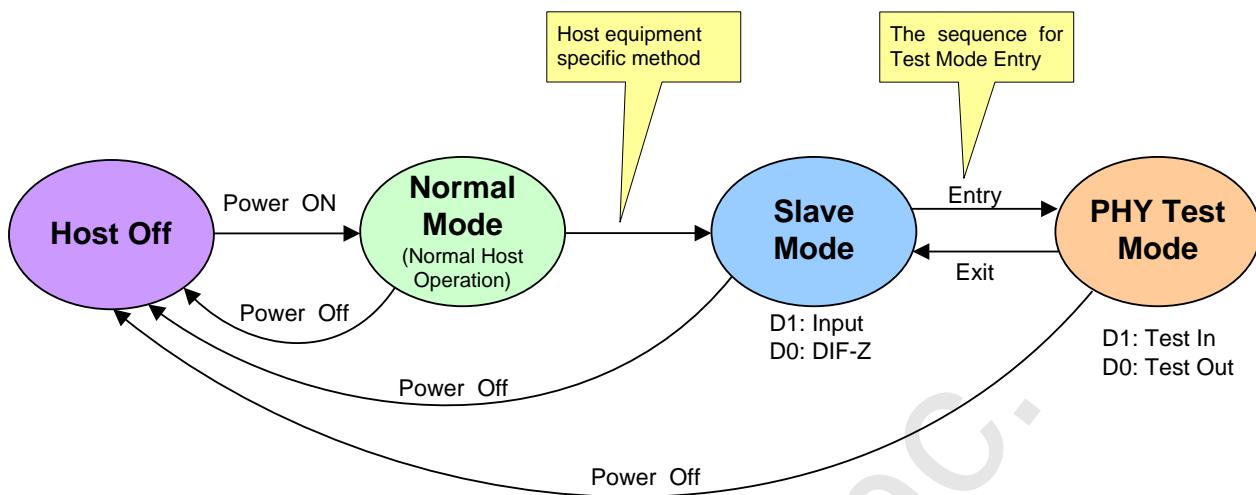


Figure 4-23: An Example Procedure (Backward Loop Back Test with PLL Multiplier is x30)

#### 4.7.5 Test Mode for Host

Host shall have "Slave Mode" and enter this mode for Host PHY test. The Slave Mode is correspondent to Dormant state of a Device. The method to enter the Slave Mode depends on Host implementation. Figure 4-24 shows the states regarding Host PHY Test.

**Figure 4-24: States Regarding Host PHY Test**

In Slave Mode,

- Host watches D1 Line to detect the sequence for Test Mode entry.
- Host continuously provides RCLK at any frequency selected by itself.
- Disable SSC when entering Slave Mode as a default.

When entering PHY test mode from Slave mode,

- PLL Multiplier may be changed by TMD2
- Backward Loop Back mode may be selected by TMD2
- SSC Enable may be changed by TMD2

When the Slave Mode and PHY Test Mode, test equipment may be connected to Host.

The following is recommended for Host:

- Disable all timeout detectors when the sequence for Test Mode entry is detected

#### **4.8 2L-HD Mode (Optional)**

Duplex mode switching (means from FD mode to 2L-HD mode, and vice versa) is controlled by LINK Layer. When a direction switching is instructed by LINK Layer, PHY shall complete the direction switch and notify the completion to LINK Layer within a defined time ( $T_{DIR\_SWITCH} = 8$  SI). Refer to Section 8.3.3 and Section 8.3.4 for more details.

#### **4.9 Additional Lanes Support (Optional)**

UHS-II may have additional Lanes in addition to D0 and D1 Lane. Refer to Chapter 9 for the details.

#### **4.10 Interface between PHY and LINK**

For the purpose of distributing PHY and Protocol IP separately, PHY-LINK I/F is defined as informative, so as to abstract the vendor-specific implementation of UHS-II PHY. Refer to Appendix F.

## 4.11 EMI

Many devices such as cellular phones, suffer from EMI problem. When designing Host and Device, it is important to intend to low EMI design. The EMI characteristic of UHS-II is improved compared to Legacy SD interface because of following features:

- **Differential signaling**
- **Low voltage swing**
- **Sending lower RCLK frequency compared to D0,D1 bit rate**

In addition to the above, the followings are recommended for further preventing EMI:

- **Minimizing intra skew**

Intra skew is the time difference between the single-ended mid-point of the  $V_{Dp}$  signal rising/falling edge, and the single-ended mid-point of the  $V_{Dn}$  signal falling/rising edge.

The more intra skew becomes, the more common mode voltage fluctuates. Intra skew has a direct impact on EMI. Wire length of two traces for each differential lane should be equivalent as much as possible.

- **Common-mode Impedance matching**

In differential signaling, it is important not only to keep differential impedance but also to keep common-mode impedance between transmission Line and termination for prevention of EMI.

- **Slow down the rise/fall time**

The rise/fall time also has a direct impact on EMI.

The frequency of RCLK is one tenth of bit rate of D0, D1, therefore it is recommended to slow down the rise/fall time of RCLK than that of D0, D1. Slowing down the rise/fall time is effective for realizing low EMI.

- **Tunable RCLK frequency range**

UHS II is providing the benefit to select the operating frequency. This feature allows keeping the EMI frequency outside the operating frequency of other sensitive system elements, like RF receivers.

- **Spread Spectrum Clocking (SSC)**

RCLK has a narrow frequency spectrum at the base frequency and its harmonics frequencies. Spread-spectrum clocking (SSC) is an effective method to reduce the spectral density of the EMI that the UHS II system is generating.

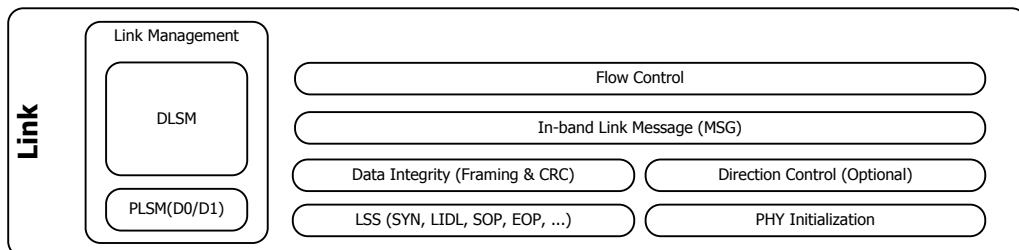
Using SSC is optional for the Host, but if used, it has to comply with the definitions at Appendix E.1.5

Device shall support receiving RCLK with SSC, but usually no special design for Device is needed.

## 5. Link Layer Specification

### 5.1 Link Layer Overview

Figure 5-1 shows the overview of Link Layer.



**Figure 5-1 : Link Layer Overview**

Link Layer is in charge of controlling data flow and making management for LINK and PHY. The key features of Link Layer are defined as follows.

- **PHY Initialization Control**
- **Data Integrity:** Packet framing with SOP and EOP, CRC generation and checking.
- **Flow Control:** Fixed window flow control only for Data packet transfer.
- **Direction Control:** Duplex mode switching between FD mode and 2L-HD mode (Optional).
- **Power Management (PM):**  
Lane level power saving state (EIDL: Electrical Idle)  
Link level power saving state (Dormant)
- **PHY and LINK error handling**
- **Packet Bypassing**

### 5.2 Link Layer Protocol

#### 5.2.1 Protocol Overview

Link Layer generates Link Symbol Set (LSS) to control PHY (synchronization, direction control, etc.), frames UHS-II packet (refer to Section 3.4.1 for more details) in terms of packet separation and data integrity. When Link accepts outgoing packets from upper layer (CM-TRAN), it generates CRC for each packet and the packet accompanied by its CRC is framed with SOP and EOP LSS. The framed UHS-II packets are transmitted through UHS-II bus via PHY. Each byte of original packet and CRC is encoded to 8b/10b Data symbol (D) in PHY. Refer to Chapter 4 for the 8b/10b encoding scheme.

#### 5.2.2 Link Symbol Set (LSS)

##### 5.2.2.1 Special Symbols

In 8b/10b encoding scheme, special symbols of 8b/10b K-symbol are defined and these are used for transmission control. Table 5-1 describes special symbols for Link Layer.

K-Symbol	Symbol name	Function	Original Byte		CurrentRD-	CurrentRD+
			Hex	HGF EDCBA	abcdei fghj	abcdei fghj
K28.0	SDB	Start of DATA Burst	1Ch	000 11100b	001111 0100	110000 1011
K28.1	SOP	Start of Packet	3Ch	001 11100b	001111 1001	110000 0110
K28.2	-	Reserved	5Ch	010 11100b	001111 0101	110000 1010
K28.3	LIDL	Logical Idle	7Ch	011 11100b	001111 0011	110000 1100
K28.4	-	Reserved	9Ch	100 11100b	001111 0010	110000 1101
K28.5	COM	Comma	BCh	101 11100b	001111 1010	110000 0101
K28.6	DIDL	Logical Idle during data transmission	DCh	110 11100b	001111 0110	110000 1001
K28.7	-	Reserved	FCh	111 11100b	001111 1000	110000 0111
K23.7	PAD	Padding	F7h	111 10111b	11010 1000	000101 0111
K27.7	EDB	End of DATA Burst	FBh	111 11011b	110110 1000	001001 0111
K29.7	EOP	End of Packet	FDh	111 11101b	101110 1000	010001 0111
K30.7	-	Reserved (See Note (1))	FEh	111 11110b	011110 1000	100001 0111

Note:

(1) K30.7 is used for PHY Test. Refer to Section0 and 4.7.3 for more details.

**Table 5-1 : Special Symbols for Link Layer**

### 5.2.2.2 Link Symbol Set

Table 5-2 describes a definition of LSS. The unit of Duration is the number of LSS. Valid reception denotes the minimum number of LSS to be regarded that LSS can receive properly. "DIR" is used for Direction Switch and refer to Chapter 8 for more details.

LSS		Function	Duration	Valid reception	
LSS Name	Symbol0				
SYN	COM (K28.5)	SYN0 (D31.5)	Synchronization for exiting from STB. See Note (1)	<ul style="list-style-type: none"> <li>Variable in Wakeup.Sync state</li> <li><math>N_{LSS\_SYN} * 4</math> in Active.Control state</li> </ul>	
		SYN1 (D26.2)			
BSYN		BSYN0 (D4.5)	Synchronization for exiting from STB and direction for Boot Code Loading. See Note (2)	<ul style="list-style-type: none"> <li>Variable in Wakeup.Sync state</li> </ul>	
		BSYN1 (D21.2)			
DIR		DIR (D31.2)	Direction Switch	<ul style="list-style-type: none"> <li><math>N_{LSS\_DIR} * 8</math> when FD mode to 2L-HD mode</li> <li>Variable when 2L-HD mode to FD mode</li> </ul>	
LIDL		LIDL0 (K28.3)	Logical Idle See Note (3)	N/A	
		LIDL1 (D16.7)			
DIDL		DIDL0 (K28.6)	Logical Idle during data transmission See Note (4)	N/A	
		DIDL1 (D12.2)			
SDB		SDB (K28.0)	Start of DATA Burst	2	
SOP		SOP (K28.1)	Start of Packet	1	
EOP		EOP (K29.7)	End of Packet	1	
EDB		EDB (K27.7)	End of DATA Burst	2	

Note:

- (1) It is required to select either SYN0 or SYN1 randomly when transmitting SYN LSS. Refer to Section 5.7.4 for more details.
- (2) It is required to select either BSYN0 or BSYN1 randomly when transmitting BSYN LSS. Refer to Section 5.7.4 and Section 5.9 for more details.
- (3) It is required to select either LIDL0 or LIDL1 randomly when transmitting LIDL LSS on Config state or Active.Control state. Refer to Section 5.7.4 for more details.
- (4) It is required to select either DIDL0 or DIDL1 randomly on Active.Trans or Active.Stream state. Refer to Section 5.7.4 for more details.

**Table 5-2 : Link Symbol Set**

For recovering from Lane standby (STB state), at least the predetermined number ( $N_{LSS\_SYN} * 4$ ) of SYN LSS shall be issued as follows (+/- denotes the running disparity). In Tx side of PHY, the initial disparity of the first transmitting "COM" is allowed to select either disparity.

- "COM-" → "SYN0 (D31.5)+" → "COM-" → "SYN1 (D26.2)+" → "COM+" → ...

In Rx side of PHY, symbol lock is established by "COM" reception at a Deserializer regardless of the next symbol of LSS. It is recommended that plural number of "COM" within a certain period of time in order to establish symbol lock because a single "COM" may be falsely generated by transmission error. In this way, repeatedly transmitted other LSSes, such as a series of LIDL, DIDL or DIR LSS, can also be used for symbol (re-)lock. Even if symbol lock is lost during transmission, it can be recovered by a

series of LSSes. Also, the running disparity of 8b/10b decoder is (re-)initialized to the disparity of "COM" used for symbol (re-)lock.

Note that "SYN0", "BSYN0", "LIDL0" and "DIDL0" keep the disparity of the following "COM" during a series of LSS transfer because these symbols are not DC balanced. On the other hand, "SYN1", "BSYN1", "LIDL1" and "DIDL1" always invert the disparity of "COM" because these symbols are DC balanced. To avoid a periodic pattern that causes EMI problem, these two types of symbols shall be randomly selected and transferred as a second symbol of LSS.

### 5.2.3 Header for UHS-II Packet

Figure 5-2 illustrates header structure for UHS-II packet that is compliant to UHS-II Addendum Version 1.00. First, Node ID whose range is from 0 to 15 denotes a value to identify the individual Hosts and Devices. Node ID = 0 is set aside for Host. For Devices, number 15 is set as the initial value for Node ID after I/F power cycle or FULL\_RESET, and one of numbers from 1 to 15 is assigned to each Device by Enumeration process described in Section 6.2.7. Note that Node ID of Boot Device is temporarily assigned for Boot Code Loading at first, then one of numbers from 1 to 15 is assigned by Enumeration (refer to Section 5.9).

Considering future extension, header format is allowed to be changed linked to LINK/TRAN Major Revision in CFG\_REG (refer to Table 6-9).

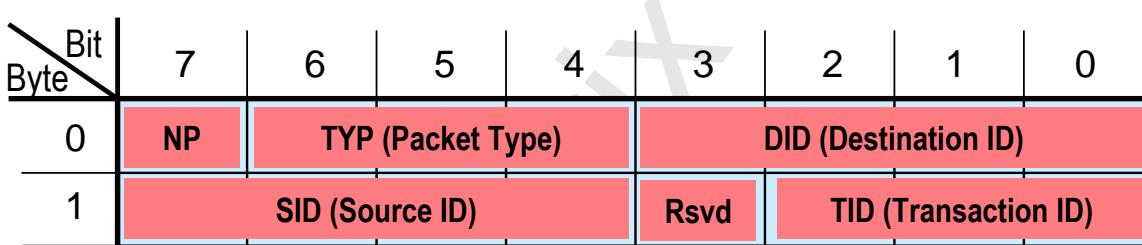


Figure 5-2 : Header Format

UHS-II Packet Header shall be composed of the following fields;

- **NP (Native Packet):** Indicator whether the packet follows native protocol or not
  - 0: not native protocol (application specific protocol)
  - 1: native protocol
  - NP field in MSG shall be set to '1'. (MSG packet transaction is defined on native protocol.)
- **TYP[2:0] (Packet Type):** Packet type described in Table 5-3.
- **DID[3:0] (Destination ID):** Node ID of destination Device or Host.
- **SID[3:0] (Source ID):** Node ID of source Device or Host.
- **TID[2:0] (Transaction ID):** Identification number of outstanding transactions
  - The TID field is defined in order to manage outstanding transactions for multiple command execution. (Details of multiple command execution will be defined in the future specification.)
  - Also refer to Section 6.2.14 for the setting of TID.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

TYP [2:0]	Packet Type	Description	Note
000b	CCMD	Control Command packet	TLP
001b	DCMD	Data Command packet	TLP
010b	RES	Response packet	TLP
011b	DATA	Data payload packet	TLP
111b	MSG	Message packet	Handled in LINK
Others	Reserved	Reserved	--

**Table 5-3 : Packet Type Encodings and Descriptions**

DID and SID are used as routing information. If SID = DID, the packet is handled as broadcast. For UHS-II Addendum Version 1.00, broadcast packet is applicable only for CCMD. Details of broadcast CCMD are described in Section 6.2.2.3.

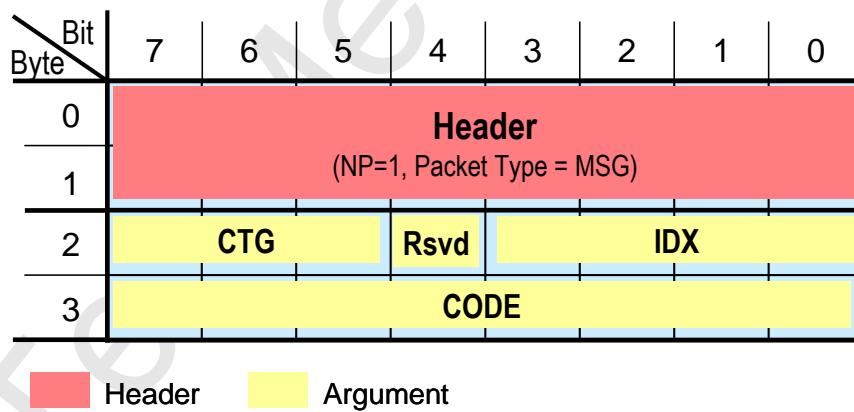
Basically, Host or Device processes a packet with the same DID as its own Node ID. In case of receiving a packet with different DID from own Node ID, Host or Device does not process it except broadcast packet and bypasses it to the next Host or Device on the bus. If Host or Device receives broadcast packet (SID = DID), it shall process even when DID is not equal to its own Node ID, and transmit to the next Host or Device.

## 5.2.4 Message Packet (MSG)

### 5.2.4.1 Overview

Message Packet (MSG) is introduced to realize flow control, error or interrupt handling instead of hard-wired signals.

Figure 5-3 illustrates a structure of MSG packet. Note that NP in Header shall be set to 1.

**Figure 5-3 : MSG Format**

- **CTG[2:0] (Message Category):** indicates category of MSG.
  - Refer to Table 5-4 for more details.
- **IDX[3:0] (Message Index):** indicates message Index related to CTG. Refer to Table 5-4 for more details.
- **CODE[7:0] (Message Code):** indicates code to define message detail.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

CTG		IDX		CODE	Description
Bits	Name	Bits	Name		
000b	LMSG (See Note (1))	0000b	FCREQ	Refer to Table 5-5	Flow Control Request from initiator of DATA
		0001b	FCRDY	Refer to Table 5-5	Flow Control Ready from receiver of DATA
		0010b	STAT	Refer to Table 5-6	Status of DATA Burst transfer notified from receiver of DATA
		others	Reserved	Reserved	Reserved
011b	INT	all	Reserved	Reserved	Reserved for interrupt
100b	AMSG	See Note (2)			Application specific message. It depends on application defined in CFG_REG.
Others	Reserved	all	Reserved	Reserved	Reserved

Note:

(1) LMSG is handled within LINK.

(2) In case of SD application, refer to Section 7.2.6.1.

**Table 5-4 : Detailed Definition of MSG**

Also refer to Section 6.2.2.8 for operating reserved bits in the packet.

#### 5.2.4.2 CODE Definition for Each IDX

Table 5-5 describes the CODE definition of FCREQ and FCRDY.

Bits	Identifier	Value	Description
7	UNRECOVERABLE_ERROR	'0' = no error '1' = error	Error occurs that it cannot be recovered by DATA Burst Retry.
6:0	Reserved	Reserved	Reserved

**Table 5-5 : Code Definition of FCREQ and FCRDY**

If Host receives an FCREQ, FCRDY or STAT MSG with UNRECOVERABLE\_ERROR = 1, it needs to abort the data transaction by issuing TRANS\_ABORT CCMD or encapsulated CMD12 (in case of SD-TRAN). This bit is not cleared until the transaction is aborted or completed. And once this bit is set, the transaction cannot be completed successfully.

Table 5-6 describes the CODE definition of STAT. Refer to Section 5.2.6 for framing rules or CRC.

Bits	Identifier	Value	Description
7	UNRECOVERABLE_ERROR	'0' = no error '1' = error	Error occurs that it cannot be recovered by DATA Burst Retry.
6:1	Reserved	Reserved	Reserved
0	RECOVERABLE_ERROR	'0' = no error '1' = error	Error occurs that it can be recovered by DATA Burst Retry. This bit is set as a request for DATA Burst Retry.

**Table 5-6 : Code Definition of STAT**

UHS-II has two types of error identifiers, one is UNRECOVERABLE\_ERROR and the other is RECOVERABLE\_ERROR. Refer to Section 5.2.5 for more details.

If LINK of DATA initiator side receives a STAT MSG with RECOVERABLE\_ERROR = 1 and UNRECOVERABLE\_ERROR = 0 just after a DATA Burst transmission, it needs to start performing DATA Burst Retry. Note that RECOVERABLE\_ERROR in STAT MSG represents status of preceding DATA Burst. Details of DATA Burst Retry are described in Section 5.5.4.

### 5.2.4.3 MSG Duplication

For the purpose of getting transaction robustness, the MSG initiator shall send the same MSG packets twice for one message transmission. There are no gaps between the duplicated MSG packets.

Receiver shall recognize the MSG reception successful if at least one of MSG packets is recognized as a valid MSG. In other word, if the receiver detects the first MSG packet as a valid MSG, it can ignore the second one. Else if it fails the first MSG but succeeds to get the second one, it shall be considered as a valid MSG reception. Otherwise, it is recognized as MSG reception error.

From now on, "MSG" means the duplicated MSG packets if not otherwise specified.

### 5.2.5 Error Identifier

Details of error identifiers in UHS-II are as follows.

- **UNRECOVERABLE\_ERROR:** includes ILLEGAL\_HEADER\_ERROR, DEVICE\_SPECIFIC\_ERROR and RETRY\_EXPIRE\_ERROR as follows.
  - **ILLEGAL\_HEADER\_ERROR:** indicates error detection in UHS-II Header on the condition of no CRC errors. Details of ILLEGAL\_HEADER\_ERROR conditions are described in Section 5.8.
  - **DEVICE\_SPECIFIC\_ERROR:** is defined as a general error occurred in outside of UHS-II interface. For example, memory write error is treated as a DEVICE\_SPECIFIC\_ERROR. That kind of error is indicated from outside of UHS-II (backend, for example) in receiver side internally.
  - **RETRY\_EXPIRE\_ERROR:** indicates the retry counter reaches to its own "MAX\_RETRY\_NUM". Details of RETRY\_EXPIRE\_ERROR conditions are described in Section 5.5.4.
- **RECOVERABLE\_ERROR:** includes FRAME\_ERROR and CRC\_ERROR as follows.
  - **FRAME\_ERROR:** indicates detection of framing error. In other words, a control packet or DATA Burst violates the framing rules described in Section 5.2.6. Details of FRAME\_ERROR conditions are described in Section 5.8.
  - **CRC\_ERROR:** indicates that CRC error is detected from a control packet or at least one of Framed DATA packet in the previous DATA Burst. Details of CRC\_ERROR conditions are described in Section 5.8.

Basically these error identifiers are indicated in Status Register (ST\_REG) described in Section 6.2.10. Moreover, when Device detects these errors during DATA Burst transmission, it should notify them to Host by STAT, FCREQ, or FCRDY MSG. Host can detect such errors by those MSGs or timeout.

### 5.2.6 Framing Rules

In this section, framing rules are described.

#### 5.2.6.1 Packet Framing

Figure 5-4 illustrates a packet framing rule of TLPs (TLP is described in 6.1.1). First, the TLP provided by CM-TRAN is supplied to CRC calculator and added the 16 bits CRC to its end. Second, the TLP with CRC is prefixed by SOP (Start of Packet) and postfixed by EOP (End of Packet) as its delimiters. Note that the target of CRC calculation is the original packet data only and it does not include SOP and EOP. Note that CRC is transmitted MSB (Most Significant Byte) first and LSB (Least Significant Byte) last. Detailed CRC specification is described in Section 5.7.

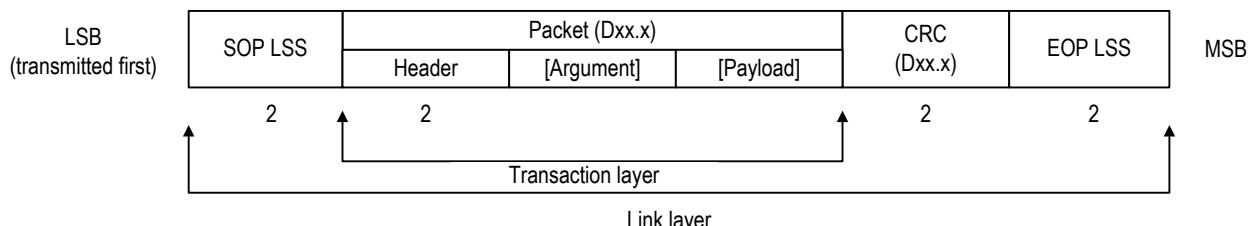
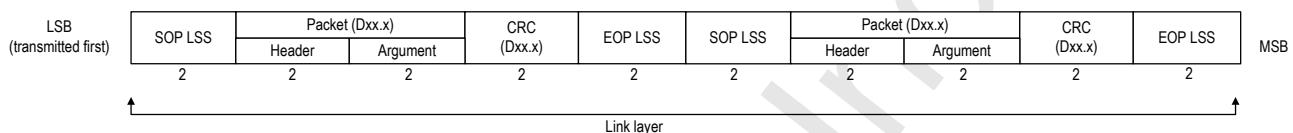
**UHS-II Addendum Version 1.02****Figure 5-4 : Packet Framing Rule of TLP**

Figure 5-5 illustrates a packet framing rule of MSG. The framing rule is same as that of TLP, but note that MSG is generated by LINK, and the MSG initiator shall duplicate MSG packets as illustrated in Figure 5-5.

**Figure 5-5 : Packet Framing Rule of MSG**

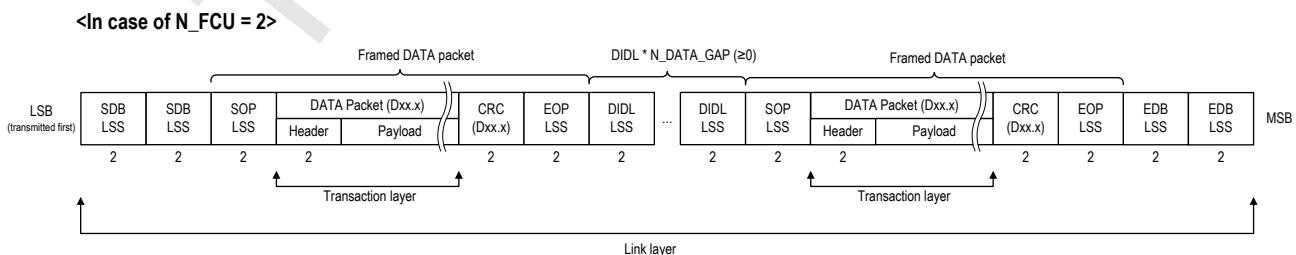
Packet deframing is basically the inverse operation of framing. Also refer to Section 5.8 for packet deframing.

**5.2.6.2 DATA Burst Framing**

Each data transfer performed by DCMD is split into some DATA Bursts, and the DATA Burst is a basis of performing flow control. The number of DATA to be bundled in DATA Burst is less than or equal to flow control unit window size ( $N\_FCU$ ) defined in Configuration Register (CFG\_REG). DATA Burst deframing is basically the inverse operation of framing.

**5.2.6.2.1 DATA Burst Framing Rule in Block Mode**

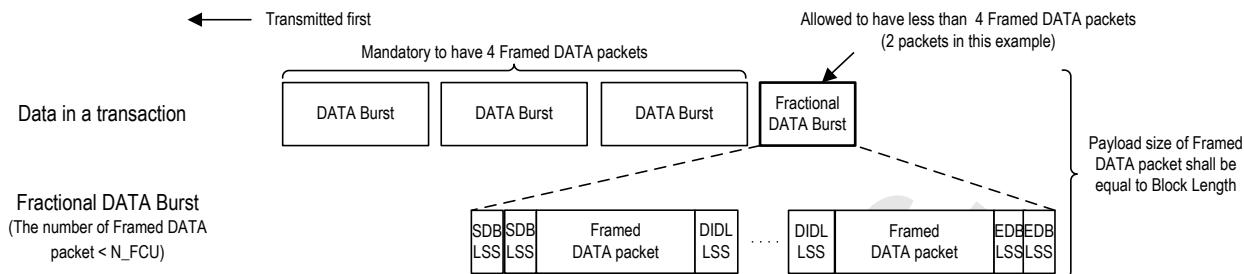
Figure 5-6 illustrates a DATA Burst framing rules in Block Mode (in case of  $N\_FCU = 2$ ). A Framed DATA packet is generated by the Packet Framing rules described in Section 5.2.6.1. The DATA Burst shall have  $N\_FCU$  Framed DATA packets. The gaps between one Framed DATA packet and another are filled with at least  $N\_DATA\_GAP$  (more than or equal to zero) of Data Idle symbol set (DIDL), and DATA Burst is generated as a result. The DATA Burst is framed again with symbol set named SDB (Start of DATA Burst) and EDB (End of DATA Burst). In other words, two SDB LSSes appear at the top of the DATA Burst, and two EDB LSSes do at the bottom.

**Figure 5-6 : DATA Burst Framing Rule in Block Mode (N\_FCU = 2)**

If TLEN is not divisible by  $N\_FCU$ , fractional DATA Burst, which consists of Framed DATA packet less than  $N\_FCU$ , can be transmitted only as a final part of data transaction, as illustrated in Figure 5-7. Note that the fractional DATA Burst is not allowed if TLEN is not specified in DCMD, except when the data

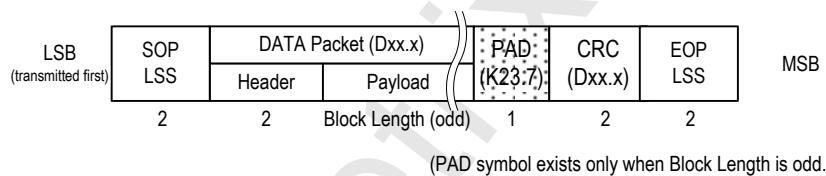
transfer length is determined by another means for the DCMD (for example, secure multi-block read / write command such as ACMD18 or ACMD25). In this exception, CMD12 is not required even in case of LM=0.

<In case of TLEN = 14, N\_FCU = 4>



**Figure 5-7 : Framing Rules for Fractional DATA Burst**

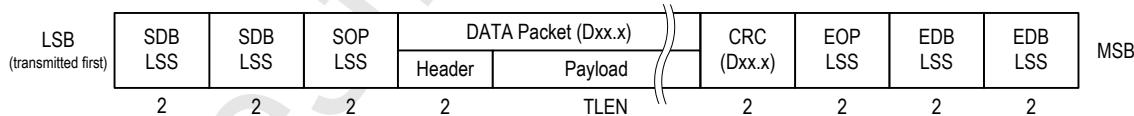
The payload length for all DATA Packets shall be equal to Block Length in Block Mode. If Block Length is odd, the DATA initiator shall insert one PAD (K23.7) at the end of each DATA Packet in order to make the length of Framed DATA Packet even bytes.



**Figure 5-8 : Framed DATA Packet Format in Case of Block Length Is Odd**

### 5.2.6.2.2 DATA Burst Framing Rule in Byte Mode

Figure 5-9 illustrates a DATA Burst Framing rule in Byte Mode.

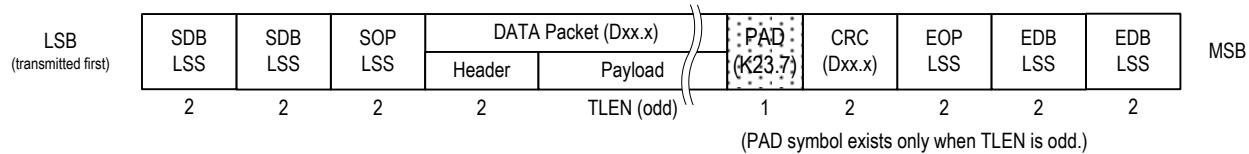


**Figure 5-9 : DATA Burst Framing Rule in Byte Mode**

Note that the following rules shall be kept in of Byte Mode.

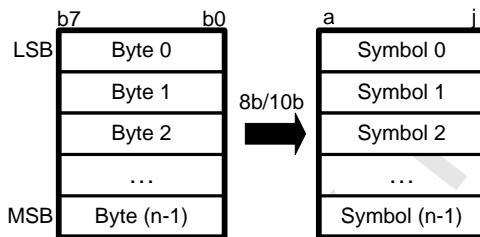
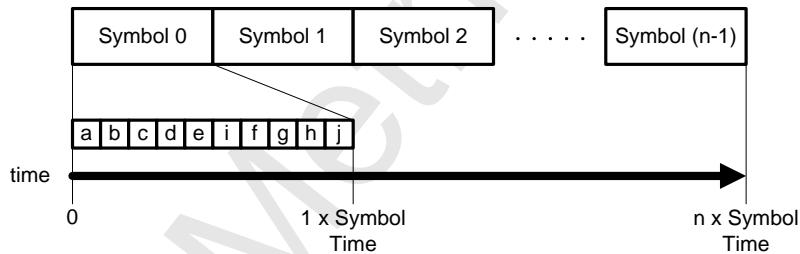
- TLEN shall be specified in DCMD.
- TLEN shall be smaller than or equal to Block Length.
- A DATA Burst shall have only one Framed DATA Packet.

Moreover, if TLEN is odd, the DATA initiator shall insert one PAD (K23.7) at the end of DATA Packet in order to make the length of Framed DATA Packet even bytes.

**Figure 5-10 : DATA Burst Framing Rule in Byte Mode When TLEN Is Odd**

### 5.2.7 Symbol Encoding and Byte Ordering in 8b/10b

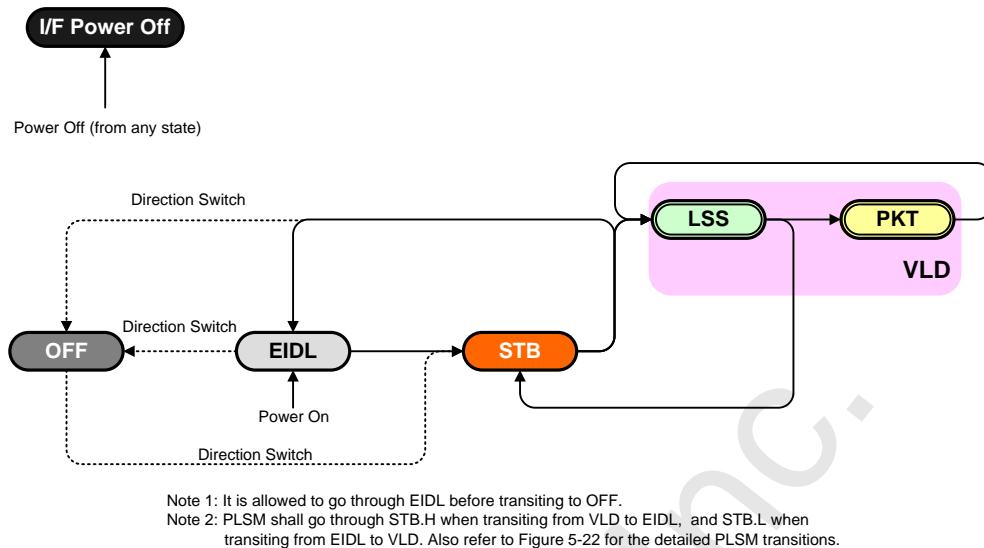
Each byte of framed packet (TLP or MSG) and LSS is encoded to corresponding symbol with 8b/10b as Figure 5-11. These symbols are transferred over each Lane from LSB (Least Significant Byte) to MSB (Most Significant Byte) as Figure 5-12.

**Figure 5-11 : Symbol Encoding****Figure 5-12 : Byte Ordering in Symbol Transfer**

### 5.2.8 Physical Lane State Machine (PLSM)

#### 5.2.8.1 Overview

Physical Lane State Machine (PLSM) denotes transmitting / receiving status for each data Lane. Figure 5-13 shows a top level state diagram of PLSM. PLSM is defined for both Tx and Rx of each data Lane and those are synchronously managed between Host and Device. For example, when D0.Tx of Host transits to EIDL, D0.Rx of Device shall also transit to EIDL soon afterward.

**Figure 5-13 : Physical Lane State Machine (PLSM)**

- **I/F Power Off state:** State indicating that I/F power supply (e.g. VDD2 in SD Memory) is off. Both Tx and Rx transit to this state from any state only when I/F power supply is off.
- **OFF state:** State indicating Tx or Rx is disabled. Both Tx and Rx transit to this state when direction switch occurs. In this state, both Tx driver and Rx termination resistor of a Lane are turned off. So, the Line between them becomes high impedance and floating state (DIF-Z).
- **EIDL state:** Electrical-Idle state with DIF-PD (pull-down) as a Lane level power saving state. In this state, the Lane state is kept to DIF-PD.
- **STB state:** Lane standby state with DIF-L (STB.L) or DIF-H (STB.H) required for transition from or to EIDL state. STB.L and STB.H are used as a prefix and postfix of a group of valid symbols respectively (refer to Section 5.4.2 for more details). Physically, Tx side keeps sending DIF-L during STB.L and DIF-H during STB.H, respectively. Rx side can receive (sample) serial data as a series of bit clocked data symbol at Deserializer after its PLL is locked. During wakeup from Dormant state, Rx side can transit from EIDL to STB.L when Amplitude Detector on Rx detects the amplitude difference between DIF-PD and DIF-L.
- **VLD state:** State for valid 8b/10b symbols including LSS sub-state and PKT sub-state (refer to Section 5.2.8.2 for more details).
  - **LSS sub-state:** State for Link layer symbol set including multiple symbol states.
  - **PKT sub-state:** State for packet including multiple symbol states.

Table 5-7 shows a PLSM state definition and the corresponding Tx and Rx status of PHY.

PLSM in Link	Line state in PHY	Tx Status		Rx Status					
		Diff. Driver	8b/10b Encode	Amp. Detector	Term. Resistor	Diff. Receiver	Symbol Lock	8b/10b Decode	
OFF	DIF-Z	Off	Not used	Not used (Masked)	Off	Off	Not locked	Not used	
EIDL	DIF-PD	-- (See Note (1))	Not used	Used (Unmasked) (See Note (2))	On	Off	Not locked	Not used	
STB	DIF-L or DIF-H	On	Not used	Not used (Masked)	On	On	Not locked (See Note (3))	Invalid Symbol	
VLD (LSS or PKT)	DIF-L or DIF-H	On	Valid Symbol	Not used (Masked)	On	On	Locked	Valid Symbol	

Note:

- (1) Both the plus and minus Lines of the Differential Lane shall be pulled down (low impedance drive to ground). It is implementation issue whether this feature is implemented utilizing the Differential driver itself or by additional circuitry.
- (2) When Amplitude Detector detects amplitude difference, PLSM transits to STB.
- (3) STB may be received even after symbol is locked. Symbol lock is lost when receiving STB continuously.

**Table 5-7 : PLSM State Definition for Tx and Rx**

### 5.2.8.2 Details of VLD State

Figure 5-14 shows a symbol state diagram for VLD state including LSS and PKT sub-state. The underlined characters in PLSM denote symbol states. Also refer to Table 5-1 and Table 5-2 for the corresponding K-symbols and D-symbols for each LSS and PAD symbol.

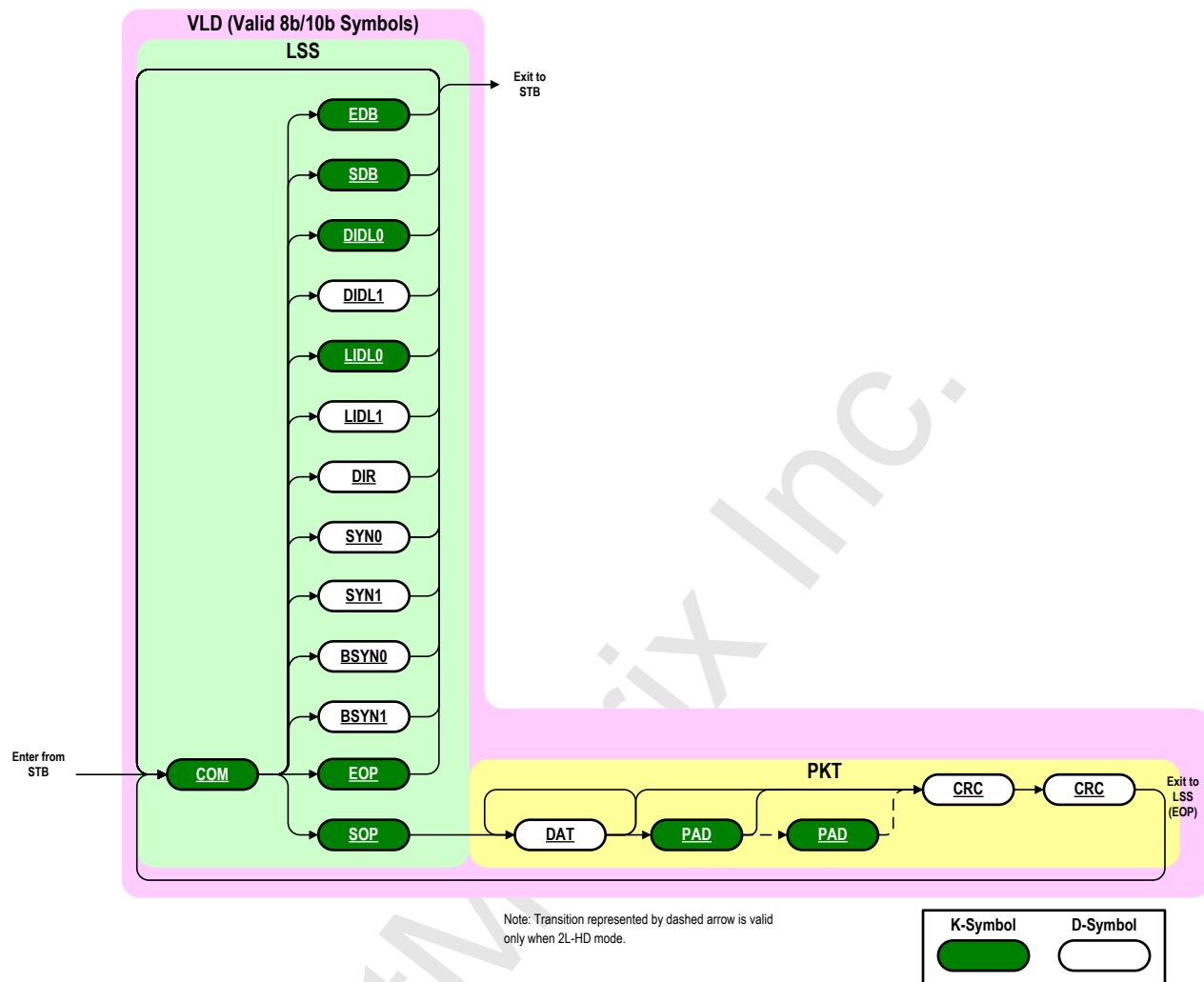


Figure 5-14 : VLD State

When entering to VLD state from STB state, PLSM shall transit to LSS sub-state and start to acquire symbol lock by transferring SYN (or DIR) LSS.

PKT sub-state requires SOP LSS at its entry and EOP LSS at its exit. DAT symbol state stands for a data symbols, and repeats predetermined number of times to construct a UHS-II packet. PAD symbol state stands for a PAD symbol. Rules of inserting PAD are described in Section 5.2.6.2 for FD mode, in Section 8.3.1 for 2L-HD mode. CRC symbol state stands for its CRC symbol. CRC is calculated for the padded packet including a series of DAT, and PAD before 8b/10b encoding, and placed just after the padded packet as described in Section 5.2.6. When exiting from VLD state, PLSM shall transit from LSS to STB again.

In addition to the transition above, Transmitter shall keep the following rules.

- State transitions related to SDB, EDB and DIDL comply with DATA Burst framing rule described in Figure 5-6.
- State transitions related to SOP and EOP comply with packet and DATA Burst framing rules described in Figure 5-4 through Figure 5-6.
- The number of repetition for SYN is regulated by "N\_LSS\_SYN" in CFG\_REG after Configuration completes.

### 5.2.8.3 In Case of 8b/10b Error

8b/10b error includes decoded error and disparity error. 8b/10b decoded error indicates that received symbol does not comply with 8b/10b decode valid 10-bit code word. And 8b/10b disparity error indicates that received symbol has unexpected disparity compared with the current disparity. Note that all 8b/10b error symbols except for all-zero symbol (STB.L) and all-one symbol (STB.H) are notified to LINK as PHY Receive Error.

If Rx side of PHY continuously detects an implementation specific period of 8b/10b error, symbol lock shall be regained as soon as possible. And also, once Rx side of PHY transits to EIDL, its symbol lock is lost and supposed to be regained by receiving plural "COM" during a series of SYN LSS. Note that the actual timing to lose symbol lock is implementation specific and beyond the scope of this specification.

When LINK detects PHY Receive Error during PKT state, it may be CRC\_ERROR. And if LINK detects PHY Receive Error related to Framing Rule violation, it may be FRAME\_ERROR. Otherwise, during LIDL period of packet gap for instance, LINK may handle PHY Receive Error as PHY internal error. Here is an example of LINK implementation related to handling PHY Receive Error.

- When PHY Receive Error = 0, LINK treats data from PHY is correct and checks Framing rule and CRC.
- When PHY Receive Error = 1 and LINK detects LIDL, LINK ignores PHY Receive Error.
- When PHY Receive Error = 1 and LINK detects Framing rule violation, LINK indicates it as FRAME\_ERROR.
- When PHY Receive Error = 1 between SOP and EOP, LINK indicates it as CRC\_ERROR without CRC check.

## 5.2.9 Data Link State Machine (DLSM)

### 5.2.9.1 Overview

Data Link State Machine (DLSM) is responsible for LINK Management such as LINK synchronization, direction control, PM and so on. Figure 5-15 shows a state diagram of DLSM.

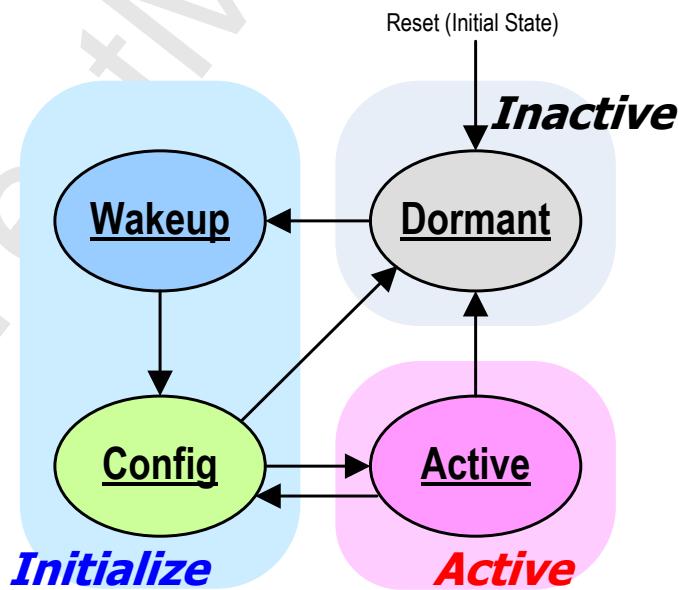


Figure 5-15 : Data Link State Machine (DLSM)

- **Dormant:** Link level power saving state. All Lanes are EIDL and PLL can be powered off.

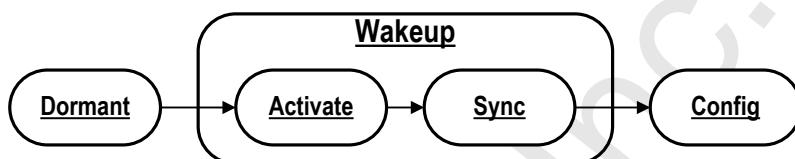
- **Wakeup:** PHY initialization state with two sub-states (refer to Section 5.2.9.3).
- **Config:** Device configuration state in which Device is initialized, enumerated and functions are configured to be available at Active state.
- **Active:** Normal operation state with four sub-states (refer to Section 5.2.9.5).

### 5.2.9.2 Dormant State

Dormant state realizes power saving. Refer to Section 5.4 for more details.

### 5.2.9.3 Wakeup State

Wakeup state includes the following two sub-states described in Figure 5-16.



**Figure 5-16 : Wakeup State**

- **Wakeup.Activate:** UHS-II Interface wakeup request and PLL activation
- **Wakeup.Sync:** LINK synchronization. All of the data Lanes are in the process of symbol locking.

Table 5-8 shows a condition of state transition related to Wakeup state.

State Transition		Transition Condition; Action	
Current State	Next State		
Dormant	Wakeup.Activate	Host	Start initializing UHS-II interface; Sending STB.L for a wakeup request.
		Device	Detecting STB.L from Host; Sending STB.L for a wakeup acknowledgement.
Wakeup.Activate	Wakeup.Sync	Host	Detecting STB.L; Starting to send SYN or BSYN LSS. (See Note (1).)
		Device	Detecting SYN or BSYN LSS from Host; Starting to send SYN or BSYN LSS. (See Note (2).)
Wakeup.Sync	Config	Host	Detecting SYN or BSYN LSS from Device; Starting to send LIDL LSS.
		Device	Detecting LIDL LSS from Host; Starting to send LIDL LSS.

Note:

- (1) Host transmits BSYN LSS if it requires loading Boot Code from Boot Device, and SYN LSS otherwise. The selection of SYN or BSYN is alternative during wakeup. Refer to Section 5.2.2.2 and 5.9 for more details.
- (2) When Device receives SYN LSS, it also sends SYN LSS from its Tx. Likewise, when Device receives BSYN LSS, it also sends BSYN LSS.

**Table 5-8 : Condition of State Transition (Wakeup)**

### 5.2.9.4 Config State

Config state is a state for preparation of transitioning to Active state. At least Device Initialization, Enumeration and Configuration take place in Config state by CCMD. Note that Host shall issue

commands after receiving LIDL from Device when transitioning from Wakeup.Sync.

Basically, state transits to Active.Control state when "Config Completion" flag in CFG\_REG is successful to set to 1.

If the flag is already set to 1 at the entry of Config state, the transition takes place after receiving EIDL or LIDL. This situation occurs when receiving BSYN LSS at PHY Initialization (refer to Section 5.9) or recovering from Dormant state.

Table 5-9 shows a condition of state transition from Config state.

State Transition		Transition Condition	
Current State	Next State		
Config	Active.Control	If "Config Completion" flag is equal to 0, the value of the flag becomes to 1, and EIDL or LIDL is received. In this case, Device shall transit to Active.Control before transmitting the broadcast CCMD or RES of P2P CCMD for setting the flag to 1. Otherwise, EIDL or LIDL is received.	
Config	Dormant	Host	Directing PHY to transit to Dormant state after the conditions are satisfied described in Section 5.4.3. As a result, RCLK may be stopped.
		Device	Directing PHY to transit to Dormant state after the conditions are satisfied described in Section 5.4.3.

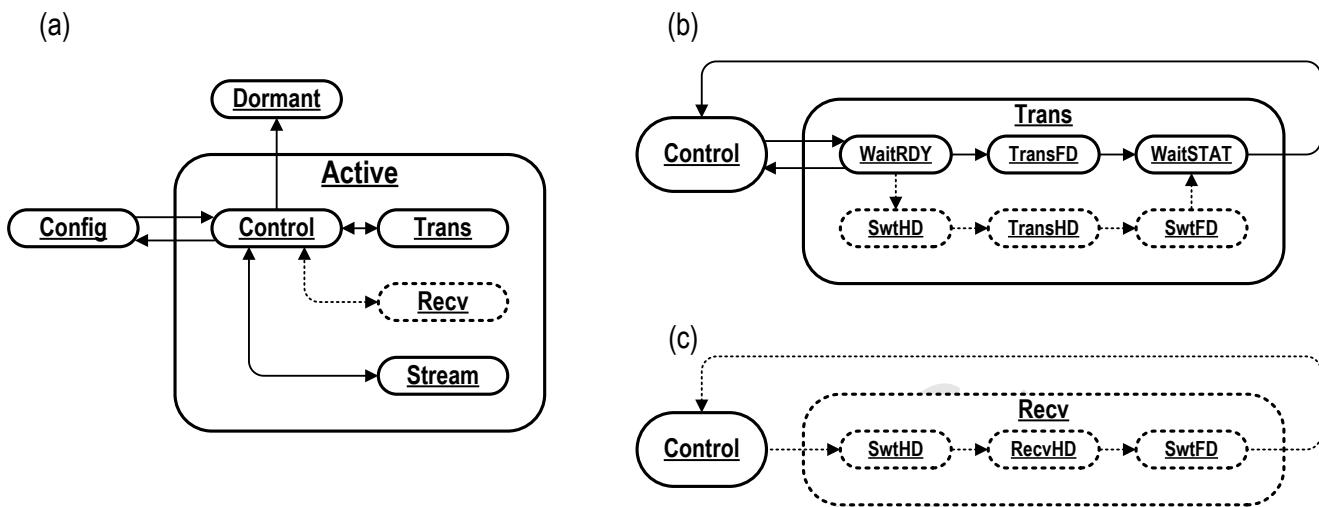
**Table 5-9 : Condition of State Transition (Config)**

**Application Note:**

In case of Ring Connection, Host shall use broadcast write CCMD to set "Config Completion" flag to 1.

### 5.2.9.5 Active State

Active state includes the following four sub-states described in Figure 5-17 (a). This state is basically used for regulating the packet transmission. Packet reception in FD mode is done on Active.Control state and that in 2L-HD mode on Active.Recv state, So, transition to Active.Recv state takes place in case of DATA Burst reception in 2L-HD mode.



Note:

- (1) Dashed line denotes transition or state relevant to the optional 2L-HD mode.
- (2) When LINK transmits or receives MSG with UNRECOVERABLE\_ERROR, it shall transit its DLSM to Active.Control state.

**Figure 5-17 : Active State**

- **Active.Control:** State for transmitting control packets or control LSSes and receiving any packets in FD mode.
- **Active.Trans:** State for transmitting DATA Burst in both FD mode and 2L-HD mode (refer to Figure 5-17 (b) for more details). Note that LINK shall not transmit control packets during Active.Trans.TranFD and Active.Trans.TranHD.
- **Active.Recv:** State for receiving DATA Burst in 2L-HD mode and associated direction switch (refer to Figure 5-17 (c) for more details). This state is optional because it is only for DATA Burst reception in 2L-HD mode. Note that any packets cannot be transmitted in this state because all data Lanes are occupied for DATA Burst reception or direction switch.
- **Active.Stream:** State for DATA Burst Streaming described in Section 5.6.

Any MSG can be transmitted in Active.Control state, but the transmitting rule of each MSG depends on other LINK specification such as Flow Control (refer to Section 5.5) or application. Moreover, any packets with NP = 0 can be transmitted only in Active state.

Conditions of state transition related to Active state are described from Table 5-10 to Table 5-12.

State Transition in Active state		Transition Condition; Action	
Current State	Next State		
Active.Control	Active.Trans (Trans.WaitRDY)	FCREQ is transmitted.	
	Active.Recv (Recv.SwtHD)	FCRDY corresponding to DCMD whose DM = 1 is transmitted.	
	Active.Stream	FCREQ is bypassed; LINK instructs the PHY to enable Loopback path.	
	Dormant	Host	Directing PHY to transit to Dormant state after the conditions are satisfied described in Section 5.4.3. As a result, RCLK may be stopped.
		Device	Directing PHY to transit to Dormant state after the conditions are satisfied described in Section 5.4.3.
	Config	The first operation of setting "Config Completion" to 0 after Wakeup synchronized by BSYN. (See Note (1))	
Active.Trans (Trans.WaitSTAT)	Active.Control	STAT MSG or TRANS_ABORT is received.	
Active.Trans (Trans.WaitRDY)	Active.Control	TRANS_ABORT is accepted. (See Note (2))	
Active.Recv (Recv.SwtFD)	Active.Control	DIDL LSS is received via unswitched Lane after DIR LSS exchange.	
Active.Stream	Active.Control	LIDL or EIDL is received after disabling Loopback path.	

Note:

- (1) This transition only takes place after finishing Boot Code Loading. Refer to Section 5.9.
- (2) If SD-TRAN is implemented, this transition also takes place in case that CMD12 is accepted.

**Table 5-10 : Condition of State Transition from Active State**

State Transition in Trans sub state		Transition Condition; Action
Current State	Next State	
Trans.WaitRDY	Trans.TransFD	FCRDY corresponding to DCMD whose DM = 0 is received.
	Trans.SwtHD	FCRDY corresponding to DCMD whose DM = 1 is received.
Trans.TransFD	Trans.WaitSTAT	EDB LSS of a DATA Burst is transmitted; starting to send DIDL LSS.
Trans.SwtHD	Trans.TransHD	After sending STB.L for T_EIDL_RECOVERY via switched Lane; Starting to send at least N_LSS_DIR * 8 of DIR LSS for each Lane.
Trans.TransHD	Trans.SwtFD	EDB LSS of a DATA Burst is transmitted through all data Lanes; Starting to send DIR LSS via unswitched Lane.
Trans.SwtFD	Trans.WaitSTAT	DIR LSS is received via switched Lane; Starting to send DIDL LSS same as in FD mode.

**Table 5-11 : Condition of State Transition within Active.Trans State**

State Transition in Recv sub state		Transition Condition
Current State	Next State	
Recv.SwtHD	Recv.RecvHD	DIR LSS is received via all data Lanes.
Recv.RecvHD	Recv.SwtFD	EDB LSS of a DATA Burst is received.

Table 5-12 : Condition of State Transition within Active.Recv State

## 5.3 PHY Initialization

In this section, PHY Initialization with no Boot Code Loading is described. Refer to Section 5.9 for that with Boot Code Loading.

### 5.3.1 PHY Initialization Sequence

Figure 5-18 illustrates a PHY initialization sequence. Initial state of DLSM is Dormant in which almost all of PHY circuits are powered off.

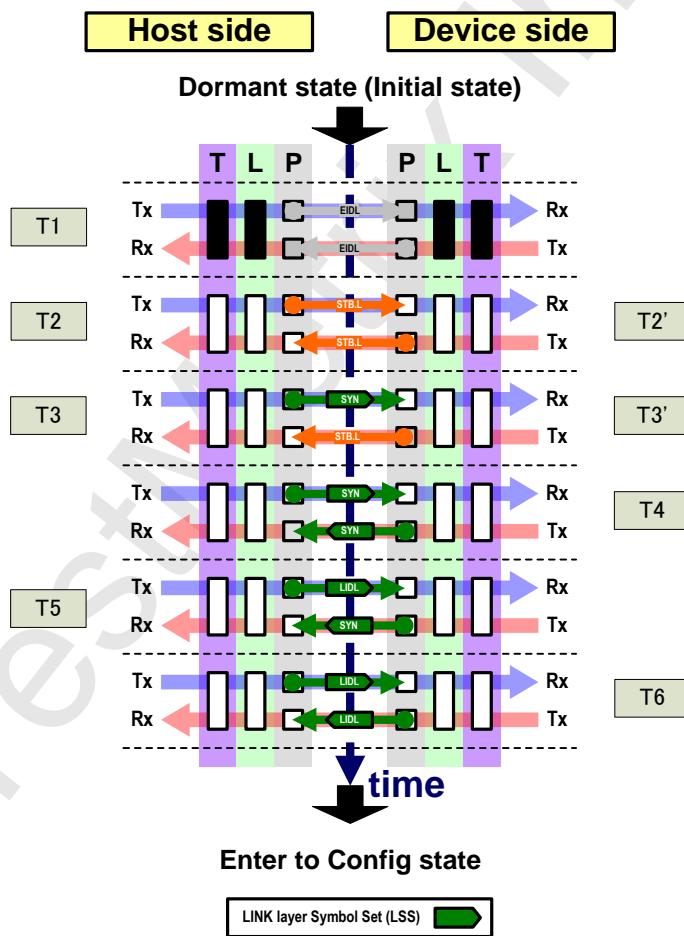


Figure 5-18 : PHY Initialization Sequence

T1: In Dormant state, both Lanes are EIDL state (Electrical Idle state with DIF-PD: pull-down).

T2: For initializing PHY, LINK of Host starts to provide RCLK, drives Tx to STB.L (Lane Standby with DIF-L) to poll the existence of UHS-II Device. After that, DLSM of Host transits to Wakeup.Activate state.

T2': After receiving RCLK and STB.L, LINK of Device also enters to Wakeup.Activate and responds by

driving Tx to STB.L and PHY of Device starts to acquire PLL lock.

T3: After Host receives STB.L, LINK of Host starts to send SYN LSS immediately for LINK synchronization, and its state transits to Wakeup.Sync.

T3': Device completes its PLL lock.

T4: If Device successfully receives SYN LSS after PLL lock, LINK of Device also starts to send SYN LSS and its state transits to Wakeup.Sync.

T5: After receiving SYN LSS from Device, LINK of Host starts to send LIDL and its state transits to Config.

T6: After receiving LIDL LSS from Host, LINK of Device starts to send LIDL and its state transits to Config.

Note that PHY speed range setting performed by "Selected Transmission Speed Range" in CFG\_REG shall be reflected to PHY before starting PLL. Both sides of LINK can set the PHY speed range during a short period just after starting RCLK in Dormant state.

### 5.3.2 LINK State Transition during PHY Initialization (Point to Point)

Figure 5-19 illustrates a LINK state transition during PHY Initialization for Point to Point Connection. Descriptions of timing such as T1 in Figure 5-19 are same as described in Section 5.3.1. Also refer to Section 6.3.1 for the detailed definition of timing parameters such as Teidl\_stb, Tactivate or Tlidl\_lidl.

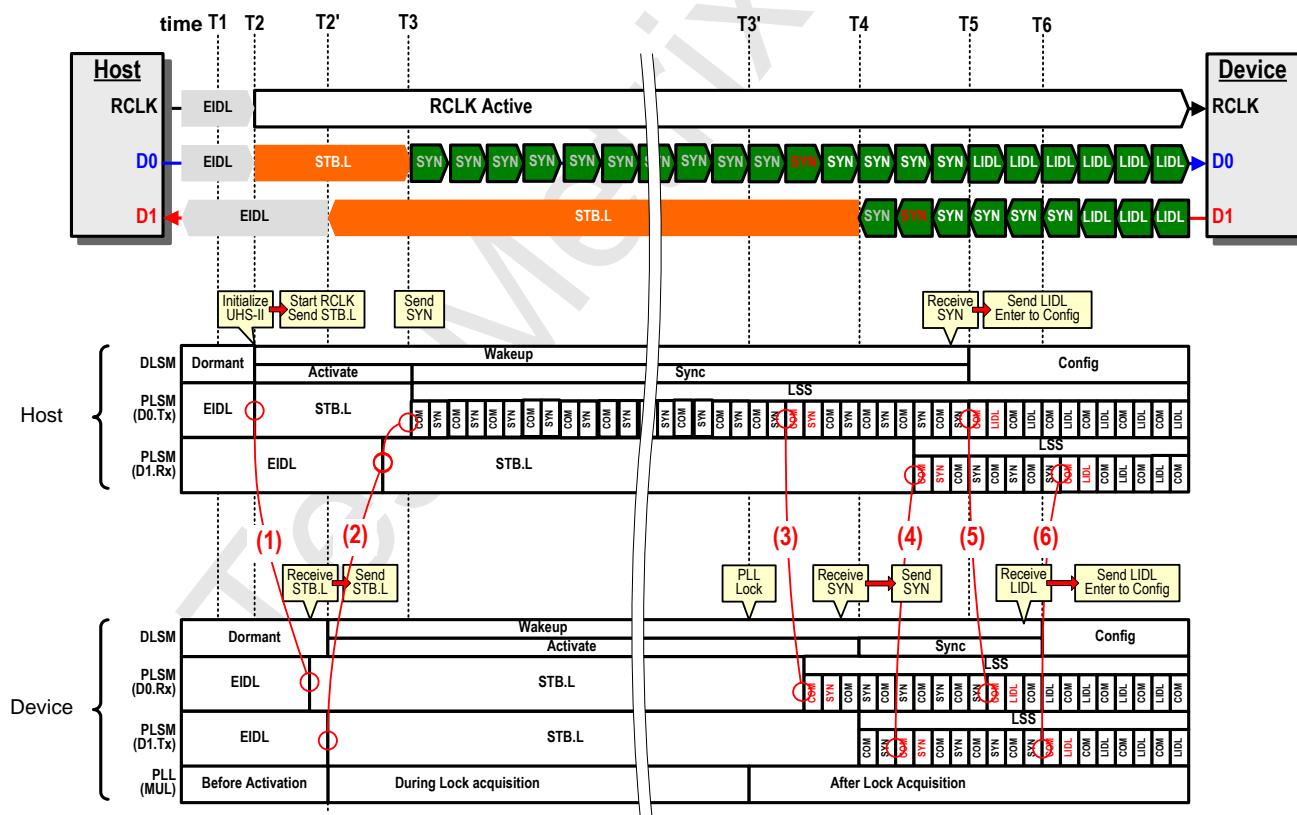


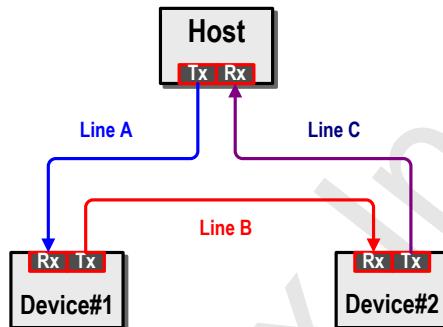
Figure 5-19 : LINK State Transition during PHY Initialization (Point to Point)

- (1) At T2, Host starts to send STB.L through D0.Tx. Device receives it on D0.Rx afterwards.
- (2) Likewise at T2', Device responds to STB.L through D1.Tx and Host receives it on D1.Rx as a result. Note that Device shall respond STB.L within Teidl\_stb. Afterwards, Host starts to send SYN LSS iteratively at T3.

- (3) Device can receive SYN LSS after PLL lock and symbol lock. Note that Device shall complete PLL lock within Tactivate after transitioning to Wakeup state.
- (4) Host receives SYN LSS from Device, and thus it is ensured that both Host and Device complete lock acquisition of PLL at this time.
- (5) After receiving SYN LSS on Host, it starts to send LIDL LSS at T5.
- (6) If Device receives LIDL LSS, it responds by sending LIDL LSS within Tlidl\_lidl.

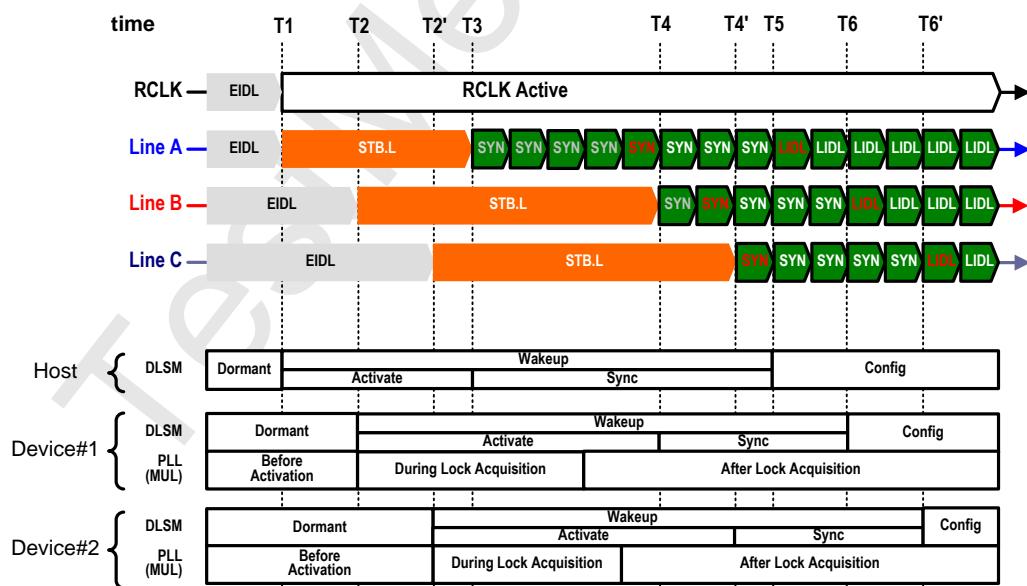
### 5.3.3 LINK State Transition during PHY Initialization (Ring Connection)

In this section, explanation of PHY Initialization in Ring topology is based on Figure 5-20



**Figure 5-20 : Ring Connection Including Two Devices**

Figure 5-21 illustrates a LINK state transition during PHY Initialization for Ring Connection described Figure 5-20. To make simple, PLSM is removed from Figure 5-21. For Link state Transitions during PHY Initialization with Boot Device option refer to Section 5.9.



**Figure 5-21 : LINK State Transition during Wakeup (Ring)**

T1: LINK of Host starts to provide RCLK, drives Tx to STB.L. As a result, DLSM of Host transits to Wakeup.Activate state.

T2: When Device#1 receives STB.L, it starts PLL lock acquisition and enters to Wakeup.Activate. Then it responds by driving Tx to STB.L. Note that Device#1 shall respond STB.L within Teidl\_stb.

T2': Same as T2 for Device#2.

T3: If Host receives STB.L, LINK of Host starts to send SYN LSS immediately for LINK synchronization, and its state transits to Wakeup.Sync.

T4: If Device#1 successfully receives SYN LSS after PLL lock, LINK of Device#1 also starts to send SYN LSS and its state transits to Wakeup.Sync. Note that Device#1 shall complete PLL lock within Tactivate after transitioning to Wakeup state.

T4': Same as T4 for Device#2.

T5: If Host can receive SYN LSS from Device#2, the DLSM transits from Wakeup.Sync to Config, and Host starts to send LIDL LSS.

T6: If Device#1 successfully receives LIDL LSS, LINK of Device#1 also starts to send LIDL LSS within Tlidl\_lidl, and its state transits to Config.

T6': Same as T6 for Device#2.

## 5.4 Power Management

### 5.4.1 Overview

For power management, the following two levels of Low Power State (LPS) are defined. Let SI denote Symbol Interval after PLL locked and it is equal to 10UI.

- **EIDL State:** Lane-level LPS defined in PLSM (Physical Lane State Machine)
  - Both Tx and Rx are synchronously powered off.
    - Lane state shall be kept by pull-down by Tx.
    - Amplitude Detector on Rx shall monitor the differential amplitude of Line whether it indicates EIDL (DIF-PD) or not.
  - Controlled by H/W
- **Dormant State:** Link-level LPS defined in DLSM (Data Link State Machine)
  - All Data Lanes are EIDL. RCLK is stopped and PLL can be powered off.
  - Controlled by S/W as well as H/W
    - GO\_DORMANT\_STATE is to transit to Dormant

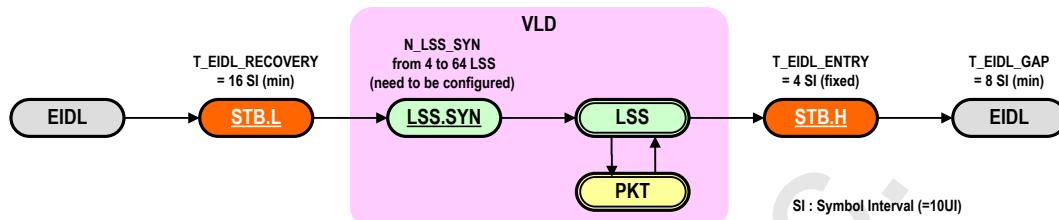
During the Valid Transmission Gap (the period that no information is being transferred in Config and Active state of DLSM), Lane is basically filled with LIDL or DIDL, and EIDL can also be used under certain conditions described below. The filling rules are as follows.

- **Config State:** Valid Transmission Gap shall be filled with LIDL.
- **Active State:** Valid Transmission Gap shall be filled with LIDL, DIDL or EIDL depending on sub state and CFG\_REG setting.
  - **Active.Control:** It is possible to select by setting "Power Control Mode in Active.Control State" in CFG\_REG.
    - **Fast Mode:** LIDL shall be used to keep its synchronization (symbol lock)
    - **Low Power Mode (LPM):** EIDL shall be used during the Valid Transmission Gap to reduce the power consumption. In transitioning from Config to Active.Control ("Config Completion" = 1), Device shall start outputting EIDL (including STB.H before that) from Tx after detecting EIDL on Rx.
    - In Active.Control sub-state under Low Power Mode, LINK shall not transmit two different control packets successively without inserting EIDL. For example, though Device can transmit RES and FCREQ successively in terms of packet transaction during read transaction, LINK of Device shall instruct Tx to transit to EIDL between RES and FCREQ transmission in Low Power Mode.
  - **Active.Trans and Active.Stream:** DIDL shall be used regardless of above two modes.

- **Active.Recv:** No need to fill the gap because both Lanes become Rx.

### 5.4.2 Lane-level LPS Management

Figure 5-22 illustrates state transition of Lane-level LPS management. This is available if Power Control Mode in Active.Control State equals to 1.



**Figure 5-22 : State Transition of Lane-level LPS Management (Tx Side)**

Transmitter side is responsible for managing Lane-level LPS.

- **Recovery from EIDL**

- Tx side shall keep STB.L for the duration of T\_EIDL\_RECOVERY (at least 16 SI) to ensure stable amplitude detection on Rx.
- Rx side shall detect transition from EIDL (DIF-PD) to STB.L (DIF-L) by some means such as Amplitude Detector in PHY to transit to STB.

- **Recovery from STB (STB.L) to VLD**

- Tx side shall transmit N\_LSS\_SYN \* 4 of SYN LSS for synchronization (symbol lock in Deserializer).
- Rx side can acquire its symbol lock by receiving COM symbol (K28.5) of SYN LSS for an implementation specific times to transit to VLD state.
- Disparity of 8b/10b decoder can be initialized to the disparity of COM used for symbol lock.
- N\_LSS\_SYN is predetermined in CFG\_REG during Configuration.

- **Entry to STB (STB.H) after VLD**

- Just after VLD (LSS or PKT) state, Tx side shall keep STB.H for the duration of T\_EIDL\_ENTRY (fixed to 4 SI) to notify Rx of VLD state termination.

- **Entry to EIDL**

- Tx side can enter to EIDL after the elapse of T\_EIDL\_ENTRY in STB.H state. After that, Tx side shall keep EIDL for the duration of T\_EIDL\_GAP (at least 8 SI) before starting next transmission.
- Rx side shall enter to EIDL state during T\_EIDL\_GAP period after STB.H reception.

### 5.4.3 Link-level LPS Management

Link-level LPS management are realized by Dormant state in DLSM. And this section is also related to FULL\_RESET CCMD (refer to Section 6.2.5).

For D0 and D1 Lanes, Line state shall be DIF-PD and Lane state shall be EIDL state for both Tx and Rx during Dormant state.

For RCLK Lane in UHS-II mode, Host should disconnect pull-up resistors of Legacy SD interface. During Dormant state, if the pull-up resistors are disconnected, Tx of RCLK should be DIF-PD to avoid floating RCLK Lane. If the pull-up resistors cannot be disconnected, Tx of RCLK should be DIF-Z to avoid consuming the power by the pull-up resistors.

Note that PLL can be off during Dormant state. Moreover, CFG\_REG values including PHY and LINK

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parameters (e.g. N\_LSS\_SYN, N\_DATA\_GAP, and N\_FCU) shall be preserved during Dormant state.

To regulate time duration to stop RCLK, timing parameter T\_DMT\_ENTRY is defined as 750 [RCLK cycle].

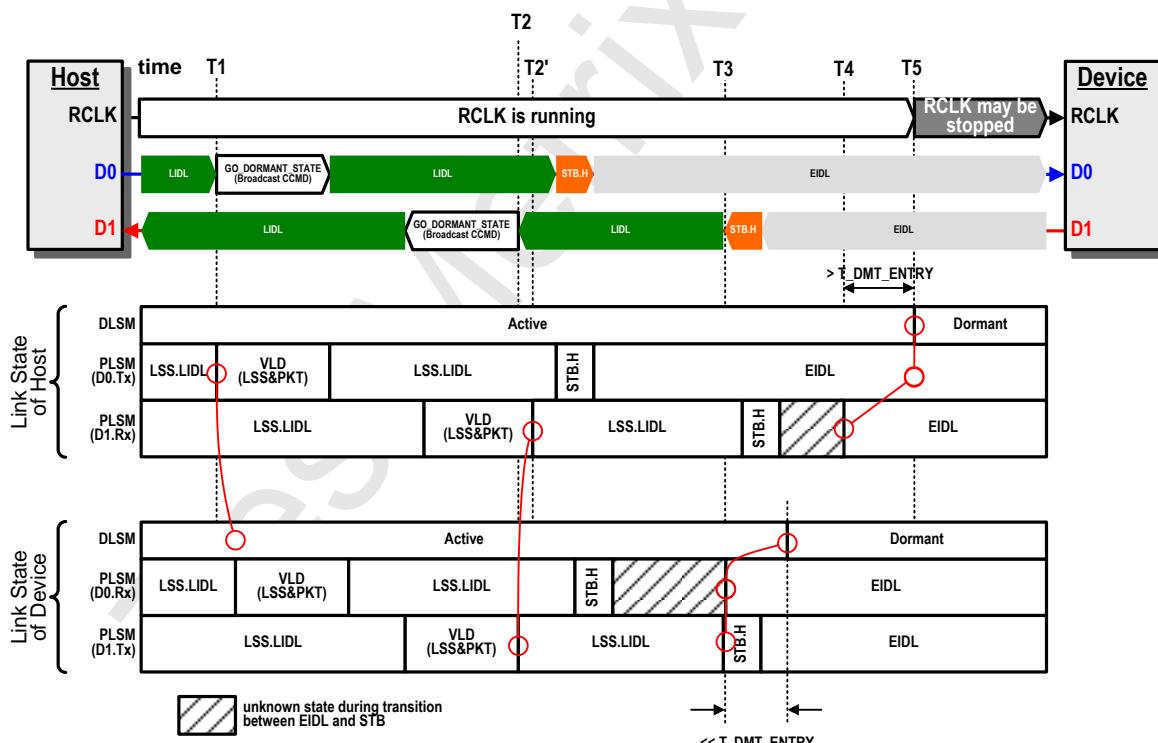
Host may stop RCLK after the elapse of more than T\_DMT\_ENTRY from the time that satisfies both of the following conditions.

- **Condition H-1:** Host receives broadcast GO\_DORMANT\_STATE CCMD, or RES of P2P GO\_DORMANT\_STATE CCMD.
- **Condition H-2:** PLSM of Host is EIDL on D1.Rx.

On the other hand, Device shall enter to Dormant state after the elapse of sufficiently less than T\_DMT\_ENTRY from the time that satisfies both of the following conditions.

- **Condition D-1:** Device transmits broadcast GO\_DORMANT\_STATE CCMD, or RES of P2P GO\_DORMANT\_STATE CCMD.
- **Condition D-2:** PLSM of Device is EIDL on D0.Rx.

Figure 5-23 illustrates a LINK state transition during entry to Dormant state in Fast Mode.



**Figure 5-23 : LINK State Transition during Entry to Dormant State (Fast Mode)**

T1: When Host intends to enter Dormant state, it issues GO\_DORMANT\_STATE CCMD. As described in Table 6-19, Host can issue GO\_DORMANT\_STATE CCMD both as P2P and broadcast. In this example, Host issues the broadcast one.

T2: Device transmits GO\_DORMANT\_STATE broadcast CCMD from D1.Tx as an acceptance of the received CMD. In case of P2P CCMD, it transmits RES instead of broadcast CCMD (Condition D-1).

T2': Host receives GO\_DORMANT\_STATE broadcast CCMD (Condition H-1).

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T3: When PLSM of Device is EIDL on D0.Rx (Condition D-2), timing conditions for Device are satisfied. Then, Device sets D1.Tx to STB.H and EIDL consequently. In addition, it shall start preparing for entry to Dormant State as soon as possible and complete it within the elapse of sufficiently less than T\_DMT\_ENTRY.

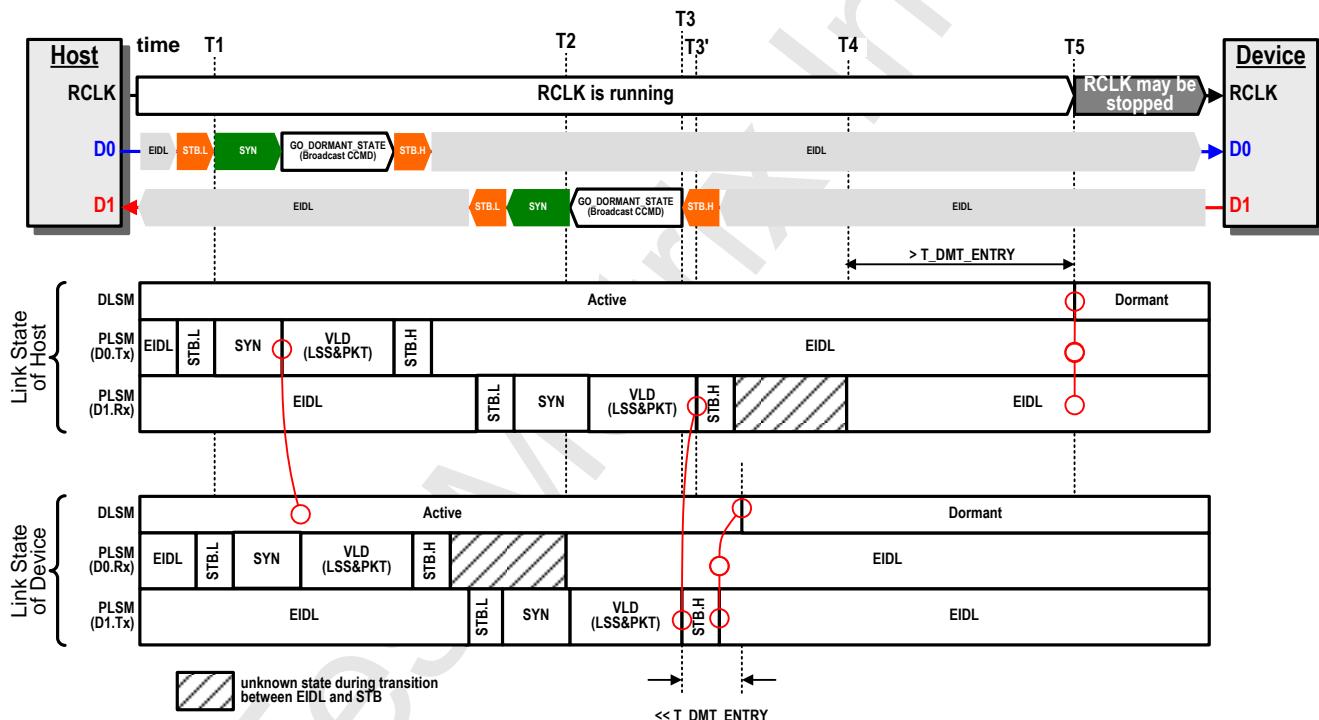
T4: When PLSM of Host is EIDL (Condition H-2) on D1.Rx, then both of timing conditions for Host are satisfied.

T5: Host may stop RCLK after the elapse of more than T\_DMT\_ENTRY from T4.

**Application Note:**

For Fast Mode, if Condition H-2 is not satisfied after the elapse of  $N * T_{DMT\_ENTRY}$  period from Host's driving D0.Tx to EIDL, Host should regard as timeout of entry to Dormant, where N is the number of connected Devices.

Figure 5-24 illustrates a LINK state transition during entry to Dormant state in Low Power Mode.



**Figure 5-24 : LINK State Transition during Entry to Dormant State (Low Power Mode)**

T1: When Host intends to enter Dormant state, it issues GO\_DORMANT\_STATE CCMD.

T2: PLSM of Device is EIDL on D0.Rx (Condition D-2).

T3: Device transmits GO\_DORMANT\_STATE broadcast CCMD from D1.Tx as an acceptance of the received CMD (Condition D-1). At this time D0.Rx is already EIDL, timing conditions for Device are satisfied. Hence, Device shall start preparing for entry to Dormant State as soon as possible and complete it within the elapse of sufficiently less than T\_DMT\_ENTRY.

T3': Host receives GO\_DORMANT\_STATE broadcast CCMD (Condition H-1).

T4: When PLSM of Host is EIDL (Condition H-2) on D1.Rx, then both of timing conditions for Host are satisfied.

T5: Host may stop RCLK after the elapse of more than T\_DMT\_ENTRY from T4.

Note the following items related to Dormant state.

- Refer to Section G.1 and G.2 if Host detects an error during GO\_DORMANT\_STATE or FULL\_RESET sequence.
- Host may stop RCLK when all devices are in Dormant state or executed FULL\_RESET. The timing of stopping RCLK shall be after T\_DMT\_ENTRY from detecting EIDL.
- Full sequence of recovery from Dormant state may depend on application specific layer described in Section 3.3 such as SD-TRAN (refer to Section 7.2.3 in case of SD-memory).

#### 5.4.4 Detailed Specifications for Low Power Mode

Figure 5-25 illustrates a sample of a block diagram of a Lane with related Tx and Rx.

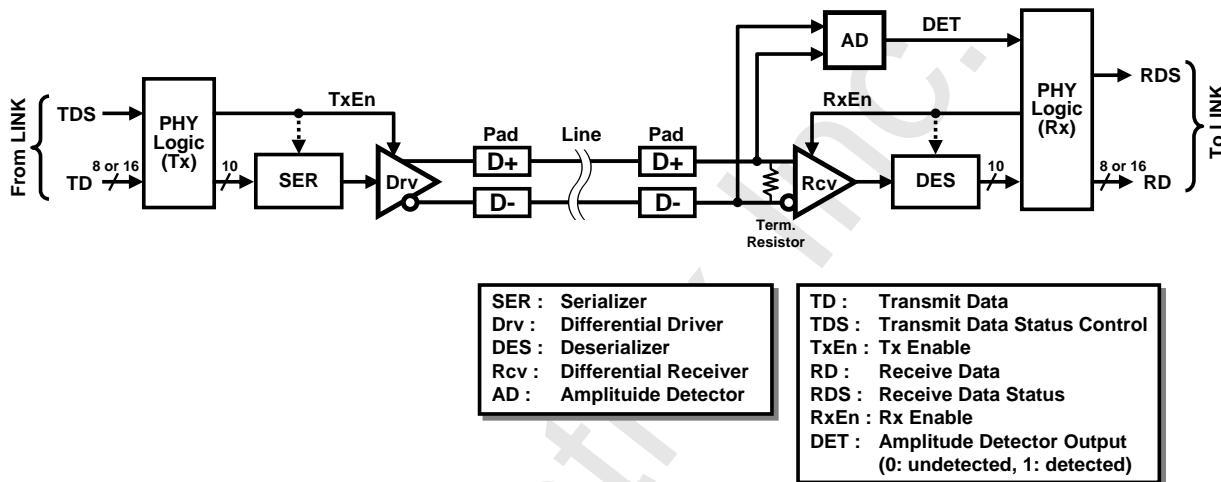


Figure 5-25 : Sample Block Diagram of a Lane

In this example, TD / TDS and RD / RDS are supposed to be defined as PHY-LINK I/F described in Appendix F.

TDS is generated in LINK and transmitted to PHY to control Tx status. It has 4 states which are same as those described in Table 5-7.

- **OFF:**
  - Driver is turned off and keeps DIF-Z (e.g. while 2L-HD mode)
- **EIDL (Electrical Idle):**
  - Driver drives DIF-PD.
- **STB (Standby):**
  - Driver is turned on. Tx output is fixed to DIF-L (= STB.L) or DIF-H (= STB.H).
- **VLD (Valid Symbol):**
  - Driver is turned on. Tx output is a valid 8b/10b symbol.

RDS is generated in PHY Logic and transmitted to LINK to notify Rx status. It has the following 4 states like TDS.

- **OFF:**
  - Receiver and termination resistor are turned off and not in use.
- **EIDL (Electrical Idle):**
  - Receiver is turned off and Amplitude Detector is undetected status (DET = 0). But termination resistor is turned on.
- **STB (Standby):**
  - Receiver is turned on because Amplitude Detector detects active amplitude of STB.L

driven by Tx. Symbol Lock is not established. Moreover all-zeros and all-ones 10 bit symbol at Deserializer are treated as STB.L and STB.H respectively.

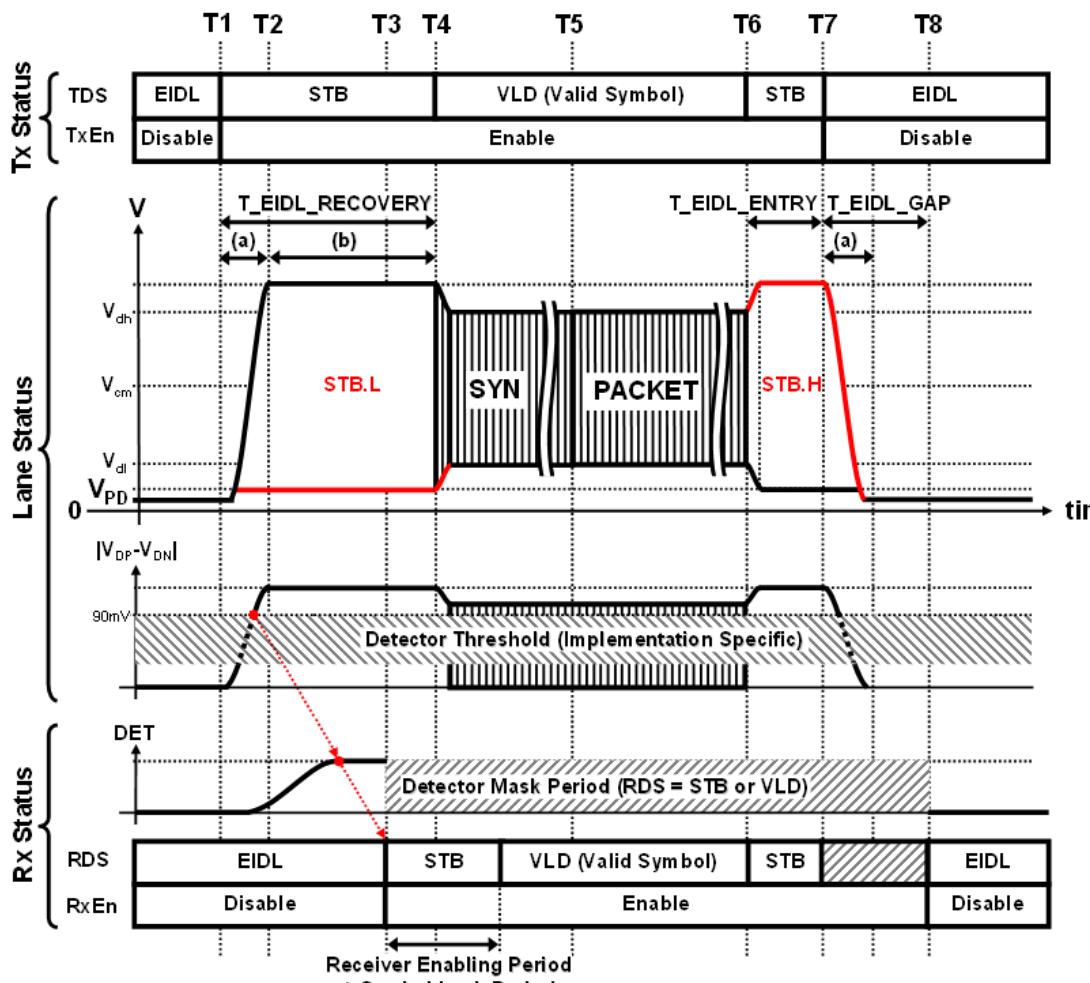
- **VLD (Valid Symbol):**

- Receiver is turned on and Rx can receive a validly aligned 8b/10b symbol because it has already acquired Symbol Lock.

RxEn (Rx enable) can be generated by both DET (Amplitude Detector output) and RDS (for example, RxEn = (DET || (RDS == STB or VLD)). During Wakeup from Dormant State, DET is directly used as RxEn because RCLK is not available at that time. But after Wakeup, DET should be sampled by RCLK before utilizing as the transition condition between EIDL and STB.

Note that RCLK.Rx should be enabled by RxEn on D0.Rx during Wakeup from Dormant because RCLK.Rx does not have Amplitude Detector to avoid unintended wakeup during the period that legacy SD I/F is used (RCLK+/- of UHS-II I/F are shared with DAT0/1 of legacy SD I/F). After exiting from Dormant, Link of Device shall keep RCLK.Rx active because RxEn on D0.Rx may be negated during Active state.

Figure 5-26 illustrates the example sequence for transition from / to EIDL corresponding to the configuration shown in Figure 5-25.



**PHY Timing**

- (a) Driver Enabling / Disabling Period = 2SI (max)
- (b) Stable STB.L Duration for detection = 14SI (min)

**LINK Timing**

- $T_{EIDL\_RECOVERY}$  = 16SI (min)  
Specified STB.L Transmission Period for EIDL Recovery
- $T_{EIDL\_ENTRY}$  = 4SI (fixed)  
Specified STB.H Transmission Period for EIDL Entry
- $T_{EIDL\_GAP}$  = 8SI (min)  
Specified Transmission Gap in EIDL

Figure 5-26 : Transition from/to EIDL

Operations of Tx are as follows.

- LINK instructs the PHY to send STB.L for the period between T1 and T4 ( $\geq T_{EIDL\_RECOVERY} = 16$  SI) to exit from EIDL.
  - $T_{EIDL\_RECOVERY}$  includes the period for Driver Enabling Period required to transit from DIF-PD to DIF-L (T1-T2) and stable STB.L period for amplitude detection (T2-T4).
  - Stable state by STB.L (T2-T4) requires at least 14 SI for stable amplitude detection.
- After sending STB.L for  $T_{EIDL\_RECOVERY}$ , LINK instructs the PHY to send SYN LSS for the period between T4 and T5 ( $= N_{LSS\_SYN} * 4$ , which is to be configured in Config State of DLSM) to establish Symbol Lock before starting packet transmission.
- After packet transmission, LINK instructs the PHY to send STB.H for the period between T6 and T7 ( $= T_{EIDL\_ENTRY} = 4$  SI) before entering to EIDL.
- After sending STB.H for  $T_{EIDL\_ENTRY}$ , LINK instructs the PHY to turn off the Tx by setting TDS

= EIDL at T7. After that, LINK shall keep EIDL for the duration of T\_EIDL\_GAP (at least 8SI) before starting next packet transmission.

Operations of Rx are as follows.

- Amplitude Detector on Rx detects transition from DIF-PD (EIDL) to DIF-L (STB.L) at around T3. After that RDS transits from EIDL to STB and therefore Rx is turned on.
- During T4-T5, Symbol Lock is acquired in Deserializer.
  - Note: Amplitude Detector detects DIF-L by T4 at the latest. So, N\_LSS\_SYN \* 4 (T4-T5) should include not only the period for actual Symbol Lock but also Rx enabling period.
- During T7-T8 (after receiving STB.H), Amplitude Detector on Rx shall be ensured to become undetected status (DET=0) again to prepare for next amplitude detection. Under the condition of DET=0 after T7, RDS can transit to EIDL and therefore Rx can be turned off.
- Output of Amplitude Detector (DET) is not used and masked while RDS = STB or VLD except just after STB.H reception (T7-T8). By T8, DET is required to be "0" (undetected) before RDS transits to EIDL.

## 5.5 Flow Control

### 5.5.1 Flow Control Overview

Fixed window Flow Control (FC) is performed in Link Layer. FC information is transmitted by the following FC MSGs.

- FCREQ (Flow Control Request):** a message packet for indicating "ready to transmit DATA Burst" and requesting FCRDY
- FCRDY (Flow Control Ready):** a message packet for indicating "ready to receive DATA Burst"

Figure 5-27 illustrates the overview of Flow Control sequence.

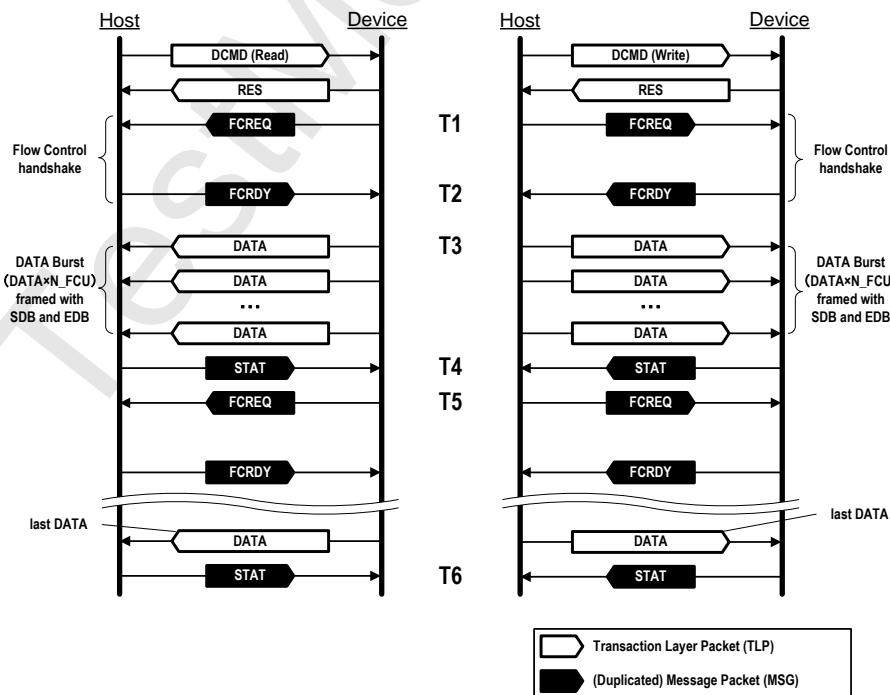


Figure 5-27 : Flow Control Sequence Overview

After DCMD is issued and RES is sent back to Host from Device, FC handshake shall be performed in Link layer before data transfer.

FC sequence is described as follows;

T1: DATA Initiator issues FCREQ when it is ready for transmitting DATA Burst.

T2: DATA Receiver responds by sending FCRDY when it is ready for receiving DATA Burst. (FC handshake is completed, and "FC handshake completion" is indicated to TRAN from LINK in both sides)

T3: DATA Initiator starts data transfer and continues until the end of DATA Burst or more specifically EDB LSS.

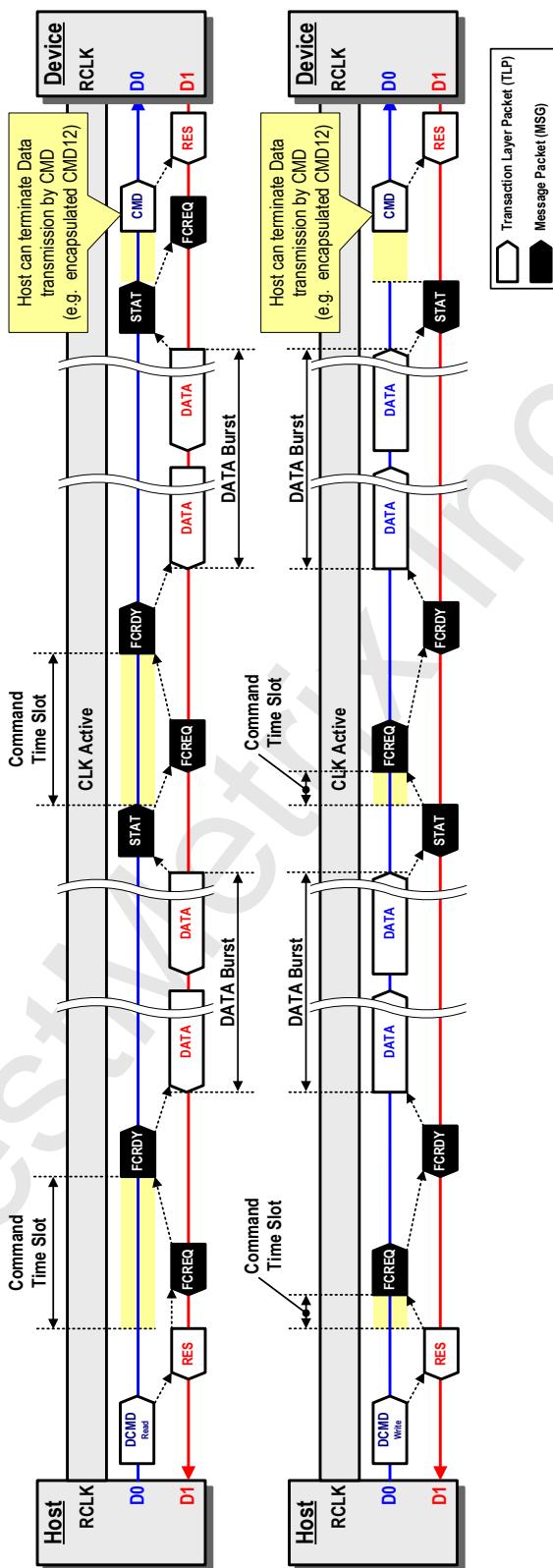
T4: After EDB is received, receiver shall issue STAT (Status) MSG including UNRECOVERABLE\_ERROR and RECOVERABLE\_ERROR identifier that represents whether error had occurred in at least one DATA packet or not.

T5: If there is no error in transmitted DATA Burst, from T1 to T4 is repeated until TLEN sized DATA transfer is completed.

T6: In the case that the last DATA Burst is received, DATA receiver shall issue STAT MSG as T4.

### **5.5.2 Flow Control Handshake and Terminating Data Transmission**

UHS-II has a capability of terminating data transmission even on the way of transaction. To realize this, Host issues either TRANS\_ABORT or application specific command (encapsulated CMD12 in case of SD-TRAN). These commands can be issued only during command time slot (CTS) described below. Figure 5-28 illustrates the overview of CTS during FC and data transmission termination.

**Figure 5-28 : CTS during FC and Terminating Data Transmission**

As shown in Figure 5-28, CTS during data read/write transaction is set as follows;

- In case of read transaction:
  - Between RES reception and FCRDY transmission
  - Between STAT transmission and FCRDY transmission
- In case of write transaction:
  - Between RES reception and FCREQ transmission
  - Between STAT reception and FCREQ transmission

After sending a command during CTS in read transaction, there are two packet order cases as follows: (1) Host receives FCREQ after RES of the command, and (2) Host receives FCREQ before RES. Host shall not ignore the RES that follows FCREQ in such sequence. In case of a Transaction Stop Command (TRANS\_ABORT, CMD12, and FULL\_RESET), any mixture of LIDL, EIDL and DIDL may be sent by Device between the command issued during CTS and its RES.

Detail definition of CTS is described in Section 6.2.13.4.

### 5.5.3 Details of Flow Control Sequence

#### 5.5.3.1 Read Transaction (FD) in Fast Mode

Figure 5-29 illustrates the detailed FC sequence during data read transaction in case of Fast mode.

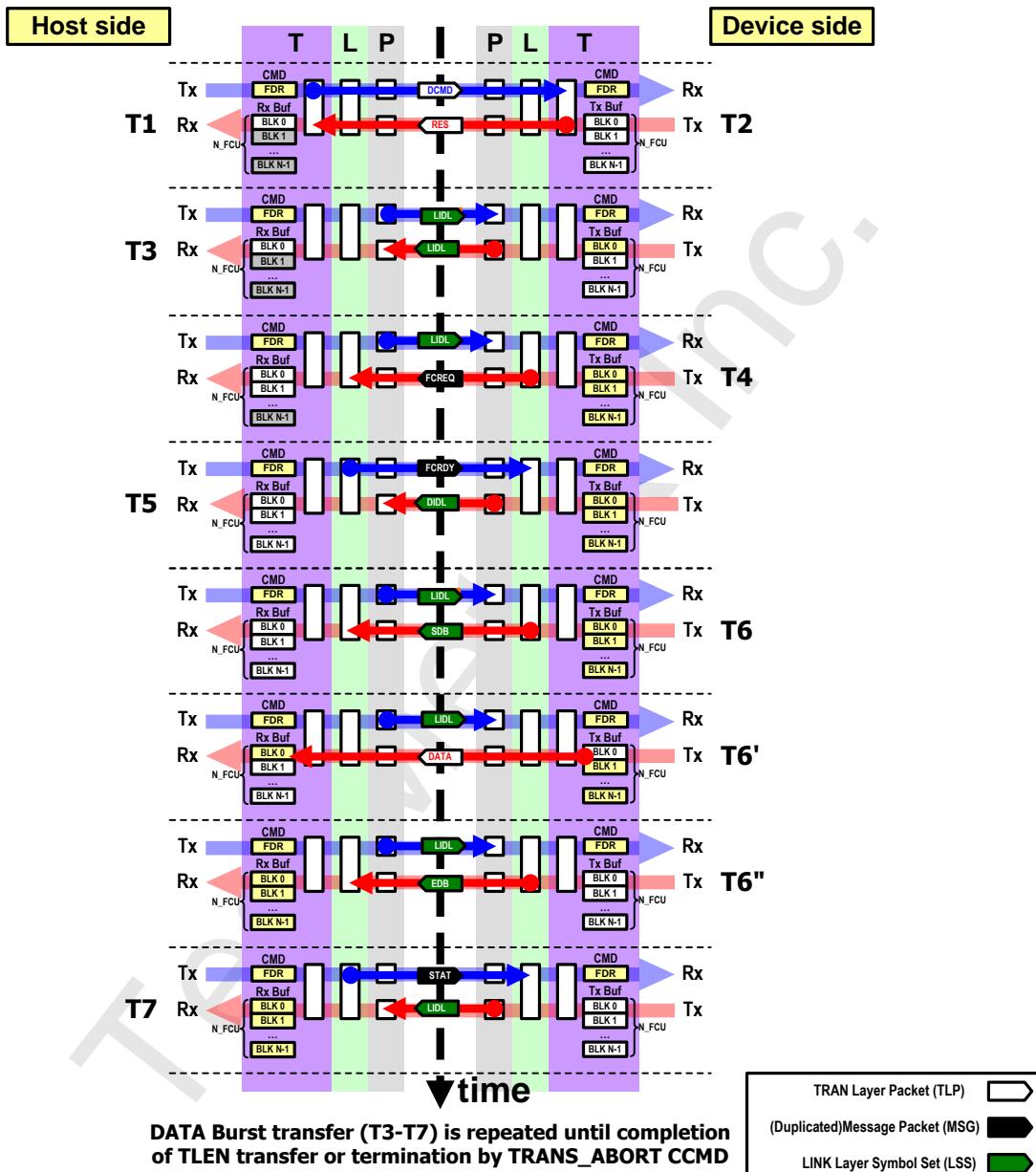


Figure 5-29 : Flow Control Sequence during Data Read (FD, Fast Mode)

T1: TRAN of Host issues DCMD with "FD mode, Read" setting (i.e. DM = 0 and R/W = 0).

T2: TRAN of Device responds by sending RES with FDR setting.

T3: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state. So, both Lanes are filled with a series of LIDL LSS including LIDL0 or LIDL1 symbol as a second symbol in random order.

T4: When Tx Buffer is ready for transmitting DATA Burst (DATA \* N\_FCU), LINK of Device (= DATA Initiator) issues FCREQ (Flow Control Request) MSG directed by TRAN and transits its DLSM from

Active.Control to Active.Trans.WaitRDY. After that, it starts to transmit DIDL LSSes including DIDL0 or DIDL1 as a second symbol in random order.

T5: When Rx Buffer is ready for receiving DATA Burst, LINK of Host (= DATA Receiver) issues FCRDY (Flow Control Ready) MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Host, LINK of Device transits to Active.Trans.TransFD state.

T6: LINK of Device starts to send two SDB (Start of DATA Burst) LSSes in Active.Trans.TransFD state.

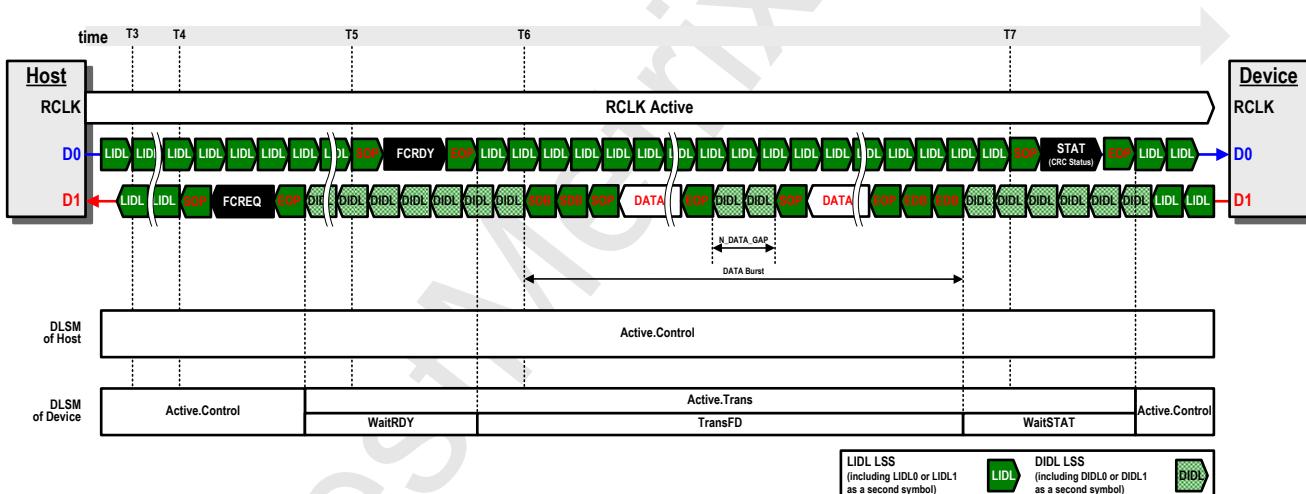
T6': TRAN of Device starts to send Flow Control Unit (= N\_FCU) of DATA packets through LINK and PHY.

T6": After sending DATA packets, LINK of Device sends two EDB (End of DATA Burst) LSSes and transits to Active Trans WaitSTAT state

T7: After receiving at least one EDB, LINK of Host sends STAT (Status) MSG with error identifier (UNRECOVERABLE\_ERROR or RECOVERABLE\_ERROR). And after receiving STAT from Host, LINK of Device goes back to Active.Control state and starts to transmit LIDL LSS.

Note: Fast Mode can be selected in CFG\_REG ("Power Control Mode in Active.Control State") during Configuration and reflected in Active state to minimize the latency during data transfer.

LINK state transition during data read transaction in FD mode and Fast mode is shown in Figure 5-30. LINK of Device transmits DIDL during Active.Trans state. Otherwise all the gaps are filled with LIDL because both sides of LINK stay in Active.Control state under Fast Mode condition.



**Figure 5-30 : LINK State Transition during Data Read (FD, Fast Mode)**

### 5.5.3.2 Read Transaction (FD) in Low Power Mode

Figure 5-31 illustrates the detailed FC sequence during data read transaction in case of Low Power mode.

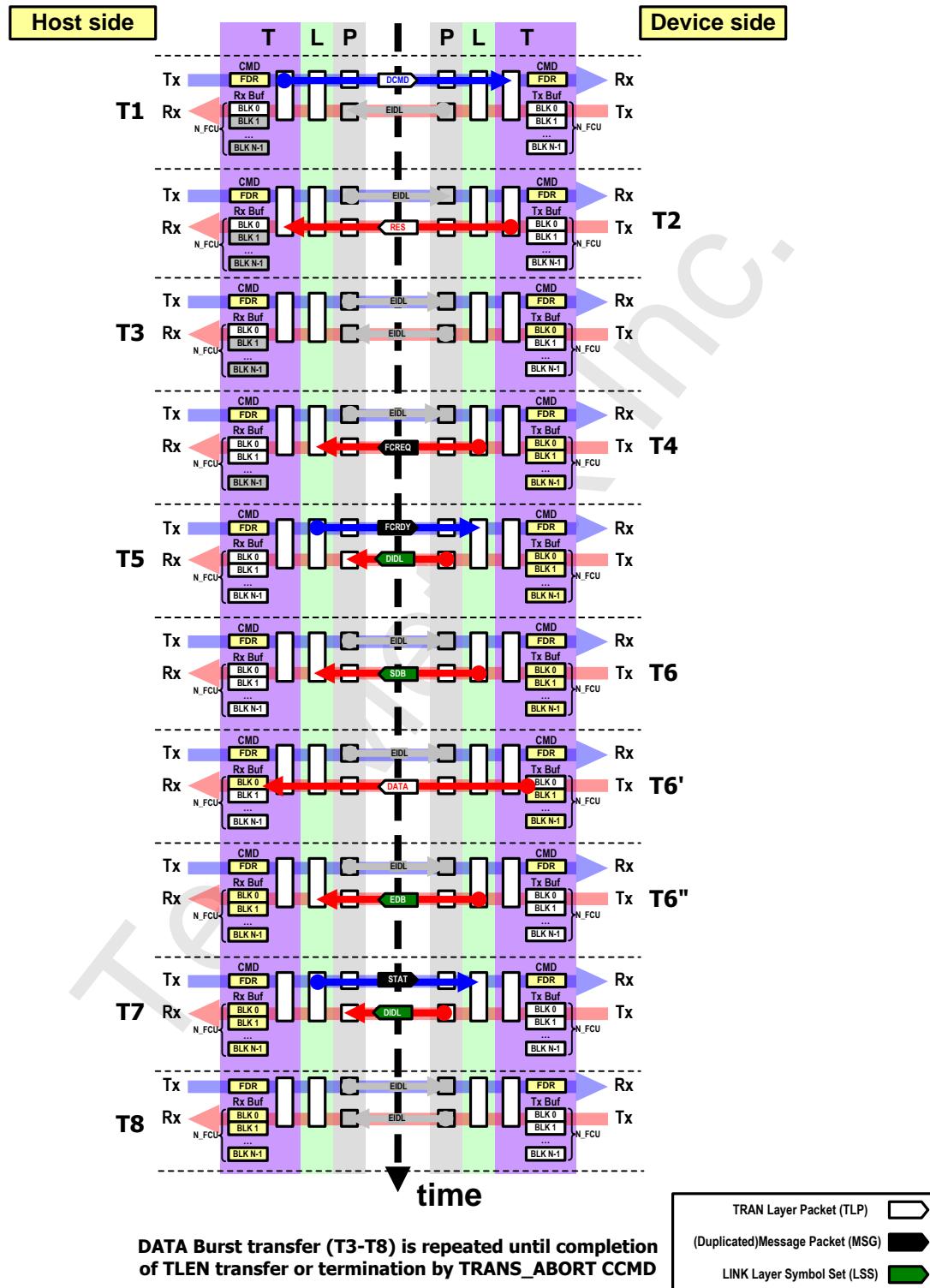


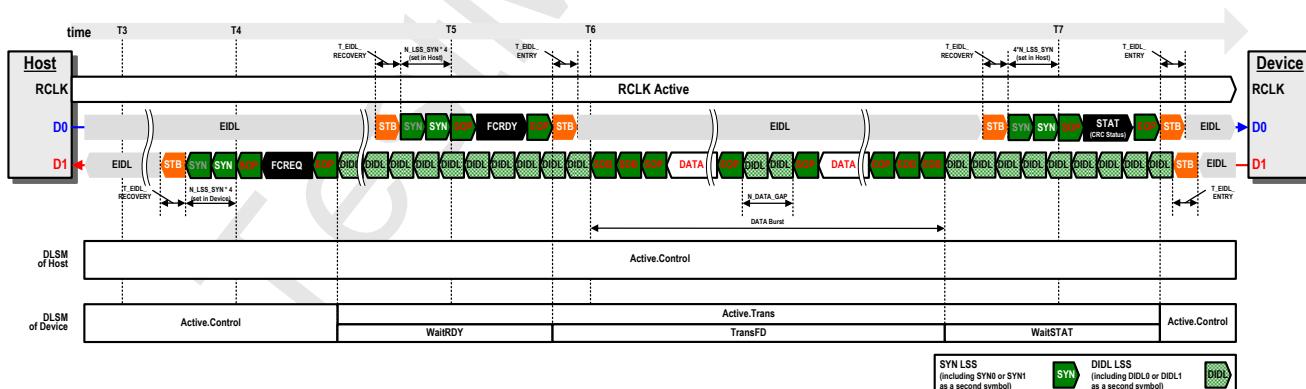
Figure 5-31 : Flow Control Sequence during Data Read (FD, Low Power Mode)

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- T1: TRAN of Host issues DCMD with "FD mode, Read" setting (i.e. DM = 0 and R/W = 0).
- T2: TRAN of Device responds by sending RES with FDR setting.
- T3: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state under Low Power Mode condition. So, both Lanes are filled with EIDL.
- T4: When Tx Buffer is ready for transmitting DATA Burst (DATA \* N\_FCU), LINK of Device (= DATA Initiator) issues FCREQ MSG directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY. After exiting from Active.Control state, LINK of Device starts to transmit DIDL LSSes including DIDL0 or DIDL1 symbol as a second symbol in random order regardless of the setting of "Power Control Mode in Active.Control State" in CFG\_REG.
- T5: When Rx Buffer is ready for receiving DATA Burst, LINK of Host (= DATA Receiver) issues FCRDY MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Host, LINK of Device transits to Active.Trans.TransFD state.
- T6: LINK of Device starts to send two SDB LSSes in Active.Trans.TransFD state.
- T6': TRAN of Device starts to send Flow Control Unit (= N\_FCU) of DATA packets through LINK and PHY.
- T6'': After sending DATA packets, LINK of Device sends two EDB LSSes and transits to Active.Trans.WaitSTAT state.
- T7: After receiving at least one EDB, LINK of Host sends STAT MSG with error identifier (UNRECOVERABLE\_ERROR or RECOVERABLE\_ERROR). And after receiving STAT from Host, LINK of Device goes back to Active.Control state and PLSM of D1 Lane transits to EIDL again.

Note: Low Power Mode can be selected in CFG\_REG ("Power Control Mode in Active.Control State") during Configuration and reflected in Active state to minimize the power consumption during data transfer.

LINK state transition during data read transaction in FD mode and Low Power mode is shown in Figure 5-32. LINK of Device transmits DIDL during Active.Trans state. Otherwise all the gaps are filled with EIDL because both sides of LINK stay in Active.Control state under Low Power Mode condition. Detailed transition from/to EIDL is described in Section 5.4.4, including definition for T\_EIDL\_ENTRY or T\_EIDL\_RECOVERY.



**Figure 5-32 : LINK State Transition during Data Read (FD, Low Power Mode)**

### 5.5.3.3 Write Transaction (FD) in Fast Mode

Figure 5-33 illustrates the detailed FC sequence during data write transaction in case of Fast mode.

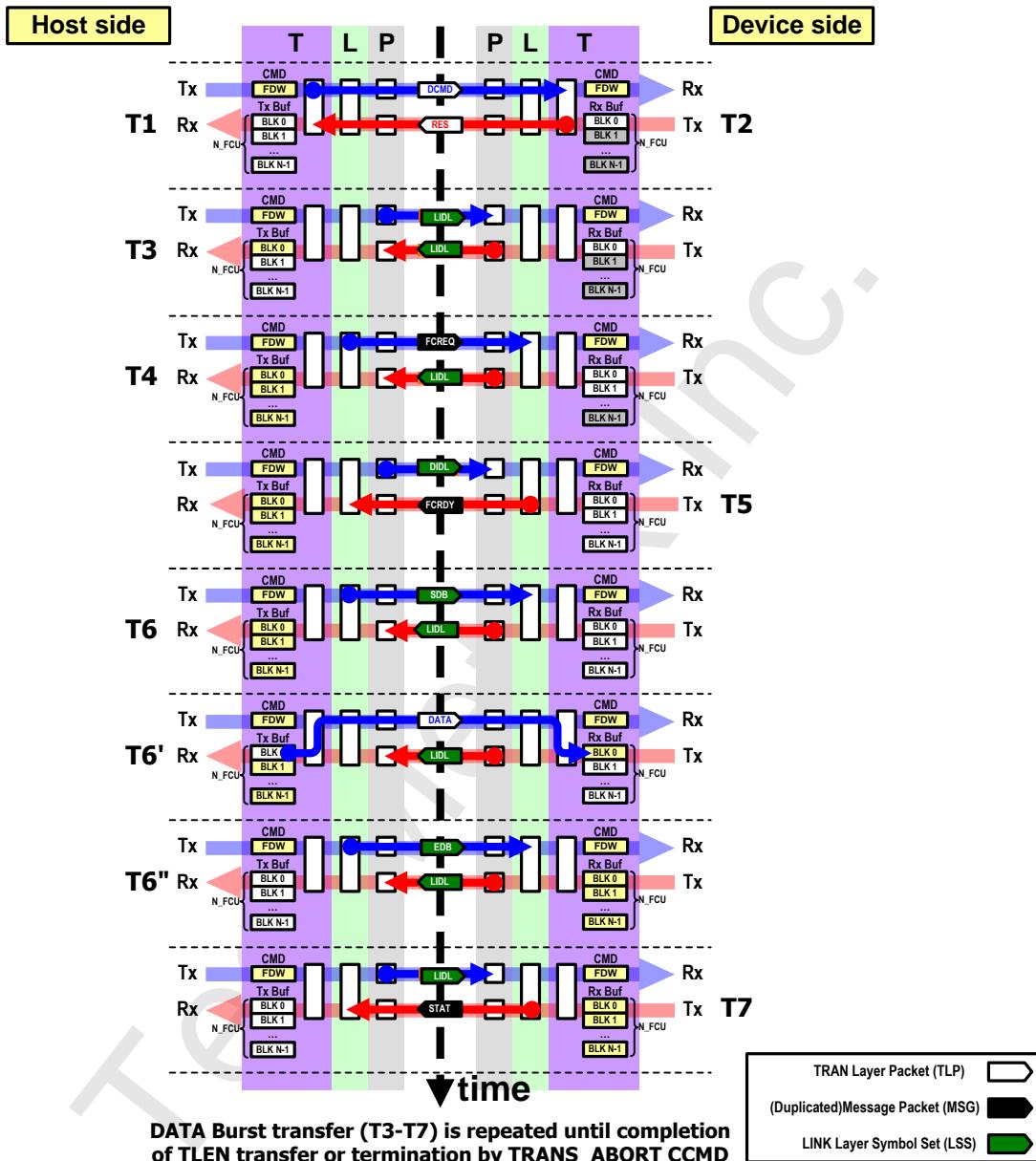


Figure 5-33 : Flow Control Sequence during Data Write (FD, Fast Mode)

T1: TRAN of Host issues DCMD with "FD mode, Write" setting (i.e. DM = 0 and R/W = 1).

T2: TRAN of Device responds by sending RES with FDW setting.

T3: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state. So, both Lanes are filled with a series of LIDL LSS including LIDL0 or LIDL1 symbol as a second symbol in random order.

T4: When Tx Buffer is ready for transmitting DATA Burst (DATA \* N\_FCU), LINK of Host (= DATA Initiator) issues FCREQ (Flow Control Request) MSG directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY. After that, it starts to transmit DIDL LSSes including DIDL0 or DIDL1 as a second symbol in random order.

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T5: When Rx Buffer is ready for receiving DATA Burst, LINK of Device (= DATA receiver) issues FCRDY (Flow Control Ready) MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Device, LINK of Host transits to Active.Trans.TransFD state.

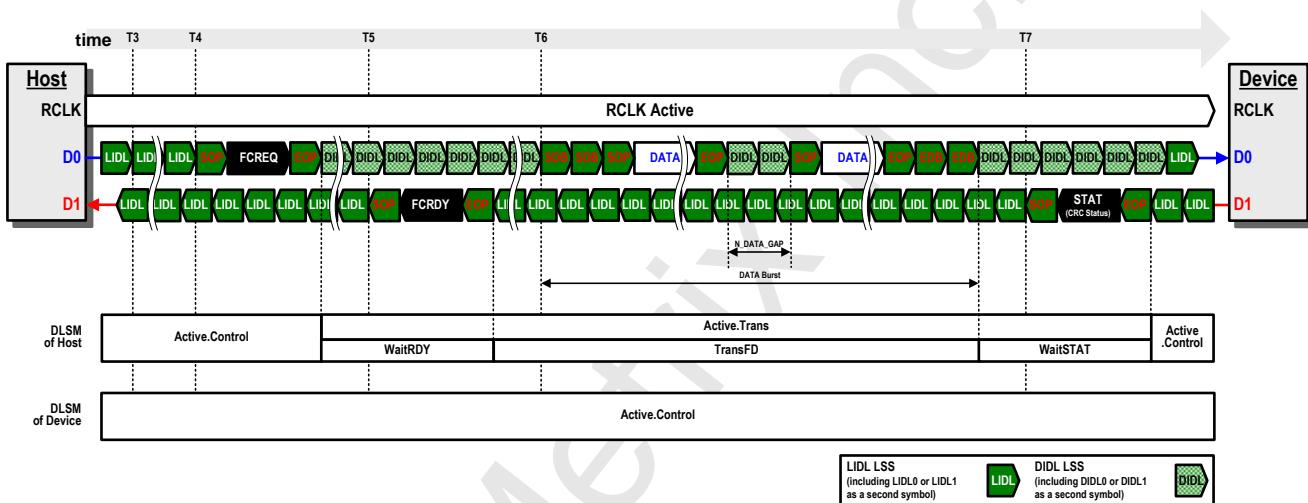
T6: LINK of Host starts to send two SDB (Start of DATA Burst) LSSes in Active.Trans.TransFD state.

T6: TRAN of Host starts to send Flow Control Unit (= N FCU) of DATA packets through LINK and PHY.

T6": After sending DATA packets, LINK of Host sends two EDB (End of DATA Burst) LSSes and transits to Active.Trans.WaitSTAT state.

T7: After receiving at least one EDB, LINK of Device sends STAT (Status) MSG with error identifier (UNRECOVERABLE\_ERROR or RECOVERABLE\_ERROR). And after receiving STAT from Device, LINK of Host goes back to Active.Control state and starts to transmit LIDL LSS.

LINK state transition during data write transaction in FD mode and Fast mode is shown in Figure 5-34.



**Figure 5-34 : LINK State Transition during Data Write (FD, Fast Mode)**

### 5.5.3.4 Write Transaction (FD) in Low Power Mode

Figure 5-35 illustrates the detailed FC sequence during data write transaction in case of Low Power mode.

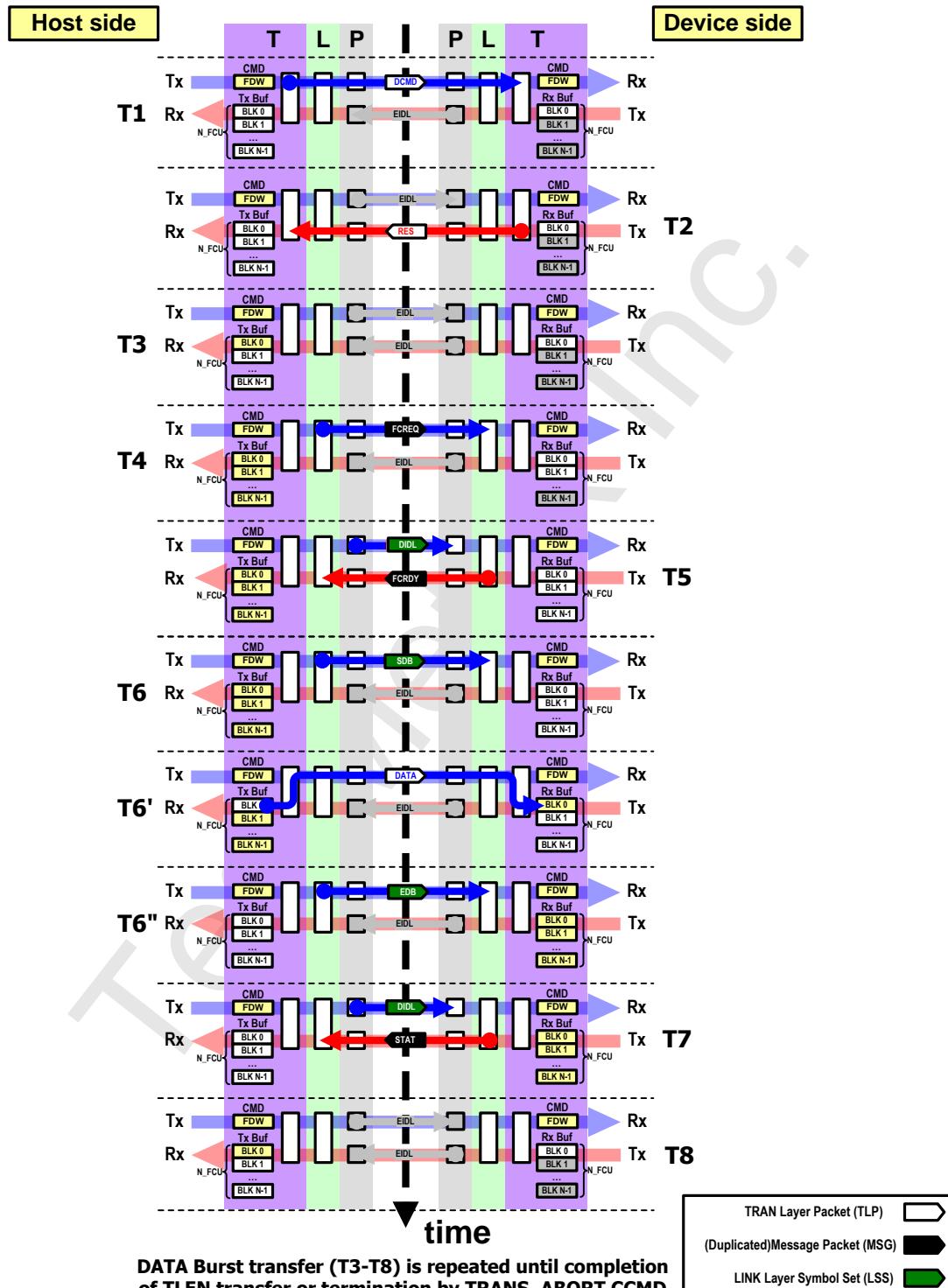


Figure 5-35 : Flow Control Sequence during Data Write (FD, Low Power Mode)

T1: TRAN of Host issues DCMD with "FD mode Write" setting (i.e. DM = 0 and R/W = 1).

T2: TRAN of Device responds by sending RES with FDW setting.

T3: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state under Low Power Mode condition. So, both Lanes are filled with EIDL.

T4: When Tx Buffer is ready for transmitting DATA Burst (DATA \* N\_FCU), LINK of Host (= DATA Initiator) issues FCREQ MSG directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY. After exiting from Active.Control state, LINK of Host starts to transmit DIDL LSSes including DIDL0 or DIDL1 as a second symbol in random order regardless of the setting of "Power Control Mode in Active.Control State" in CFG\_REG.

T5: When Rx Buffer is ready for receiving DATA Burst, LINK of Device (= DATA Receiver) issues FCRDY MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Device, LINK of Host transits to Active.Trans.TransFD state.

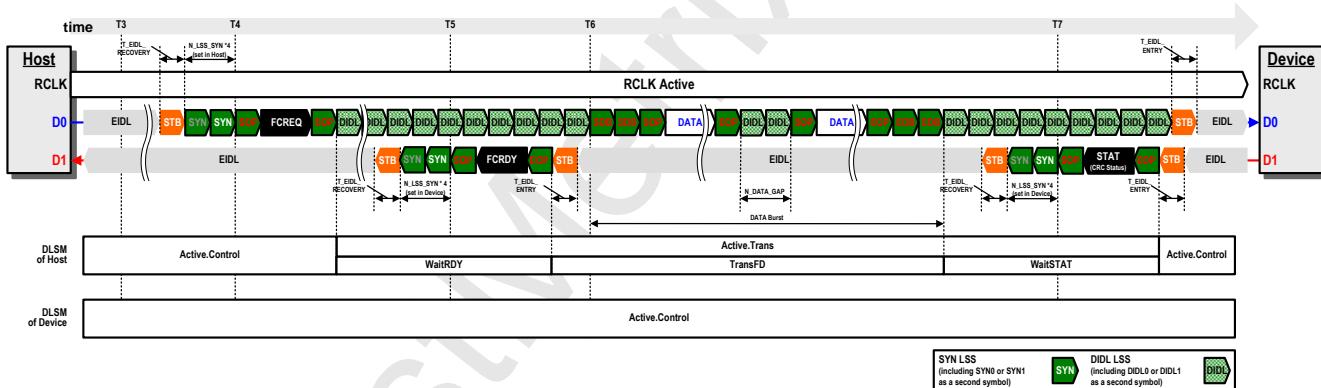
T6: LINK of Host starts to send two SDB LSSes in Active.Trans.TransFD state.

T6': TRAN of Host starts to send Flow Control Unit (= N\_FCU) of DATA packets through LINK and PHY.

T6": After sending DATA packets, LINK of Host sends two EDB LSSes and transits to Active.Trans.WaitSTAT state.

T7: After receiving at least one EDB, LINK of Device sends STAT MSG with error identifier (UNRECOVERABLE\_ERROR or RECOVERABLE\_ERROR). And after receiving STAT from Device, LINK of Host goes back to Active.Control state and PLSM of D0 Lane transits to EIDL again.

LINK state transition during data write transaction in FD mode and Low Power mode is shown in Figure 5-36.



**Figure 5-36 : LINK State Transition during Data Write (FD, Low Power Mode)**

As described in this section, Flow Control and associated DATA Burst transfer protocol are defined symmetrically for both read and write case.

#### 5.5.4 DATA Burst Retry

In order to prevent stalling DATA transaction due to transmission error, the following DATA Burst Retry function shall be available. All Nodes shall have retry counter and set to 0 at the DCMD transaction.

- During DATA Burst transfer, transmission error causes FRAME\_ERROR or CRC\_ERROR at the DATA Receiver side. If the error is detected in the DATA Burst framing, it shall be handled as FRAME\_ERROR. Note that SDB and EDB are placed twice for improving transmission error tolerance. So, even if either one is corrupted, it does not cause FRAME\_ERROR. And if the error occurs during the actual packet between SOP and EOP, it can be detected as CRC\_ERROR in LINK. LINK can detect those transmission error in accordance with Packet Receiving Flow Chart described in Section 5.8.
- If DATA Receiver side detects occasional transmission error during DATA Burst reception, it

notifies the Initiator side of the error via STAT MSG with RECOVERABLE\_ERROR = 1. Moreover, if it detects RETRY\_EXPIRE\_ERROR, it should notify the Initiator side of the error via STAT MSG with UNRECOVERABLE\_ERROR = 1.

- If DATA Initiator side receives STAT MSG or FCRDY MSG with UNRECOVERABLE\_ERROR = 1 during DATA transaction, it means the DATA transaction cannot be recovered by DATA Burst Retry mechanism regardless of RECOVERABLE\_ERROR. In that case, flow control sequences shall be given up and Host should send TRANS\_ABORT CCMD or encapsulated CMD12 (in case of SD-TRAN) to terminate the DATA transaction.
- If DATA Initiator side receives STAT MSG with RECOVERABLE\_ERROR = 1 and UNRECOVERABLE\_ERROR = 0 after DATA Burst transmission, it compares its retry counter and "MAX\_RETRY\_NUM" in CFG\_REG. If retry counter is smaller than "MAX\_RETRY\_NUM", it shall increment retry counter by 1 and start from a flow control handshake to retransmit the whole DATA Burst again without any software operation. Otherwise, Initiator shall stop flow control sequence, and in addition, Host should abort the DATA transaction same as the case of UNRECOVERABLE\_ERROR.
- When Device detects that retry counter reaches to "MAX\_RETRY\_NUM", it sets RETRY\_EXPIRE\_ERROR to 1 in ST\_REG. Moreover, it should notify UNRECOVERABLE\_ERROR = 1 by MSG as described in Section 5.2.5.
- In case that DATA Initiator side receives STAT MSG with UNRECOVERABLE\_ERROR = RECOVERABLE\_ERROR = 0, it transmits next DATA Burst and sets retry counter to 0.
- DATA Burst Retry function is available only for the DATA Burst, not for control packets.

Figure 5-37 illustrates DATA Burst Retry sequence and its possible implementation related to Tx / Rx Buffer.

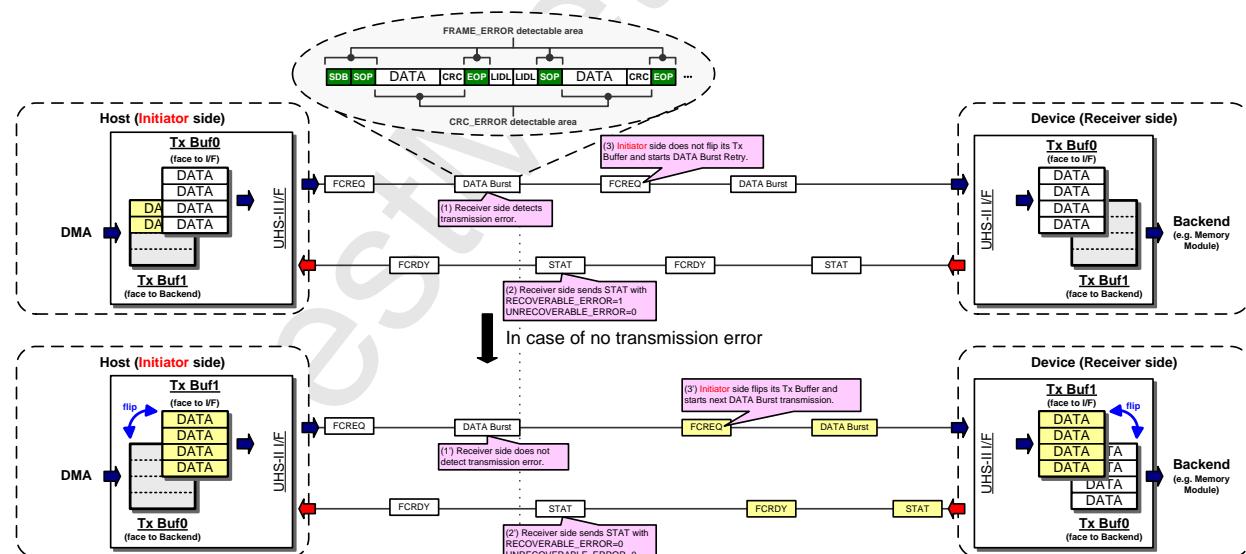


Figure 5-37 : DATA Burst Retry Sequence

If both sides have dual buffer (like ping-pong buffer), one of the dual buffer is supposed to be connected to UHS-II I/F and the buffers can be flipped only after transferring STAT MSG with UNRECOVERABLE\_ERROR = RECOVERABLE\_ERROR = 0 and preparing Tx or Rx Buffer for the next DATA Burst transfer. If the initiator side receives STAT MSG with RECOVERABLE\_ERROR only, it does not flip the buffer and its remaining source data shall be retransmitted with DATA Burst Retry mechanism. DATA Burst Retry can be continued until the retry counter reaches to "MAX\_RETRY\_NUM" in CFG\_REG.

## 5.6 Packet Bypassing

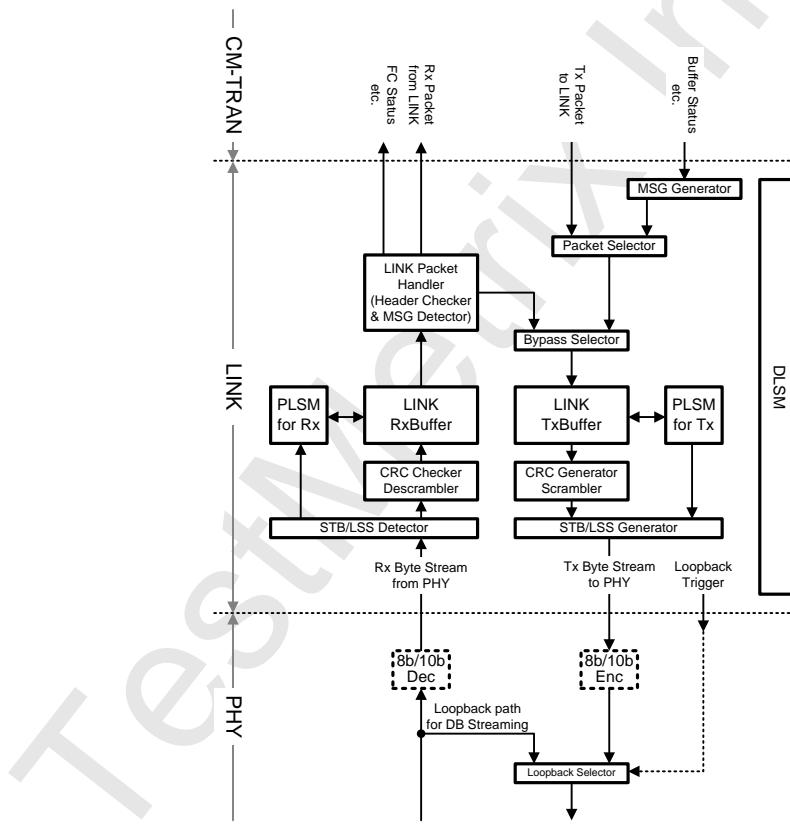
### 5.6.1 Overview

It is required that both Host and the target Device can communicate as if they are connected Point to Point regardless of actual topology, in terms of small latency and power consumption. In other words, non-target (= intermediate) Device shall be transparent from Host and the target Device. Considering UHS-II Ring topology, LINK is responsible for bypassing the received packet according to SID and DID in its Header to make more topology-independent protocol of upper layer (= TRAN). And to take full advantage of UHS-II Ring, DATA Burst Streaming is introduced for transferring DATA Burst to the target Device with minimum latency.

### 5.6.2 Control Packet Bypassing

This section shows how LINK bypasses a control packet (= non-DATA packet) internally.

Figure 5-38 illustrates an example of LINK architecture for packet bypassing.



Note: 8b/10b Decoder may notify detecting all-zero symbols and all-one symbols as STB.L and STB.H respectively.

Figure 5-38 : Example of LINK Architecture for Packet Bypassing

When LINK receives the Rx Byte Stream from PHY, it detects SOP LSS by the STB/LSS Detector and stores the following packet content in the LINK RxBuffer, with descrambling and CRC calculation. Afterward, when it detects EOP LSS, it stops CRC calculation and compares the result of the calculation with CRC embedded in the received packet. If no CRC\_ERROR, it checks Header of received packet in the LINK Packet Handler and determines either to accept it, to bypass it or to discard it as an error. Refer to Section 5.8 for details of Packet receiving flows and conditions of Header checking mentioned above. If the determination is to bypass, it switches the Bypass Selector and

enables to store the packet in the LINK TxBuffer. That packet is treated as to calculate CRC and to scramble, and added SOP and EOP LSS by STB/LSS Generator, and transmitted to PHY as the Tx byte Stream.

As the Control Packet Bypassing takes place in Active.Control state of DLSM, the packet gap is EIDL if Low Power Mode is selected. If the state of Tx is EIDL before bypassing, the STB/LSS Generator shall transmit STB.L and SYN LSS for the period of T\_EIDL\_RECOVERY and N\_LSS\_SYN \* 4 respectively as mentioned in Section 5.4.4. During this period, LINK shall wait to transmit the bypassed packet in the LINK TxBuffer. Even if the following packet is coming from PHY at this time, LINK does not need to store it in the LINK RxBuffer immediately because it takes the same period for STB.L and SYN LSS before starting its reception. So, the size of LINK TxBuffer or RxBuffer can be determined considering maximum size of one Control Packet.

Device shall bypass Control Packets without any modifications if DID is not its own Node ID. Note that payload field of DEVICE\_INIT, ENUMERATE, and INQUIRY\_CONFIG may be modified before these CMDs are transmitted to the next Node.

### 5.6.3 DATA Burst Streaming

This section shows how LINK bypasses a DATA Burst in cooperation with PHY by means of DATA Burst Streaming. As FCREQ always precedes a DATA Burst and it is reliably routed through Ring to the target Device in accordance with packet receiving flow described in Section 5.8, the pathway for a DATA Burst is ensured by the corresponding FCREQ. Refer to Figure 5-38 for more architectural information about DATA Burst Streaming.

If LINK receives FCREQ which is targeted to other Device, LINK Packet Handler determines to bypass that. Just after bypassing the FCREQ, LINK transits to Active.Stream sub-state and starts to transmit DIDL LSS from STB/LSS Generator. When entering to this state, LINK instructs to PHY to enable Loopback path for entering to DATA Burst Streaming mode. When PHY enables Loopback path, plural DIDL LSS transmitted after FCREQ are removed because Loopback path shortcuts the transmission route inside PHY and LINK. PHY is responsible for preserving the disparity and LSS boundary before and after enabling Loopback path. During DATA Burst Streaming, LINK shall continuously monitor Rx byte stream from PHY in STB/LSS Detector to detect EDB LSS as a condition for exiting from DATA Burst Streaming mode. Loopback path for Data Burst Streaming is permitted to be located either before or behind 8b/10b decoder (refer to Appendix F for more details about how to instruct PHY to enable or disable Loopback path and how to keep the disparity before and after switching Loopback Selector).

If at least one of the two EDB LSSes is certainly detected, LINK instructs PHY again to disable Loopback path. LINK continues to transmit DIDL LSS during Active.Stream sub-state, and PHY is responsible for preserving the disparity and LSS boundary before and after disabling Loopback path. Otherwise, symbol re-lock and the associated re-initialization of the disparity may be additionally required at the next Device. After disabling Loopback path, LINK continues to transmit DIDL LSS in Active.Stream sub-state and it goes back to Active.Control sub-state when it detects the following LIDL LSS (in case of Fast Mode) or EIDL (in case of Low Power Mode). Even if both EDB LSSes are lost, LINK can exceptionally exit from DATA Burst Streaming mode by detecting LIDL LSS or EIDL.

It is mandatory for PHY to keep the disparity and LSS boundary when switching the Loopback Selector. In addition, the following rules shall be kept in order to execute DATA Burst Streaming properly.

- LINK shall direct to enable Loopback path when EOP of FCREQ is transmitted.
- LINK shall also direct to disable Loopback path when EDB is received.
- Enabling or disabling Loopback path shall be completed within 20SI after direction from LINK.

Moreover, not only VLD symbols but also STB.H and EIDL shall be bypassed when enabling Loopback path.

Figure 5-39 illustrates an entry and exit sequence for DATA Burst Streaming. Suppose that Device#2 is the target Device in this example.

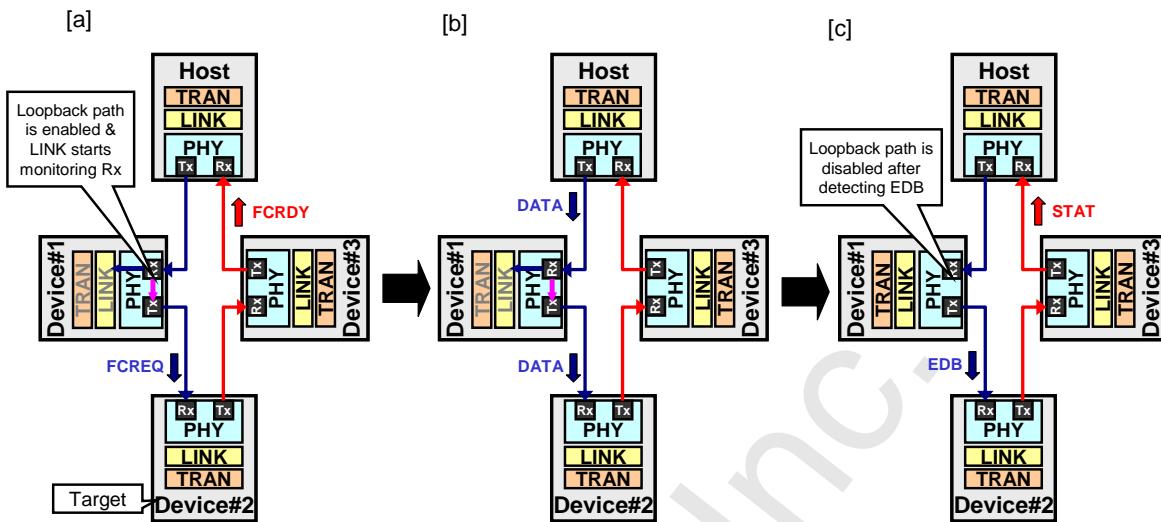


Figure 5-39 : Packet Handling for DATA Bypassing

In Figure 5-39 [a], as Device#1 is not a target Device, it enters to DATA Burst Streaming mode after it bypasses FCREQ from its Tx Port. While DATA Burst Streaming mode, DATA Burst is bypassed directly from Rx to Tx through Loopback path (Figure 5-39 [b]). If Device#1 detects EDB LSS, it exits from the mode by disabling the Loopback path (Figure 5-39 [c]).

As mentioned in Section 5.4.1, the Valid Transmission Gap between FCREQ transmission and STAT reception shall be filled with DIDL regardless of the setting of "Power Control Mode in Active.Control State" in CFG\_REG. So, Loopback path is enabled and disabled during DIDL period.

## 5.7 Data Integrity

### 5.7.1 Overview

All UHS-II packets are added CRC for data integrity. Calculation and verification of CRC are performed in LINK.

### 5.7.2 Detection and Notification of CRC Error

LINK of receiver calculates CRC of incoming packet and compares to its CRC field. When receiver detects CRC error from at least one DATA packet within DATA Burst, it shall send STAT MSG whose RECOVERABLE\_ERROR = 1 after completing reception of the DATA Burst (Refer to Section 6.2.15.2 for more details). On the other hand, receiver sends nothing if it detects CRC error from packets other than DATA. Host can detect error by not receiving the expected packet within the predetermined period.

### 5.7.3 CRC16 Generation Polynomial

#### 5.7.3.1 Overview

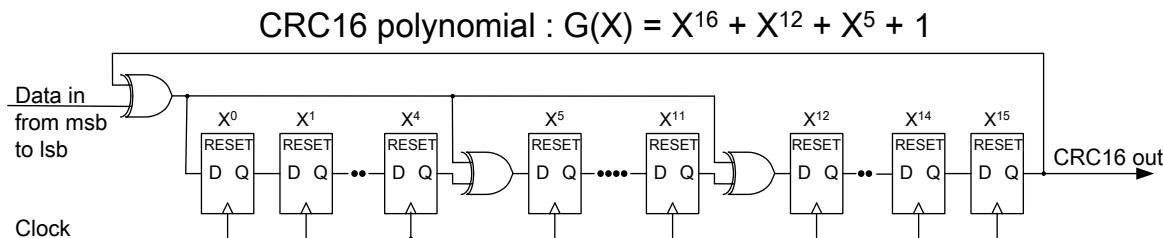
The length of CRC for all types of UHS-II packet is fixed to 16bits (CRC16). CRC16 is calculated with all bits (including reserved bits) of UHS-II packets including PAD (K23.7) if exists. PAD (K23.7) shall be treated as D23.7 (F7h) in CRC calculation. The generator polynomial is as follows.

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

Before starting the CRC16 calculation, the initial value of CRC16 shall be set to 0000h and the CRC16 calculation shall be processed in order from msb to lsb. The result of CRC16 shall be transmitted MSB

first and then LSB.

Figure 5-40 shows a block diagram of CRC16 calculation.



**Figure 5-40 : CRC16 Calculation**

### 5.7.3.2 Example of CRC16 Calculation

Let the input packet containing 4 bytes be as follows (one of FCRDY MSG).

{a7, a6, ..., a0} = 1111_0001 :	NP = 1, TYP = 111b (MSG), DID=1
{b7, b6, ..., b0} = 0000_0000 :	SID = 0, TID = 0
{c7, c6, ..., c0} = 0000_0001 :	CTG = 000b (LMSG), IDX = 0001b (FCRDY)
{d7, d6, ..., d0} = 1000_0000 :	CODE = 1000000b (UNRECOVERABLE_ERROR)

As the data is input to the CRC16 calculator in the order of a7, a6, ..., a0, b7, ..., d0, the result of CRC16 calculation is 4B40h. In this case, MSB (4Bh) is transmitted first and LSB (40h) is transmitted second.

## 5.7.4 Scrambling

### 5.7.4.1 Overview

Both Host and Device shall have scrambling function as mentioned below.

The CRC of a frame is a 2 bytes (16-bit) field that shall follow the last byte of the contents of a Packet and precede EOP LSS.

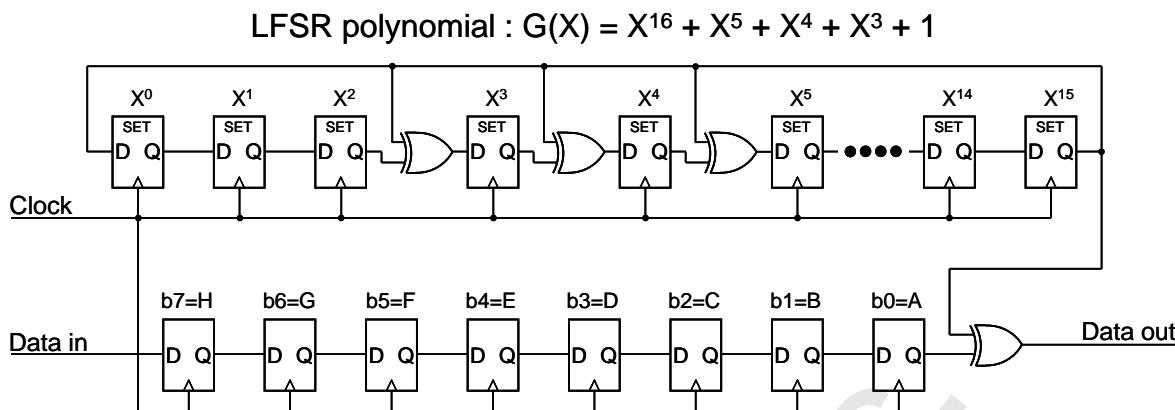
The contents of a frame shall be scrambled before transmission.

Scrambling shall be performed by XOR operation on the transmitting data with the output of a linear feedback shift register (LFSR). The LFSR shall be implemented with the following polynomial:

$$G(X) = X^{16} + X^5 + X^4 + X^3 + 1$$

The LFSR shall be initialized with the value of FFFFh before the first shift of the LFSR. The shift register shall be initialized to the seed value before SOP LSS is transmitted. All data words between the SOP LSS and EOP LSS shall be scrambled, including the CRC. If PAD (K23.7) is scrambled, the scrambled PAD data shall be replaced with PAD (K23.7) before transmitting from transmitter.

Figure 5-41 shows a block diagram for LFSR with scrambling polynomial.



**Figure 5-41 : LFSR with Scrambling Polynomial**

#### 5.7.4.2 The Operation Order of CRC, Scrambling and 8b/10b

On the transmitter side, the operation order of CRC, scrambling and 8b/10b shall be as follows. The CRC calculation shall be applied on the packet data following SOP LSS. The packet data shall be applied the XOR operation with LFSR output, if the PAD exists in the packet data it shall be replaced with PAD (K23.7) after the XOR operation of the scrambler. And then, the frame data shall be submitted to the 8b/10b encoder.

Similarly, on the receiver side, the frame data shall be decoded by a 10b/8b decoder, and the decoded packet data shall be applied on XOR operation with the scrambler output, if the PAD (K23.7) exists in the packet data, it shall be reverted to PAD (K23.7) after XOR operation.

And then, the operated packet data presented to the Link layer and subsequently used in calculating the CRC.

#### 5.7.4.3 LSS Scrambling

To prevent fixed bit stream repetition, LIDL, DIDL, SYN and BSYN LSS have some variations.

Each LSS consists of 2 symbols, COM = K28.5 symbol and LIDL / DIDL / SYN / BSYN symbol as described in Section 5.2.2.2.

These second symbols have 2 variations as follows;

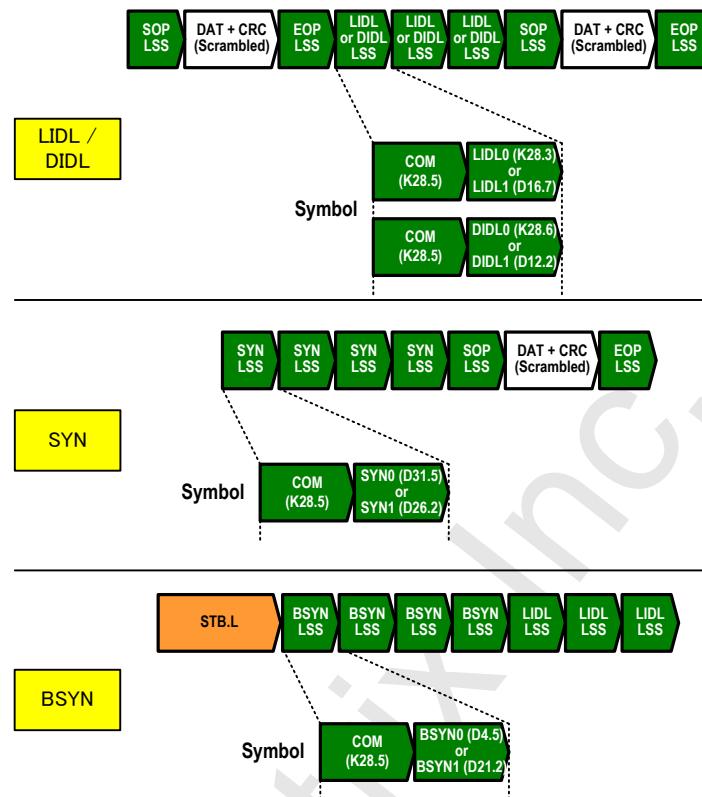
$$\text{LIDL}_0 / \text{LIDL}_1 = \text{K28.3} / \text{D16.7}$$

$$\text{DIDL}_0 / \text{DIDL}_1 = \text{K28.6} / \text{D12.2}$$

$$\text{SYN}_0 / \text{SYN}_1 = \text{D31.5} / \text{D26.2}$$

$$\text{BSYN}_0 / \text{BSYN}_1 = \text{D4.5} / \text{D21.2}$$

To ensure randomness of each symbol selection, for example, the selection can be controlled by a pseudo random bit stream generator.

**Figure 5-42 : LSS Scrambling****Application Note:**

For the purpose of verification, both Host and Device can have a register in Vendor Unique Register (described as VU\_REG in Section 6.2.1) in order to disable scrambling for contents of packet.

**5.7.4.4 Example of Scrambling Calculation**

Let the input packet containing 5 bytes be as follows (DATA packet with 3 byte Payload).

```

0xB1 : NP = 1, TYP = 011b (DATA), DID = 1
0x00 : SID = 0, TID = 0
0xAA : (Payload0)
0xBB : (Payload1)
0xCC : (Payload2)

```

The output of scrambled data including LSS is as follows.

Transmission order	Packet Data	Code	Scramble pattern	Scrambled Data	Scrambled Code
0	COM	K28.5		COM	K28.5
1	SDB	K28.0		SDB	K28.0
2	COM	K28.5		COM	K28.5
3	SDB	K28.0		SDB	K28.0
4	COM	K28.5		COM	K28.5
5	SOP	K28.1		SOP	K28.1
6	0xB1	D17.5	0xFF	0x4E	D14.2
7	0x00	D0.0	0x17	0x17	D23.0
8	0xAA	D10.5	0xC0	0x6A	D10.3
9	0xBB	D27.5	0x14	0xAF	D15.5
10	0xCC	D12.6	0xB2	0x7E	D30.3
11	PAD	K23.7	0xE7	PAD	K23.7
12	0xFE	D30.7	0x02	0xFC	D28.7
13	0x1E	D30.0	0x82	0x9C	D28.4
14	COM	K28.5		COM	K28.5
15	EOP	K29.7		EOP	K29.7
16	COM	K28.5		COM	K28.5
17	EDB	K27.7		EDB	K27.7
18	COM	K28.5		COM	K28.5
19	EDB	K27.7		EDB	K27.7

Table 5-13 : Example of Scrambling

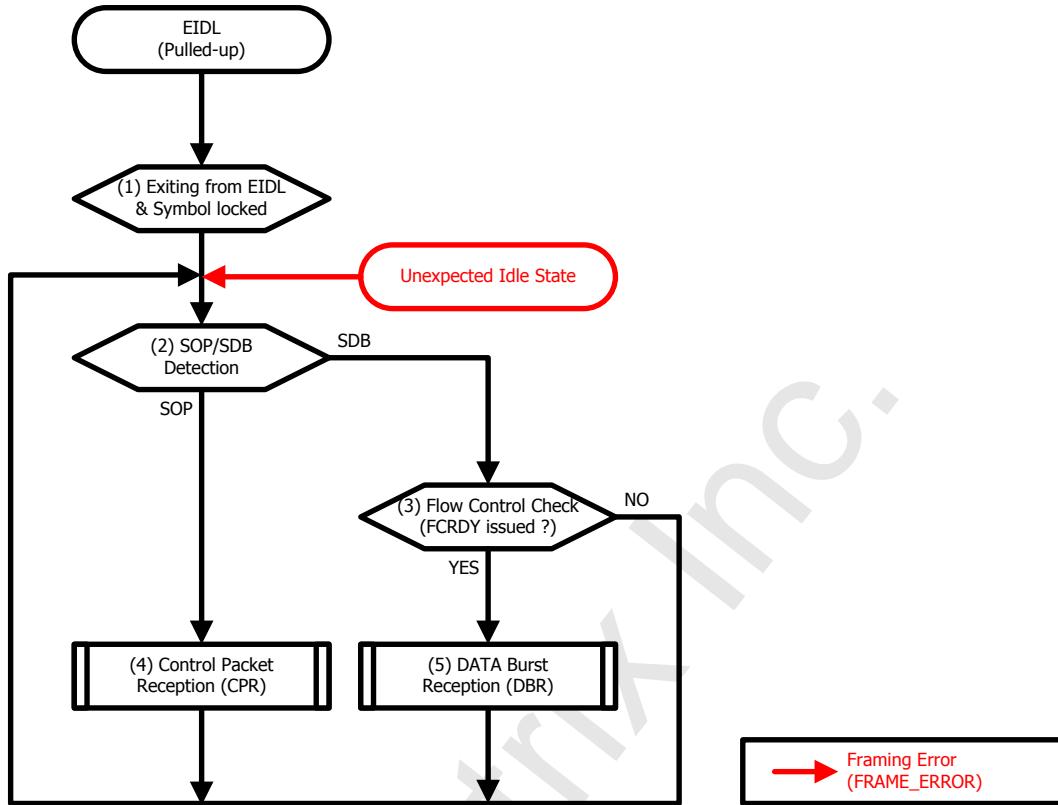
## 5.8 Packet Receiving Flow Chart

### 5.8.1 Overview

This section describes how to handle all received packets in LINK. LINK shall determine whether the received packet needs to be certainly processed or to be discarded in accordance with the rule described below.

### 5.8.2 Top Level Flow Chart

Figure 5-43 illustrates a top level flow chart for control packet or DATA Burst reception.



**Figure 5-43 : Top Level Flow Chart for Starting Packet Reception**

- (1) LINK of receiver side can start receiving a packet only after Rx exits from EIDL and establishes its symbol lock.
- (2) During SOP/SDB Detection step, all incoming symbols are discarded until SOP LSS or SDB LSS is detected. If the receiver side detects at least one of the two SDB LSSes, it moves to Flow Control Check step (3). On the other hand if it detects SOP LSS, it moves to Control Packet Reception (CPR) step (4) and the following packet is regarded as a control packet.
- (3) During Flow Control Check step, the receiver side needs to check if Flow Control handshake is already completed (FCRDY has been issued). If that condition is satisfied (YES), each of the following packets before receiving EDB LSS can be received as a DATA packet in DATA Burst Reception (DBR) step (5), and all of them form a DATA Burst. In this step, the receiver side only considers the packet whose DID is the same as its own Node ID. For, the DATA Burst whose destination is other Device are bypassed in the CPR step (4) based on the rule of DATA Burst Streaming described in Section 5.6.3.

Detailed flow charts for CPR (4) and DBR (5) are described in Section 5.8.3 and Section 5.8.4 respectively.

LINK of receiver can detect EOP corruption by an unexpected LIDL or EIDL (unexpected Idle State). For EDB corruption, Host and Device can detect EDB corruption as the following method (also refer to Section 0 for timing parameters such as Tfcrdy\_edb).

- Host detects EDB corruption by Tfcrdy\_edb timeout in read transaction, or Tedb\_stat timeout in write transaction.
- Then Host transmits LIDL or EIDL according to the setting of "Power Control Mode in Active.Control State".

- Device receives the unexpected Idle State by receiving the LIDL or EIDL mentioned above, and detects EDB corruption as a result.

When receiving the unexpected Idle State, the receiver side regards it as Framing Error (FRAME\_ERROR) and executes step (2) again. Moreover, it may notify errors detected in DBR step to the DATA initiator by STAT MSG when exiting from DBR step.

### 5.8.3 Control Packet Reception Flow Chart

Figure 5-44 illustrates a Control Packet Reception Flow Chart. Note that the handlings of conditions not described in this section are implementation matter.

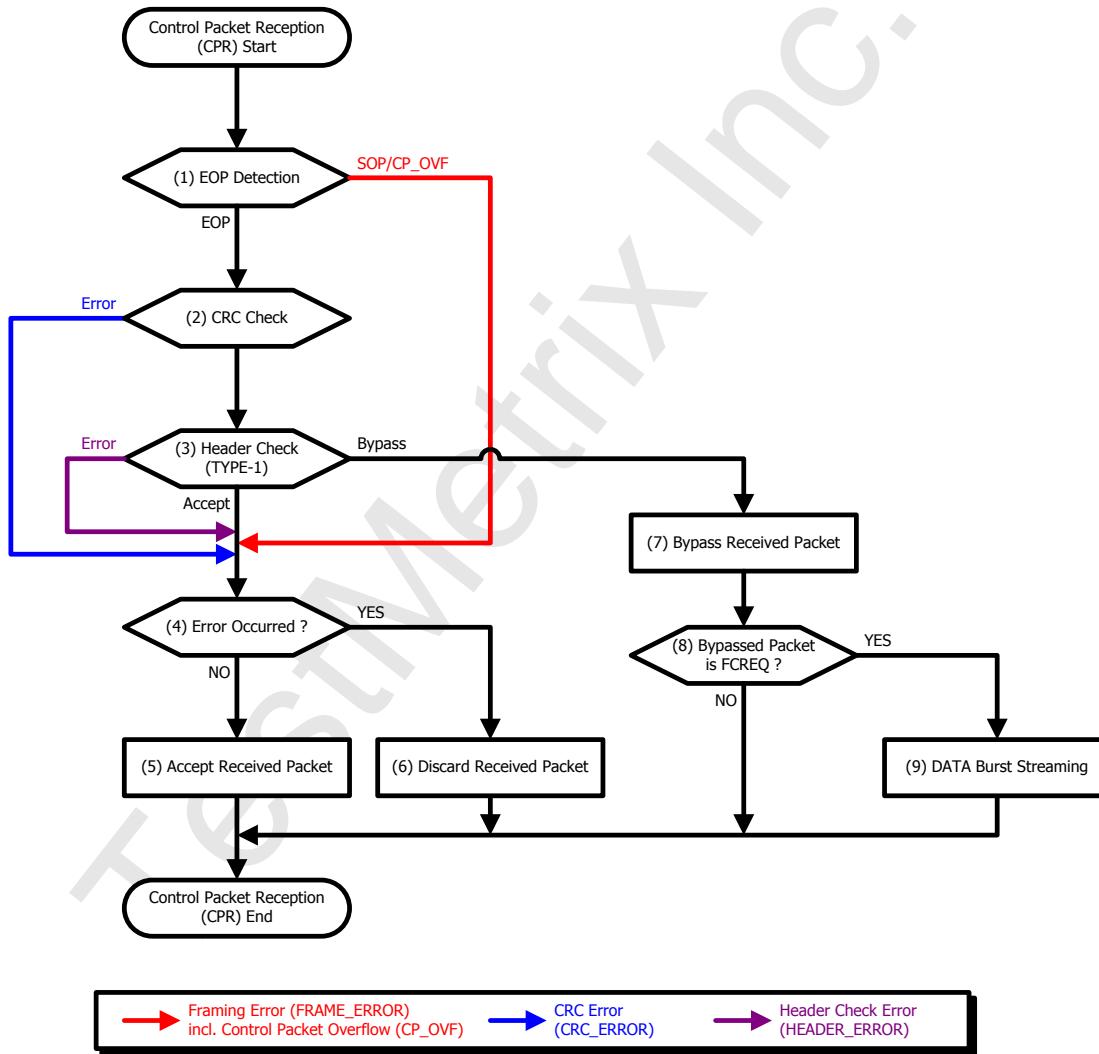


Figure 5-44 : Control Packet Reception Flow Chart

- (1) LINK of receiver side starts to buffer incoming byte stream until it detects EOP LSS and calculates its CRC. When the buffering size exceeds maximum length of control packet, it causes control packet overflow (CP\_OVF). As CP\_OVF is typically occurred as a result of EOP corruption, it is categorized as FRAME\_ERROR.
- (2) In this step, calculated CRC is compared with CRC field of the received packet. If the receiver side fails CRC check, (in other words, it detects CRC\_ERROR), it will discard the packet in step

- (6). Otherwise, it can move to Header Check (TYPE-1) step (3) because Header of the packet is reliable.
- (3) In this step, Header of the packet is analyzed in accordance with the prioritized conditions shown in Table 5-14. Note that errors detected during Header Check are categorized as ILLEGAL\_HEADER\_ERROR.
- (4) The receiver side checks error occurrence from step (1) to (3) which corresponds to any of FRAME\_ERROR, CRC\_ERROR, or ILLEGAL\_HEADER\_ERROR.
- (5) If it does not detect any errors in step (4), it accepts the packet.
- (6) Otherwise, it discards the packet in this step.
- (7) The result of Header Check (step (3)) is "Bypass in LINK" (refer to Table 5-14), it bypasses the received packet.
- (8) If the bypassed packet is not FCREQ MSG, it completes CPR.
- (9) Otherwise, it transfers the received packet with DATA Burst streaming described in 5.6.3.

Prioritized Condition Number	Header of Received Packet			Results of Header Check			Note
	TYP	SID	DID	Accept	Bypass in LINK	Error	
0	-	At least either one is unused				✓	Host shall remove a packet which has unused ID.
1	DATA	-	-			✓	DATA packet is unexpected in CPR.
2	CCMD	SID = DID		✓			Broadcast CCMD is bypassed in CM-TRAM.
3	Other than DATA	= Own ID	-			✓	Issued packet is not received in all other Devices.
4	Other than DATA	-	!= Own ID		✓		Packet is targeted to other Device.
5	Other than DATA	-	= Own ID	✓			Packet is targeted to own Device.

**Table 5-14 : Header Check (TYPE-1)**

If LINK receives SOP during CPR for any packets, it discards the former packet and starts again the CPR flow for the packet following the recently received SOP.

#### 5.8.4 DATA Burst Reception Flow Chart

Figure 5-45 illustrates a DATA Burst Reception Flow Chart. Note that the handlings of conditions not described in this section are implementation matter.

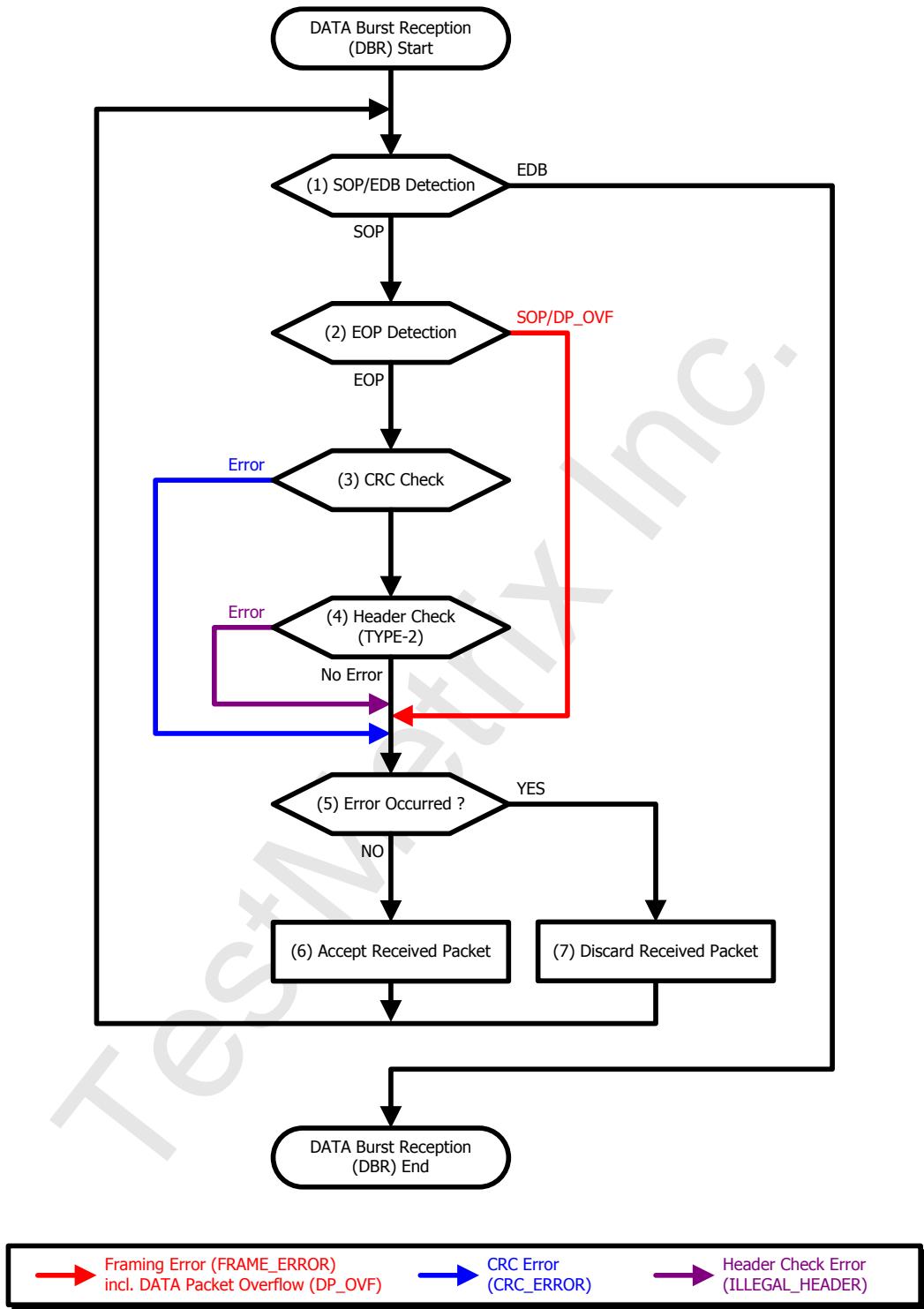


Figure 5-45 : DATA Burst Reception Flow Chart

- (1) LINK of receiver side starts detecting SOP or EDB LSS. If at least one EDB is detected in this step, then DBR is completed.
- (2) If SOP is detected in step (1), LINK of receiver side starts to buffer incoming byte stream until it detects EOP LSS and calculates its CRC. When the buffering size exceeds MAX\_BLKLEN

defined in CFG\_REG, it causes DATA packet overflow (DP\_OVF). As DP\_OVF is typically occurred as a result of EOP corruption, it is categorized as FRAME\_ERROR.

- (3) In this step, calculated CRC is compared with CRC field of the received packet. If the receiver side fails CRC check, (in other words, it detects CRC\_ERROR), it discard the packet in step (7). Otherwise, it can move to Header Check (TYPE-2) step (4) because Header of the packet is reliable.
- (4) In this step, Header of the packet is analyzed in accordance with the prioritized conditions shown in Table 5-15. Note that errors detected during Header Check are categorized as ILLEGAL\_HEADER\_ERROR. Note that DATA packet whose destination is other Device shall be handled as ILLEGAL\_HEADER\_ERROR because it shall be bypassed as the rule of DATA Burst Streaming shown in step (9) of CPR.
- (5) The receiver side checks error occurrence from step (2) to (4) which corresponds to any of FRAME\_ERROR, CRC\_ERROR, or ILLEGAL\_HEADER\_ERROR.
- (6) If it does not detect any errors in step (5), it accepts the packet.
- (7) Otherwise, it discards the packet in this step.

Prioritized Condition Number	Header of Received Packet			Results of Header Check			Note
	TYP	SID	DID	Accept	Bypass in LINK	Error	
0	Other than DATA	-	-			✓	Control packet is unexpected in DBR in UHS-II Addendum Version 1.00.
1	DATA	-	!= Own ID			✓	DATA packet shall be bypassed by DATA Burst Streaming in CPR.
2	DATA	-	= Own ID	✓			Issued packet is not received in all other Devices.

Table 5-15 : Header Check (TYPE-2)

## 5.9 Details of Boot Code Loading

It is optional to have a Boot Device in the UHS-II system. But all Devices shall support state transitions and packet bypassing considering Boot Code Loading. Moreover, the system can include at most one Boot Device.

### 5.9.1 LINK State Transition during Wakeup including Boot Device (Ring Connection)

In this section, explanation of Wakeup in Ring topology is based on Figure 5-46. In this example, Device#2 is supposed to the Boot Device.

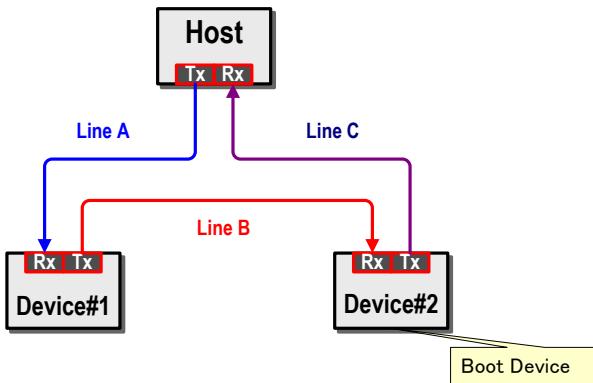
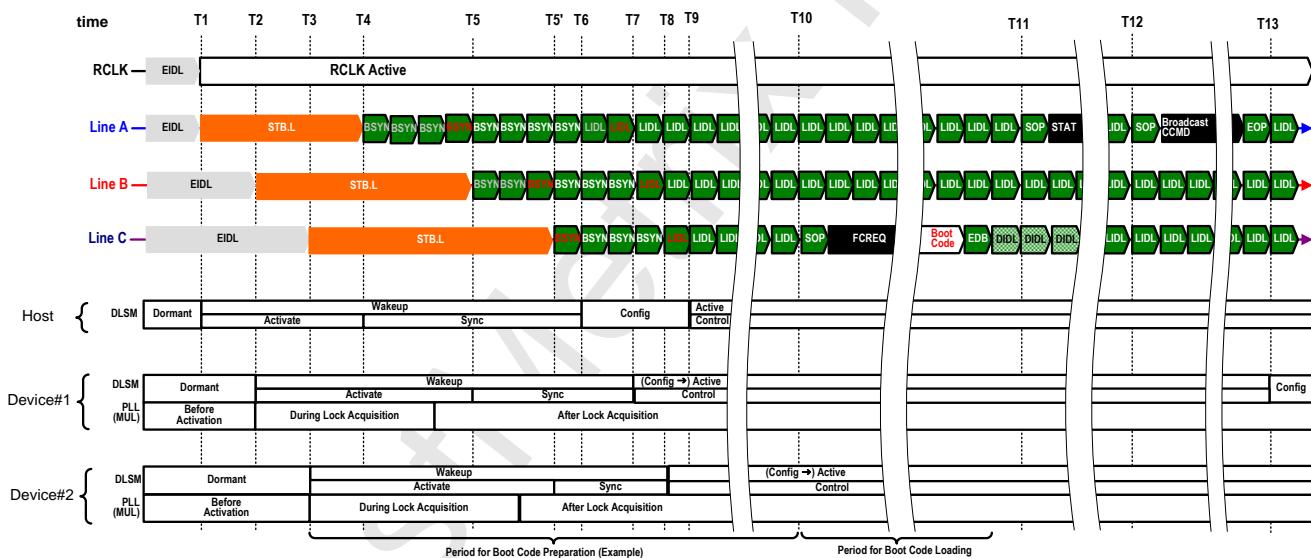
**Figure 5-46 : Ring Connection Including a Boot Device**

Figure 5-47 illustrates a LINK state transition during Wakeup for Ring Connection including Boot Device described Figure 5-46., Only FCREQ is appeared in Figure 5-47, but in fact, flow control described in Section 5.5 takes place during Boot Code transmission.

**Figure 5-47 : LINK State Transition during Wakeup when Including a Boot Device**

T1: LINK of Host starts to provide RCLK, drives Tx to STB.L. As a result, DLSM of Host transits to Wakeup.Activate state.

T2: When Device#1 receives STB.L, it starts PLL lock acquisition and responds by driving Tx drives to STB.L. Note that Device#1 shall respond STB.L within Teidl\_stb. As a result, DLSM of Device#1 transits to Wakeup.Activate state.

T3 When Device#2 (Boot Device) receives STB.L, it starts PLL lock acquisition and may also start Boot Code Preparation. Then it responds by driving Tx drives to STB.L and enters to Wakeup.Activate state. Note that Device#1 shall respond STB.L within Teidl\_stb.

T4: If Host receives STB.L LINK of Host starts to send BSYN LSS immediately for LINK synchronization and Boot Code Loading direction, and its state transits to Wakeup.Sync.

T5: If Device#1 successfully receives BSYN LSS after PLL lock, Device#1 starts to send BSYN LSS to Device#2 and its state transits to Wakeup.Sync. Note that Device#1 shall complete PLL lock within Tactivate after transitioning to Wakeup state.

T5': Same as T5' for Device#2.

T6: If Host can receive BSYN LSS from Device#2, it makes DLSM to Config (not Active because it has

not received LIDL or EIDL yet), and it starts to send LIDL LSS.

T7: If Device#1 successfully receives LIDL LSS, it starts to send LIDL LSS within Tlidl\_lidl. Moreover, it shall set "Config Completion" to 1 and "Power Control Mode in Active.Control State" to 0 respectively before sending LIDL. As a result, its DLSM transits to Active.Control state.

T8: If Device#2 successfully receives LIDL LSS, it starts to send LIDL LSS within Tlidl\_lidl. Moreover, it shall set "Config Completion" to 1 and "Power Control Mode in Active.Control State" to 0 respectively before sending LIDL. As a result, its DLSM transits to Active.Control state.

T9: Host shall set "Config Completion" to 1 and "Power Control Mode in Active.Control State" to 0 respectively by receiving LIDL. As a result, if Host successfully receives LIDL LSS, its DLSM transits to Active.Control state."

T10: When Device#2 completes Boot Code Preparation, it loads a temporal Node ID for Boot Code Loading (which is one of numbers from 1 to 14 and preset by system designer) and sends FCREQ to start Flow Control for transmitting Boot Code to Host. Note that Boot Device shall send FCREQ within Tlidl\_freq\_boot after transmitting the first LIDL LSS.

T11: When Host receives the final Boot Code from Device#2, Host transmits STAT for the final DATA Burst (Boot Code).

T12: Host issues broadcast write CCMD to set "Config Completion" to 0 for all Devices and Host.

T13: When Device#1 receives the broadcast CCMD mentioned above, it makes DLSM to Config state before transmitting the command to Device#2. Note that also Device#2 and Host execute the same operation when receiving the broadcast CCMD.

During Wakeup state, Host can transmit either SYN or BSYN LSS alternatively depending on execution of Boot Code Loading or not.

### 5.9.2 Protocol for Boot Code Transmission

Boot Code is transmitted from Boot Device to Host with similar manner using Flow Control, but differences are as follows.

- There is no CMD-RES handshake, so the trigger of Boot Code transmission is done by sending FCREQ from Boot Device.
- During the Boot Code transmission, Node ID for Host and Non-boot Device are 0 and 15 respectively. On the other hand, that for Boot Device is assigned a value from 1 to 14 as a temporal Node ID preset by system designer. Such Node IDs for Device are cleared and set again by Enumeration process.
- NP is 1 and TID is 0 for all MSG and DATA packets during Boot Code Loading.

Parameters for Boot Code transmission are described in Table 5-16. For the recommended values, Host may use optimized values for Boot Code Loading between specific Host and Boot Device.

Parameter	Value
Block Length (MAX_BLKLEN)	512 bytes (mandatory)
N_FCU	1 (recommended)
MAX_RETRY_NUM	3 (recommended)

Table 5-16 : Parameters for Boot Code Transmission

If Host detects errors from DATA Burst of Boot Code, DATA Burst retry also takes place by notifying errors with STAT MSG. Furthermore, CCMD cannot be issued until Boot Code Loading completes.

## 6. Transaction Layer Specification

The details of UHS-II protocol including packet format, Configuration, state machine, initialization and flow control are described in this chapter.

### 6.1 Transaction Layer Overview

Figure 6-1 shows the overview of Transaction Layer.

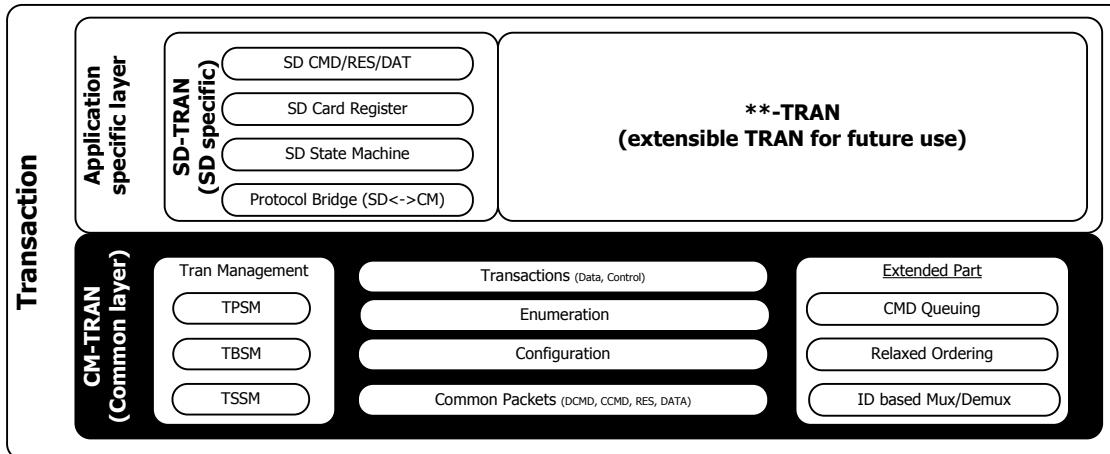


Figure 6-1 : Transaction Layer Overview

The key features of Transaction Layer are defined as follows:

- **New packet based protocol considering Legacy SD compatibility**
  - ID based routing for multiple device connectivity
  - CM-TRAN for common architecture between Host and Device

Transaction Layer consists of two sub-layers called CM-TRAN (lower sub-layer) and application specific layer including SD-TRAN (upper sub-layer). This layering is intended to define the common part of TRAN (CM-TRAN) between Host and Device. As a result, the same CM-TRAN can be used in both Host and Device side.

CM-TRAN provides basic functions to realize transactions on UHS-II native protocol.

CM-TRAN components are the following;

- **Generating UHS-II common packets and processing**
  - Configuration mechanism
  - Transaction management supporting multiple device connection
  - Future extension support (e.g. CMD Queuing)

CM-TRAN is also defined to be the common sub-layer between all application specific layers in order to realize UHS-II specific functions (e.g. multiple device connection, CMD Queuing, etc.) with application specific protocol.

For example, in Figure 6-1, CM-TRAN can provide SD protocol with a CMD Queuing feature as a future extension.

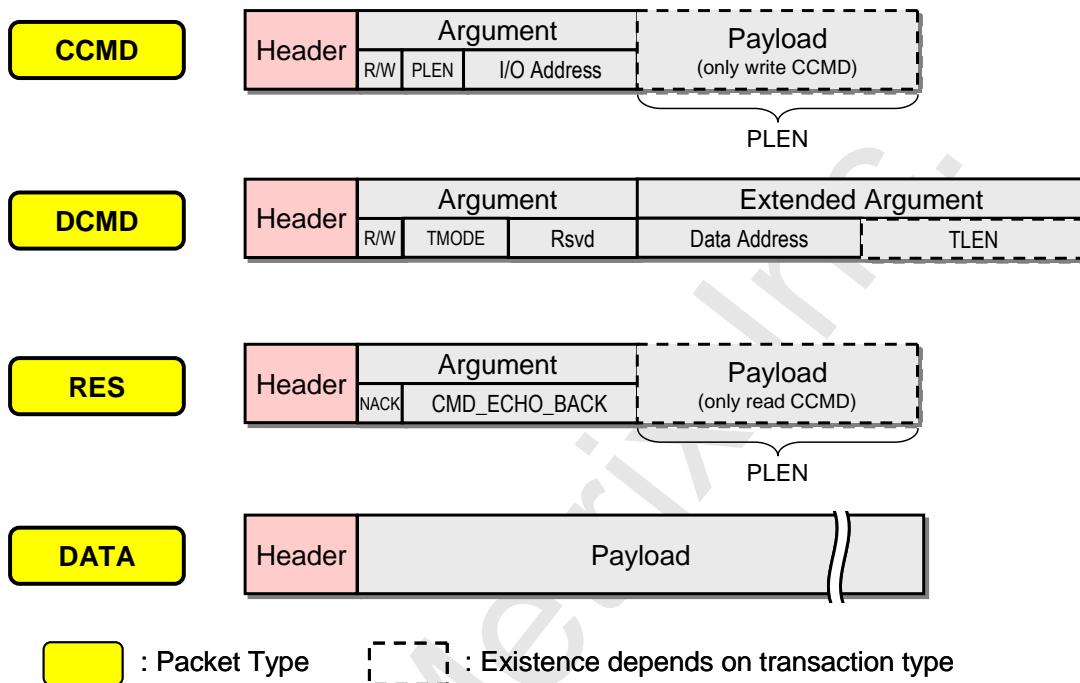
SD-TRAN is an application specific layer for compatibility with SD protocol and preserves the same state machine and registers as Legacy SD protocol. SD-TRAN works as a protocol bridging between Legacy SD and UHS-II native protocol. (Refer to Chapter 7 for details of SD-TRAN.)

Other application specific layers (\*\*-TRAN) can be defined for future extension.

In Chapter 6, the details of CM-TRAN are presented.

### 6.1.1 Packet Types and Format Overview

Figure 6-2 illustrates the Transaction Layer Packet (TLP) types and format overview.



**Figure 6-2 : TLP Format Overview**

In Transaction Layer, four TLP types are defined to realize Legacy SD-compatible protocol and new functions of UHS-II native protocol.

- CCMD (Control CMD): control command packet for accessing to control registers in I/O space
- DCMD (Data CMD): data command packet for transferring data
- RES (Response): response packet associated with CCMD or DCMD
- DATA (Data payload): packet for data transmission

TLP consists of Header, Argument and Payload.

Each type of TLP shall have a common "Header". Header includes ID fields for packet identification and routing information. "Argument" is used for setting supplementary information such as data length (PLEN, TLEN), address information (I/O address, data address) and other information exchanged between Host and Device (TMODE). Only DCMD has "Extended Argument" for setting more information about data length and address. "Payload" is the field for setting data payload to be transmitted.

Argument in CCMD includes read/write flag, I/O address and payload length (PLEN) field. In the case of write CCMD, PLEN represents the length of write data which is assigned in Payload of CCMD. In the case of read CCMD, PLEN basically represents the length of read data which is assigned in Payload of the following RES.

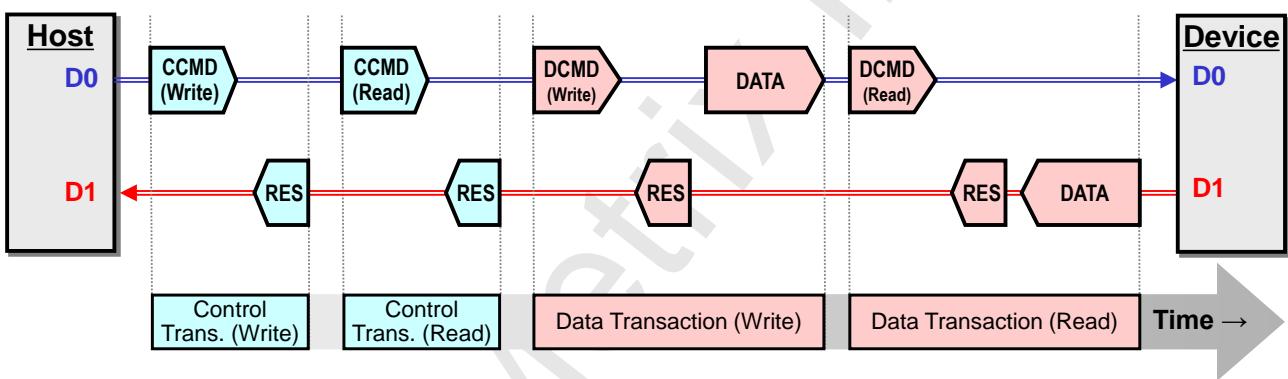
Argument in DCMD includes read/write flag and transfer mode (TMODE) for representing detailed transfer settings such as Length Mode (TLEN is specified or not), TLEN Unit Mode (Block Mode or Byte Mode), etc.

Extended Argument includes transfer length (TLEN) field if Length Mode in TMODE is set to "TLEN is specified". TLEN represents the total length of data to be transmitted by a DCMD.

Extended Argument in DCMD also includes data address (DADR). The unit of data address is specified in Data Access Mode (DAM) in TMODE field. DAM also specifies which address space is to be accessed (refer to DAM explanation in Section 6.2.2.4).

Argument in RES is set to the same value as Argument in the corresponding CMD except read/write flag (command echo back). NACK field shows whether the associated CMD has an error or not. Only the case of CCMD read transaction, Payload field in RES exists and its size is shown by PLEN.

Figure 6-3 shows the basic concept of control transaction and data write/read transaction sequence.



**Figure 6-3 : Control Transaction and Data Transaction Sequence**

The sequences of control transaction and data transaction are defined as follows;

- **Control Transaction:** CCMD -> RES (without DATA packet)
  - Broadcast control transaction does not bring RES.
- **Data Transaction:** DCMD -> RES -> DATA

Control transaction is performed for accessing to UHS-II I/O Registers such as Configuration Register, Command Register and so on, and consists of CCMD from Host and RES from Device. Note that broadcast control transaction does not accompany RES, and the transaction completes when Host receives broadcast CCMD. Special CCMDs such as FULL\_RESET or TRANS\_ABORT are defined in Command Register (refer to Section 6.2.12).

Data transaction is performed for transferring data, and consists of DCMD from Host, RES from Device and DATA from Host or Device. Flow control shall be executed during data transaction.

After issuing a CMD, Host shall not issue all types of packet until RES is received

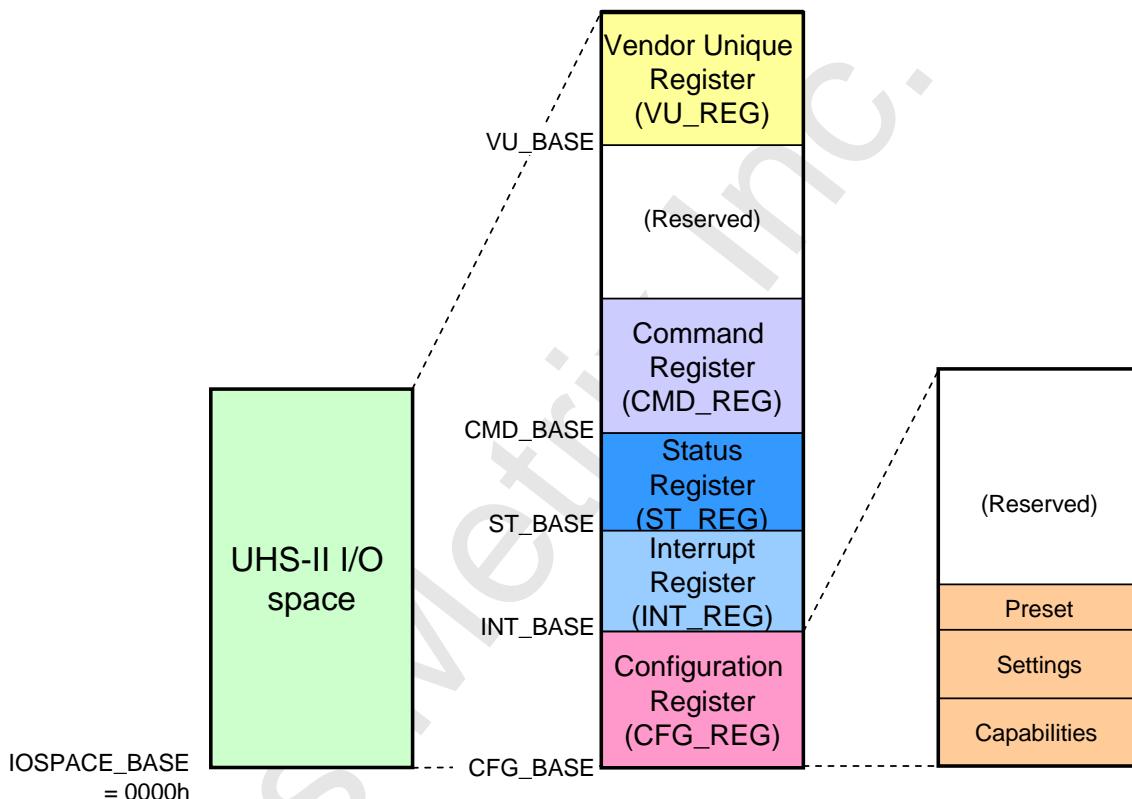
## 6.2 Transaction Layer Protocol

### 6.2.1 UHS-II I/O Space and Memory Address Space

Two types of address spaces are defined.

- **UHS-II I/O space:** Address space for UHS-II I/O Registers expressed by 14bit address number.
- **Memory address space:** Logical address for the memory Device.

Figure 6-4 shows the layout of UHS-II I/O space.



**Figure 6-4 : UHS-II I/O Space Layout for Device**

UHS-II I/O space consists of Configuration Register (CFG\_REG), Interrupt Register (INT\_REG), Status Register (ST\_REG), Command Register (CMD\_REG) and other areas including Vendor Unique Register (VU\_REG). Host can access to the registers described below only by a CCMD.

- Configuration Register (CFG\_REG): Register to assign device-dependent capabilities and determined operating settings during Configuration.
- Interrupt Register (INT\_REG): Register for realizing interrupt.
- Command Register (CMD\_REG): Register to assign UHS-II CCMDs (e.g. reset, abort, etc.)
- Vendor Unique Register (VU\_REG): Register to be defined by vendors individually.

Register area indicated by "Reserved" means that it is initialized to zero and writing operation to them is ignored. The followings are Device behavior when accessed to its Reserved bit including bits inside CMD\_REG.

- **P2P CCMD Read:** Device shall issue RES with NACK=0 and its Payload field corresponding to the reserved bit is set to 0.
- **P2P CCMD Write:** Device shall issue RES with NACK=0 and value of reserved bit is not changed.

- **Broadcast CCMD Write:** Device shall forward broadcast CCMD to the next node, and value of reserved bit is not changed.

Table 6-1 shows the map of UHS-II I/O space. Offset means the relative address based on IOSPACE\_BASE = 0000h.

Offset		Register
Byte address	IOADR	
0000h : 03FFh	000h : 0FFh	Configuration Register (CFG_REG)
0400h : 05FFh	100h : 17Fh	Interrupt Register (INT_REG)
0600h : 07FFh	180h : 1FFh	Status Register (ST_REG)
0800h : 0BFFh	200h : 2FFh	Command Register (CMD_REG)
0C00h : 3BFFh	300h : EFFh	Reserved
3C00h : 3FFFh	F00h : FFFh	Vendor Unique Register (VU_REG)

**Table 6-1 : I/O Address Space Map**

During Configuration, CFG\_REG values are negotiated between Host and Device by CCMDs. Refer to Section 6.2.8 for details of Configuration procedure.

## 6.2.2 Packet Format Details

In this section, msb denotes "most significant bit", lsb denotes "least significant bit" respectively. (Notice that they are different from MSB or LSB.) Moreover, smaller byte in a packet is transmitted first

### 6.2.2.1 Header

Refer to Section 5.2.3 for details of Header structure.

### 6.2.2.2 CCMD

Figure 6-5 illustrates CCMD structure.

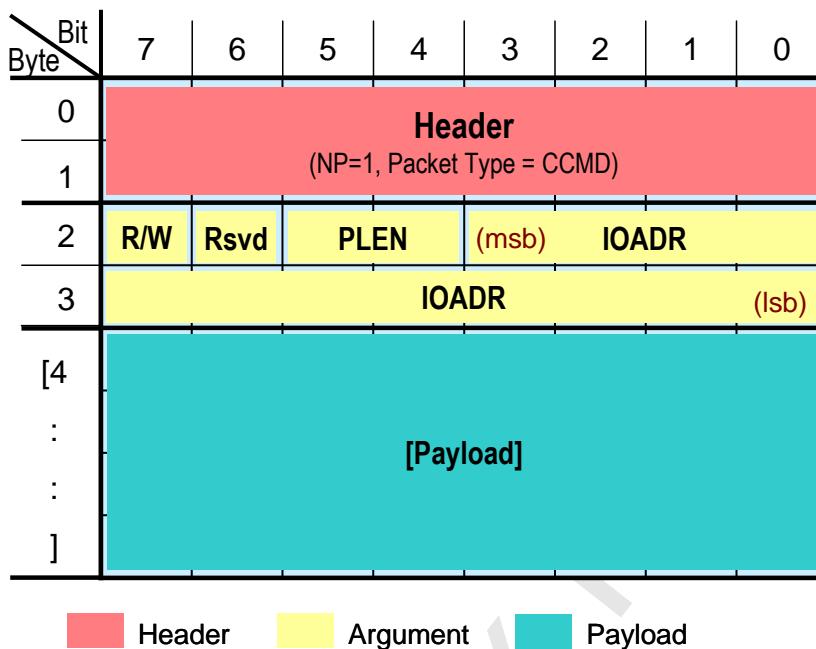
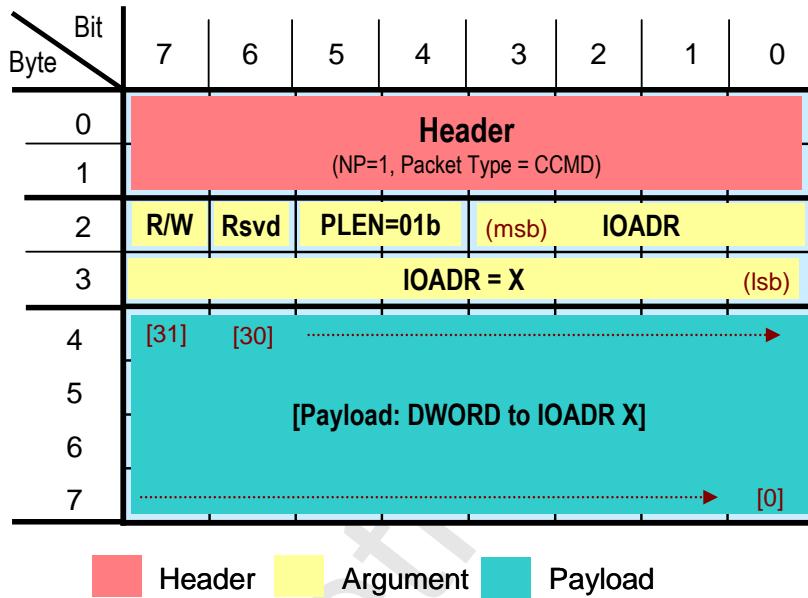
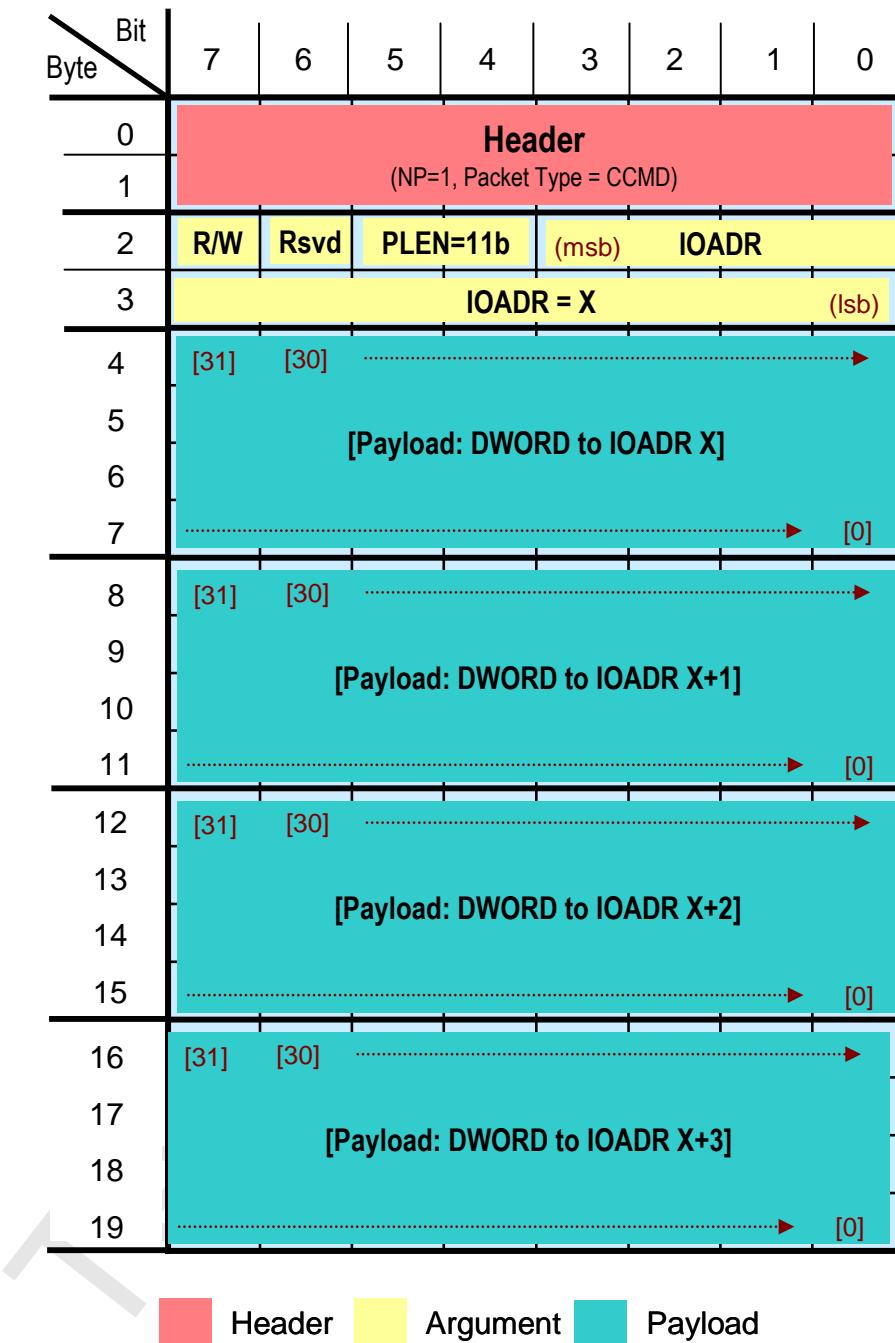


Figure 6-5 : CCMD Format

- **R/W (Read/Write):** Indicator for representing read or write command.
  - 0: Control read command
  - 1: Control write command
- **PLEN[1:0] (Payload Length):** Length of payload field in CCMD or RES.
  - PLEN field represents the length of payload field in CCMD or RES (Definition of PLEN is shown in Table 6-2)
  - In the case of write CCMD (R/W = 1), PLEN represents the length of write data which is assigned in Payload of CCMD.
  - In the case of read CCMD (R/W = 0), PLEN represents the length of read data which is assigned in Payload of the following RES.
- **IOADR[11:0] (I/O Address):** Address of register in UHS-II I/O space accessed by CCMD.
  - The unit of IOADR is 4 bytes. So quadruple of IOADR represents the absolute address in UHS-II I/O space.
  - It is transmitted in msb first, lsb last.
- **Payload:** Write data included with CCMD.
  - The length of payload field is assigned in PLEN.
  - In the case of read CCMD (R/W = 0), Payload field does not exist.
  - In the case that PLEN is set to "00b" (payload length is 0 byte), Payload field does not exist.
  - The Payload field is divided into a unit of DWORD (4byte data), and the transmission order within a DWORD is big endian. Refer to Figure 6-6 and Figure 6-7 for details of the transmission order of Payload. In these figures, bracketed numbers denote the bit order within a DWORD.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

PLEN[1:0]	Payload Length
00b	0 byte
01b	4 bytes
10b	8 bytes
11b	16 byte

**Table 6-2 : Definition of PLEN****Figure 6-6 : Transmission Order of Payload in CCMD (PLEN = 01b)**



**Figure 6-7 : Transmission Order of Payload in CCMD (PLen = 11b)**

In the case of application specific protocol (NP = 0), the definition of payload field existence may be different from the case of native protocol (NP = 1). Refer to Section 7.2.1.1 for details of CCMD format for SD application.

### 6.2.2.3 Broadcast CCMD

Broadcast CCMD operates to all Devices on the bus. On the other hand, CCMD that operates to a specified Device shown by DID is P2P CCMD.

In case of broadcast commands each Device may either transfer commands transparently (e.g. GO\_DORMANT\_STATE) or make some modifications to the continuing command to the following Node (e.g. ENUMERATE).

Features of broadcast CCMD are as follows.

- Broadcast CCMD issued by Host is represented as DID = SID = 0. In UHS-II Addendum Version 1.XX, broadcast packet is only permitted whose TYPE is CCMD and DID = SID = 0.
- If R/W = 1, broadcast CCMD writes content in its payload to the address in UHS-II I/O space calculated from IOADR for all connected Devices.
- Basically, broadcast CCMD with R/W = 0 is not available, but INQUIRY\_CONFIG described in Section 6.2.8.3 is admitted as a special case of broadcast read CCMD. In this case, PLEN represents its payload length even if R/W = 0.
- Each Device shall process broadcast CCMD though DID is not equal to its own Node ID, and transmit it to the next Device or Host.
- Broadcast CCMD does not accompany RES. So if Host receives broadcast CCMD, Host shall terminate its transaction.
- If a Device detects some error from broadcast CCMD, it shall not transmit to the next Device or Host. In this case, Host can detect the error by timeout.

Note that the broadcast command behavior is the same for all topologies. In case of Hub topology the Hub shall emulate a Ring topology in a way that the CCMD shall be transferred in a serial manner passing the CCMDs between the Devices through the Hub.

#### 6.2.2.4 DCMD

Figure 6-8 illustrates DCMD structure.

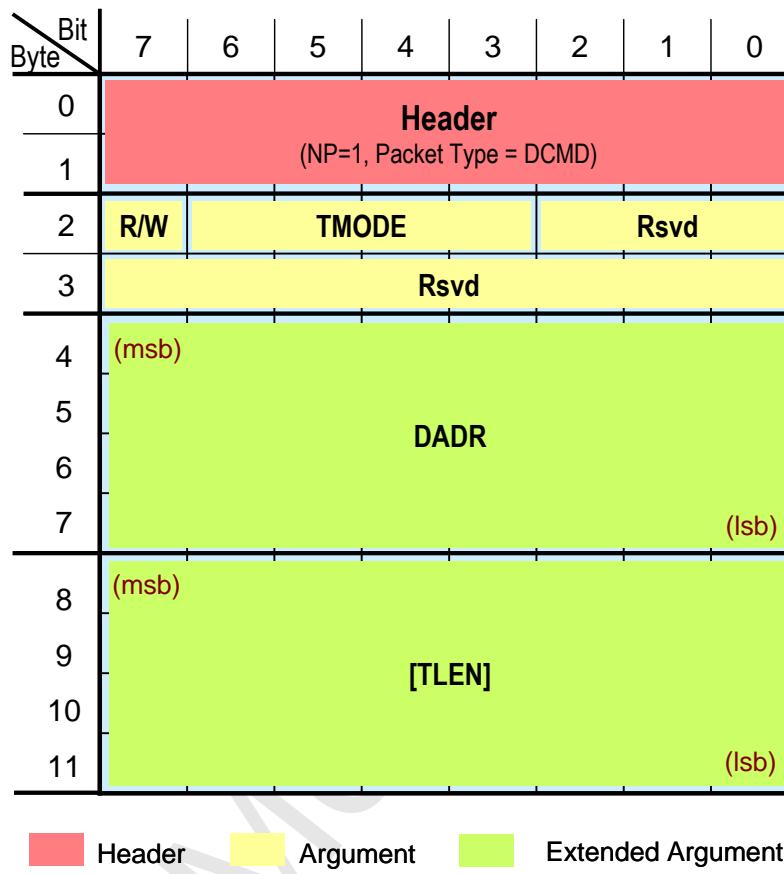


Figure 6-8 : DCMD Format

- **R/W (Read/Write):** Indicator for representing read or write command.
  - 0: Data read command
  - 1: Data write command
- **TMODE[3:0] (Transfer Mode):** Parameter settings for data transaction. (Refer to Figure 6-9 and Table 6-3.)
  - DM (Duplex Mode): Duplex mode selection of data transfer associated with DCMD
  - LM (Length Mode): Indicator whether TLEN is specified or not
  - TLUM (TLEN Unit Mode): Indicator for unit of TLEN
  - DAM (Data Access Mode): Data access mode selection.

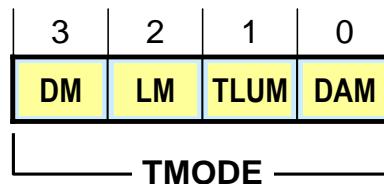


Figure 6-9 : TMODE Parameters

- **DM (Duplex Mode):**
  - 0: FD mode
  - 1: 2L-HD mode
  - If Host issues DCMD with DM = 1 to Device which does not support 2L-HD mode, Device returns RES with NACK = 1.
- **LM (Length Mode):**
  - 0: Data transfer length is not specified (TLEN field does not exist).
  - 1: Data transfer length is specified (TLEN field exists).
- **TLUM (TLEN Unit Mode):**
  - 0: Block Mode
  - 1: Byte Mode
  - In case of TLUM = 1, LM shall be equal to 1. If TLUM = 1 and LM = 0, the DCMD shall be handled as an illegal command and RES (NACK = 1) with ARG\_ERR is responded (refer to Section 6.2.2.6).
  - In case of DM = 1, TLUM shall be equal 0. If DM = 1 and TLUM = 1, the DCMD shall be handled as an illegal command and RES (NACK = 1) with ARG\_ERR is responded.
- **DAM (Data Access Mode):**
  - 0: Data access with incrementing the address by 1. In this case, DADR represents address in memory space address and unit of DADR is a block.
  - 1: Data access to fixed address, which is used in multiple data transfer to the same address like FIFO memory access. In this case, DADR represents address for specified UHS-II I/O address space to support FIFO memory access and unit of DADR is a byte.
  - In the case that DAM = 1 and DADR is not for FIFO memory access, the DCMD shall be handled as an illegal command and RES (NACK = 1) with ARG\_ERR is responded. On UHS-II Addendum Version 1.00, as there are no fields to support FIFO memory access in the UHS-II I/O space, DCMD cannot access to UHS-II I/O space.
- **DADR[31:0] (Data Address):** data address in memory address space or I/O address space accessed by DCMD according to DAM.
  - In the case of DAM=0, DADR is for memory address space and its unit is a block.
  - In the case of DAM=1, DADR is for UHS-II I/O address space and its unit is a byte.
  - It is transmitted in msb first, lsb last.
- **TLEN[31:0] (Transfer Length):** Total length of data transmitted during a data transaction (unit depends on TLUM field setting).
  - In the case that LM = 0 (data transfer length is not specified), TLEN field does not exist.
  - In the case of TLUM = 0 (Block Mode):
 

TLEN field represents the data length within the range of 1 to (4G – 1) blocks.  
If TLEN = 0000000h, it does not affect the data transaction (same as LM = 0).
  - In the case of TLUM = 1 (Byte Mode):
 

TLEN field represents the data length.  
Note that TLEN shall be smaller than or equal to Block Length.  
If TLEN = 0000000h, it is regarded same as LM = 0, and becomes ARG\_ERR as a result.
  - It is transmitted in msb first, lsb last.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

Table 6-3 shows availability of TMODE. Marks in 'Availability' column mean as follows.

- **X:** TMODE is available.
- **-:** TMODE is not available.
- **-(1):** TMODE is not available in UHS-II Addendum Version 1.00. (It is subject to change in the future specification.)

TMODE				Avail-ability	Remark
DM	LM	TLUM	DAM		
0	0	0	0	X	FD mode, No TLEN, Block Mode, Memory Access
0	0	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
0	0	1	0	-	TLEN shall be specified in Byte Mode
0	0	1	1	-	TLEN shall be specified in Byte Mode
0	1	0	0	X	FD mode, TLEN, Block Mode, Memory Access
0	1	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
0	1	1	0	X	FD mode, TLEN, Byte Mode, Memory Access
0	1	1	1	-(1)	DCMD cannot access I/O space in Version 1.00
1	0	0	0	X	2L-HD mode, No TLEN, Block Mode, Memory Access
1	0	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
1	0	1	0	-	TLEN shall be specified in Byte Mode
1	0	1	1	-	TLEN shall be specified in Byte Mode
1	1	0	0	X	2L-HD mode, TLEN, Block Mode, Memory Access
1	1	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
1	1	1	0	-	Byte Mode is not available in 2L-HD mode
1	1	1	1	-	Byte Mode is not available in 2L-HD mode

Table 6-3 : Availability of TMODE

### 6.2.2.5 RES (NACK = 0)

Figure 6-10 illustrates the RES (NACK = 0) structure.

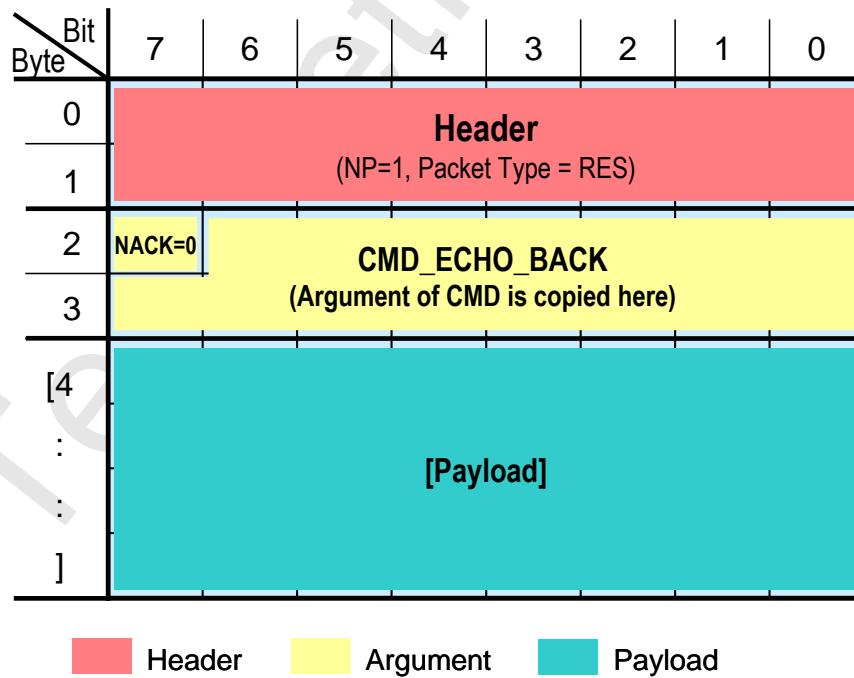


Figure 6-10 : RES (NACK = 0) Format

- **NACK (Negative Acknowledgement):** Indicator whether the corresponding CMD is accepted or not.
  - 0: The corresponding CMD is accepted.
  - 1: The corresponding CMD is rejected.

- In the case of NACK = 0 (CMD is accepted), the requested operation is in execution or waiting for execution.
- In the case of NACK = 1 (CMD is rejected), the requested operation is not in execution (an error has occurred in the corresponding CMD).
- Refer to Section 6.2.2.6 for details of RES with NACK = 1.
- **CMD\_ECHO\_BACK[14:0] (Command Echo Back):** Copied field of CMD Argument.
  - The same values in Argument field are copied from the corresponding CMD (echo back). Specifically, [6:0] in the second byte, and [7:0] in the third byte of CMD packet are copied to the same location of RES packet.
- **Payload:** Read data for control read transaction.
  - The length of payload field is assigned in PLEN of the corresponding read CCMD.
  - In the case that PLEN of the CCMD is set to "00b" (payload length is 0 byte), Payload field does not exist.
  - In the case that write CCMD is issued, Payload field in RES does not exist.
  - In the case that DCMD is issued (data transaction), Payload field in RES does not exist.
  - The Payload field is divided into a unit of DWORD (4byte data), and the transmission order within a DWORD is big endian. Refer to Figure 6-11 and Figure 6-12 for details of the transmission order of Payload. In these figures, bracketed numbers denote the bit order within a DWORD.

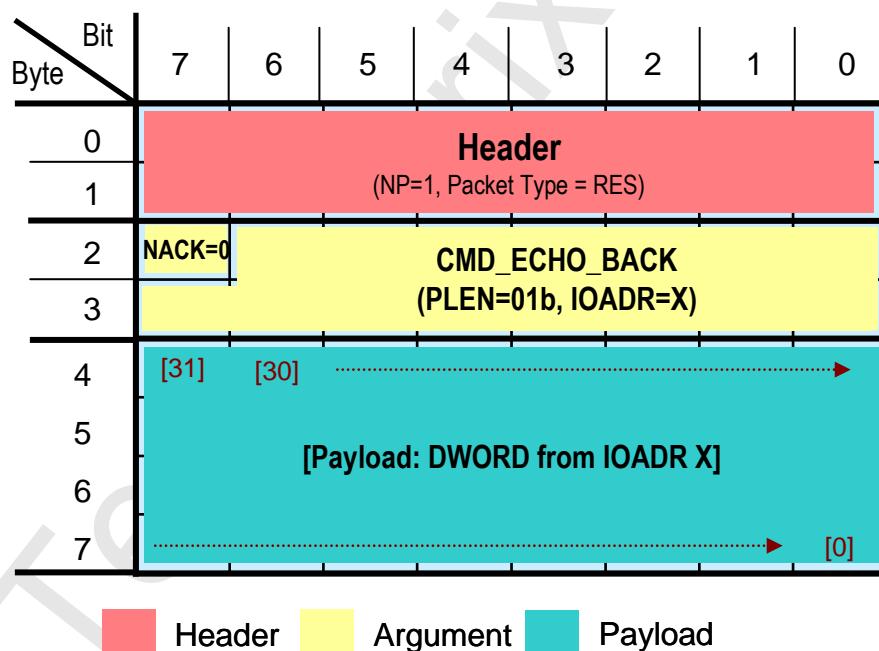
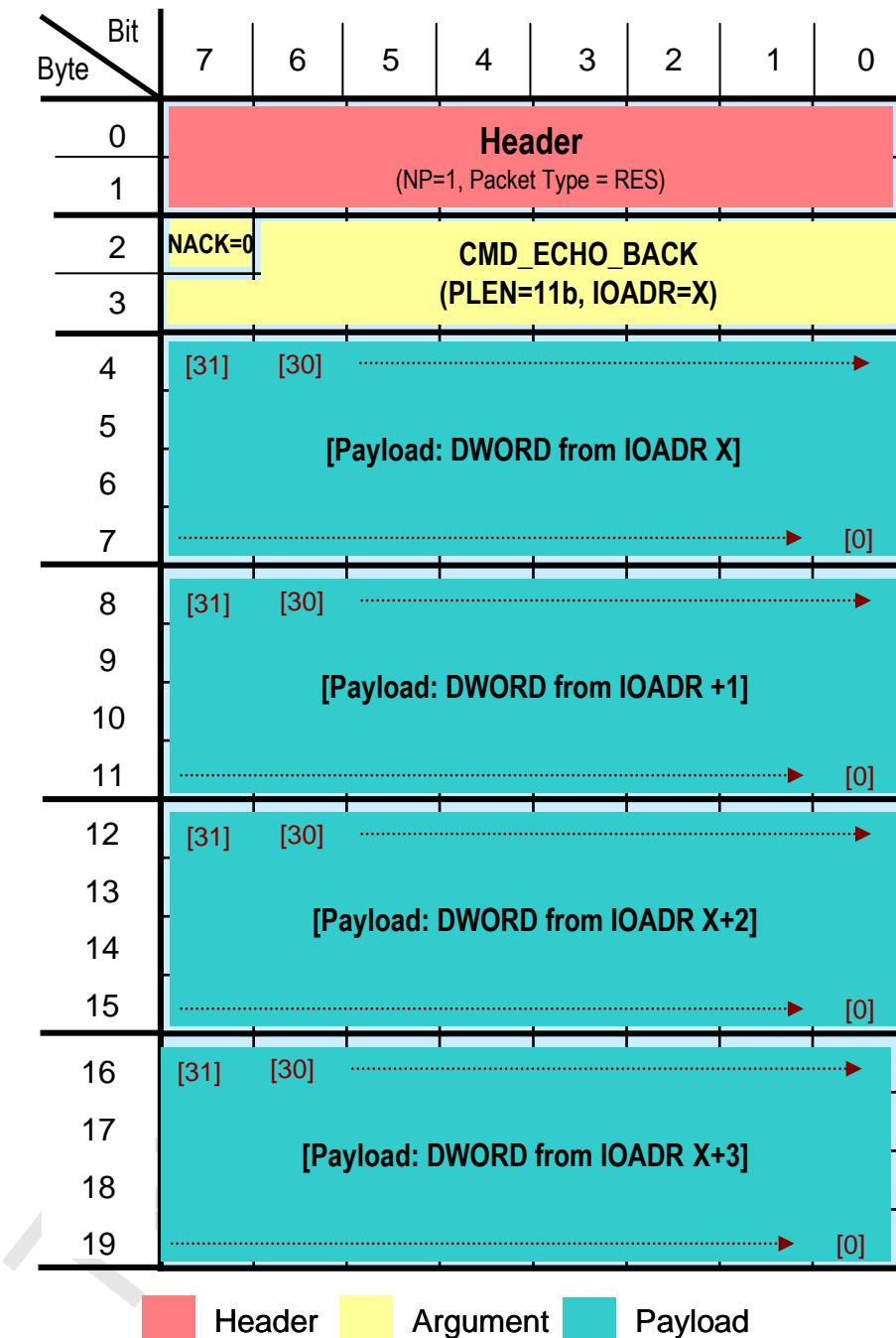


Figure 6-11 : Transmission Order of Payload in RES (NACK = 0, PLEN = 01b)



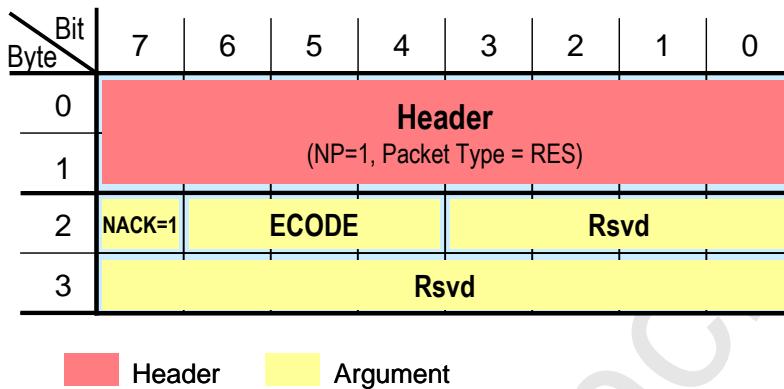
**Figure 6-12 : Transmission Order of Payload in RES (NACK = 0, PLEN = 11b)**

DID field in Header of RES is set to the same value as SID field in Header of the corresponding command. TID field in Header is set to the same value as TID field in Header of the corresponding command.

In the case of application specific protocol (NP = 0), the definition of payload field existence may be different from the case of native protocol (NP = 1). Refer to Section 7.2.1.3 for details of RES format for SD application.

### 6.2.2.6 RES (NACK = 1)

Figure 6-13 illustrates RES (NACK = 1) structure.



**Figure 6-13 : RES (NACK = 1) Format**

- **NACK (Negative Acknowledgement):** Indicator whether the corresponding CMD is accepted or not.
  - NACK = 1 means the corresponding CMD is rejected.
  - In the case of NACK = 1 (CMD is rejected), the requested operation is not in execution (an error has occurred in the corresponding CMD).
- **ECODE[2:0] (Error Code):** Error code to represent error descriptions (refer to Table 6-4).
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

Refer to Section 6.2.15 for details of CMD error sequence.

Table 6-4 shows the error descriptions represented by ECODE. If CMD includes multiple errors, RES with NACK = 1 is generated with the error whose ECODE value is the smallest. For example, when some command is issued at improper state with illegal argument (e.g. illegal address), the ECODE of its RES with NACK = 1 is COND\_ERR.

ECODE		Description
Value	Name	
001b	COND_ERR	Command is issued in any improper states defined in all layers in this specification.
010b	ARG_ERR	At least one of parameters in any of Argument field, Extended Argument field, or Payload field is improper in the CMD.
011b	GEN_ERR	Other errors not belonging to the errors above.
others	Reserved	Reserved

**Table 6-4 : Error Categories and Descriptions**

### 6.2.2.7 DATA

Figure 6-14 illustrates a basic DATA structure.

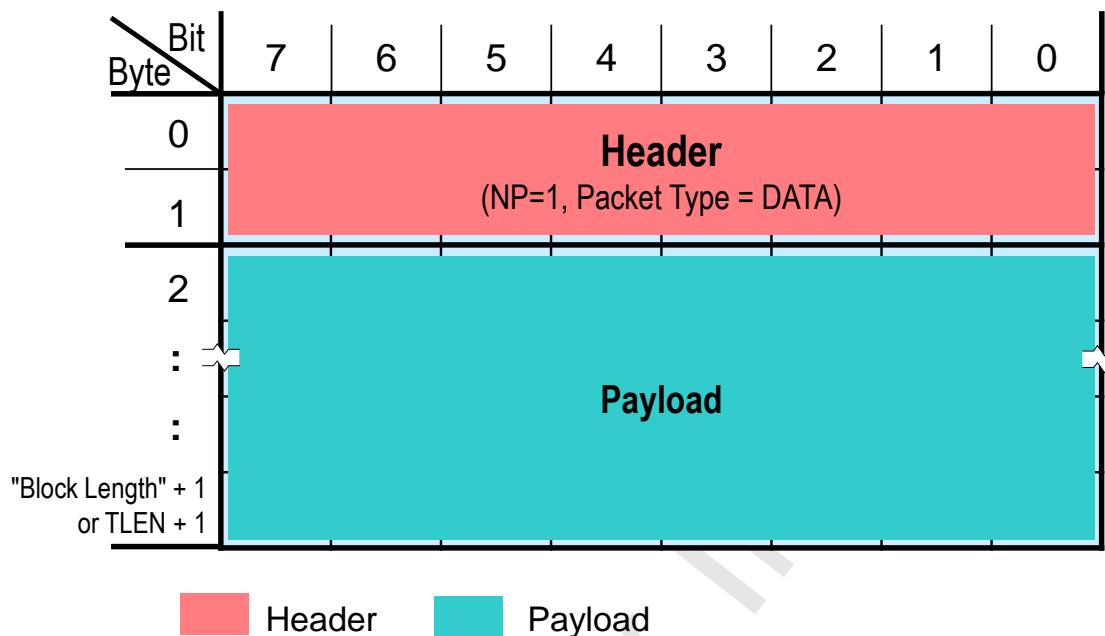


Figure 6-14 : Basic DATA Format

- **Payload:** Data included with DATA.
  - The length of payload is equal to Block Length in Block Mode and TLEN in Byte Mode.
  - It is transmitted in LSB first, MSB last. For the individual byte, it is msb first, lsb last.

#### 6.2.2.8 Operation of Reserved Bits in the Packet

The following table indicates how each Node operates reserved bits in the packet.

Node	Operation
Initiator (both Host and Device)	Reserved bits shall be set to '0' other than in CMD_ECHO_BACK field
Device bypassing control packet	Reserved bits shall be ignored upon reception, and not to be set or cleared upon transmission.
Device handling broadcast packet	Reserved bits shall be ignored upon reception, and not to be set or cleared upon transmission.

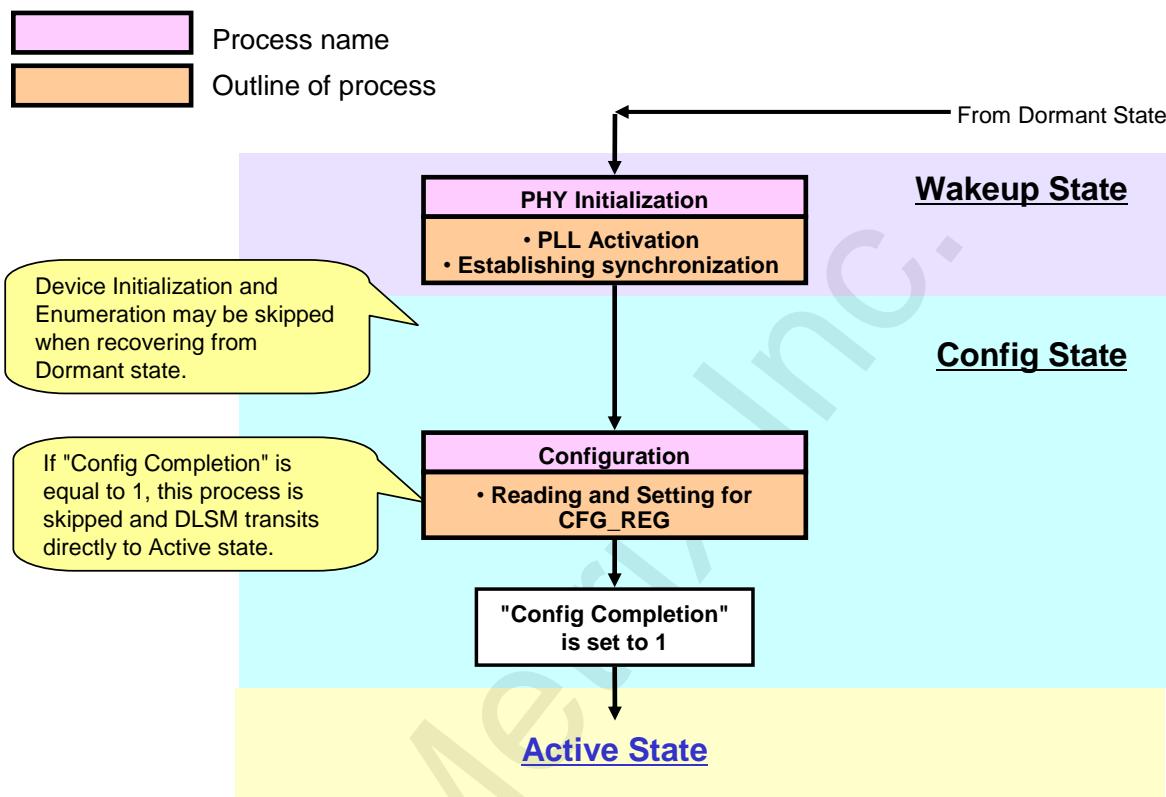
Table 6-5 : Operation for the Reserved Bits in the Packet

Host should use Reserved bits considering the specification versions that all devices that exist in the ring topology.

### 6.2.3 Supplements of UHS-II Initialization

In this section, supplements of UHS-II Initialization are described. Refer to Section 3.5 for the basic specifications.

Figure 6-15 shows UHS-II Initialization flow in case of recovery from Dormant state.

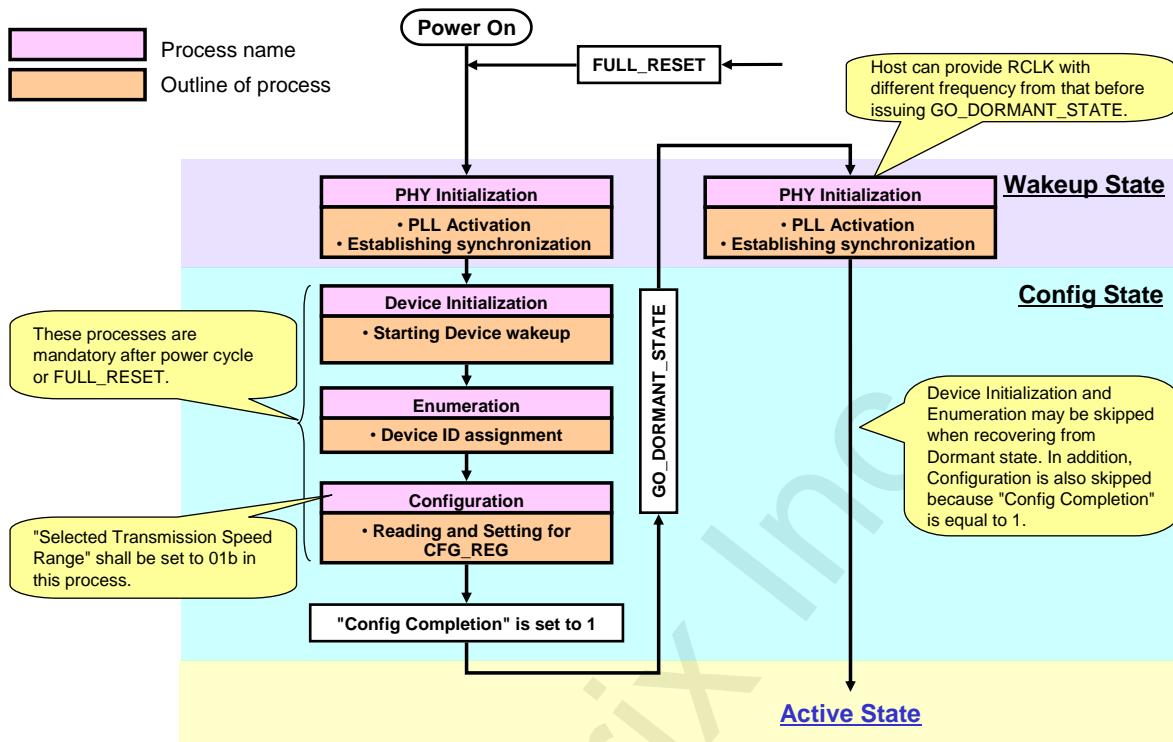


**Figure 6-15 : UHS-II Initialization Flow When Recovery from Dormant State**

If Device receives BSYN LSS after recovering from Dormant State, Device behavior is up to implementation. Note that Host shall not transmit BSYN LSS after recovering from Dormant State.

Both Device Initialization process and Enumeration process may be skipped when recovering from Dormant state, for whole functions of each Device and Node ID. If "Config Completion" is equal to 0, Configuration process can be done, but otherwise, that process is skipped and DLSM transits to Active state.

Figure 6-16 shows an example of Initialization flow in case of using Range B as a transmission speed range (refer to Section 6.2.9.2.5 for more details).



**Figure 6-16 : An Example of UHS-II Initialization Flow (in Case of Using Higher Speed Range)**

Host shall set "Selected Transmission Speed Range" in CFG\_REG to the desire range (01b, in this case) at the Configuration process. After setting "Config Completion" to 1, Host issues GO\_DORMANT\_STATE in order to enable "Selected Transmission Speed Range". Afterwards, it provides RCLK to do PHY Initialization again. Note that frequency of RCLK may be changed during Dormant state only. At the end of PHY Initialization, DLSM transits to Active State where higher speed range is available because "Config Completion" has been already set to 1.

## 6.2.4 Transition to Dormant State

### 6.2.4.1 General

When Device receives GO\_DORMANT\_STATE CCMD, it makes its DLSM transit to Dormant state for interface power saving. During Dormant state, state machines defined in Chapter 6 get back to the initial state. On the other hand, all registers defined in Chapter 6 are kept and some Settings Registers in CFG\_REG are reflected by transitioning to Dormant state (refer to Section 6.2.9.2).

Refer to Section 5.4.3 for the detailed transition to Dormant state.

Figure 6-17 illustrates a format of GO\_DORMANT\_STATE CCMD.

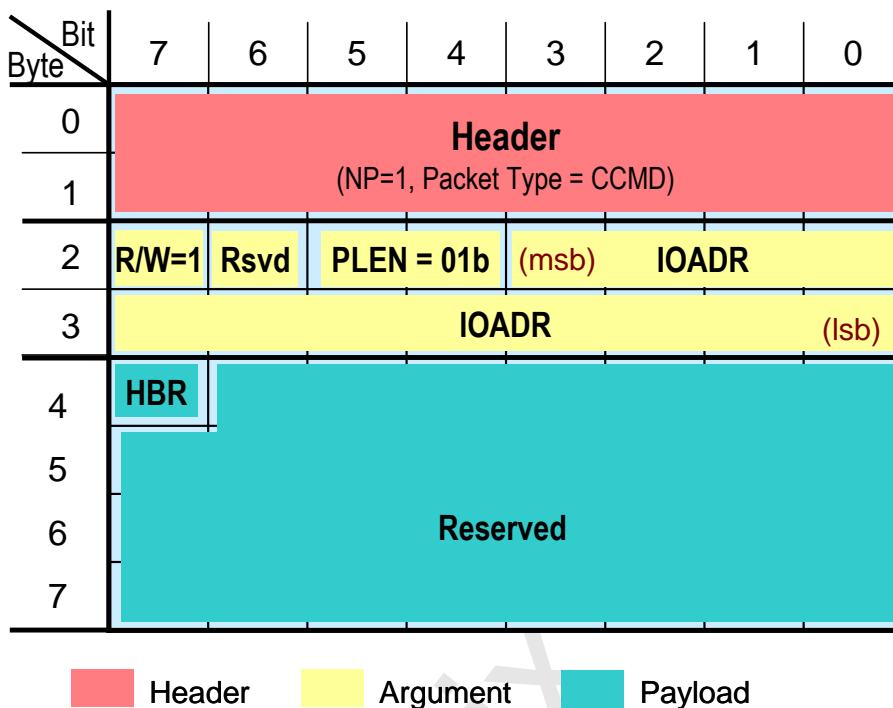


Figure 6-17 : GO\_DORMANT\_STATE CCMD Format

- **HBR (Entry to Hibernate Mode):** This value indicates entry to Hibernate mode (refer to Section 6.2.4.2 for more details). If Host intends to enter to Hibernate mode during Dormant state, it issues GO\_DORMANT\_STATE CCMD with HBR = 1. If Device not supporting Hibernate mode receives GO\_DORMANT\_STATE CCMD with HBR = 1, Device shall handle it as an illegal CMD.

## 6.2.4.2 Hibernate Mode

### 6.2.4.2.1 Overview

Hibernate mode is an enhanced power saving mode by turning off VDD1 (refer to Chapter 4 for the details) during Dormant state, and optional by UHS-II Device. Time for recovering from Hibernate mode is much shorter than that in case of power cycle. To realize Hibernate mode, Device will indicate if Hibernate mode is supported through "Supporting Hibernate Mode" field located in PHY Capabilities Register, bit position #15 (refer to Table 6-8 for more details).

Host shall inquire if Device or system is capable of Hibernate mode. In case that Hibernate mode is supported, Host may activate this mode. Activation of Hibernate mode is done through setting HBR bit in GO\_DORMANT\_STATE CCMD payload.

Note that in case of Multi-device connection such as Ring, the condition to operate Hibernate mode is that all connected Devices support Hibernate mode. If Device not supporting Hibernate mode is turned off VDD1 during Dormant state, its behavior is not guaranteed.

Figure 6-18 illustrates a brief sequence of transition from / to Hibernate mode. When Host turns off VDD1, VDD1 should be less than 0.5V within 250 [msec]. Once VDD1 is less than 0.5V, this voltage level should be kept for at least 1 [msec]. In case of exit from Hibernate mode, ramp up of VDD1 shall comply with "Power up" specifications (refer to SD Specifications Part 1 Physical Layer Specification Version 4.00 for "Power up").

During Hibernate mode, D0, D1 and RCLK signals shall comply with DORMANT state specifications to avoid a situation in which the operating current is drawn through the Lines. Different from in case of Dormant state, Host shall settle the RCLK Lane to DIF-PD during Hibernate mode.

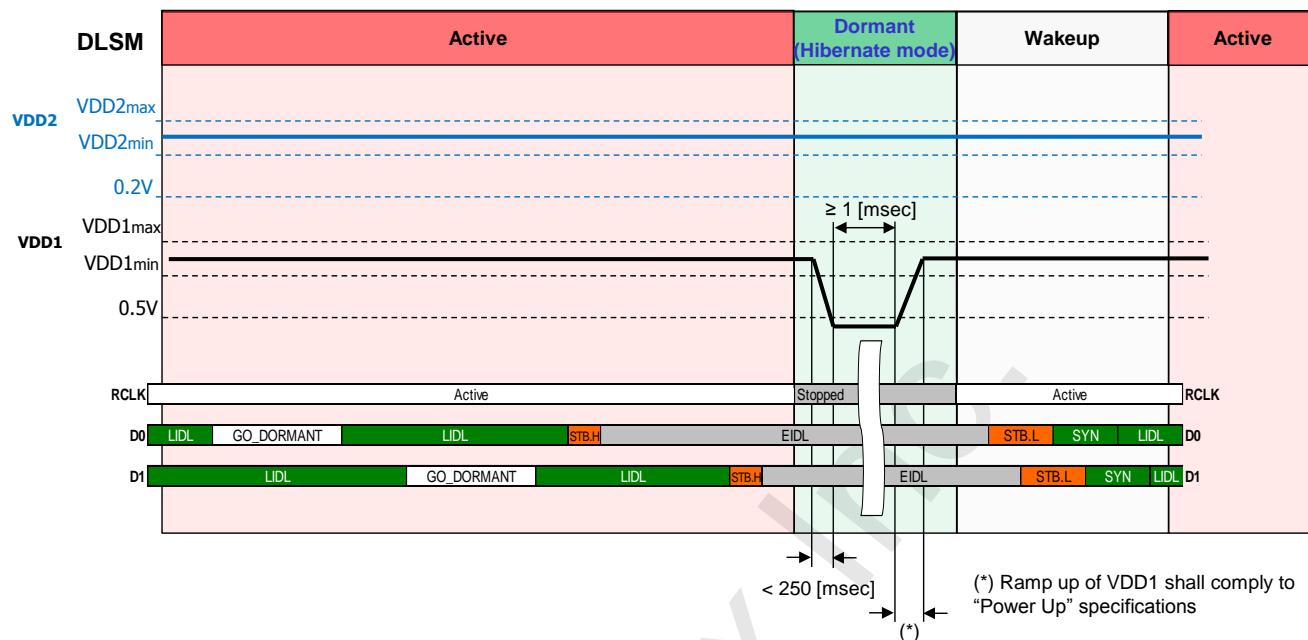


Figure 6-18 : Transition from / to Hibernate Mode

#### 6.2.4.2.2 Entry to Hibernate Mode

As mentioned before, Host shall inquire if Hibernate mode is supported by all connected Devices. Sequence of entering to Hibernate mode is as follows.

- (1) Host inquires HBR field from PHY Capabilities Register of Device.
- (2) If all connected Devices indicate that Hibernate mode is supported, Host may activate Hibernate mode.
- (3) To activate Hibernate mode, Host sends GO\_DORMANT\_STATE CCMD with HBR = 1. After sequence of enter to DORMANT state is completed and after RCLK is stopped, Host may turn off VDD1 (refer to Figure 6-19).

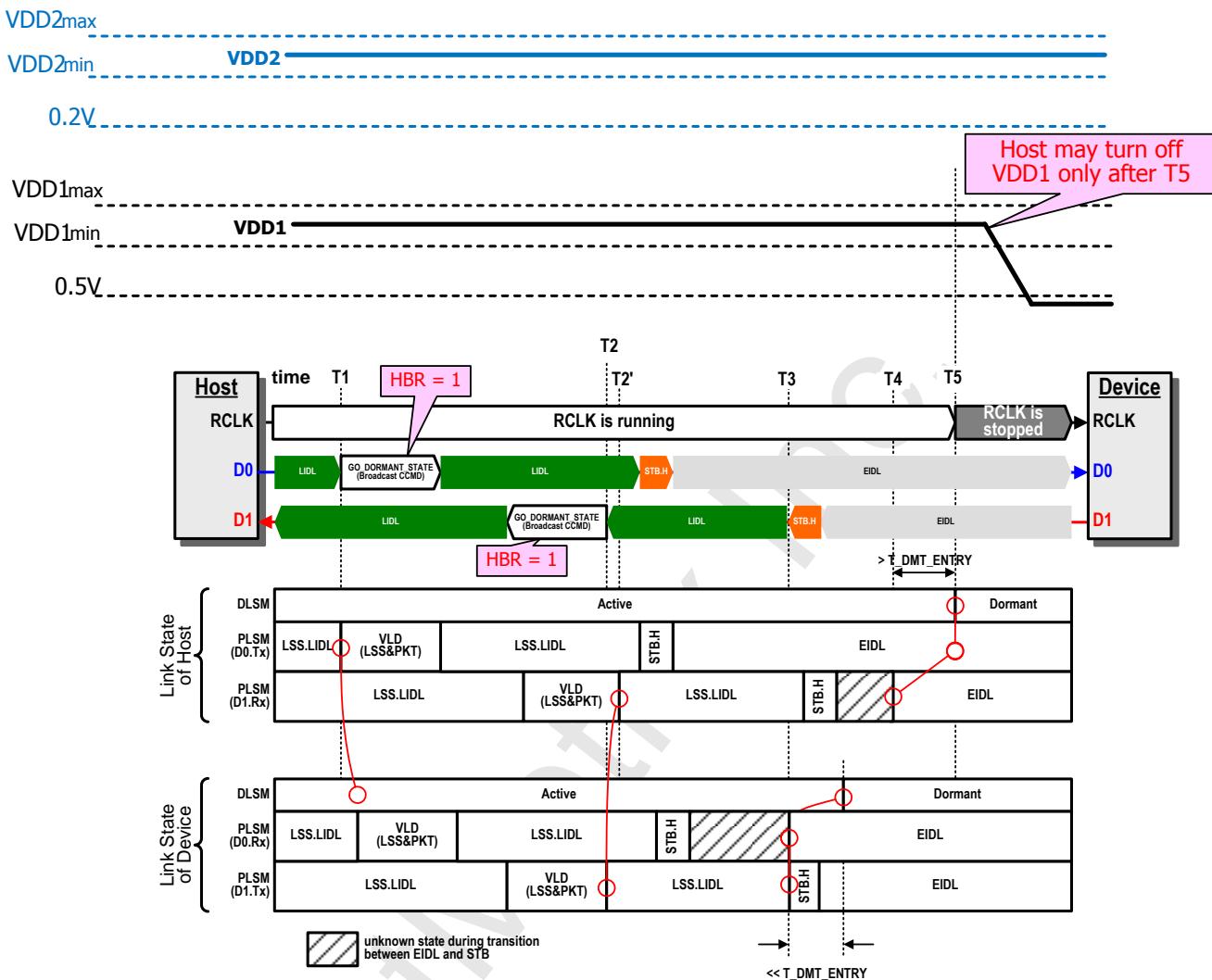


Figure 6-19 : Entry to Hibernate Mode

#### 6.2.4.2.3 Exit from Hibernate Mode

Sequence of exiting from Hibernate mode is as follows (refer to Figure 6-20).

- (1) Host ramps up  $VDD1$  according to "Power Up" specifications.
- (2) Host starts PHY initialization of Device.
- (3) After Wakeup state is completed and LIDL is received, Device transits to Active state if "Config Completion" flag is already set to 1 before enter to Hibernate mode. In case of "Config Completion" flag is 0 before enter to Hibernate mode, Device transits to Config state after wakeup.

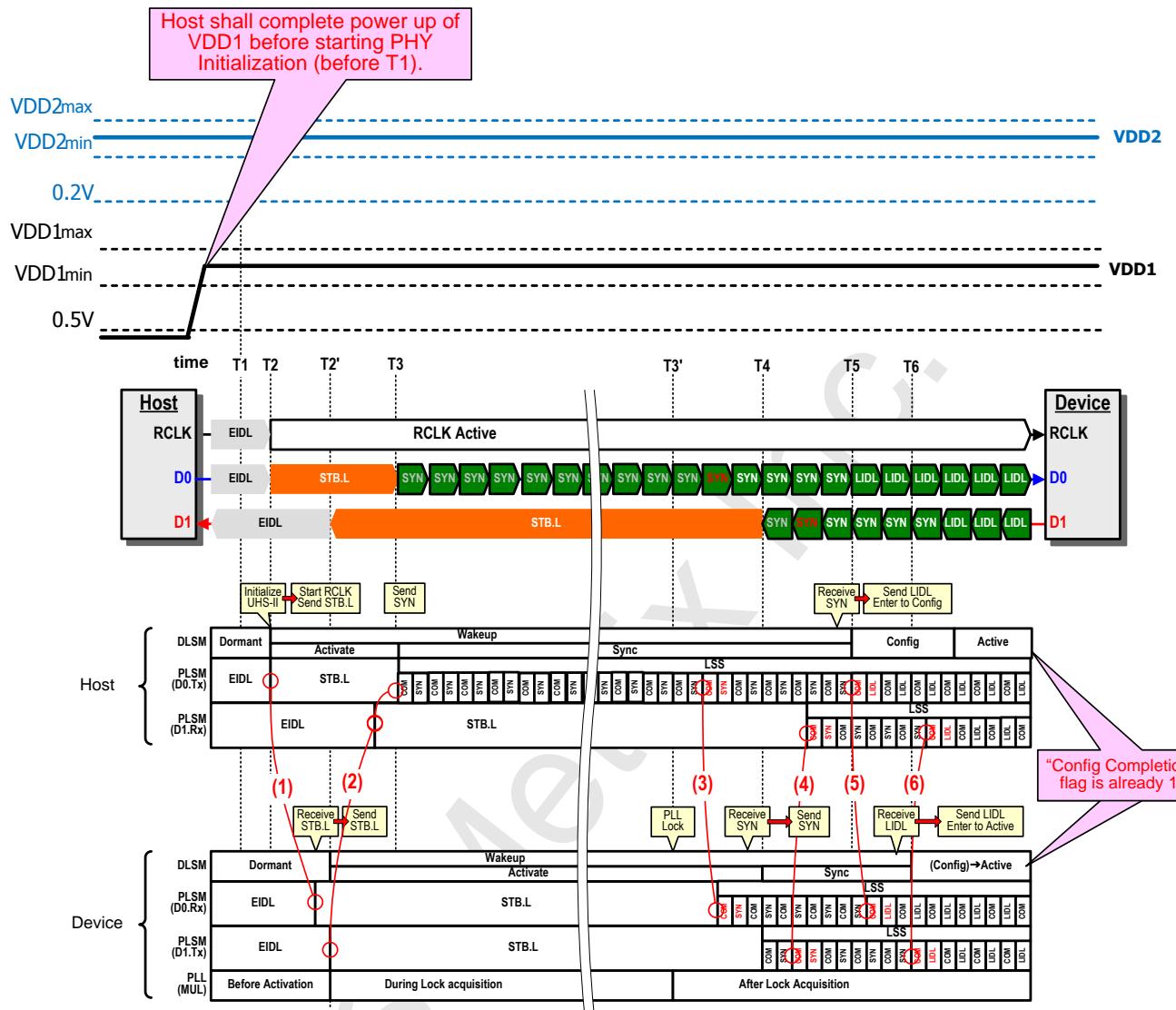


Figure 6-20 : Exit from Hibernate Mode

### 6.2.5 Reset

FULL\_RESET CCMD is used for resetting all components in Device. After it transmits the CCMD or RES to the next node, all state machines defined in this specification get back to the initial state, and in addition, all registers in all layers defined in this specification are reset to the initial value.

After receiving FULL\_RESET CCMD or RES, state transitions take place as described in Figure 5-23 for Fast Mode, and in Figure 5-24 for Low Power Mode, equivalent to those of GO\_DORMANT\_STATE CCMD. Host outputs LIDL (in case of Fast Mode), STB.H, and EIDL in this order on D0 lane after issuing FULL\_RESET CCMD. When Device receives FULL\_RESET CCMD, it transmits FULL\_RESET CCMD or RES, and then it outputs STB.H and EIDL on D1 lane after detecting EIDL on D0.Rx. Sequence of restarting the reset Device is same as wakeup described in Section 3.5.1. Execution of FULL\_RESET is completed by T5 in Figure 5-23 or Figure 5-24 to accept the next PHY Initialization sequence after T5.

## 6.2.6 Device Initialization Mechanism

### 6.2.6.1 General

Device initialization mechanism enables Host system to optimize initialization time considering power consumption. Under Multi-device connection Host may perform initializations for multiple Devices at the same time with in a range of a Host's power supply capability. Device Initialization takes place by issuing the broadcast CCMD called DEVICE\_INIT iteratively, and the Host's power supply capability is provided by the argument of DEVICE\_INIT to each Device.

Figure 6-21 illustrates a format of DEVICE\_INIT CCMD.

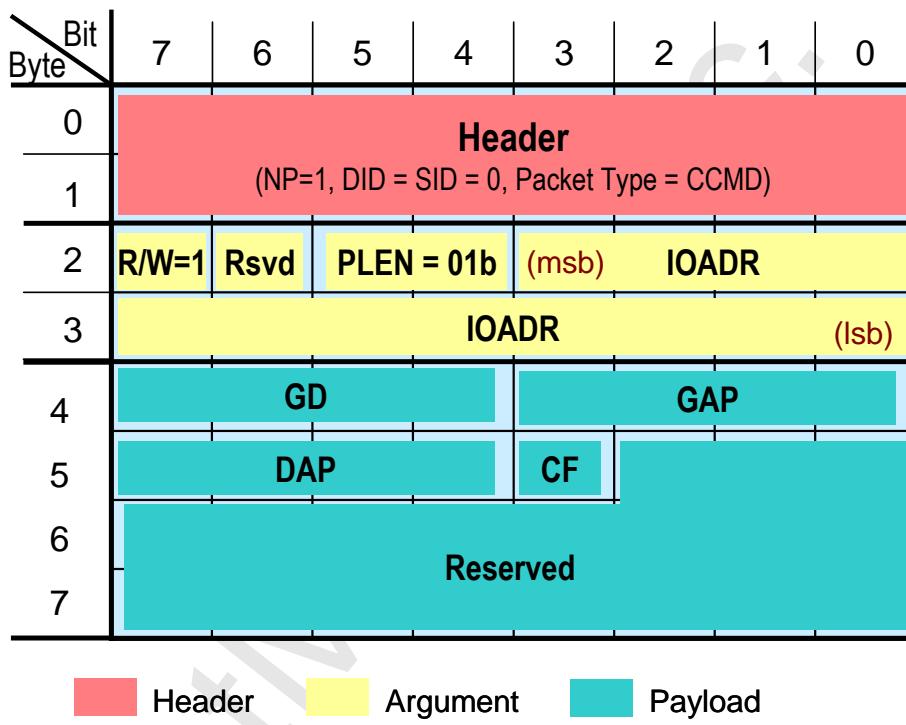


Figure 6-21 : DEVICE\_INIT CCMD Format

- **GD[3:0] (Group Descriptor):** This value indicates the group number to be initialized. The start value is 0 and incremented when all Devices in the group are initialized.
- **GAP[3:0] (Group Allocated Power):** This value indicates the maximum Host's power supply capability that is allowed to certain group. A Device which starts initialization updates this value by subtracting own power consumption from this value. In such a way this field represents the currently remained power resource for a given group.
  - 0: Reserved
  - 1: 360 [mW] (3.6Vx100mA)
  - 2: 720 [mW]
  - 3: 1080 [mW]
  - :
  - n: 360n [mW] (n ≤ 15)
- **DAP[3:0] (Device Allocated Power):** This value is the maximum Host's power supply capability

that is allowed to a certain Device.

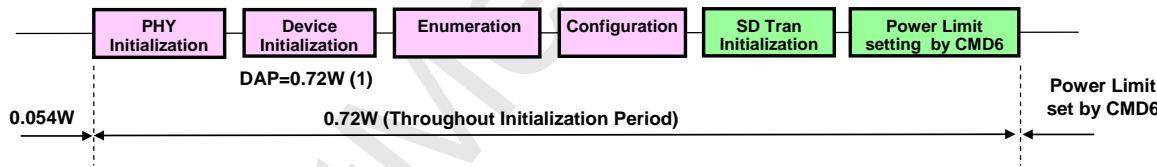
- 0: 360 [mW] Default (Host does not know own power capability)
- 1: 360 [mW] (3.6Vx100mA)
- 2: 720 [mW]
- 3: 1080 [mW]
- :
- n: 360n [mW] ( $n \leq 15$ )
- 
- **CF (Completion Flag):** Device shall clear this bit to "0" if it is not initialized yet. Host uses this value to check whether all Devices are initialized in the system. If Host detects CF = 0 (not all Devices are initialized) from the received DEVICE\_INIT, Host continues to issue DEVICE\_INIT CCMD.
  - 0: Not all Devices complete initialization.
  - 1: All Devices complete initialization.

Device can accept DEVICE\_INIT CCMD only in Config state. So Device shall regard it as an illegal CMD and shall not transmit it to the next Node in case of other than Config state.

**Application Note:**

Host should estimate at least 0.72W power supply capability for a UHS-II SD memory card until Power Limit is set, including settings of DAP and GAP (refer to SD Specifications Part 1 Physical Layer Specification Version 4.00).

When DAP or GAP is set to 0.36W, whether device can be initialized or not is dependent on implementation.



Note (1) : Host should set DAP to 0.72W ( $\leq$ GAP).

**Figure 6-22 : Power Consumption during Initialization**

In case of embedded devices, device manufacturer should provide detail power consumption specification to host system vendor if necessary so that host system vendor can calculate required power budget.

- (1) Power consumption during PHY Initialization (Ppi).
- (2) Power consumption during packet bypassing (Ppb).
- (3) Power consumption in Dormant State (Pds)

Host system calculates required power budget by using device information for all embedded devices and reserves additional power 0.72W for a UHS-II memory card.

### 6.2.6.2 Operation of Device

Let DCP (Device Consumed Power) be the 4 bits index of power actually consumed by each Device Initialization. Device can support multiple DCPs, but it shall support at least DCP = 1 Unit of DCP is 360 [mW] (3.6Vx100mA).

- 1: 360 [mW]
- 2: 720 [mW]
- 3: 1080 [mW]
- :
- n: 360n [mW] ( $n \leq 15$ )

Device shall have the following two parameters in the Preset field in CFG\_REG by system manufacturer.

- **CDCP[3:0] (Candidate DCP):** This parameter indicates the candidate DCP used in actual initialization procedure, including power consumption in UHS-II interface. Removable Devices shall set it to 0. In case of embedded Devices, system manufacturer can preset the parameter considering DCPs supported by the Device.
  - 0: Device may select one of supported DCPs according to DAP and GAP (Default).
  - n: Device shall use the DCP = n. (It is necessary for the Device to support DCP = n.)
- **GN[3:0] (Group Number):** This parameter indicates the group number of the Device. The default number is 0. Removable Devices shall set this parameter to 0. In case of embedded Devices, system manufacturer can preset this parameter ( $GN \geq 0$ ).

Figure 6-23 shows the operation flow of a Device in receiving DEVICE\_INIT. Note that when Device receives the command during its initialization, it shall not transmit the command until its initialization completes. When the Device starts initialization by the command, it shall transmit the command to the next Node without waiting initialization completion of the Device.

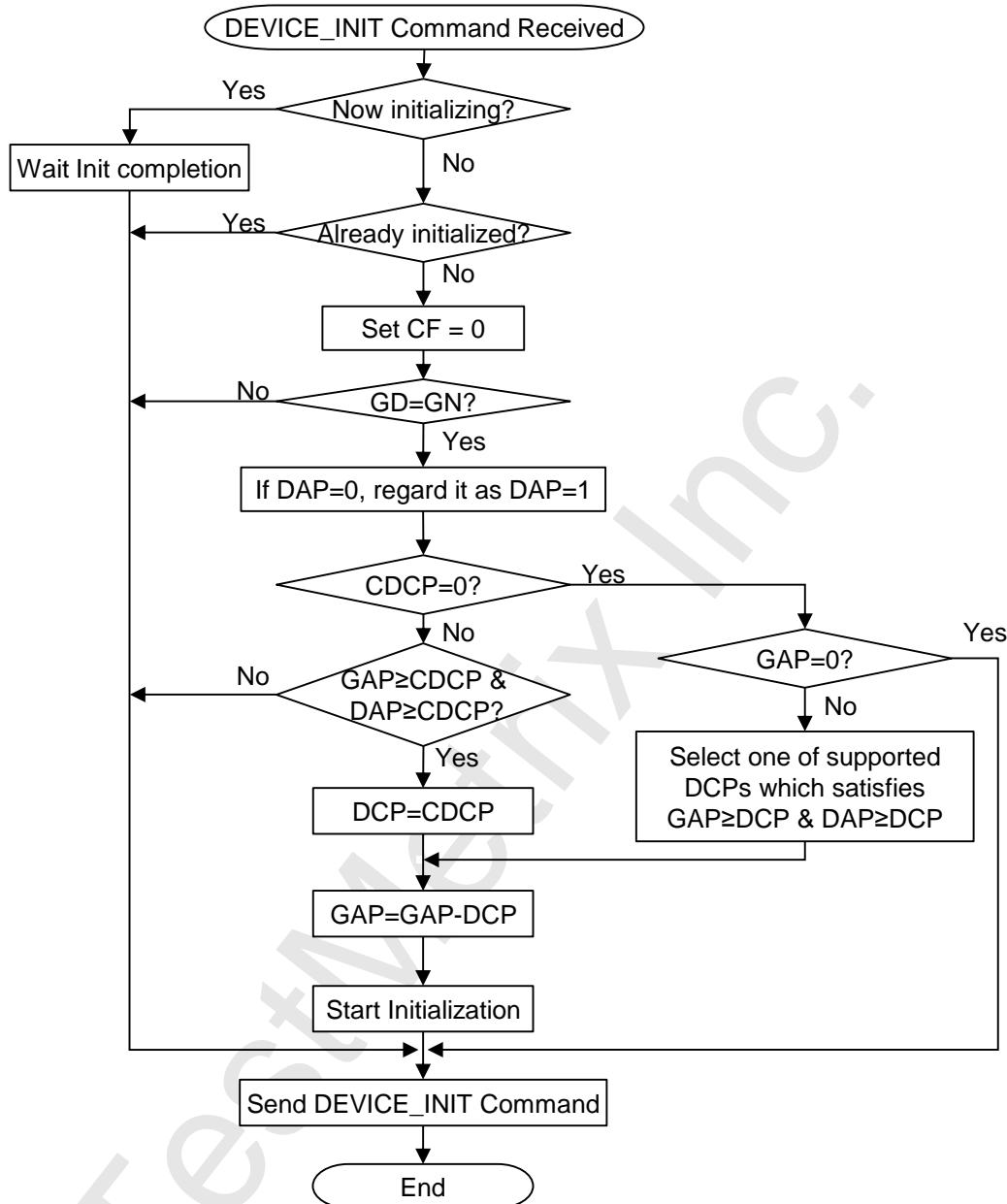
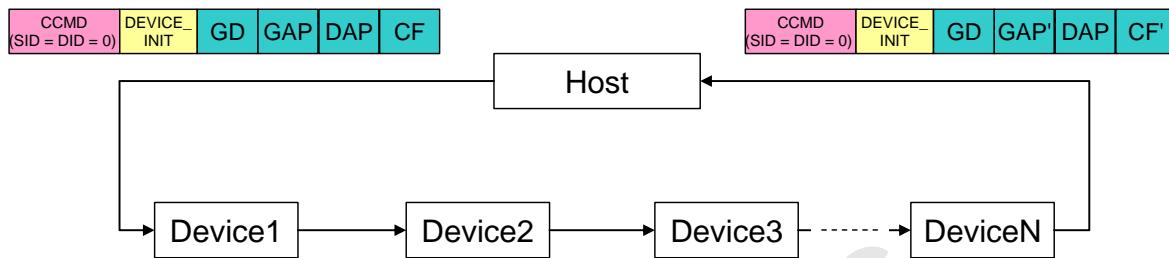


Figure 6-23 : Device's Operation Flow of Receiving DEVICE\_INIT

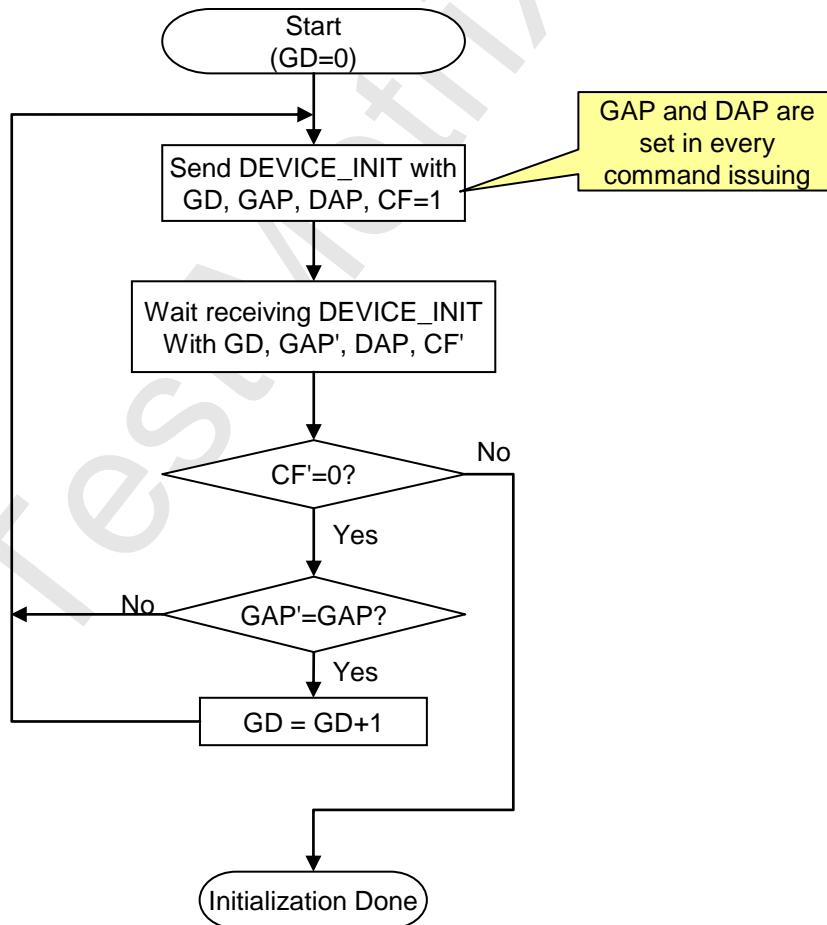
### 6.2.6.3 Operation of Host

GAP and CF denote the parameters in DEVICE\_INIT command issued by Host. GAP' and CF' denote the parameters in DEVICE\_INIT command received by Host (refer to Figure 6-24).



**Figure 6-24 : DEVICE\_INIT Broadcast CCMD Issued by Host**

Figure 6-25 shows the Host's operation flow when it receives DEVICE\_INIT CCMD from the last Device. GAP and CF may be modified to GAP' and CF' by Devices. Host sets initial values to GAP, DAP and CF (= 1) every time the DEVICE\_INIT command is issued and checks the GAP' and CF' in the received DEVICE\_INIT command. If CF' = 1, it means all Devices are initialized and Host stops issuing the DEVICE\_INIT command. If GAP is equal to GAP', it means that the current group completed its initialization. Therefore Host increments GD by 1 in order to initialize the next group.

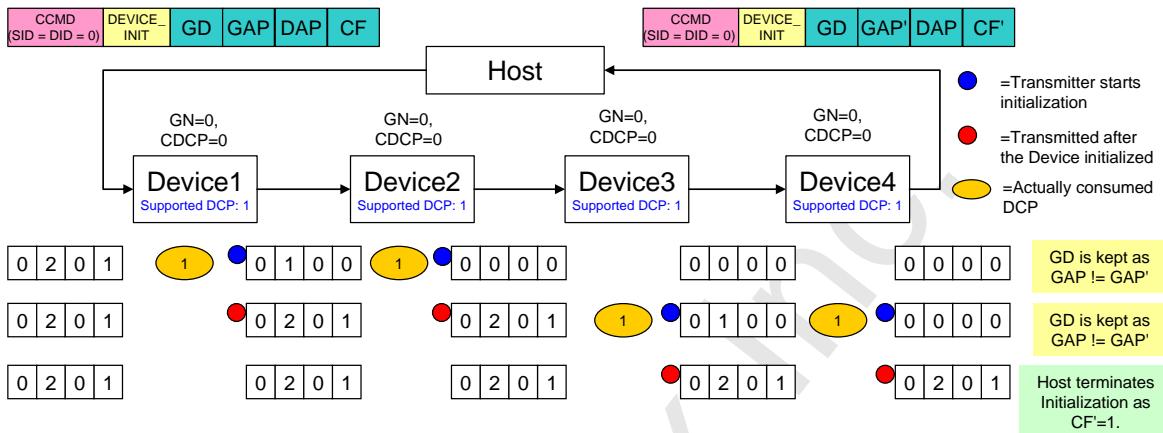


**Figure 6-25 : Host's Operation Flow of Receiving DEVICE\_INIT**

**UHS-II Addendum Version 1.02**

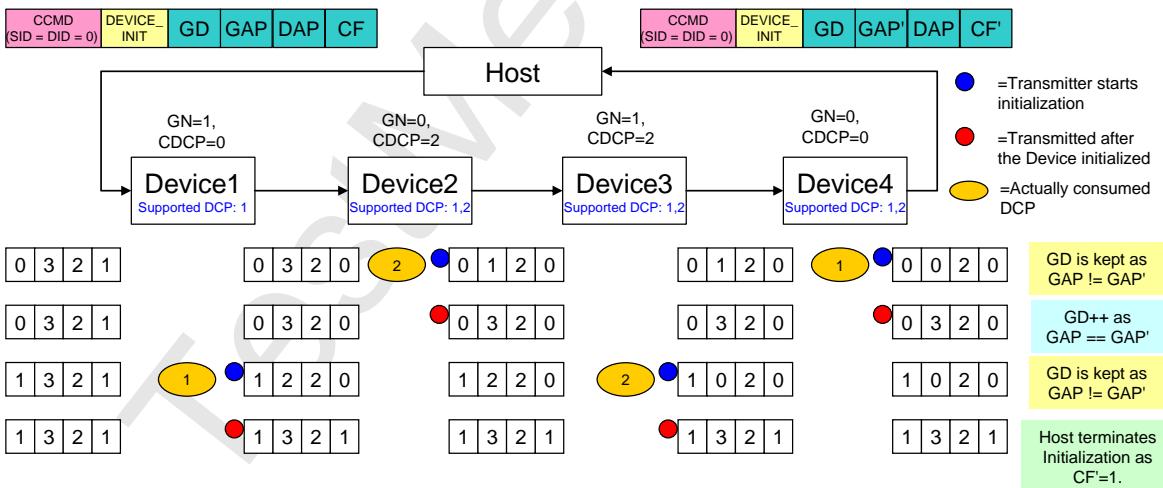
When the number of the DEVICE\_INIT commands is reached to 30 times, Host shall stop issuing the DEVICE\_INIT command and regard it as an error.

Figure 6-26 and Figure 6-27 illustrate some examples of Device Initialization process with different parameters. Note that DAP shall be set by Host greater than or equal to the maximum CDCP in the system.



**Figure 6-26 : Device Initialization Process (Example 1)**

Figure 6-26 shows the case when all preset parameters in Device are default. In this case, each Device is initialized sequentially (As GAP = 2, Device1 and 2 start their initialization by the first CCMD and Device 3 and 4 start by the second one).



**Figure 6-27 : Device Initialization Process (Example 2)**

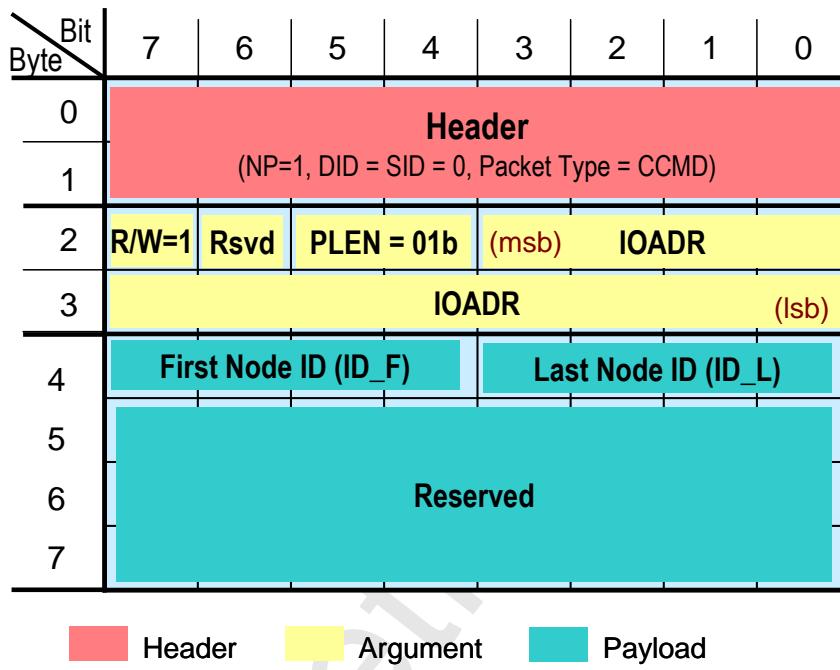
Figure 6-27 shows the case that the initialization order is managed by settings of GN. Device2 and Device3 are set DCP = 2. Device 4 selects DCP = 1 because it receives DEVICE\_INIT CCMD with GAP = 1.

## 6.2.7 Enumeration Mechanism

### 6.2.7.1 General

After initialization, Enumeration process takes place.

Figure 6-28 illustrates a format of ENUMERATE CCMD.



**Figure 6-28 : ENUMERATE CCMD Format**

There are two parameters in Payload area named First Node ID (abbreviated to ID\_F) and Last Node ID (abbreviated to ID\_L) to perform Enumeration.

The algorithm of Enumeration process from the Device's point of view is as described in Figure 6-29. Note that Host shall issue ENUMERATE CCMD with ID\_L = 0.

- Device receives ENUMERATE CCMD with (ID\_F, ID\_L).
- If (ID\_L == 0h),
  - OWN\_NODE\_ID = (ID\_F == Fh) ? ARBITRARY\_ID : ID\_F + 1.
  - Device sets OWN\_NODE\_ID to its Node ID, and transmits ENUMERATE CCMD with (OWN\_NODE\_ID, OWN\_NODE\_ID).
- Else,
  - OWN\_NODE\_ID = (ID\_L == Fh) ? 1 : ID\_L + 1.
  - If (ID\_F == 0h || ID\_F == OWN\_NODE\_ID),
    - Device does not transmit ENUMERATE CCMD because of error.
  - Else
    - Device sets OWN\_NODE\_ID to its Node ID, and transmits ENUMERATE CCMD with (ID\_F, OWN\_NODE\_ID).

Note: ARBITRARY\_ID is any number from 1 to 15 but different from current OWN\_NODE\_ID.

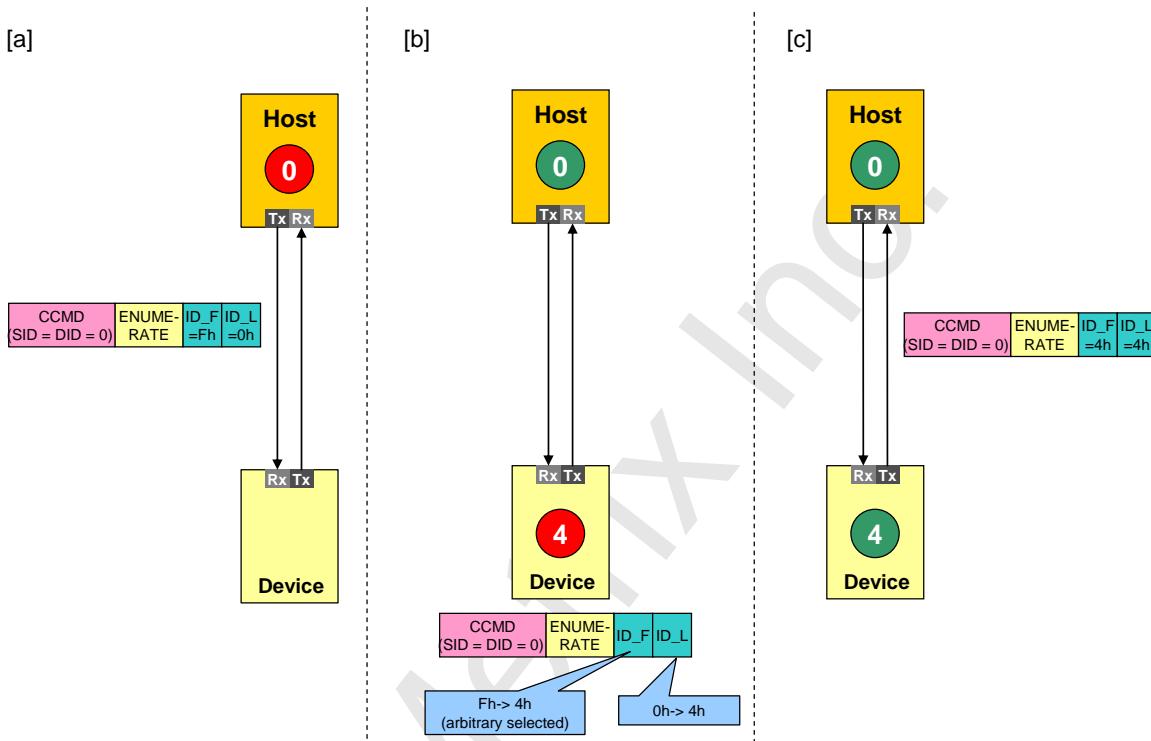
**Figure 6-29 : Device's Algorithm for Enumeration Process**

Device can accept ENUMERATE CCMD only in Config state. So Device shall regard it as an illegal CMD and shall not transmit it to the next Node in case of other than Config state.

Note that ENUMERATE CCMD may be repeated if Host would like to change the set of the generated Node IDs.

### 6.2.7.2 Enumeration Examples in Point to Point Connection

Figure 6-30 illustrates an example of Enumeration method in case of Point to Point connection.



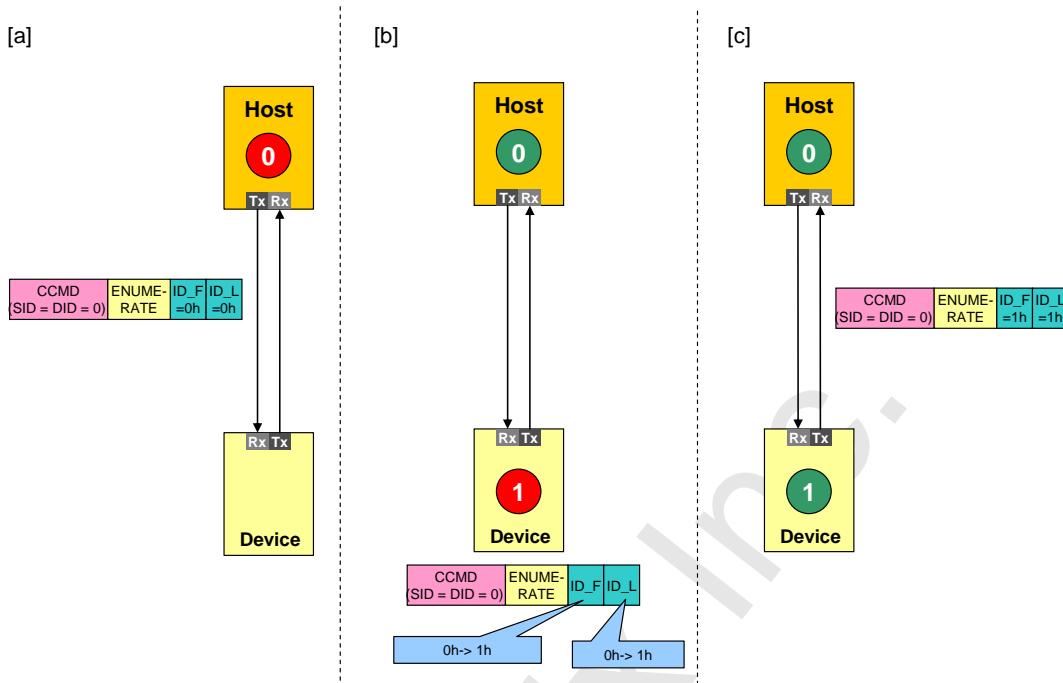
**Figure 6-30 : Enumeration Process in Point to Point Connection (Example 1)**

Host is already set number '0' as its Node ID. Host issues ENUMERATE CCMD with (ID\_F, ID\_L) = (Fh, 0h) as described in Figure 6-30 [a]. When Device receives the CCMD, its Node ID is assigned distinctively referring ID\_F and ID\_L included in the CCMD.

In Figure 6-30 [b], as Device receives ID\_F = Fh and ID\_L = 0h, Device generates its Node ID arbitrarily (number '4' in this example). Then ID\_F and ID\_L are modified to 4h and 4h respectively.

After modifying ID\_F and ID\_L, Device transmits the ENUMERATE CCMD to Host. Since Host detects DID = SID (= its own Node ID) from the header of CCMD, it terminates to transmit the CCMD and Enumeration process ends as a result (Figure 6-30 [c]).

Figure 6-31 illustrates another example of Enumeration method in case of Point to Point connection.

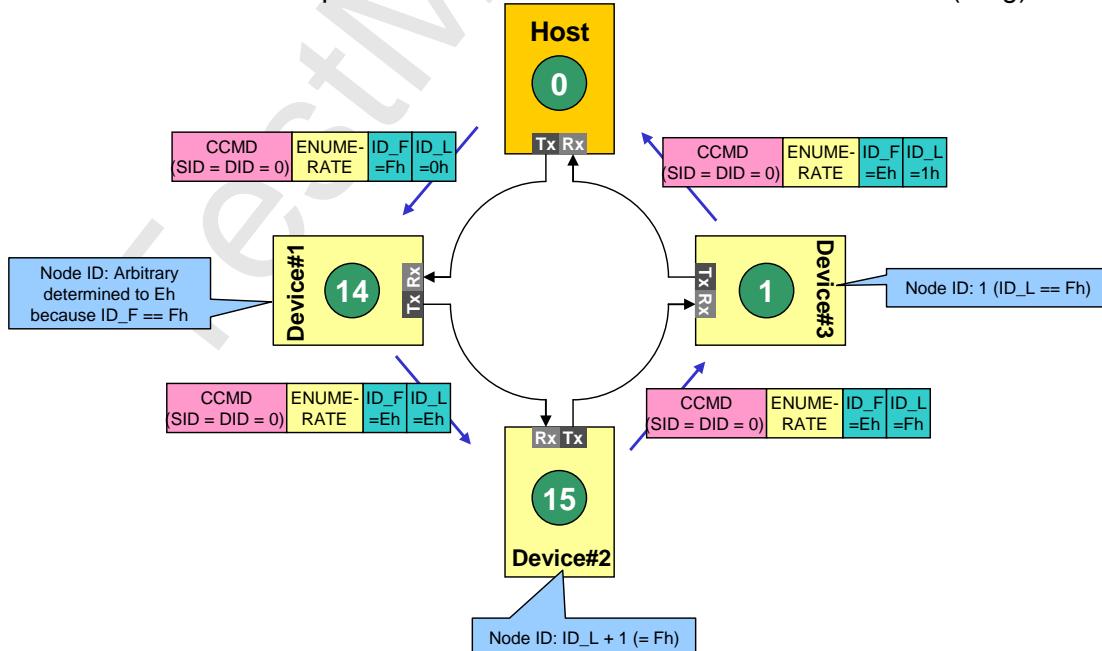


**Figure 6-31 : Enumeration Process in Point to Point Connection (Example 2)**

In this example, Host issues ENUMERATE CCMD with  $(ID\_F, ID\_L) = (0h, 0h)$  as described in Figure 6-31 [a]. So Device sets its Node ID to  $ID\_F + 1$ , that is, number '1' as described the algorithm in Figure 6-29. Other operations are same as in Figure 6-30.

#### 6.2.7.3 Enumeration Examples in Multi-device Connection (Ring)

Figure 6-32 illustrates an example of Enumeration method in case of Multi-device (Ring) Connection.



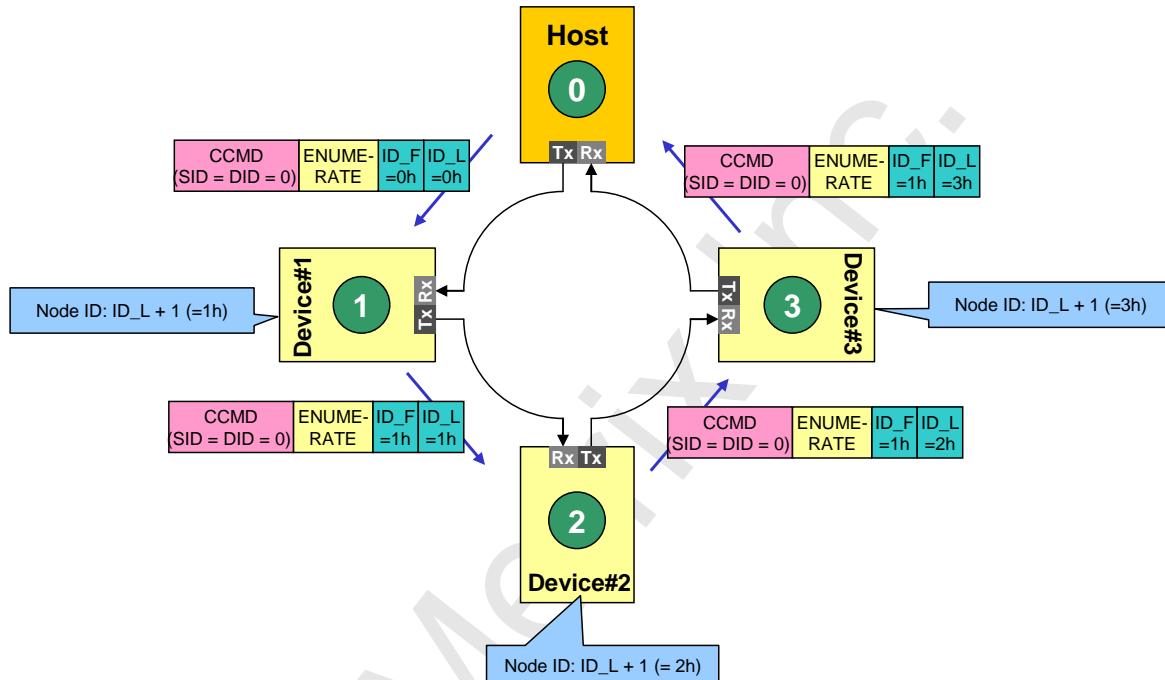
**Figure 6-32 : Enumeration Process in Ring Connection (Example 1)**

In this example, Host issues ENUMERATE CCMD with (ID\_F, ID\_L) = (Fh, 0h). In this case, Device#1 sets its own Node ID '14' arbitrarily according to the algorithm described in Figure 6-29.

Device#2 receives the CMD with (ID\_F, ID\_L) = (Eh, Eh), so its Node ID is assigned to '15'. Node ID of Device#3 is assigned to '1' because it receives ID\_L = Fh (Node ID '0' is set aside for Host).

Same as in Point to Point connection, the transaction ends when Host receives the broadcast CCMD.

Figure 6-31 illustrates another example of Enumeration method in case of Ring. In this case, Node IDs of Devices are assigned incrementally from '1' to '3'.



**Figure 6-33 : Enumeration Process in Ring Connection (Example 2)**

In Multi-device connection, Host may easily generate a table with all the system's Device IDs out of the given First and Last IDs.

## 6.2.8 Configuration Mechanism

### 6.2.8.1 Basic Specification

After Enumeration, Configuration process takes place.

All UHS-II Host and Device shall have their own Configuration Register (CFG\_REG). Its details are described in Section 6.2.9.

CFG\_REG consists of the following fields;

- **Capabilities:** Device-dependent initial capabilities are set to this field.
- **Settings:** Negotiated operating values are assigned to this field.
- **Preset:** Preset values are indicated to this field.

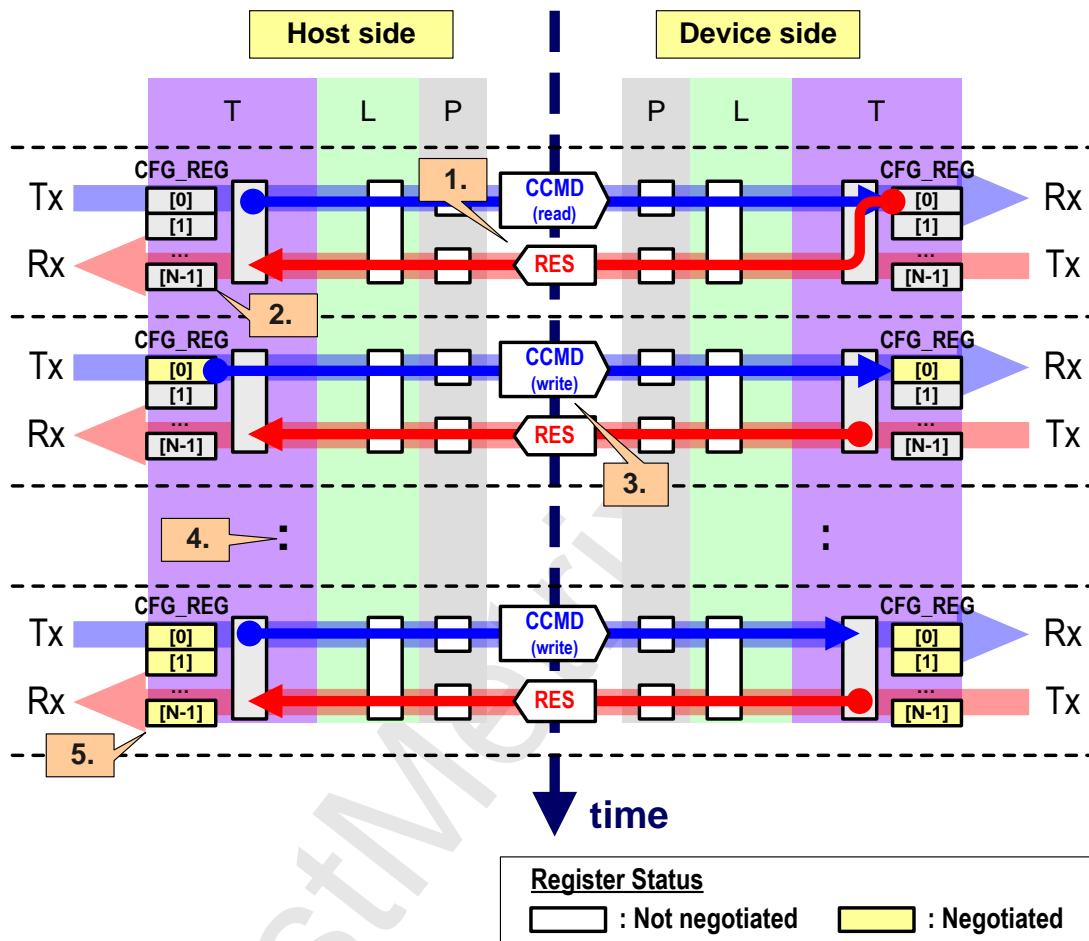
In Capabilities field, device-specific initial capabilities or properties are set, and this field is referred for deciding operating conditions during Configuration.

In Settings field, negotiated values between Host and Device are assigned as operating conditions after Configuration.

Moreover, some parameters can be preset by system manufactures or so, and these are indicated in

Preset field.

Figure 6-34 illustrates Configuration flow in TRAN. The numbers in Figure 6-34 corresponds to the number of the following Configuration procedure.



**Figure 6-34 : Device Configuration Flow**

- (1) After Enumeration, Host issues a read CCMD to obtain capabilities in CFG\_REG of Device.
- (2) Host compares the capability of Host and Device, and lower capabilities are determined as negotiated operating values.
- (3) Host issues a write CCMD to assign the determined operating value to Settings field in CFG\_REG of Device. In the case that the operating value to be set by the CCMD is not supported for Device, the value in CFG\_REG is not updated. (Refer to Section 6.2.15 for details of CMD error sequence.)
- (4) From (1) to (3) are repeated until all necessary operating values are determined.
- (5) Finally, Host issues a write CCMD in order to set "Config Completion" flag to 1. When a Device receives the command and succeeds to set the flag to 1, it makes their own DLSM to Active state before transmitting the RES of the CCMD.

**Application Note:**

In case of Ring Connection, Host shall use broadcast write CCMD to set "Config Completion" flag to 1.

"Config Completion" in CFG\_REG is set to 0 in I/F power cycle or FULL\_RESET.

Host can read values from CFG\_REG regardless of "Config Completion". Moreover, DLSM transits from Active to Config by Host's writing '0' to "Config Completion" only one time after being synchronized by BSYN LSS (This transition only takes place after finishing Boot Code Loading. Refer to Section 5.9). Otherwise, it is possible for Host to write '0' to "Config Completion", but no state transitions in Device occur. In this case, DLSM stays in Config state after issuing GO\_DORMANT\_STATE and finishing PHY Initialization.

### 6.2.8.2 Determination of Block Length

Block Length is determined as follows.

- (1) Host reads "Device-specific MAX\_BLKLEN" from LINK/TRAN Capabilities Registers in Device.
- (2) Host determines the feasible value for "MAX\_BLKLEN" and writes to LINK/TRAN Settings Registers in Device.
- (3) If Device has an application specific layer, Block Length is finally determined by the setting in the application specific layer. Note that Block Length shall be set smaller than or equal to "MAX\_BLKLEN" in the application specific layer.
- (4) Otherwise, Block Length is equal to "MAX\_BLKLEN". Only in this case, Block Length is immediately changed even in Active State when Host writes the value of "MAX\_BLKLEN" by CCMD.

If the application is SD-memory, both "Device-specific MAX\_BLKLEN" and "MAX\_BLKLEN" shall be 512 bytes.

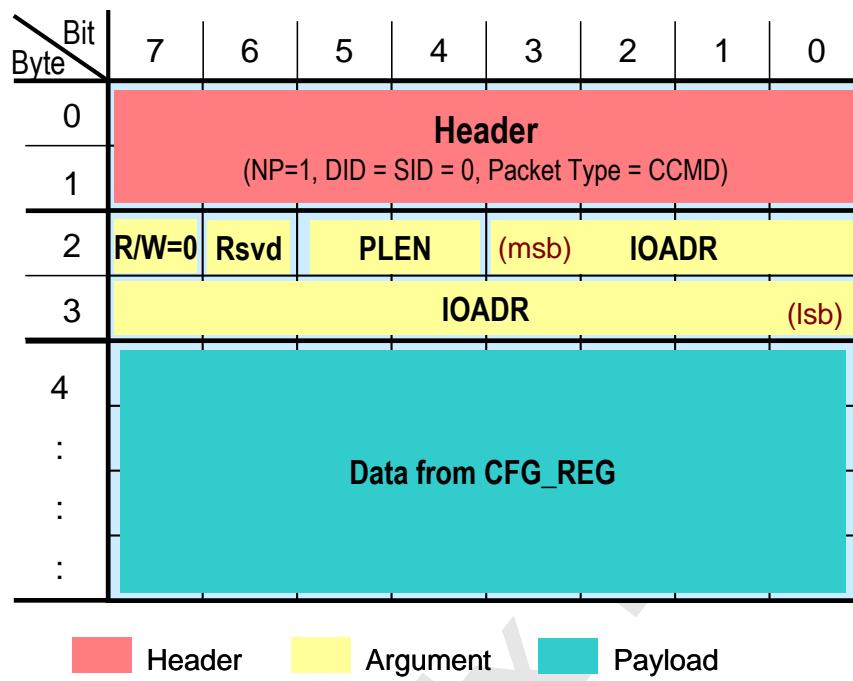
### 6.2.8.3 Quick Configuration

The basic Configuration mentioned above takes place for one Device. So it takes much time for Configuration if there are many Devices connected to Host, because Host shall repeat the process.

In order to make Configuration more efficient, Quick Configuration mechanism is introduced.

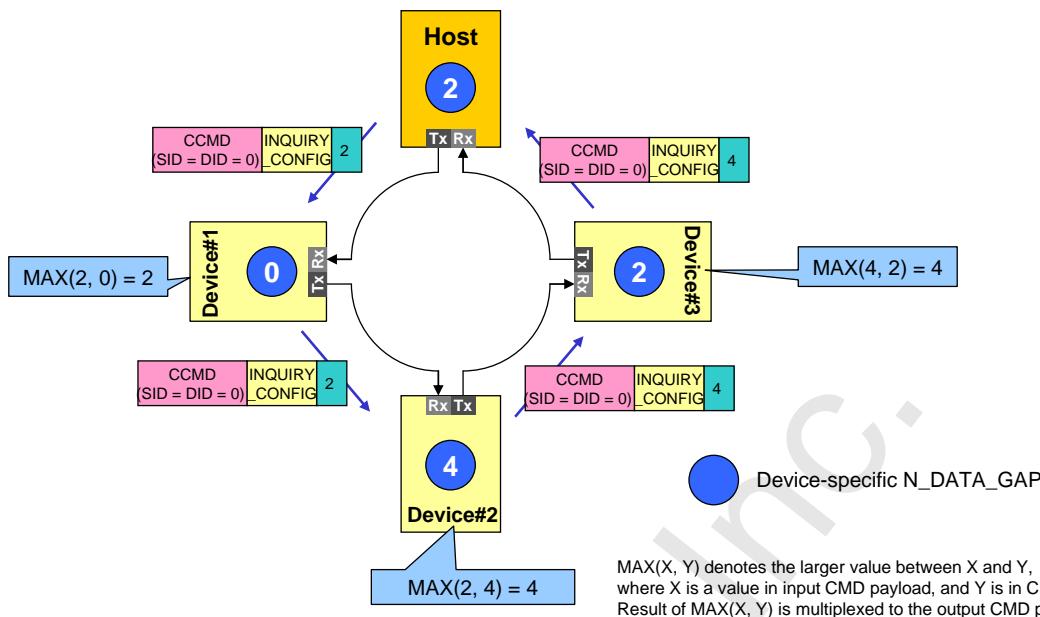
Quick Configuration can be established by the following two broadcast CCMDs, one is INQUIRY\_CONFIG and the other is SET\_COMMON\_CONFIG. Note that these two commands are not defined in CMD\_REG, because IOADR for these commands are set the address for CFG\_REG.

Figure 6-35 illustrates a format of INQUIRY\_CONFIG.

**Figure 6-35 : INQUIRY\_CONFIG Format**

INQUIRY\_CONFIG queries to each Device and returns the values that all Devices satisfy for their settings. IOADR is set the quarter of the absolute address to access in CFG\_REG. The target field of INQUIRY\_CONFIG specified by PLEN and IOADR shall consist entirely of Capabilities registers. Otherwise, INQUIRY\_CONFIG commands are discarded.

Figure 6-36 illustrates an example operation for INQUIRY\_CONFIG. In this example, Device-specific N\_DATA\_GAP (simply called as "the parameter" in this example) is used. In that case, Host sets the beginning address of LINK/TRAN Capabilities Register to IOADR and 001b (4 bytes), to PLEN for instance.

**Figure 6-36 : Operation of INQUIRY\_CONFIG**

Host sets the payload including the parameter and issues INQUIRY\_CONFIG. When Device receives the broadcast CCMD, it compares the parameter in the input CMD payload and that in CFG\_REG in its own, selects appropriate value between them, and overwrites the selected parameter to the broadcast CCMD. Then Device sends the updated broadcast CCMD from its Tx Port. The comparison conditions may be different for each parameter and are described in Section 6.2.9.2. No operations take place for some parameters specified in Section 6.2.9.2, and Reserved field.

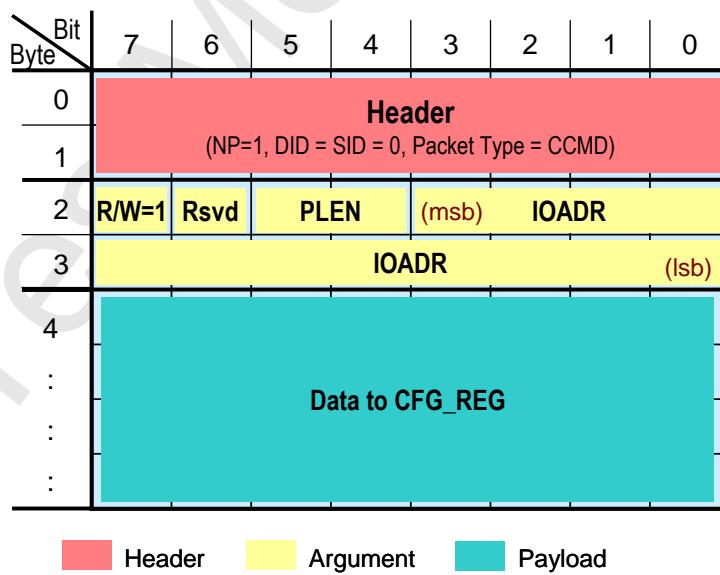
**Figure 6-37 : SET\_COMMON\_CONFIG CCMD Format**

Figure 6-37 illustrates a format of SET\_COMMON\_CONFIG. This broadcast CCMD writes content of Payload area to CFG\_REG specified by IOADR and PLEN. So Host can set the same parameters to all Devices by issuing this broadcast CCMD.

### 6.2.9 Configuration Register (CFG\_REG)

Parameters related to Configuration are assigned to CFG\_REG. CFG\_REG can be accessed by CCMD, not DCMD.

#### 6.2.9.1 Register Map

Table 6-6 shows the map of CFG\_REG. Offset means the relative address based on CFG\_BASE. The parenthetic values indicate bit location in each register. In case of writing to Settings Register, SET\_COMMON\_CONFIG (broadcast CCMD) shall be used for Generic Settings Register and PHY Settings Register in case of Ring connection. In other words, common values shall be set for the two registers among all Devices.

Offset	Register	
Byte address	IOADR	
0000h : 0007h	000h : 001h (63)	(00) Generic Capabilities Register
0008h : 000Fh	002h : 003h (63)	(00) PHY Capabilities Register
0010h : 0017h	004h : 005h (63)	(00) LINK/TRAN Capabilities Register
0018h : 001Fh	006h : 007h	Reserved for Capabilities Register
0020h : 0027h	008h : 009h (63)	(00) Generic Settings Register
0028h : 002Fh	00Ah : 00Bh (63)	(00) PHY Settings Register
0030h : 0037h	00Ch : 00Dh (63)	(00) LINK/TRAN Settings Register
0038h : 00FFh	00Eh : 03Fh	Reserved
0100h : 0107h	040h : 041h (63)	(00) Preset Register
0108h : 03FFh	042h : 0FFh	Reserved

Table 6-6 : CFG\_REG Map

#### 6.2.9.2 CFG\_REG Description

The details of CFG\_REG fields are described below. Refer to Appendix D for the details of registers, and in addition, refer to Table D- 1 for the description of "Attrib" in this specification.

It is recommended for Host to use INQUIRY\_CONFIG (whose initial values are set to Host's capabilities) and SET\_COMMON\_CONFIG regardless of topology (P2P or Ring). Refer to Section

6.2.8.3 for the details of INQUIRY\_CONFIG and SET\_COMMON\_CONFIG. For each Capabilities register, the operation is defined when receiving INQUIRY\_CONFIG. Note that no operations take place to the Capabilities field whose "Attrib" is Rsvd when receiving INQUIRY\_CONFIG.

The followings are Device behavior when written to the register whose "Attrib" is RO or HwInit.

- **P2P CCMD Write:** Device shall issue RES with NACK=0 and bit value of such register is not changed.
- **Broadcast CCMD Write:** Device shall forward broadcast CCMD to the next node, and bit value such register is not changed.

Some Settings registers can be written in both Config and Active state as far as Device receives write CCMD when TSSM is TS\_STNBY (refer to Section 6.2.13.1 for the details of TSSM). In following cases, Device shall not update all Settings Register fields indicated by receiving write command to Settings Registers, and respond RES with NACK = 1 (in case of P2P write CCMD), or shall not respond (in case of Broadcast write CCMD).

- (1) In Active state, the write command targets Settings registers whose writable states are "Config only".
- (2) The write command includes parameters that Device does not support.

**6.2.9.2.1 Generic Capabilities Register**

The table shown below describes Generic Capabilities Register.

<b>Location</b>	<b>Attrib</b>	<b>Register Field Name and Explanation</b>	<b>CMD category</b>																																				
63-24	Rsvd	--	Broadcast /P2P																																				
23-16	RO	<b>Application Type</b> This field indicates a type of Application. Bit 16: 0 = Non-SD memory, 1 = SD Memory Bit 17: 0 = Non-SDIO, 1 = SDIO Bit 18: 0 = Card, 1 = Embedded Others = reserved No operations take place when receiving INQUIRY_CONFIG.																																					
15	Rsvd	--																																					
14	RO	<b>DADR Length</b> This field indicates the length of DADR. 0b = 4 bytes 1b = Reserved for the future use No operations take place when receiving INQUIRY_CONFIG. (See Note (1)).																																					
13-08	RO	<b>Device-specific Number of Lanes and Functionality</b> This field indicates capabilities of number of Lanes and 2L-HD mode. As Device shall support FD mode, the following table shows the optional capabilities. If functionality mentioned below is available, the corresponding bit is set to 1, and otherwise 0. Device can indicate pluralities of options. <table border="1"> <thead> <tr> <th><b>Bit Location</b></th><th><b>Mode</b></th><th><b>D0</b></th><th><b>D1</b></th><th><b>D2</b></th><th><b>D3</b></th></tr> </thead> <tbody> <tr> <td>08</td><td>2L-HD</td><td>Bi</td><td>Bi</td><td>NA</td><td>NA</td></tr> <tr> <td>09</td><td>2D1U-FD</td><td>Dn</td><td>Up</td><td>Dn</td><td>NA</td></tr> <tr> <td>10</td><td>1D2U-FD</td><td>Dn</td><td>Up</td><td>NA</td><td>Up</td></tr> <tr> <td>11</td><td>2D2U-FD</td><td>Dn</td><td>Up</td><td>Dn</td><td>Up</td></tr> <tr> <td>12, 13</td><td>Reserved</td><td>-</td><td>-</td><td>-</td><td>-</td></tr> </tbody> </table> Legends: Bi = Lane is bidirectional Dn = Lane is fixed to downstream Up = Lane is fixed to upstream NA = Not available  Refer to Chapter 8 and 9 for more details. No operations take place when receiving INQUIRY_CONFIG.	<b>Bit Location</b>	<b>Mode</b>	<b>D0</b>	<b>D1</b>	<b>D2</b>	<b>D3</b>	08	2L-HD	Bi	Bi	NA	NA	09	2D1U-FD	Dn	Up	Dn	NA	10	1D2U-FD	Dn	Up	NA	Up	11	2D2U-FD	Dn	Up	Dn	Up	12, 13	Reserved	-	-	-	-	
<b>Bit Location</b>	<b>Mode</b>	<b>D0</b>	<b>D1</b>	<b>D2</b>	<b>D3</b>																																		
08	2L-HD	Bi	Bi	NA	NA																																		
09	2D1U-FD	Dn	Up	Dn	NA																																		
10	1D2U-FD	Dn	Up	NA	Up																																		
11	2D2U-FD	Dn	Up	Dn	Up																																		
12, 13	Reserved	-	-	-	-																																		
07-00	Rsvd	--																																					

Note:

(1) Host which handles 4 bytes address cannot access to the Device whose DADR Length is other than 0b.

**Table 6-7 : Generic Capabilities Register**

### 6.2.9.2.2 PHY Capabilities Register

The table shown below describes PHY Capabilities Register.

Location	Attrib	Register Field Name and Explanation	CMD category
63-40	Rsvd	--	
39-36	RO	<b>Device-specific N_LSS_DIR</b> This field indicates the device-specific number of "DIR" LSS in order that Rx can recognize to have switched 2L-HD mode. It is indicated in unit of eight (8), and 0000b means 128 (16x8). Larger value is set on the command payload field when receiving INQUIRY_CONFIG. (Note that 0000b is regarded as the largest value.)	Broadcast /P2P
35-32	RO	<b>Device-specific N_LSS_SYN</b> This field indicates the device-specific number of "SYN" LSS in order that Rx can recognize as a trigger of synchronization. It is indicated in unit of four (4), and 0000b means 64 (16x4). Larger value is set on the command payload field when receiving INQUIRY_CONFIG. (Note that 0000b is regarded as the largest value.)	
31-16	Rsvd	--	
15	RO	<b>Supporting Hibernate Mode</b> This field indicates whether Device supports Hibernate Mode (refer to Section 6.2.4.2) or not. 0b = Not supporting Hibernate Mode 1b = Supporting Hibernate Mode Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
14-06	Rsvd	--	
05-04	RO	<b>PHY Major Revision</b> This field indicates PHY major revision. 00b = UHS156 (Maximum speed of a Lane is 1.56Gbps)  Others = Reserved. Smaller value is set on the command payload field when receiving INQUIRY_CONFIG	
03-00	RO	<b>PHY Minor Revision</b> It is defined incrementally from 0 to 15 and reset to 0 if PHY Major Revision is updated. No operations take place when receiving INQUIRY_CONFIG.	

Table 6-8 : PHY Capabilities Register

**Application Note:**

Host shall accept Device with any PHY Major Revision. And Host shall use PHY functions which defined by minimum capability of PHY Major Revision.  
 e.g. Host whose PHY Major Revision is 00b shall accept Device whose PHY Major Revision is 00b or more. In this case, Host can use PHY functions which are defined in Revision 00b regardless of Device's Major Revision.

**6.2.9.2.3 LINK/TRAN Capabilities Register**

The table shown below describes LINK/TRAN Capabilities Register.

<b>Location</b>	<b>Attrib</b>	<b>Register Field Name and Explanation</b>	<b>CMD category</b>
63-40	Rsvd	--	
39-32	RO	<b>Device-specific N_DATA_GAP</b> This field indicates device-specific number of DIDL between DATA packets. N_DATA_GAP is finally determined with reference to this parameter and set in LINK/TRAN Settings Register during Configuration. Larger value is set on the command payload field when receiving INQUIRY_CONFIG	Broadcast /P2P
31-20	RO	<b>Device-specific MAX_BLKLEN</b> This field indicates maximum payload length of one block in byte supported by the Device (000h is reserved). Block Length is finally determined with reference to this parameter (refer to Section 6.2.8.2 for more details). If bit 16 in Generic Capabilities Register is equal to 1 ("Application Type" is SD-memory), this field shall be 200h (512 bytes). Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
19	Rsvd	--	
18-16	RO	<b>Device Type</b> This field indicates a type of Device as follows. 001b = Host 010b = Device 011b = Reserved for CMD issuable Device Others = Reserved. No operations take place when receiving INQUIRY_CONFIG.	
15-08	RO	<b>Device-specific N_FCU</b> This field indicates maximum block number in a flow control unit (FCU) supported by the Device. 00h means 256. N_FCU is finally determined with reference to this parameter and set in LINK/TRAN Settings Register during Configuration. Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
07-06	Rsvd	--	
05-04	RO	<b>LINK/TRAN Major Revision</b> This field indicates LINK/TRAN major revision. 00b = Compliant to UHS-II Addendum Version 1.00 01b = Reserved for the future extension Others = Reserved. Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
03-00	RO	<b>LINK/TRAN Minor Revision</b> It is defined incrementally from 0 to 15 and reset to 0 if LINK/TRAN Major Revision is updated. No operations take place when receiving INQUIRY_CONFIG.	

**Table 6-9 : LINK/TRAN Capabilities Register**

**Application Note:**

Host shall accept Device with any LINK/TRAN Major Revision.

e.g. Host whose LINK/TRAN Major Revision is 00b shall accept Device whose LINK/TRAN Major Revision is 00b or more.

**6.2.9.2.4 Generic Settings Register**

The table shown below describes Generic Settings Register.

Loca-tion	Attrib	Register Field Name and Explanation	Writable State	Effective Timing	CMD category
63	RW	<b>Config Completion</b> This field is used for DLSM transition between Config and Active state. In Config state, DLSM transits to Active state immediately when this field is set to 1. In Active state, there are two cases of DLSM transitions when this field is set to 0. DLSM transits to Config state immediately after completing of Boot Code Loading. In other cases, DLSM does not transit to Config state (See Note (1)).	Config/ Active	(See Note (2))	Broadcast /P2P (See Note (3))
62-32	Rsvd	--		--	
31-12	Rsvd	--		--	
11-08	RW	<b>Number of Lanes and Functionality</b> This field indicates the number of Lanes determined through Configuration (See Note (4) and (5)). The default setting is 0000b. 0000b = 2 Lanes – operated by FD mode or 2L-HD mode (if supported) 0010b = 3 Lanes – operated by 2D1U-FD mode. 0011b = 3 Lanes – operated by 1D2U-FD mode. 0100b = 4 Lanes – operated by 2D2U-FD mode. Others = reserved	Config only	After exiting from Dormant	
07-01	Rsvd	--		--	
00	RW	<b>Power Control Mode in Active.Control State</b> This field indicates the mode for power control in Active state. In other words, it indicates symbols to be filled in the gaps on VLD state (refer to Section 5.4, and see Note (6)). 0b = Fast mode (filled with LIDL) 1b = Low power mode (filled with EIDL, STB, and SYN)		In Active	

## Note:

- (1) In case of synchronization by BSYN LSS, it is automatically set to 1 for executing Boot Code Loading and DLSM transits to Active state. After the Boot Code Loading, Host shall set the parameter to 0 in order to make DLSM Config state. (Refer to Section 3.5.2 and Section 5.9.)
- (2) "Config Completion" becomes effective immediately if it is written in Config state. On the other hand, it becomes effective after exiting from Dormant if it is written in Active State except the case of Boot Code Loading described in Note (1).
- (3) In Ring connection, Host shall issue broadcast CCMD for writing Generic Settings Register.
- (4) "Number of Lanes and Functionality" becomes valid by transitioning to Dormant state. So if more than 2 Lanes are used, Host shall issue GO\_DORMANT\_STATE after setting appropriate value to "Number of Lanes and Functionality" (refer to Section 9.4.1). On the other hand, transition to Dormant state is not necessary in case of using only 2 Lanes.
- (5) Even Device supports 2D1U-FD mode, it is impossible to configure 1D2U-FD mode if it does not support 1D2U-FD mode, and vice versa
- (6) In case of synchronization by BSYN LSS, it is automatically set to 0.

**Table 6-10 : Generic Settings Register**

### 6.2.9.2.5 PHY Settings Register

The table shown below describes PHY Settings Register.

Location	Attrib	Register Field Name and Explanation	Writable State	Effective Timing	CMD category
63-40	Rsvd	--		--	
39-36	RW	<b>N_LSS_DIR</b> This field indicates minimum number of "DIR" LSS to be sent from Tx (refer to Figure 8-10 for more details). This value is set during Configuration with reference to "Device-specific N_LSS_DIR" field in other side, and becomes valid in Active state. It is indicated in unit of eight (8), and 0000b means 128 (16x8).	Config only	In Active	Broadcast /P2P (See Note (1))
35-32	RW	<b>N_LSS_SYN</b> This field indicates minimum number of "SYN" LSS to be sent from Tx when starting to synchronize. This value is set during Configuration with reference to "Device-specific N_LSS_SYN" field in other side, and becomes valid in Active state. It is indicated in unit of four (4), and 0000b means 64 (16x4).		In Active	
31-08	Rsvd	--		--	
07-06	RW	<b>Selected Transmission Speed Range</b> This field indicates the range of transmission speed. 00b = Range A (default) 01b = Range B Others = Reserved (See Note (2))	Config/ Active	After exiting from Dormant	
05-04	Rsvd	<b>Selected PHY Major Revision</b> This field is reserved for future use.		--	
03-00	Rsvd	--		--	

Note:

- (1) In Ring connection, Host shall issue broadcast CCMD for writing PHY Settings Register.
- (2) Detailed definitions of Transmission Speed Range are shown in Table 6-12. Host may support only Range A and it may support an arbitrary RCLK frequency from 26 MHz to 52 MHz. On the other hand, Device shall support both Range A and B, and all RCLK frequency from 26 MHz to 52 MHz.

**Table 6-11 : PHY Settings Register**

Range	Speed Range [Mbps]		RCLK Frequency Range [MHz]		RCLK:D0/D1 Ratio
	Min	Max	Min	Max	
A	390	780	26	52	1:15
B	780	1,560	26	52	1:30

**Table 6-12 : Detailed Definitions of Transmission Speed Range**

### 6.2.9.2.6 LINK/TRAN Settings Register

The table shown below describes LINK/TRAN Settings Register.

Loca-tion	Attrib	Register Field Name and Explanation	Writable State	Effective Timing	CMD category
63-40	Rsvd	--	Config/ Active	--	Broadcast /P2P
39-32	RW	<b>N_DATA_GAP</b> This field indicates minimum number of DIDL between DATA packets determined through Configuration. Initiator shall send DIDL at least N_DATA_GAP between EOP and SOP with in the DATA Burst. It is common for both read and write transaction.		In Active (See Note (1))	
31-20	RW	<b>MAX_BLKLEN</b> This field indicates maximum payload length of one block in byte determined through Configuration (000h is reserved). Block Length shall be smaller or equal to this value (refer to Section 6.2.8.2 for more details). If bit 16 in Generic Capabilities Register is equal to 1 ("Application Type" is SD-memory), this field shall be 200h (512 bytes). Default value is 200h.		In Active (See Note (2))	
19-18	Rsvd	--		--	
17-16	RW	<b>MAX_RETRY_NUM</b> This field indicates maximum retry times of DATA Burst Retry (refer to Section 5.5.4). If MAX_RETRY_NUM = 00b, DATA Burst Retry becomes disable. Default value is 11b.		In Active (See Note (1))	
15-08	RW	<b>N_FCU</b> This field indicates maximum number of blocks in a flow control unit (FCU) determined through Configuration. 00h means 256. Default value is 01h. (See Note (3) and (4).)		In Active (See Note (1))	
07-00	Rsvd	--		--	

Note:

- (1) It is immediately effective in Active State.
- (2) It is immediately effective in Active State if there are no application specific layers. With any application specific layers, this parameter is not reflected immediately if it is written in Active State.
- (3) If bit 16 in Generic Capabilities Register is equal to 1 ("Application Type" is SD-memory), its possible settings are 01h, 02h, 04h, 08h, 10h, 20h, 40h, and 80h.
- (4) The length of a DATA Burst obtained by Block Length and N\_FCU shall be smaller than or equal to 64K (65,536) bytes

**Table 6-13 : LINK/TRAN Settings Register**

### 6.2.9.2.7 Preset Register

The table shown below describes Preset Register.

Location	Attrib	Register Field Name and Explanation
63-08	Rsvd	
07-04	HwInit	<b>CDCP</b> This field indicates the value of CDCP (Candidate DCP) for Device Initialization. Refer to Section 6.2.6 for more details.
03-00	HwInit	<b>GN</b> This field indicates the value of GN (Group Number) for Device Initialization. Refer to Section 6.2.6 for more details.

**Table 6-14 : Preset Register**

### 6.2.10 Status Register (ST\_REG)

Status Register indicates detecting error and states of CM-TRAN. ST\_REG can be accessed by CCMD, not DCMD.

#### 6.2.10.1 Register Map

Table 6-15 shows the map of ST\_REG. Offset means the relative address based on ST\_BASE.

Offset		Register
Byte address	IOADR	
0000h	000h	(00)
:	:	
0003h	000h	Status in TRANS_ABORT (31)
0004h	001h	
:	:	
01FFh	07Fh	Reserved

**Table 6-15 : Status Register**

#### 6.2.10.2 ST\_REG Description

The details of ST\_REG fields are described below. Refer to Table D- 1 for the description of "Attrib" in this specification.

##### 6.2.10.2.1 Status in TRANS\_ABORT Register

The table shown below describes Status in TRANS\_ABORT Register. After I/F power cycle or FULL\_RESET, all bits in this field are set to 0.

Fields of TBSM, TPSM and TSSM are updated only when Device accepts TRANS\_ABORT CCMD, and reflected the last status of each state machine before accepting TRANS\_ABORT CCMD.

On the other hand, fields of error identifier (refer to Section 5.2.5) are updated when each error is detected, and cleared after Device issues RES of the corresponding any P2P commands for that Device other than TRANS\_ABORT. Different from RECOVERABLE\_ERROR in MSG (STAT), RECOVERABLE\_ERROR in ST\_REG shall be accumulated until its clear condition described above is satisfied.

This Register can be read by CCMD, but it makes sense only when Host can get RES of the previous TRANS\_ABORT.

Location	Attrib	Register Field Name and Explanation
31-25	Rsvd	
24	RO	<b>RECOVERABLE_ERROR</b> It indicates whether RECOVERABLE_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
23-19	Rsvd	
18	RO	<b>RETRY_EXPIRE_ERROR</b> It indicates whether RETRY_EXPIRE_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
17	RO	<b>DEVICE_SPECIFIC_ERROR</b> It indicates whether DEVICE_SPECIFIC_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
16	RO	<b>ILLEGAL_HEADER_ERROR</b> It indicates whether ILLEGAL_HEADER_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
15-12	Rsvd	
11-08	RO	<b>TSSM</b> It indicates the last TSSM when receiving TRANS_ABORT. 0000b = TS_INIT 0001b = TS_STNBY 0011b = TS_SCBSY 0010b = TS_SCRDY Others = Reserved
07-04	RO	<b>TPSM</b> It indicates the last TPSM when receiving TRANS_ABORT. 0000b = TP_IDLE 0001b = TP_WAIT 0110b = TP_INTERVAL 0010b = TP_DIN 0100b = TP_DOUT 1000b = TP_C_WAIT Others = Reserved
03-00	RO	<b>TBSM</b> It indicates the last TBSM when receiving TRANS_ABORT. 0000b = TB_BUSY 0001b = TB_IN_REQ 0011b = TB_IN_PREP 0010b = TB_IN_RDY 0100b = TB_OUT_PREP 1100b = TB_OUT_REQ 1000b = TB_OUT_RDY Others=Reserved

Note:

(1) Refer to Section 5.2.5 for the definition of each error identifier.

**Table 6-16 : Status in TRANS\_ABORT Register**

### 6.2.11 Interrupt Register (INT\_REG)

Interrupt can be operated through INT\_REG. INT\_REG can be accessed by CCMD, not DCMD. If the application is SD-memory, it is not necessary to implement INT\_REG.

#### 6.2.11.1 Register Map

Table 6-17 shows the map of INT\_REG. Offset means the relative address based on INT\_BASE.

Offset		Register
Byte address	IOADR	
0000h : 0003h	000h : 000h	INT Enable (00) (31)
0004h : 0007h	001h : 001h	INT Status (00) (31)
0008h : 01FFh	002h : 07Fh	Reserved

Table 6-17 : Interrupt Register

#### 6.2.11.2 INT\_REG Description

The details of INT\_REG fields are described below. Refer to Table D- 1 for the description of "Attrib" in this specification.

##### 6.2.11.2.1 INT Enable

The table shown below describes INT Enable Register. Up to eight kinds of interrupt factors (from Factor#0 to Factor#7) can be defined in UHS-II. In this specification, all interrupt factors are not defined and reserved for the future specifications.

Location	Attrib	Register Field Name and Explanation
31-08	Rsvd	
07-00	RW	<b>INT Enable</b> This field indicates enables of each interrupt factors. Location X ( $0 \leq X \leq 7$ ) corresponds to the enable bit for Factor#X. 0b = Interrupt disable 1b = Interrupt enable

Table 6-18 : INT Enable Register

##### 6.2.11.2.2 INT Status

The table shown below describes INT Status Register. Up to eight kinds of interrupt factors (from Factor#0 to Factor#7) can be defined in UHS-II. In this specification, all interrupt factors are not defined and reserved for the future specifications.

Location	Attrib	Register Field Name and Explanation
31-08	Rsvd	
07-00	RO	<p><b>INT Status</b>  This field indicates status for each interrupt factors. Location X (<math>0 \leq X \leq 7</math>) corresponds to the status bit for Factor#X.  0b = Interrupt is not pending  1b = Interrupt is pending</p>

**Table 6-19 : INT Status Register**

### 6.2.12 Command Register (CMD\_REG)

UHS-II native commands are executed by "writing" to the specific address in CMD\_REG by CCMD, not DCMD.

Table 6-20 shows CMD\_REG. Offset means the relative address based on CMD\_BASE.

Offset		Register Field Name and Explanation	PLEN	CMD category
Byte address	IOADR			
0000h	000h	<p><b>FULL_RESET</b>  - To reset all components in Device (same situation before I/F power up).  - Refer to Section 6.2.5 for more details.</p>	00b	Broadcast/P2P
0004h	001h	<p><b>GO_DORMANT_STATE</b>  - To make DLSM transit to Dormant state for power saving including Hibernate Mode.  - Refer to Section 6.2.4 for more details.</p>	01b (4 bytes)	Broadcast/P2P
0008h	002h	<p><b>DEVICE_INIT</b>  - To start Device Initialization according to the payload settings.  - Refer to Section 6.2.6 for more details.</p>	01b (4 bytes)	Broadcast
000Ch	003h	<p><b>ENUMERATE</b>  - To perform Device Enumeration.  - Refer to Section 6.2.7 for more details.</p>	01b (4 bytes)	Broadcast
0010h	004h	<p><b>TRANS_ABORT</b>  - To abort outstanding transaction.  - In case of UHS-II native protocol, this command also terminates the DATA Burst transmission.  - TRANS_ABORT shall terminate all existing transactions regardless of its TID.  - Refer to Section 3.4.5 for more details.</p>	00b	P2P
Others		Reserved	---	---

**Table 6-20 : Command Register****Application Note:**

In case of Ring connection, Host shall not issue P2P FULL\_RESET CCMD or P2P GO\_DORMANT\_STATE CCMD.

## 6.2.13 Transaction Control and Management State Machine

### 6.2.13.1 Transaction Scheduling State Machine (TSSM)

Transaction Scheduling State Machine (TSSM) is the state machine for managing conditions of issuing commands considering multiple command execution.

TSSM observes execution states of each TID (the execution states are managed in Transaction Processing State Machine) and controls available timing of issuing commands (for example, available timing for issuing a TRANS\_ABORT CCMD during DCMD execution).

Figure 6-38 shows the state diagram of TSSM.

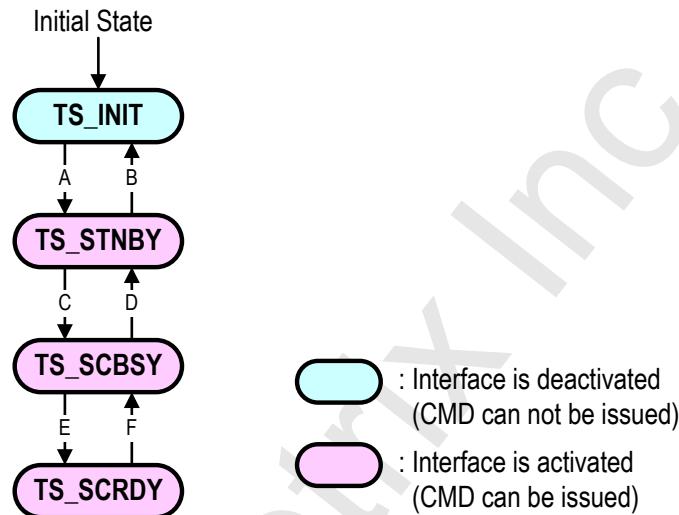


Figure 6-38 : State Diagram of TSSM

The TSSM state definitions are the following;

- **TS\_INIT:** Before interface activation.
  - TRAN directs LINK to start PHY wakeup process in this state (DLSM is in Dormant, or Wakeup).
  - Any command cannot be issued.
- **TS\_STNBY:** Command scheduling standby.
  - No transaction is in execution.
  - Arbitrary CCMD or DCMD can be issued. However, issuing DCMD is permitted only in Active State of DLSM.
- **TS\_SCBSY:** Command scheduling busy.
  - At least one transaction is in execution and either transaction is not in Command Time Slot (CTS).
  - Host can issue TRANS\_ABORT and FULL\_RESET CCMD when it detects illegal situations such as timeout. In addition, Host can not issue any other command than TRANS\_ABORT or FULL\_RESET CCMD.
  - Device should accept TRANS\_ABORT and FULL\_RESET CCMD. If Device does not respond to TRANS\_ABORT or FULL\_RESET CCMD, Device behavior is undefined.
- **TS\_SCRDY:** Command scheduling ready.
  - At least one transaction is in execution and all of transaction is in CTS.
  - Specific CCMD can be issued.
  - TRANS\_ABORT CCMD can be issued in this state to terminate data transaction.

Transition conditions of TSSM are shown in Table 6-21.

TSSM Transition			Transition Timing (Condition)
Case	Current State	Next State	
A	TS_INIT	TS_STNBY	DLSM transition from Wakeup to Config
B	TS_STNBY	TS_INIT	DLSM transition from Config to Dormant DLSM transition from Active to Dormant
C		TS_SCBSY	At least one TPSM is in TP_WAIT (*1)
D	TS_SCBSY	TS_STNBY	All of TPSMs are in TP_IDLE (*1)
E		TS_SCRDY	Both of the following conditions are met. - All of transactions are in either CTS or TP_IDLE of TPSM - At least one transaction is in CTS
F	TS_SCRDY	TS_SCBSY	At least one transaction is not in CTS and not in TP_IDLE of TPSM

\*1: During multiple command execution, TPSM is managed for each transaction. For example, two transactions are executed at the same time, two TPSMs are managed in TRAN.

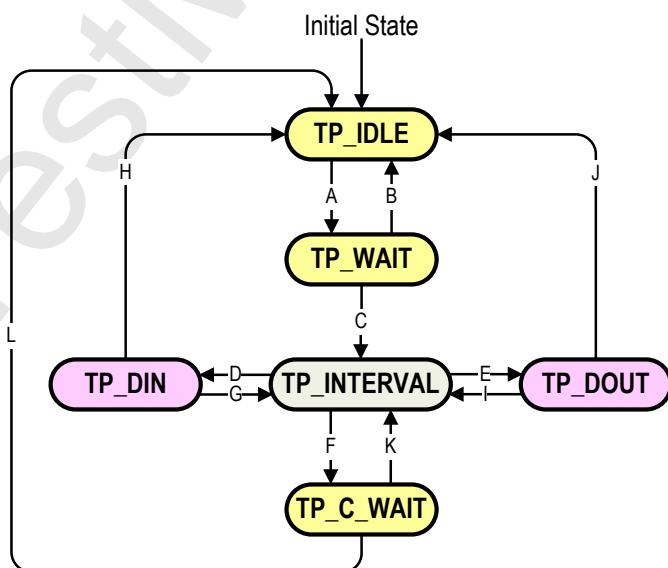
**Table 6-21 : Transaction Conditions of TSSM**

### 6.2.13.2 Transaction Processing State Machine (TPSM)

TRAN controls all transactions by Transaction Processing State Machine (TPSM).

Both Host and Device have TPSM, and the states of TPSM in Host and Device are transferred in relation to each other through packet transaction and an indication from LINK.

Figure 6-39 shows the state diagram of TPSM.



**Figure 6-39 : State Diagram of TPSM**

The TPSM state definitions are the following;

- **TP\_IDLE:** Before starting transaction.
  - Host can issue arbitrary CCMD or DCMD only in this state.
- **TP\_WAIT:** Expecting response.
  - Device will transmit RES or Broadcast CCMD if no errors occur.
  - Host is waiting for RES after issuing P2P CCMD or DCMD, or waiting for Broadcast CCMD.
  - Device can issue Broadcast CCMD, RES and MSG.
  - Host is not allowed to issue any packet including MSG in this state.
- **TP\_INTERVAL:** Interval period between data transfers.
  - Both Host and Device wait for "flow control handshake completion" notification from LINK. (Refer to Chapter 0 for details of flow control.)
  - Host can issue a particular CCMD for controlling transaction before issuing a flow control MSG.  
[e.g. TRANS\_ABORT CCMD]  
In the case of data read transaction, Host shall issue TRANS\_ABORT CCMD before issuing FCRDY MSG. In the case of data write, Host shall issue TRANS\_ABORT CCMD before issuing FCREQ MSG.
- **TP\_DIN:** Receiving DATA.
  - Only DATA packet can be received in this state.
- **TP\_DOUT:** Transmitting DATA.
  - Only DATA packet can be transmitted in this state.
- **TP\_C\_WAIT:** Waiting for RES to CCMD.
  - Host waits for RES to CCMD which is issued during TP\_INTERVAL.
  - Only RES and MSG from Device can be issued.

Transition conditions of TPSM are shown in Table 6-22.

TPSM Transition			Transition Timing (Condition)
Case	Current State	Next State	
A	TP_IDLE	TP_WAIT	Receiving CCMD or DCMD.
B	TP_WAIT	TP_IDLE	Transmitting RES for CCMD. Transmitting RES with NACK = 1 for CMD (See Note (1)). Transmitting broadcast CCMD. Detecting error from broadcast CCMD (See Note (2))
C		TP_INTERVAL	Transmitting RES with NACK = 0 for DCMD.
D	TP_INTERVAL	TP_DIN	TBSM transition from TB_IN_PREP to TB_IN_RDY.
E		TP_DOUT	TBSM transition from TB_OUT_REQ to TB_OUT_RDY.
F		TP_C_WAIT	Receiving CCMD during TP_INTERVAL.
G	TP_DIN	TP_INTERVAL	Transmitting STAT MSG in case of not completing all DATA Bursts reception, including in case of DCMD with LM = 0. (See Note (3))
H		TP_IDLE	Completing all DATA Bursts reception (in case of DCMD transaction with LM = 1) and transmitting STAT MSG without any error indications.
I	TP_DOUT	TP_INTERVAL	Receiving STAT MSG in case of not completing all DATA Bursts transmission, including in case of DCMD with LM = 0. (See Note (3))
J		TP_IDLE	Completing all DATA Bursts transmission (in case of DCMD transaction with LM = 1) and receiving STAT MSG without any error indications.
K	TP_C_WAIT	TP_INTERVAL	Transmitting RES for CCMD (except FULL_RESET (P2P) and TRANS_ABORT). Transmitting RES with NACK = 1 for CCMD (See Note (1)). Detecting error from FULL_RESET (broadcast) (See Note (2))
L		TP_IDLE	Transmitting RES for FULL_RESET(P2P) or TRANS_ABORT. Transmitting FULL_RESET broadcast CCMD.

Note:

- (1) Refer to Section 6.2.15.1 when detecting errors from P2P CCMD or DCMD.
- (2) Refer to Section 6.2.15.3 when detecting errors from broadcast CCMD.
- (3) If DATA Burst retry is going to take place next time, TPSM transits to TP\_INTERVAL, not TP\_IDLE.

**Table 6-22 : Transaction Conditions of TPSM**

In case of timeout, Device may receive TRANS\_ABORT or FULL\_RESET CCMD in TP\_WAIT, TP\_DIN or TP\_DOUT. In this case, its TPSM transits to TP\_IDLE after it transmits RES to TRANS\_ABORT or FULL\_RESET. If Device does not respond to TRANS\_ABORT or FULL\_RESET CCMD, Device behavior is undefined.

Examples of TPSM transition during data read and write transactions are shown in Figure 6-40. Message packet is defined in Section 5.2.4 as a Link Layer Packet. Flow control message (FCREQ and FCRDY MSG) handshake is performed in LINK. Moreover, detecting "data burst end" is also performed in LINK.

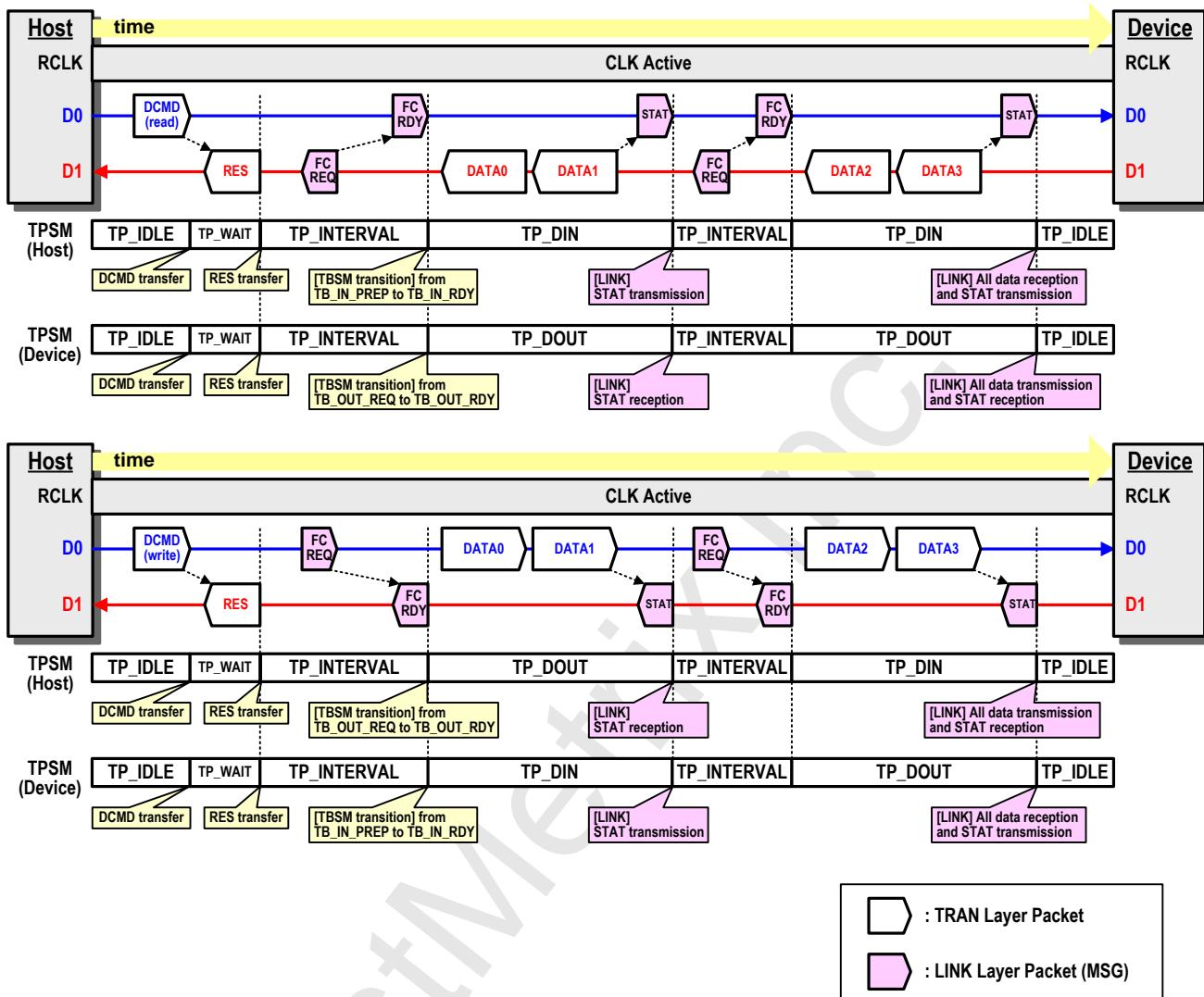


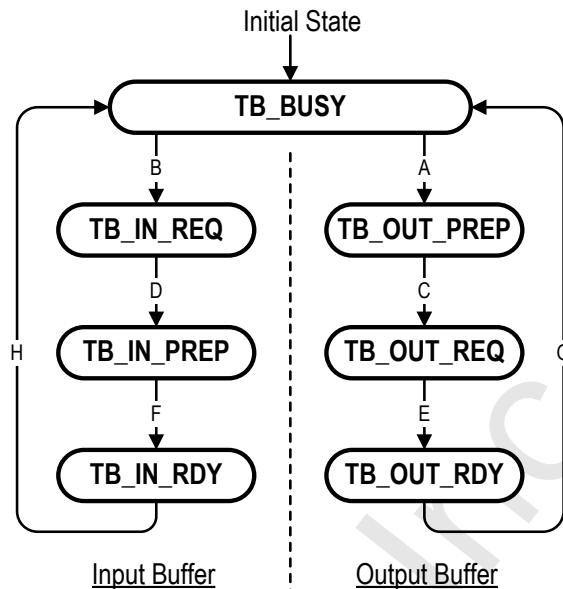
Figure 6-40 : State Transition of TPSM during Data Transaction

### 6.2.13.3 Transaction Buffer-management State Machine (TBSM)

Input/Output buffer state is managed by Transaction Buffer-management State Machine (TBSM) in TRAN.

The states of input/output buffer transmit according to Flow Control sequence performed in LINK. TRAN informs LINK of the buffer state, and LINK informs TRAN of flow control information such as FCREQ/FCRDY transmission and reception.

Figure 6-41 shows the state diagram of TBSM.

**Figure 6-41 : State Diagram of TBSM**

The TBSM state definitions are the following;

- **TB\_BUSY:** Input/Output buffer is busy.
  - DCMD is not issued, or DCMD is issued and output buffer is not ready to transmit data.
- [Input buffer state]
  - **TB\_IN\_REQ:** FC handshake is requested
    - Data receiver is requested to make input buffer prepared for receiving data and reply FCRDY MSG.
  - **TB\_IN\_PREP:** Input buffer is prepared.
    - Input buffer is prepared for receiving DATA packets, and TRAN allows LINK to issue FCRDY MSG in the case that there is no CCMD (e.g. TRANS\_ABORT CCMD) to issue.
  - **TB\_IN\_RDY:** Ready to receive data.
    - Data receiver is waiting for receiving DATA packets, or data receiver is currently receiving DATA packets.
- [Output buffer state]
  - **TB\_OUT\_PREP:** Output buffer is prepared.
    - Output buffer is prepared for transmitting DATA packets, and TRAN allows LINK to issue FCREQ MSG in the case that there is no CCMD (e.g. TRANS\_ABORT CCMD) to issue.
  - **TB\_OUT\_REQ:** FC handshake is requested.
    - Data initiator waits for FCRDY MSG from data receiver.
  - **TB\_OUT\_RDY:** Ready to transmit data.
    - Data initiator is currently transmitting DATA packets.

Transition conditions of TBSM are shown in Table 6-23

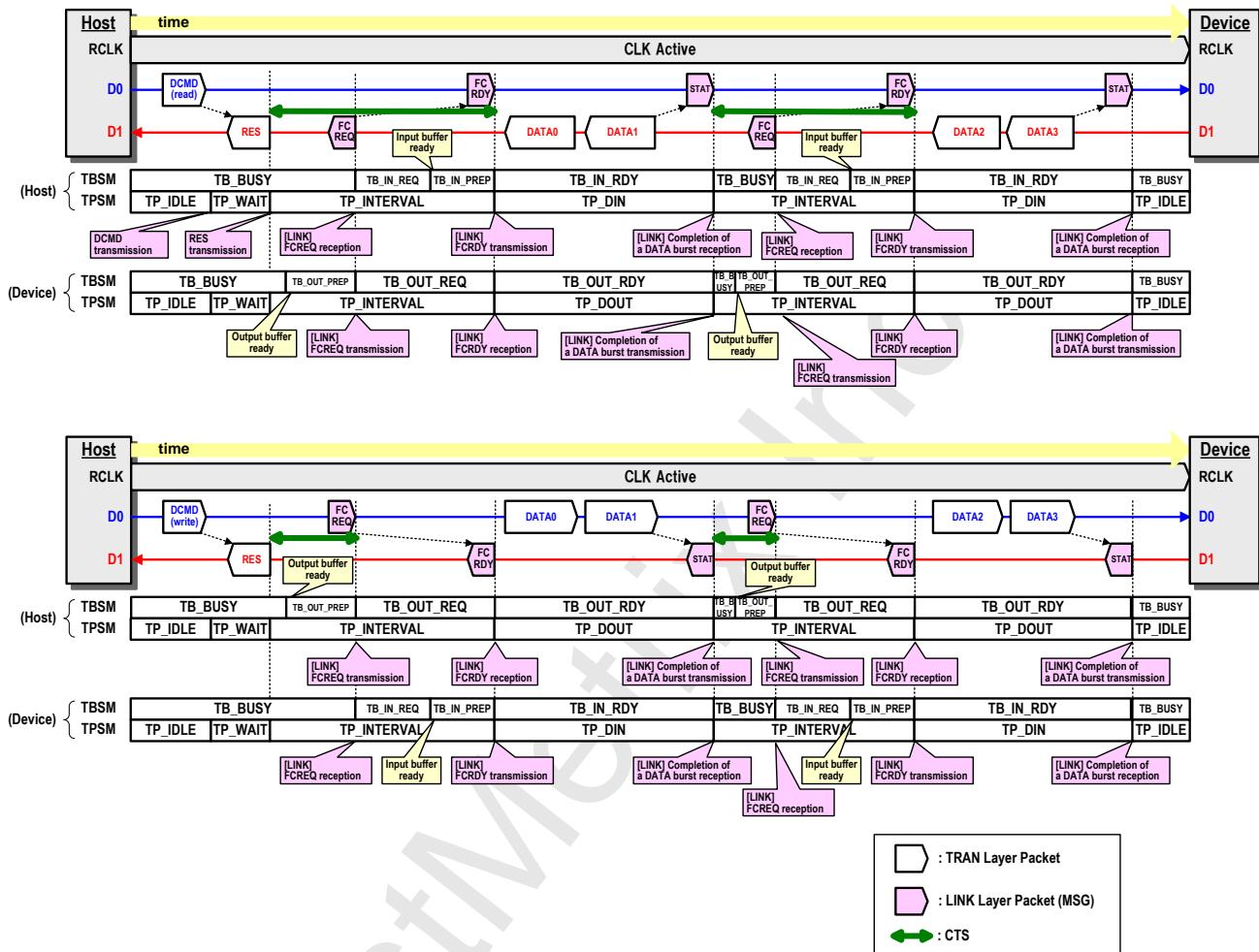
TBSM Transition			Transition Timing (Condition)
Case	Current State	Next State	
A	TB_BUSY	TB_OUT_PREP	Output buffer ready
B		TB_IN_REQ	FCREQ reception in LINK
C	TB_OUT_PREP	TB_OUT_REQ	FCREQ transmission in LINK
D	TB_IN_REQ	TB_IN_PREP	Input buffer ready
E	TB_OUT_REQ	TB_OUT_RDY	FCRDY reception in LINK
F	TB_IN_PREP	TB_IN_RDY	FCRDY transmission in LINK
G	TB_OUT_RDY	TB_BUSY	Completion of a DATA Burst transmission in LINK
H	TB_IN_RDY		Completion of a DATA Burst reception in LINK

**Table 6-23 : Transaction Conditions of TBSM**

If Device receives TRANS\_ABORT CCMD in TB\_IN\_REQ, TB\_IN\_RDY, TB\_OUT\_PREP, TB\_OUT\_REQ, and TB\_OUT\_RDY, its TBSM transits to TB\_BUSY after it transmits RES to TRANS\_ABORT.

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Examples of TBSM transition during data read and write transactions are shown in Figure 6-42. This figure includes TPSM transition as a reference.



**Figure 6-42 : State Transition of TBSM and TPSM during Data Transaction**

#### 6.2.13.4 Detail Definition of Command Time Slot

Command Time Slot (CTS) is defined as a time period that FULL\_RESET, TRANS\_ABORT, and arbitrary read CCMD are allowed to be issued or accepted on the way of data transmission. Note that other CCMDs and all DCMDs are prohibited to issue during CTS at UHS-II Addendum Version 1.00. Moreover at UHS-II Addendum Version 1.00, while Host is executing data transaction for one Device, Host shall not issue any commands to other Devices, even in CTS period.

From Device's point of view, definition of CTS is as follows.

- During read transaction, CTS is when TPSM is TP\_INTERVAL.
- During write transaction, CTS is when TPSM is TP\_INTERVAL and TBSM is either TB\_BUSY or TB\_OUT\_PREP.

On the other hand, definition of CTS is as follows from Host's point of view.

- During read transaction, CTS is when TPSM is TP\_INTERVAL.
- During write transaction, CTS is when TPSM is TP\_INTERVAL and TBSM is either TB\_BUSY or TB\_OUT\_PREP.

Figure 6-43 illustrates the relation between CTS and read CCMD.

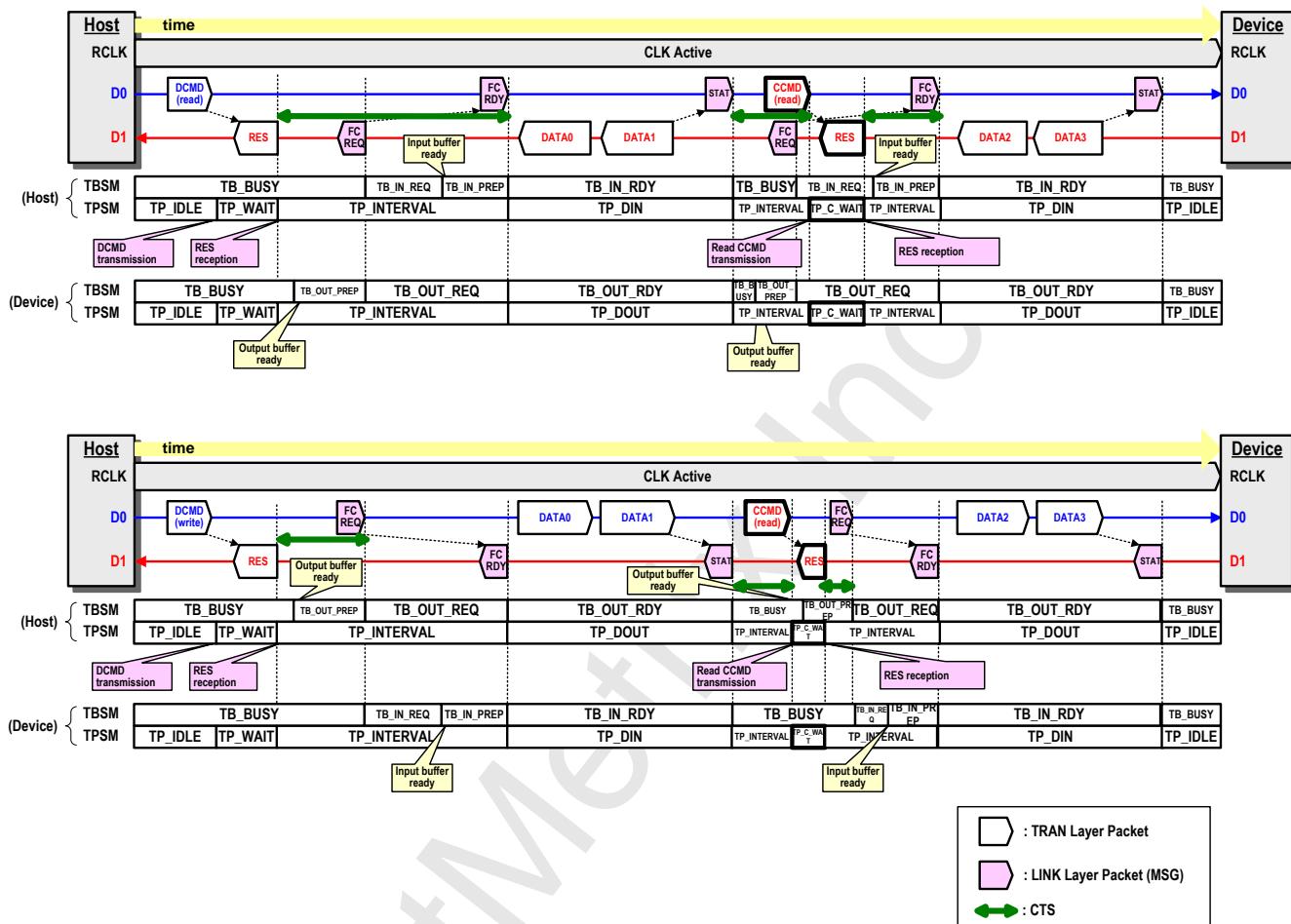


Figure 6-43 : Relation between CTS and TP\_C\_WAIT

As mentioned above, arbitrary read CCMD can be issued during CTS. In case of read transaction, Host can transmit it during CTS regardless of FCREQ reception. However, Host shall not transmit MSG (FCRDY) before receiving RES accompanied with the read CCMD.

In case of write transaction, on the other hand, Host shall not transmit MSG (FCREQ) before receiving RES if read CCMD issued during CTS.

### 6.2.13.5 State Machines during Boot Code Loading

As described in Section 5.9, when Boot Device is directed to execute Boot Code Loading by BSYN LSS, it transits to Active state after PLL lock acquisition. In this time, TBSM, TPSM and TSSM are defined as follows.

- **TBSM:**

- Initial State is TB\_BUSY.
- For Boot Device, TBSM transits to TB\_OUT\_PREP, TB\_OUT\_REQ, TB\_OUT\_RDY, and goes back to TB\_BUSY again during the period of one FCU transmission, according to the condition described in Table 6-23.
- For Host, TBSM transits to TB\_IN\_REQ, TB\_IN\_PREP, TB\_IN\_RDY, and goes back to

TB\_BUSY again during the period of one FCU reception, according to the condition described in Table 6-23.

- **TPSM:**
  - Initial State is TP\_INTERVAL.
  - For Boot Device, TPSM toggles between TP\_INTERVAL and TP\_DOUT according to the condition described in Table 6-24.
  - For Host, TPSM toggles between TP\_INTERVAL and TP\_IN according to the condition described in Table 6-24. Note that Host cannot issue any commands even in TP\_INTERVAL during Boot Code Loading.
- **TSSM:**
  - Fixed to TS\_SCBSY.

TPSM Transition			Transition Timing (Condition)	Note
Case	Current State	Next State		
E'	TP_INTERVAL	TP_DOUT	TBSM transition from TB_OUT_REQ to TB_OUT_RDY	Applied for Boot Device
I'	TP_DOUT	TP_INTERVAL	Completion of a DATA Burst transmission and STAT MSG reception	
D'	TP_INTERVAL	TP_DIN	TBSM transition from TB_IN_PREP to TB_IN_RDY.	Applied for Host
G'	TP_DIN	TP_INTERVAL	Completion of a DATA Burst reception and STAT MSG transmission	

**Table 6-24 : Transaction Conditions of TPSM while Boot Code Loading**

### 6.2.14 Transaction Rules

In this section, example sequences of control transaction and data transaction in native protocol (NP = 1) are described. About the error case, refer to Section 6.2.15 for details of error sequence.

Both Host and Device shall set the same TID of the CMD to the corresponding RES, DATA, and MSG within a transaction. Moreover, Host should transmit packets with TID = 0.

#### 6.2.14.1 Control Transaction Sequence

Figure 6-44 illustrates an example sequence of control read transaction.

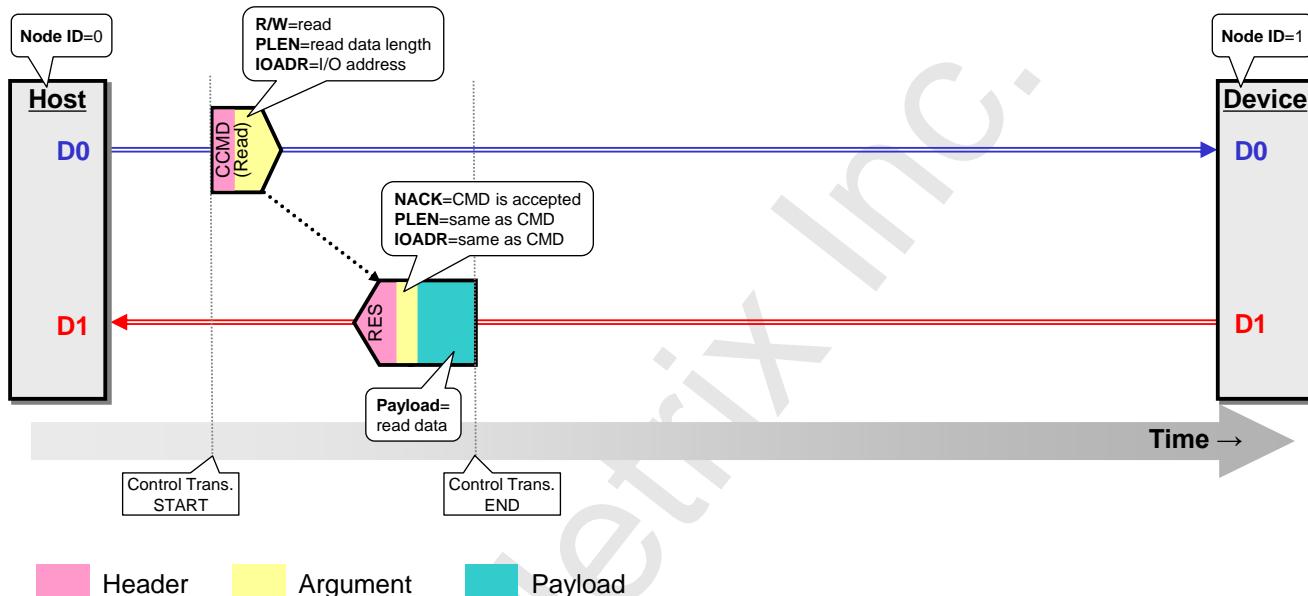


Figure 6-44 : Example Sequence of Control Read Transaction

Host issues a CCMD to obtain the I/O register values from Device (control read operation).

In control read operation, requested read data (I/O register values) is assigned in payload field in RES associated with the corresponding CCMD, and sent to Host from Device.

The detailed field values of CCMD in Figure 6-44 are as follows;

- **Header (CCMD):**

- NP = 1 (native protocol)
- Packet Type = CCMD
- DID = 1 (Node ID of destination Device)
- SID = 0 (Node ID of Host)
- TID = Transaction ID decided by Host

- **Argument (CCMD):**

- R/W = read
- PLEN = read data length
- IOADR = the I/O space address to read data

- **Payload (CCMD):**

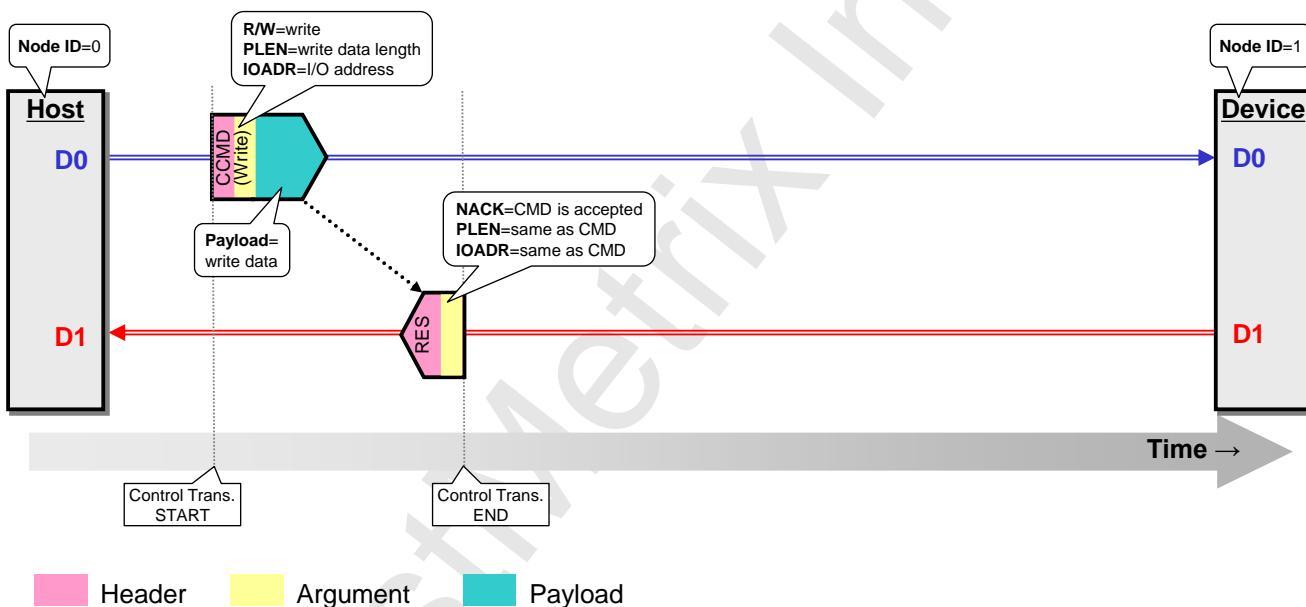
- In the case of control read operation, payload field in CCMD does not exist.

The detailed field values of RES associated with CCMD in Figure 6-44 are as follows;

- **Header (RES):**

- NP = 1 (native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding CCMD)
- SID = 1 (Node ID of Device)
- TID = the same value as TID in the corresponding CCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - PLEN = the same value as PLEN in the corresponding CCMD
  - IOADR = the same value as IOADR in the corresponding CCMD
- **Payload (RES):**
  - Requested read data by Host.
  - In the case that PLEN=0 in the corresponding CCMD, this field does not exist.

Figure 6-45 illustrates an example sequence of control write transaction.



**Figure 6-45 : Example Sequence of Control Write Transaction**

Host issues a CCMD to configure the I/O register values of Device (control write operation). In control write operation, write data transferred to I/O register is assigned in payload field in the CCMD, and sent to Device from Host.

The detailed field values of CCMD in Figure 6-45 are as follows;

- **Header (CCMD):**
  - NP = 1 (native protocol)
  - Packet Type = CCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (CCMD):**
  - R/W = Write
  - PLEN = write data length
  - IOADR = the I/O space address to write data

- Payload (CCMD):**

- Write data to be transferred to I/O register in Device.
- In the case that PLEN=0, this field does not exist.

The detailed field values of RES associated with CCMD in Figure 6-45 are as follows;

- Header (RES):**

- NP = 1 (native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding CCMD)
- SID = 1 (Node ID of Device)
- TID = the same value as TID of the corresponding CCMD

- Argument (RES):**

- NACK = 0 (the corresponding CMD is accepted)
- PLEN = the same value as PLEN in the corresponding CCMD
- IOADR = the same value as IOADR in the corresponding CCMD

- Payload (RES):**

- In the case of control write operation, payload field in RES does not exist.

### 6.2.14.2 Data Transaction Sequence (Outline)

In this section, some data transaction sequences are described only by TLP.

Figure 6-46 illustrates an example sequence of data read transaction (LM = 1 and TLUM = 0).

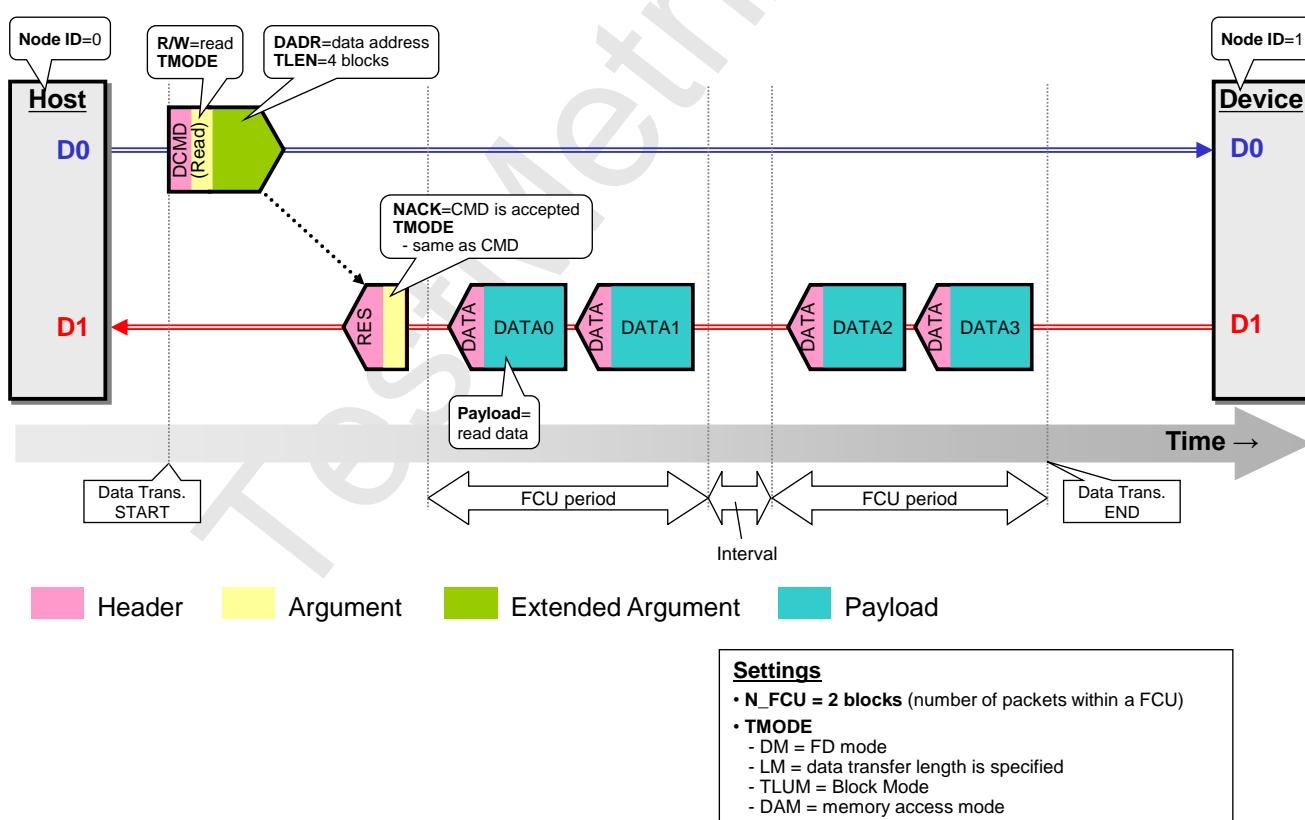


Figure 6-46 : Example Sequence of Data Read Transaction (LM = 1, TLUM = 0)

Host issues a DCMD (read) to obtain the data in memory address space or UHS-II I/O address space (data read operation). The requested read data is assigned in Payload field of DATA and sent to Host

from Device.

In the case that Host issues a DCMD with LM = 1, and in this case, TLEN field exists.

The detailed field values of DCMD (read) in Figure 6-46 are as follows;

- **Header (DCMD):**

- NP = 1 (native protocol)
- Packet Type = DCMD
- DID = 1 (Node ID of destination Device)
- SID = 0 (Node ID of Host)
- TID = Transaction ID decided by Host

- **Argument (DCMD):**

- R/W = Read
- [TMODE]
  - DM = FD mode (It depends on whether Host chooses "FD mode" or "2L-HD mode" for data transfer mode.)
  - LM = Data transfer length is specified (TLEN field in Extended Argument exists.)
  - TLUM = Block Mode.
  - DAM = Memory access mode

- **Extended Argument (DCMD):**

- DADR = Address of Memory address space for read data (DAM = 0)
- TLEN = 4 blocks (total length of data transferred during a data transaction)

The detailed field values of RES associated with DCMD (read) in Figure 6-46 are as follows;

- **Header (RES):**

- NP = 1 (native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding DCMD)
- SID = 1 (Node ID of Device)
- TID = the same value as TID of the corresponding DCMD

- **Argument (RES):**

- NACK = 0 (the corresponding CMD is accepted)
- TMODE = the same value as TMODE of the corresponding DCMD

- **Payload (RES):**

- In the case of data transaction, payload field in RES does not exist.

The detailed field values of DATA in Figure 6-46 are as follows;

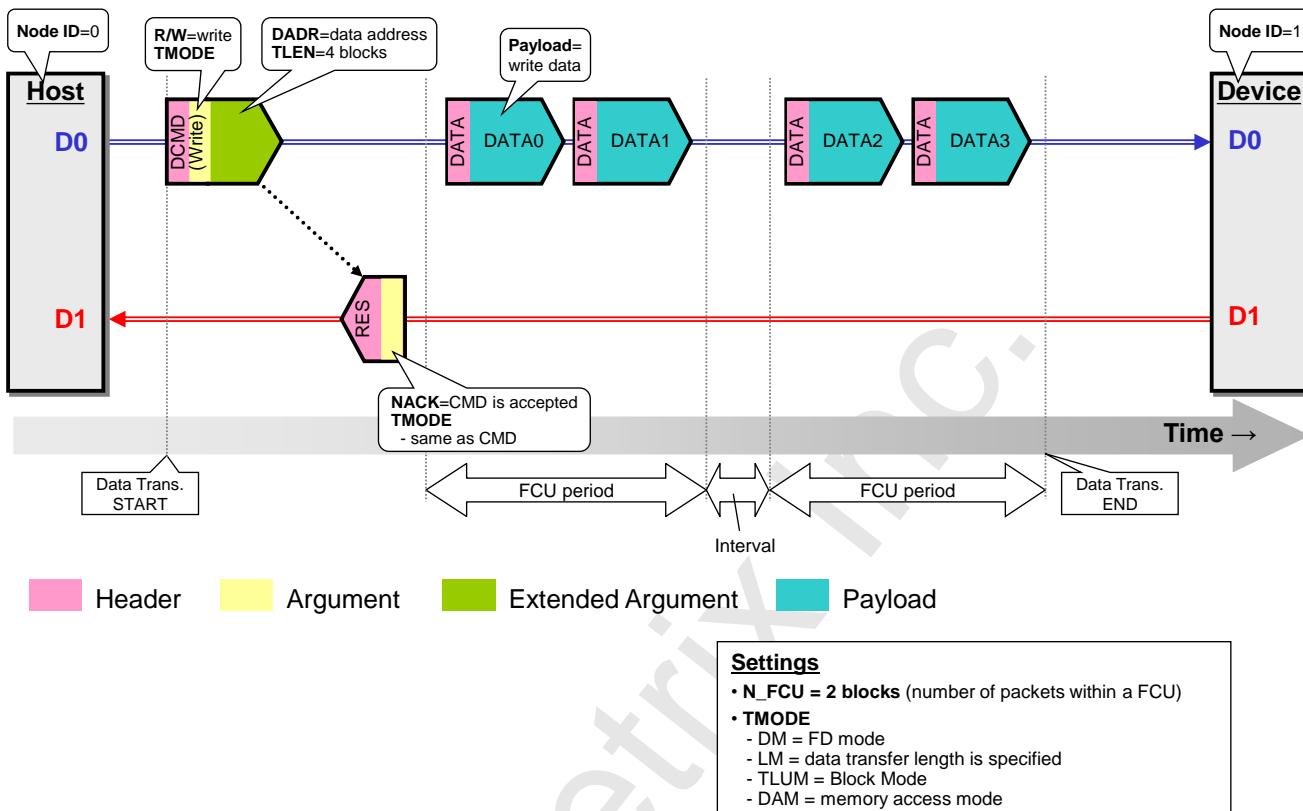
- **Header (DATA):**

- NP = 1 (native protocol)
- Packet Type = DATA
- DID = 0 (Node ID of Host)
- SID = 1 (Node ID of source Device)
- TID = the same value as TID of the corresponding DCMD

- **Payload (DATA):** requested read data by Host

In this case, Host is not required to issue TRANS\_ABORT CCMD to terminate the data transmission.

Figure 6-47 illustrates an example sequence of data write transaction ( $LM = 1$  and  $TLUM = 0$ ).



**Figure 6-47 : Example Sequence of Data Write Transaction ( $LM = 1$ ,  $TLUM = 0$ )**

Host issues a DCMD (write) to update or store data in memory address space or I/O address space (data write operation). The prepared write data is assigned in Payload field of DATA and sent to Device from Host.

The detailed field values of DCMD (write) in Figure 6-47 are as follows;

- Header (DCMD):**
  - NP = 1 (native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- Argument (DCMD):**
  - R/W = Write
  - [TMODE]
    - DM = FD mode (It depends on whether Host chooses "FD mode" or "2L-HD mode" for data transfer mode.)
    - LM = Data transfer length is specified (TLEN field in Extended Argument exists.)
    - TLUM = Block Mode.
    - DAM = Memory access mode.
- Extended Argument (DCMD):**
  - DADDR = Address of Memory address space for write data (DAM = 0).
  - TLEN = 4 blocks (total length of data transferred during a data transaction)

The detailed field values of RES associated with DCMD (write) in Figure 6-47 are as follows;

- **Header (RES):**
  - NP = 1 (native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - TMODE = the same value as TMODE of the corresponding DCMD
- **Payload (RES):**
  - In the case of data transaction, payload field in RES does not exist.

The detailed field values of DATA in Figure 6-47 are as follows;

- **Header (DATA):**
  - NP = 1 (native protocol)
  - Packet Type = DATA
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Payload (DATA):** transferred write data to Device

In this case, Host is not required to issue TRANS\_ABORT CCMD to terminate the data transmission.

Figure 6-48 illustrates an example sequence of data write transaction (LM = 1, TLUM = 1).

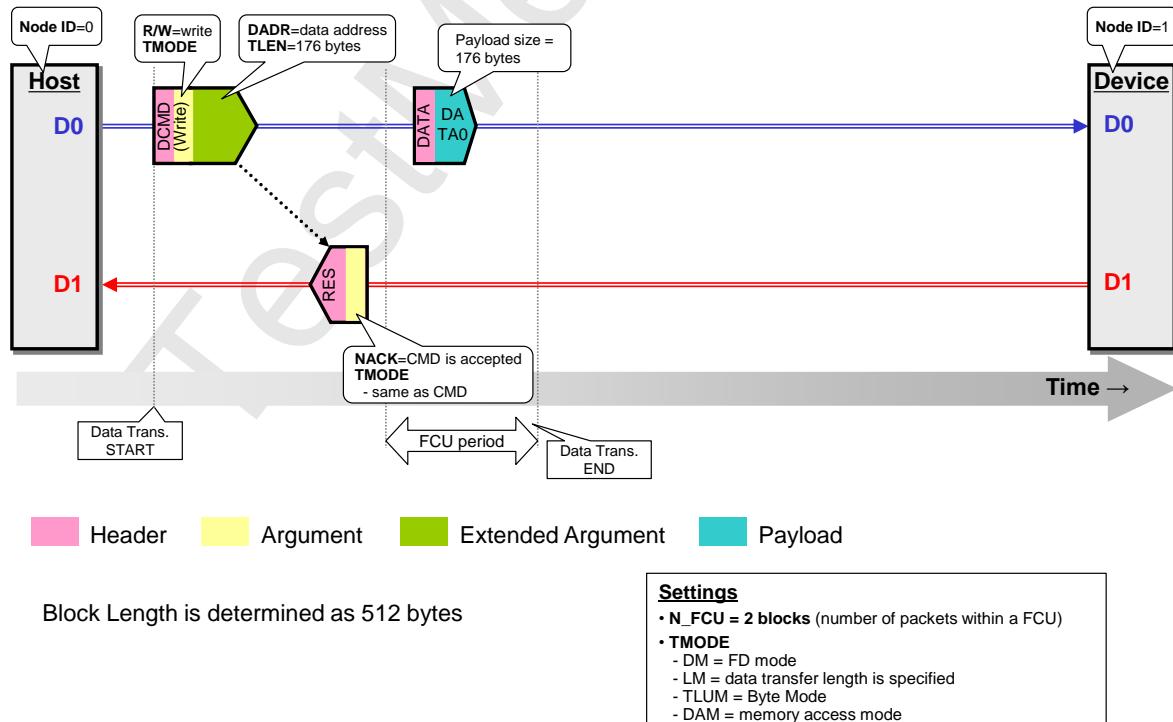


Figure 6-48 : Example Sequence of Data Write Transaction (LM = 1, TLUM = 1)

As mentioned in Section 5.2.6.2.2 TLEN shall be less than or equal to Block Length. So in this example, only one DATA whose payload size is 176 bytes is transmitted in FCU period, and then the transaction finishes without TRANS\_ABORT CCMD.

In this case, LM shall be 1. Otherwise, the DCMD shall be regarded as illegal (ARG\_ERR).

The detailed field values of DCMD (write) in Figure 6-48 are as follows;

- **Header (DCMD):**

- NP = 1 (native protocol)
- Packet Type = DCMD
- DID = 1 (Node ID of destination Device)
- SID = 0 (Node ID of Host)
- TID = Transaction ID decided by Host

- **Argument (DCMD):**

- R/W = write
- [TMODE]
  - DM = FD mode (It depends on whether Host chooses "FD mode" or "2L-HD mode" for data transfer mode.)
  - LM = Data transfer length is specified (TLEN field in Extended Argument exists.)
  - TLUM = Byte Mode
  - DAM = Memory access mode.

- **Extended Argument (DCMD):**

- DADR = Address of Memory address space for write data (DAM = 0).
- TLEN = 176 bytes (total length in byte of data transferred during a data transaction)

The detailed field values of RES associated with DCMD (write) in Figure 6-48 are as follows;

- **Header (RES):**

- NP = 1 (native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding DCMD)
- SID = 1 (Node ID of Device)
- TID = the same value as TID of the corresponding DCMD

- **Argument (RES):**

- NACK = 0 (the corresponding CMD is accepted)
- [TMODE]
  - TMODE = the same value as TMODE of the corresponding DCMD

- **Payload (RES):**

- In the case of data transaction, payload field in RES does not exist.

The detailed field values of DATA in Figure 6-48 are as follows;

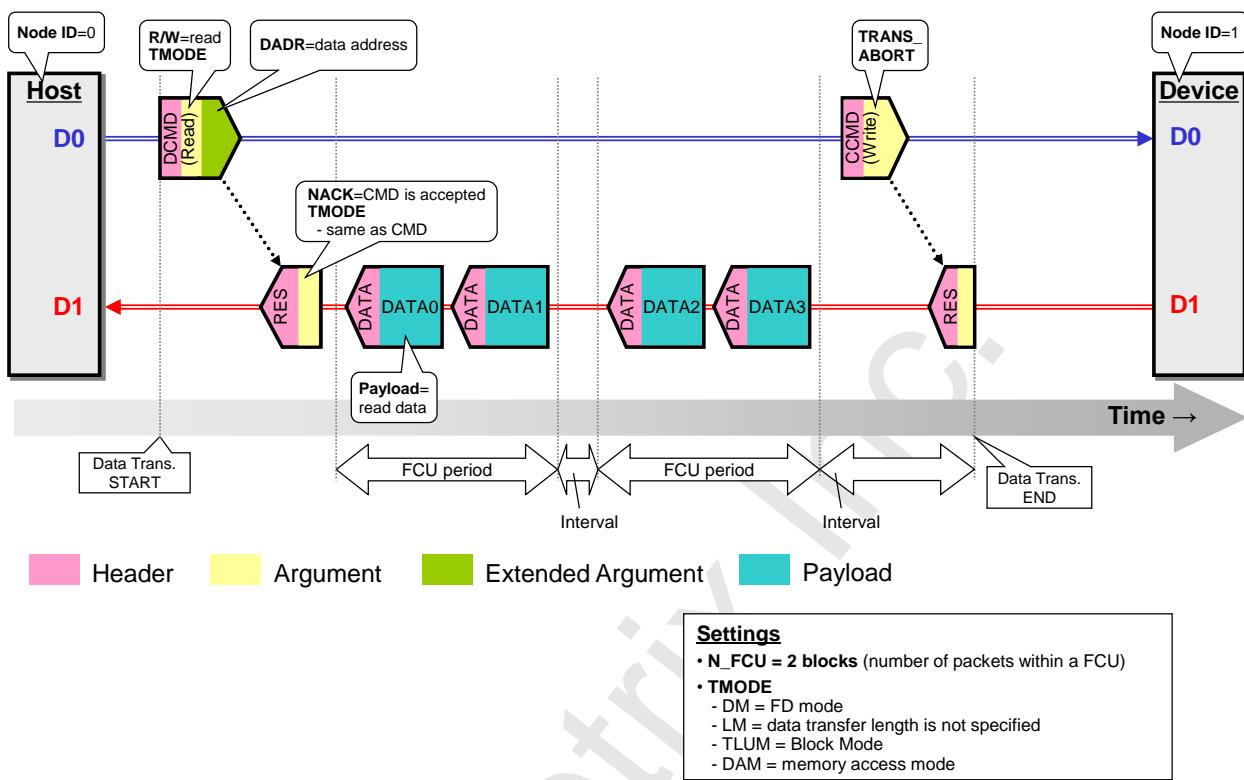
- **Header (DATA):**

- NP = 1 (native protocol)
- Packet Type = DATA
- DID = 1 (Node ID of destination Device)
- SID = 0 (Node ID of Host)
- TID = Transaction ID decided by Host

- **Payload (DATA):** Transferred write data to Device. Payload size of the DATA packet (DATA0) is 176 bytes.

In this case, Host is not required to issue TRANS\_ABORT CCMD to terminate the data transmission.

Figure 6-49 illustrates an example sequence of data read transaction (LM = 0).



**Figure 6-49 : Example Sequence of Data Read Transaction (LM = 0)**

In the case that Host issues a DCMD for infinite data transfer, LM in DCMD is set to '0' (data transfer length is not specified) and TLEN field does not exist. In this case, Host shall issue TRANS\_ABORT CCMD during interval period (CTS in other words) to terminate data transaction.

The detailed field values of DCMD (read) in Figure 6-49 are as follows;

- **Header (DCMD):**
  - NP = 1 (native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**
  - R/W = Read
  - [TMODE]
    - DM = FD mode (It depends on whether Host chooses "FD mode" or "2L-HD mode" for data transfer mode.)
    - LM = Data transfer length is not specified (TLEN field in Extended Argument does not exist.)
    - TLUM = Block Mode (Note that TLUM shall be Block Mode if LM = 0)
    - DAM = Memory access mode.
- **Extended Argument (DCMD):**
  - DADR = Address of Memory address space for read data (DAM = 0)

The detailed field values of RES associated with DCMD (read) in Figure 6-49 are as follows;

- **Header (RES):**
  - NP = 1 (native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - TMODE = the same value as TMODE of the corresponding DCMD
- **Payload (RES):**
  - In the case of data transaction, payload field in RES does not exist.

The detailed field values of DATA in Figure 6-49 are as follows;

- **Header (DATA):**
  - NP = 1 (native protocol)
  - Packet Type = DATA
  - DID = 0 (Node ID of Host)
  - SID = 1 (Node ID of source Device)
  - TID = the same value as TID of the corresponding DCMD
- **Payload (DATA):** Requested read data by Host

#### 6.2.14.3 Data Transaction Sequence (Detail)

In this section, transaction sequences including both TLP and LMSG (Link Message Packet) are described to show the order of CMD-RES handshake, flow control, and data transmission

Figure 6-50 illustrates an example sequence of data read transaction including LMSG.

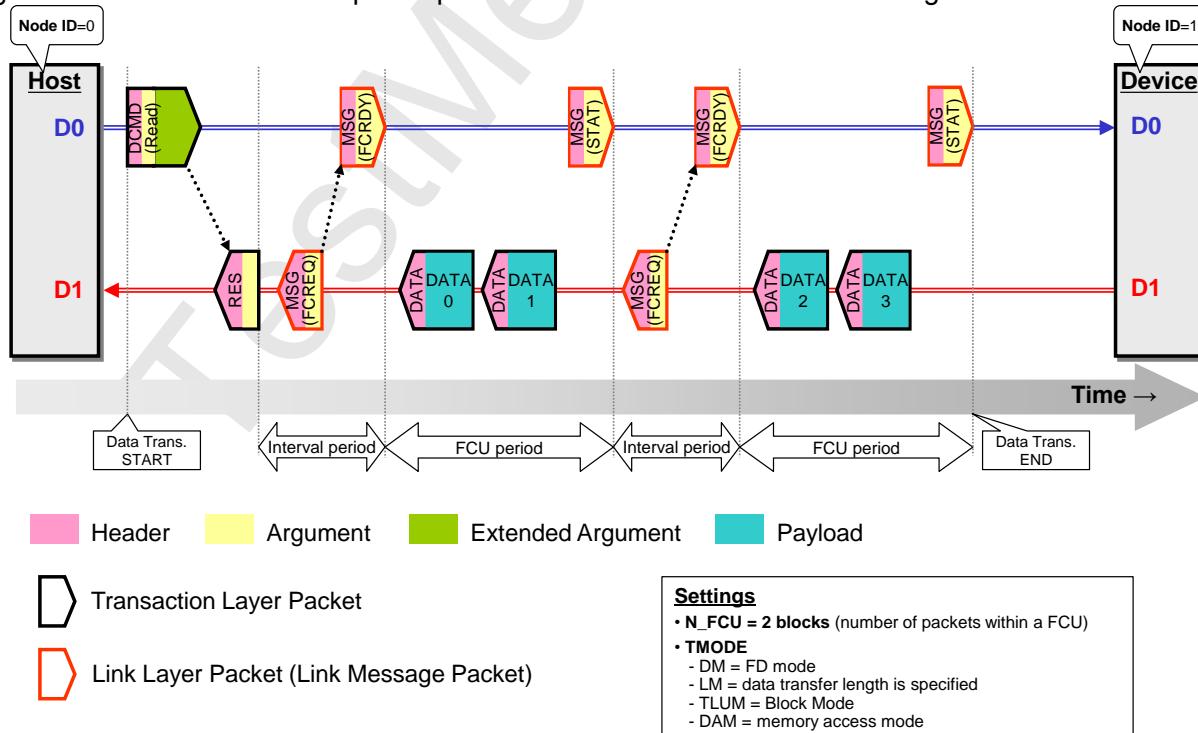
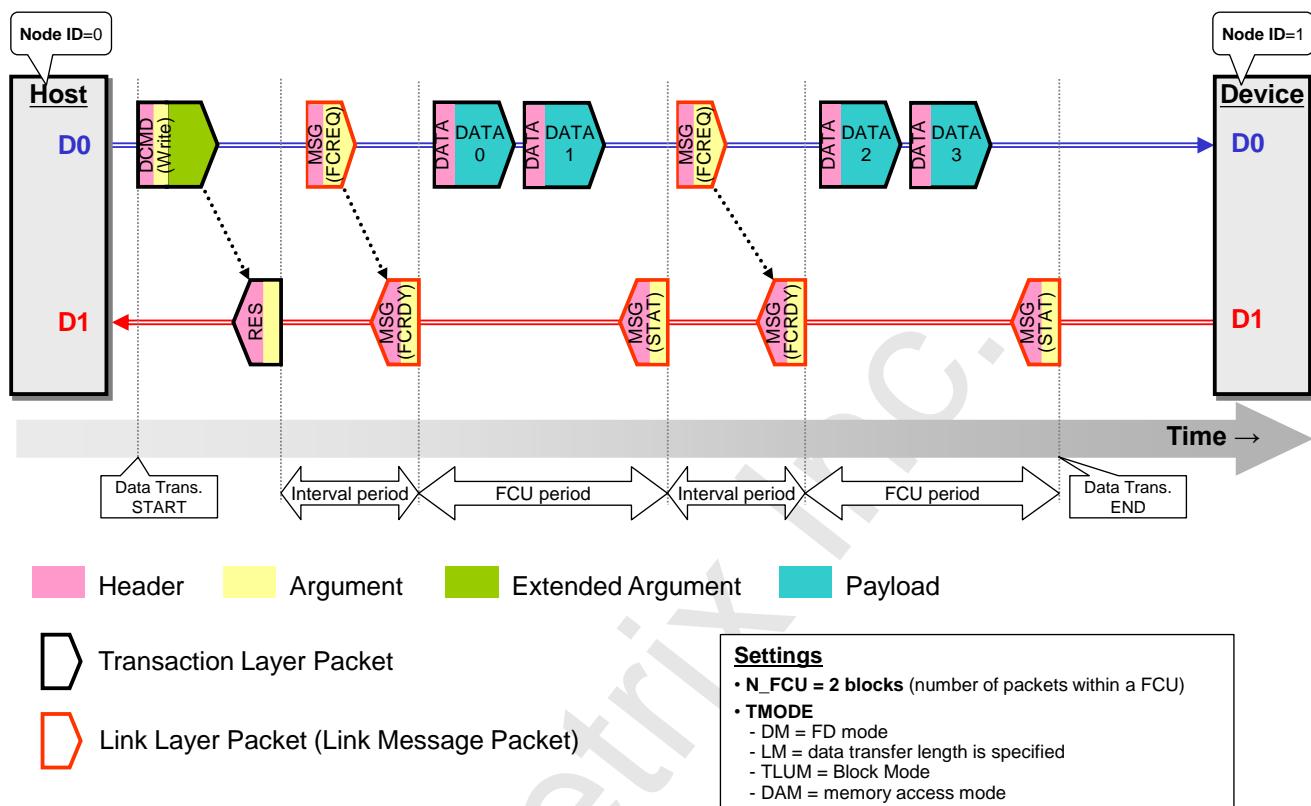


Figure 6-50 : Example Sequence of Data Read Transaction with LMSG

Figure 6-51 illustrates an example sequence of data write transaction including LMSG.



**Figure 6-51 : Example Sequence of Data Write Transaction with LMSG**

After CMD-RES handshake between Host and Device, flow control handshake is performed by FCREQ and MSG (FCRDY).

In the case that flow control handshake is done, data transfer is started and continued until N\_FCUs data packets are transmitted. (In the above example, data transfer is continued until 2 data blocks are transmitted.)

After N\_FCUs data packets transmission, MSG (STAT) including error identifier is issued from data receiver side. If there are no errors in the transferred data, flow control handshake and data transfer are performed continuously.

Both cases described in Figure 6-50 and Figure 6-51, Host is not required to issue TRANS\_ABORT CCMD to terminate the data transmission.

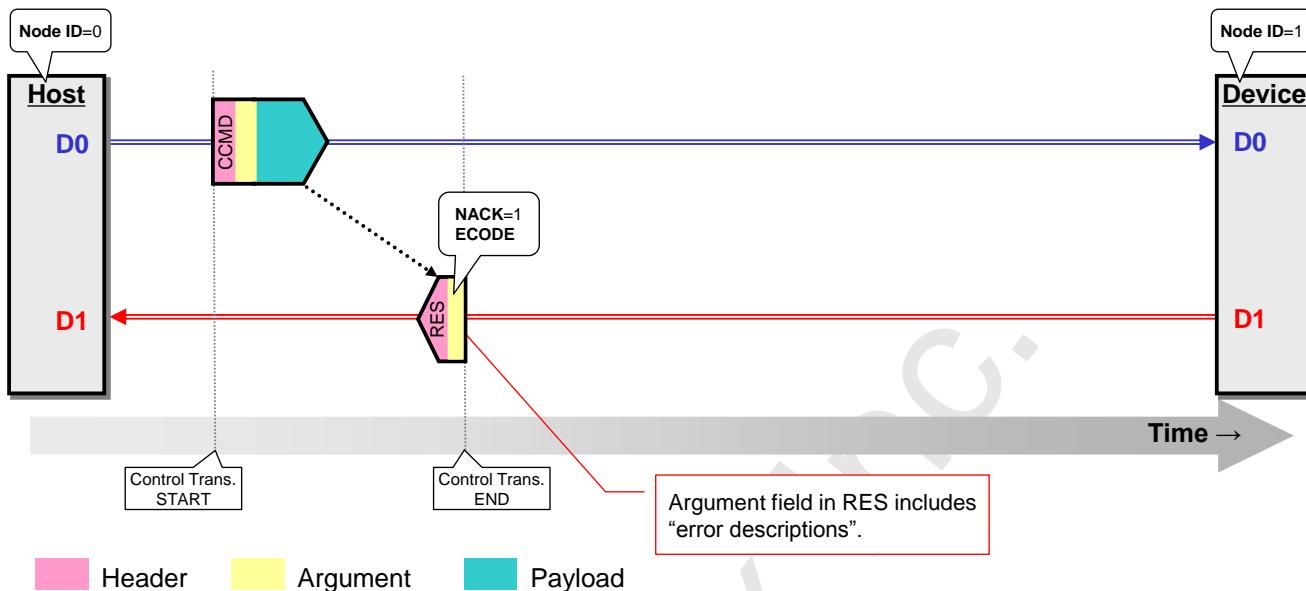
## 6.2.15 Error Handling

### 6.2.15.1 NACK Notification for Command Error

If CM-TRAN in Device detects a UHS-II command error in TP\_IDLE or TP\_INTERVAL state, Device shall send RES with NACK = 1 to Host to notify error occurrence and its descriptions immediately. As a result, the command is not performed.

ECODE can be assigned in RES (NACK = 1) as described in Table 6-4.

Figure 6-52 illustrates an example of CCMD error sequence.



**Figure 6-52 : CCMD Error Sequence**

In the case that the corresponding CCMD has an error, Device sends RES with NACK = 1 (Negative Acknowledgement) to Host to notify error occurrence and its descriptions immediately. After the RES is issued, the control transaction is finished.

The detailed field values of RES in Figure 6-52 are as follows;

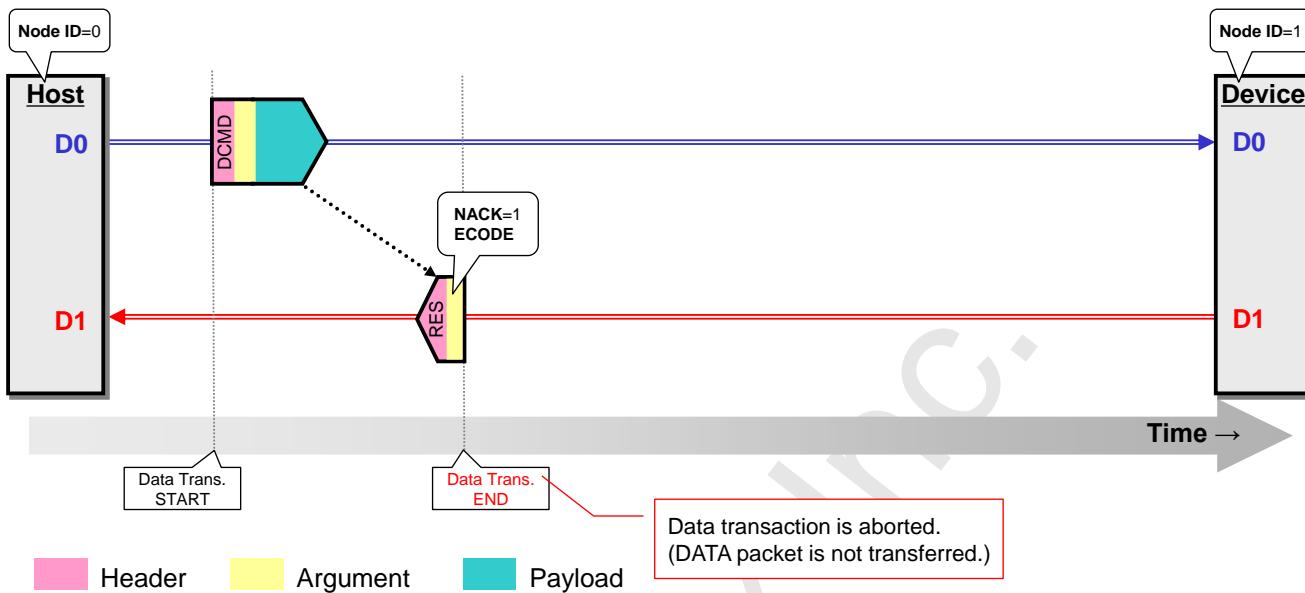
- **Argument (RES):**
  - NACK = 1 (The corresponding CCMD has an error.)
  - ECODE = (It depends on the reason of errors.)
- **Payload (RES):**
  - Payload field does not exist.

Other field values in Header are set to the same value as Header in RES (NACK = 0).

In the case of error with read CCMD, read transaction is aborted and Device sends RES (NACK = 1) without requested data.

In the case of error with write CCMD, write transaction is aborted and Device sends RES (NACK = 1). The transferred data is not written in register of Device.

Figure 6-53 illustrates an example of DCMD error sequence.



**Figure 6-53 : DCMD Error Sequence**

In the case that the corresponding DCMD has an error, Device sends RES with NACK = 1 to Host to notify error occurrence and its descriptions immediately. After the RES is issued, DATA packet is not transferred and the data transaction is aborted. Only the RES with error code in its payload field is sent to Host from Device.

The detailed field values of RES in Figure 6-53 are as follows;

- **Argument (RES):**
  - NACK = 1 (The corresponding DCMD has an error.)
  - ECODE = (It depends on error cause.)
- **Payload (RES):**
  - Payload field does not exist.

Other field values in Header are set to the same value as Header in RES (NACK = 0).

### 6.2.15.2 Error Notification during Data Transaction

DATA Burst error notification takes place by STAT MSG, and DATA Burst Retry takes place as described in Section 5.5.4.

Figure 6-54 illustrates an example of DATA read sequence when Host detects UNRECOVERABLE\_ERROR from receiving DATA Burst. In this example, Host shall issue STAT MSG with UNRECOVERABLE\_ERROR = 1 and should issue TRANS\_ABORT CCMD to terminate the data transaction.

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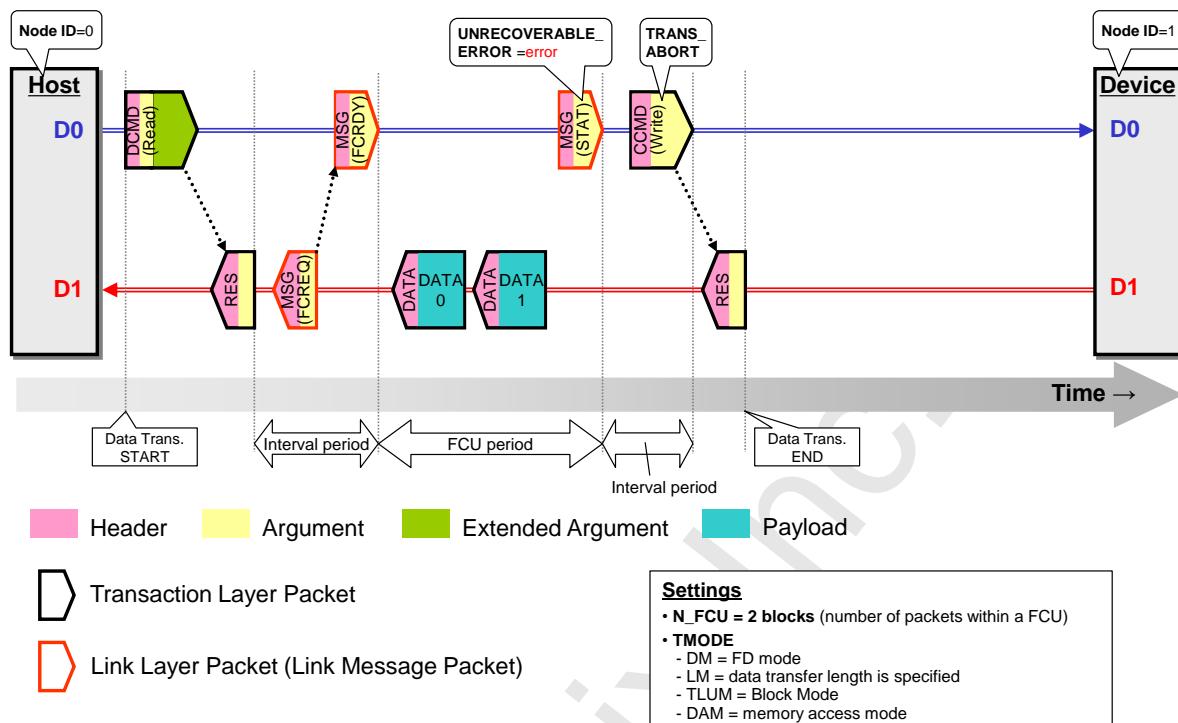


Figure 6-54 : Example Sequence Including UNRECOVERABLE\_ERROR with Read Data Packet

Figure 6-55 illustrates an example of DATA write sequence when Host detects UNRECOVERABLE\_ERROR from receiving STAT MSG. In this example, Host should issue TRANS\_ABORT CCMD to terminate the data transaction.

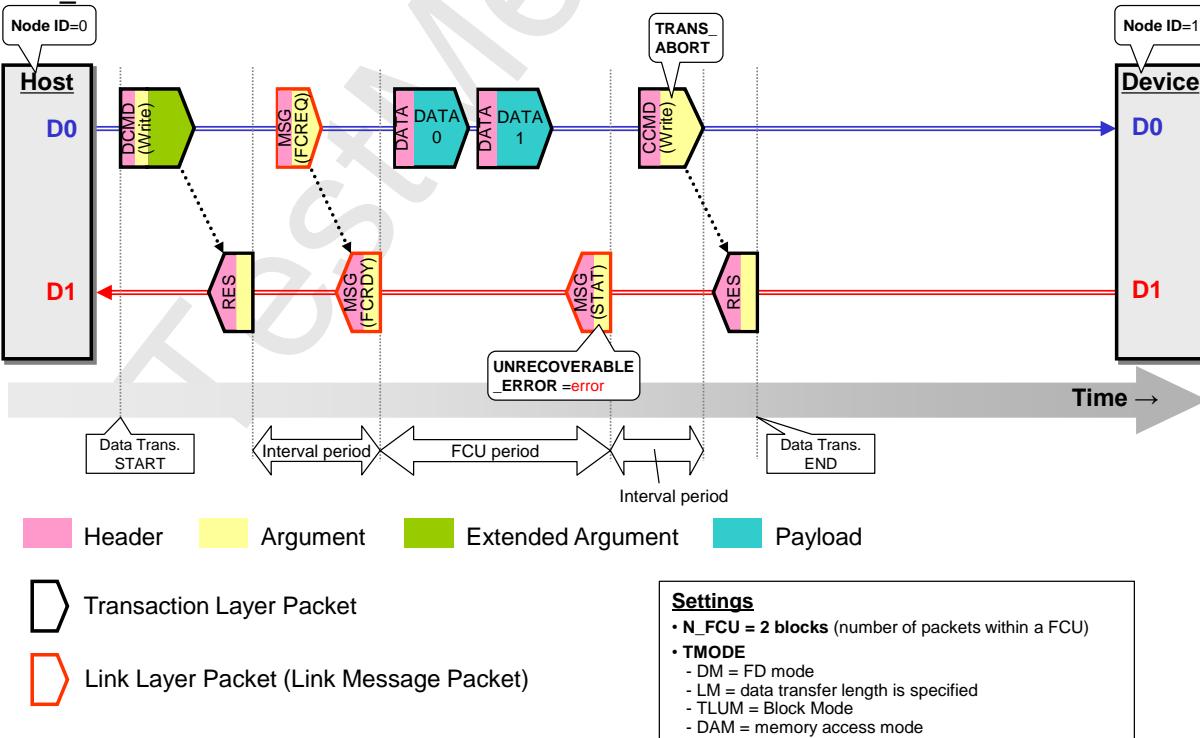
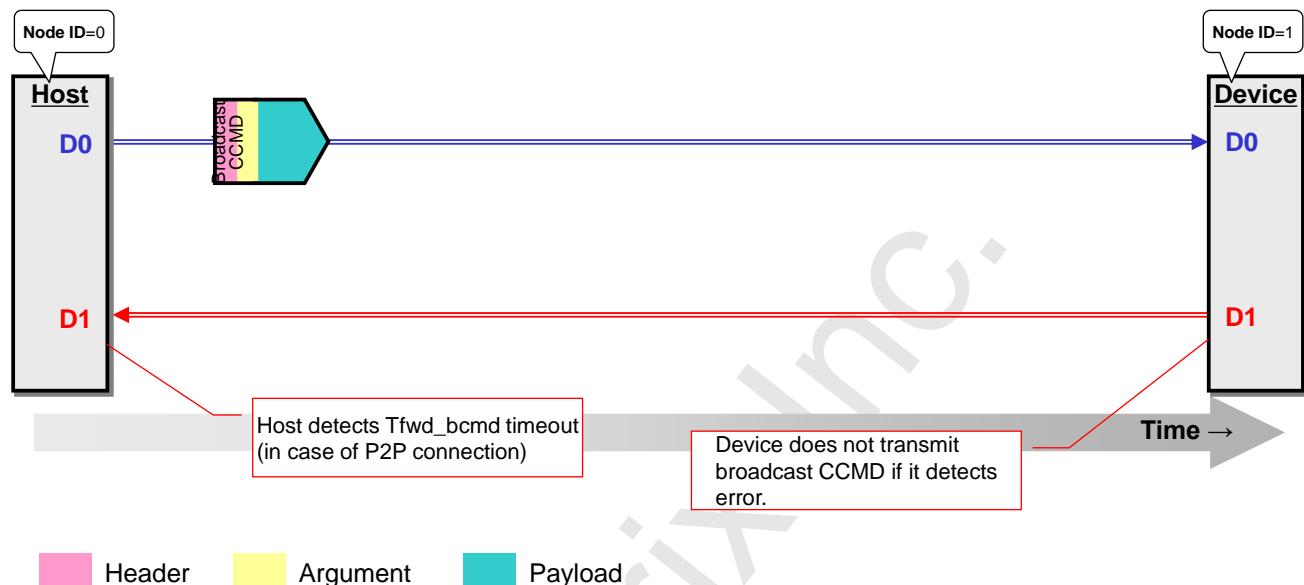


Figure 6-55 : Example Sequence Including UNRECOVERABLE\_ERROR with Write Data Packet

### 6.2.15.3 Error Detection from Broadcast CCMD

As mentioned in Section 6.2.2.3, if Device detects some error from receiving broadcast CCMD, it does not transmit the command to the next node.

Figure 6-56 illustrates a sequence when Device detects error from broadcast CCMD.

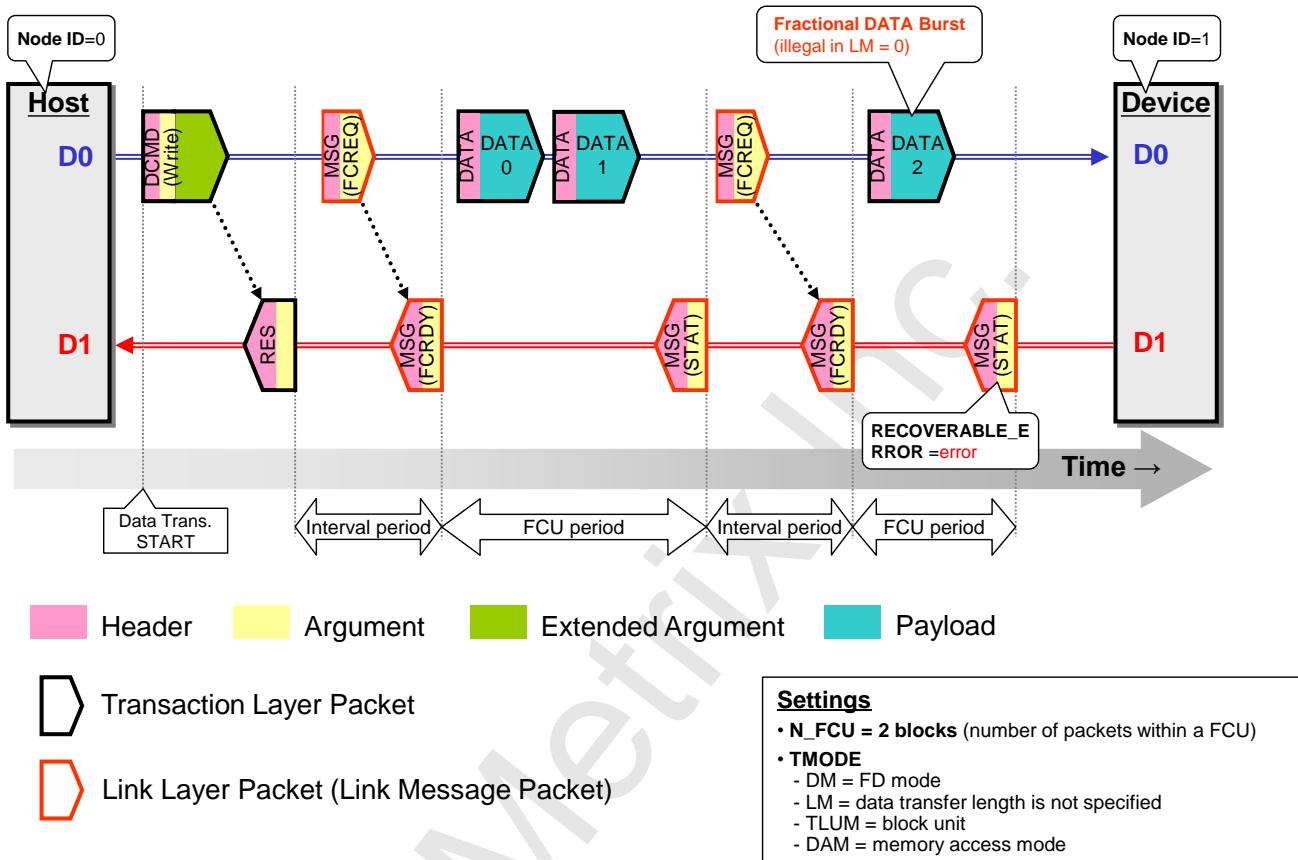


**Figure 6-56 : Sequence in Case of Error Detection from Broadcast CCMD**

In this case, Host can detect the error on the broadcast CCMD by timeout which is estimated by Tfwd\_bcmb (refer to Table 6-25) and the number of connected Devices.

### 6.2.15.4 Fractional DATA Burst in LM = 0

Figure 6-57 illustrates an example sequence of data write transaction if fractional DATA Burst is transmitted in LM = 0.



**Figure 6-57 : Example Sequence of Write Transaction with Fractional DATA Burst in LM = 0**

As mentioned in Section 5.2.6.2, fractional DATA Burst is permitted only in LM = 1 except when the data transfer length is determined by another means. So If Device detects that DATA2 is fractional DATA Burst, Device regards as FRAME\_ERROR and transmits MSG (STAT) with RECOVERABLE\_ERROR = error.

## 6.3 Timing Rules

### 6.3.1 Overview

Device shall keep the following timing rules and Host should detect errors by timeout.

If Host detects that one of these rules is violated, it transits its DLSM to Active.Control, then it issues TRANS\_ABORT CCMD after transmitting LIDL or EIDL according to the setting of "Power Control Mode in Active.Control State". If it fails to receive RES of TRANS\_ABORT, it should manage to recover from the illegal situation by other means (for example, by taking place I/F power cycle). These timing rules are given for a single UHS-II Device, and note that Host shall consider accumulated timings in case of Multi-device connection.

From Device's point of view, Device shall respond for TRANS\_ABORT CCMD during TP\_IDLE state or CTS, and otherwise, it responds if it can recognize the CCMD.

Table 6-25 shows Device timing parameters, and Figure 6-58 and Figure 6-59 illustrates the period for applying the timing rules for some parameter groups. Host estimates system's timeout values according to Table 6-25.

Group	Abbreviation	Description	Max Value
Wakeup	Teidl_stb	Time from first STB, after EIDL, on Device Rx to STB on Device Tx.	200 [usec]
	Tactivate	Time from first STB on Device Tx to first SYN LSS on Device Tx.	100 [msec] (at the first time after power up, or in case of recovering from Hibernate mode. See Note (1)) 2 [msec] (otherwise)
	Tlidl_lidl	Time from LIDL on Device Rx to LIDL on Device Tx.	750 [RCLK cycle]
	Tlidl_freq_boot	Time from LIDL on Boot Device Rx to the first SOP FCREQ for the Boot Code on Boot Device Tx.	1 [sec]
Initialization	Tfwd_init_cmd	Time from DEVICE_INIT CCMD EOP reception on Device Rx to its SOP transmission on Device Tx	1 [sec] (See Note (1))
Basic	Tcmd_res	Time from P2P CCMD or DCMD EOP reception on Device Rx to RES SOP transmission on Device Tx.	5 [msec]
	Tfwd_bcmd	Time from broadcast CCMD (except DEVICE_INIT) EOP reception on Device Rx to its SOP transmission on Device Tx.	5 [msec]
Flow Control	Tres_freq(r)	Time from RES EOP reception to FCREQ SOP transmission in read transaction.	Defined in application specific layers (See Note (2).)
	Tres_freq(w)	Time from RES EOP reception to FCREQ SOP transmission in write transaction	N/A
	Tstat_freq(r)	Time from STAT EOP reception to FCREQ SOP transmission in read transaction. This is related to read busy timeout.	Defined in application specific layers (See Note (2).)
	Tstat_freq(w)	Time from STAT EOP reception to FCREQ SOP transmission in write transaction.	N/A
	Tfcrdy_edb	From FCRDY EOP reception to DATA Burst EDB transmission	20 [msec]
	Tfreq_fcrdy(r)	Time from FCREQ EOP reception to FCRDY SOP transmission in read transaction.	N/A
	Tfreq_fcrdy(w)	Time from FCREQ EOP reception to FCRDY SOP transmission in write transaction. This is related to write busy timeout.	Defined in application specific layers (See Note (2).)
	Tedb_stat	From DATA Burst EDB reception to STAT SOP transmission	200 [usec]

Note: (1) Device shall also satisfy the inequality  $Tactivate + Tfwd\_init\_cmd(s) + Tfwd\_init\_cmd(c) \leq 1$  [sec], where.

- $Tfwd\_init\_cmd(s)$  is duration of DEVICE\_INIT CCMD by which Device starts its Device Initialization process
- $Tfwd\_init\_cmd(c)$  is duration of DEVICE\_INIT CCMD which Device transmits at the completion of Device Initialization process.

(2) In case of SD-memory Card, refer to SD-TRAN specification (Chapter 7).

**Table 6-25 : Device Timing Parameters in CM-TRAN**

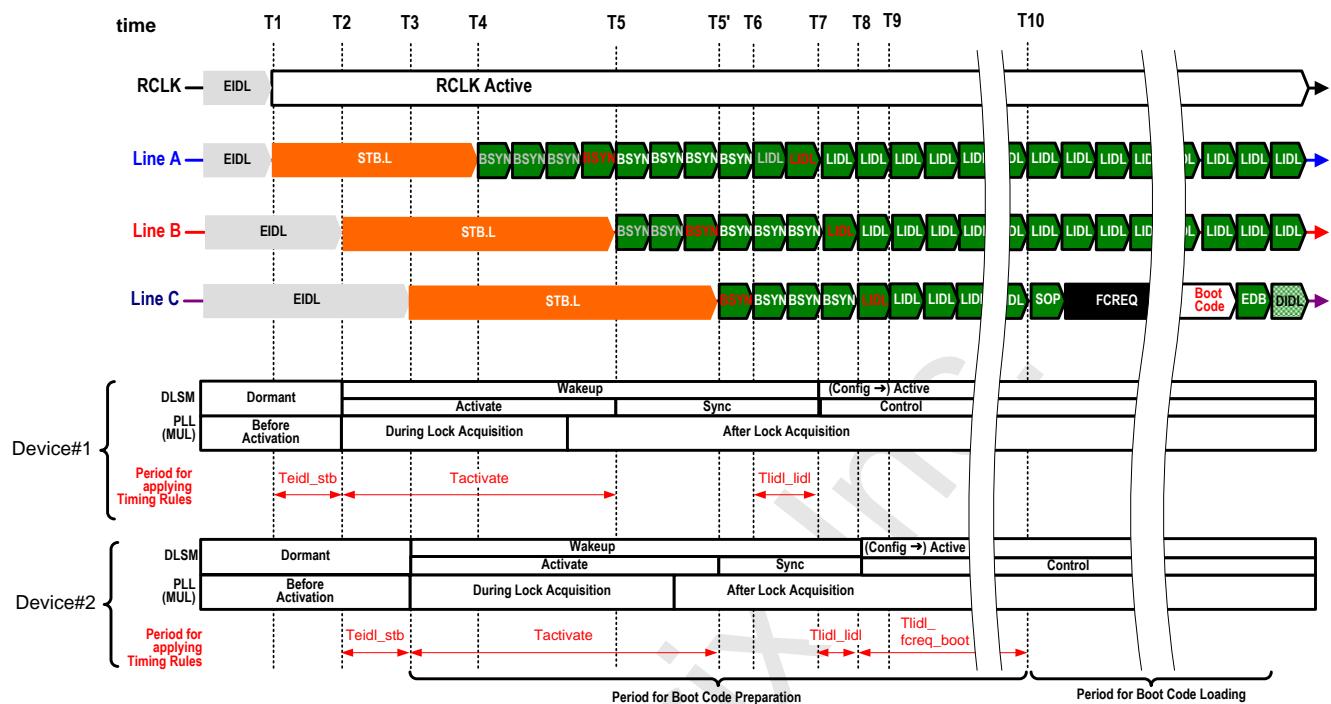


Figure 6-58 : Device Timing Parameters Related to Wakeup Group

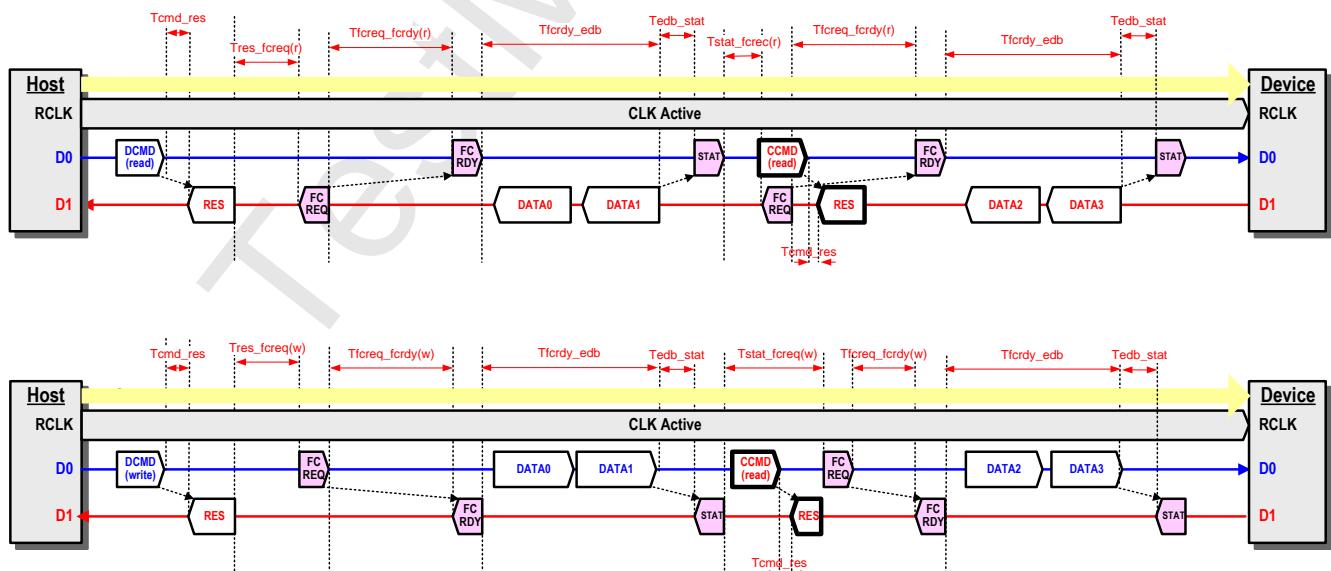
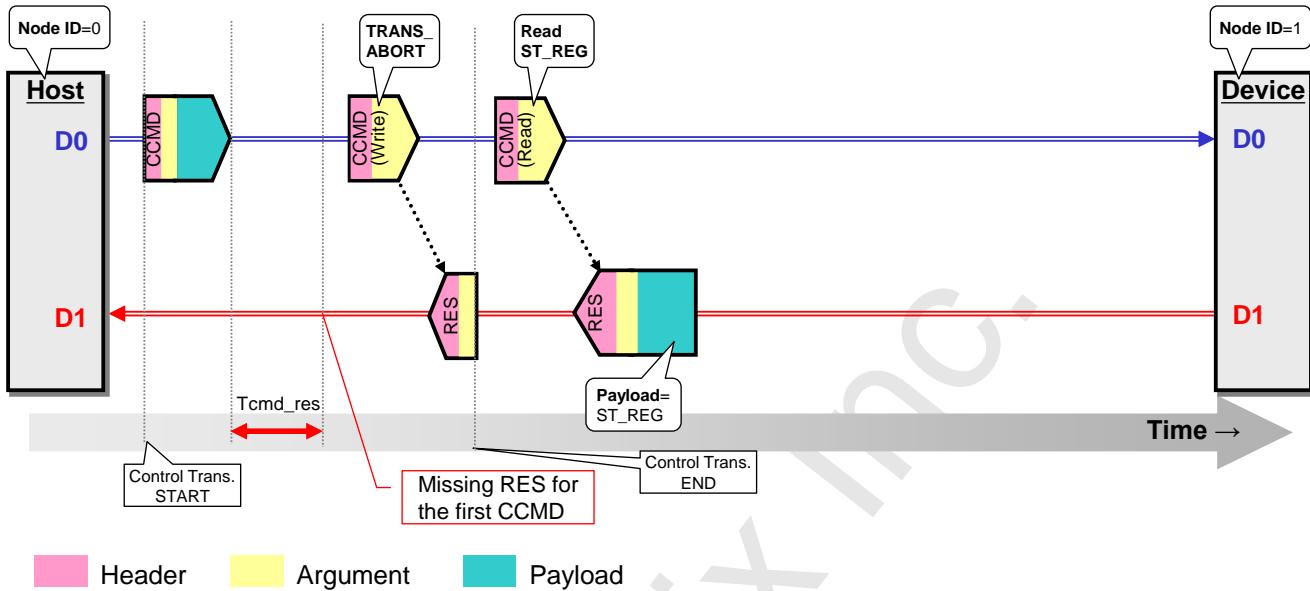


Figure 6-59 : Device Timing Parameters Related to Basic or Flow Control Group

### 6.3.2 Example Sequence of Timeout Occurrence

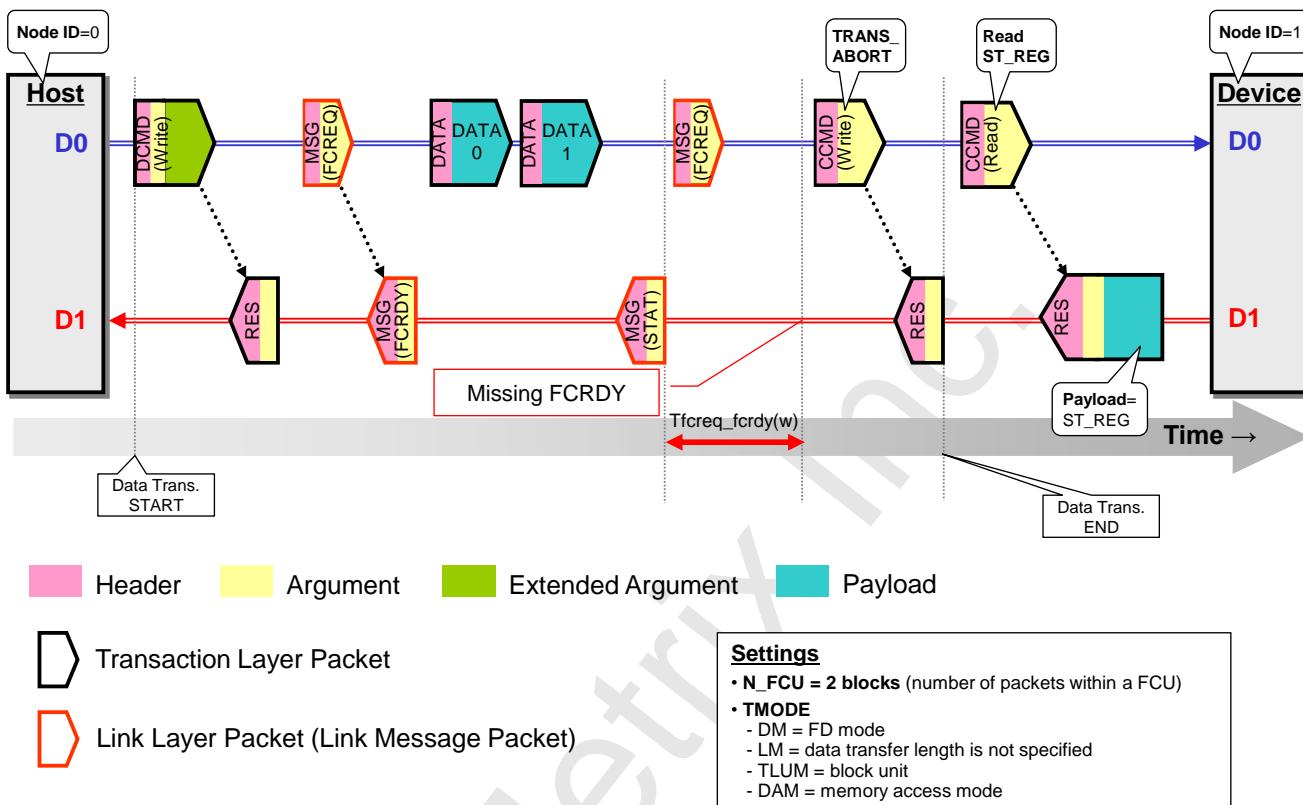
Figure 6-60 illustrates an example sequence when Host cannot receive the RES of CCMD.



**Figure 6-60 : Example Sequence When Missing RES**

When Host detects timeout of  $T_{cmd\_res}$ , Host should issue TRANS\_ABORT CCMD to terminate the first CCMD transaction. Then Host should read error identifiers and status of Device indicated in Device's ST\_REG.

Figure 6-61 illustrates an example sequence when Host cannot receive FCRDY MSG during data transaction.



**Figure 6-61 : Example Sequence When Missing FCRDY during Write Transaction**

When Host detects timeout of  $T_{fcreq\_fcrdy}(w)$  during data transaction, Host should issue TRANS\_ABORT CCMD to terminate this transaction. Note that this TRANS\_ABORT also terminates the outstanding data transmission in UHS-II native protocol. In this case, transmitted data is not guaranteed. Then Host should read error identifiers and status of Device indicated in Device's ST\_REG.

## 7. SD-TRAN Specification

SD-TRAN rides over CM-TRAN and acts as bridge between Legacy SD protocol and UHS-II common protocol for SD-compatibility. This chapter presents encapsulated SD packet formats, transaction sequences, initialization for SD-TRAN, state machine, error handling and timing rules. These are based on CM-TRAN specification, but SD-memory is applied to some specific rules described in this chapter. In this case, the specific rules in SD-TRAN are effective instead of those in CM-TRAN.

In this section, UHS-II specifications for SD-memory are described, not included for SDIO.

### 7.1 SD-TRAN Overview

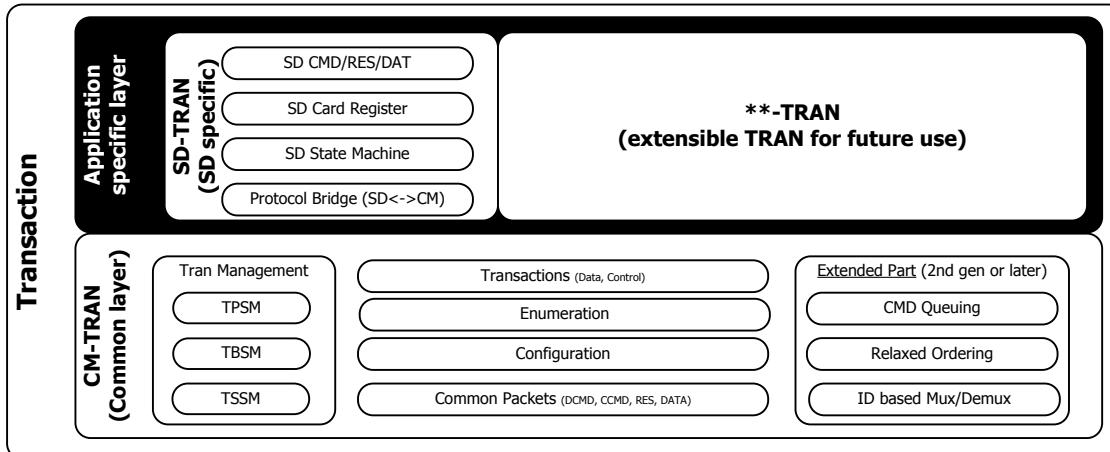


Figure 7-1 : SD-TRAN Overview

The features of SD-TRAN are shown below;

- Preserving Legacy SD infrastructures (CMD, RES, status, errors and etc.)
- Bridging between Legacy SD protocol (e.g. Host/Device register interface) and UHS-II common protocol (CM-TRAN)

#### 7.1.1 Packet Types and Format Overview

Encapsulated SD packets are defined in SD-TRAN in order to ensure Legacy SD compatibility and preserve Legacy SD infrastructures.

Conceptual diagram of SD-encapsulation is shown in Figure 7-2.

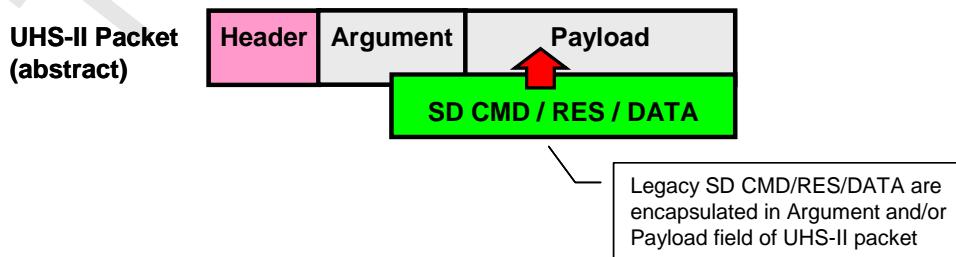


Figure 7-2 : Conceptual Diagram of SD-encapsulation

SD-encapsulation formats in each types of TLP are shown in Figure 7-3.

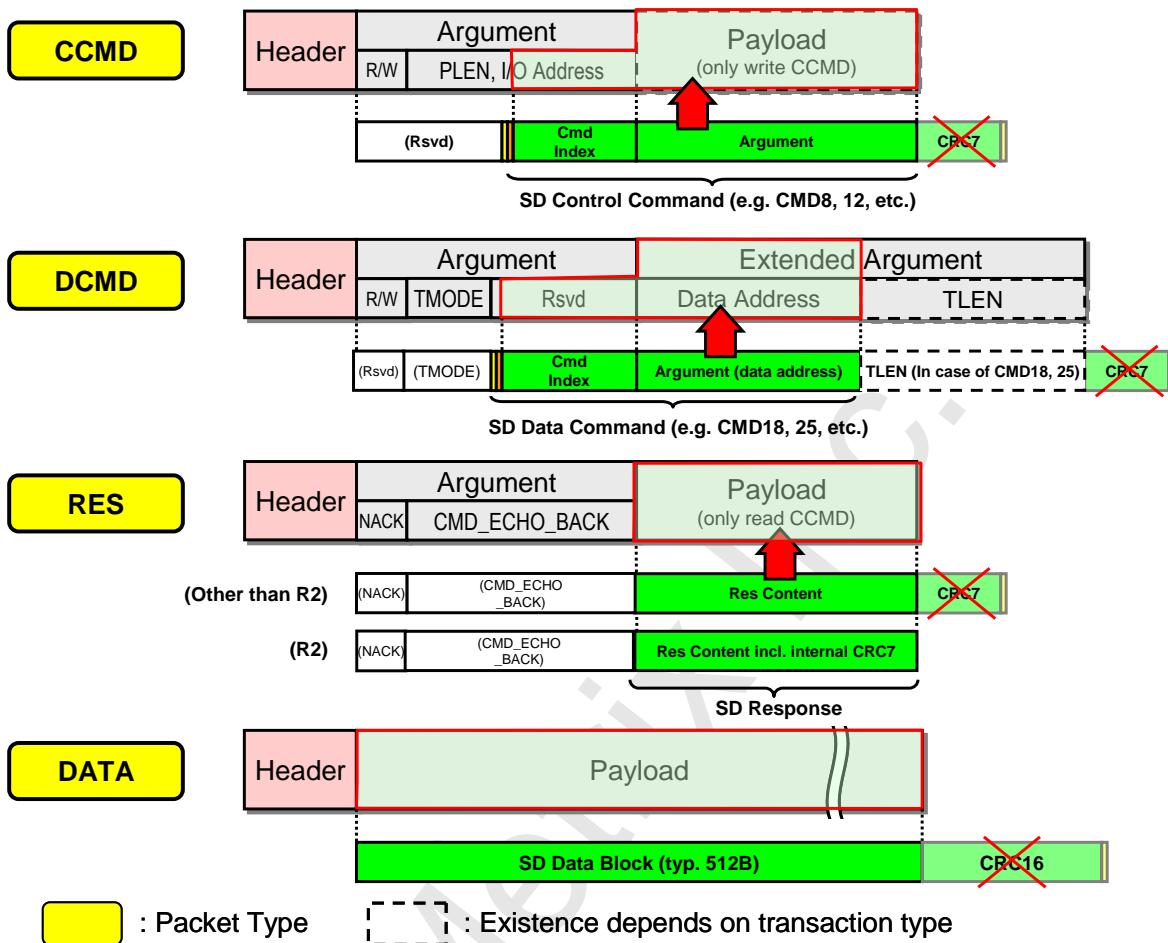


Figure 7-3 : Encapsulation of Legacy SD Format

Basically, CRC7 or CRC16 for Legacy SD are not overridden in SD-encapsulation format because all TLPs are added CRC16 in Link Layer.  
Details are described in next section.

### 7.1.2 Registers for Legacy SD

Registers for Legacy SD such as CID or CSD can be accessed only by SD encapsulated CMD. For example, when Host wants to get CID, Host sends an encapsulated CMD2 (ALL\_SEND\_CID).

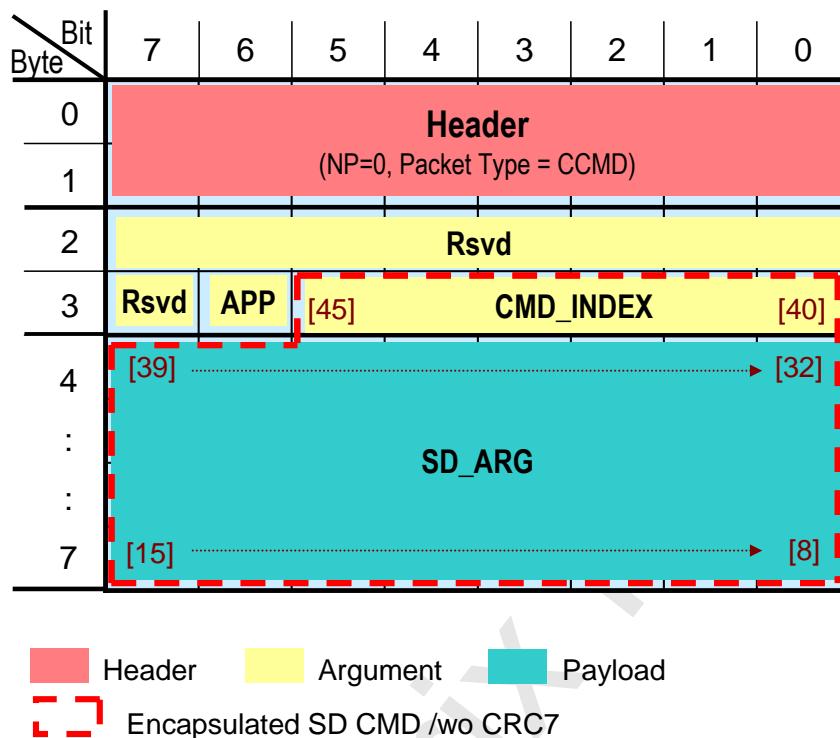
## 7.2 SD-TRAN Protocol

### 7.2.1 Packet Format Details

In this section, the bracketed number in the figures denotes the bit position in Legacy SD command or response format. Note that broadcast packet is not permitted in SD-TRAN.

#### 7.2.1.1 CCMD

Figure 7-4 illustrates CCMD on SD-TRAN.

**Figure 7-4 : CCMD Format on SD-TRAN**

- **APP:** Indicator for application command. APP = 1 means application command, otherwise regular command. Device shall regard as application command if APP = 1.
- **CMD\_INDEX[5:0]:** CMD Index in Legacy SD Command to be issued.
- **SD\_ARG:** Corresponding argument for the Legacy SD Command.
  - Notice the bit order of Payload field.
- **Rsvd (Reserved):** Reserved bits. Initiator (Host) shall set them to '0', and receiver (Device) shall ignore them.

### 7.2.1.2 DCMD

Figure 7-5 illustrates DCMD on SD-TRAN.

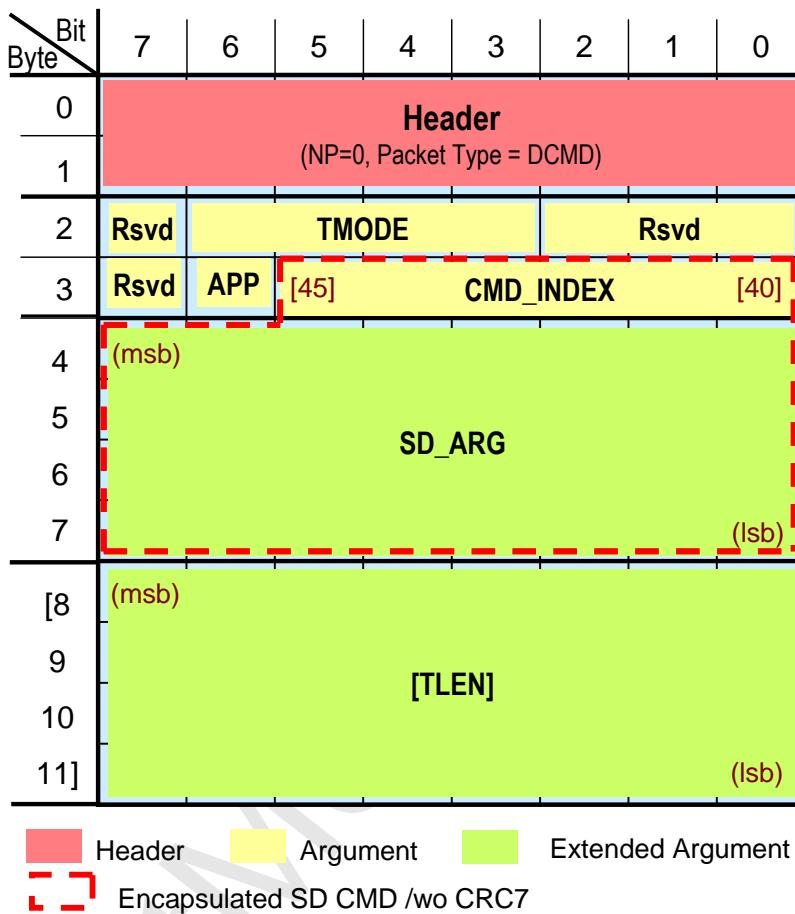


Figure 7-5 : DCMD Format on SD-TRAN

- **TMODE[3:0] (Transfer Mode):** Parameter settings for data transaction.
  - Host may set DM to 1 for DCMD which supports multi-block read / write regardless of data transfer length (e.g., CMD18, CMD25). Otherwise, it shall not set DM to 1. (e.g. CMD6, CMD17, CMD24). These rules are also applied to other multi-block read / write commands defined in other Part of SD specifications (for example, Host may set DM to 1 for ACMD18 or ACMD25).
  - LM is alternative only for CMD18 and 25, and it shall be set to 0 for other DCMDs.
  - Both DAM and TLUM shall be set to 0.
  - If Host issues DCMD with DM = 1 to Device which does not support 2L-HD mode, Device returns RES with NACK = 1.
- **APP:** Indicator for application command. APP = 1 means application command, otherwise regular command. Device shall regard as application command if APP = 1.
- **CMD\_INDEX[5:0]:** CMD Index in Legacy SD Command to be issued.
- **SD\_ARG:** Corresponding argument for the Legacy SD Command.
- **TLEN[31:0] (Transfer Length):** Total length of data transmitted during a data transaction
  - This field exists only for CMD18 or CMD25 with LM = 1, and unit of TLEN is a block (512 bytes in SD-memory). It is strongly recommended for Host to be set LM = 1 and TLEN > 0 in case of CMD18 and CMD25.

- If TLEN = 0000000h, it does not affect the data transaction (same as LM = 0).
- It is transmitted in msb first, lsb last.
- **Rsvd (Reserved):** Reserved bits. Initiator (Host) shall set them to '0', and receiver (Device) shall ignore them.

### 7.2.1.3 RES

Figure 7-6 illustrates the generic structure of RES associated with CCMD and DCMD on SD-TRAN.

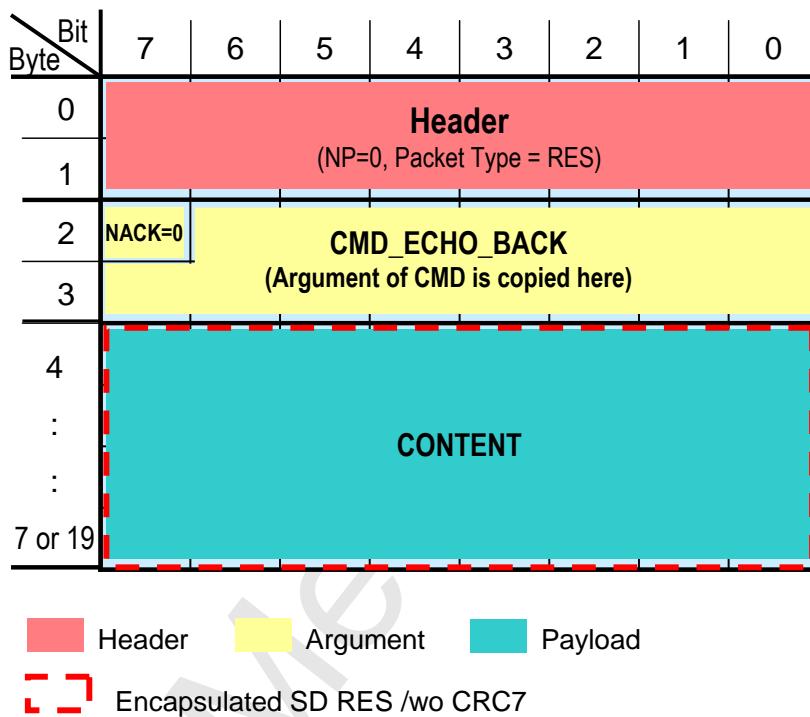
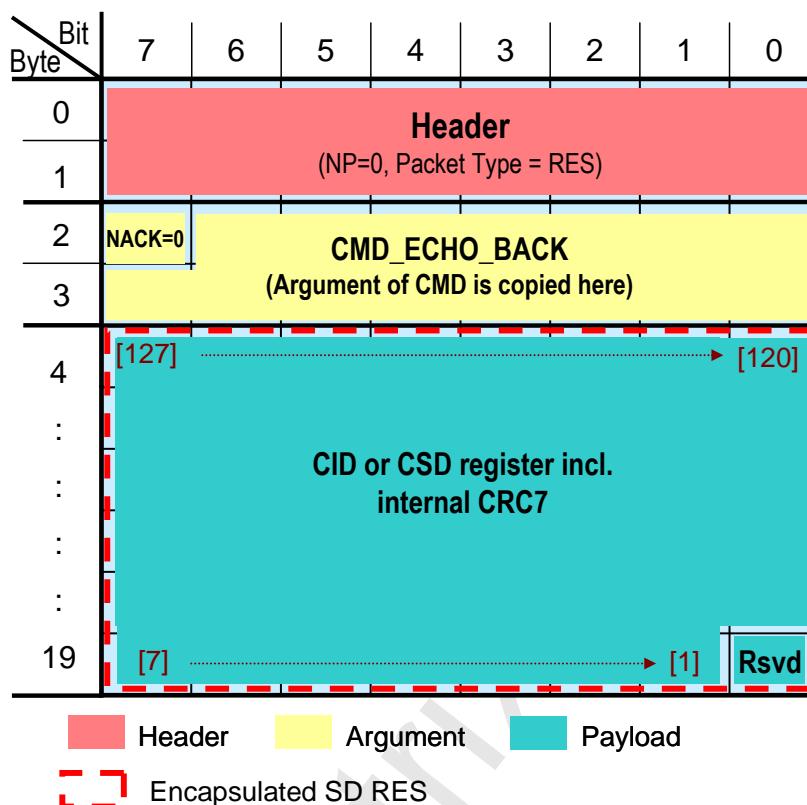


Figure 7-6 : RES Format on SD-TRAN (Generic)

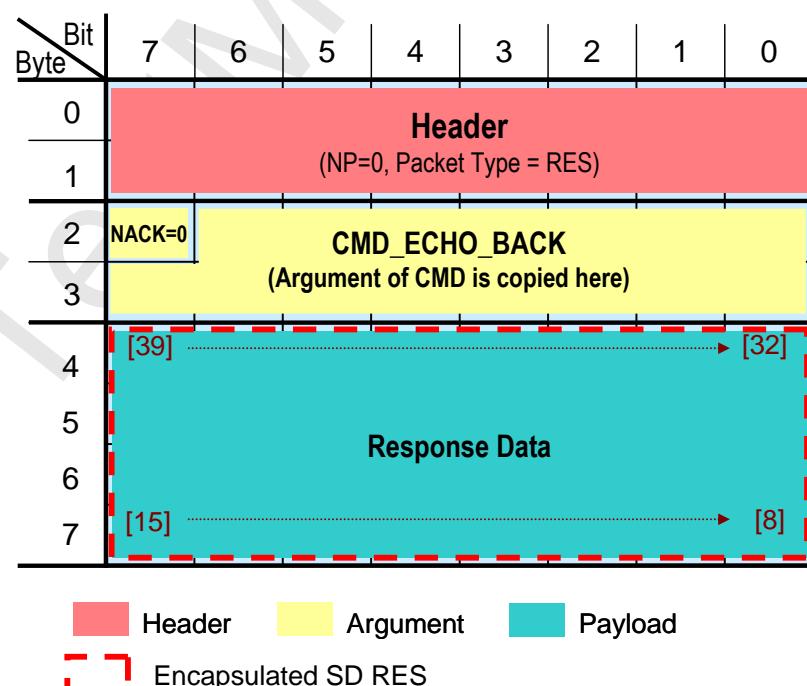
- **NACK (Negative Acknowledgement):** Indicator whether the corresponding CMD is accepted or not. In case of command error, refer to Section 7.2.1.4 and Section 7.2.8.2.
- **CMD\_ECHO\_BACK[14:0] (Command Echo Back):** Copied field of CMD Argument.
  - The same values in Argument field such as CMD\_INDEX or TMODE are copied from the corresponding CMD (echo back). Specifically, [6:0] in the second byte, and [7:0] in the third byte of CMD packet are copied to the same location of RES packet.
- **CONTENT:** Content of Response. Refer to Figure 7-7 for R2, and Figure 7-8 for other than R2 for more details. Rsvd in Figure 7-7 is reserved bits, so initiator (Device) shall set it to '0' and receiver (Host) shall ignore them.

DID field in Header is set to the same value as SID field in Header of the corresponding command. TID field in Header is set to the same value as TID field in Header of the corresponding command.



Note: In UHS-II mode, field of CRC7 in R2 response is not used to check CRC, and may be set any value

**Figure 7-7 : RES Format on SD-TRAN (R2)**



**Figure 7-8 : RES Format on SD-TRAN (Other than R2)**

#### 7.2.1.4 RES (NACK = 1)

Unlike the Legacy SD protocol, Device shall respond RES with NACK = 1 if it receives illegal CMD. Figure 7-9 illustrates the RES with NACK = 1 on SD-TRAN.

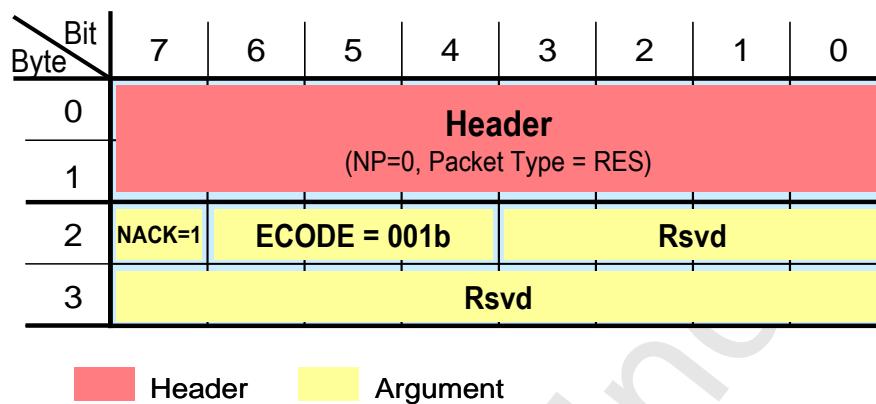
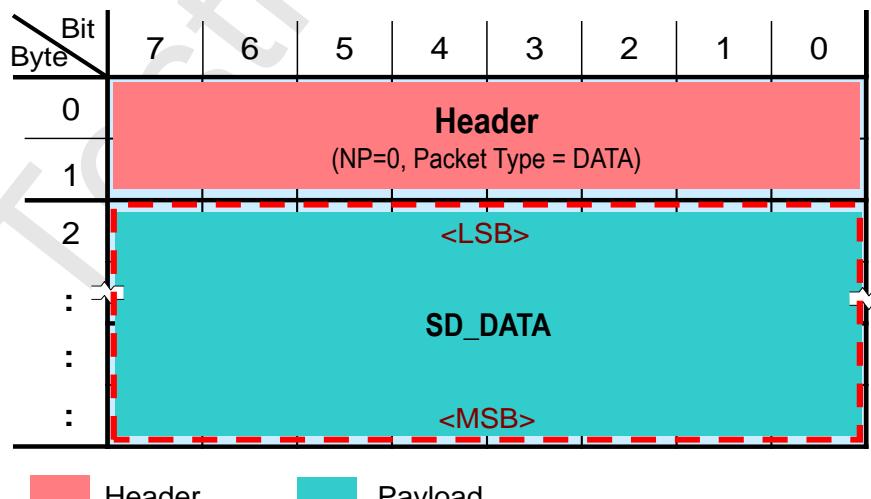


Figure 7-9 : RES (NACK = 1) Format on SD-TRAN

- **NACK (Negative Acknowledgement):** indicator whether the corresponding CMD is accepted or not.
  - NACK = 1 means the corresponding CMD is rejected.
  - In the case of NACK = 1 (CMD is rejected), Device shall not execute the requested operation (an error has occurred in the corresponding CMD).
- **ECODE[2:0] (Error Code):** Error code to represent error descriptions. It shall be set to 001b in SD-TRAN.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

#### 7.2.1.5 DATA

Figure 7-10 illustrates DATA on SD-TRAN.



Encapsulated data payload on SD /wo CRC16

Figure 7-10 : DATA Format on SD-TRAN

- **SD\_DATA:** Data included with DATA
  - The length of Payload field depends on CMD\_INDEX. Refer to Section 7.2.2 for more details.
  - It is transmitted in LSB first, MSB last.

### 7.2.1.6 Application Commands

In SD-TRAN, application commands such as ACMD41 shall be realized in one command by setting APP field to 1b in CCMD or DCMD (refer to Section 7.2.1.1 and Section 7.2.1.2). Device ignores CMD55 on SD-TRAN. Moreover, unlike Legacy SD, undefined ACMD such as ACMD42 or ACMD55 is also handled as illegal command on SD-TRAN.

### 7.2.1.7 Note for Legacy SD Commands

Packet Type for each Legacy SD command in order to generate encapsulated UHS-II command packets is defined as follows. The legacy command whose type is 'adtc' is assigned to DCMD, and otherwise is assigned to CCMD. If Packet Type is not proper in encapsulated SD command, Device shall return RES with NACK = 1. At the end of the transaction by CCMDs whose response are R1b or all DCMDs, MSG (EBSY), which is defined in Section 7.2.6.3, is transmitted. Note that Device does not send EBSY packet for the corresponding command if responding RES with NACK = 1.

These rules mentioned above are applied to all SD commands not only defined in Part 1 but also defined in other Part of SD specifications such as Part 3. Note that DCMDs corresponding to security commands defined in the Part 3 or Part A4 (DPS) shall be set LM to 0 and shall not have TLEN field.

The followings are additional rules for using Legacy SD command on UHS-II interface.

CMD	Description
CMD0	The corresponding RES has no payload (refer to Section 7.2.6.2).
CMD7	R1 returns when selected, RES without payload (refer to Section 7.2.6.2) returns when deselected.
CMD18, CMD25	Value of LM in TMODE is selectable by Host.
CMD23	If Host would like to specify the data transmission length when issuing CMD18 or CMD25, it shall set LM = 1 and assign the length to TLEN field on CMD packet.

Table 7-1 : Additional Rules of Legacy SD Commands in UHS-II

## 7.2.2 DATA Burst Framing Rules in SD-TRAN

### 7.2.2.1 Multi-block Read / Write Command

DATA Bursts accompanied by multi-block Read / Write command such as CMD18 or CMD25 shall follow the DATA Burst framing rule in Block Mode described in Section 5.2.6.2.1. Note that Block Length shall be 512 bytes in case of SD-memory, and the fractional DATA Burst is not permitted when LM = 0 except when the data transfer length for multi-block Read / Write command is determined by another means. For example, as data transfer length for ACMD18 or ACMD25 is determined by ACMD45 previously, fractional DATA Burst is permitted for ACMD18 or ACMD25 even their LM is equal to 0. In addition, fractional DATA Burst is also permitted for ACMD43 because its argument includes 'Unit\_Count' (the number of blocks to read),

### 7.2.2.2 CMD42

DATA Burst accompanied by CMD42 shall follow the DATA Burst framing rule in Byte Mode in Section 5.2.6.2.2. The payload length of DATA is equal to the block length set by CMD16 (regulated in Legacy

SD specification). Moreover, if block length set by CMD16 is odd, Host shall insert one PAD (K23.7) at the end of DATA Packet in order to make the length of Framed DATA Packet even bytes, as shown in Figure 5-10.

### 7.2.2.3 Other DCMD on SD-TRAN

For other DCMD, DATA Bursts shall follow the DATA Burst framing rule in Byte Mode described in Section 5.2.6.2.2. The payload length of DATA depends on the Legacy SD specification. For example, payload length associated to CMD6 is 64 bytes.

## 7.2.3 Interface Selection for UHS-II Card and Initialization

### 7.2.3.1 Overview

As Hosts and Devices supporting UHS-II interface shall also support SD Legacy interface, Host supporting UHS-II (simply described as "Host") interface may select either UHS-II interface or Legacy SD interface after power up. Only in Section 7.2.3, "CMD" denotes the command described in SD Physical Specification Version 4.00, and SD command on UHS-II is described as "encapsulated CMD".

### 7.2.3.2 Interface Selection after Power Up

Figure 7-11 shows a concept diagram of initialization flow after power up.

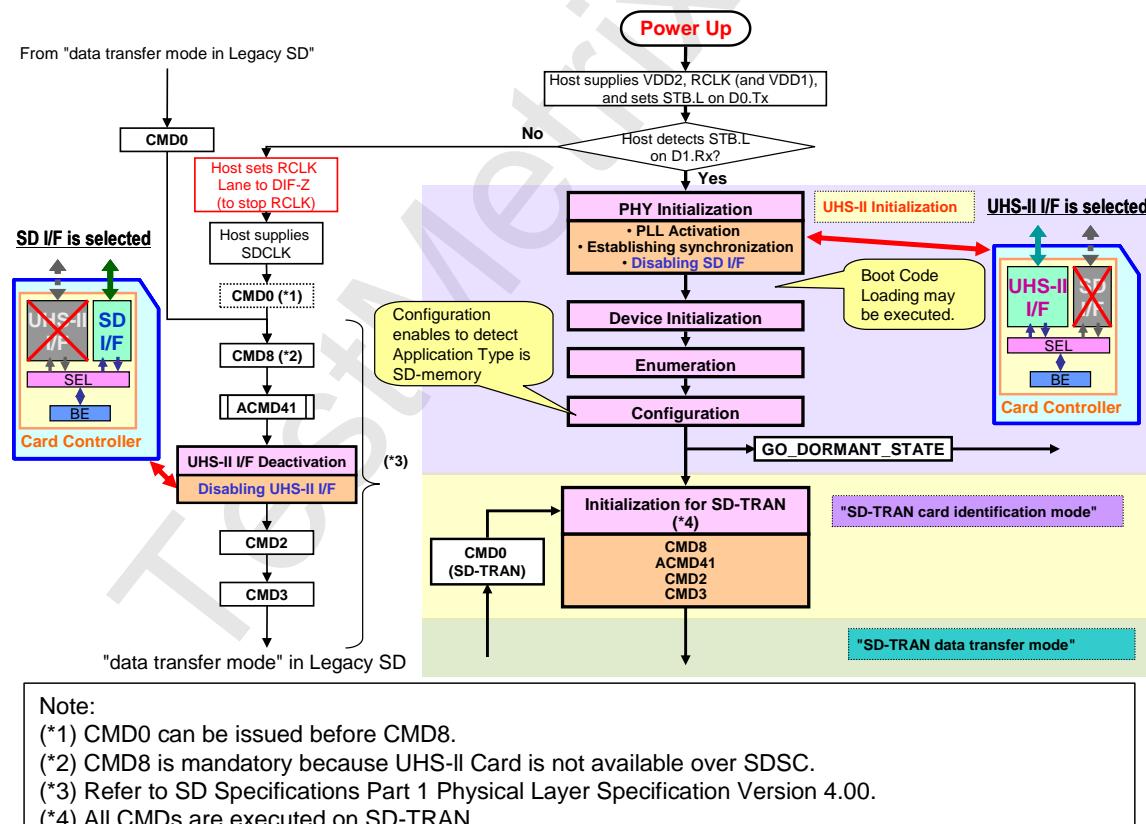


Figure 7-11 : Initialization Flow after Power Up

If Host intends to use UHS-II interface, it supplies VDD2, RCLK and VDD1 after power up, and sets STB.L on D0.Tx. As described in Section 5.3, Device connects termination resistors of RCLK Lanes after power up. Device starts PHY Initialization when receiving STB.L and responds STB.L if it

succeeds.

The method for Host to distinguish whether Device fails to start PHY initialization is through detecting timeout from Host's setting STB.L on D0.Tx to receiving it on D1.Rx, which can be estimated from Teidl\_stb and UHS-II bus topology.

If Host detects timeout, Host sets RCLK Lane to DIF-Z to stop supplying RCLK, and then Host supplies SDCLK and issues CMD8 and ACMD41 for Legacy SD protocol to initialize SD interface. Then, Host proceeds card identification and the card status transits to "data transfer mode" in Legacy SD (same as data transfer mode defined in SD Specifications Part 1 Physical Layer Specification Version 4.00) as a result. When Legacy SD interface is selected, UHS-II interface that is activated by power up is disabled before ACMD41 is completed. Moreover, termination resistors of RCLK Lanes in Device are disconnected when disabling UHS-II interface. As the sequence to "data transfer mode" in Legacy SD in Figure 7-11 is simplified, refer to SD Specifications Part 1 Physical Layer Specification Version 4.00 for detailed specifications of Legacy SD initialization. Note that if CMD0 is issued in Legacy SD card state transits to 'idle'. (Note that it is impossible to execute (UHS-II) PHY Initialization.)

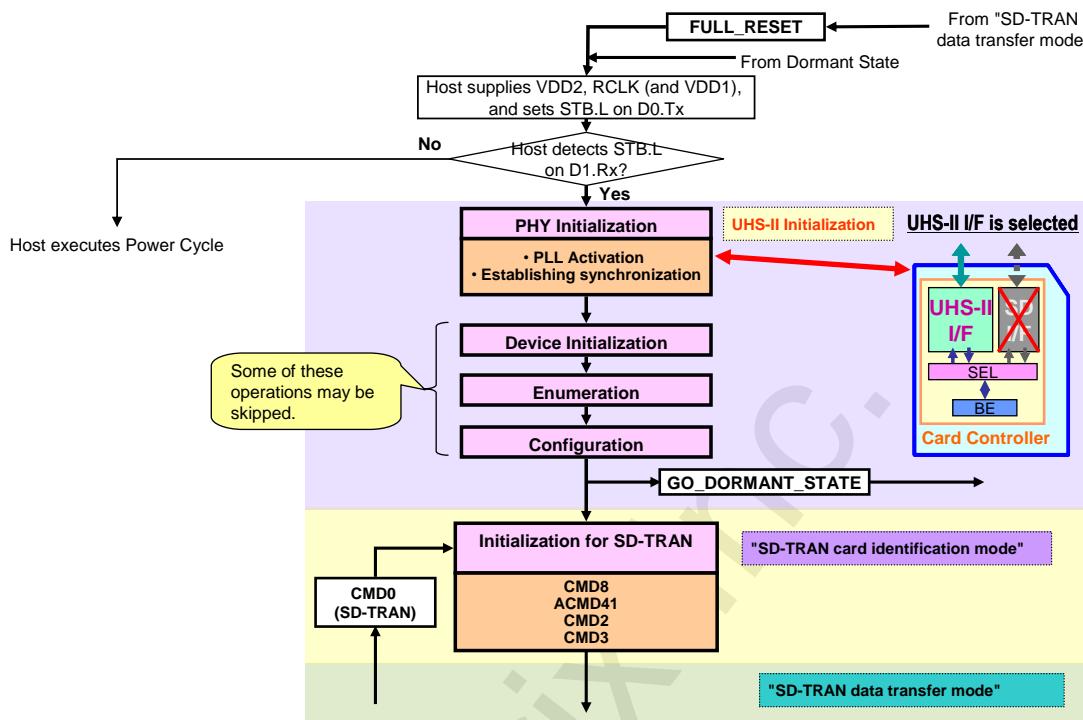
On the other hand, if Device succeeds PHY Initialization, UHS-II interface is available and then, Device Initialization, Enumeration and Configuration take place in this order. If Host detects "Application Type" is "SD memory" or "SDIO" during Configuration, it can issue the encapsulated SD CMD. Host shall execute card identification described in Section 7.2.4.1 by encapsulated SD CMDs in case of detecting "SD memory". If encapsulated CMD0 is issued, card state transits to 'idle' in SD-TRAN. On the other hand, if FULL\_RESET CCMD is issued, Device waits STB.L for PHY Initialization.

If Host intends to use only Legacy SD interface or detects that Legacy SD Card is inserted, it is allowed to supply only VDD1 and SDCLK, and issue CMD8 in order to accelerate initialization of Legacy SD interface. Note that once UHS-II I/F is disabled, Host requires power cycle to enable UHS-II again. Refer to Section 3.10.4 in SD Specification Part 1 Version 4.00 for more details about VDD2 supply.

Note that Device's power consumption during Device Initialization is not regulated by Power Limit specified by CMD6, but parameters specified by DEVICE\_INIT CCMD.

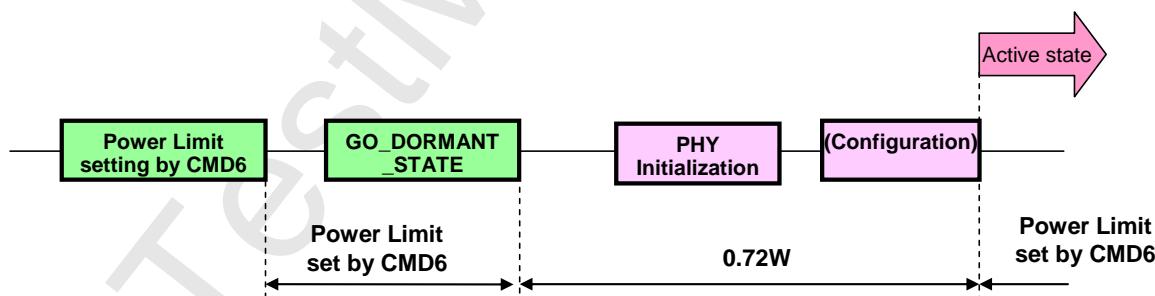
### 7.2.3.3 Interface Selection after FULL\_RESET or GO\_DORMANT\_STATE

Figure 7-12 shows a concept diagram of initialization flow after executing FULL\_RESET or GO\_DORMANT\_STATE CCMD.



**Figure 7-12 : Initialization Flow after FULL\_RESET or GO\_DORMANT\_STATE**

Host shall not select Legacy SD interface after issuing these CMDs. Then if Host detects that Device fails to start PHY Initialization, Host requires power cycle to recover this illegal situation. Setting of Power Limit specified by CMD6 is kept after recovering from Dormant State. After exiting Dormant State and until going into Active state, power consumption of Device is up to 0.72W. Setting of Power Limit which has been specified by CMD6 is effective in Active state again.



**Figure 7-13 : Power Consumption after Exiting from Dormant State**

#### 7.2.4 Transaction Control and Management State Machine

From this section, an "encapsulated CMD" is described as just a "CMD" for simplicity (e.g. "encapsulated CMD0" is described as "CMD0"). In this section, state diagrams in card identification mode and data transfer mode for SD-TRAN are shown. They are based on those in Legacy SD, but some differences exist as described below.

##### 7.2.4.1 Card Identification Mode

Figure 7-14 shows a state diagram for card identification mode on SD-TRAN.

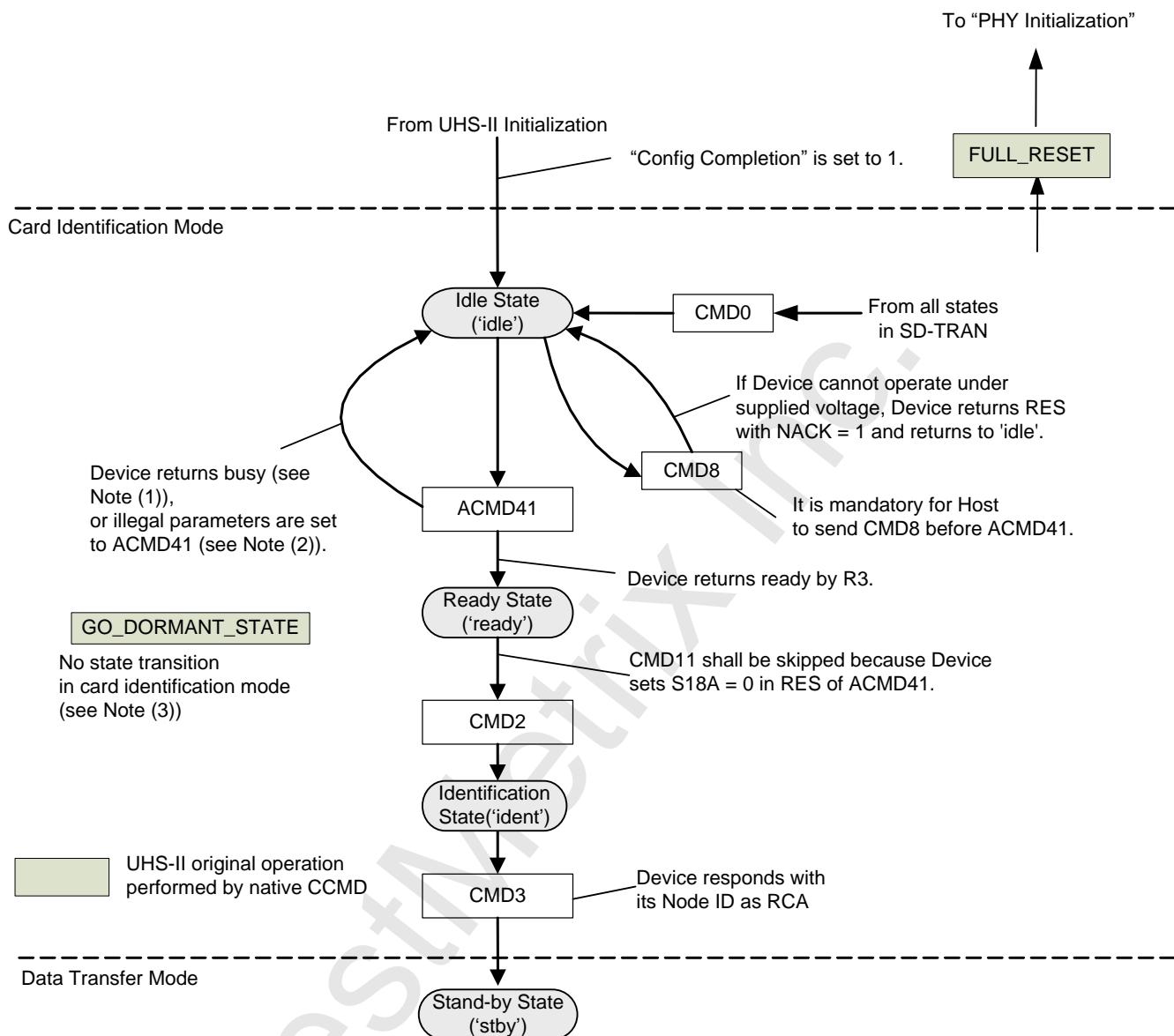


Figure 7-14 : State Diagram on SD-TRAN (Card Identification Mode)

Differences from the Legacy SD are as follows.

- Like Legacy SD, Host shall issue CMD8 and then ACMD41 in order to transit from 'idle' to 'ready'.
- If Device receives CMD with illegal parameters, Device shall return RES with NACK = 1 on SD-TRAN.
  - RES with NACK = 1 is transmitted in illegal CMD8.

- Device never returns ready in illegal ACMD41, and the state transits to 'idle' state.
- CMD11 shall be skipped. Related to this Device shall set '0' to S18A field in RES of ACMD41.
- If Device receives CMD3, Device responds with its own Node ID as new RCA. As each Device's Node ID is guaranteed to be distinctive even in case of multiple-Device connection, Host does not need to reissue CMD3 for avoiding RCA duplication.
- The 'ina' state and its related transition are removed from SD-TRAN.

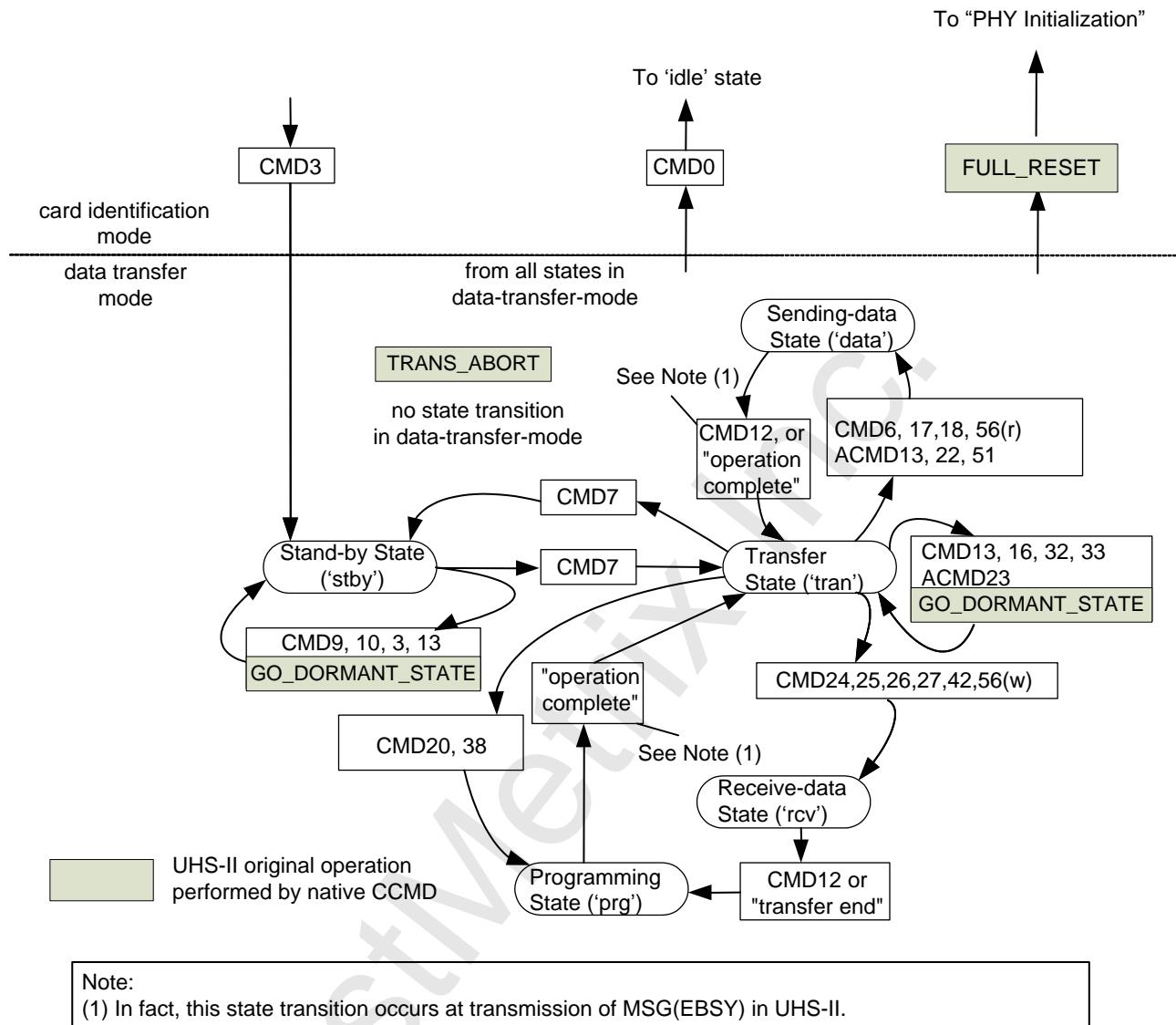
During card identification mode, Device operation when receiving native CMD is same as that in Active state. Host cannot issue arbitrary DCMD during this mode. Note that card status is kept when receiving GO\_DORMANT\_STATE CCMD. So Device directly transits to the appropriate card status after UHS-II Initialization in case of recovery from Dormant state. For example, if card status was 'ready' before transitioning to Dormant state, it is still 'ready' after recovering from Dormant state. This rule is same as for 'idle' and 'ident' (and also same as 'stby' and 'tran' in Data Transfer Mode).

#### 7.2.4.2 Data Transfer Mode

Figure 7-15 shows a state diagram for data transfer mode of SD-TRAN. Differences from the Legacy SD are as follows.

- Common CMDs with Legacy SD shall be executed through SD-TRAN.
- The 'dis' state and its related transitions are abandoned for simplicity. And transition from 'data' state to 'stby' state is also removed.
- Transitions by CMD7 are defined as follows.
  - Transits to 'tran' if RCA in CMD7 is equal to Device's Node ID.
  - Transits to 'stby' if RCA in CMD7 is not equal to Device's Node ID.
- RCA in the argument shall be ignored other than CMD7.
- If Device receives illegal command in 'stby' state, Device shall return RES with NACK = 1.
- CMD13 can be issued only in 'stby' or 'tran' state. In other words, CMD13 cannot be issued during CTS in case of SD memory.
- When Device receives CMD3 in 'ident' state or 'stby' state, Device shall always return its Device ID as RCA.

For read transaction, state transits from 'data' to 'tran' at transmission of MSG (EBSY). For write transaction, state transits from 'rcv' to 'prg' when Device receives all DATA packets specified by TLEN on write DCMD, or it transmits RES (R1b) of CMD12 corresponding to write DCMD. In addition, state transits from 'prg' to 'tran' at transmission of MSG (EBSY).



**Figure 7-15 : State Diagram on SD-TRAN (Data Transfer Mode)**

In addition, there are following restrictions for Host to issue native CMDs related to data transfer mode in SD-TRAN. If Host violates the rules about native CMDs mentioned below, Device behavior is undefined.

- DEVICE\_INIT, ENUMERATE and arbitrary native DCMD cannot be issued in data transfer mode.
- FULL\_RESET and TRANS\_ABORT can be issued all state in data transfer mode, but they can be issued only in CTS during data transmission. Also refer to Section 5.2.3 and 6.2.5 for issuing FULL\_RESET,
- Native Read or native Write CCMD other than defined in Table 6-19 can be issued only in 'stby' or 'tran' state. Device shall also accept native Read CCMD in 'data' or 'rcv' if it responds properly to the preceding TRANS\_ABORT.
- GO\_DORMANT\_STATE are valid in both 'stby' and 'tran' state.
- TRANS\_ABORT can be issued only when timeout occurs. Moreover, not TRANS\_ABORT but encapsulated CMD12 shall be used in case of terminating data transmission.
- FULL\_RESET will terminate any pending or active programming operation in SD-TRAN. This may

destroy the data contents on the Device. It is the Host's responsibility to prevent this.

#### 7.2.4.3 Relation to State Machines in CM-TRAN and LINK

CMD or RES transmission in SD-TRAN shall be reflected all state machines defined in CM-TRAN and LINK. In this case, CMD12 is taken as TRANS\_ABORT CCMD in CM-TRAN and LINK.

For instance, when CMD18 is issued, TPSM shall transit from TP\_IDLE to TP\_WAIT. Likewise in case of read transaction, if Device receives CMD12 during the time period from transmitting FCREQ to receiving FCRDY, TPSM shall transit from TP\_C\_WAIT to TP\_IDLE and DLSM shall transit from Active.Trans.WaitRDY to Active.Control at the transmission of RES of CMD12.

Also in case of read transaction, if Device receives CMD0 during the time period from transmitting FCREQ to receiving FCRDY, TPSM shall transit from TP\_C\_WAIT to TP\_IDLE and DLSM shall transit from Active.Trans.WaitRDY to Active.Control at the transmission of RES of CMD0.

#### 7.2.4.4 Card State Transition by UHS-II Native Command

Table 7-2 shows card state transition by UHS-II native commands. Mark "\*" indicates that Device behavior is undefined for the command.

	current state (SD-TRAN)							
	idle	ready	ident	stby	tran	data	rcv	prg
UHS-II Native CMD								
FULL_RESET	idle	idle	idle	idle	idle	idle (See Note (2))	idle (See Note (2))	idle
GO_DORMANT_STATE	idle	ready	ident	stby	tran	*	*	*
DEVICE_INIT (See Note (1))	idle	*	*	*	*	*	*	*
ENUMERATE (See Note (1))	idle	*	*	*	*	*	*	*
TRANS_ABORT	idle	ready	ident	stby	tran	data (See Note (2))	rcv (See Note (2))	prg
Other Native Write CCMD	idle	ready	ident	stby	tran	*	*	*
Native Read CCMD	idle	ready	ident	stby	tran	data (See Note (3))	rcv (See Note (3))	*
Native DCMD	*	*	*	*	*	*	*	*

Note:

- (1) These commands can be issued in any card states in SD-TRAN if Host sets "Config Completion" flag to 0 before transitioning to Dormant. However, it is strongly recommended that Host should not issue this command after recovering from Dormant.
- (2) Host can issue only during CTS period for this state
- (3) This transition is available if Device responds properly to the preceding TRANS\_ABORT.

**Table 7-2 : Card State Transition by UHS-II Native Command**

## 7.2.5 Basic Transaction Rules

Needless to say, transaction rules in CM-TRAN shall be kept also in SD-TRAN. In this section, some examples of basic transaction rules are shown in SD-TRAN. Note that NP in Header field of TLP is 0 on SD-TRAN.

### 7.2.5.1 CCMD

Figure 7-16 illustrates a sequence for CCMD in SD-TRAN. In this section, CMD9 (SEND\_CSD) is used as an example. Refer to Table 7-1 for other adaptable commands in SD-TRAN.

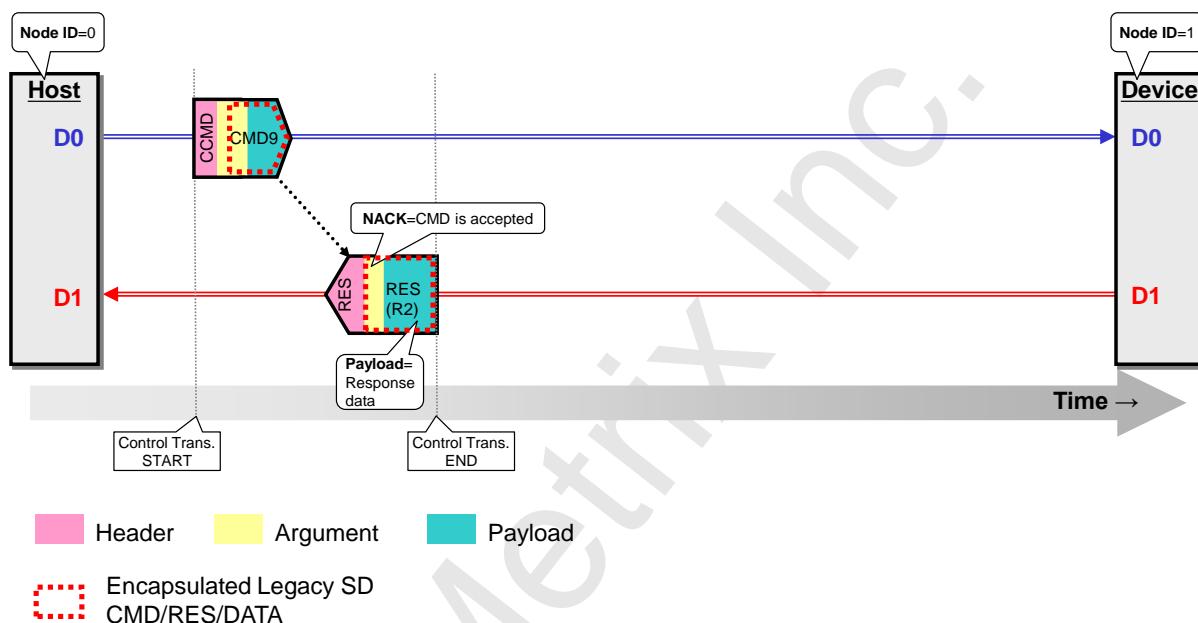


Figure 7-16 : Sequence of CCMD on SD-TRAN (CMD9)

The detailed field values in Figure 7-16 are as follows;

#### [CCMD]

- **Header (CCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = CCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (CCMD):**
  - APP = 0 (regular command)
  - CMD\_INDEX = 9 (command index in Legacy SD)
- **Payload (CCMD):**
  - SD\_ARG = Argument of CMD9.

#### [RES]

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding CCMD)
  - SID = 1 (Node ID of Device)

- TID = the same value as TID of the corresponding CCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from CCMD
- **Payload (RES):**
  - CONTENT = Content of CSD Register (the length of Payload is 16 in this case)

### 7.2.5.2 Read DCMD (Fixed Transfer Length)

In the examples shown below, N\_FCU is supposed to set to 2.

Figure 7-17 illustrates a sequence for Read DCMD (fixed transfer length) in SD-TRAN. In this case only CMD18 (READ\_MULTIPLE\_BLOCK) is available in SD-TRAN.

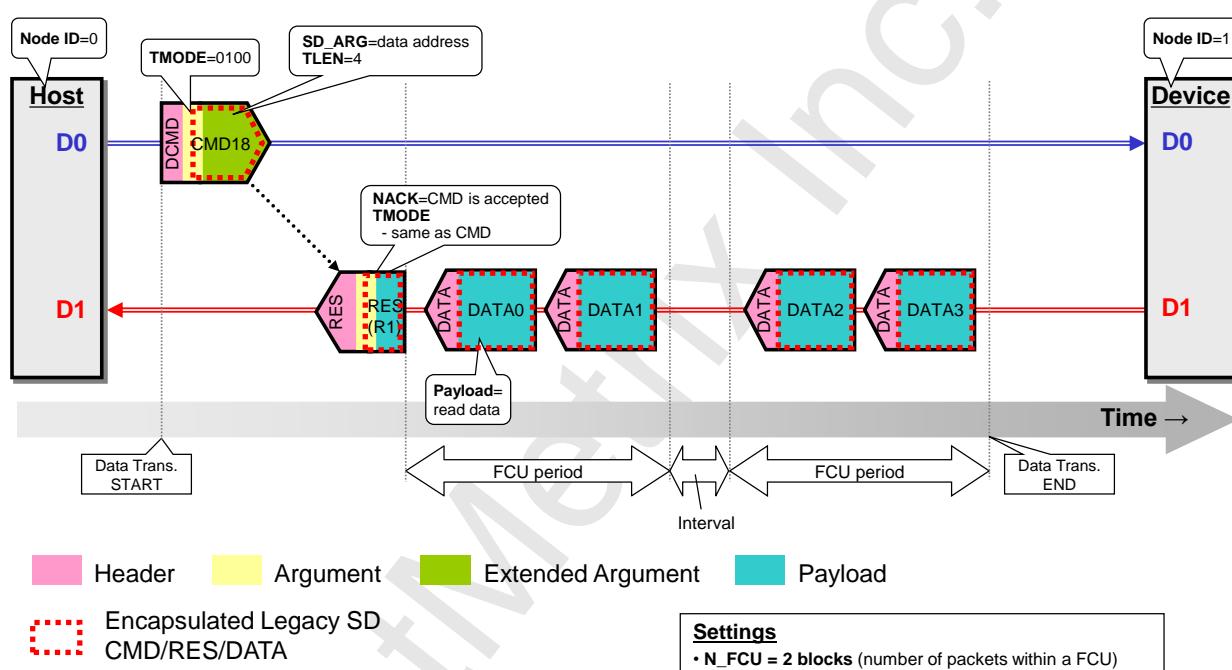


Figure 7-17 : Sequence of Read DCMD on SD-TRAN (CMD18, LM = 1)

The detailed field values in Figure 7-17 are as follows;

#### [DCMD]

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**
  - TMODE = 0100b (LM = 1, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 18 (command index in Legacy SD)
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD18.
  - TLEN = 4 blocks (total length of data transferred during a data transaction)

**[RES]****• Header (RES):**

- NP = 0 (not native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding DCMD)
- SID = 1 (Node ID of Device)
- TID = the same value as TID of the corresponding DCMD

**• Argument (RES):**

- NACK = 0 (the corresponding CMD is accepted)
- Other field is copied from DCMD

**• Payload (RES):**

- CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]****• Header (DATA):**

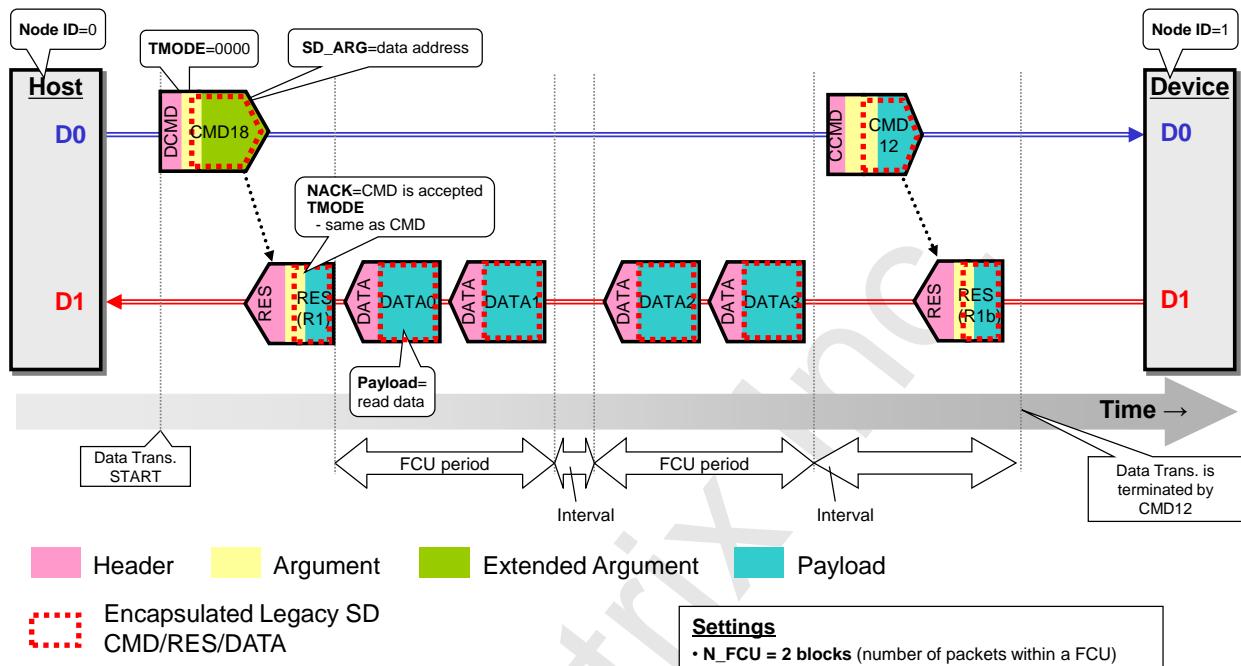
- NP = 0 (not native protocol)
- Packet Type = DATA
- DID = 0 (Node ID of Host)
- SID = 1 (Node ID of source Device)
- TID = the same value as TID of the corresponding DCMD

**• Payload (DATA):** Requested read data by Host

In this case, Host is not required to issue CMD12 to terminate the data transmission.

### 7.2.5.3 Read DCMD (Infinite Transfer Length)

Figure 7-18 illustrates a sequence for Read DCMD (infinite transfer length) in SD-TRAN. In this section, CMD18 is used as an example. Refer to Table 7-1 for other adaptable commands in SD-TRAN.



**Figure 7-18 : Sequence of Read DCMD on SD-TRAN (CMD18, LM = 0)**

The detailed field values in Figure 7-18 are as follows;

#### [DCMD]

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**
  - TMODE = 0000b (LM = 0, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 18 (command index in Legacy SD)
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD18.

#### [RES]

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)

- Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

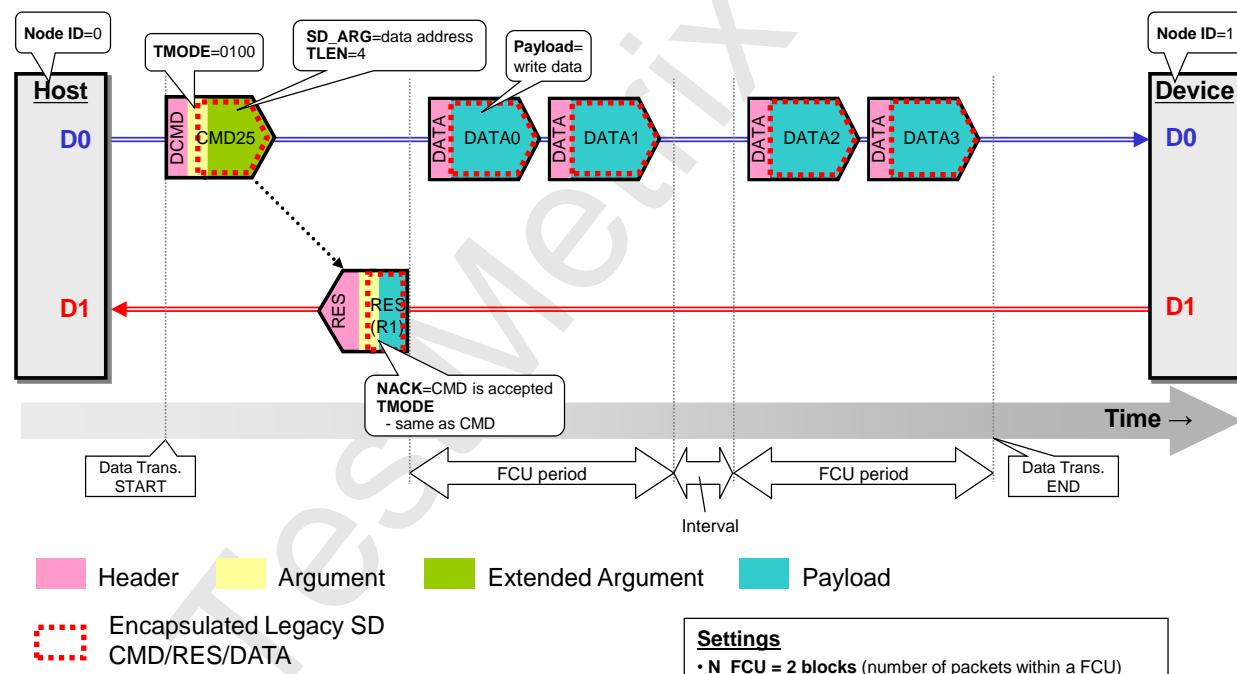
**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 0 (Node ID of Host)
  - SID = 1 (Node ID of source Device)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** Requested read data by Host

CMD12 can be issued only during interval period in order to terminate data transaction.

#### 7.2.5.4 Write DCMD (Fixed Transfer Length)

Figure 7-19 illustrates a sequence for Write DCMD (fixed transfer length) in SD-TRAN. In this case only CMD25 (WRITE\_MULTIPLE\_BLOCK) is available in SD-TRAN.



**Figure 7-19 : Sequence of Write DCMD on SD-TRAN (CMD25, LM = 1)**

The detailed field values in Figure 7-19 are as follows;

**[DCMD]**

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**

- TMODE = 0100b (LM = 1, DM = 0)
- APP = 0 (regular command)
- CMD\_INDEX = 25 (command index in Legacy SD)
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD25.
  - TLEN = 4 blocks (total length of data transferred during a data transaction)

**[RES]**

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = The same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** Transferred write data to Device

In this case, Host is not required to issue CMD12 to terminate the data transmission.

### 7.2.5.5 Write DCMD (Infinite Transfer Length)

Figure 7-20 illustrates a sequence for Write DCMD (infinite transfer length) in SD-TRAN. In this section, CMD25 is used as an example. Refer to Table 7-1 for other adaptable commands in SD-TRAN.

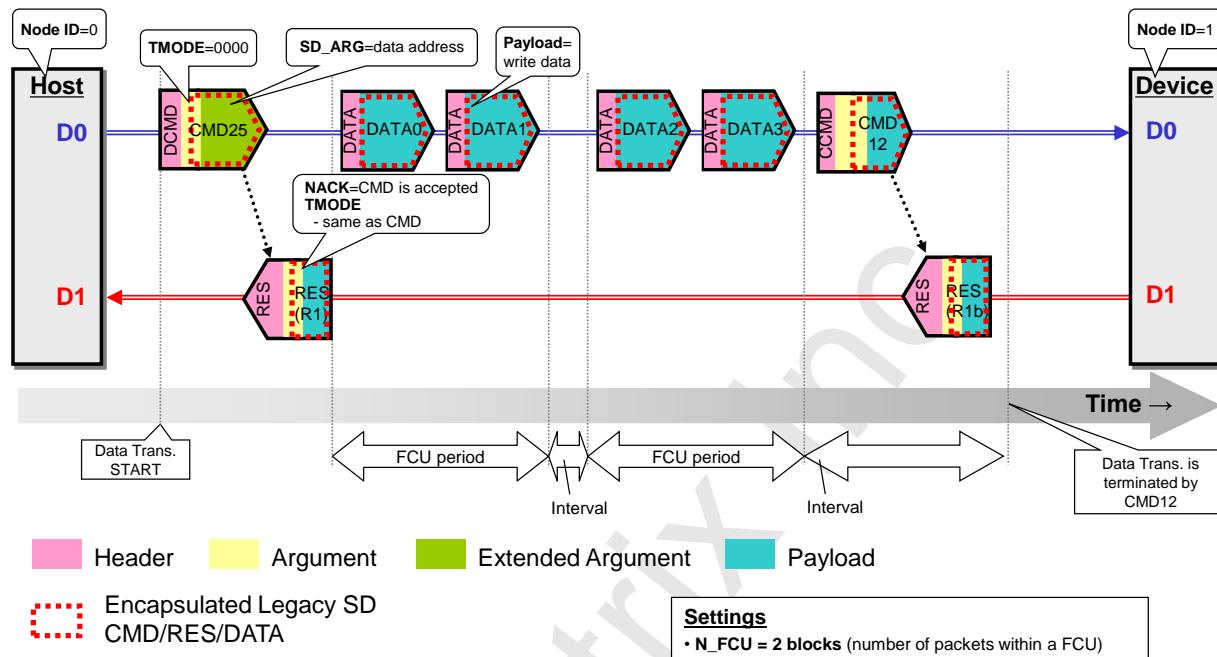


Figure 7-20 : Sequence of Write DCMD on SD-TRAN (CMD25, LM = 0)

The detailed field values in Figure 7-20 are as follows;

#### [DCMD]

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**
  - TMODE = 0000b (LM = 0, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 25 (command index in Legacy SD)
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD25.

#### [RES]

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = The same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)

- Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

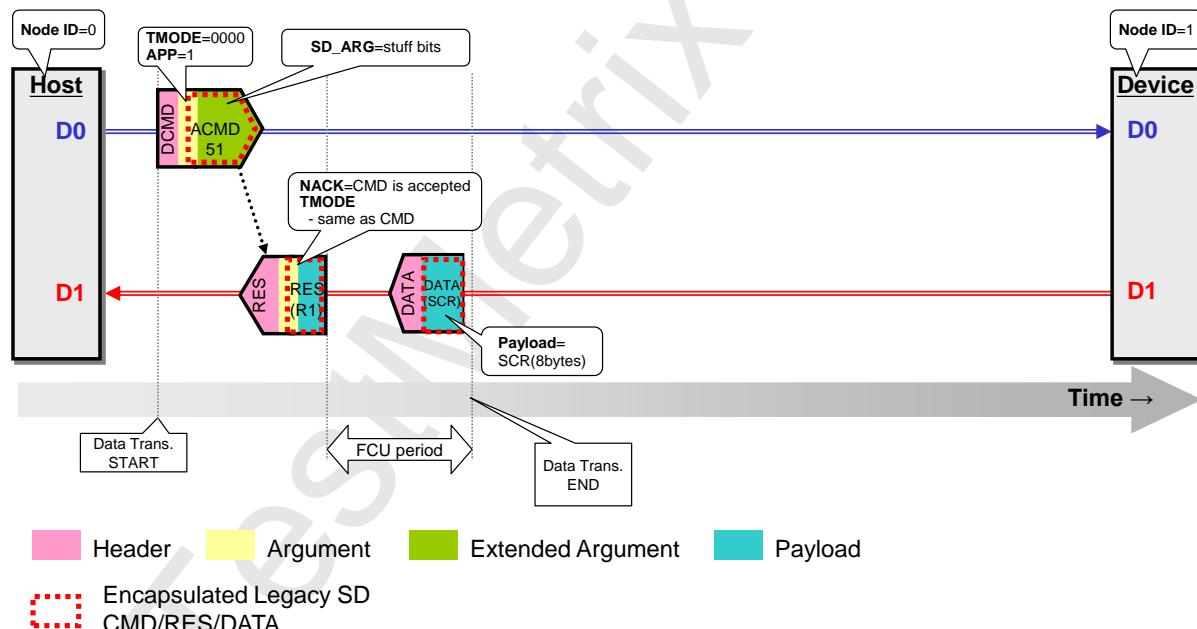
**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** Transferred write data to Device

CMD12 can be issued only during interval period in order to terminate this transaction.

**7.2.5.6 Other DCMD**

Figure 7-21 illustrates a sequence for DCMD whose data size is specified by CMD\_INDEX. In this section, ACMD51 is used as an example.



**Figure 7-21 : Sequence of ACMD51 on SD-TRAN**

The detailed field values in Figure 7-21 are as follows;

**[DCMD]**

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**
  - TMODE = 0000b (LM = 0, DM = 0)

- APP = 1 (application command)
- CMD\_INDEX = 51 (command index in Legacy SD. Note that ACMD51 is realized by CMD\_INDEX = 51 with APP = 1).
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of ACMD51 (stuff bits).

**[RES]**

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = The same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** Transferred SCR data to Host. Note that the length of Payload field of DATA is 8 bytes.

**7.2.6 SD-TRAN Specific Transaction Rules**

In this section, some examples of SD-TRAN specific transaction rules are shown.

**7.2.6.1 Definition of Application Specific MSG**

Table 7-3 illustrates detailed definitions of application specific MSG for SD-TRAN.

CTG		IDX		CODE	Description
Bits	Name	Bits	Name		
100b	AMSG	0000b	EBSY	Refer to Table 7-4	End of Busy Period for memory access
		others	Reserved	Reserved	Reserved

**Table 7-3 : Detailed Definition of SD-TRAN Specific MSG**

Data transmission on SD-TRAN is based on that on CM-TRAN, so other MSGs such as MSG (FCREQ) are also used. Refer to Section 5.2.4 for details of other MSG definition.

Table 7-4 describes the CODE definition of EBSY.

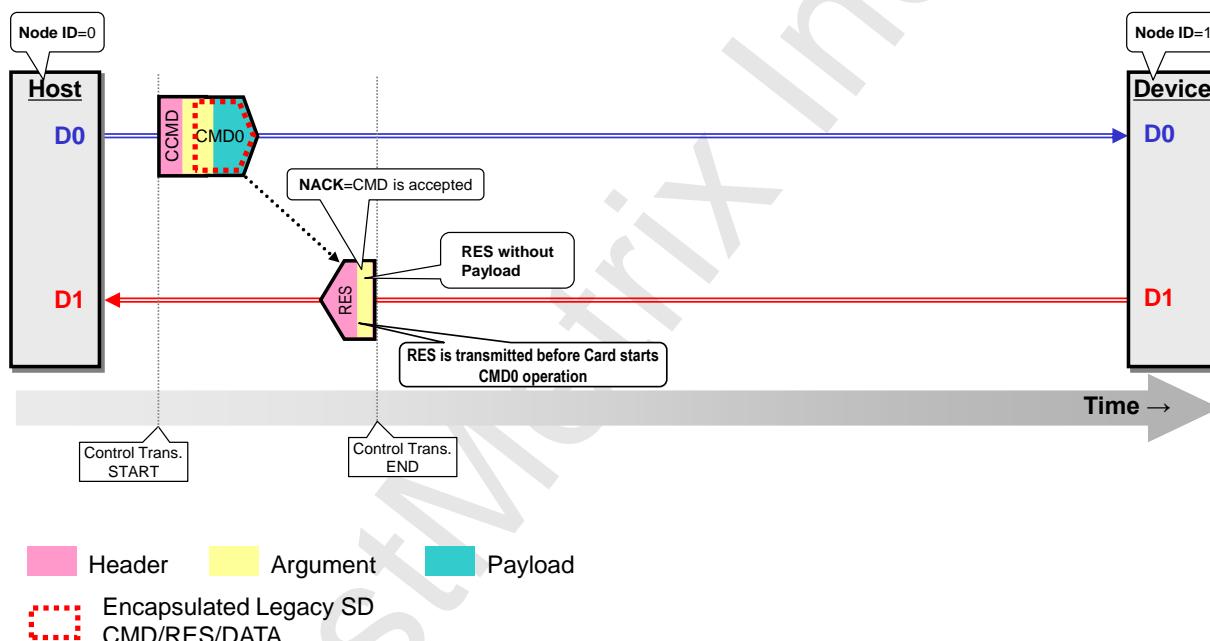
Bits	Identifier	Value	Description
7	MEMORY_ERROR	'0' = no error '1' = error	Memory error occurs during BUSY period.
6:0	Reserved	Reserved	Reserved

**Table 7-4 : Code Definition of EBSY**

- **MEMORY\_ERROR:** Indicates that memory error occurs during BUSY period.

### 7.2.6.2 CMD0

Figure 7-22 illustrates a sequence for CMD0 (GO\_IDLE\_STATE). CMD0 in Legacy SD protocol originally has no response. In UHS-II protocol, however, Device shall transmit RES without payload to Host before CMD0 operation. This rule is also applied in case of CMD7 (SELECT/DESELECT\_CARD) for deselect.

**Figure 7-22 : Sequence of CMD0 on SD-TRAN**

The detailed field values in Figure 7-22 are as follows;

#### [CCMD]

- **Header (CCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = CCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (CCMD):**
  - APP = 0 (regular command)
  - CMD\_INDEX = 0 (command index in Legacy SD)
- **Payload (CCMD):**
  - SD\_ARG = Argument of CMD0.

**[RES]****• Header (RES):**

- NP = 0 (not native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding CCMD)
- SID = 1 (Node ID of Device)
- TID = The same value as TID of the corresponding CCMD

**• Argument (RES):**

- NACK = 0 (the corresponding CMD is accepted)
- Other field is copied from CCMD

**• Payload (RES):**

- No payloads for RES of CMD0.

**7.2.6.3 Representing Busy Period and 'prg' State**

In SD-TRAN, Busy Period is defined as follows.

- Busy Period starts at the transmission of
  - RES (R1b)
  - RES (R1) of DCMD, or the last DATA in the DATA Burst in case of read transaction
  - MSG (STAT) in case of write transaction
- Busy Period ends at the transmission of
  - MSG (EBSY)
  - MSG (FCREQ) in case of read transaction
  - MSG (FCRDY) in case of write transaction

In addition, 'prg' state (programming state) is regulated as follows.

- From RES (R1b) to MSG (EBSY) in case of write or erase transaction.
- From MSG (STAT) for completing data reception by Device to MSG (EBSY)

Figure 7-23 illustrates a sequence for representing Busy Period and 'prg' state after R1b in SD-TRAN. In this section, CMD38 (ERASE) is used as an example.

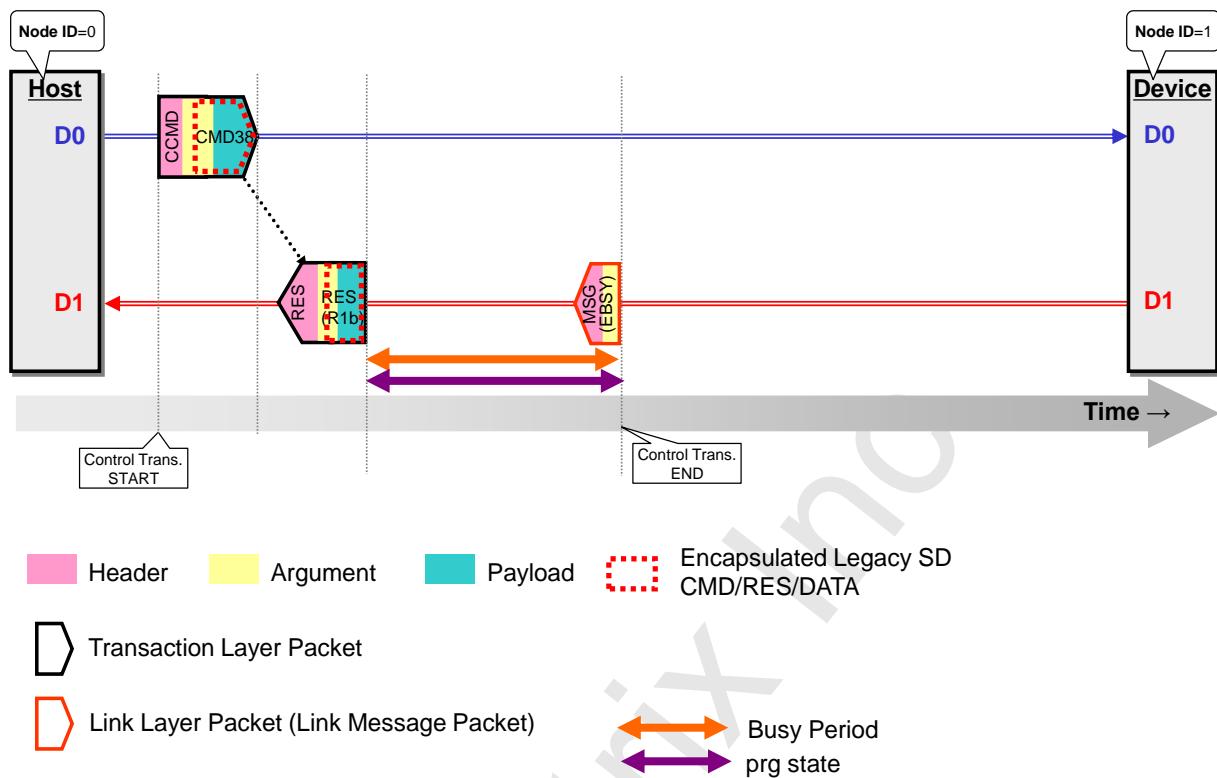


Figure 7-23 : Sequence of CMD38 on SD-TRAN

The detailed field values in Figure 7-23 are as follows;

#### [CCMD]

- **Header (CCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = CCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (CCMD):**
  - APP = 0 (regular command)
  - CMD\_INDEX = 38 (command index in Legacy SD)
- **Payload (CCMD):**
  - SD\_ARG = Argument of CMD38.

#### [RES]

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding CCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding CCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from CCMD
- **Payload (RES):**

- CONTENT = Response data of R1b (the length of Payload is 4 in this case)

As mentioned above, Busy Period in SD-TRAN starts at transmitting RES (R1b), and ends at MSG (EBSY). This example can be adapted to CMD20 in SD-TRAN. Moreover 'prg' state starts at transmitting RES (R1b), and ends at MSG (EBSY).

Figure 7-24 illustrates a sequence for representing Busy Period by Write DCMD with fixed data length. Figure 7-24 includes Link Layer Packet not only for representing Busy Period, but also for realizing flow control.

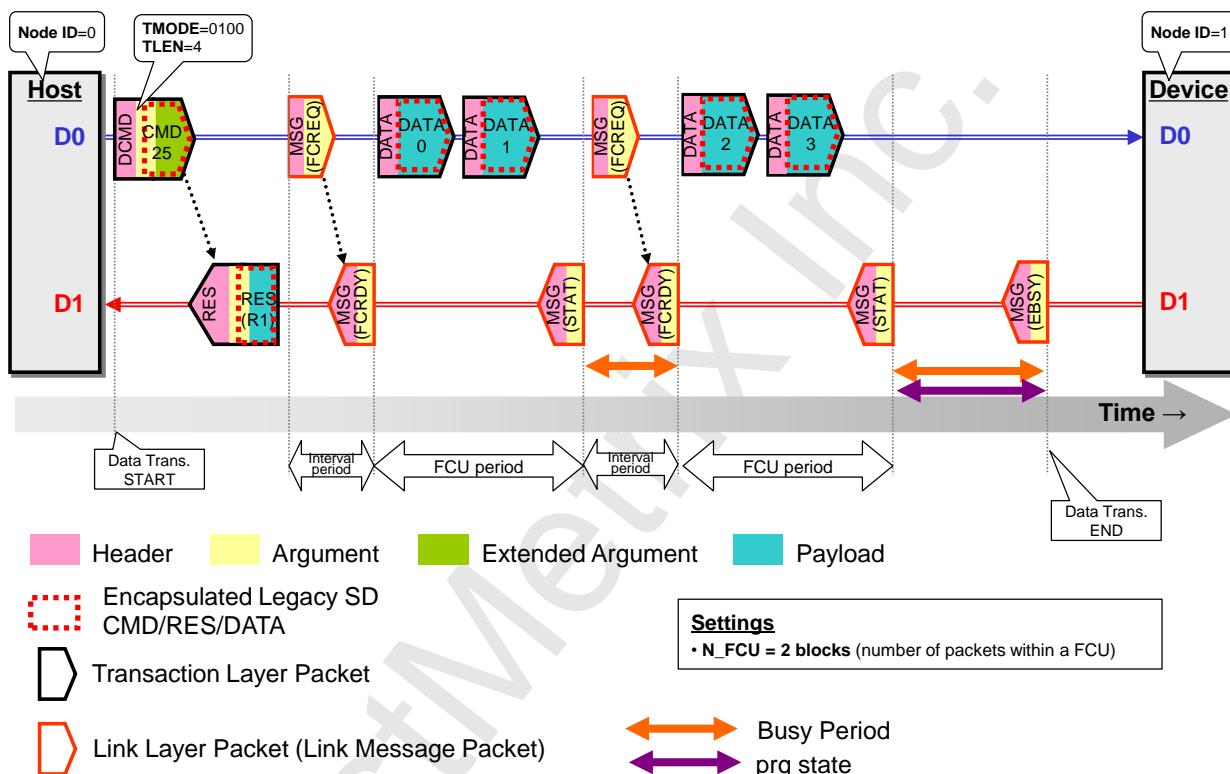


Figure 7-24 : Sequence of Write DCMD on SD-TRAN with Busy Period (Fixed Transfer Length)

The detailed field values in Figure 7-24 are as follows;

#### [DCMD]

- Header (DCMD):
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- Argument (DCMD):
  - TMODE = 0100b (LM = 1, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 25 (command index in Legacy SD)
- Extended Argument (DCMD):
  - SD\_ARG = Argument of CMD25.

- TLEN = 4 (total length of data transferred during a data transaction)

**[RES]**

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 1 (Node ID of source Device)
  - SID = 0 (Node ID of Host)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** transferred write data to Device

After Device receives DATA specified in TLEN of CMD25, it transmits MSG (STAT), and notifies Busy Period start to Host. Device transmits MSG (EBSY) at the end of Busy Period.

Figure 7-25 illustrates a sequence for representing Busy Period by Write DCMD in case of infinite transfer length.

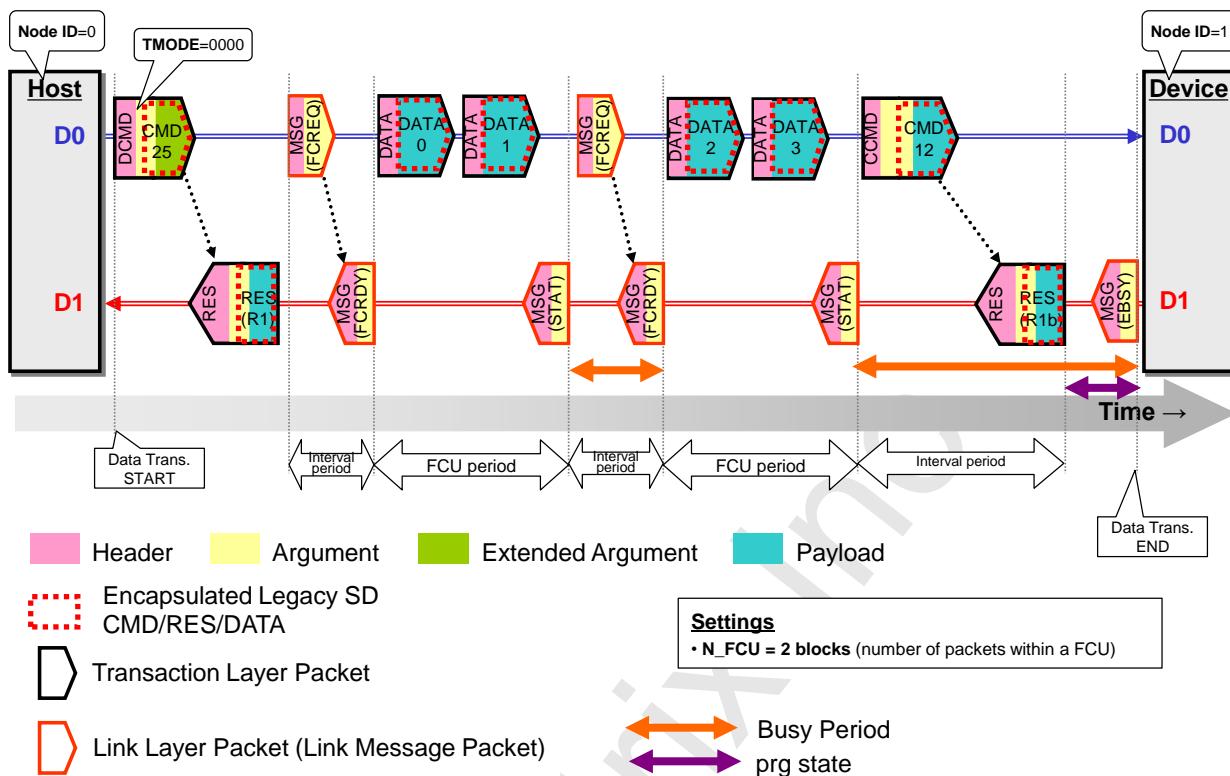


Figure 7-25 : Sequence of Write DCMD on SD-TRAN with Busy Period (Infinite Transfer Length)

The detailed field values in Figure 7-25 are as follows;

#### [DCMD]

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- **Argument (DCMD):**
  - TMODE = 0000b (LM = 0, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 25 (command index in Legacy SD)
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD25.

#### [RES]

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = The same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD

- Payload (RES):**

- CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- Header (DATA):**

- NP = 0 (not native protocol)
- Packet Type = DATA
- DID = 1 (Node ID of source Device)
- SID = 0 (Node ID of Host)
- TID = The same value as TID of the corresponding DCMD

- Payload (DATA):** transferred write data to Device

Host can issue CMD12 after receiving MSG (STAT) from Device (in other word, during Command Time Slot described in Section 5.5.2). Device sends RES (R1b), and MSG (EBSY) at the end of this transaction.

Figure 7-26 illustrates a sequence for representing Busy Period by read DCMD with fixed data length.

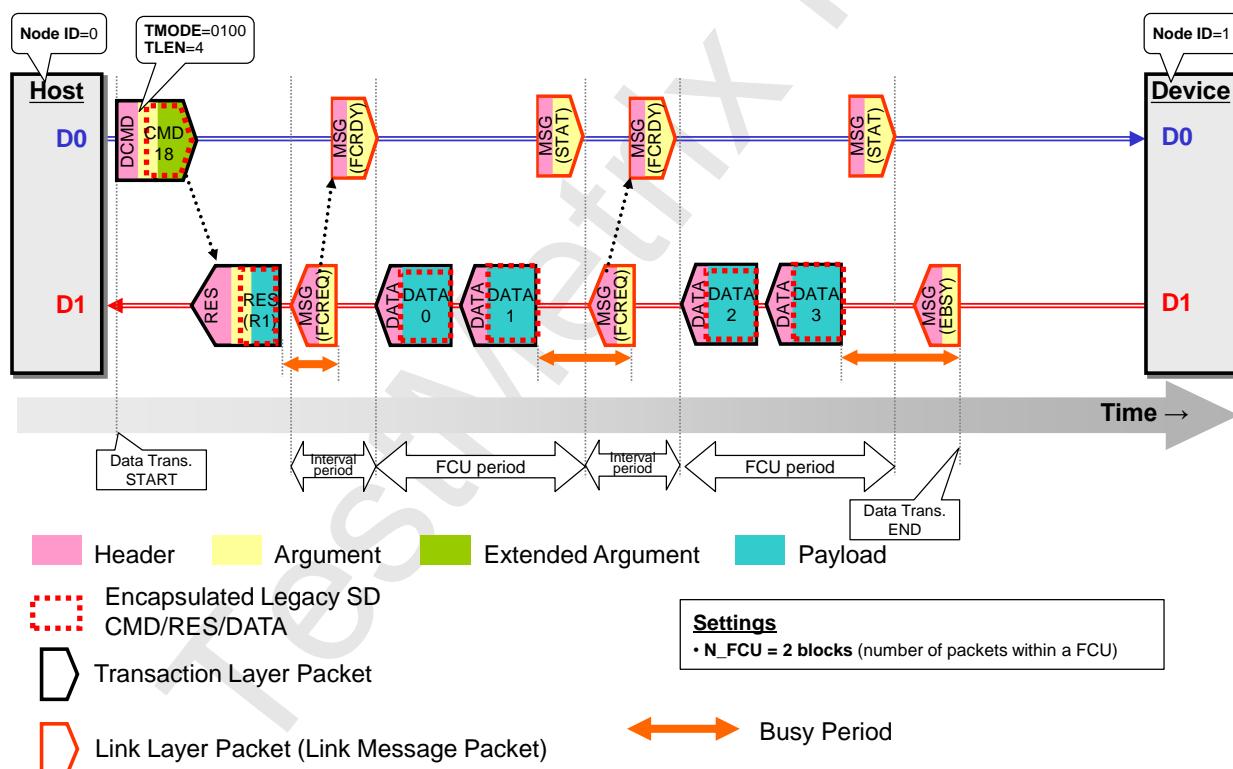


Figure 7-26 : Sequence of Read DCMD on SD-TRAN with Busy Period (Fixed Transfer Length)

The detailed field values in Figure 7-26 are as follows;

**[DCMD]**

- Header (DCMD):**

- NP = 0 (not native protocol)
- Packet Type = DCMD
- DID = 1 (Node ID of destination Device)
- SID = 0 (Node ID of Host)
- TID = Transaction ID decided by Host

- **Argument (DCMD):**
  - TMODE = 0100b (LM = 1, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 18 (command index in Legacy SD)

- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD18.
  - TLEN = 4 (total length of data transferred during a data transaction)

**[RES]**

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 0 (Node ID of Host)
  - SID = 1 (Node ID of destination Device)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** transferred write data to Device

In read transaction, after Host receives DATA specified in TLEN of CMD18, it transmits MSG (STAT). Then, Device shall transmit MSG (EBSY) when it is able to accept the next command. In other words, the data transaction terminates when Host receives MSG (EBSY). This rule is applied for all read SD commands including security commands..

Figure 7-27 illustrates a sequence for representing Busy Period by read DCMD with infinite data length.

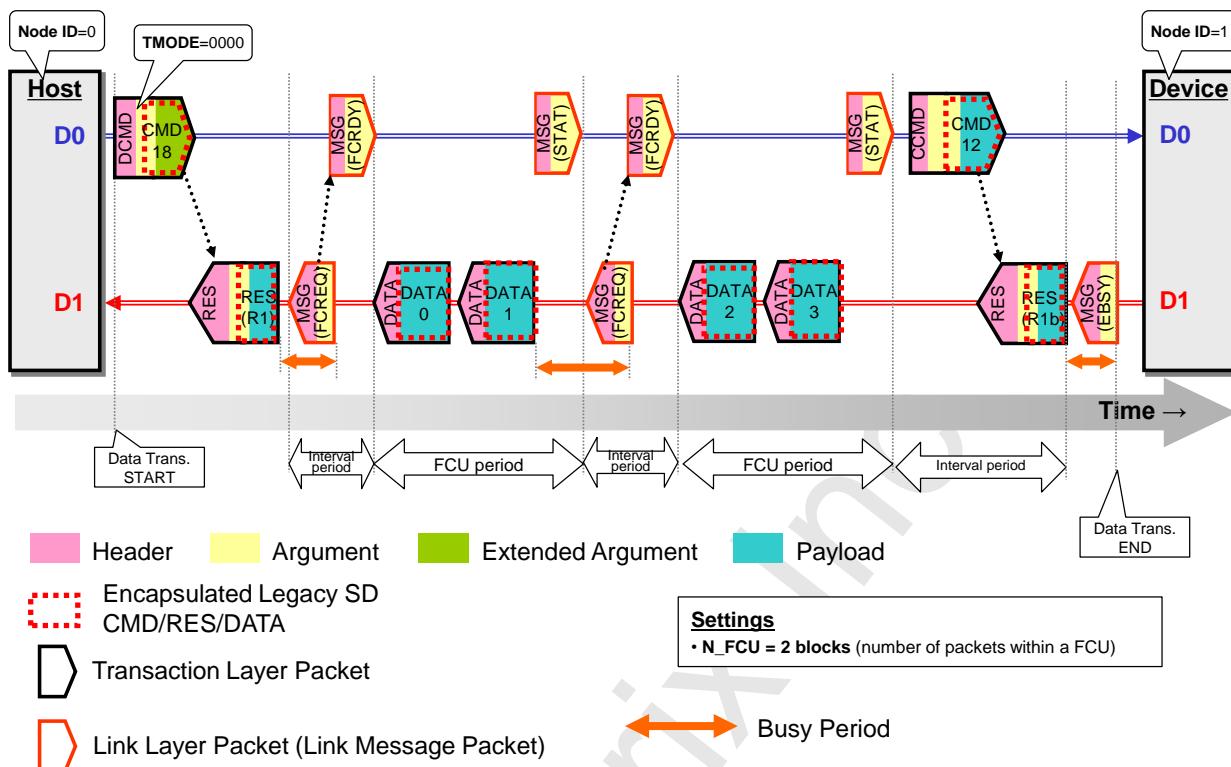


Figure 7-27 : Sequence of Read DCMD on SD-TRAN with Busy Period (Infinite Transfer Length)

The detailed field values in Figure 7-27 are as follows;

#### [DCMD]

- Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- Argument (DCMD):**
  - TMODE = 0000b (LM = 0, DM = 0)
  - APP = 0 (regular command)
  - CMD\_INDEX = 18 (command index in Legacy SD)
- Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD18.

#### [RES]

- Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD

- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 0 (Node ID of Host)
  - SID = 1 (Node ID of destination Device)
  - TID = The same value as TID of the corresponding DCMD
- **Payload (DATA):** transferred write data to Device

Different from Figure 7-26, Host shall issue CMD12 when terminating the transaction. Moreover, Device shall transmit EBSY after RES (R1b).

#### 7.2.6.4 Other Transaction Rules

The following items are other transaction rules on SD-TRAN.

- CMD0, CMD12, FULL\_RESET CCMD and TRANS\_ABORT CCMD can be issued during the Command Time Slot (CTS) defined in Section 6.2.13.4. Note that transaction rules related to CTS is same as in case of CM-TRAN.
- CMD0 may be issued in any state. In case of during 'prg' or 'data' state, MSG (EBSY) is not transmitted after RES of CMD0.
- Host shall not use native DCMD but encapsulated command such as CMD18 for Devices with application type = SD Memory. If Host issues native DCMD to Devices with application type = SD Memory, then Device behavior is not defined.
- When Host reads data from Device, Host sends MSG (STAT) at the end of each FCU period to keep compatibility to data read transaction in CM-TRAN (refer to Figure 6-50).
- During the transaction of CMD18 or CMD25, Device shall terminate the transaction when it receives CMD12 with arbitrary TID.

#### 7.2.7 Packet Handling

When Device receives a UHS-II packet whose DID corresponds with its Node ID, acceptability is defined by following rules.

- CMD (CCMD or DCMD): it follows the Card State Transition Table described in SD Specifications Part 1 Physical Layer Specification Version 4.00.
- RES: Device shall not accept RES packet.
- DAT: Device accepts DAT only in 'rcv' state in Figure 7-15. It shall not accept in other state.

#### 7.2.8 Error Handling

##### 7.2.8.1 Concept

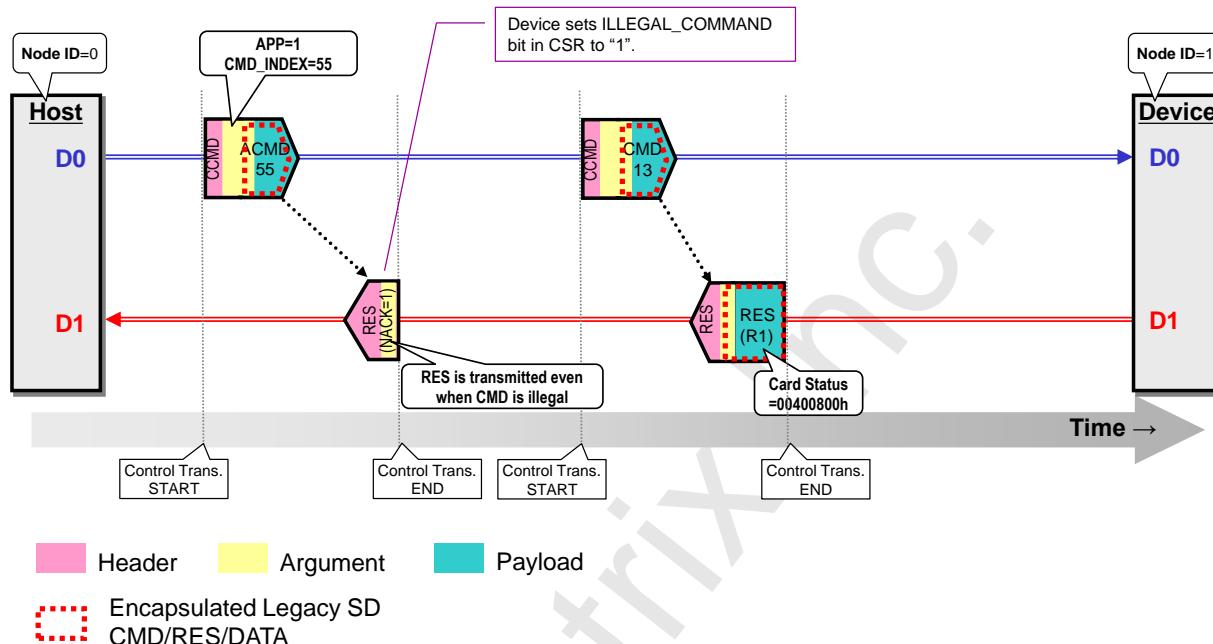
Same as Legacy SD specifications, Host can know the error of the corresponding CMD from Card Status Register (CSR). Error registers in CSR are automatically cleared when Host reads them.

In UHS-II, the following two points are different from Legacy SD.

- Device shall respond RES with NACK = 1 if it receives illegal CMD.
- CRC error is notified by MSG (STAT) only during interval period (Refer to Section 6.2.15 for more details).

### 7.2.8.2 Detecting Illegal CMD

Figure 7-28 illustrates a transaction rule when undefined CMD (ACMD55) is issued, as an example of detecting illegal command



**Figure 7-28 : Detecting Illegal CMD (Example 1)**

Originally, Device does not respond for illegal command in Legacy SD protocol, but in UHS-II protocol, Device shall transmit RES with NACK = 1 to Host in this case. The RES format is described in Section 7.2.1.4.

Same as Legacy SD protocol, Host can get the reason of the error from Card Status (00400800h in above case) by issuing CMD13 (SEND\_STATUS).

Figure 7-29 illustrates another example that Host issues CMD12 in 'tran' state.

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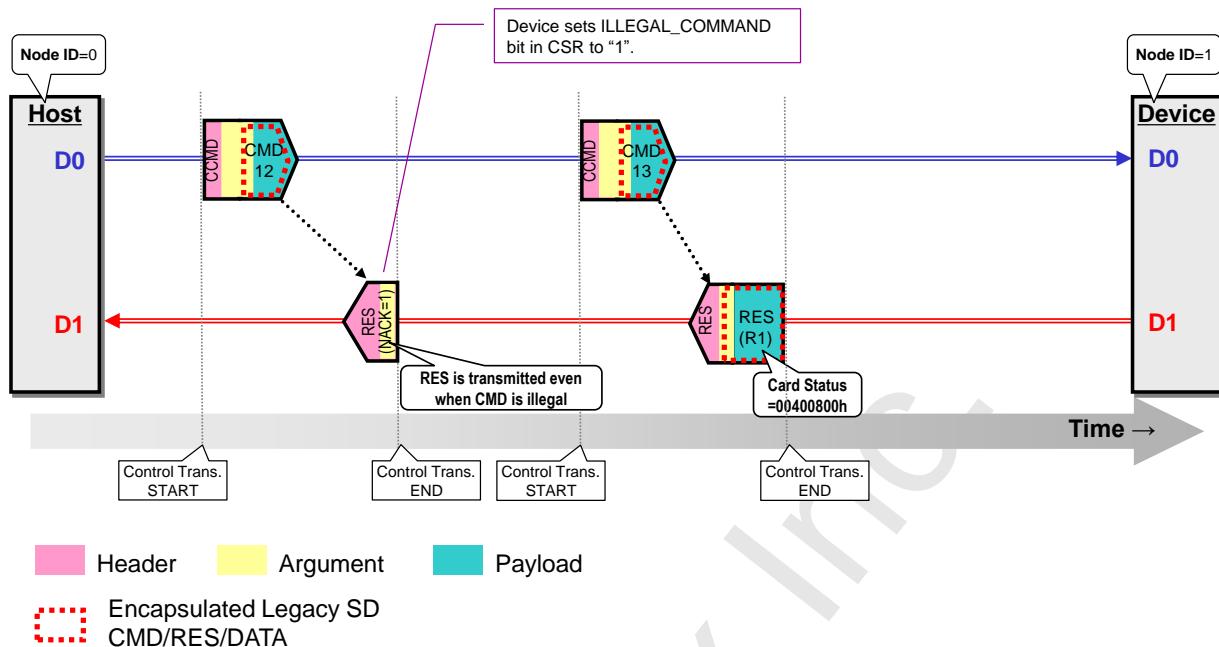


Figure 7-29 : Detecting Illegal CMD (Example 2)

## 7.2.8.3 Reaching Read Address to the End of User Data Area

Figure 7-30 illustrates a sequence for CMD18 if the read address comes at the last block of User Data Area.

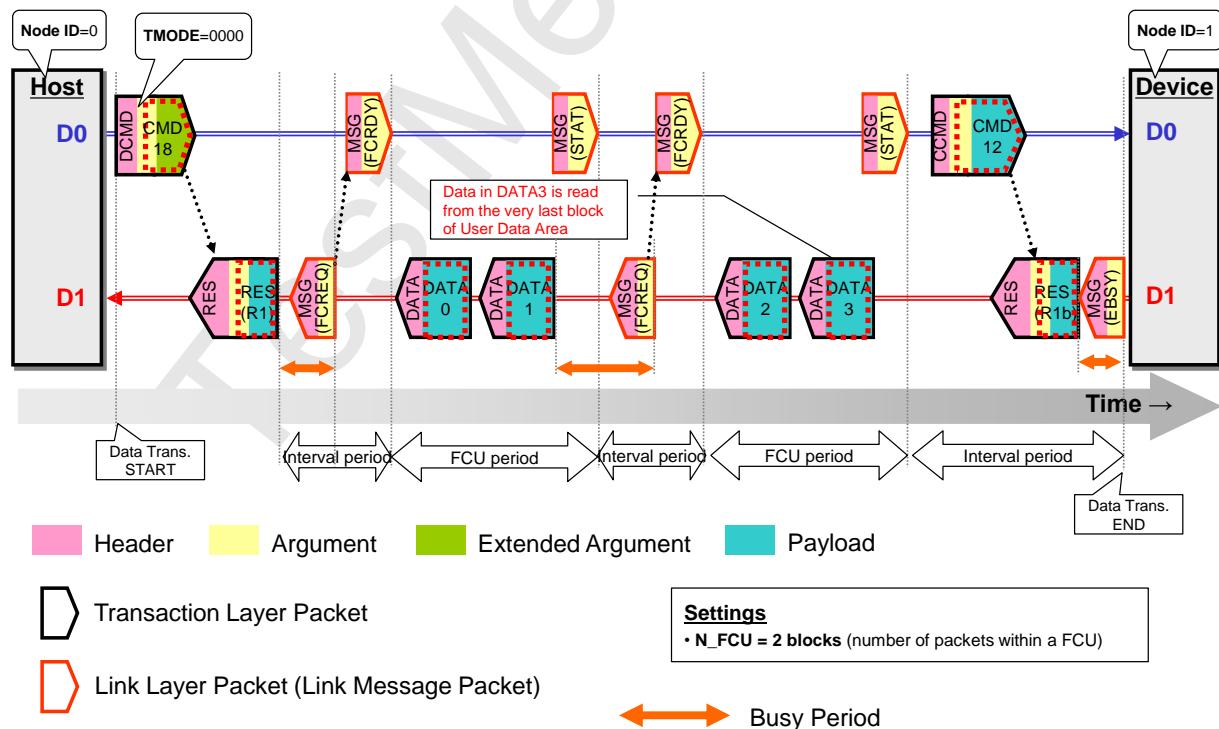


Figure 7-30 : Sequence of Read DCMD (at the End of User Data Area)

Device shall not send MSG (FCREQ) with UNRECOVERABLE\_ERROR = 0 if it completes sending the last block (DATA3, in the above example) after receiving MSG (STAT). Host detects the illegal situation from timeout defined in Section 7.3. Host is required to issue CMD12 in order to terminate this transaction.

In addition, Device shall not transmit the whole DATA Burst if the reading address reaches the end of User Data Area on the way of constructing the DATA Burst. In this case, Device can transmit MSG (FCREQ) with UNRECOVERABLE\_ERROR or give up transmitting MSG (FCREQ). Refer to Section 7.3.2 for the detailed sequence of timeout.

This error can be also occurred in the following cases.

- Other read DCMD
- Reading other memory area such as Protected Area.
- CMD18 with LM = 1 if TLEN is so large as to exceed the end of memory area.
- Other errors occur during read operation such as ECC failure.

#### 7.2.8.4 Reaching Write Address to the End of User Data Area

Figure 7-31 and Figure 7-32 illustrate sequences for CMD25 if the write address comes at the last block of User Data Area.

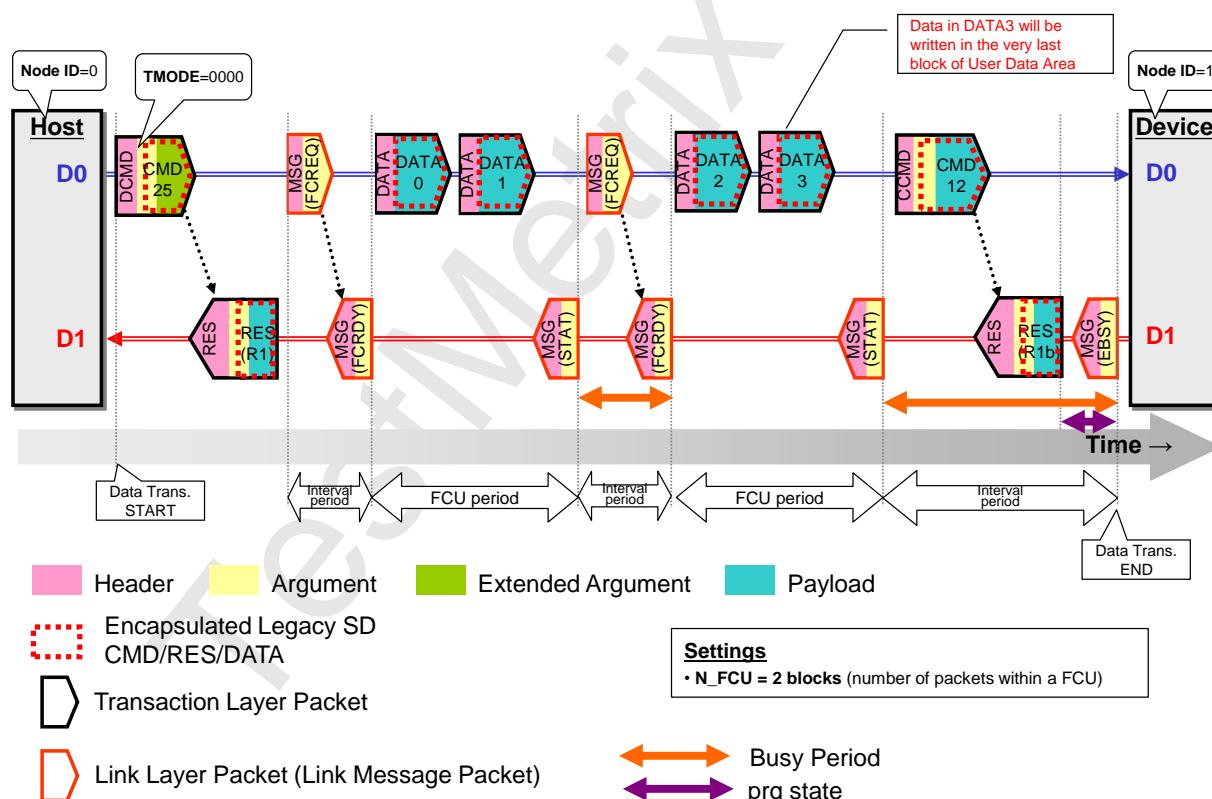
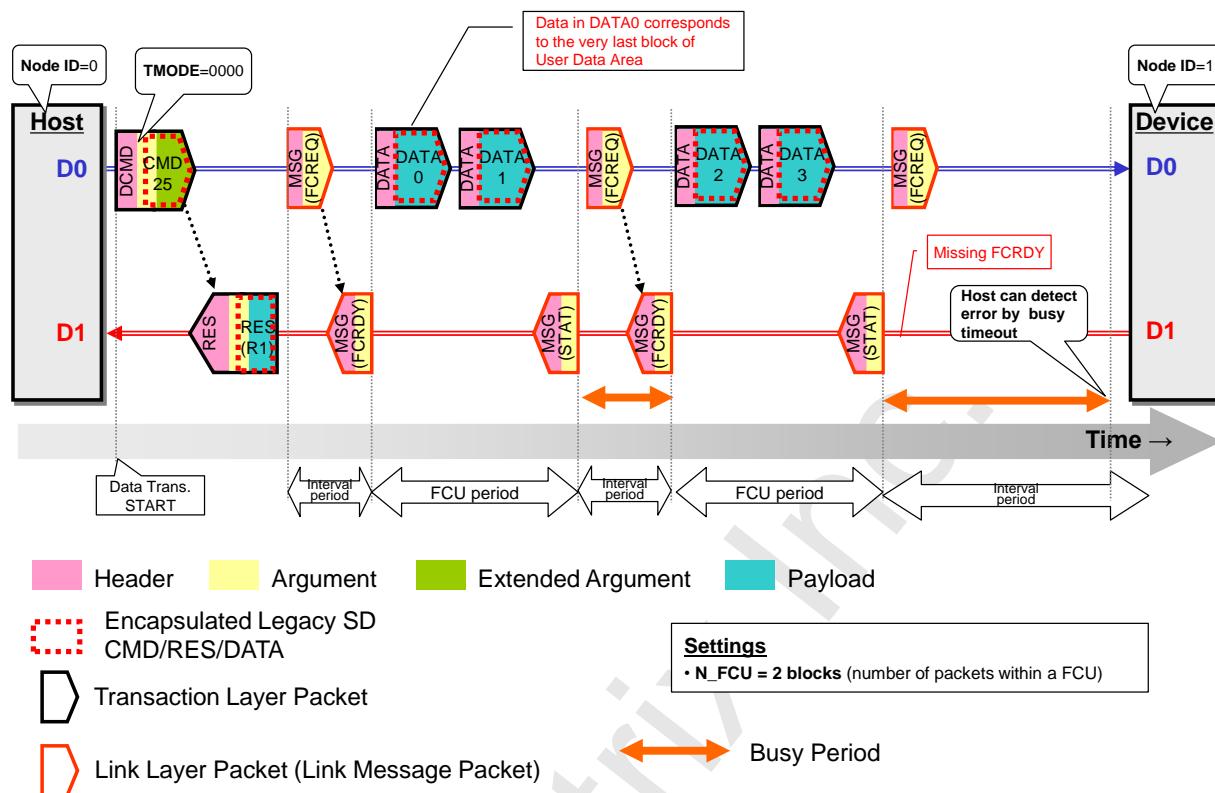


Figure 7-31 : Sequence of Write DCMD (at the End of User Data Area 1)

Like Figure 7-31, Host shall issue CMD12 just after receiving MSG (STAT) associated with the last block of Use Data Area. In this case, OUT\_OF\_RANGE flag is not set to 1 in RES of CMD12.

Figure 7-32 illustrates the case that Host accidentally sends DATA Burst or MSG (FCREQ) after the writing address reaches the end of User Data Area.



**Figure 7-32 : Sequence of Write DCMD (at the End of User Data Area 2)**

In this case, Data in DATA0 is written properly, but Data in other DATA packets are not written. Device notifies the illegal situation to Host by MSG (STAT or FCRDY) with UNRECOVERABLE\_ERROR or MSG (EBSY) with MEMORY\_ERROR, or gives up transmitting these MSGs in order to lead timeout when it becomes possible. Refer to Section 7.3.2 for the detailed sequence of timeout.

This error can be also occurred in the following cases.

- Other write DCMD
- Writing other memory area such as Protected Area.
- CMD25 with LM = 1 if TLEN is so large as to exceed the end of memory area.

## 7.3 Timing Rules

### 7.3.1 Overview

Based on the timing rules described in Section 6.3.1, timing rules for SD-TRAN are specified as follows.

Group	Abbreviation	Description	Max Value
Flow Control in SD-TRAN	Tres_freq(r)	Time from RES EOP reception to FCREQ SOP issuing in read transaction. This is related to read busy timeout or access time.	See Note (1)
	Tres_freq(w)	Time from RES EOP reception to FCREQ SOP issuing in write transaction	N/A
	Tstat_freq(r)	Time from STAT EOP reception to FCREQ SOP issuing in read transaction. This is related to read busy timeout or access time.	See Note (1)
	Tstat_freq(w)	Time from STAT EOP reception to FCREQ SOP issuing in write transaction.	N/A
	Tfreq_fcrdy(r)	Time from FCREQ EOP reception to FCRDY SOP issuing in read transaction.	N/A
	Tfreq_fcrdy(w)	Time from FCREQ EOP reception to FCRDY SOP issuing in write transaction. This is related to write busy timeout.	1 [sec] (See Note (2))
Busy MSG operation in SD-TRAN	Tr_stat_ebsy	Time from MSG (STAT) EOP transmission to MSG (EBSY) SOP issuing in case of read operation.	100 [msec]
	Tw_stat_ebsy	Time from MSG (STAT) EOP reception to MSG (EBSY) SOP issuing in case of write operation. This is related to write busy timeout or busy length	1 [sec] (See Note (2))
	Tr_res_ebsy	Time from RES (R1b) EOP reception to MSG (EBSY) SOP issuing in case of read operation.	100 [msec]
	Tw_res_ebsy	Time from RES (R1b) EOP reception to MSG (EBSY) SOP issuing in case of write operation. This is related to write busy timeout or busy length.	1 [sec] (See Note (2))
	Te_res_ebsy	From RES (R1b) EOP reception to MSG (EBSY) SOP issuing in case of erase operation. This is related to erase busy timeout.	See Note (3)

Note:

- (1) If the Application Type is SD-memory Card regulated in CFG\_REG, they shall be applied the value defined in Section 4.6.2.1 for memory commands, and Section 5.7.2.1 and 5.7.2.4 for extension commands on "SD Specifications Part 1 Physical Layer Specification Version 4.10".
- (2) This value is not applied during the "recording period" defined by Speed Grade specification. Refer to "SD Specifications Part 1 Physical Layer Specification Version 4.10" for more details.
- (3) If the Application Type is SD-memory Card regulated in CFG\_REG, they shall be applied the value defined in Section 4.10.2 and Section 4.14 of "SD Specifications Part 1 Physical Layer Specification Version 4.10".

**Table 7-5 : Device Timing Parameters in SD-TRAN**

Note that maximum time from R1b to EBSY not appeared in Table 7-5 (e.g. CMD20) shall be applied the value defined in "SD Specifications Part 1 Physical Layer Specification Version 4.00".

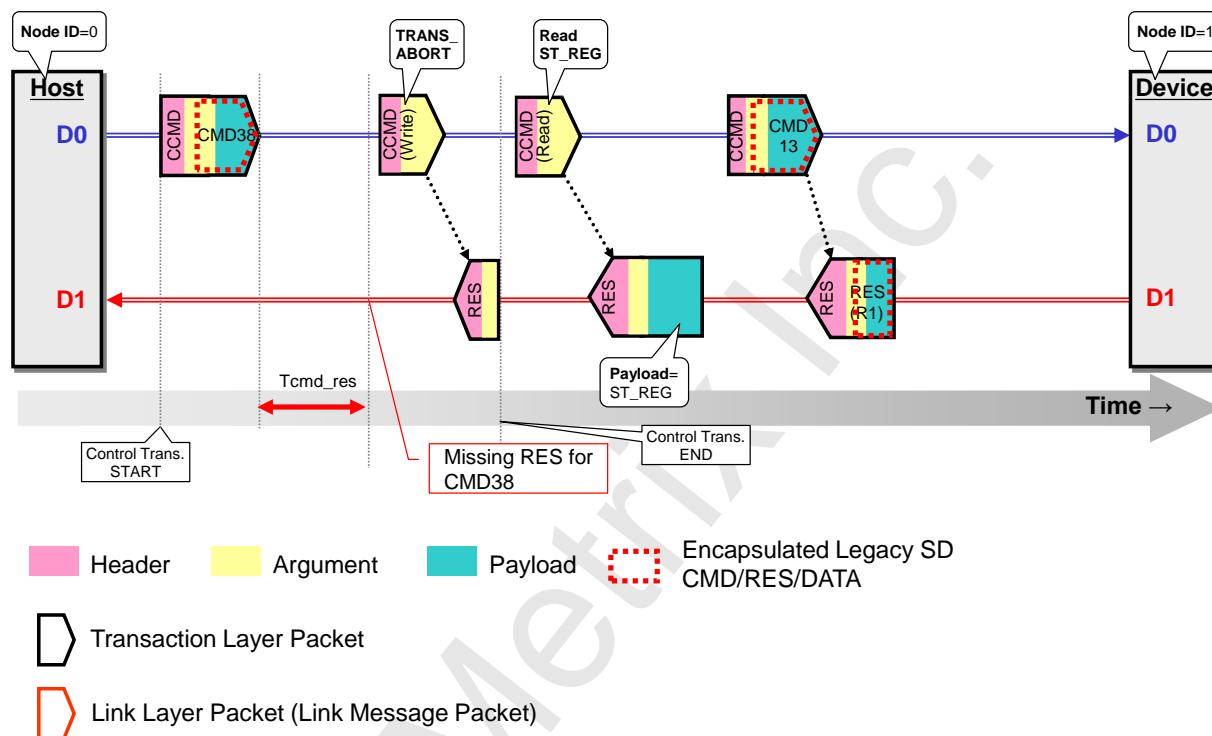
Total time for Initialization of SD-TRAN Device shall be up to 1 [sec]. To say strictly, when SD-TRAN is implemented, Device shall satisfy the following inequality:

- Tactivate + Tfwd\_init\_cmd(s) + Tfwd\_init\_cmd(c) + Tacmd41 ≤ 1 [sec], where,
- Tacmd41 is duration from the first ACMD41 to the completion of Initialization by ACMD41.

- Other parameters are defined in Section 6.3.1.

### 7.3.2 Example Sequence of Timeout Occurrence in SD-TRAN

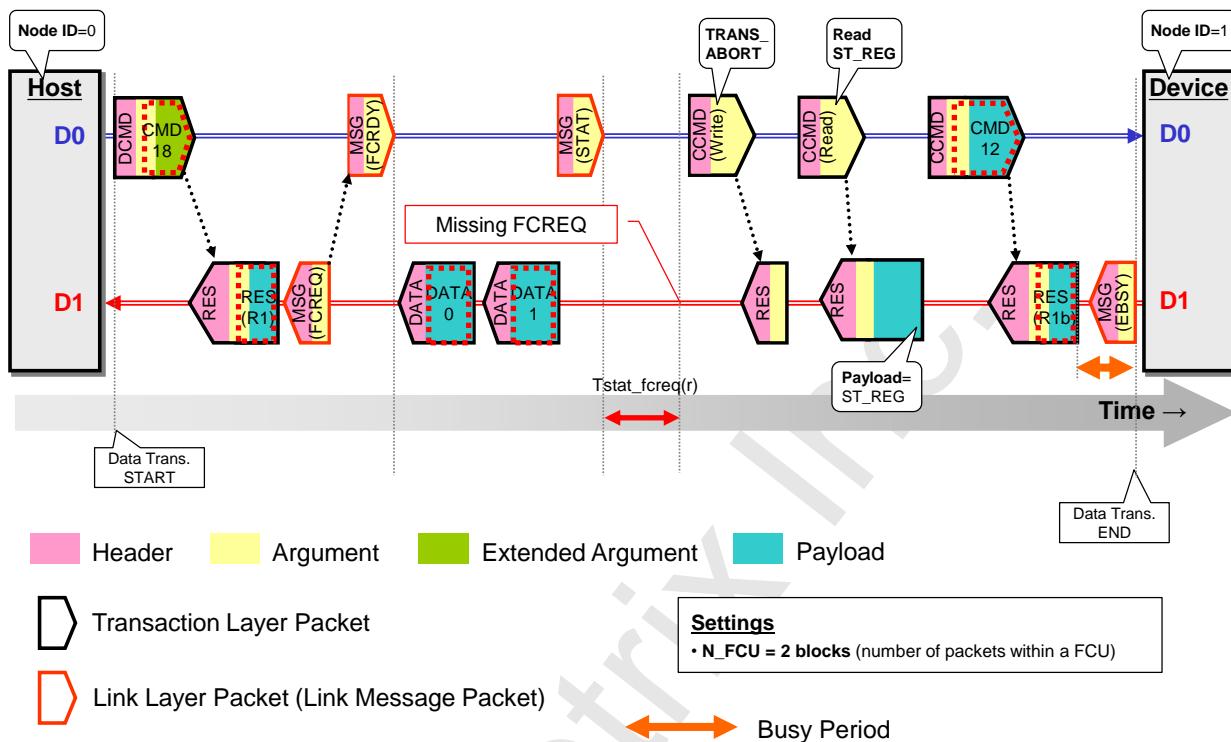
Figure 7-33 illustrates an example sequence when Host cannot receive the RES of encapsulated CCMD (CMD38 in this example).



**Figure 7-33 : Example Sequence When Missing RES of CMD38**

When Host detects timeout of Tcmd\_res after issuing CMD38, Host should issue TRANS\_ABORT CCMD to terminate the transaction of CMD38. Then Host should read error identifiers and status of Device indicated in Device's ST\_REG. Additionally, Host can issue CMD13 to get Card Status.

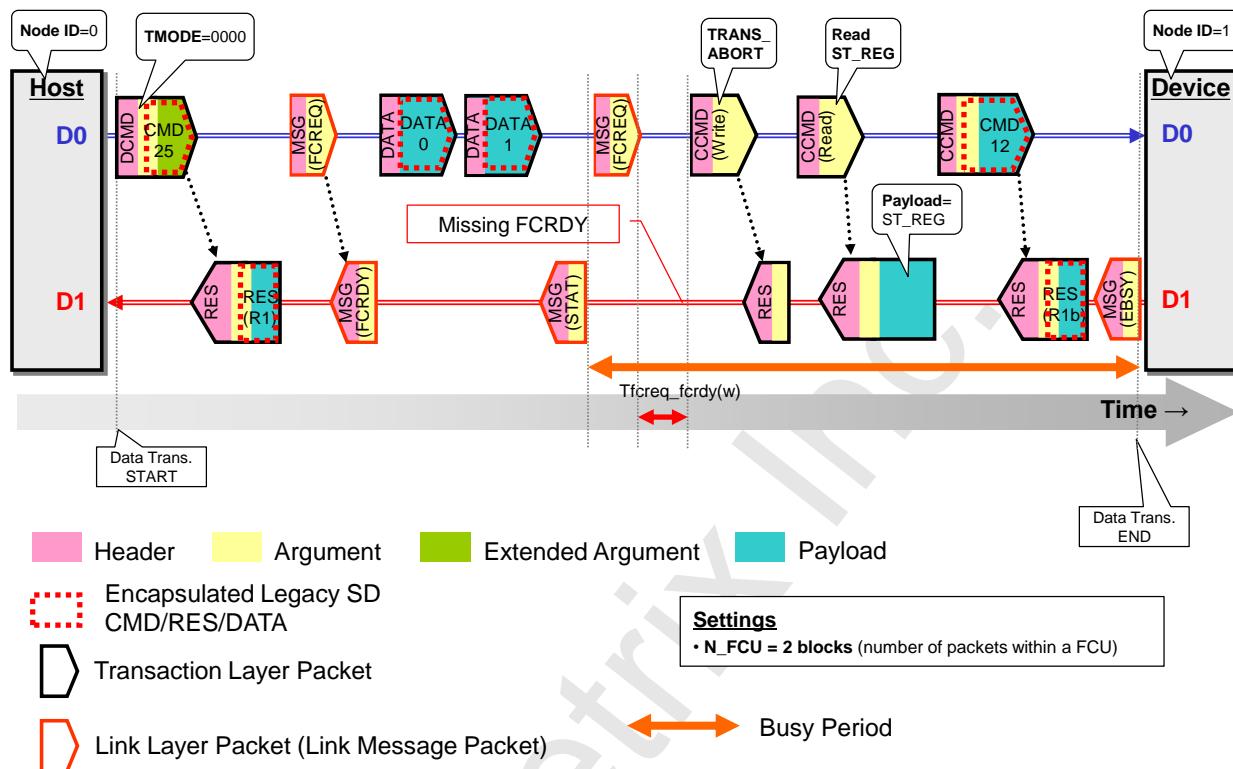
Figure 7-34 illustrates an example sequence when Host cannot receive FCREQ during data transaction by CMD18.



**Figure 7-34 : Example Sequence When Missing FCREQ during Data Transaction by CMD18**

Different from the example in UHS-II native protocol (described in Figure 6-61), when Host detects timeout of  $T_{stat\_freq}(r)$  during data read transaction, Host should issue TRANS\_ABORT CCMD at first to recover from the illegal situations, read error identifiers and status of Device indicated in Device's ST\_REG, and then it shall issue the encapsulated CMD12 to terminate the outstanding data transmission. Moreover, Host can issue CMD13 if necessary (not illustrated in Figure 7-34).

Figure 7-35 illustrates an example sequence when Host cannot receive FCRDY during data transaction by CMD25.



**Figure 7-35 : Example Sequence When Missing FCRDY during Data Transaction by CMD25**

Same as the example illustrated in Figure 7-34, when Host detects timeout of Tfcreq\_fcrdy(w) during data write transaction, Host should issue TRANS\_ABORT CCMD, read ST\_REG, and shall issue CMD12 in this order. In addition, transmitted data is not guaranteed in this case.

## 8. 2L-HD Mode (optional)

### 8.1 Overview

Lower operating frequency generally provides applicability to a variety of hosts due to easy implementation of whole system. Duplex mode switching between FD mode and 2L-HD mode achieves a good balance between easy controllability and higher bus efficiency under I/O pin count restriction as in SD Memory.

FD mode provides easy controllability by setting D0 and D1 to different directions, because handshake between Host and Device can be performed anytime. It is the default mode in UHS-II. On the other hand, 2L-HD mode realizes higher speed data transfer than FD mode by setting D0 and D1 to the same direction. 2L-HD mode is optional in UHS-II specification.

Basically, CCMD, DCMD, RES and MSG are transmitted in FD mode. Only DATA can be transmitted in both FD mode and 2L-HD mode. If Host intends to read or write data in 2L-HD mode, duplex mode switching shall be executed after DCMD and RES handshake.

On the way of data transmission in 2L-HD mode, it suspends data transmission and switches to FD mode temporarily in order to keep room for sending CCMD or MSG. Then it switches to 2L-HD mode again and continue data transmission.

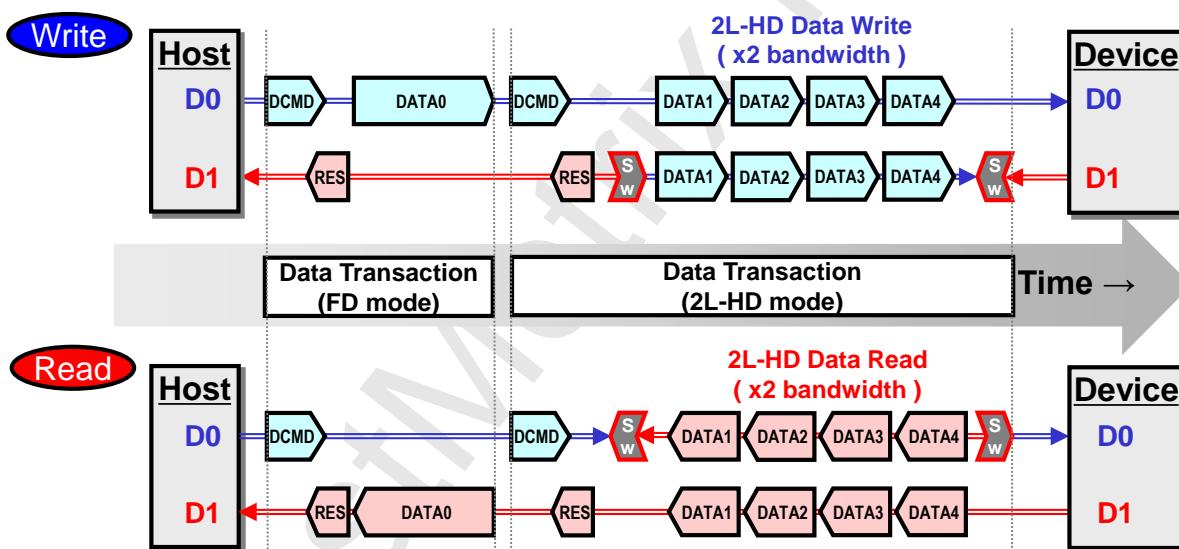


Figure 8-1 : Overview of FD Mode and 2L-HD Mode

### 8.2 PHY Layer Specification

#### 8.2.1 Direction Switching

Refer to Chapter 4.

### 8.3 Link Layer Specification

#### 8.3.1 Framing Rules for 2L-HD Mode

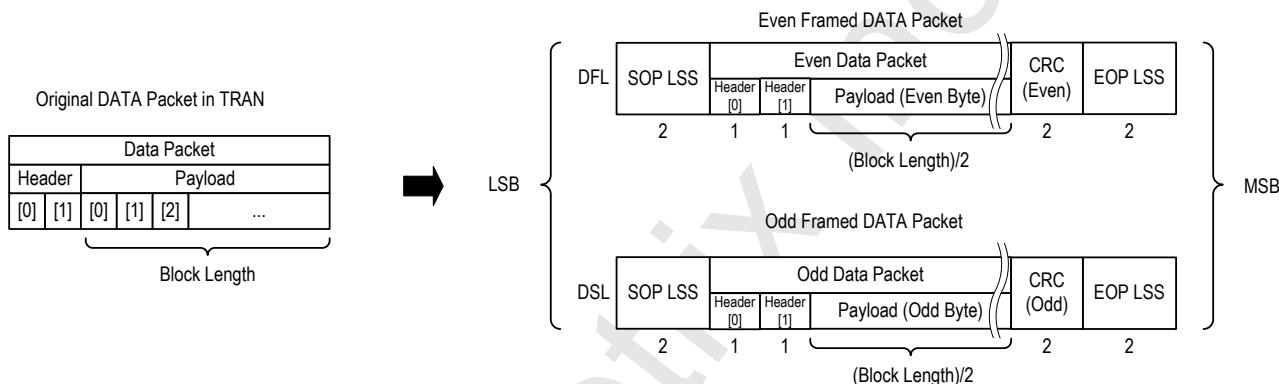
Framing rules for CCMD, DCMD, RES and MSG are identical to those described in Section 5.2.6, because such packets are transmitted only in FD mode.

##### 8.3.1.1 Block Mode

Figure 8-2 illustrates a framing rule for DATA packet for 2L-HD mode in case of Block Mode. Payload in the original DATA packet in TRAN is divided into two framed DATA packet called "Even Framed DATA

packet" and "Odd Framed DATA packet". That is, Payload[0], Payload[2], ... are assigned to Even Framed Data Packet, Payload[1], Payload[3], ... are assigned to Odd Framed Data Packet respectively, where the bracketed number denotes the byte position in each field counted from 0. Note that Header is not divided and assigned to both Data Packets as it is.

Even Framed DATA packet consists of SOP LSS, Even Data Packet, CRC (Even), and EOP LSS. Similarly, Odd Framed DATA packet consists of SOP LSS, Odd Data Packet, CRC (Odd), and EOP LSS. CRC (Even) is calculated from Even Data Packet, and CRC (Odd) is calculated from Odd Data Packet. Even Framed DATA packet is transmitted through the Direction Fixed Lane (abbreviated to DFL) whose direction does not change within a transaction of 2L-HD mode (D0 for Host and D1 for Device). On the other hand, Odd Framed DATA packet is transmitted through the Direction Switched Lane (abbreviated to DSL) whose direction changes within a transaction of 2L-HD mode (D0 for Device and D1 for Host). Note that the basic length of Payload in each Framed DATA packet is half of the Block Length.



**Figure 8-2 : DATA Packet Framing Rule for 2L-HD Mode (Block Mode)**

The rule illustrated in Figure 8-2 is applicable when Block Length is multiple of 4. Otherwise, PAD shall be inserted adequately between Data Packet and CRC, for the length of each Framed DATA Packet shall be even byte. Figure 8-3 illustrates three patterns ([a], [b], and [c]) of framing rule in 2L-HD mode if the Block Length of original payload is an aliquant of 4. Note that two PADs are inserted in case of pattern [a].

The CRC calculating and adding rules are same as described in Section 5.2.6.2.1.

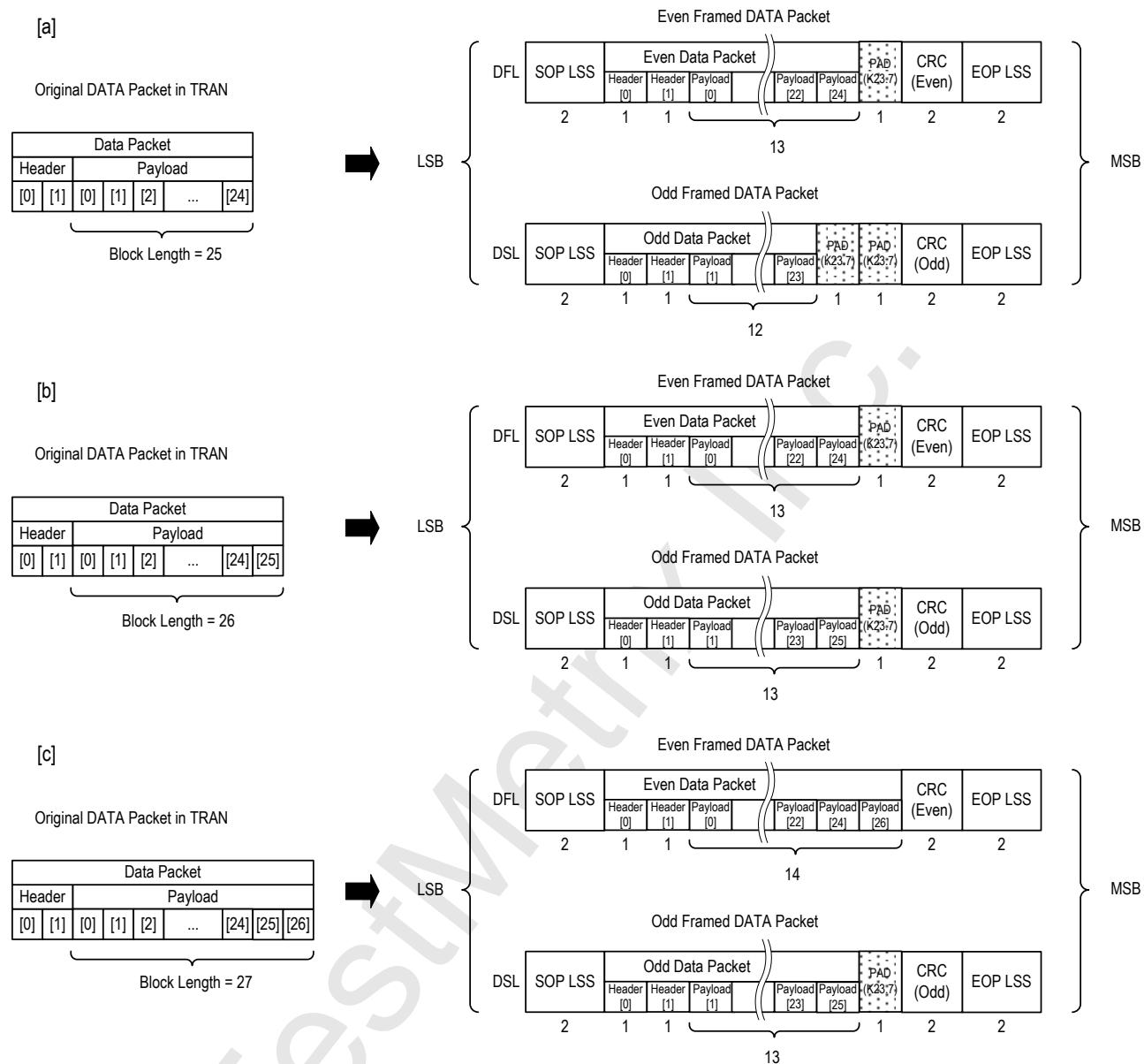
**Figure 8-3 : DATA Packet Framing Rule in 2L-HD Mode (Block Length Is Aliquot of 4)**

Figure 8-4 illustrates a DATA Burst framing rule in 2L-HD mode. The rule is similar to that in FD mode described in Section 5.2.6.2. As a result, two DATA Bursts are generated in the same time; one is for D0 and the other is for D1.

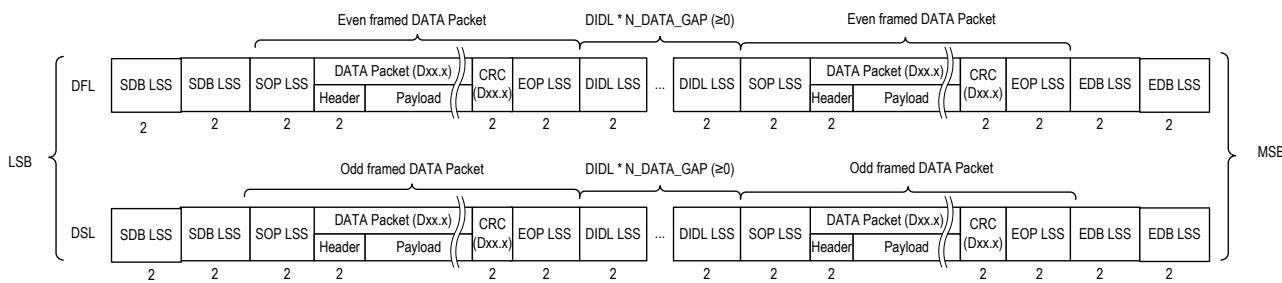


Figure 8-4 : DATA Burst Framing Rule in 2L-HD Mode

### 8.3.1.2 Byte Mode

As mentioned in Section 6.2.2.4, Data transmission by Byte Mode is inhibited in 2L-HD mode. So DCMD with DM = 1 and TLUM = 1 shall be regarded as an illegal command (ARG\_ERR).

### 8.3.2 Sequence for Duplex Mode Switching

Figure 8-5 illustrates a duplex mode switching sequence in case of data read in 2L-HD mode.

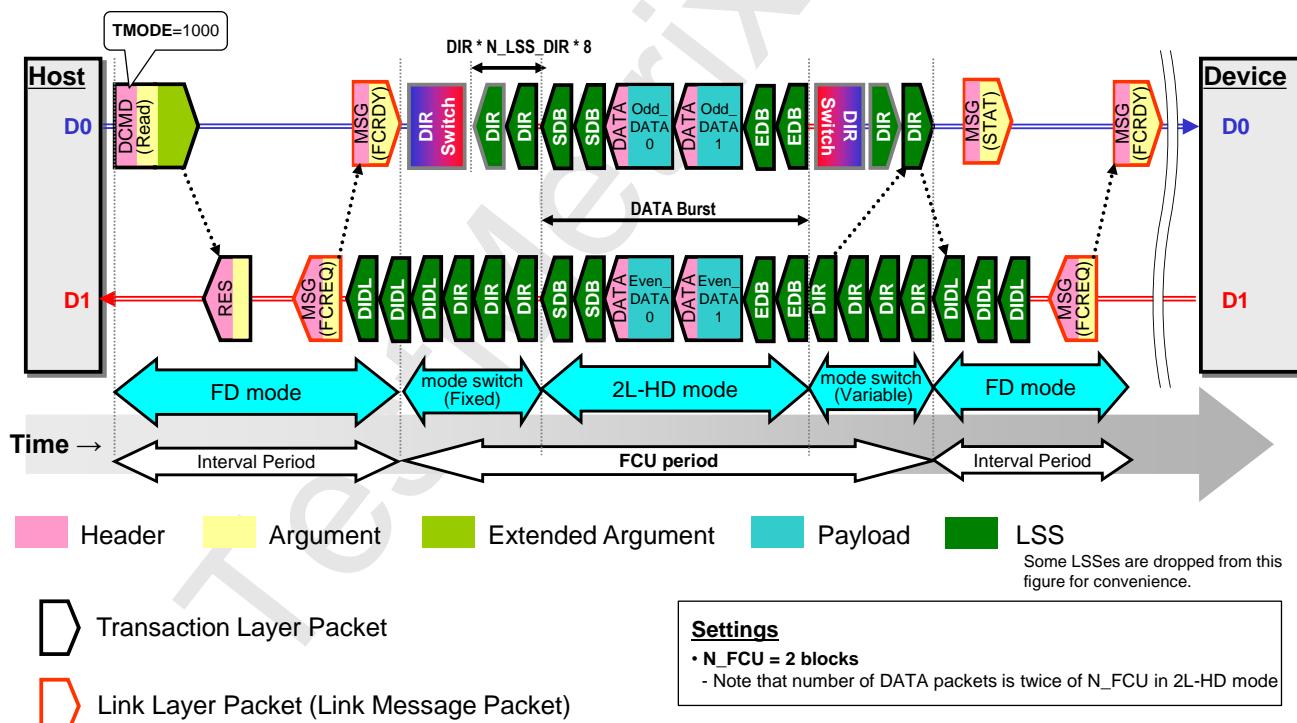


Figure 8-5 : Duplex Mode Switching Sequence in Data Read

First, Host (= DATA Receiver) sends Read DCMD with TMODE = 1000b which means 2L-HD mode. Duplex mode switching from FD mode to 2L-HD mode is triggered by FCRDY transfer via switching Lane (in this case, D0 Lane) and completed by DIR LSS transfer via both Lanes.

Just after transmitting FCRDY MSG, Host starts switching D0 Lane direction from default Tx to Rx. On the other hand, when Device (= DATA Initiator) receives the FCRDY MSG, it starts transmitting DIR LSS on D1 Lane iteratively. Then Device also starts switching D0 Lane direction from default Rx to Tx. To avoid a contention, the direction switch from Tx to Rx shall always be performed prior to the one from

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Rx to Tx. Refer to Section 8.3.4 for more details. After completing direction switch, Device transmits at least the predetermined number ( $N_{LSS\_DIR} * 8$ ) of DIR LSS for each Lane to ensure symbol lock of the switched D0 Lane.

During FCU period for 2L-HD mode, DATA Bursts are transmitted via both Lanes in parallel. Note that the number of DATA packets in an FCU is twice as much as  $N_{FCU}$ .

Duplex mode switching from 2L-HD mode to FD mode is triggered by EDB transfer via both Lanes and completed by DIDL LSS transfer via unswitched Lane (in this case, D1 Lane). At the termination of 2L-HD mode, Device shall transmit EDB LSS via both Lanes simultaneously. Just after that, Device starts switching D0 Lane direction from Tx to default Rx and transmitting DIR LSS on D1 Lane iteratively. If Host receives at least one of the EDB LSS from two Lanes, and the following DIR LSS via D1 Lane, it also starts switching D0 Lane direction from Rx to default Tx. This is same for Device in case of write transaction shown in Figure 8-6. After completing direction switch, Host transmits DIR LSS via D0 Lane. Then Device transmits DIDL LSS when it succeeds to receive DIR LSS. Host continues to transmit DIR LSS until it receives DIDL LSS via D1 Lane. After receiving DIDL LSS, Host can send STAT MSG in FD mode.

Figure 8-6 illustrates a duplex mode switching sequence in case of data write in 2L-HD mode. Except DCMD - RES handshake, whole operations are symmetrical to the data read case shown in Figure 8-5.

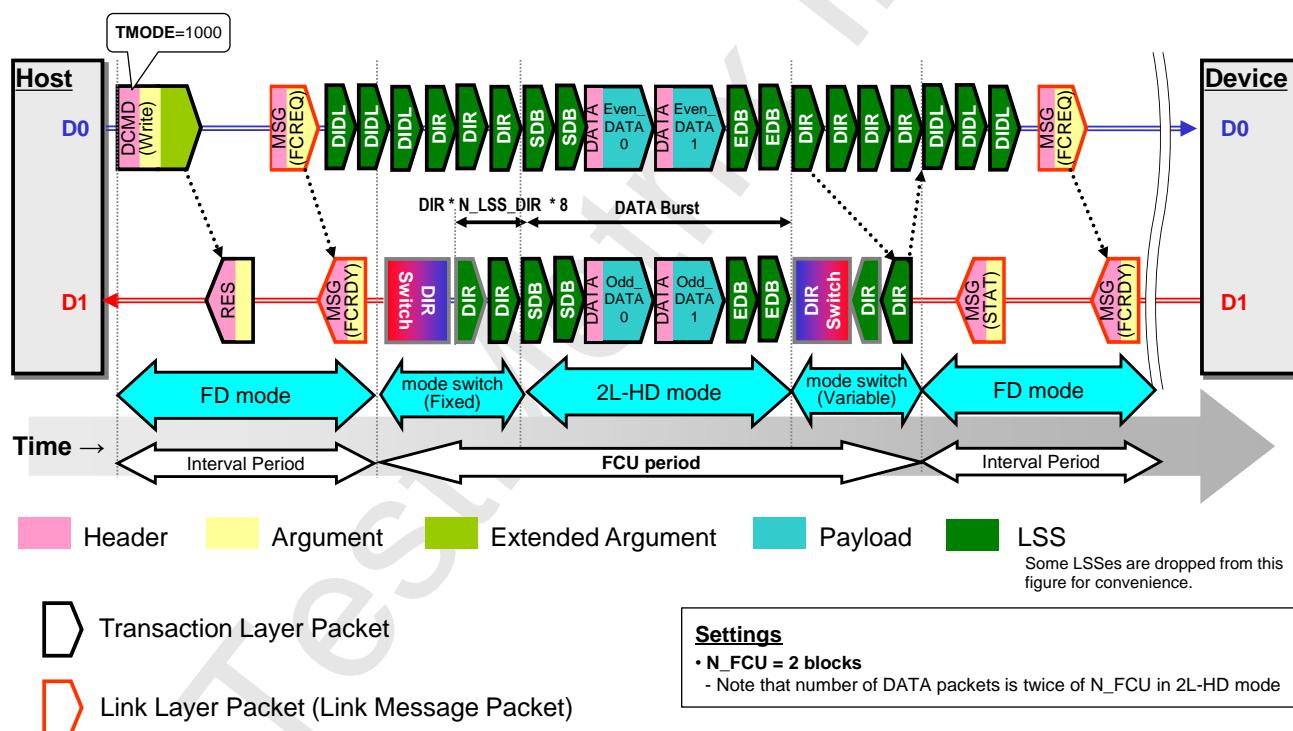
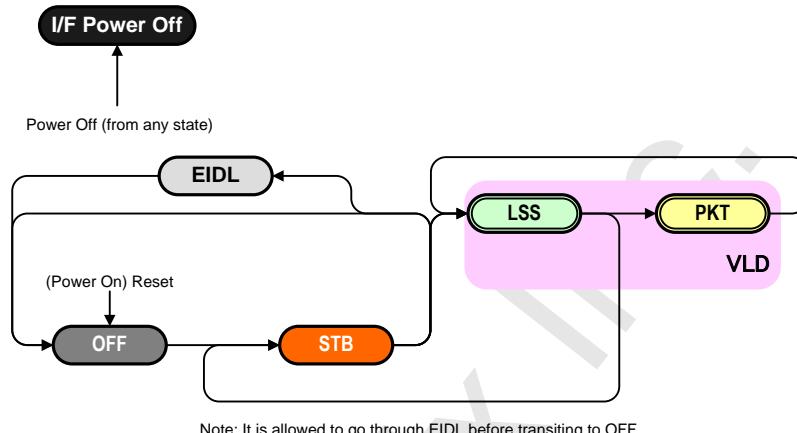


Figure 8-6 : Duplex Mode Switching Sequence in Data Write

### 8.3.3 PLSM for 2L-HD Mode

In FD mode, Host sets D0 Lane to Tx and D1 Lane to Rx. On the other hand, Device sets D0 Lane to Rx and D1 Lane to Tx as a default. These default Tx and Rx are controlled in accordance with PLSM shown in Figure 5-13. On the other hand, non-default Tx, such as D0.Tx of Device, needs not to transit to EIDL because non-default Rx does not have an Amplitude Detector in PHY.

Figure 8-7 illustrates a PLSM for non-default Tx or Rx in 2L-HD mode.



**Figure 8-7 : PLSM for Non-default Tx or Rx in 2L-HD Mode**

For supporting 2L-HD mode, both sides of LINK need to have two different PLSMs for each Lane, one for default Tx or Rx and the other for non-default Tx or Rx.

### 8.3.4 Details of Duplex Mode Switching Sequence

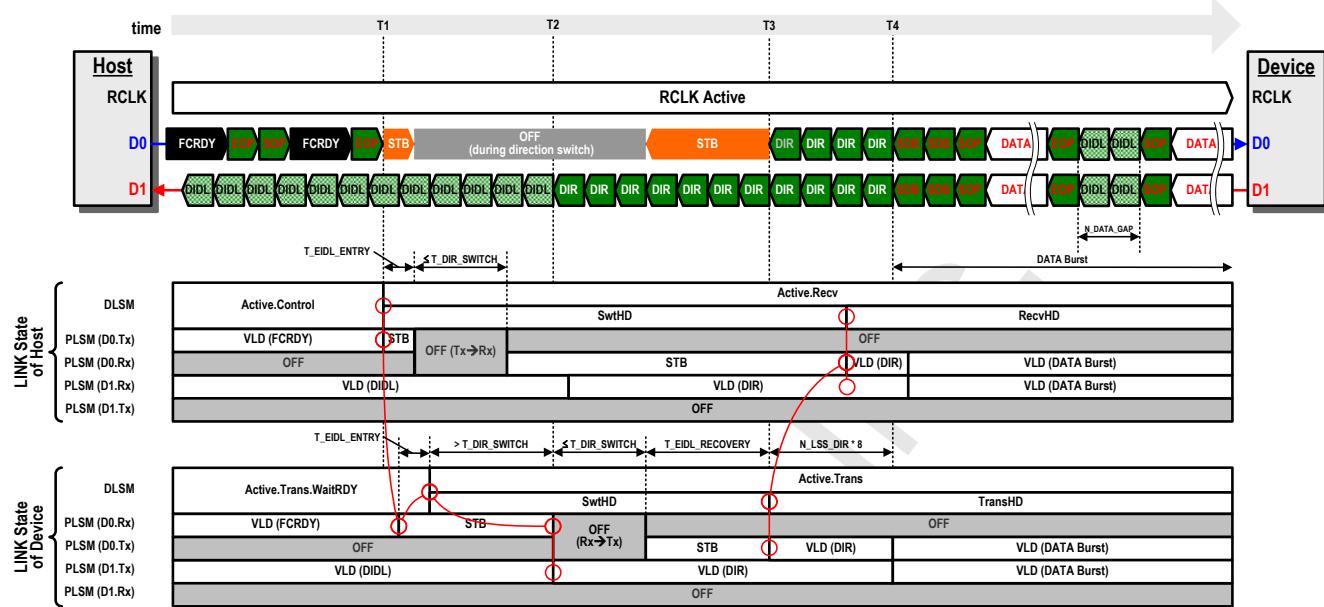
To avoid bus conflict, nodes shall comply with the sequence and timing of switching Lane direction.

- Direction Switch from Tx to Rx
  - The Node shall transmit STB.H during T\_EIDL\_ENTRY (4 SI) after transmitting EOP of FCRDY MSG or EDB.
  - The Node shall complete switching direction from Tx to Rx within T\_DIR\_SWITCH (8 SI) after completing transmission of STB.H.
  - When transmitting FCRDY MSG with UNRECOVERABLE\_ERROR=1, the Node shall not perform duplex mode switching.
- Direction Switch from Rx to Tx
  - The Node shall wait completion of direction switching from Tx to Rx for other side. How to detect whether the other Node completes direction switch from Tx to Rx is up to implementation.
  - When receiving FCRDY MSG with UNRECOVERABLE\_ERROR=1, the Node shall not perform duplex mode switching.

In following subsections, examples of detailed sequence for duplex mode switching are described.

### 8.3.4.1 2L-HD Read Transaction

Figure 8-8 illustrates a LINK state transition during duplex mode switching from FD to 2L-HD mode in case of data read.



**Figure 8-8 : Example LINK State Transition during Duplex Mode Switching (FD to 2L-HD Read)**

T1: Just after transmitting FCRDY MSG in Active.Control, LINK of Host (= DATA Receiver) transits its DLSM to Active.Recv.SwtHD and instructs the PHY to send STB.H for the duration of T\_EIDL\_ENTRY (= 4 SI) before entering to OFF state. After that, LINK of Host requests the PHY to start direction switch of D0 Lane from default Tx to non-default Rx. And PHY of Host performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, PLSM for D0.Rx (non-default Rx) of Host transits from OFF to STB immediately inside PHY to get ready for receiving valid symbols via switched D0 Lane.

On the other hand, it takes LINK of Device (= DATA Initiator) a while to determine whether the receiving packet is FCRDY in accordance with Packet Receiving Flow described in Section 5.8. And after receiving FCRDY MSG, LINK of Device waits T\_EIDL\_ENTRY and transits its DLSM to Active.Trans.SwtHD. But prior to starting direction switch, LINK of Device waits for more than T\_DIR\_SWITCH to avoid a contention between both sides of Tx in D0 Lane.

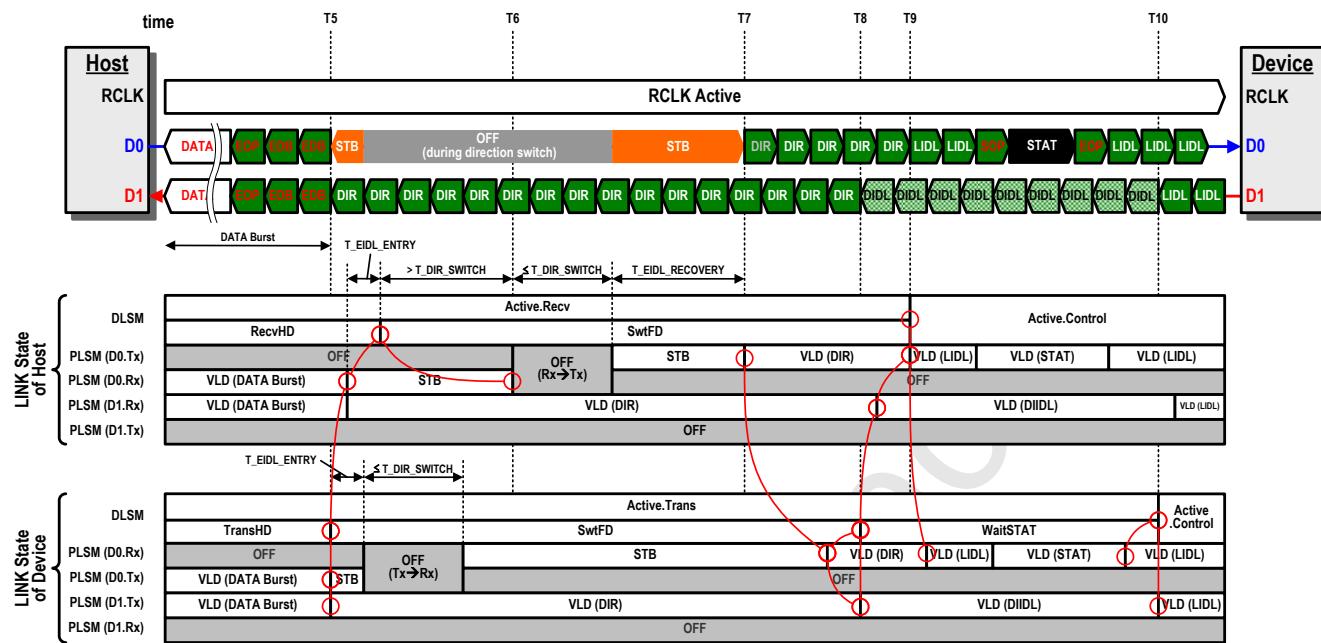
T2: After the elapse of more than T\_DIR\_SWITCH in Active.Trans.SwtHD, LINK of Device starts to send DIR LSS via unswitched D1 Lane and it also requests the PHY to start direction switch of D0 Lane from default Rx to non-default Tx. And PHY of Device performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, LINK of Device transits its PLSM for D0.Tx (non-default Tx) from OFF to STB and instructs the PHY to send STB.L for the duration of T\_EIDL\_RECOVERY to get ready for transmitting valid symbols via switched D0 Lane.

T3: After the elapse of T\_EIDL\_RECOVERY in STB.L, LINK of Device transits to Active.Trans.TransHD and starts to send at least the predetermined number (N\_LSS\_DIR \* 8) of DIR LSS for each Lane to acquire symbol lock. On the other hand, LINK of Host transits to Active.Recv.RecvHD after receiving DIR LSS via both Lanes.

T4: After transmitting N\_LSS\_DIR \* 8 of DIR LSS, Device starts to send DATA Burst via both Lanes.

Figure 8-9 illustrates a LINK state transition during duplex mode switching from 2L-HD to FD mode in case of data read.

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**Figure 8-9 : Example LINK State Transition during Duplex Mode Switching  
(2L-HD Read to FD)**

T5: Just after transmitting EDB LSS via both Lanes, LINK of Device (=DATA Initiator) transits its DLSM to Active.Trans.SwtFD and starts to send DIR LSS via unswitched D1 Lane and instructs the PHY to send STB.H via switched D0 Lane for the duration of T\_EIDL\_ENTRY before entering to OFF state. After that, LINK of Device requests the PHY to start direction switch of D0 Lane from non-default Tx to default Rx. And PHY of Device performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, PLSM for D0.Rx (default Rx) of Device transits from OFF to STB immediately inside PHY to get ready for receiving valid symbols via switched D0 Lane.

On the other hand, after receiving at least one of the EDB LSS via both Lanes, LINK of Host (= DATA Receiver) waits T\_EIDL\_ENTRY and transits its DLSM to Active.Recv.SwtFD. But prior to starting direction switch, LINK of Host waits for more than T\_DIR\_SWITCH to avoid a contention between both sides of Tx in D0 Lane.

T6: After the elapse of more than T\_DIR\_SWITCH in Active.Recv.SwtFD, LINK of Host also requests the PHY to start direction switch of D0 Lane from non-default Rx to default Tx. And PHY of Host performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, LINK of Host transits its PLSM for D0.Tx (default Tx) from OFF to STB and instructs the PHY to send STB.L for the duration of T\_EIDL\_RECOVERY to get ready for transmitting valid symbols via switched D0 Lane.

T7: After the elapse of T\_EIDL\_RECOVERY in STB.L, LINK of Host starts to send DIR LSS to acquire symbol lock in switched D0 Lane.

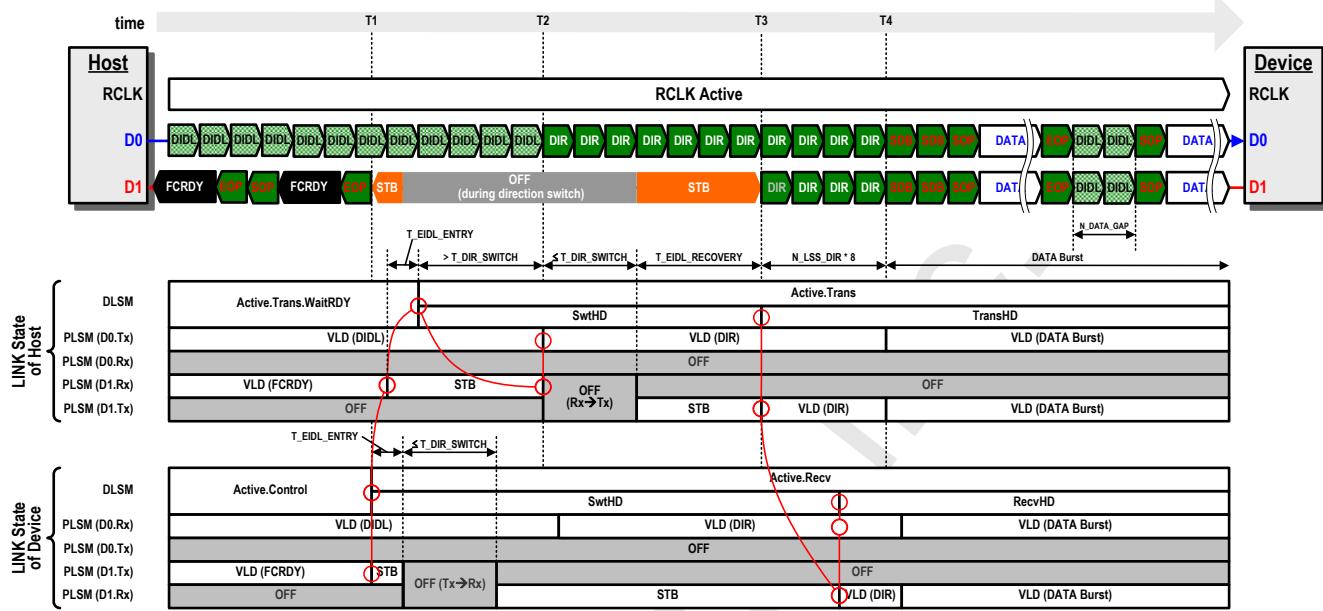
T8: After receiving DIR LSS from Host via switched D0 Lane, LINK of Device transits to Active.Trans.WaitSTAT and starts to send DIDL LSS same as in FD mode.

T9: After receiving DIDL LSS from Device via unswitched D1 Lane, LINK of Host transits to Active.Control and starts to send STAT MSG same as in FD mode. Note that LINK of Host sets D0 Lane to EIDL before and after transmitting STAT MSG in case of Low Power Mode.

T10: After receiving STAT MSG from Host, Device also transits to Active.Control and starts to send LIDL LSS in Fast Mode or set to EIDL in Low Power Mode.

### 8.3.4.2 2L-HD Write Transaction

Figure 8-10 illustrates a LINK state transition during duplex mode switching from FD to 2L-HD mode in case of data write.



**Figure 8-10 : Example LINK State Transition during Duplex Mode Switching (FD to 2L-HD Write)**

T1: Just after transmitting FCRDY MSG in Active.Control, LINK of Device (= DATA Receiver) transits its DLSM to Active.Recv.SwtHD and instructs the PHY to send STB.H for the duration of T\_EIDL\_ENTRY (= 4 SI) before entering to OFF state. After that, LINK of Device requests the PHY to start direction switch of D1 Lane from default Tx to non-default Rx. And PHY of Device performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, PLSM for D1.Rx (non-default Rx) of Device transits from OFF to STB immediately inside PHY to get ready for receiving valid symbols via switched D1 Lane.

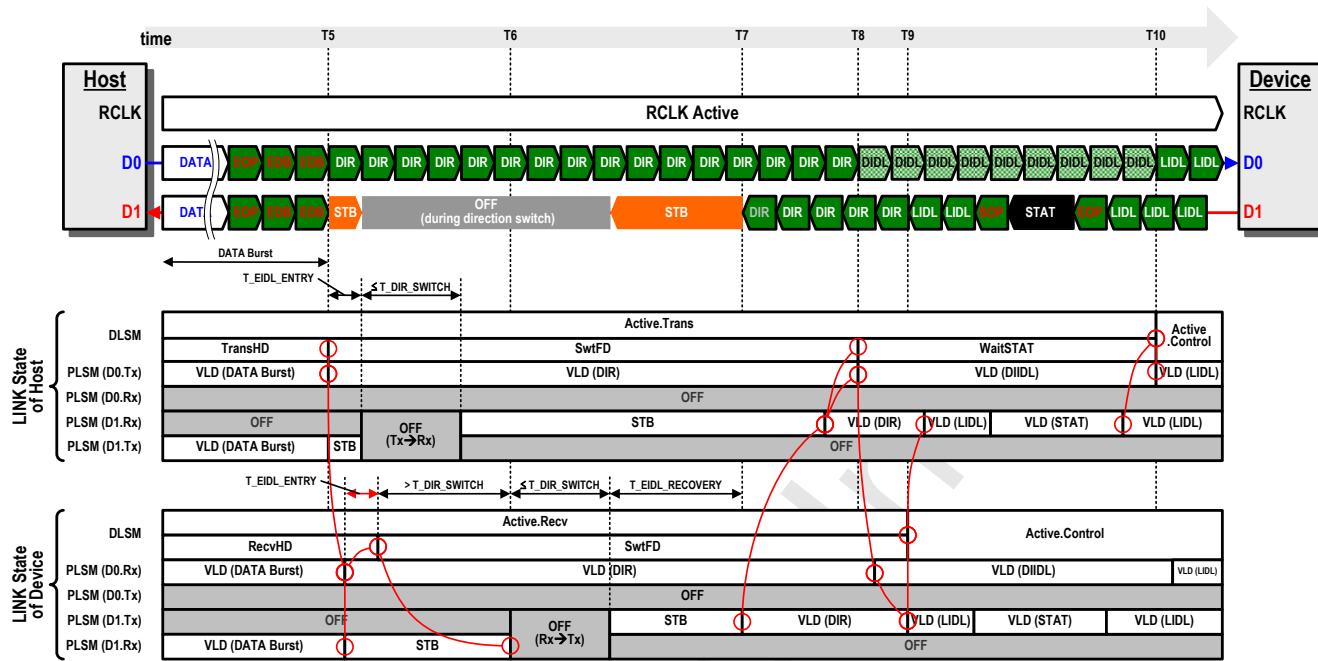
On the other hand, it takes LINK of Host (=DATA Initiator) a while to determine whether the receiving packet is FCRDY in accordance with Packet Receiving Flow described in Section 5.8. And after receiving FCRDY MSG, LINK of Host waits T\_EIDL\_ENTRY and transits its DLSM to Active.Trans.SwtHD. But prior to starting direction switch, LINK of Host waits for more than T\_DIR\_SWITCH to avoid a contention between both sides of Tx in D1 Lane.

T2: After the elapse of more than T\_DIR\_SWITCH in Active.Trans.SwtHD, LINK of Host starts to send DIR LSS via unswitched D0 Lane also requests the PHY to start direction switch of D1 Lane from default Rx to non-default Tx. And PHY of Host performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, LINK of Host transits its PLSM for D1.Tx (non-default Tx) from OFF to STB and instructs the PHY to send STB.L for the duration of T\_EIDL\_RECOVERY to get ready for transmitting valid symbols via switched D1 Lane.

T3: After the elapse of T\_EIDL\_RECOVERY in STB.L, LINK of Host transits to Active.Trans.TransHD and starts to send at least the predetermined number ( $N_{LSS\_DIR} * 8$ ) of DIR LSS for each Lane to acquire symbol lock. On the other hand, LINK of Device transits to Active.Recv.RecvHD after receiving DIR LSS via both Lanes.

T4: After transmitting  $N_{LSS\_DIR} * 8$  of DIR LSS, Host starts to send DATA Burst via both Lanes.

Figure 8-11 illustrates a LINK state transition during duplex mode switching from 2L-HD to FD mode in case of data write.



**Figure 8-11 : Example LINK State Transition during Duplex Mode Switching  
(2L-HD Write to FD)**

T5: Just after transmitting EDB LSS via both Lanes, LINK of Host (=DATA Initiator) transits its DLSM to Active.Trans.SwtFD and starts to send DIR LSS via unswitched D0 Lane and instructs the PHY to send STB.H via switched D1 Lane for the duration of T\_EIDL\_ENTRY before entering to OFF state. After that, LINK of Host requests the PHY to start direction switch of D1 Lane from non-default Tx to default Rx. And PHY of Host performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, PLSM for D1.Rx (default Rx) of Host transits from OFF to STB immediately inside PHY to get ready for receiving valid symbols via switched D1 Lane.

On the other hand, after receiving at least one of the EDB LSS via both Lanes, LINK of Device (= DATA Receiver) waits T\_EIDL\_ENTRY and transits its DLSM to Active.Recv.SwtFD. But prior to starting direction switch, LINK of Device waits for more than T\_DIR\_SWITCH to avoid a contention between both sides of Tx in D1 Lane.

T6: After the elapse of more than T\_DIR\_SWITCH in Active.Recv.SwtFD, LINK of Device also requests the PHY to start direction switch of D1 Lane from non-default Rx to default Tx. And PHY of Device performs the direction switch and notify its completion to the LINK within T\_DIR\_SWITCH (= 8 SI). After completing direction switch, LINK of Device transits its PLSM for D1.Tx (default Tx) from OFF to STB and instructs the PHY to send STB.L for the duration of T\_EIDL\_RECOVERY to get ready for transmitting valid symbols via switched D1 Lane.

T7: After the elapse of T\_EIDL\_RECOVERY in STB.L, LINK of Device starts to send DIR LSS to acquire symbol lock in switched D1 Lane.

T8: After receiving DIR LSS from Device via switched D1 Lane, LINK of Host transits to Active.Trans.WaitSTAT and starts to send DIDL LSS same as in FD mode.

T9: After receiving DIDL LSS from Host via unswitched D0 Lane, LINK of Device transits to Active.Control and starts to send STAT MSG same as in FD mode. Note that LINK of Device sets D1 Lane to EIDL before and after transmitting STAT MSG in case of Low Power Mode.

T10: After receiving STAT MSG from Device, Host also transits to Active.Control and starts to send LIDL LSS in Fast Mode or set to EIDL in Low Power Mode.

## 8.4 Transaction Layer Specification

### 8.4.1 Transaction Control and Management State Machine

This is common to FD mode. Refer to Section 6.2.13.

### 8.4.2 Error Handling

#### 8.4.2.1 Handling CRC Error

Same as in FD mode, if CRC error is detected in some DATA packet in FCU, the error is notified by the next MSG (STAT).

## 8.5 SD-TRAN Specification

### 8.5.1 Basic Transaction Rules in SD-TRAN

In the examples shown below, N\_FCU is supposed to be set to 2.

Figure 8-12 illustrates a sequence for Read DCMD with TMODE = 1100b (fixed transfer length, 2L-HD mode) in SD-TRAN.

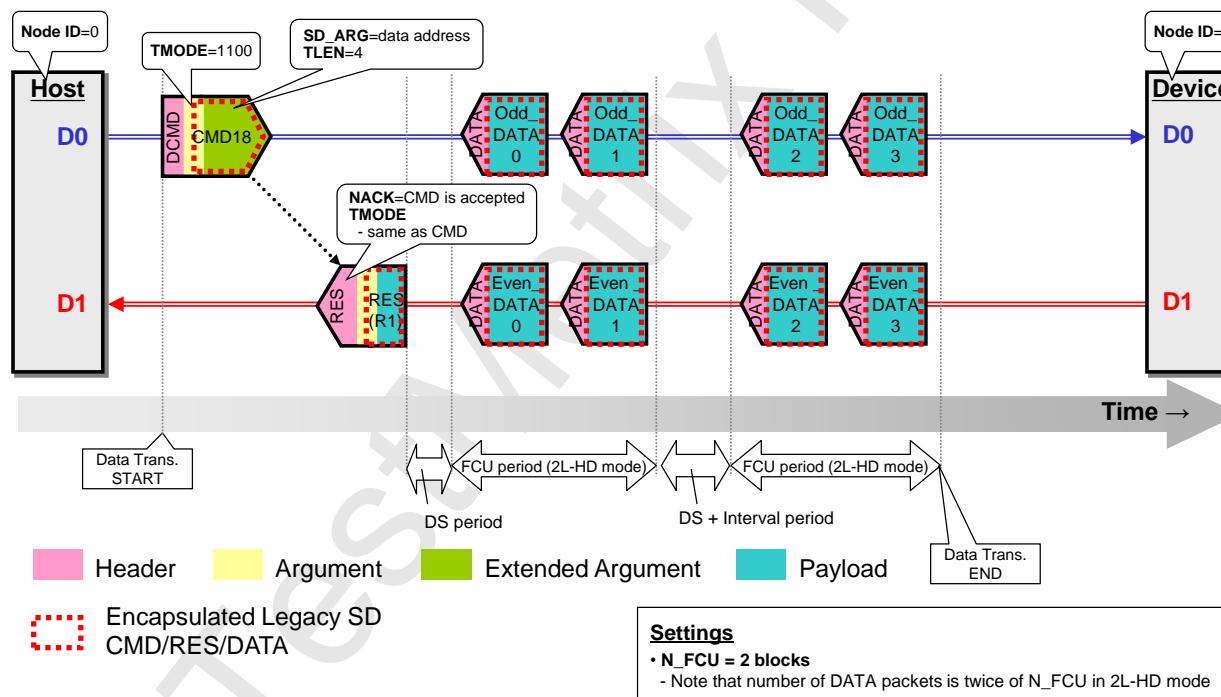


Figure 8-12 : Sequence of Read DCMD on SD-TRAN (CMD18, TMODE = 1100)

The detailed field values in Figure 8-12 are as follows;

#### [DCMD]

- Header (DCMD):
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host
- Argument (DCMD):
  - TMODE = 1100b (LM = 1, DM = 1)

- APP = 0 (regular command)
- CMD\_INDEX = 18 (command index in Legacy SD)
- **Extended Argument (DCMD):**
  - SD\_ARG = Argument of CMD18.
  - TLEN = 4 (total length of data transferred during a data transaction)

**[RES]**

- **Header (RES):**
  - NP = 0 (not native protocol)
  - Packet Type = RES
  - DID = 0 (the same value as SID in the corresponding DCMD)
  - SID = 1 (Node ID of Device)
  - TID = the same value as TID of the corresponding DCMD
- **Argument (RES):**
  - NACK = 0 (the corresponding CMD is accepted)
  - Other field is copied from DCMD
- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

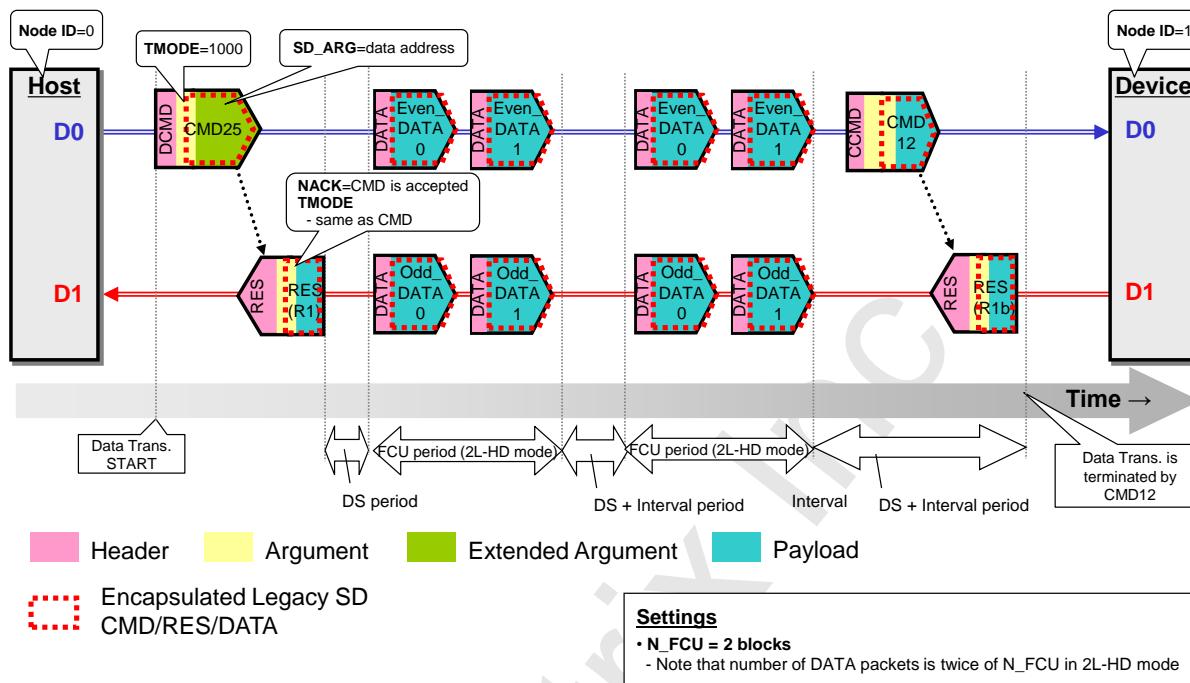
**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 0 (Node ID of Host)
  - SID = 1 (Node ID of source Device)
  - TID = the same value as TID of the corresponding DCMD
- **Payload (DATA):** requested read data by Host
  - The framing rules are described in Section 8.3.1.

Same in FD mode, CMD23 is ignored (Card responds R1 but does not operate).

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Figure 8-13 illustrates a sequence for Write DCMD with TMODE = 1000b (infinite transfer length, 2L-HD mode) in SD-TRAN.



**Figure 8-13 : Sequence of Write DCMD on SD-TRAN (CMD25, TMODE = 1000)**

The detailed field values in Figure 8-13 are as follows;

**[DCMD]**

- **Header (DCMD):**
  - NP = 0 (not native protocol)
  - Packet Type = DCMD
  - DID = 1 (Node ID of destination Device)
  - SID = 0 (Node ID of Host)
  - TID = Transaction ID decided by Host

**• Argument (DCMD):**

- TMODE = 1000b (LM = 0, DM = 1)
- APP = 0 (regular command)
- CMD\_INDEX = 25 (command index in Legacy SD)

**• Extended Argument (DCMD):**

- SD\_ARG = Argument of CMD25.

**[RES]**

**• Header (RES):**

- NP = 0 (not native protocol)
- Packet Type = RES
- DID = 0 (the same value as SID in the corresponding DCMD)
- SID = 1 (Node ID of Device)
- TID = the same value as TID of the corresponding DCMD

**• Argument (RES):**

- NACK = 0 (the corresponding CMD is accepted)
- Other field is copied from DCMD

- **Payload (RES):**
  - CONTENT = Response data of R1 (the length of Payload is 4 in this case)

**[DATA]**

- **Header (DATA):**
  - NP = 0 (not native protocol)
  - Packet Type = DATA
  - DID = 0 (Node ID of Host)
  - SID = 1 (Node ID of destination Device)
  - TID = the same value as TID of the corresponding DCMD
- **Payload (DATA):** transferred write data to Device
  - The framing rules are described in Section 8.3.1.

Same in FD mode, CMD12 can be issued only during interval period in order to terminate this transaction.

## 8.5.2 Error Handling

### 8.5.2.1 Handling CRC Error

Same as in FD mode, if CRC error is detected in some DATA packet in FCU, the error is notified by the next MSG (STAT).

### 8.5.2.2 Reaching Address to the End of User Data Area

If Host accesses the very last block in User Data Area, Device acts as described in Section 7.2.8.3 or Section 7.2.8.4.

## 8.6 Timing Rules

Both Host and Device shall keep the following timing rules related to direction switching.

Group	Abbreviation	Description	Value
Direction Switch	T_DIR_SWITCH	<p>Timing parameter of duration for direction switching.</p> <p>In case of switching from Tx to Rx, port shall complete it within the time period of T_DIR_SWITCH after transmitting STB.</p> <p>In case of switching from Rx to Tx, on the other hand, port shall wait for the time period more than T_DIR_SWITCH after receiving STB, then complete direction switching within the time period within T_DIR_SWITCH.</p>	8 SI

Table 8-1 : Timing Parameters Related to Direction Switch

## 9. Additional Lanes Support (optional)

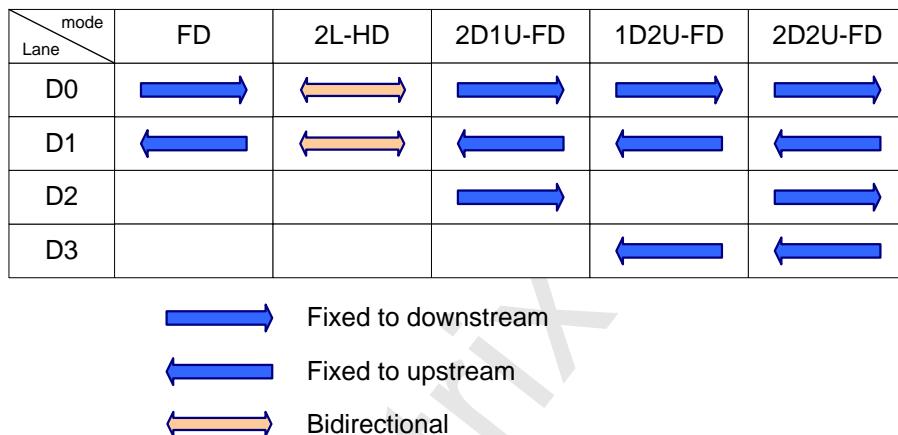
### 9.1 Overview

Lower operating frequency generally provides applicability to a variety of Hosts due to easy implementation of whole system. Adding more Lanes can give a good balance between performance and complexity.

The basic idea is to extend the concept of FD mode and 2L-HD mode for DATA packets. Host and Device can have one additional Lane (D2 or D3) or two additional Lanes (D2, D3), both are optional.

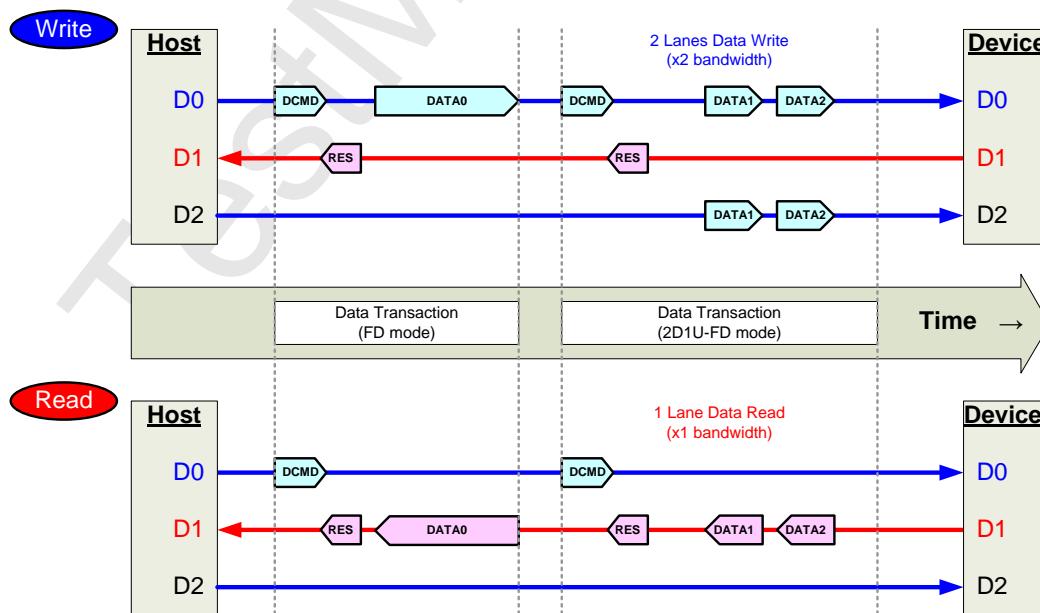
Device reports its capabilities in Generic Capabilities Register.

Figure 9-1 shows the entire possible Lane configuration.



**Figure 9-1 : Possible Lanes Configurations in FD / 2L-HD Mode**

Figure 9-2 shows a case of 2D1U-FD mode, which is expected write performance boost. On the other hand, Figure 9-3 shows a case of 1D2U-FD mode, which is expected double read performance boost.



**Figure 9-2 : Overview of 2D1U-FD Mode – Write Boost**

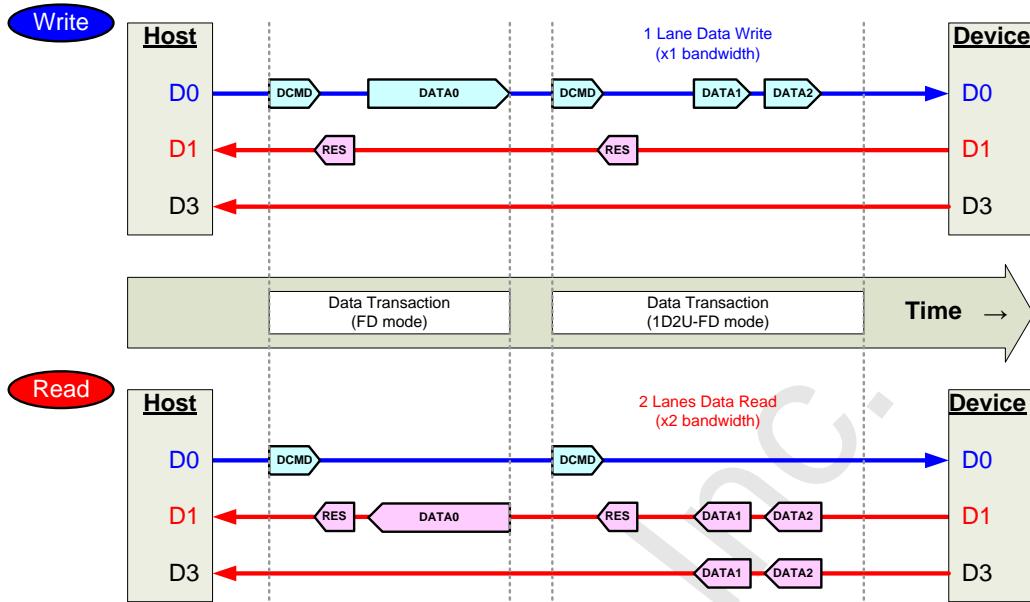
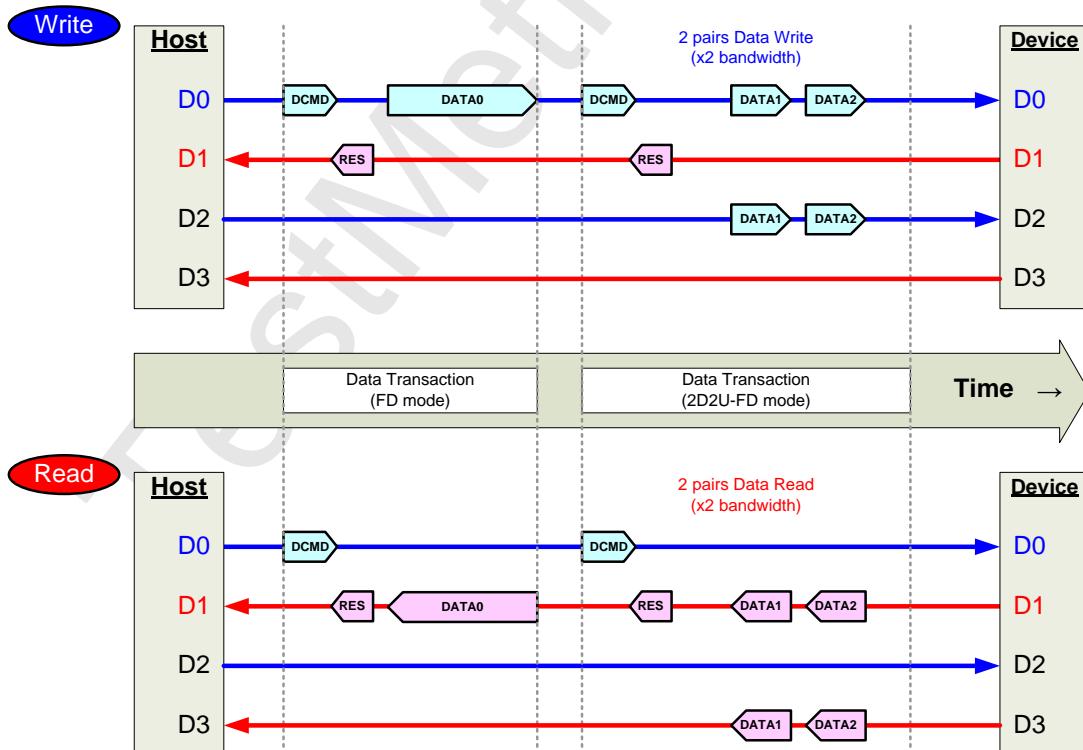
**Figure 9-3 : Overview of 1D2U-FD Mode – Read Boost**

Figure 9-4 shows the case of 2D2U-FD mode: D2 is downstream and D3 is upstream – x2 read/write performance boost.

**Figure 9-4 : Overview of 2D2U-FD Mode**

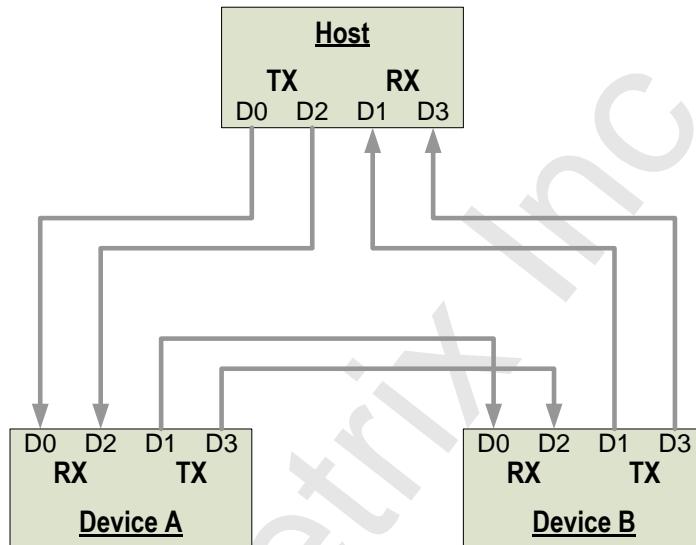
### 9.1.1 Capabilities and Settings

The capabilities of a Device regarding Lanes support is described in Table 6-7 (Device-specific Number of Lanes and Functionality). Device can indicate more than one option.

The setting is determined by Table 6-10 (Number of Lanes and Functionality)

### 9.1.2 Additional Lanes and Multi-device Topologies

Additional Lanes can be used also in Multi-device topologies. Figure 9-5 shows Ring topology making use of additional two Lanes in FD mode for achieving x2 performance boost.



**Figure 9-5 : Usage of 4 Lanes in Ring Topology**

In UHS-II Addendum Version 1.00, Ring connection is limited to use only in case of FD mode by 2 Lanes and 2D2U-FD mode by 4 Lanes (refer to Figure 9-5). 2D1U-FD mode or 1D2U-FD mode can be available in P2P or HUB connections.

## 9.2 PHY Layer Specification

### 9.2.1 PHY Specification and Direction Switching

The added Lanes shall use the same PHY as used for D0 and D1 Lanes complying with Chapter 4.

Note that specifications of D2 and D3 shall conform to those of D0 and D1 except the followings.

In order to reduce the number of Amplitude Detectors, the Amplitude Detector output of D0.Rx can be used also for D2.Rx. And similarly, the Amplitude Detector output of D1.Rx can be used also for D3.Rx.

### 9.2.2 Default Behavior

The state of the additional Lanes before enabled is defined in PHY specification – "Disconnected state". The Rx and Tx are in power off / Dormant states.

## 9.3 Link Layer Specification

This section shows the case of 2D2U-FD mode, but it is also applied to both 2D1U-FD mode and 1D2U-FD mode.

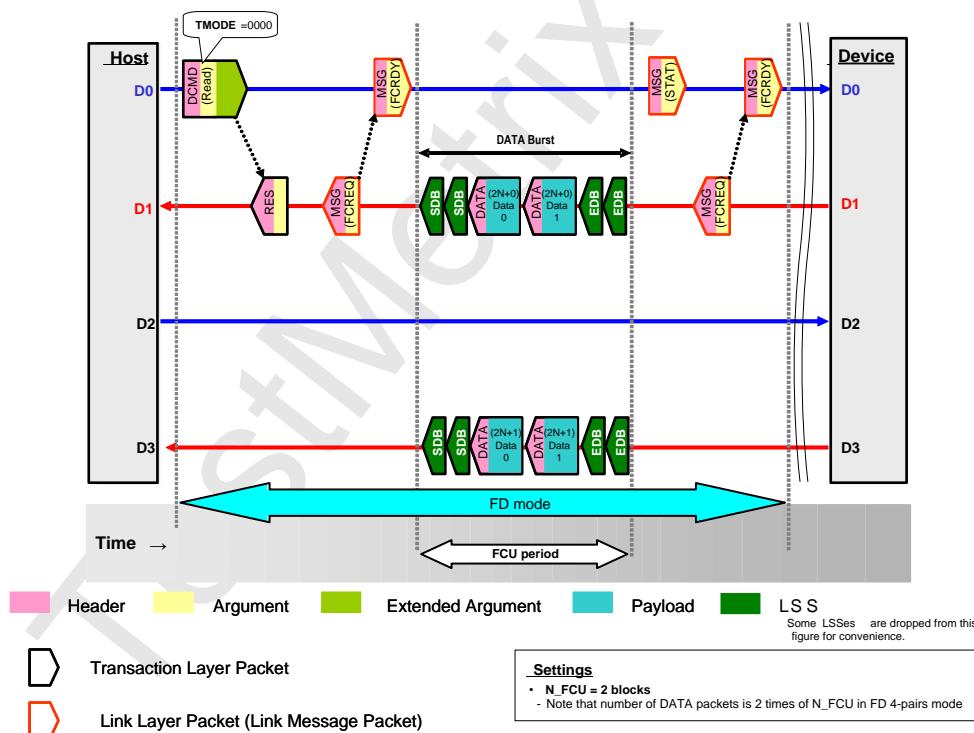
When the Additional Lanes Support is available, synchronization among plural Lanes with same direction should be considered in state transitions, if necessary.

### 9.3.1 Framing Rules

The Framing rules of DATA packet are similar to those of 2L-HD mode described in Section 8.3.1. Differences between them are as follows.

- Even Framed DATA Packet is transmitted through D0 or D1, and Odd Framed DATA Packet thought D2 and D3.
- Byte Mode is also available. Its framing rule is defined by substituting from Block Length to TLEN in Section 8.3.1.

Figure 9-6 shows read operation in 2D2U-FD mode. The command and responses are sent and received by D0 and D1. During FCU Period, even bytes are carried on D1 and odd bytes are carried on D3.



**Figure 9-6 : Read Operation in 2D2U-FD Mode**

Figure 9-7 shows write operation in 2D2U-FD mode. Again, even bytes are carried on D0 and odd bytes are carried on D2.

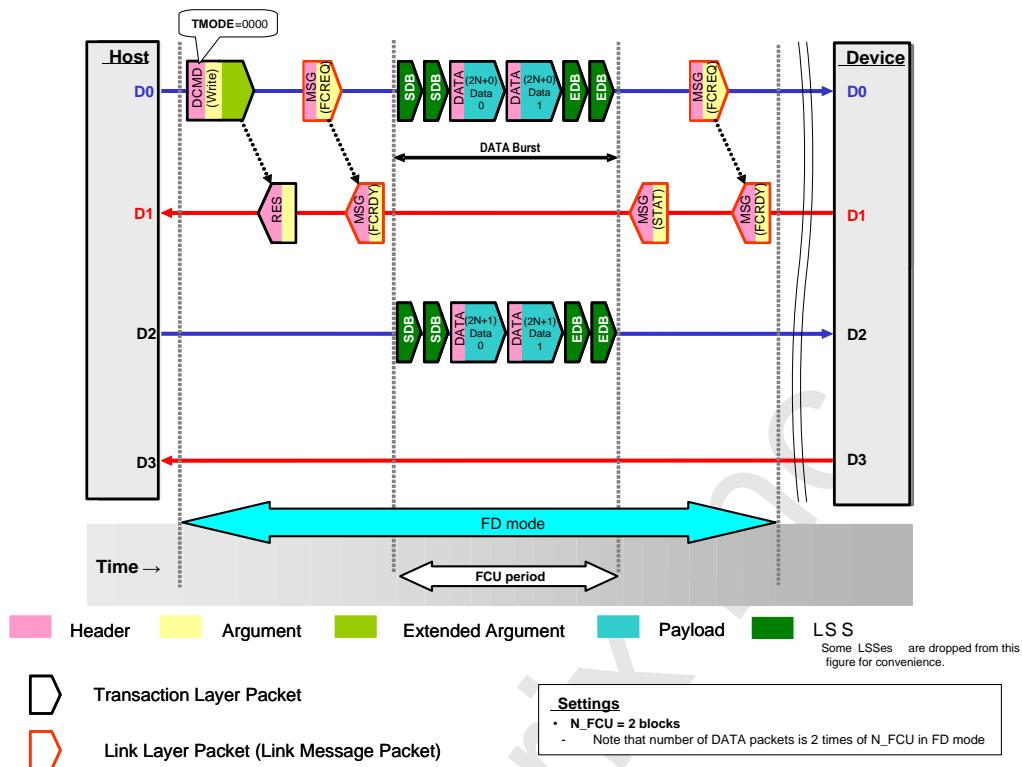


Figure 9-7 : Write Operation in 2D2U-FD Mode

### 9.3.2 Lane Direction for 2D2U-FD Mode

Figure 9-8 shows Lane direction for 2D2U-FD mode between Host and Device.

Host sets D0 and D2 Lanes to Tx and D1 and D3 Lane to Rx, on the other hand, Device sets D0 and D2 Lanes to Rx and D1 and D3 Lanes to Tx as default.

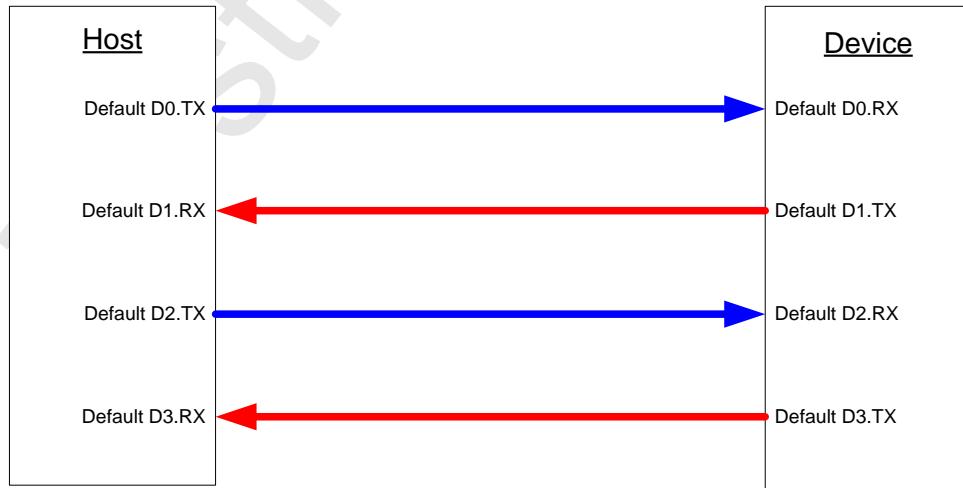
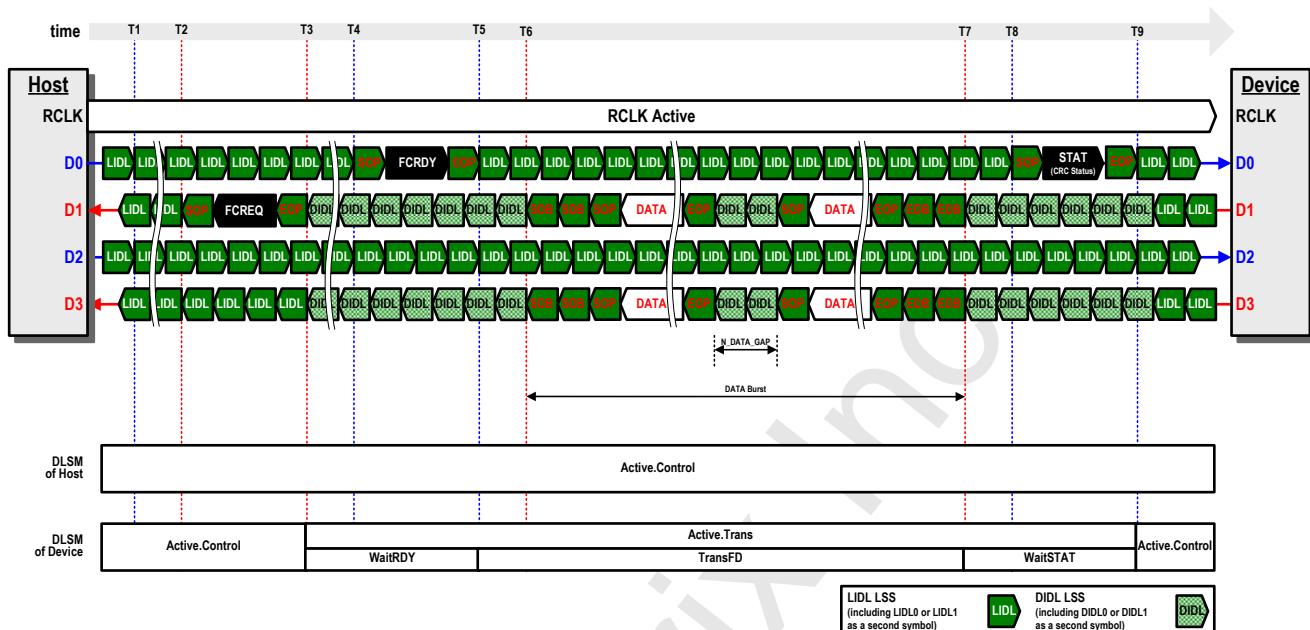


Figure 9-8 : Lane Direction for 2D2U-FD Mode

D2.Rx in Device can use the Amplitude Detector of D0.Rx. Similarly, the D3.Rx in Host can use the Amplitude Detector of D1.Rx.

### 9.3.3 LINK State Transition for 2D2U-FD Mode during Data Read – Fast Mode

Figure 9-9 illustrates LINK state transition for 2D2U-FD mode during data read in Fast Mode.



**Figure 9-9 : LINK State Transition for 2D2U-FD mode during Data Read – Fast Mode**

T1: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state. So, all Lanes are filled with a series of LIDL LSS including LIDL0 or LIDL1 symbol as a second symbol in random order.

T2: When Tx Buffer is ready for transmitting DATA Burst (DATA \* N\_FCU \* 2), LINK of Device (= DATA Initiator) issues FCREQ (Flow Control Request) MSG directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY.

T3: Device starts to transmit DIDL LSSes including DIDL0 or DIDL1 as a second symbol in random order on D1 and D3

T4: When Rx Buffer is ready for receiving DATA Burst, LINK of Host (= DATA Receiver) issues FCRDY (Flow Control Ready) MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Host, LINK of Device transits to Active.Trans.TransFD state.

T6: LINK of Device starts to send two SDB (Start of DATA Burst) LSSes in Active.Trans.TransFD state.

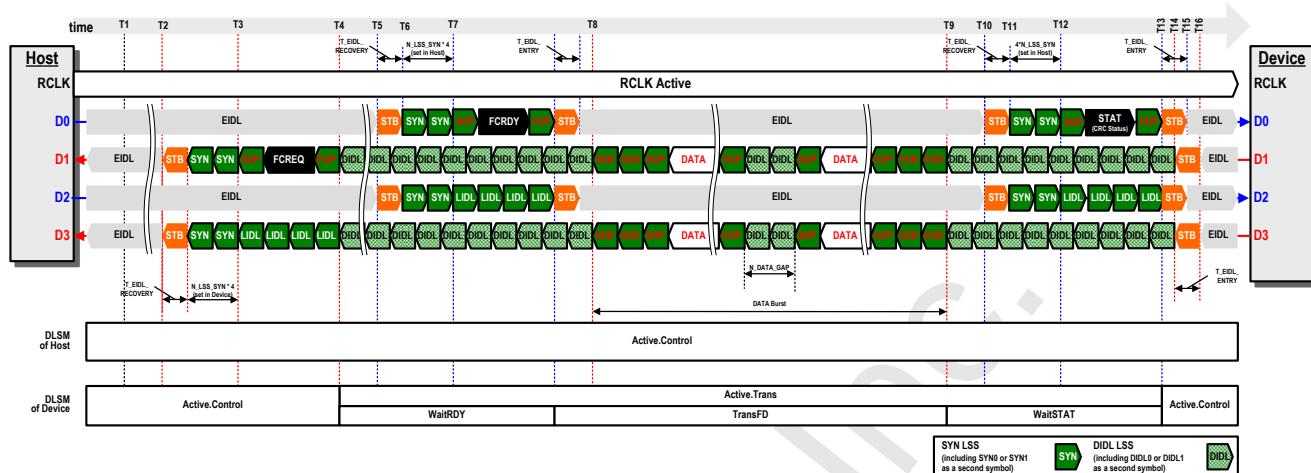
T7: After sending DATA packets, LINK of Device sends two EDB (End of DATA Burst) LSSes and transits to Active.Trans.WaitSTAT state.

T8: After receiving at least one EDB, LINK of Host sends STAT MSG. And after receiving STAT from Host, LINK of Device goes back to Active.Control state and starts to transmit LIDL LSS.

Note: Fast Mode can be selected in CFG\_REG ("Power Control Mode in Active.Control State") during Configuration and reflected in Active state to minimize the latency during data transfer.

### 9.3.4 LINK State Transition for 2D2U-FD Mode during Data Read – Low Power Mode

Figure 9-10 illustrates LINK state transition for 2D2U-FD mode during data read in Low Power Mode.



**Figure 9-10 : LINK State Transition for 2D2U-FD Mode during Data Read – Low Power Mode**

T1: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state under Low Power Mode condition. So, all Lanes are filled with EIDL.

T2: Before sending the FCREQ message, Device changes D1 and D3 from EIDL to STB.L. The Amplitude Detector in Host D1.Rx detects the transition from EIDL to STB.L and notifies the PLSM of D1.Rx and D3.Rx. After STB.L, Device is sending SYN LSS to synchronize the D1.Rx and D3.Rx of Host.

T3: When Tx Buffer is ready for transmitting DATA Burst ( $DATA * N\_FCU * 2$ ), LINK of Device issues FCREQ MSG directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY. Device sends the FCREQ message on D1 and LIDL on D3.

T4: After exiting from Active.Control state, LINK of Device starts to transmit DIDL LSSes including DIDL0 or DIDL1 symbol as a second symbol in random order regardless of the setting of "Power Control Mode in Active.Control State" in CFG\_REG.

T5: When Rx Buffer is ready for receiving DATA Burst, LINK of Host issues FCRDY MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Host, LINK of Device transits to Active.Trans.TransFD state. Host starts with sending STB.L followed by SYN LSS on D0 and D2.

T7: Host is sending the FCRDY message on D0 and LIDL LSS on D2.

T8: LINK of Device starts to send two SDB LSSes in Active.Trans.TransFD state. TRAN of Device starts to send Flow Control Unit (= N\_FCU) of DATA packets through LINK and PHY.

T9: After sending DATA packets, LINK of Device sends two EDB LSSes and transits to Active.Trans.WaitSTAT state.

T10: After receiving at least one EDB, LINK of Host is preparing to send STAT MSG. Host is sending STB.L and SYN LSS on D0 and on D2 Lanes.

T11: Host sends SYN LSS on D0 and D2.

T12: Host sends the STAT message on D0 and LIDL LSS on D2.

T13: Host sends STB.H on D0 and D2.

T14: Device sends STB.H on D1 and D3

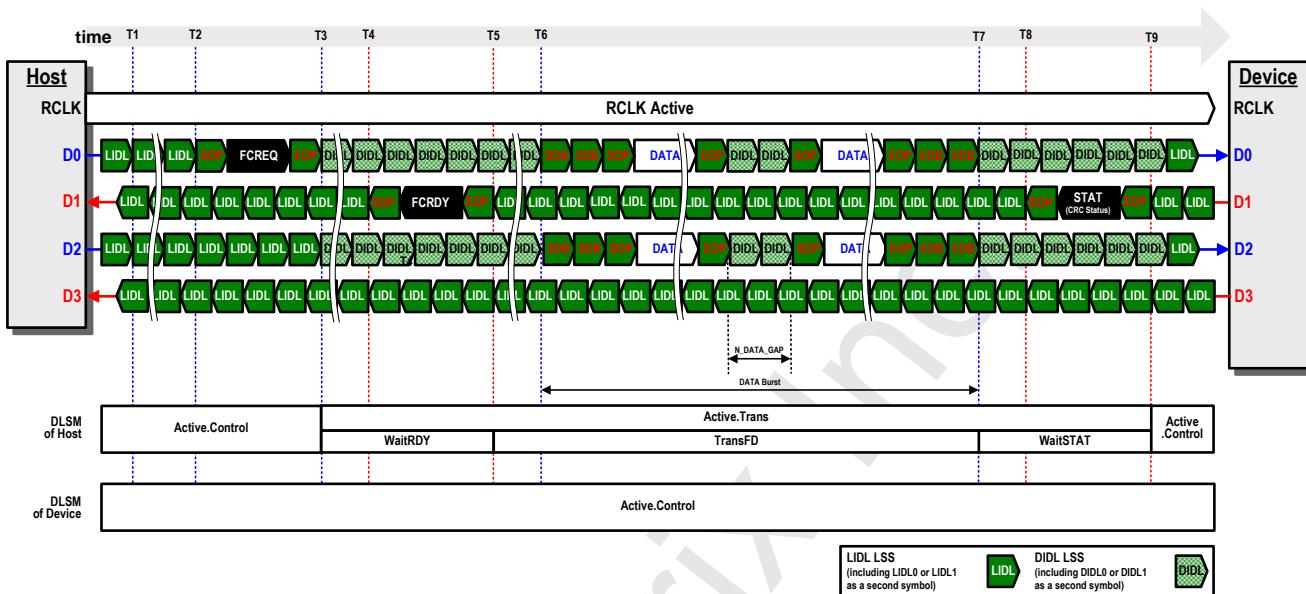
T15: Host sends EIDL on D0 and D2.

T16: Device sends EIDL on D1 and D3

Note: Low Power Mode can be selected in CFG\_REG ("Power Control Mode in Active.Control State") during Configuration and reflected in Active state to minimize the power consumption during data transfer.

### 9.3.5 LINK State Transition for 2D2U-FD Mode during Data Write – Fast Mode

Figure 9-11 illustrates LINK state transition for 2D2U-FD mode during data write in Fast Mode.



**Figure 9-11 : LINK State Transition for 2D2U-FD Mode during Data Write – Fast Mode**

T1: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state. So, both Lanes are filled with a series of LIDL LSS including LIDL0 or LIDL1 symbol as a second symbol in random order.

T2: When Tx Buffer is ready for transmitting DATA Burst (DATA \* N\_FCU \* 2), LINK of Host issues FCREQ MSG on D0 directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY. In same time, Host sends LIDL0 or LIDL1 randomly on D2.

T3: Host starts to transmit DIDL LSSes including DIDL0 or DIDL1 in random order on both D0 and D2.

T4: When Rx Buffer is ready for receiving DATA Burst, LINK of Device issues FCRDY MSG on D1 Lane directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Device, LINK of Host transits to Active.Trans.TransFD state. In same time, Device sends LIDL0 or LIDL1 on D3.

T6: LINK of Host starts to send two SDB (Start of DATA Burst) LSSes in Active.Trans.TransFD state and then Host starts to send N\_FCU \* 2 of DATA packets through LINK and PHY.

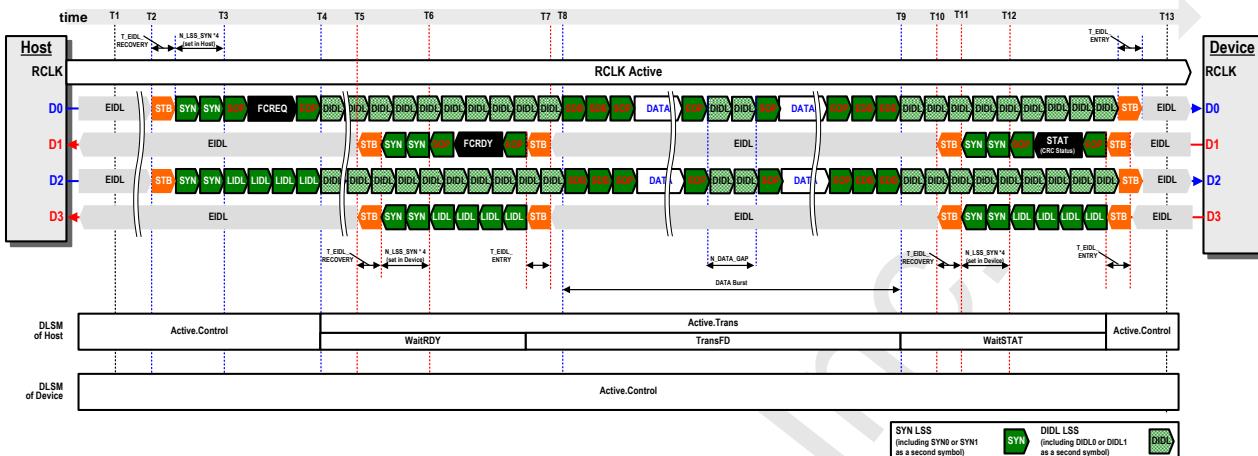
T7: After sending DATA packets, LINK of Host sends two EDB (End of DATA Burst) LSSes and transits to Active.Trans.WaitSTAT state.

T8: After receiving at least one EDB, LINK of Device sends STAT (Status) MSG.

T9: Device is sending LIDL LSS.

### 9.3.6 LINK State Transition for 2D2U-FD Mode during Data Write – Low Power Mode

Figure 9-12 illustrates LINK state transition for 2D2U-FD mode during data read in Low Power Mode.



**Figure 9-12 : LINK State Transition for 2D2U-FD Mode during Data Write – Low Power Mode**

T1: Before starting FC handshake (FCREQ and FCRDY), both sides of LINK stay in Active.Control state under Low Power Mode condition. All Lanes are filled with EIDL.

T2: Host is getting ready to transmit FCREQ by sending STB.L on D0 and D2. On Device side the STB.L is detected by the Amplitude Detector of D0 and the PLSM of D2 is notified accordingly. After STB, Host sends SYN LSS on D0 and D2 Lanes.

T3: When Tx Buffer is ready for transmitting DATA Burst ( $\text{DATA} * \text{N_FCU} * 2$ ), LINK of Host issues FCREQ MSG directed by TRAN and transits its DLSM from Active.Control to Active.Trans.WaitRDY. Host sends FCREQ on D0 Lane and LIDL on D2 Lane.

T4: After exiting from Active.Control state, LINK of Host starts to transmit DIDL LSSes including DIDL0 or DIDL1 as a second symbol in random order regardless of the setting of "Power Control Mode in Active.Control State" in CFG\_REG.

T5: Device is preparing to send FCRDY by transmitting STB and then SYN LSS on D1. On D3 Lane, Device transmits STB only.

T6: When Rx Buffer is ready for receiving DATA Burst, LINK of Device issues FCRDY MSG directed by TRAN and stays in Active.Control state. And after receiving FCRDY from Device, LINK of Host transits to Active.Trans.TransFD state. Device sends the FCRDY message on D1 Lane and LIDL on D3 Lane.

T7: LINK of Device is going back to EIDL.

T8: LINK of Host starts to send two SDB LSSes in Active.Trans.TransFD state. TRAN of Host starts to send  $\text{N_FCU} * 2$  of DATA packets through LINK and PHY.

T9: After sending DATA packets, LINK of Host sends two EDB LSSes and transits to Active.Trans.WaitSTAT state.

T10: LINK of Device is getting prepared to send STAT message by transmitting STB on D1 and D3 Lanes.

T11: Device sends SYN LSS on D1 and D3 Lanes.

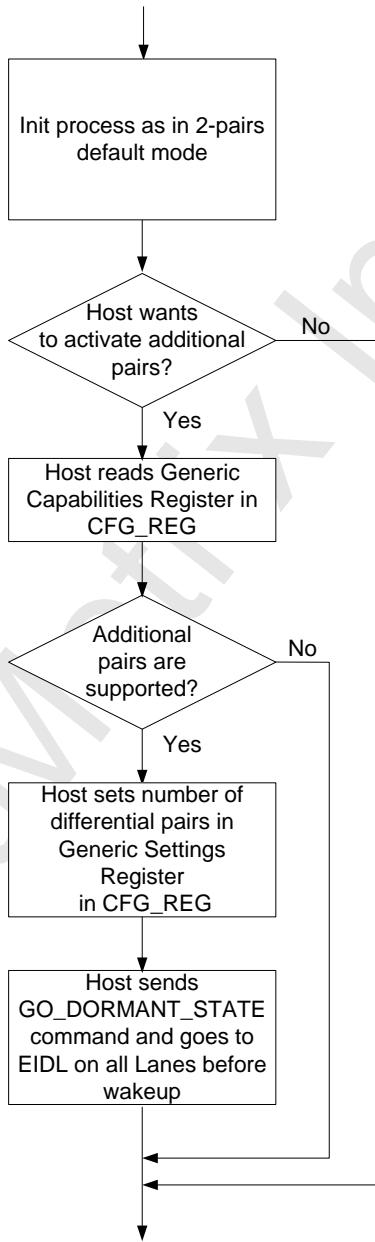
T12: LINK of Device sends STAT MSG on D1 Lane and LIDL on D3 Lane.

T13: All Lanes are back to EIDL

## 9.4 Transaction Layer Specification

### 9.4.1 Initialization

Host shall always be connected to D0 and D1 signals. The initialization process shall be carried through D0 and D1 as described in Chapters 6 and 7. In order to use D2 or D3, an additional stage is required as described in Figure 9-13.



**Figure 9-13 : Flow Chart of Activating Additional Lanes**

Figure 9-14 shows the timing diagram of activating the additional Lanes and entry / exit of Dormant state. Note that it is also applied to both 2D1U-FD mode and 1D2U-FD mode.

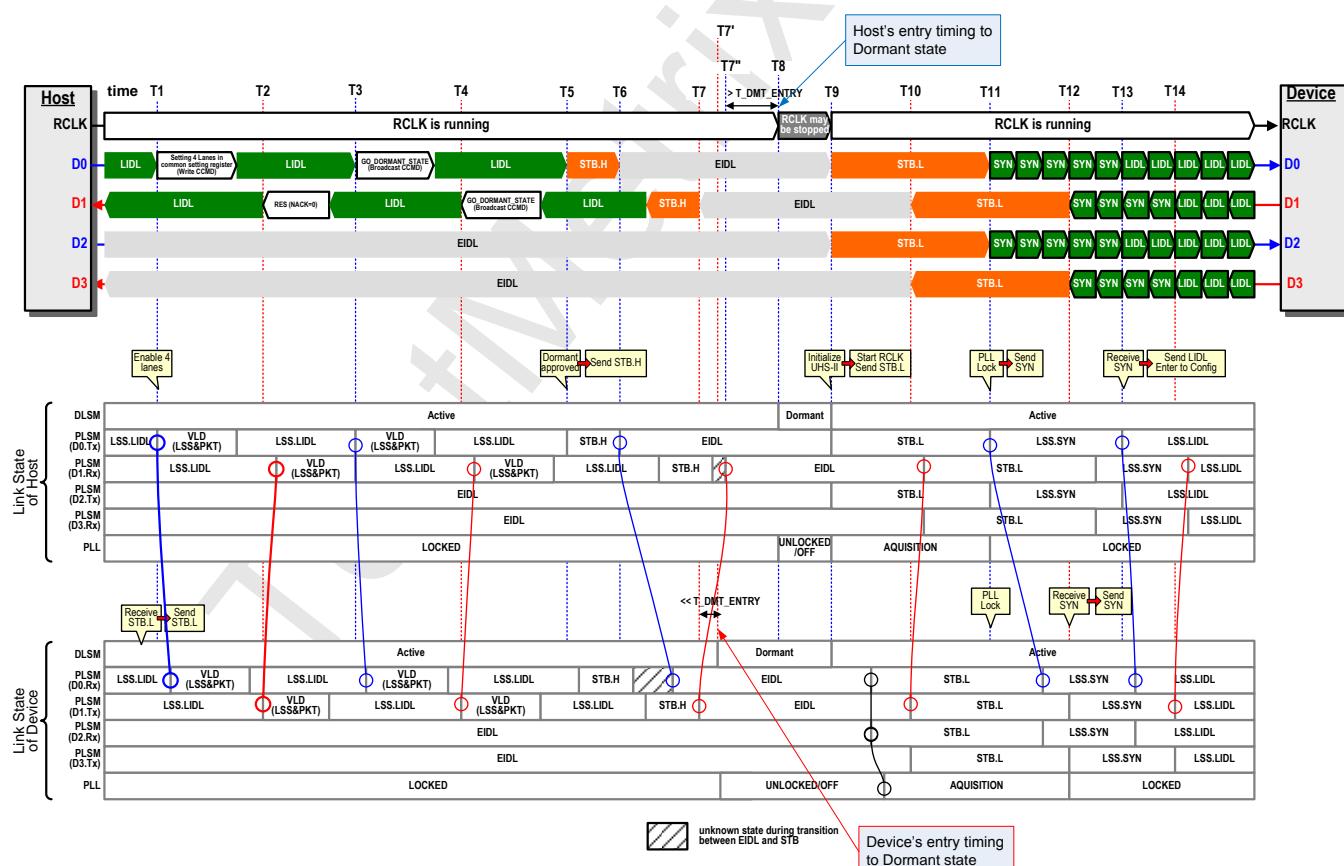
T1: Host sets the desired Lanes configuration in Generic Settings Register by sending write CCMD.

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- T2: Device sends a response (NACK = 0).  
 T3: Host sends the GO\_DORMANT\_STATE command.  
 T4: Device sends back the GO\_DORMANT\_STATE command.  
 T5: Host starts dormant sequence by sending STB.H.  
 T6: Host sends EIDL.  
 T7: Device sends EIDL. Then it starts preparing for entry to Dormant State.  
 T7': Device transits to Dormant State within the elapse of sufficiently less than T\_DMT\_ENTRY from T7.  
 T7'': PLSM of D1.Rx (Host) is EIDL.  
 T8: Host transits to Dormant State after the elapse of more than T\_DMT\_ENTRY from T7'', and may stop RCLK.

Between T1 and T9, D2 and D3 are in EIDL (before activation).

- T9: Host activates its RCLK and sends STB.L on D0 and D2. The Amplitude Detector in D0.Rx of Device detects the STB.L and notifies the PLSM of D0.Rx and D2.Rx.  
 T10: Device sends STB.L on D1 and D3.  
 T11: Host sends SYN LSS on D0 and D2 in order to synchronize Device.  
 T12: The PLL of Device is synchronized and Device can send SYN LSS to Host.  
 T13: Host sends LIDL (Fast Mode).  
 T14: Device sends LIDL (Fast Mode).



**Figure 9-14 : Activating Additional Lanes through GO\_DORMANT\_STATE Command**

### 9.4.2 Transaction Control and Management State Machine

This is common to FD mode. Refer to Section 6.2.13.

### 9.4.3 Error Handling

#### 9.4.3.1 Handling CRC Error

Same as in FD mode, if CRC error is detected in some DATA packet in FCU, the error is notified by the next MSG (STAT).

## 9.5 SD-TRAN Specification

### 9.5.1 Error Handling

#### 9.5.1.1 Handling CRC Error

Same as in FD mode, if CRC error is detected in some DATA packet in FCU, the error is notified by the next MSG (STAT).

#### 9.5.1.2 Reaching Address to the End of User Data Area

If Host accesses the very last block in User Data Area, Device acts as described in Section 7.2.8.3 or Section 7.2.8.4.

## Appendix A (Normative) : Reference

### A.1 Related Documentation

- SD Specifications Part 1 Physical Layer Specification Version 4.00 or later
- SD Specifications Part 1 Standard Size SD Card Mechanical Addendum Version 4.00 or later
- SD Specifications Part 1 microSD Mechanical Addendum Version 4.00 or later
- SD Specifications Part 2 File System Specification Version 3.00 or later
- ANSI X3.230-1994, clause 11 (and also IEEE 802.3z, 36.2.4)

## Appendix B (Normative) : Special Terms

### B.1 Terminology

2L-HD mode	Half Duplex with 2 Lanes mode
8b/10b	One of line coding that maps 8-bit symbols to 10-bit symbols to achieve DC-balance and bounded disparity.
Block	Data unit to be transmitted by one DATA packet
Block Length	Data length for one Block
Boot Code	Code including initial set of operations using bootstrapping process
Boot Code Loading	Transmitting Boot Code from Boot Device to Host immediately after PHY Initialization
Boot Device	Device that stores Boot Code
broadcast	Operating to all connecting nodes (Devices)
BUSY period	Period that Host cannot access to backend (flash memory for SD-memory)
Card	SD memory card
CM	Common Mode
CM-TRAN	Common transaction layer in UHS-II
Command Time Slot	Time period that FULL_RESET, TRANS_ABORT, and arbitrary read CCMD are allowed to be issued on the way of data transmission
Configuration	An arrangement of functional unit or parameters according to capabilities of Host and Devices
DATA Burst	A unit that consists of one or more DATA packets and related LSS and can be sent in one flow control unit
DATA Burst Streaming	Bypassing DATA Bursts to the next Node without passing through LINK.
De-embedding	Removing the effect of unwanted component from the measurement result
Device	The electrical equipment which transmit/receive data to/from Host and communication is controlled by Host. Device includes Card and Embedded Device
Device Initialization	Process to make Device enable its all functions
downstream	Transmission from Host to Device
Embedded Device	Non-removable SD Device without form factor
Enumeration	Assigning Node ID for each connecting Device
FD mode	Full Duplex mode
Flow Control	Process of managing the data transmission to prevent data overflow or underflow.
Flow Control Unit	A unit of period for data transmission accompanied by FCREQ-FCRDY handshake. Also refer to DATA Burst.
Fractional DATA Burst	A DATA Burst which consists of Framed DATA packet less than N_FCU
Framing	Prefixing SOP and postfixing EOP for packets, and prefixing SDB and postfixing EDB for DATA Burst.
Full Duplex mode	Communication mode that the direction of two Lanes is opposite each other.
Half Duplex with 2 Lanes mode	Communication mode that the direction of two Lanes is same. It is optional in UHS-II.
Host	The electrical equipment which transmit/receive data to/from Device (e. g. SD Card) and control the communication. Only Host can issue commands.
Hub	Device that allows many Devices to be connected to a single port on a Host
I/F power cycle	Act of turning whole UHS-II interface off and then on again by I/F power

	supply
I/F power supply	Power supplement for UHS-II interface (e.g. VDD2 for SD-memory)
Inter skew	The skew between differential Lanes transmitting in same direction.
Intra skew	The skew between Positive Line signal and Negative Line signal of one differential pair.
Jitter	Jitter is undesirable time variation of a periodic signal, which is caused by ISI and some fluctuations such as voltage supply and temperature etc.
Lane	Each set which consists of Tx Port, transmission Line and Rx Port. For example, D0 consists of D0.Tx in Host, D0 Line and D0.Rx in Device.
Legacy SD	SD card not supporting UHS-II interface
Line	Component for connecting a Tx (Transmitter) Port and an Rx (Receiver) Port and realizing differential transmission
LINK	The interface layer above PHY Layer. LINK is in charge of controlling data flow and making management for LINK and PHY.
Loopback	Method or procedure of routing electronic signals from their originating facility quickly back to the same source entity without intentional processing or modification
Node	Host or Device
Node ID	Number to identify Nodes
Packet bypassing	Sending packets to the next Node without any operations in TRAN
Parallel termination	Termination connecting positive and negative Lines of a differential Lane
PHY	Physical Interface Layer
Return loss	Reflection ratio of signal power in a transmission Line
Rx	Receiver Circuit, which is responsible for outputting differential signal
SD-TRAN	One of application specific layers in UHS-II. It bridges CM-TRAN and Legacy SD applications or drivers.
Serializer/Deserializer	A pair of functional blocks to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction.
skew	Time difference of transmission delay between two transmission Lines
TRAN	The interface layer above LINK. It is divided into CM-TRAN and an application specific TRAN.
transaction	A unit of communication that takes place by one command
Tx	Transmitter circuit, which is responsible for outputting differential signal
UHS-II Card	SD card supporting UHS-II Interface
UHS-II native	UHS-II without (or not considering) application specific layers
upstream	Transmission from Device to Host
Wakeup	PHY initialization state
X5R,X7R	Symbol for dielectric material of capacitors

## B.2 Abbreviations

BSYN	Synchronization for Boot Code Loading
CCMD	Control Command
CDCP	Candidate DCP
CF	Completion Flag of Device Initialization
CFG_REG	Configuration Register

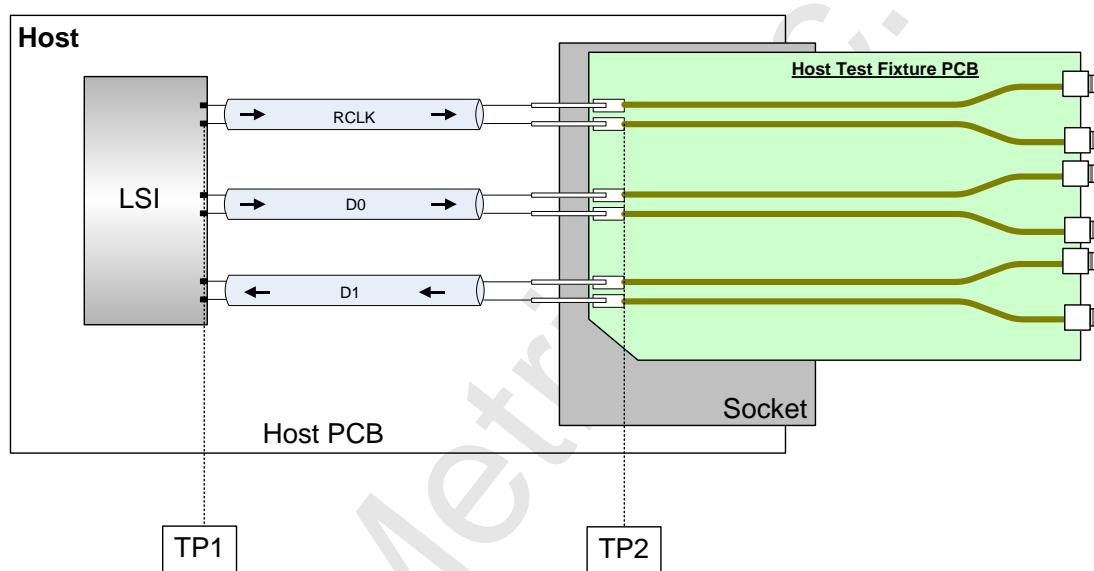
CMD	Command
CMD_REG	Command Register
COM	Comma Symbol
CPR	Control Packet Reception
CRC	Cyclic Redundancy Check
CTS	Command Time Slot
DAM	Data Access Mode
DAP	Device Allocated Power
DATA	DATA packet
DBR	DATA Burst Reception
DCMD	Data Command
DCP	Device Consumed Power
DFL	Direction Fixed Lane
DID	Destination ID
DidL	Data Idle
DIF-H	Differential High state
DIF-L	Differential Low state
DIF-PD	Pull-down state
DIF-Z	High-Z (high impedance)
DIR	Direction
D <sub>J</sub>	Deterministic jitter
DLSM	Data Link State Machine
DM	Duplex Mode
DSL	Direction Switched Lane
EDB	End of DATA Burst
EIDL	Electrical Idle
EMI	Electromagnetic interference
EOP	End Of Packet
ESD	Electrostatic Discharge
FC	Flow Control
FCRDY	Flow Control Ready
FCREQ	Flow Control Request
FCU	Flow Control Unit
GAP	Group Allocated Power
GD	Group Descriptor
GN	Group Number
INT	Interrupt
INT_REG	Interrupt Register
IP	Intellectual Property
ISI	Inter Symbol Interference
LFSR	Linear Feedback Shift Register
LIDL	Logical Idle
LM	Length Mode
LPM	Low Power Mode
LPS	Low Power State
lsb	Least Significant Bit
LSB	Least Significant Byte

LSI	Large Scale Integration
LSS	Link Symbol Set
MAX_BLKLEN	Maximum payload length of one block
MLCC	Multi-Layer ceramic capacitor
msb	Most Significant Bit
MSB	Most Significant Byte
MSG	Message
NACK	Negative-acknowledge
N_FCU	Number of blocks in a FCU
P2P	Point to Point
PAD	Padding Symbol
PLEN	Payload Length
PLL	Phase-Locked Loop
PLSM	Physical Lane State Machine
PM	Power Management
RCLK	Referential Clock
RES	Response
R <sub>J</sub>	Random jitter
SDB	Start of DATA Burst
SI	Symbol Interval, equal to 10 * UI
SID	Source ID
SOP	Start Of Packet
SSC	Spread Spectrum Clocking
STAT	Status Message
STB	Standby
ST_REG	Status Register
SYN	Synchronization
TBD	To Be Determined
TBSM	Transaction Buffer-management State Machine
TDR	Time Domain Reflection
TID	Transaction ID
T <sub>J</sub>	Total jitter
TLEN	Transfer Length
TLP	Transaction Layer Packet
TLUM	TLEN Unit Mode
TPSM	Transaction Processing State Machine
TSSM	Transaction Scheduling State Machine
UI	Unit Interval or data bit time interval
VLD	Valid State
VU_REG	Vendor Unique Register

## Appendix C (Normative) : Test Condition of Measuring Output Signals

### C.1 Test Condition for Host Output Signal at TP2

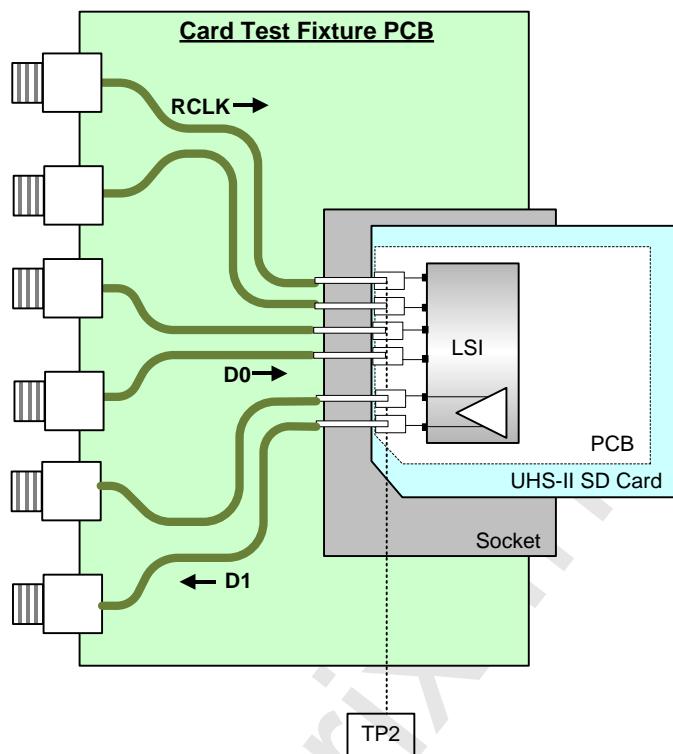
By using Host test fixture, illustrated in Figure C- 1, a measurement for output waveform of Host transceiver is performed. The Test fixture is designed to be as ideal as possible (100ohm differential impedance and 250hm common-mode impedance as the target). A detailed description of the test fixture and the test procedure is defined in UHS-II PHY Test Guideline document



**Figure C- 1: Host Test Fixture Illustration (Concept)**

### C.2 Test Condition for Card Output Signal at TP2

By using Card test fixture, illustrated in Figure C- 2, a measurement for output waveform of Card transceiver is performed. The test fixture is designed to be as ideal as possible (100ohm differential impedance and 250hm common-mode impedance as the target). A detailed description of the test fixture and the test procedure is defined in UHS-II PHY Test Guideline document



**Figure C- 2: Card Test Fixture Illustration (Concept)**

## Appendix D (Normative) : Register

### D.1 Register Summary

#### D.1.1 Register Types

Attribute of register field should be defined as an example shown below. It may help easy to understand register specification

Register fields are assigned one of the attributes described below:

Register Attribute	Description
RO	Read-only register: Register bits are read-only and cannot be altered by software or any reset operation. Writes to these bits are ignored.
ROC	Read-only status: These bits are cleared to zero at reset. Writes to these bits are ignored.
ROW1C	Read-only status, Write-1-to-clear status: Register bits indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to ROW1C bits has no effect.
RW	Read-Write register: Register bits are read-write and may be either set or cleared by software to the desired state. These bits are cleared to zero at reset.
RWAC	Read-Write, automatic clear register: Software requests an operation by setting the bit. The hardware shall clear the bit automatically when the operation completes. Writing a 0 to RWAC bits has no effect.
HwInit	Hardware Initialized: Register bits are initialized by firmware or hardware mechanisms. Bits are read-only after initialization, and writes to these bits are ignored.
Rsvd	Reserved. Device shall initialize to zero on reserved bits and ignore writes to these bits. Host shall ignore these bits. The bit can be defined for future use.

**Table D- 1 : Register Attribute Table**

#### D.1.2 Register Initial Values

Hardware should set registers to their initial values at power-on reset. Initial values for RO and HwInit are specified by each Device. Those for other types of register shall be set to zero except parameters used in Boot Code Loading.

## Appendix E (Informative) : Design Guide

For the ease of Host transmitter and receiver design, the informative specifications and eye masks at TP1 are defined below and shown at Figure 4-6.

### E.1 Host Design

#### E.1.1 Informative Specification of Host Transmitter at TP1

For the design of Host transceiver, an informative electrical specification and eye mask at TP1 are shown in Table E- 1, Table E- 2 and Figure 4-6 (1). When designing Host transceiver, these specification and eye mask may be used as a reference.

Item	Symbol	value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	140	200	280	mV	Absolute value. Note.1
Rise/Fall time of Differential signal	$T_r, T_f$	100	-	-	ps	From 20% to 80% of voltage swing. Note 2
Common mode voltage	$V_{CM}$	150	200	250	mV	Note 1, 7
EIDL state differential voltage	$V_{diff\_PD}$	-10	0	10	mV	Note 3
EIDL state common mode voltage	$V_{CM\_PD}$	-10	0	10	mV	Note. 3,7
Intra skew	$Sk_{intra}$	-	-	25	ps	Note. 4, Note 5
Inter skew	$Sk_{inter}$	-	-	0.35	UI	Note 6

Note 1: With a differential termination of  $100\Omega$ .

Note 2: Designers should consider improvement of signal integrity and reduction of EMI to determine rise/fall time of Host and Device output. Use of slower rise/fall time in Range A compare with Range B is an example implementation.

Note 3: In EIDL state, both positive and negative lines of D0 Lane are pulled down by Tx.

Note 4: This spec is tested by using a differential termination of  $100\Omega$ .

(More details in UHS-II PHY Test Guideline document).

Note 5: Intra skew means the skew between D0+ and D0- (and also D1+ and D1- when transmit from Host to Device in 2L-HD mode), as measured between half voltage swing of both signals.

Note 6: Inter skew means the skew between D0 and D1, when both transmitters transmit from Host to Device, as measured between cross points of each differential pair in 2L-HD mode.

Note 7:  $V_{CM\_PD}$  and  $V_{CM}$  are measured in reference to its local GND.  
(more details in UHS-II PHY Test Guideline document).

**Table E- 1: D0, D1 Output Requirement for Host Transmitter at TP1 (Informative)**

Item	Symbol	value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	140	200	280	mV	Absolute value. Note.1
Rise/Fall time of Differential signal	$T_{R,Tf}$	-	-	0.2	$T_{RCLK}$	From 20% to 80% of voltage swing. Refer to Section 4.11 for low EMI. Note.2
Common mode voltage	$V_{CM}$	150	200	280	mV	Note.1,4,5
Total Jitter	$T_J$	-	-	0.25	UI	Refer to section 4.3.4. Note 7
Intra skew	$Sk_{intra}$	-	-	200	ps	Note 3,6
Duty cycle	$T_{CKH}$	42.5		57.5	%	Of $T_{RCLK}$

Note.1: With a differential termination of  $100\Omega$ .

Note.2:  $T_{RCLK}$  means the period time of RCLK

Note 3: Intra skew means the skew between RCLK+ and RCLK- as measured between half voltage swings of both signals.

Note 4:  $V_{CM}$  is measured in reference to its local GND. (more details in UHS-II PHY Test Guideline document)

Note 5: It is recommended for Host to disconnect legacy DAT0 DAT1 pull up resistors by switch in UHS II mode.

Note 6: Refer to Section 4.11 for reducing EMI.

Note 7: RCLK jitter for Host transmitter is measured related to itself using a 2nd order soft PLL with BW of  $2.34MHz/S_r$ , inside the test equipment. Detailed measurement procedure is described in UHS-II PHY Test Guideline document.

**Table E- 2: RCLK Output Specification for Host Transmitter at TP1 (Informative)**

### E.1.2 Informative Specification of Host Receiver at TP1

For the design of Host receiver, an informative electrical specification and eye mask at TP1 are shown in Table E- 3 and Figure 4-6 (6). When designing Host receiver these specification and eye mask may be used as a reference.

Item	Symbol	Value			Unit	Note
		Min	Typ	Max		
Differential voltage	$V_{diff}$	95	-	-	mV	Absolute value.
Common mode voltage	$V_{CM}$	50	200	400	mV	The allowed common mode voltage under any condition.
EIDL state common mode voltage	$V_{CM\_PD}$	-110	0	160	mV	Note 1,2
Total Jitter	$T_J$	-	-	0.5	UI	
Inter skew	$Sk_{inter}$	-	-	1.25	UI	Note 3

Note 1: In EIDL state, both positive and negative lines of D1 Lane are pulled down by Tx.

Note 2: $V_{CM\_PD}$  and  $V_{CM}$  are measured in reference to its local GND.( more details in UHS-II PHY Test Guideline document)

Note 3: Host Receiver shall tolerate the inter skew spec defined at Table 4-10 and additional inter skew caused in Host PCB.

**Table E- 3: D0, D1 Input Specification for Host Receiver at TP1 (Informative)**

### E.1.3 Host PCB Design

The difference of the trace length between positive and negative of a differential Line causes intra skew. Intra skew relates to Eye opening and EMI. The less Intra Skew the much more eye opening. For the target of Host PCB design, it is recommended the difference between the length of positive and negative in the Host PCB is less than 1mm.

### E.1.4 Care for the Floating Input

In below 2 cases, Host receivers might face with floating input or Hi-Z. Host designer should take care for these cases in order to avoid the false operation:

- Empty socket (No Card inserted)

In this case Host input Lines is floating and uncertain state should be avoided.

Host may use Card detect indication to enable/disable its input receiver and amplitude detector.

- Power cycle

When Host issue power cycles, it turns off VDD2 and input Lines become Hi-Z or floating.

Power cycle is under Host control, so it may easily enable/disable its input receiver and amplitude detector to prevent uncertain state.

## E.1.5 Spread Spectrum Clocking (SSC)

Host may use SSC modulation with down spreading method which modulates the carrier frequency toward only lower frequency.

The SSC is treated as in-band clock spectrum and therefore not filtered out by the Host and Device PLLs. The one sided SSC (down spreading in UHS-II) is slightly decrease the average RCLK rate. Therefore the average data transfer rate is also decreased accordingly with half of the SSC deviation frequency e.g.  $\Delta f_{RCLK}/2$ .

If SSC is supported, there should be on/off configuration options. The SSC should be at "on" state during power up and wakeup from Dormant state. The SSC is modulated by the Host side and no special configuration is needed at the Device side. Nevertheless, Device designer should consider the influence of SSC on Rx PLL, data recovery function and Device Tx. For example: Certain amount of additional jitter is expected to appear on Device Rx PLL output, depending upon various PLL design.

Host that utilizes SSC should be aware that the SSC goes through the Device Tx circuitry. The SSC received with the signal on Host Rx may be reduced (dependent on Device implementation, and Device Tx circuitry BW).

Three cases should be considered:

- I. SSC may not appear at all on the data transmitted by Device.
- II. SSC may partially appear on the data transmitted by Device.
- III. SSC may fully appear on the data transmitted by Device.

SSC may be implemented as a method of reducing EMI. It is up to Host implementation to choose the amount of RCLK spreading,  $\Delta f_{RCLK}$ , between 0ppm (equal to no spreading) to -5000ppm maximum frequency spreading. The modulation frequency shall be within the 30 kHz – 33 kHz range.

Item	Symbol	Value		Unit	Note
		Min	Max		
SSC modulation frequency	$f_{ssc}$	30	33	kHz	
SSC peak frequency deviation	$\Delta f_{RCLK}$	0	-5000	ppm	
SSC Deviation rate	(df/dt)	-30	30	kHz/usec	

Table E- 4: SSC Parameters

The exact modulation shape for the SSC is Host implementation.

An example of the frequency modulation by triangular SSC waveform is shown in Figure E- 1 for the maximum RCLK frequency of 52 MHz, data rate of 1.5GHz and SSC modulation frequency = 30KHz. The frequency of the RCLK is varying by time according to triangular modulation.

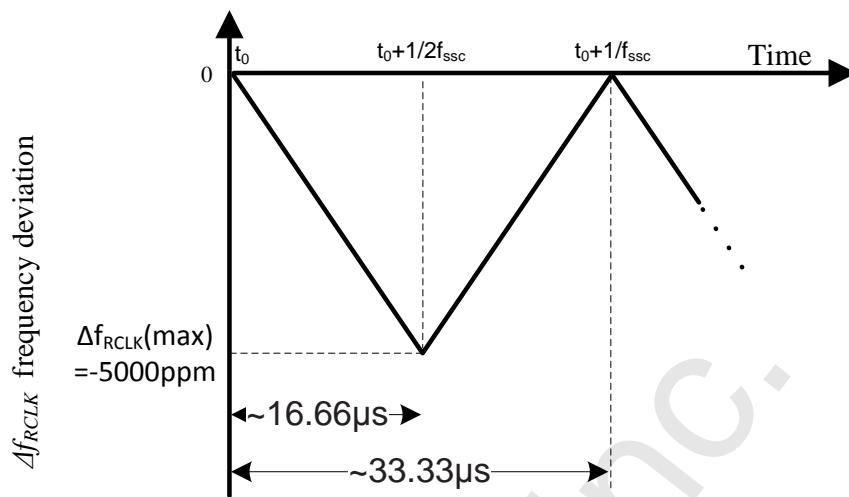


Figure E- 1: Example Period Modulation for Triangular SSC

## E.2 Device Design

### E.2.1 Device Transmitter Design

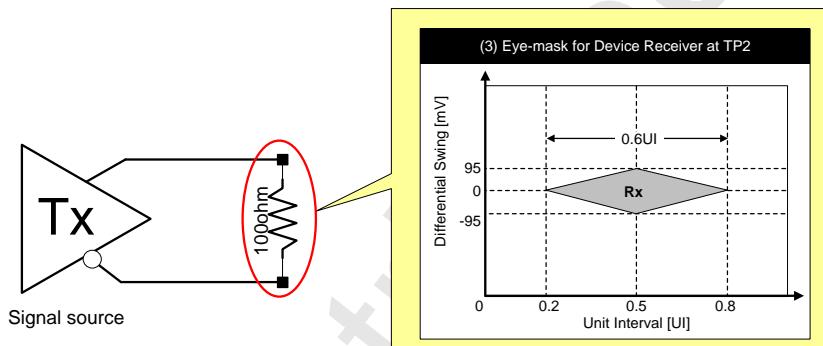
The less Intra Skew the wider eye opening. It is recommended Intra Skew of D1 (and D0 in 2L-HD mode) transferred from Device is less than 30ps for the target of Device design.

### E.2.2 Device Receiver Design

The following steps are useful for designing Receiver.

(Step.1) Calibrate the eye opening of signal source so as to close to (3) eye-mask at SI simulation.

In this calibration, output impedance of signal source is 50ohm as single-ended (100ohm as differential) and Rterm for output calibration is 100ohm.



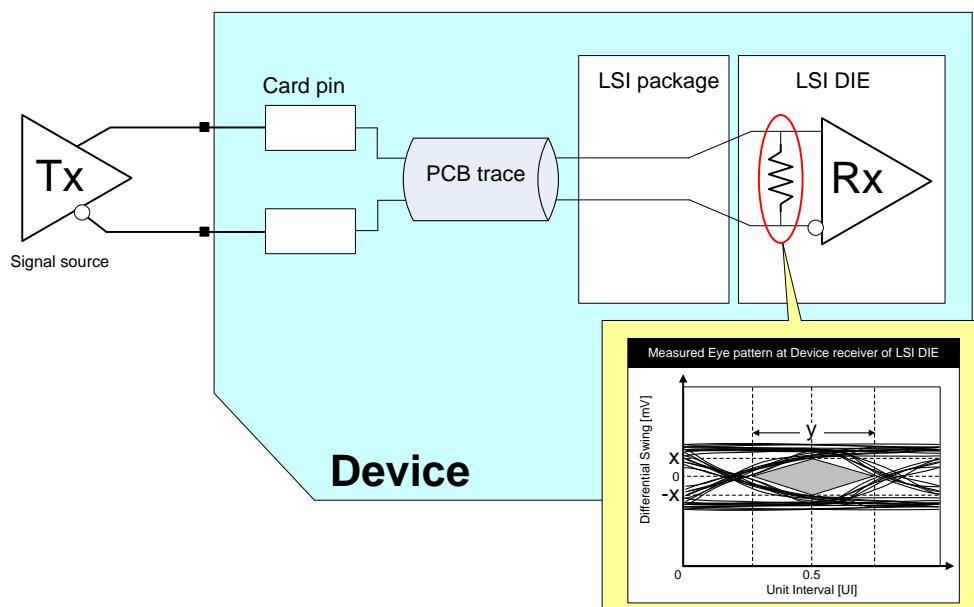
**Figure E- 2: Calibration of Signal Source**

(Step.2) Verify that the worst characteristic of Device Rx Lane components meets RLDD specification.

Device Rx Lane components mean Card Pin, PCB trace, LSI package and Termination resistor of Receiver, Center-Tap capacitor, parasitic capacitance, etc.)

(Step.3) Connect the signal source calibrated at step.1 to the Device Rx Lane model at SI simulation. And measure the eye opening at the Termination resistor of Receiver.

(Step.4) The eye opening measured at the Step.3 is helpful for designing Receiver input sensitivity since it reflects the eye opening resulting at the Rx LSI after Device Rx Lane losses.



**Figure E- 3: SI Simulation for Checking the Eye Opening at Receiver Termination**

### E.2.3 Device System Level CM Noise

In a Device, UHS-II PHY is integrated in a system that may cause CM noise to be experienced by the PHY circuitry.

An example for typical CM noise source is the Device internal IO toggling. Other noise sources should be considered as well, depending on specific device system implementation.

It is strongly recommended that Device designer would take the CM noise phenomenon into account. The CM noise is generated inside the device, and its amount is dependent on the specific Device implementation. Device designer should make sure that the Rx design is tolerable to this noise and Tx signals meet Device Tx specification.

It is recommended to take the 'worst case' device operating conditions into account. Since 'worst case' operation condition is individual per specific Device implementation, it is not defined herein. Device designer is responsible to define the 'worst case' operation condition for a specific Device.

Nevertheless, it is recommended that 'worst case' operating condition will include also the Device system internal IO toggling.

The following aspects should be taken into account when designing the Device:

**Device Tx output** – In order to address V<sub>cm\_noise</sub> and V<sub>cm\_pd\_noise</sub>, it is recommended to take the impact of the socket into account. For Device that supports Half Duplex, Device designer should take into account that D0 and D1 transmitters might be differently affected by CM noise.

**Device Rx input (on LSI)** – Since the Device internal CM noise is very strongly dependent with the Device system implementation, there is no specific parameter defined for it in the UHS-II PHY specification. Device designer should assure that the CM noise generated by the Device may be tolerated by the device PHY Rx design.

**Other Device elements** – In addition the CM noise should be taken into account, otherwise it may affect very strongly other elements inside the device (e.g. analog circuits)

## Appendix F (Informative) : PHY-LINK I/F

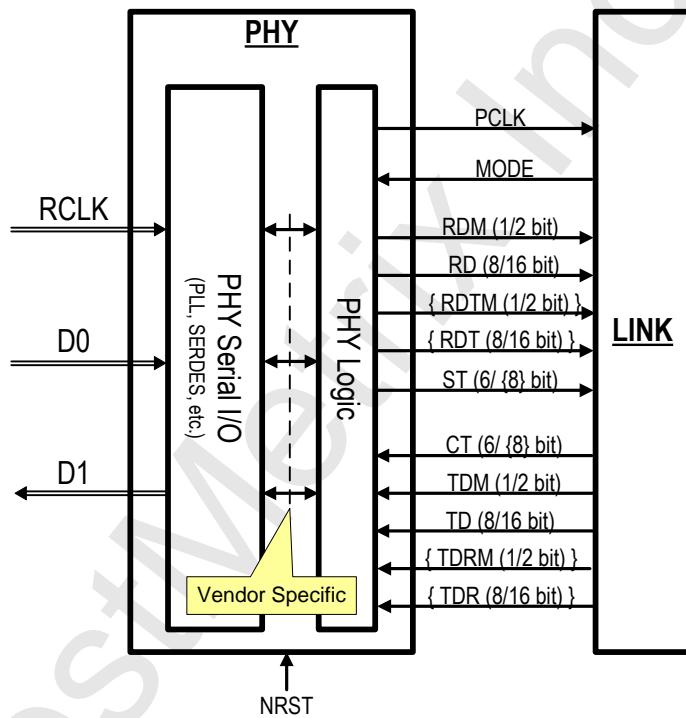
### F.1 Overview

PHY-LINK I/F is defined to abstract the vendor-specific implementation of UHS-II PHY for the purpose of distributing PHY and Protocol IP separately.

### F.2 I/F Detail

#### F.2.1 Block Diagram

Figure F- 1 illustrates the block diagram of PHY-LINK I/F for Device. Signals or parameters with brace mean that they are required in case of supporting 2L-HD mode.



**Figure F- 1 : Block Diagram of PHY-LINK I/F for Device**

PHY control and status signals are encoded by CT (Control) and ST (Status) signals respectively, and these signals are transferred across PHY-LINK I/F based on PCLK. PHY-Logic is responsible for converting CT and ST to meet the vendor-specific I/F of Serial I/O including PLL, SERDES, and so on.

The interface signals are divided into the following three categories.

- Transmit / Control data
- Receive / Status data
- Miscellaneous data

#### F.2.2 Definition of Interface Signal

From Table F- 1 to Table F- 3 show the detailed descriptions of the interface signals. In addition, Table F- 4 shows the external signals provided from external part of PHY-LINK I/F. Note that P, L, and Ex in

**UHS-II Addendum Version 1.02**

"Direction" column stand for PHY, LINK, and external part respectively. Moreover, signals and explanations with asterisk mean that they are required in case of supporting 2L-HD mode.

Name	Direction (P:PHY, L:LINK)	Width	Description
TD	L→P	8 or 16	Transmit Data for Tx Block †1
TDM	L→P	1 or 2	TD Coding Mode (0: D-Symbol, 1: K-Symbol) †2
TDR*	L→P	8 or 16	Transmit Data for Rx Block †1
TDRM*	L→P	1 or 2	TDR Coding Mode (0: D-Symbol, 1: K-Symbol) †2
CT	L→P	6 or 8*	PHY Control (CT[3:0] = PINIT/PCMD depending on MODE)
			PHY Initialization parameter in Dormant state
			[1:0]: Selected PHY Major Revision Reserved (set 00b for UHS156) [3:2]: Selected Transmission Speed Range 00: Range A (390 – 780 Mbps per Lane at UHS156) 01: Range B (780 – 1,560 Mbps per Lane at UHS156) others: Reserved
			[3:0]: PINIT (when MODE=0)
CT	L→P	6 or 8*	PHY Command
			0000: No Command Operation 0001: Enter to Loopback mode for DB Streaming 0011: Exit from Loopback mode for DB Streaming 0101: Enter to (2L-)HDIN mode (Default TxàRx) * 0110: Enter to (2L-)HDOUT mode (Default RxàTx) * 0111: Exit from (2L-)HD mode * 11XX : Reserved for Vendor Unique Command others: Reserved
			[3:0]: PCMD (when MODE=1)
			[5:4]: TDS
CT	L→P	6 or 8*	TD State Control
			00: EIDL (Electrical Idle state with DIF-PD) 01: OFF (Electrical Off state with DIF-Z) 10: STB (Standby state with fixed DIF-L or DIF-H) 11: VLD (Valid 8b/10b Symbol state with DIF-L or DIF-H)
			[7:6]: TDRS*
			TDR State Control
CT	L→P	6 or 8*	00: EIDL (Electrical Idle state with DIF-PD) 01: OFF (Electrical Off state with DIF-Z) 10: STB (Standby state with fixed DIF-L or DIF-H) 11: VLD (Valid 8b/10b Symbol state with DIF-L or DIF-H)

†1: When TDS/TDRS = STB, TD/TDR[0] = 0 and TD/TDR[0] = 1 indicate STB.L and STB.H respectively, and TD/TDR[15:1] can be set arbitrary values.

If the width of TD/TDR is 16bit, "COM" symbol is always transmitted on TD/TDR[7:0].

†2: If the width of TD/TDR is 16bit, TDM/TDRM[0] and TDM/TDRM[1] corresponds to TD/TDR[7:0] and TD/TDR[15:8] respectively.

**Table F- 1 : Interface Signals (Transmit / Control Data)**

Name	Direction (P:PHY, L:LINK)	Width	Description	
RD	P→L	8 or 16	Receive Data of Rx Block †3	
RDM	P→L	1 or 2	RD Coding Mode (0: D-Symbol, 1: K-Symbol) †4	
RDT*	P→L	8 or 16	Receive Data of Tx Block †3	
RDTM*	P→L	1 or 2	RDT Coding Mode (0: D-Symbol, 1: K-Symbol) †4	
ST	P→L	6 or 8*	PHY Status	
			[0]: DET	Amplitude Detector Output (high active) †5
			[1]: LOCK	PLL Lock (high active)
			[2]: PACK	PCMD acknowledge (high active)
			[3]: ERR	PHY Receive Error Status (0: No Error, 1: Error occurs on at least one data Lane) †6
			[5:4]: RDS	RD Status
			00: EIDL (Electrical Idle state with DIF-PD)	
			01: OFF (Electrical Off state with DIF-Z)	
			10: STB (Invalid 8b/10b Symbol with DIF-L or DIF-H)	
			11: VLD (Valid 8b/10b Symbol with DIF-L or DIF-H)	
[7:6]: RDTS*	RDT Status			
00: EIDL (Electrical Idle state with DIF-PD)				
01: OFF (Electrical Off state with DIF-Z)				
10: STB (Invalid 8b/10b Symbol with DIF-L or DIF-H)				
11: VLD (Valid 8b/10b Symbol with DIF-L or DIF-H)				

†3: When RDS/RDTS = STB and ERR = 0, RD/RDT[0] = 0 and RD/RDT[0] = 1 indicate STB.L and STB.H respectively, and RD/RDT[15:1] can be ignored.

If the width of RD/RDT is 16bit, "COM" symbol is always transmitted on RD/RDT[7:0].

†4: If the width of RD/RDT is 16bit, RDM/RDTM[0] and RDM/RDTM[1] correspond to RD/RDT[7:0] and RD/RDT[15:8] respectively.

†5: DET is negated during DIF-PD and asserted when Amplitude Detector detects fixed DIF-L of STB.L. And DET is asynchronous signal because it may be used without RCLK during Wakeup.

†6: PHY Receive Error includes 8b/10b decode error (notified to LINK by ERR=1, RDS=STB, RD=0) and 8b/10b disparity error (notified to LINK by ERR=1, RDS=VLD, RD=decoded data).

**Table F- 2 : Interface Signals (Receive / Status Data)**

Name	Direction	Width	Description
PCLK	P→L	1	Parallel Interface Clock for LINK
MODE	L→P	1	PHY Power Mode (0: Dormant state, 1: After exiting from Dormant)

**Table F- 3 : Interface Signals (Miscellaneous Data)**

Name	Direction	Width	Description
CLK	Ex→P	1	Source Clock (Only for Host)
NRST	Ex→P&L	1	Asynchronous Reset (low active) e.g. Power On Reset

**Table F- 4 : External Signals**

### F.2.3 Details of PCMD and PACK

PCMD stands for PHY Command and is used to perform specific functions directed by LINK.

Its value is "0000b" when no commands are requested. When LINK requests PHY to perform a function, it set PCMD to the defined value other than "0000b". Note that PCMD is valid after exiting from Dormant state (MODE = 1). Before that, CT[3:0] is used as PINIT to configure PHY speed range. PHY shall be configured by PINIT at the last positive edge of PCLK before MODE assertion.

PACK is a pulse signal transferred from PHY to LINK as a PCMD acknowledgement. Assertion timing of PACK depends on each PCMD. Just after receiving PACK, LINK shall set PCMD to "0000b" for at least one cycle before requesting next PCMD.

Figure F- 2 shows an example sequence of PCMD and PACK.

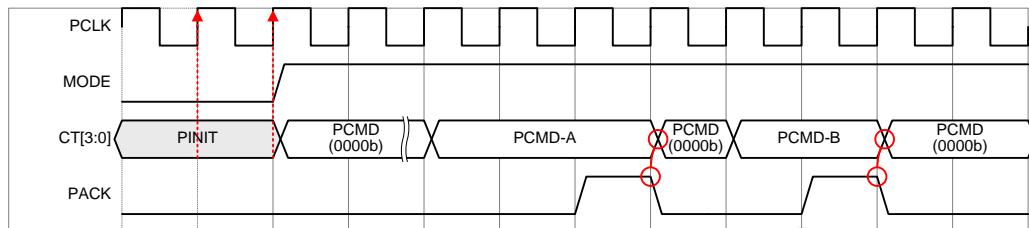


Figure F- 2 : An Example Sequence of PCMD and PACK

## F.3 Clock Generation

### F.3.1 Clock Generation in Host

Figure F- 3 shows an example of clock generation in Host.

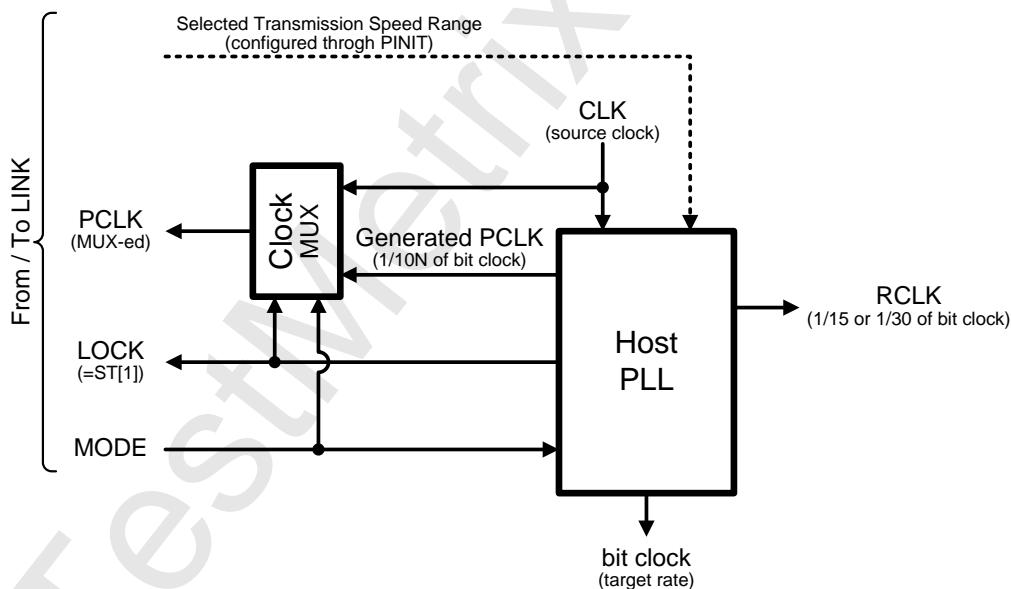


Figure F- 3 : Clock Generation in Host

Host PLL generates bit clock based on source clock (CLK) before starting Wakeup sequence. MODE signal is asserted when Host wants to exit from Dormant and start PHY activation. Moreover, MODE signal is used as a trigger for starting PLL lock. Before asserting MODE signal, PLL shall be configured by the setting of "Selected Transmission Speed Range" in CFG\_REG through CT[3:0] (= PINIT).

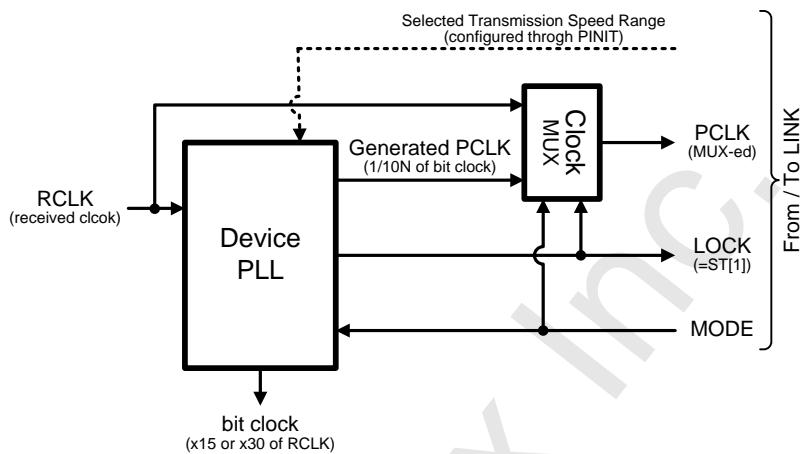
After bit clock generation, RCLK shall be generated by dividing bit clock for the purpose of having a correlation with it. Divider ratio is regulated by the setting of "Selected Transmission Speed Range" in CFG\_REG. In addition, bit clock is divided by 10N to generate PCLK, where N is a data width of TD and RD in bytes.

LOCK signal (= ST[1]) is asserted when PLL completes all clock generation (i.e. bit clock, RCLK and PCLK). CLK (source clock) and generated PCLK are multiplexed into PCLK which interface PHY and LINK. Clock MUX shall switch these clocks with glitch-free manner triggered by LOCK or MODE signal

transition as described later in this chapter. During Dormant state, RCLK output is gated by LOCK signal. And therefore, RCLK distribution is started after LOCK is asserted.

### F.3.2 Clock Generation in Device

Figure F- 4 shows clock generation in Device.



**Figure F- 4 : Clock Generation in Device**

Device PLL shall generate bit clock by multiplying RCLK. MODE signal is asserted when Device receives RCLK and exits from Dormant. Moreover, MODE signal is used as a trigger for starting PLL lock. Before asserting MODE signal, PLL shall be configured by the setting of "Selected Transmission Speed Range" in CFG\_REG through CT[3:0] (= PINIT). Multiplier ratio is regulated by the setting of "Selected Transmission Speed Range".

After bit clock generation, bit clock is divided by 10N to generate PCLK, where N is a data width of TD and RD in bytes.

LOCK signal (= ST[1]) is asserted when PLL completes all clock generation (i.e. bit clock and PCLK). Received RCLK and generated PCLK are multiplexed into PCLK which interface PHY and LINK. Clock MUX shall switch these clocks with glitch-free manner triggered by LOCK or MODE signal transition as described later in this chapter.

## F.4 I/F Timing Sequence

On the I/F timing sequences described in this section, "D" in TDM, RDM, TDRM and RDTM rows mean D-Symbol (in other words, TDM = 0 if "D" is indicated in TDM row). Moreover, "C0" in TD and RD rows indicates MSB of (scrambled) CRC16, and "C1" does LSB of (scrambled) CRC16.

### F.4.1 Reset and Activation (Exiting from Dormant state)

Figure F- 5 illustrates the I/F timing sequence of packet transfer in reset and activation for Host.

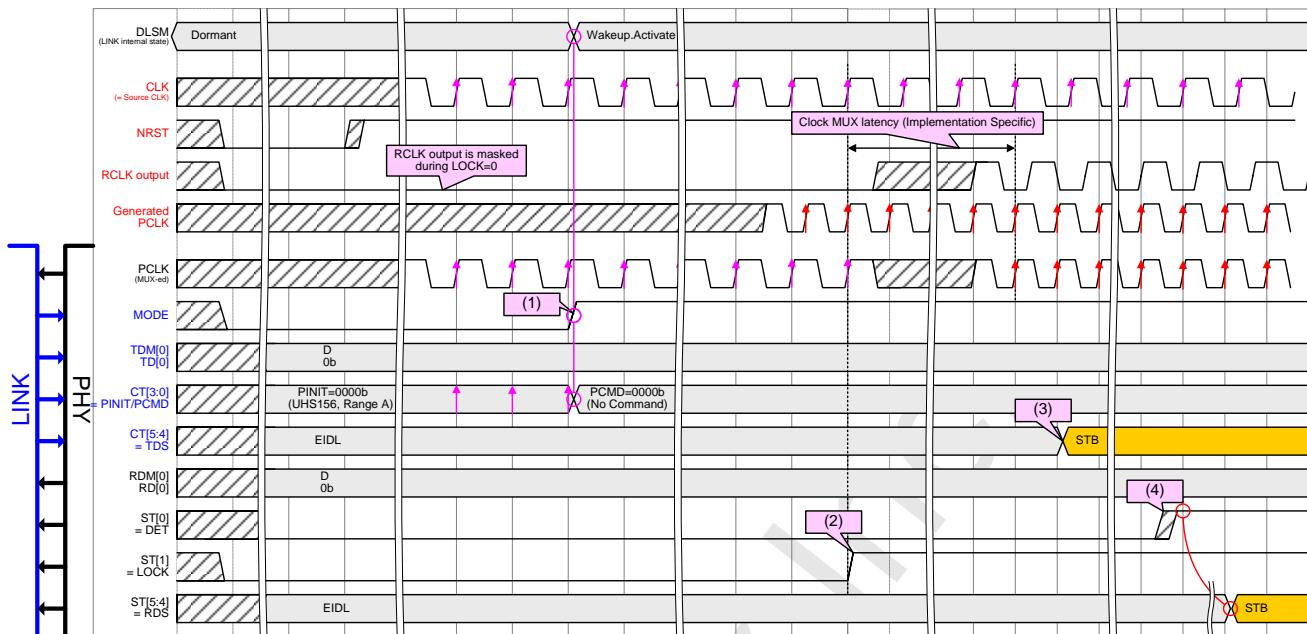


Figure F- 5 : I/F Timing Sequence (Reset and Activation for Host)

- (1) PHY shall be configured by CT[3:0] (=PINIT) at the last positive edge of PCLK before MODE assertion. LINK asserts MODE signal when Host wants to start PHY activation. And then, Host PLL starts bit clock generation according to PINIT setting. Note that LINK shall keep MODE signal negated at least one PCLK period after it receives PCLK from PHY.
- (2) When Host PLL completes all clock generation (i.e. bit clock, RCLK and PCLK), it asserts LOCK signal. Then, Host starts to distribute RCLK to Device and PCLK is switched to the generated one which can be used for valid symbol transfer across PHY-LINK I/F.
- (3) After PCLK is certainly switched, LINK instructs PHY to send STB.L by setting TDS = STB, TDM[0] = 0 and TD[0] = 0. Moreover, TDM[1] is also equal to 0 when width of TD is 2 bytes.
- (4) Host can detect STB.L sent from Device with DET assertion or the following STB via RDS.

Figure F- 6 illustrates the I/F timing sequence of packet transfer in reset and activation for Device.

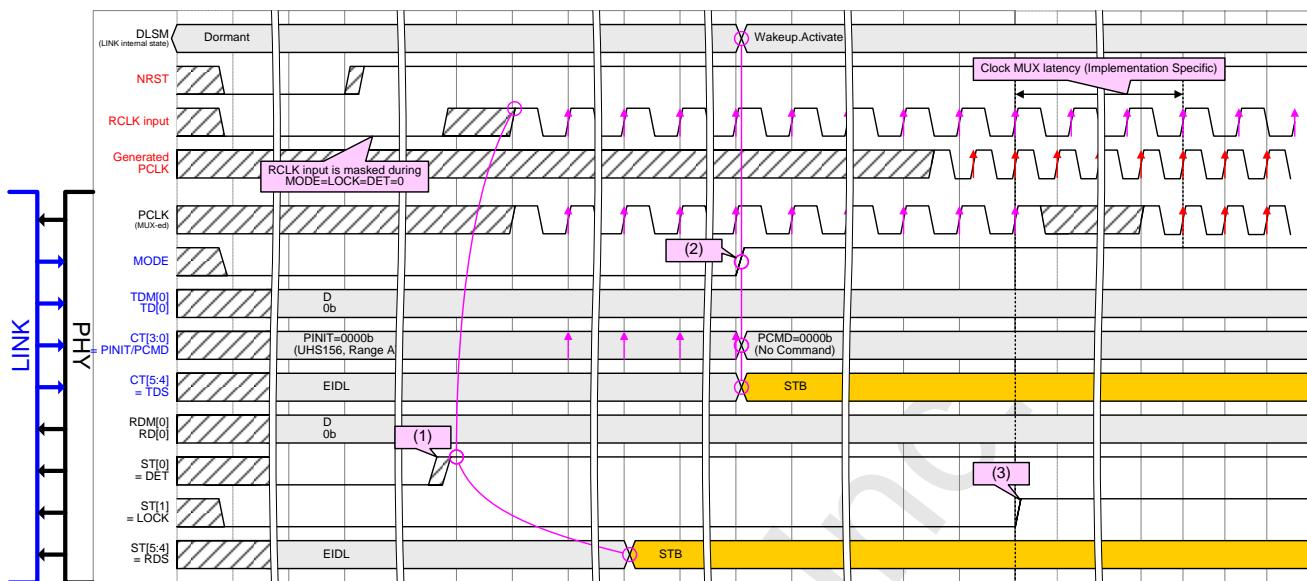


Figure F- 6 : I/F Timing Sequence (Reset and Activation for Device)

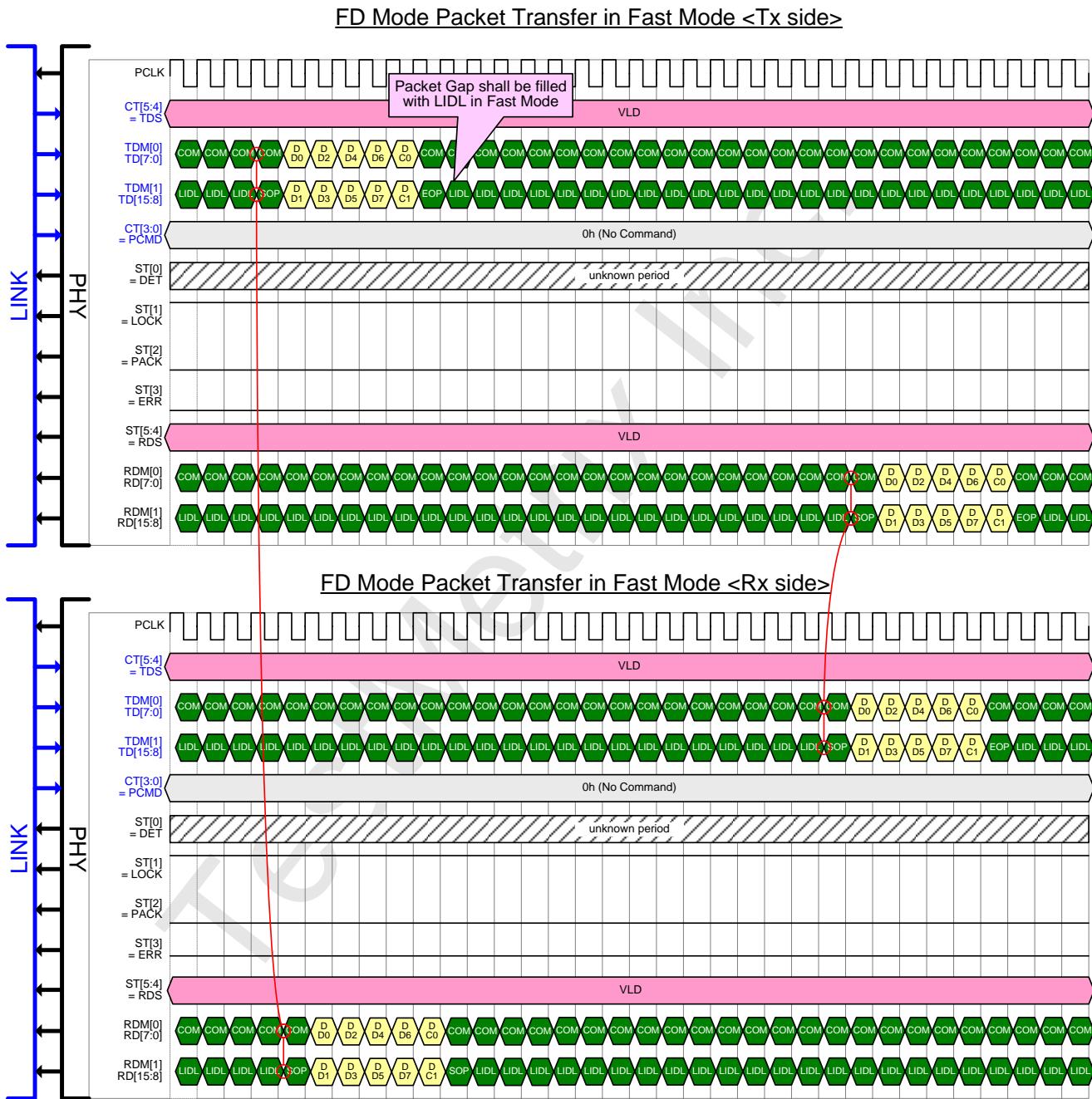
- (1) Device detects STB.L sent from Host with DET assertion or the following STB via RDS. DET is used for enabling RCLK.Rx and therefore, Device starts to receive RCLK. Note that RCLK.Rx does not have Amplitude Detector because RCLK+/- are supposed to be shared with DAT0/1 of Legacy SD I/F. So, RCLK.Rx is enabled by DET on D0.Rx and kept enable by MODE or LOCK after exiting from Dormant.
- (2) PHY shall be configured by CT[3:0] (= PINIT) until MODE assertion. LINK asserts MODE signal after the PHY configuration using PINIT. Note that LINK shall keep MODE signal negated at least one PCLK period after it receives PCLK from PHY. Then, Device PLL starts bit clock generation according to the PINIT setting. At this time, LINK instructs PHY to send STB.L by setting TDS = STB, TDM[0] = 0 and TD[0] = 0. Moreover, TDM[1] is also equal to 0 when width of TD is 2 bytes. Device PHY needs to be capable of sending STB.L even if its PLL is not locked.
- (3) When Device PLL completes all clock generation (i.e. bit clock and PCLK), it asserts LOCK signal. Before LOCK assertion, PCLK is same as input RCLK. But after LOCK is asserted, PCLK is switched to the generated one which can be used for valid symbol transfer across PHY-LINK I/F.

Before exiting from Dormant state, LINK of both Host and Device shall hold MODE to "0b" and CT[3:0] (= PINIT) to the desired value in order to configure PHY initial parameter (i.e. Speed Range). Note that PINIT shall be set to "0000b" as a default value just after power on.

## F.4.2 Packet Transfer in Fast Mode

In the examples described from Figure F- 7 to Figure F- 9, data width of TD and RD is 16 bits.

Figure F- 7 illustrates the I/F timing sequence of packet transfer in Fast Mode.



**Figure F- 7 : I/F Timing Sequence (Packet Transfer in Fast Mode)**

Note that the packet gap shall be filled with LIDL in Fast Mode as described in Section 5.4.

### F.4.3 Packet Transfer in Low Power Mode

Figure F- 8 illustrates the I/F timing sequence of packet transfer in Low Power Mode.

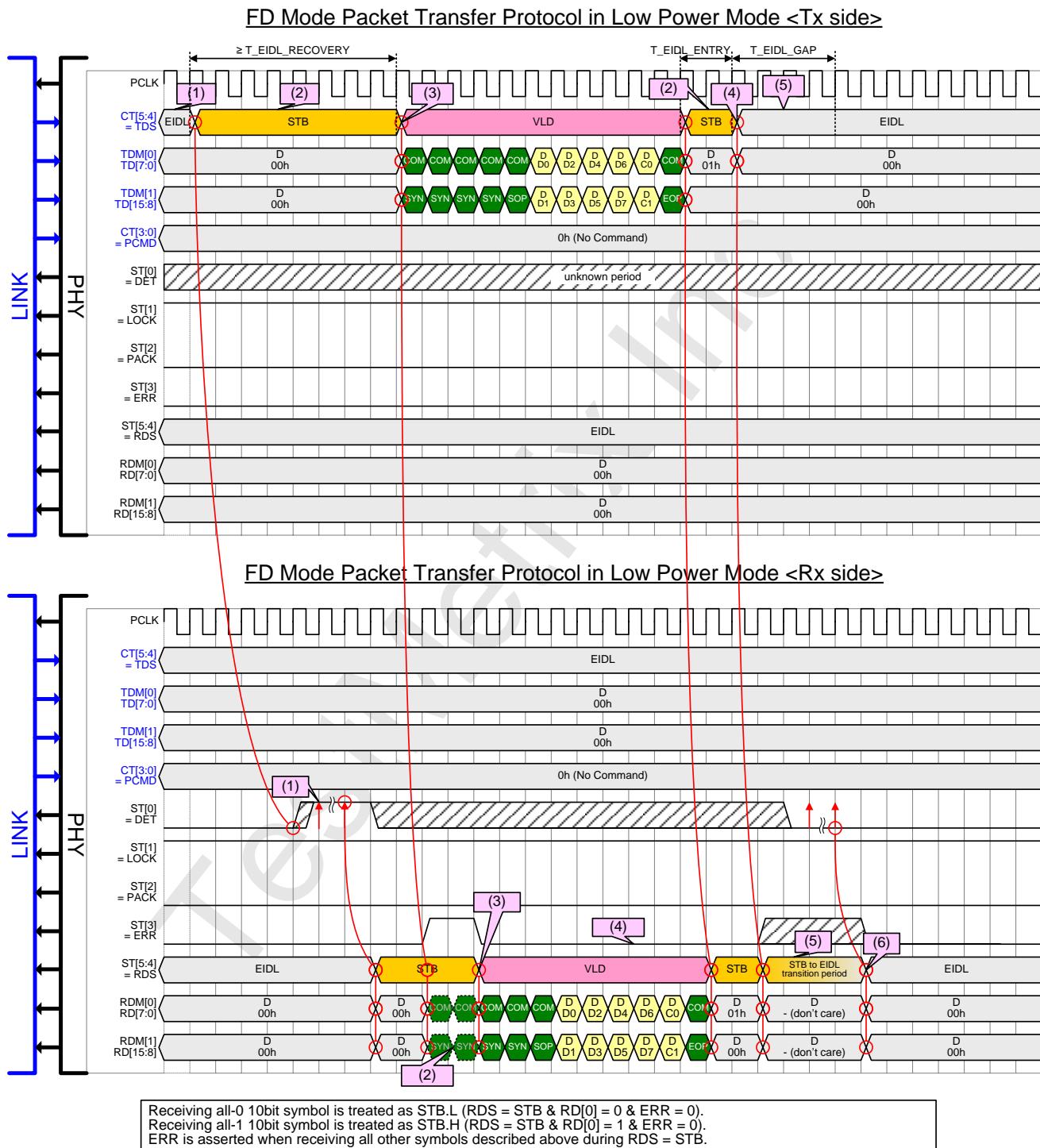


Figure F- 8 : I/F Timing Sequence (Packet Transfer in Low Power Mode)

For Tx side:

- (1) During TDS = EIDL, TDM = 00b and TD = 00h.

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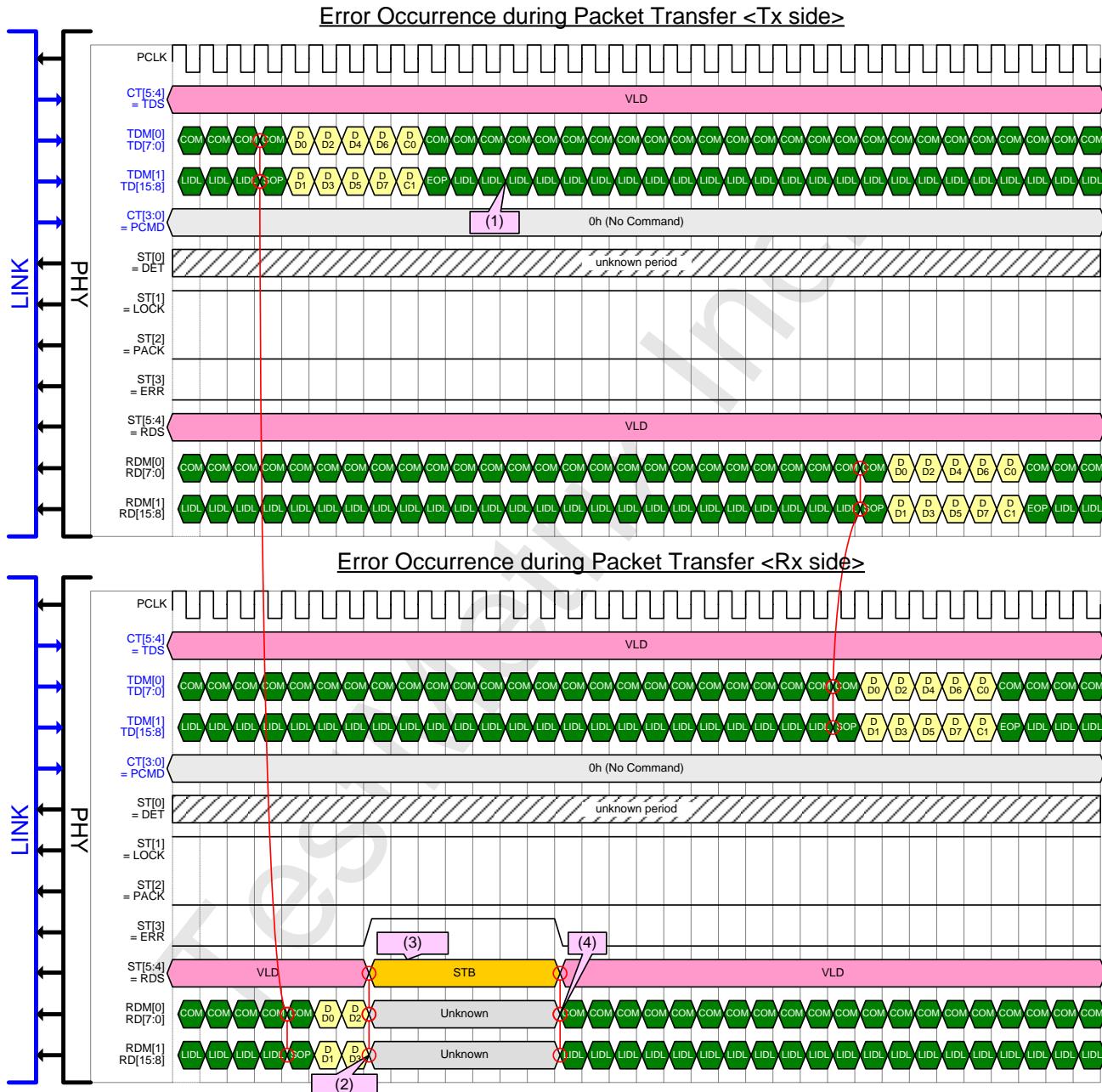
- 
- (2) During TDS = STB, TD[0] = 0 and TD[0] = 1 indicate STB.L and STB.H respectively.
  - (3) After elapsing of T\_EIDL\_RECOVERY (min 16 SI) in STB.L, Tx enters to VLD.
  - (4) After elapsing of T\_EIDL\_ENTRY (4 SI) in STB.H, Tx enters to EIDL.
  - (5) Tx shall be in EIDL at least T\_EIDL\_GAP before starting next transmission.

For Rx side:

- (1) DET assertion is reflected to RDS transition from EIDL to STB after the implementation specific period of sampling. After transition to STB, DET is not used until STB.H reception.
- (2) Leading SYN LSS may be corrupted until symbol lock is acquired. During this period, ERR is asserted because receiving data is neither all-zero nor all-one symbol.
- (3) After symbol lock, Valid 8b/10b symbols are transferred from PHY to LINK with RDS = VLD.
- (4) Between SOP and EOP, LINK shall monitor ERR to detect the PHY Receive Error.
- (5) RDS may be unknown because Lane state is during transition from STB to EIDL. Before EIDL transition, DET is required to be negated to prepare for next STB.L detection.
- (6) After receiving STB.H, RDS transits from STB to EIDL.

#### F.4.4 Error Occurrence during Packet Transfer

Figure F- 9 illustrates the I/F timing sequence of error occurrence during packet transfer in Fast Mode.



**Figure F- 9 : I/F Timing Sequence (Error Occurrence during Packet Transfer)**

- (1) Packet Gap shall be filled with LIDL in Fast Mode.
- (2) If Rx detects PHY Receive Error, ERR is asserted. And if the error is 8b/10b decoded error except all-zero and all-one 10bit symbol, RDS and RD indicates STB.L. On the other hand, if the error is 8b/10b disparity error, RDS stays in VLD and RDM / RD indicates decoded data same as valid data reception.
- (3) Above mentioned ERR state continues until valid symbol reception is recovered.

- (4) If symbol lock is lost during ERR state, it can be recovered by receiving a series of COM. In this case, LINK can detect packet loss by receiving LIDL without EOP

#### **F.4.5 Loopback Control for DATA Burst Streaming**

There are two possible locations for implementing the Loopback path for DATA Burst streaming.

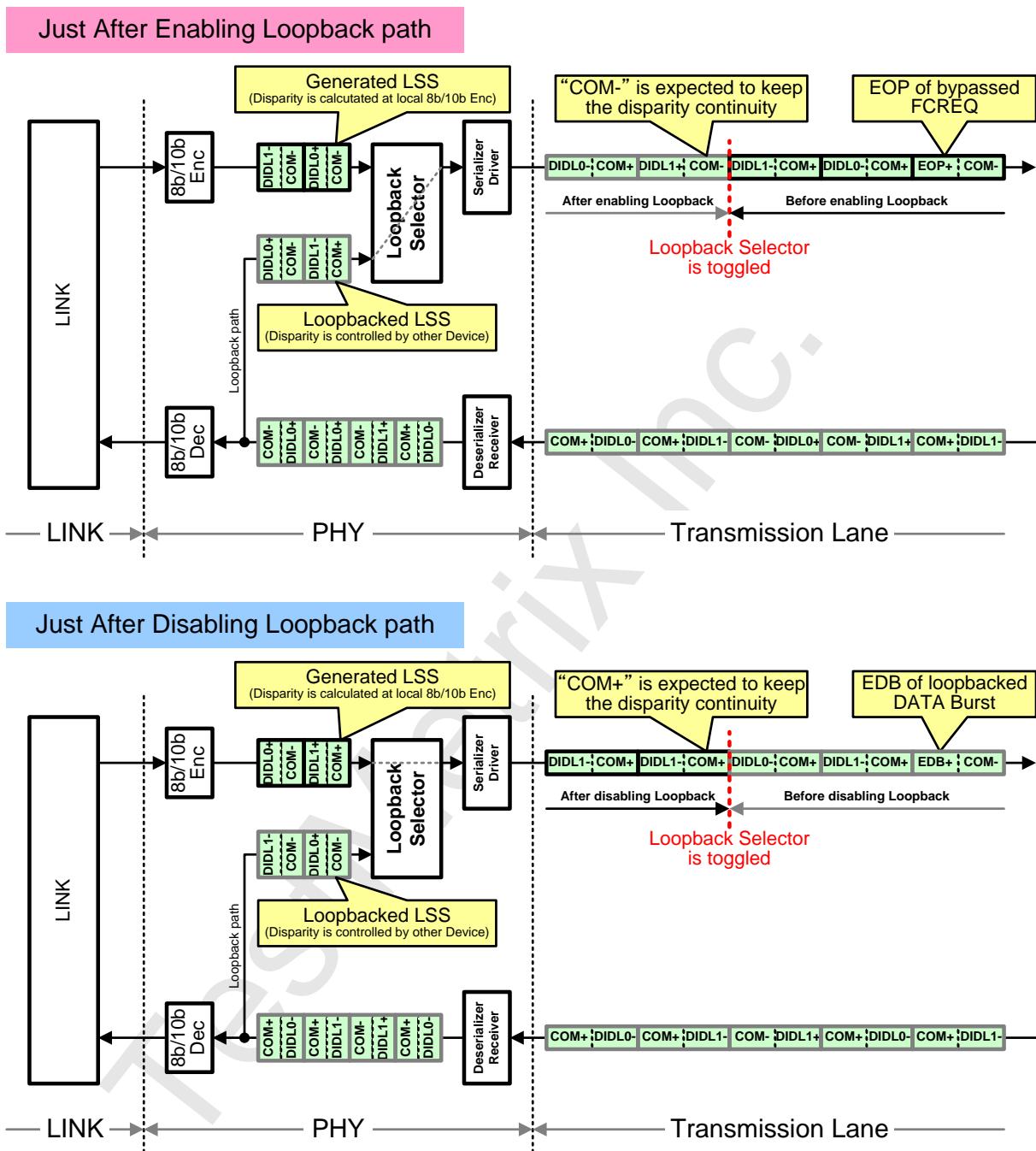
- (1) 8bit region (behind the 8b/10b decoder.)
- (2) 10bit region (before the 8b/10b decoder.)

In both Loopback cases, PHY shall adjust the position of "COM" between loopbacked LSS and generated LSS before switching Loopback Selector to keep the LSS boundary of transmitting data.

When implementing option (1), PHY does not need to take care of the disparity continuity when it switches Loopback Selector.

When implementing option (2), PHY shall keep the disparity continuity when it switches Loopback Selector. The rest of this section (Appendix F.4.5 ) explains what need to be done in order to implement this option.

Figure F- 10 illustrates ensuring disparity continuity when PHY toggles Loopback Selector in 10bit Loopback case.

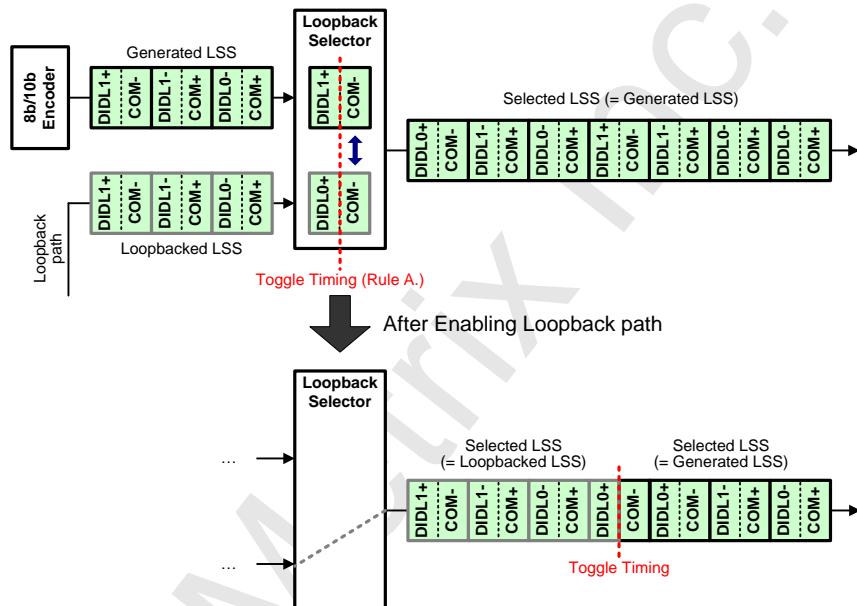
**Figure F- 10 : Ensuring Disparity Continuity**

In case of 10bit Loopback path, the disparity of loopbacked LSS is controlled by other Device. On the other hand, the disparity of generated LSS is calculated at local 8b/10b Encoder. So, these LSSes may have the opposite disparity. In this case, PHY is responsible for adjusting both loopbacked LSSes and generated LSS to have the same disparity when it switches Loopback Selector. To realize this, PHY shall compare disparities of "COM" and symbol types of the following "DIDL" (i.e. either "DIDL0" or "DIDL1") between loopbacked DIDL LSS and generated DIDL LSS at Loopback Selector. And PHY may need to swap the symbol type of "DIDL" between "DIDL0" and "DIDL1" according to the following rules.

Loopback Selector rules:

- Rule A. If both "COM" have the same disparity, Loopback Selector is toggled just after that "COM".
- Rule B. If both "COM" have the opposite disparity and both of the following "DIDL" are not the same symbol type, Loopback Selector is toggled just after that "DIDL".
- Rule C. If both "COM" have the opposite disparity and both of the following "DIDL" are the same symbol type, that "DIDL" is swapped its symbol type between "DIDL0" and "DIDL1" while its disparity is kept. And Loopback Selector is toggled just after swapped "DIDL".

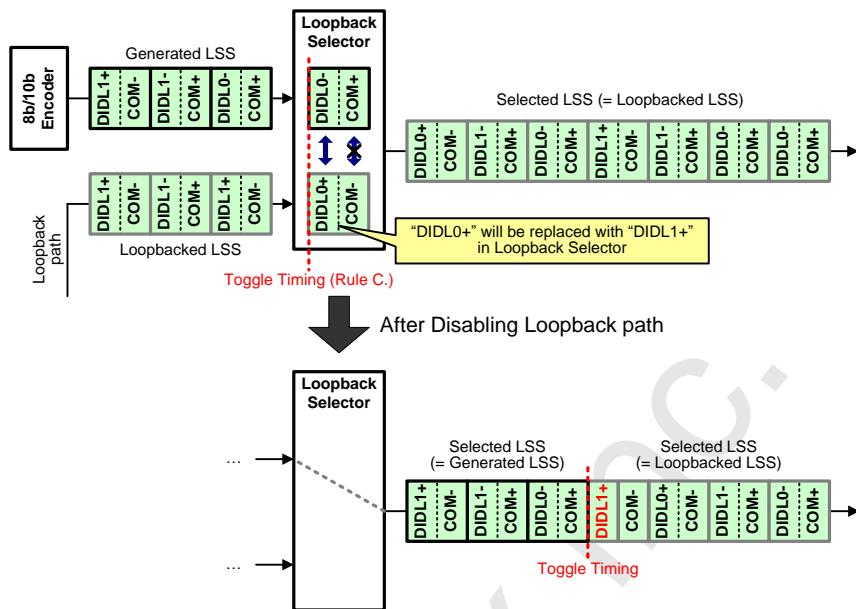
Figure F- 11 illustrates example of Loopback Selector operation (Rule A.) during Loopback entry.



**Figure F- 11 : Example of Loopback Selector Operation (Rule A.)**

In this case, both "COM" have the minus disparity at Loopback Selector. So, toggle timing is just after "COM-" in accordance with Rule A. described above.

Figure F- 12 illustrates example of Loopback Selector operation (Rule C.) during Loopback exit.

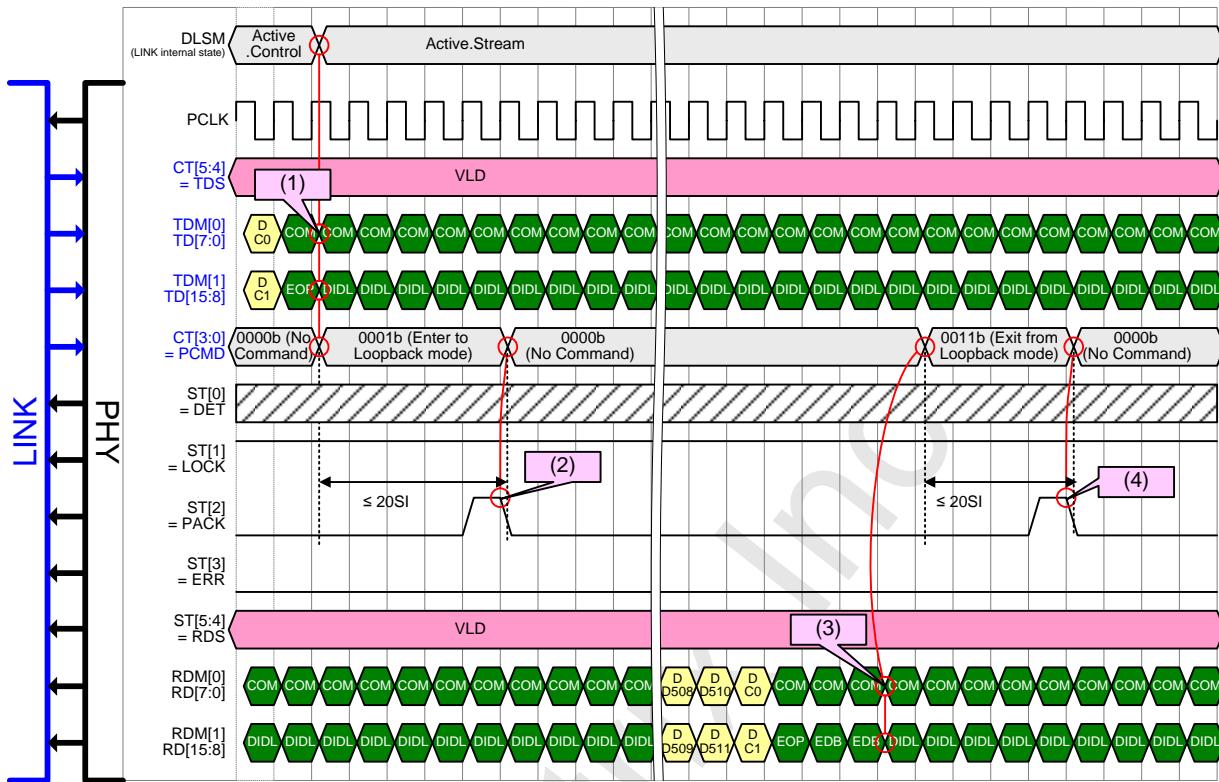


**Figure F- 12 : Example of Loopback Selector Operation (Rule C.)**

In this case, both "COM" have the opposite disparity and both of the following "DIDL" are "DIDL0" at Loopback Selector. So, "DIDL0+" is replaced with "DIDL1+" and Loopback Selector is toggled just after replaced "DIDL1+" in accordance with Rule C. described above.

Note that Loopback latency of PHY can be minimized by 10bit Loopback path and that path can be commonly used for both Data Burst Streaming and Loopback Test, although it is required to ensure the disparity continuity.

Figure F- 13 illustrates the I/F timing sequence of Loopback control for DATA Burst streaming.



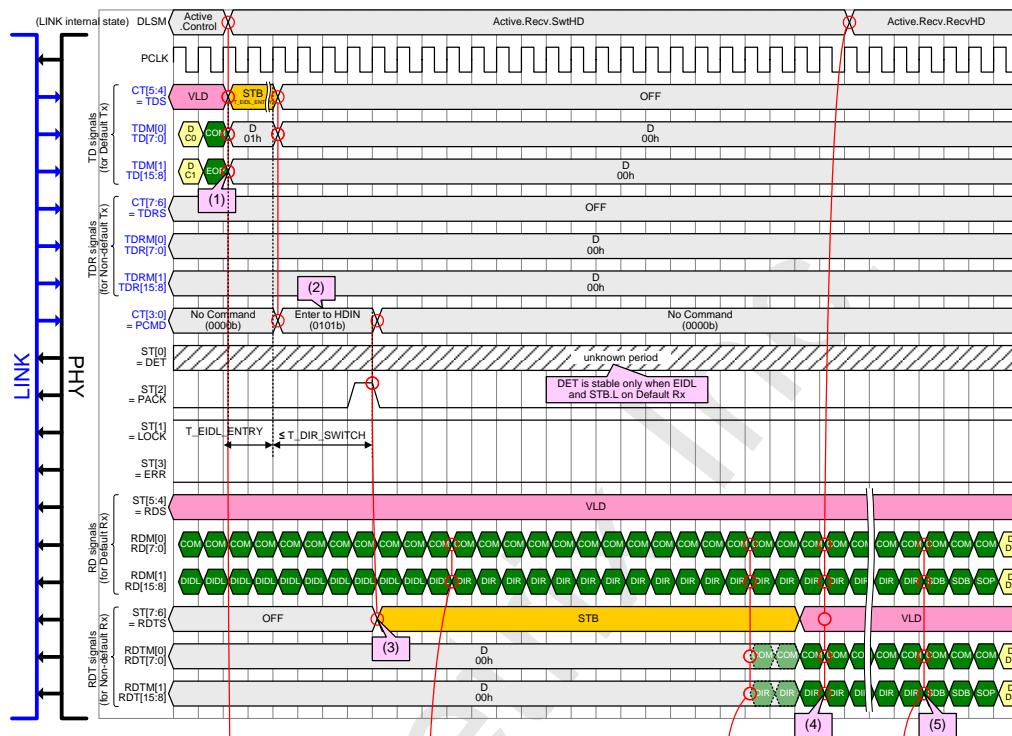
**Figure F- 13 : I/F Timing Sequence (Loopback Control for DATA Burst Streaming)**

- (1) LINK transits from Active.Control to Active.Stream when it completes FCREQ bypassing. At this time, LINK starts to send DIDL LSS and PCMD is set to "0001b" to enter to Loopback mode.
- (2) PHY is responsible for enabling its Loopback path considering continuity of transmitting data in terms of running disparity and LSS boundary before and after enabling Loopback path. PACK is asserted as an acknowledgement of PCMD when Loopback path is certainly enabled. Note that duration of PCMD for "Enter to Loopback mode" shall be asserted within 20 SI. Even after enabling Loopback path, LINK shall monitor RD signals to detect EDB as a trigger for disabling Loopback path.
- (3) After LINK detects EDB, PCMD is set to "0011b" to exit from Loopback mode.
- (4) PHY is responsible for disabling its Loopback path considering continuity of transmitting data, same as in the case of enabling Loopback path. PACK is asserted when Loopback path is certainly disabled. Note that duration of PCMD for "Exit from Loopback mode" shall be asserted within 20 SI.

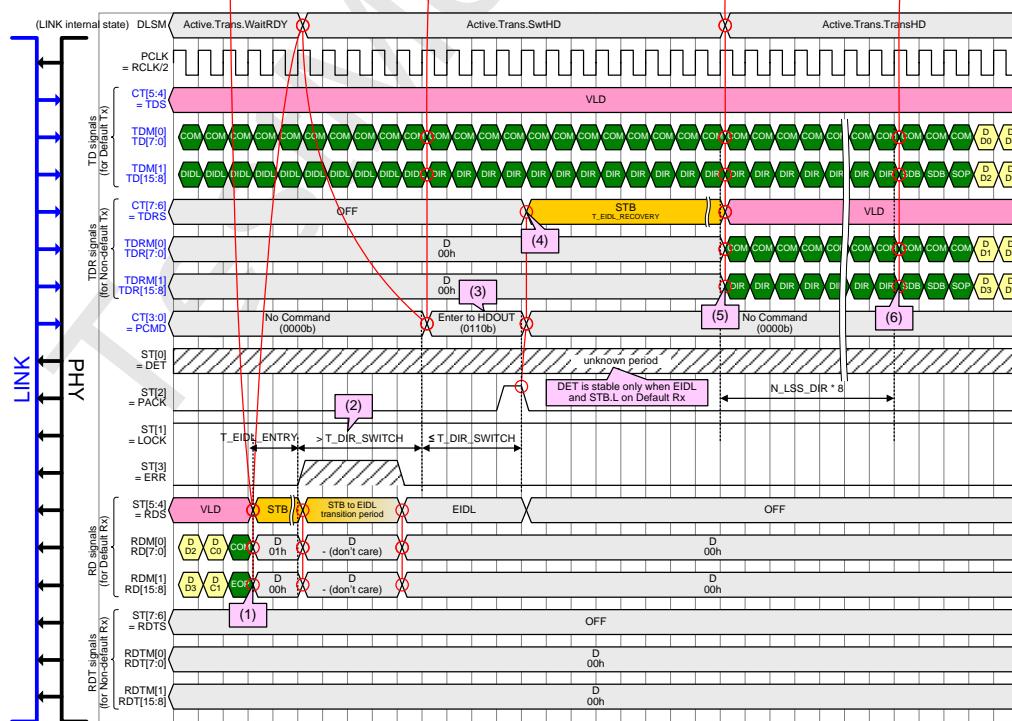
## F.4.6 Switching of Duplex Mode

Figure F- 14 illustrates the I/F timing sequence of switching from FD mode to 2L-HD mode.

### Switching from FD to HDIN Mode



### Switching from FD to HDOUT Mode



**Figure F- 14 : I/F Timing Sequence (Switching from FD to HDIN or HDOUT)**

For data receiver (Switching from FD to HDIN):

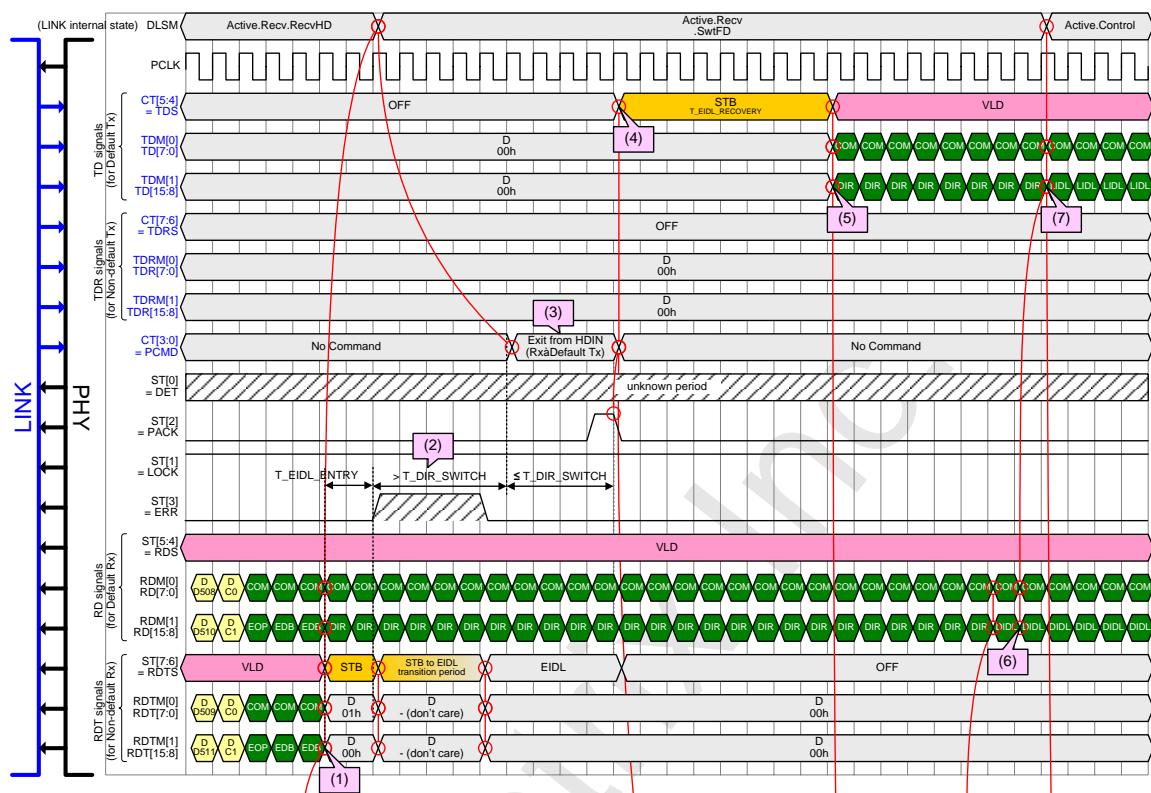
- (1) EOP of FCRDY is a trigger for direction switch
- (2) Just after transmitting FCRDY, LINK transits from Active.Control to Active.Recv.SwtHD, and it instructs PHY to start direction switch from default Tx (TD) to non-default Rx (RDT) by setting PCMD = "0101b" after transmitting STB.H for the duration of T\_EIDL\_ENTRY (= 4 SI).
- (3) PHY completes the direction switch within the period of T\_DIR\_SWITCH and notifies LINK of its completion by PACK. And the state of non-default Rx (RDTS) transits from OFF to STB to prepare for receiving valid symbols.
- (4) Non-default Rx (RDT) acquires symbol lock. LINK transits to Active.Recv.RecvHD and starts to receive DIR LSS via both data Lanes.
- (5) LINK starts to receive DATA Burst via both data Lanes.

For data initiator (Switching from FD to HDOUT):

- (1) EOP of FCRDY is a trigger for direction switch
- (2) Just after receiving FCRDY, LINK transits from Active.Trans.WaitRDY to Active.Trans.SwtHD after the duration of T\_EIDL\_ENTRY. And before starting direction switch, LINK waits for more than T\_DIR\_SWITCH to avoid a contention between both sides of Tx in a same Lane. During this period, RDS transits from STB to EIDL.
- (3) After the elapse of more than T\_DIR\_SWITCH, LINK starts to transmit DIR LSS via default Tx. LINK instructs PHY to start direction switch from default Rx (RD) to non-default Tx (TDR) by setting PCMD = "0110b". After receiving the PCMD, RDS transits to OFF.
- (4) PHY completes the direction switch within the period of T\_DIR\_SWITCH and notifies LINK of its completion by PACK. After completing direction switch, LINK instructs PHY to transmit STB.L for T\_EIDL\_RECOVERY to prepare for transmitting valid symbols.
- (5) After the elapse of T\_EIDL\_RECOVERY in STB.L, LINK transits to Active.Trans.TransHD and starts to transmit at least the predetermined number (= N\_LSS\_DIR \* 8) of DIR LSS for each Lane to acquire symbol lock.
- (6) LINK starts to transmit DATA Burst via both data Lanes.

Figure F- 15 illustrates the I/F timing sequence of switching from 2L-HD mode to FD mode.

## Switching from HDIN to FD Mode



## Switching from HDOUT to FD Mode

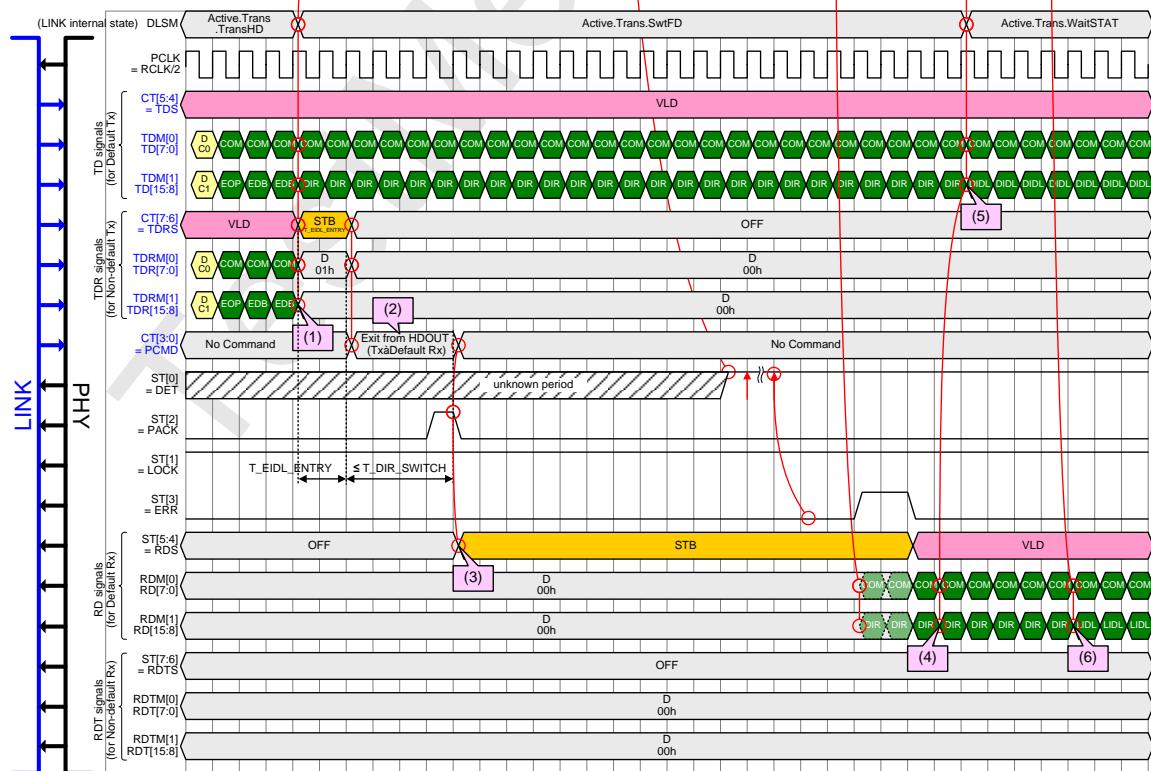


Figure F- 15 : I/F Timing Sequence (Switching from HDIN or HDOUT to FD)

For data receiver (Switching from HDIN to FD):

- (1) EDB of DATA Burst is a trigger for direction switch.
- (2) Just after receiving EDB, LINK receives DIR LSS as an in-band direction switch request and transits from Active.Recv.RecvHD to Active.Recv.SwtFD after the duration of T\_EIDL\_ENTRY (= 4 SI). In addition, before starting direction switch, LINK waits for more than T\_DIR\_SWITCH to avoid a contention between both sides of Tx in a same Lane. During this period, RDTS transits from STB to EIDL.
- (3) After the elapse of more than T\_DIR\_SWITCH, LINK instructs PHY to start direction switch from non-default Rx (RDT) to default Tx (TD) by setting PCMD = "0111b". After receiving the PCMD, RDTS transits to OFF.
- (4) PHY completes the direction switch within the period of T\_DIR\_SWITCH and notifies LINK of its completion by PACK. After completing the direction switch, LINK instructs PHY to transmit STB.L for T\_EIDL\_RECOVERY to prepare for transmitting valid symbols.
- (5) After the elapse of T\_EIDL\_RECOVERY in STB.L, LINK starts to transmit DIR LSS as an in-band direction switch acknowledge until it receives DIDL LSS.
- (6-7) After receiving DIDL via default Rx (RD), LINK transits to Active.Control and starts to transmit LIDL via default Tx (TD) in Fast Mode or EIDL in Low Power Mode.

For data initiator (Switching from HDOUT to FD):

- (1) EDB of DATA Burst is a trigger for Duplex mode switching. And LINK starts to transmit DIR LSS via default Tx (TD) as an in-band direction switch request.
- (2) Just after transmitting EDB, LINK transits from Active.Trans.TransHD to Active.Trans.SwtFD. LINK instructs PHY to start direction switch from non-default Tx (TDR) to default Rx (RD) by setting PCMD = "0111b" after transmitting STB.H for the duration of T\_EIDL\_ENTRY.
- (3) PHY completes direction switch within the period of T\_DIR\_SWITCH and notifies LINK of its completion by PACK. And the state of default Rx (RDS) transits from OFF to STB to prepare for receiving valid symbols.
- (4) Default Rx (RD) acquires symbol lock and LINK receives DIR LSS as an in-band direction switch acknowledgement.
- (5) After completing DIR handshake, LINK transits to Active.Trans.WaitSTAT and starts to transmit DIDL LSS until it receives STAT MSG.
- (6) After transmitting DIDL LSS, LINK receives LIDL in Fast Mode or EIDL in Low Power Mode.

## F.4.7 Entering to Dormant State

Figure F- 16 illustrates the I/F timing sequence of entering to Dormant state. Refer to Section 5.4.3 for details of Dormant state entry.

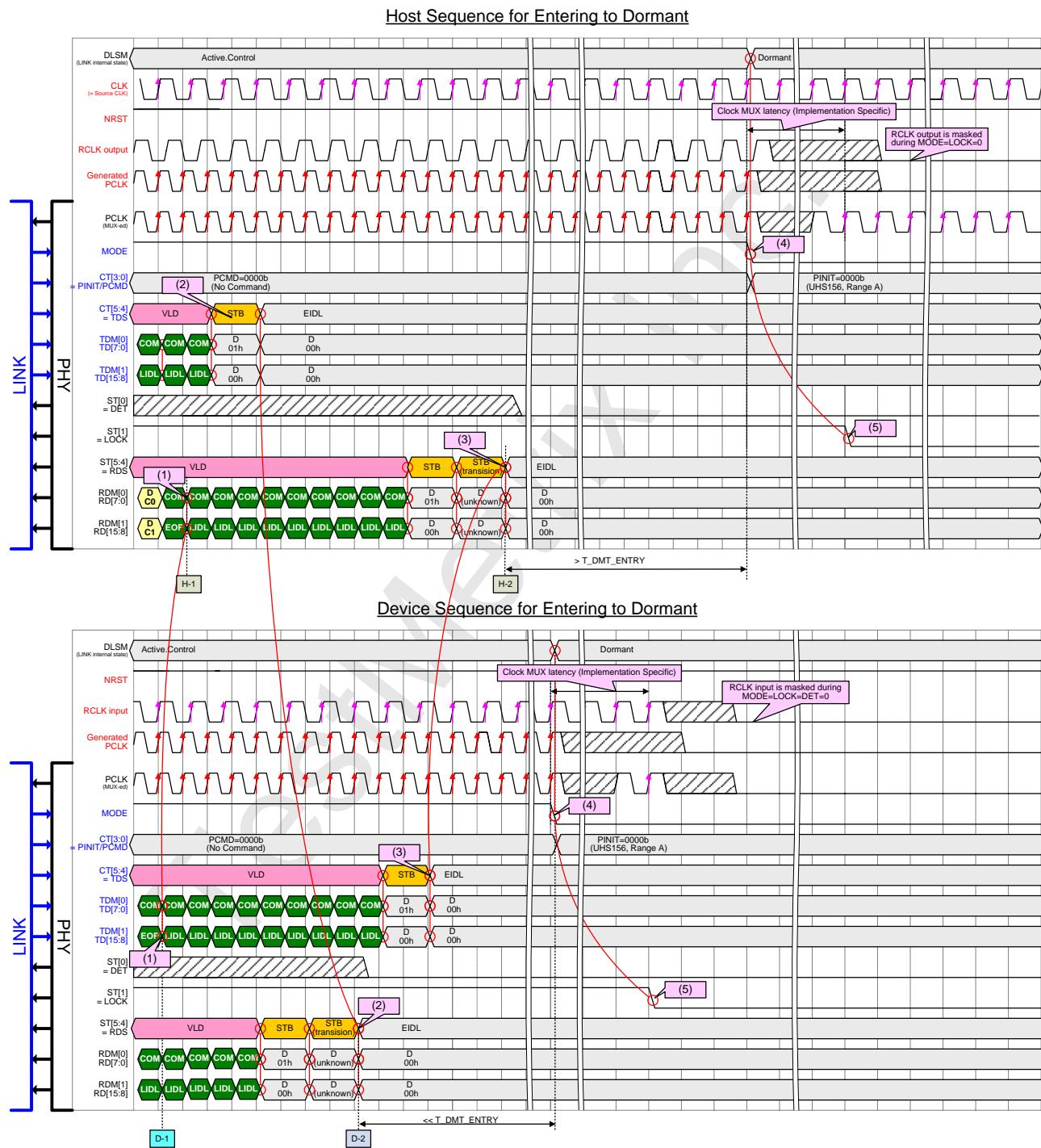


Figure F- 16 : I/F Timing Sequence (Entering to Dormant State)

For Host:

- (1) Host receives GO\_DORMANT\_STATE CCMD issued from Device (Condition H-1).
- (2) Host sets its TDS to STB and TD to 0001h respectively. Then Host sets its TDS to EIDL.
- (3) RDS of Host becomes EIDL (Condition H-2). Then both Condition H-1 and H-2 are satisfied.
- (4) After the elapse of more than T\_DMT\_ENTRY from the time detecting EIDL on RDS (Condition H-2), Host instructs its PHY to enter to Dormant state by negating MODE signal. And Host PHY starts to switch PCLK from generated one to CLK (source clock).
- (5) When PCLK is certainly switched, Host PHY negates LOCK signal and stops RCLK distribution to Device(s). Note that RCLK output is supposed to be masked when LOCK = 0.

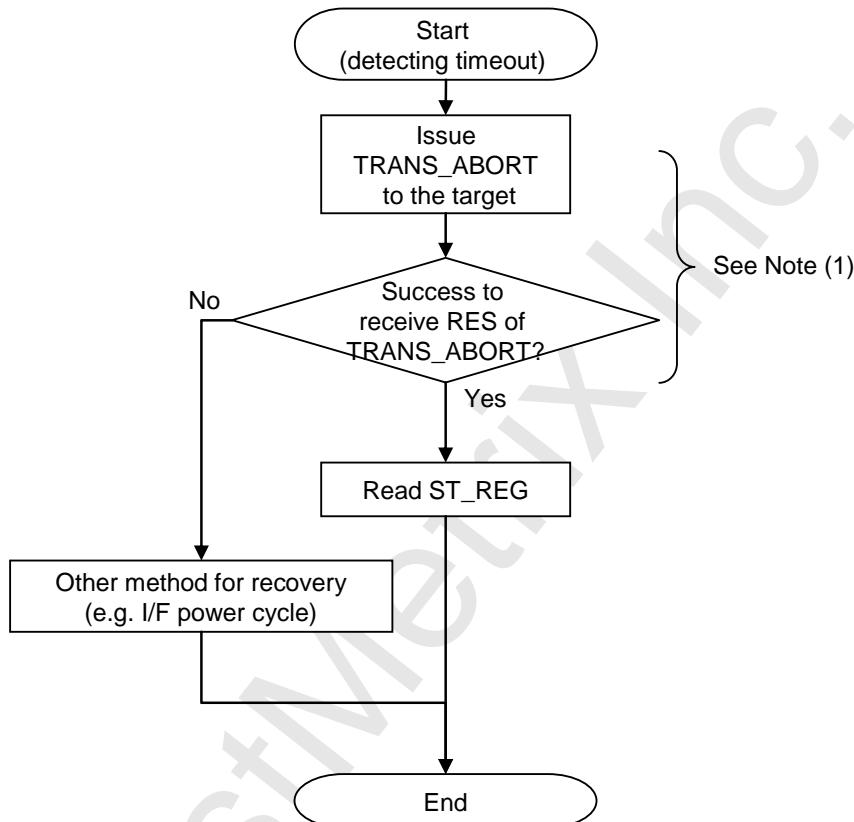
For Device:

- (1) Device transmits GO\_DORMANT\_STATE CCMD (Condition D-1).
- (2) RDS of Device becomes EIDL (Condition D-2). Then both Condition D-1 and D-2 are satisfied.
- (3) Device sets its TDS to STB and TD to 0001h respectively. Then Device sets its TDS to EIDL.
- (4) After the elapse of sufficiently less than T\_DMT\_ENTRY from the timing detecting EIDL on RDS (Condition D-2), Device instructs its PHY to enter to Dormant state by negating MODE signal to avoid an unexpected stop of RCLK distribution from Host. And Device PHY starts to switch PCLK from generated one to received RCLK.
- (5) When PCLK is certainly switched, Device PHY negates LOCK signal and stops RCLK input. Note that RCLK input is supposed to be enabled with the signal generated by (DET || MODE || LOCK).

## Appendix G (Informative) : Host's Operation in Detecting Timeout

### G.1 P2P CMD of UHS-II Native Protocol

Figure G- 1 illustrates Host's operation when it detects timeout in case of P2P CMD for UHS-II native protocol.



Note:

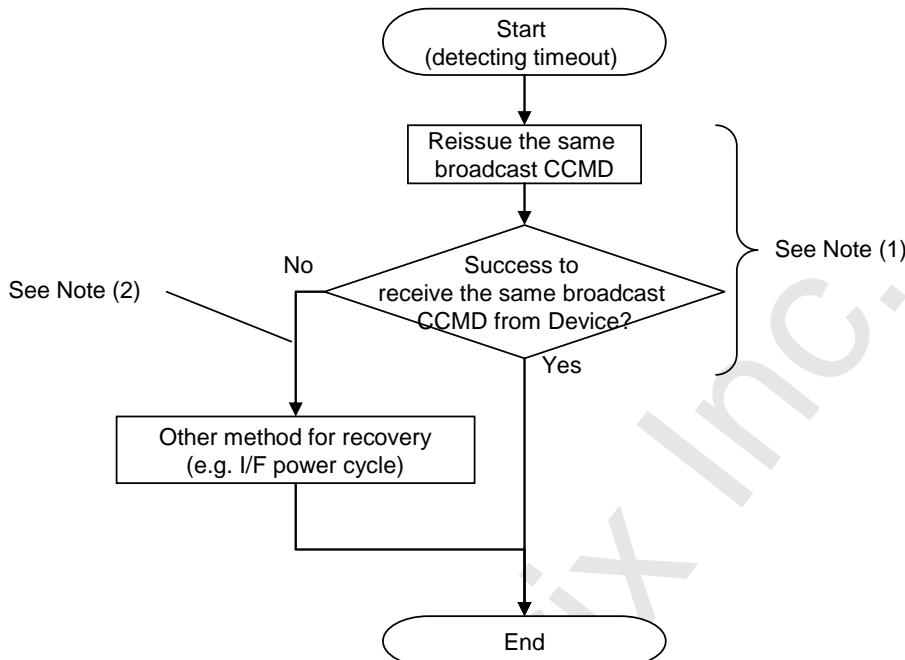
- (1) Host can repeat to issue TRANS\_ABORT when it detects timeout again.
- (2) Host can issue TRANS\_ABORT for all connected Devices for debugging.
- (3) Error identifiers in the intermediate Device are cleared if it responds to the P2P commands other than TRANS\_ABORT.

**Figure G- 1 : Host's Operation for Timeout in Case of P2P CMD for UHS-II Native Protocol**

When Host detects timeout, Host should issue TRANS\_ABORT CCMD to terminate the outstanding transaction. If it succeeds to receive RES of TRANS\_ABORT, it should read error identifiers and status of Device indicated in Device's ST\_REG.

## G.2 Broadcast CCMD

Figure G- 2 illustrates Host's operation when it detects timeout in case of Broadcast CCMD.



Note:

- (1) Host can repeat to issue the same broadcast CCMD when it detects timeout again.
- (2) Host can issue TRANS\_ABORT for all connected Devices for debugging before other method for recovery.

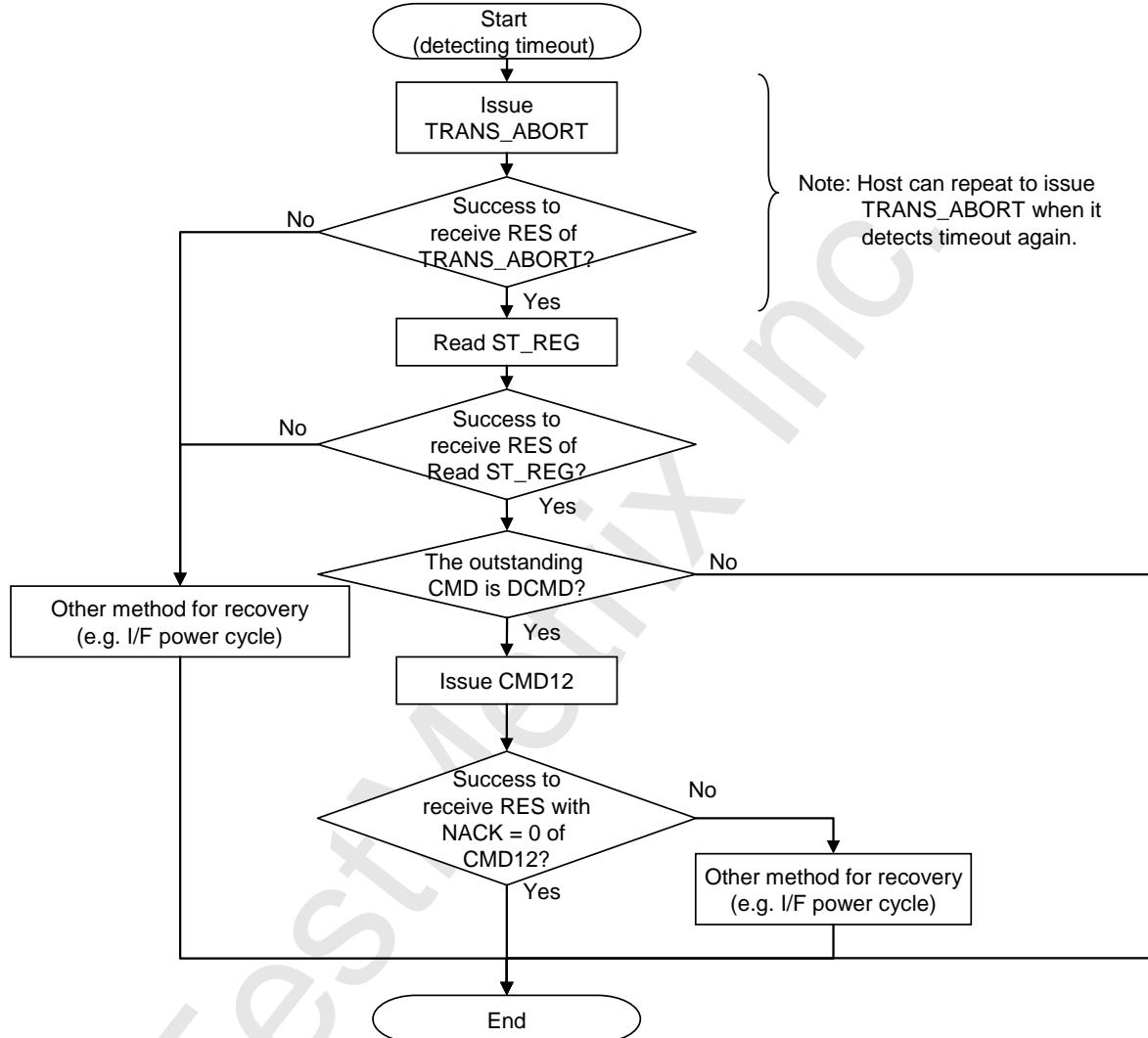
**Figure G- 2 : Host's Operation for Timeout in Case of Broadcast CCMD**

Different from the case of P2P CMD, Host also detects timeout when the broadcast CCMD includes COND\_ERR, ARG\_ERR, or GEN\_ERROR described in Table 6-4. This is because Device does not transmit the broadcast CCMD any more when it detects at least one of these errors.

Therefore, Host should reissue the same broadcast CCMD to recover from the illegal situation. If Host can receive the RES after some times trial, it can make judgment that the system recovers from the illegal situation. Note that in case of FULL\_RESET CCMD and GO\_DORMANT\_STATE CCMD, another method for recovery should be used instead of issuing retry command. Host should execute power cycle if FULL\_RESET sequence is not completed.

### G.3 CMD of SD-TRAN

Figure G- 3 illustrates Host's operation when it detects timeout in case of CMD for SD-TRAN. Note that the encapsulated CMD12 is required when Host detects timeout during data transaction.



**Figure G- 3 : Host's Operation for Timeout in Case of SD-TRAN**