TESTMETRIX

UHS-II Protocol & Performance Tests

Ver 0.1a

- Preliminary -

Note: This document defines the UHS-II Protocol and Performance tests to be implemented on the VTE-4100 tester.

Introduction:

The VTE-4100 Protocol / Performance tests will be executed by the TP (MBLZ) under the control of a VTE test script. The communication between the VTE and the TP will be performed via the TPCP protocol. Each test item will be given a Test Number. The test script running on the VTE-4100 application will call for individual tests to be executed by the TP (will provide required test data via TPCP). Upon completion of the test the TP will return the results to the VTE via TPCP.

UHS-II Protocol Tests

The list and description of the Protocol Tests are contained in the document SDA spec:

Part 1 UHS-II Protocol Test Guidelines Ver 1.00 Final 140714.pdf

This document organizes tests in 6 groups.

1 Systems Tests

1-1 Interface Speed Test (FD Mode)
1-3 Interface Speed Test (2L-HD mode)
1-5 Direction of D0 and D1
1-6 Direction of D0 and D1 on 2L-HD mode write
1-7 Direction of D0 and D1 on 2L-HD mode read
1-9 Block Mode and Byte Mode
1-11 Device operation before completing Device Initialization without Boot Code Loading
1-13 Device operation after completing Boot Code Loading

2 Link Layer Tests

2-1 Number of SYN LSS:
2-3 Initial Value of Node ID of Device
2-4 SID and DID fields in Header of Boot Device before Enumeration
….
2-64 Valid Transmission Gap in Active Stream

3 CM-Tran Layer Tests

4 SD-Tran Tests

5 2L-HD Mode Tests

6 Additional Lanes Tests

7 Custom Tests

UHS-II Test Sequence

The numbering and nomenclature used in this document should be used for reference also in the tests implemented on the VTE-4100 tester. Given that the numbering in the spec is counterintuitive it should be used in parenthesis, the actual order of the tests being determined in a logical fashion based on the typical flow of operations executed by real UHS-II devices:

1. PHY Initialization Tests:

   COM + SYN Activation
   COM + BSYN activation (Boot Code Loading Sequence)

2. Link Layer Tests:

   Wake-Up Test
   Link Layer Tests 2.1 – 2.64

3. Configuration Tests:

   Device_Init test
   Enumeration Test
   Checking Capabilities Registers
   - Inquiry_Config
   - P2P Read CCMD

   Writing Setting Registers
   - Set_COMMON_CONFIG
   - P2P Write CCMD

4. Operations in Active State:

   Update Settings Registers
   CM - Tran Tests (3.1-3.93)
   - 3.22 Data Transaction
   - Read Performance Test
   - Write Performance Test

   SD – Tran Tests (4.1-4.43)
   - CMD0/CMD8/CMD55/ACMC41

5. 2L-HD Tests

6. Additional Lanes Tests

7. Custom Tests

Note: Items in yellow were already preliminary implemented and tested
Items in green are top priority