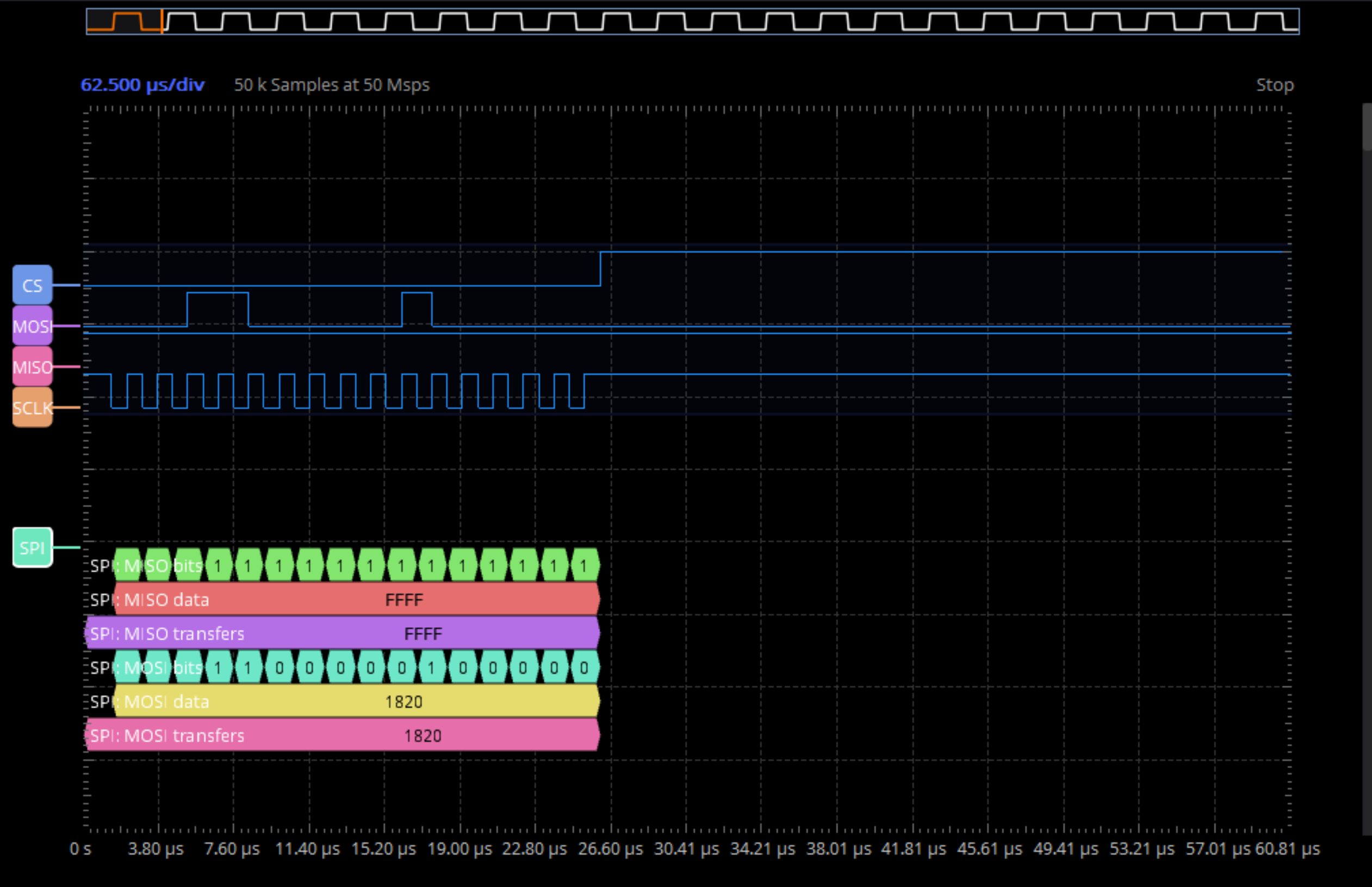
ad5592r\_reg\_write(dev, *AD5592R\_REG\_CTRL*, 0x20) ­



AD5592R\_REG\_CTRL = 0x3h

b0 to b3 reserved

b4 = 0 => DAC output range is 0 to V\_ref

b5 = 1 => ADC gain is 0 to 2xV\_ref (NOT DEFAULT!!)

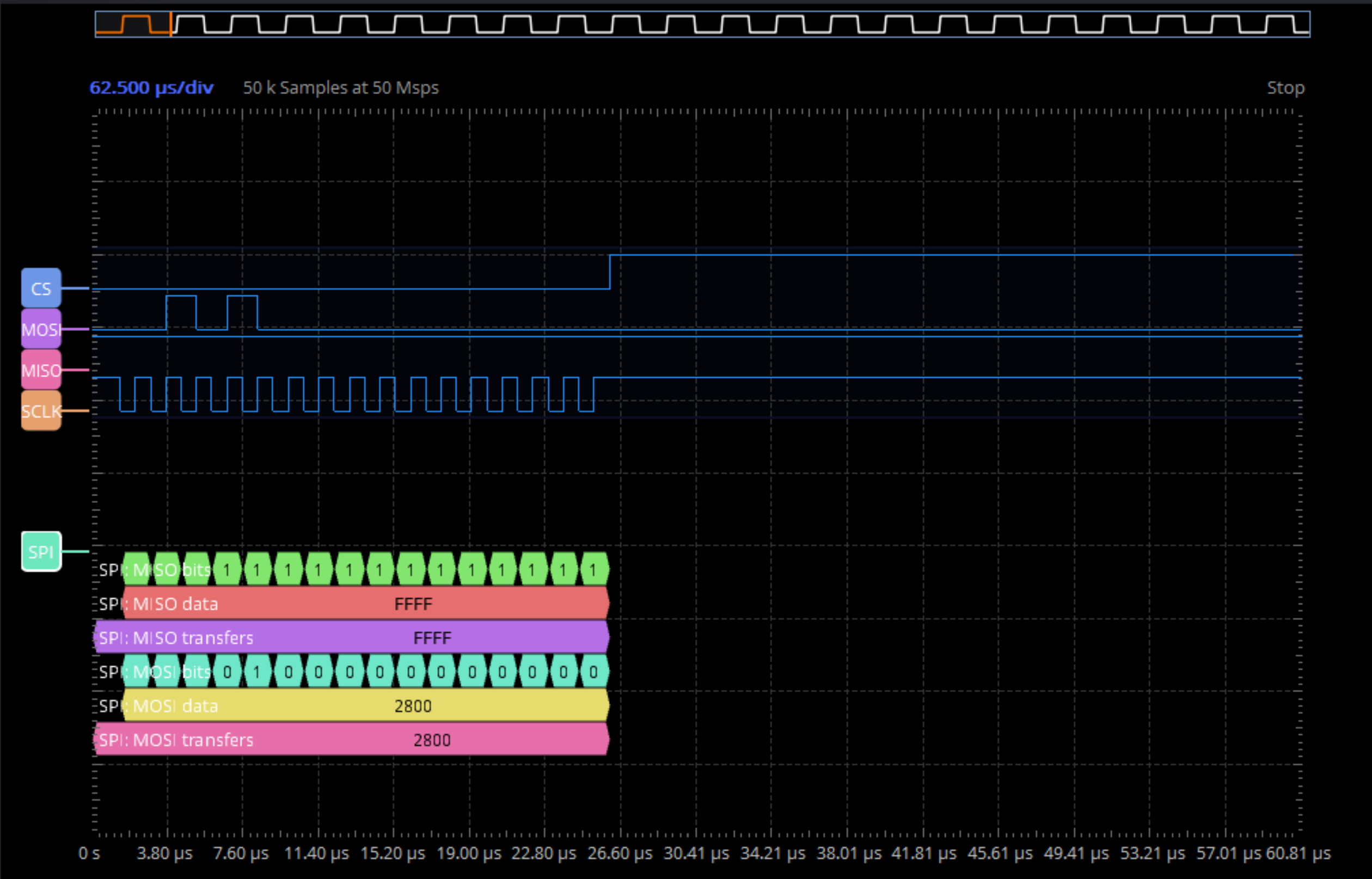
b6 = 0 => for future DAC writes, the DAC addres bits determine which DAC is written to

b7 = 0 => the contents of the I/O\_x pin configuration register can be changed

b8 = 0 => ADC buffer is disabled

b9 = 0 => ADC buffer is not used to precharge the adc

ad5592r\_reg\_write(dev, *AD5592R\_REG\_DAC\_EN*, 0x0);

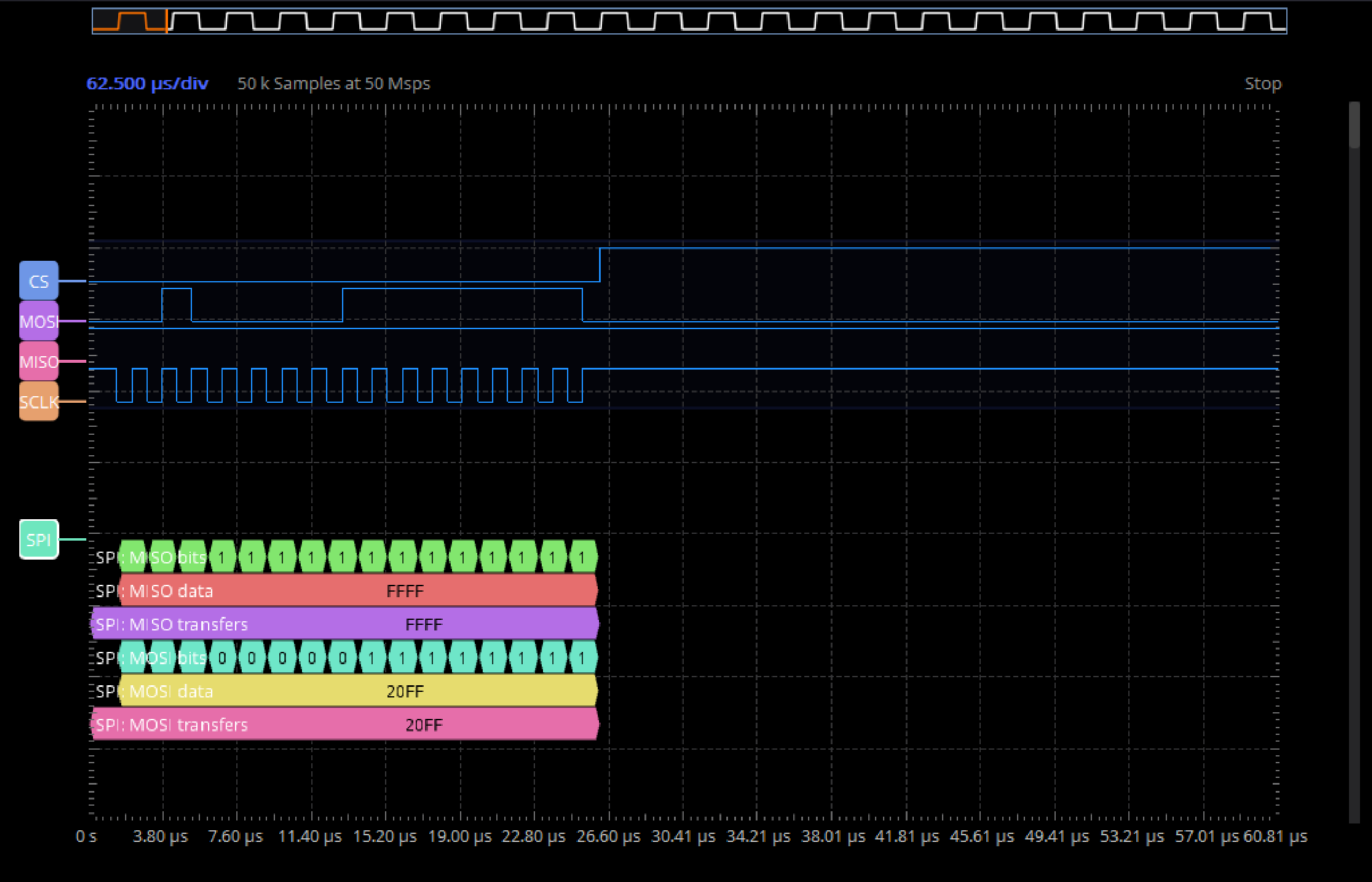


AD5592R\_REG\_DAC\_EN = 0x5h

B9=1 => selects the I/O pin 7 as output

B7 to B0 = 00h => the I/O pin function is determined by the pin configuration registers

ad5592r\_reg\_write(dev, *AD5592R\_REG\_ADC\_EN*, 0xff);

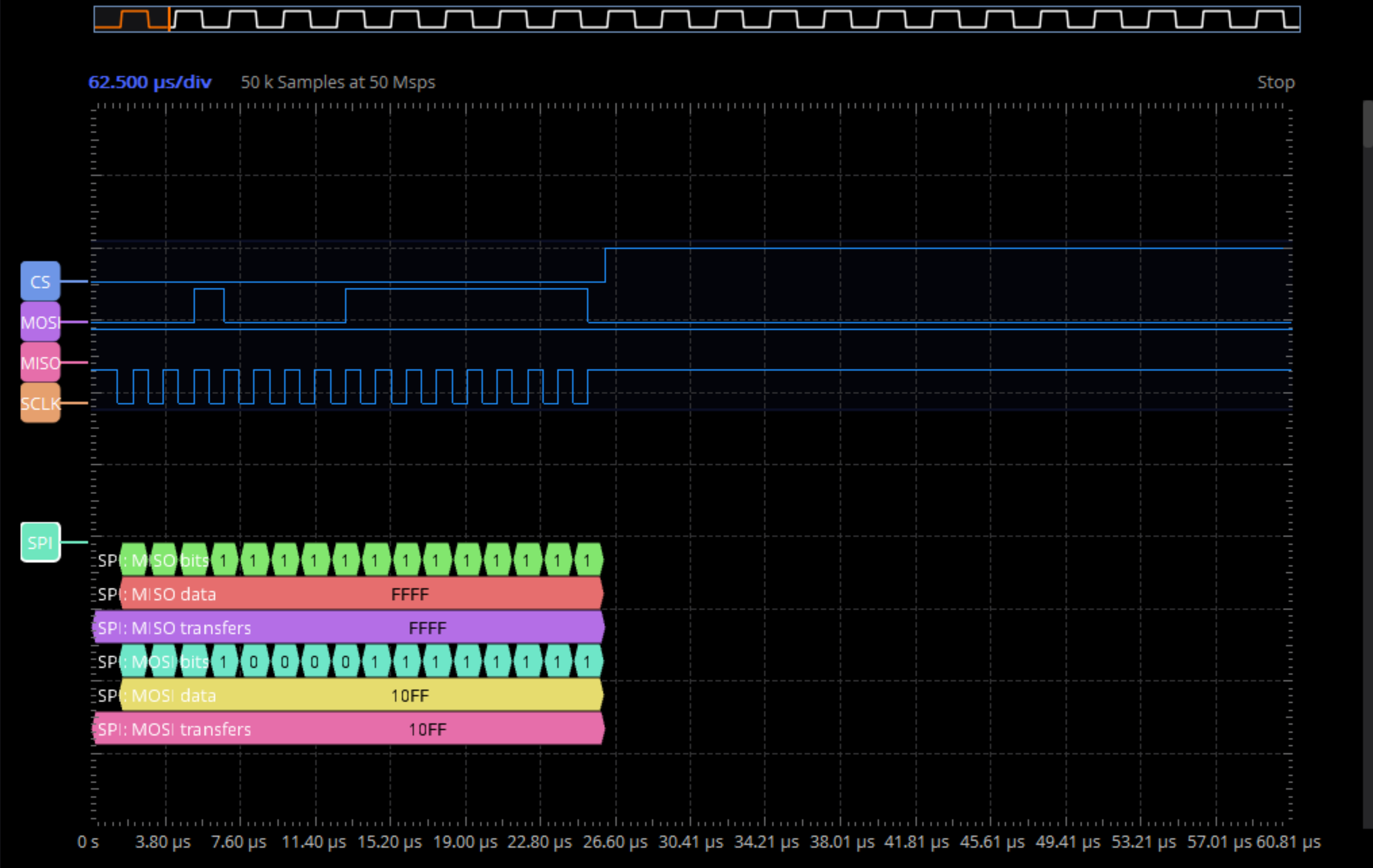


*Asta e configuration register*

*AD5592R\_REG\_ADC\_EN* = 0x4

B7…B0 = ffh => selects I/O pins 7 to 0 as ADC input

ad5592r\_reg\_write(dev, *AD5592R\_REG\_ADC\_SEQ*, 0xff);



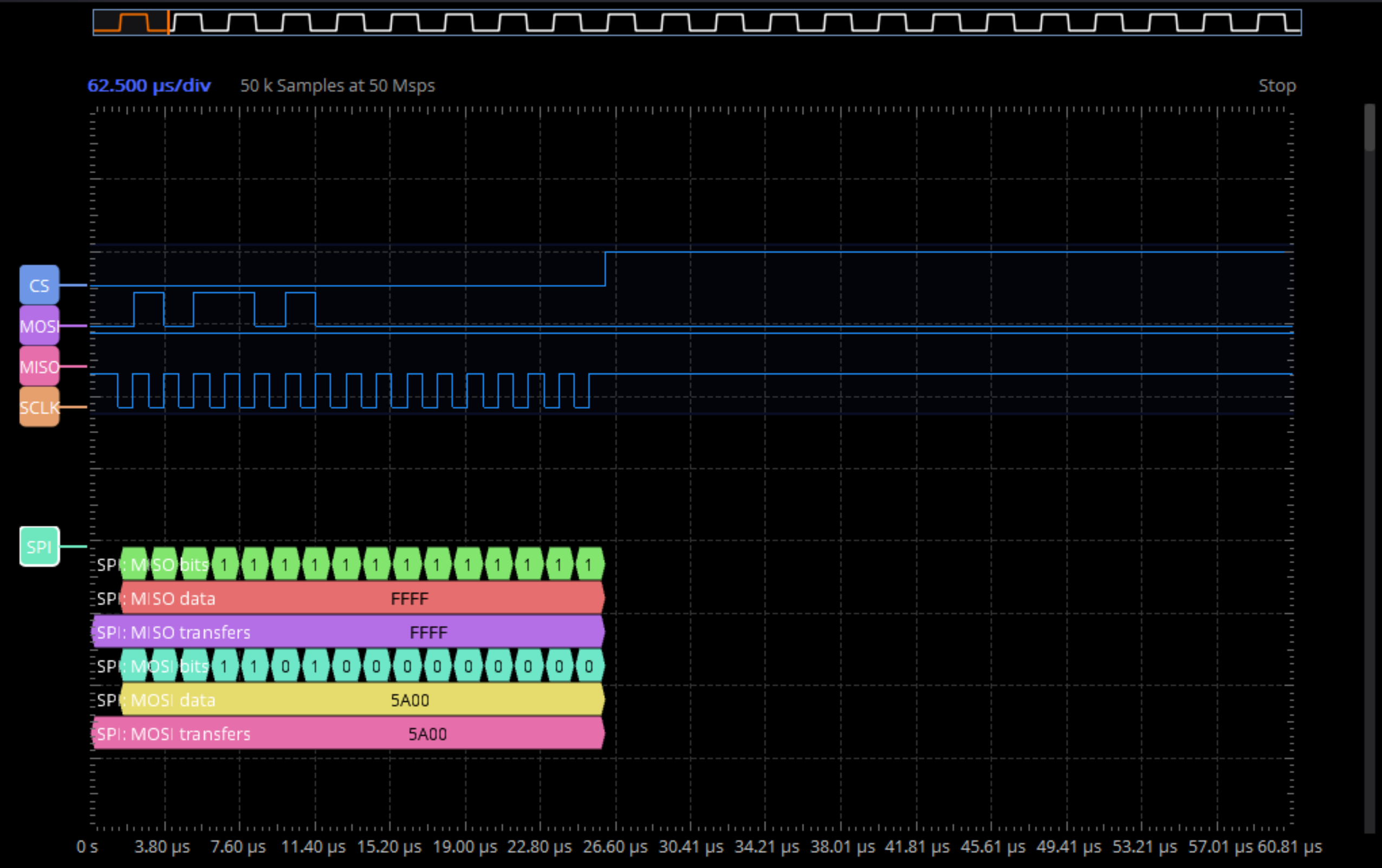
*AD5592R\_REG\_ADC\_SEQ* = 0x2,

B7…B0 = ffh => includes ADC channels 7 to 0 in conversion sequence

B8 = 0 => Disable temperature indicator readback.

B9 = 0 => Sequence repetition disabled

ad5592r\_reg\_write(dev, *AD5592R\_REG\_PD*, 0x200);



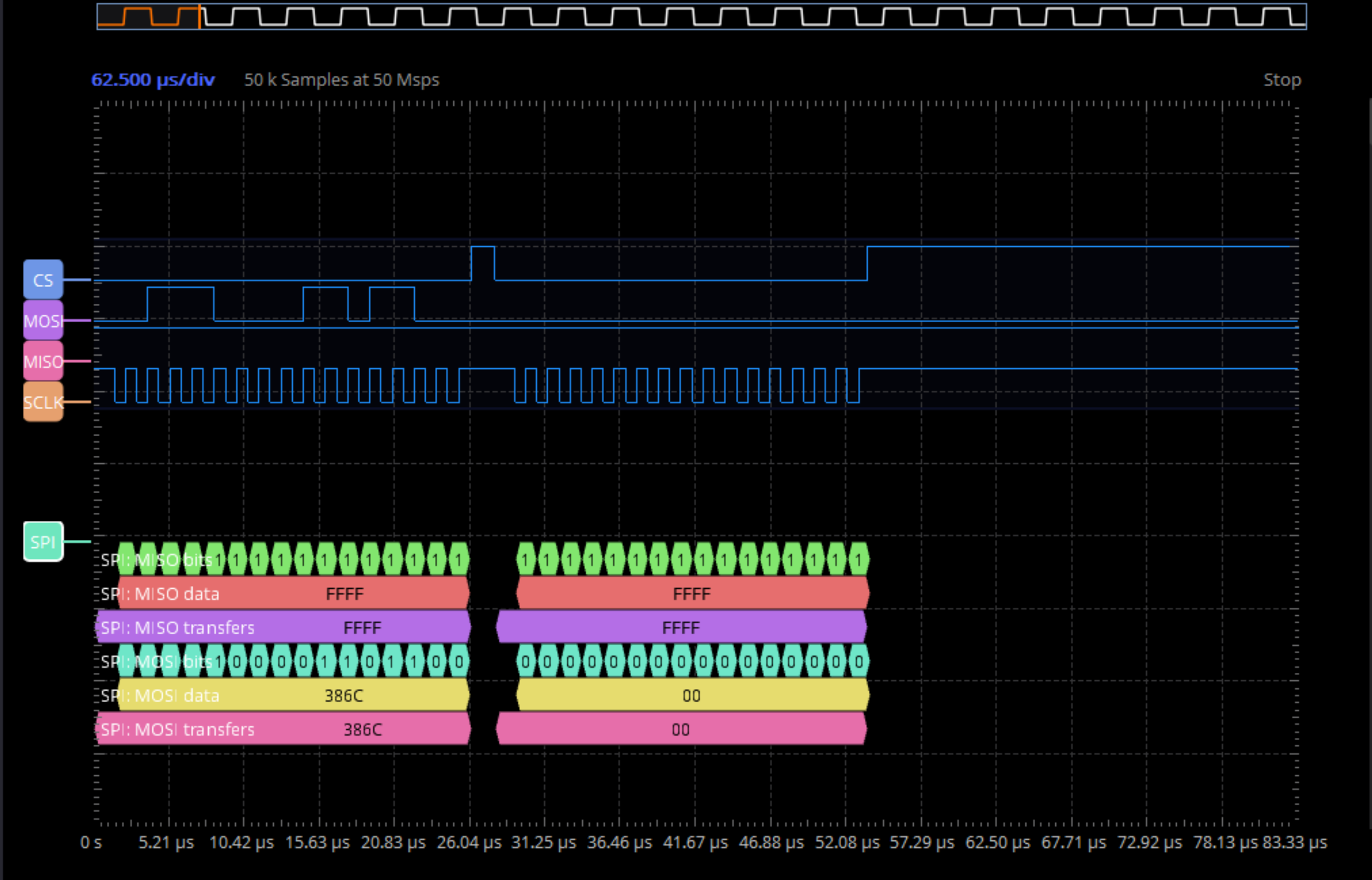
*AD5592R\_REG\_PD* = 0xB

B7…B0 = 00h => channels 7 to 0 operate in normal mode

B9 = 1 => the reference and it’s buffer are powered up

B10 = 0 => the reference and DACs power down states are determined by EN\_REF and PD7 to PD0 bits.

ad5592r\_reg\_read(dev, *AD5592R\_REG\_PD*,&temp\_reg\_val);



*AD5592R\_REG\_PD* = 0xB

The second transaction is a noop