Lab 6: Introduction to FPGA

Backgorund

- Watch this video

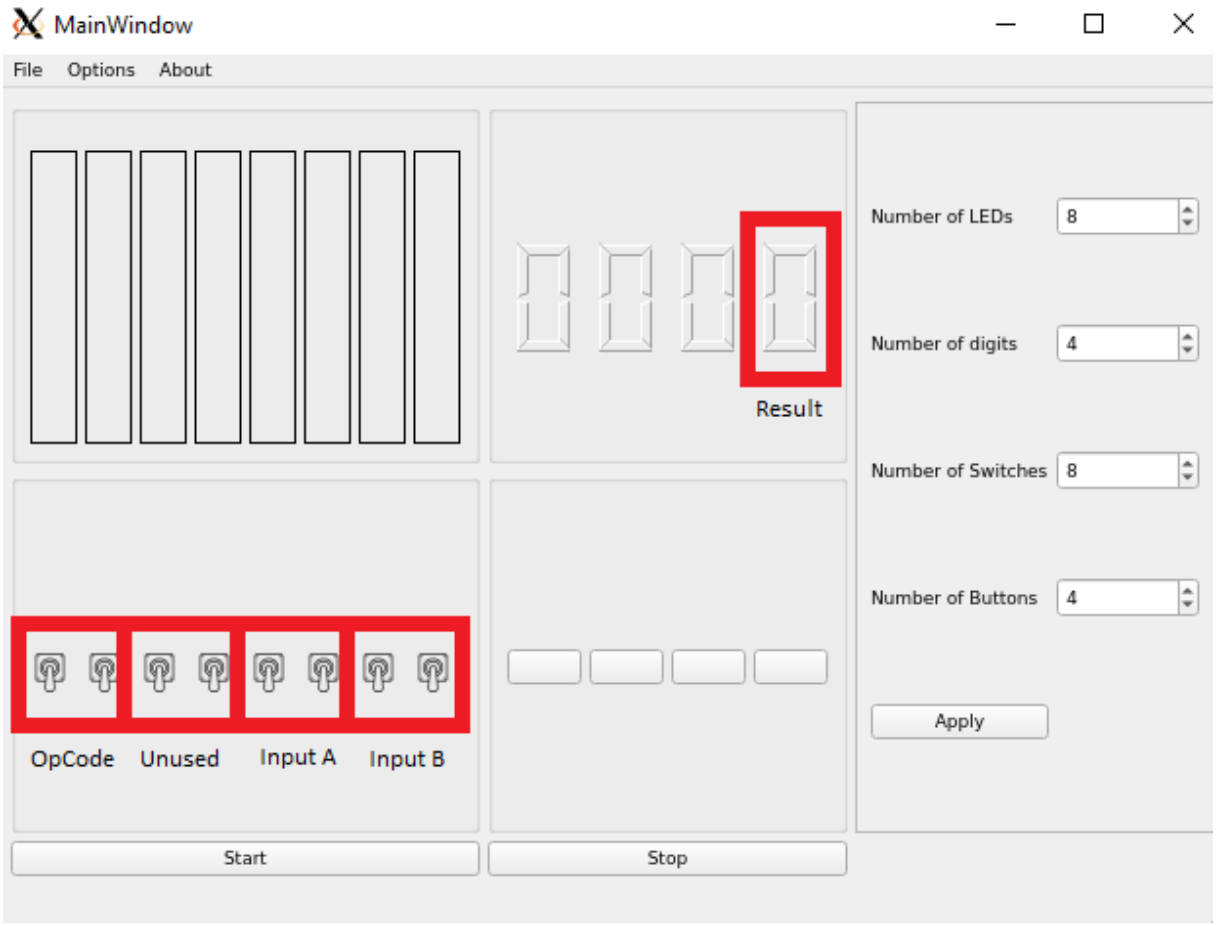
Part 1 – SevenSegment Driver Modification

1. Open VirtualFPGA.
2. Click Open. Add fourDigitSevenSegment Verilog file using the “Add” button.
3. Add the given top wrapper file to the top wrapper section using the “Browse” button.
4. Click “Done”. Then on the main page press “Start”.
5. See how the design works by switching on/off switches on the FPGA and review sevenSegment Verilog and top wrapper files.
6. Modify the Seven Segment design so that it can display between 0-15 instead of 0-3. You need to use hexadecimal representation, ie. 10 = A, 11 = B … (You may find seven segment datasheet on last page)
7. Run the modified module on VirtualFPGA.
8. Synthesize your design and take a screenshot of ISE with the warnings tab open.

Part 2 – Introduction to CPU design

We will design a processor capable of 4 different operations. These operations are addition, subtraction, multiplication and bitwise or. Switches and seven segment on the FPGA board will be used. The specifications of the design are given below.

- Since it can execute 4 operations, operation code is a 2 bit number.
    - 0: addition
    - 1: subtraction
    - 2: multiplication
    - 3: bitwise or operation
- Input numbers A and B are also 2 bit numbers.
- The leftmost two of the 8 switches on the board indicate the operation, the rightmost two is the number A, and next two represents B number. Check below image.

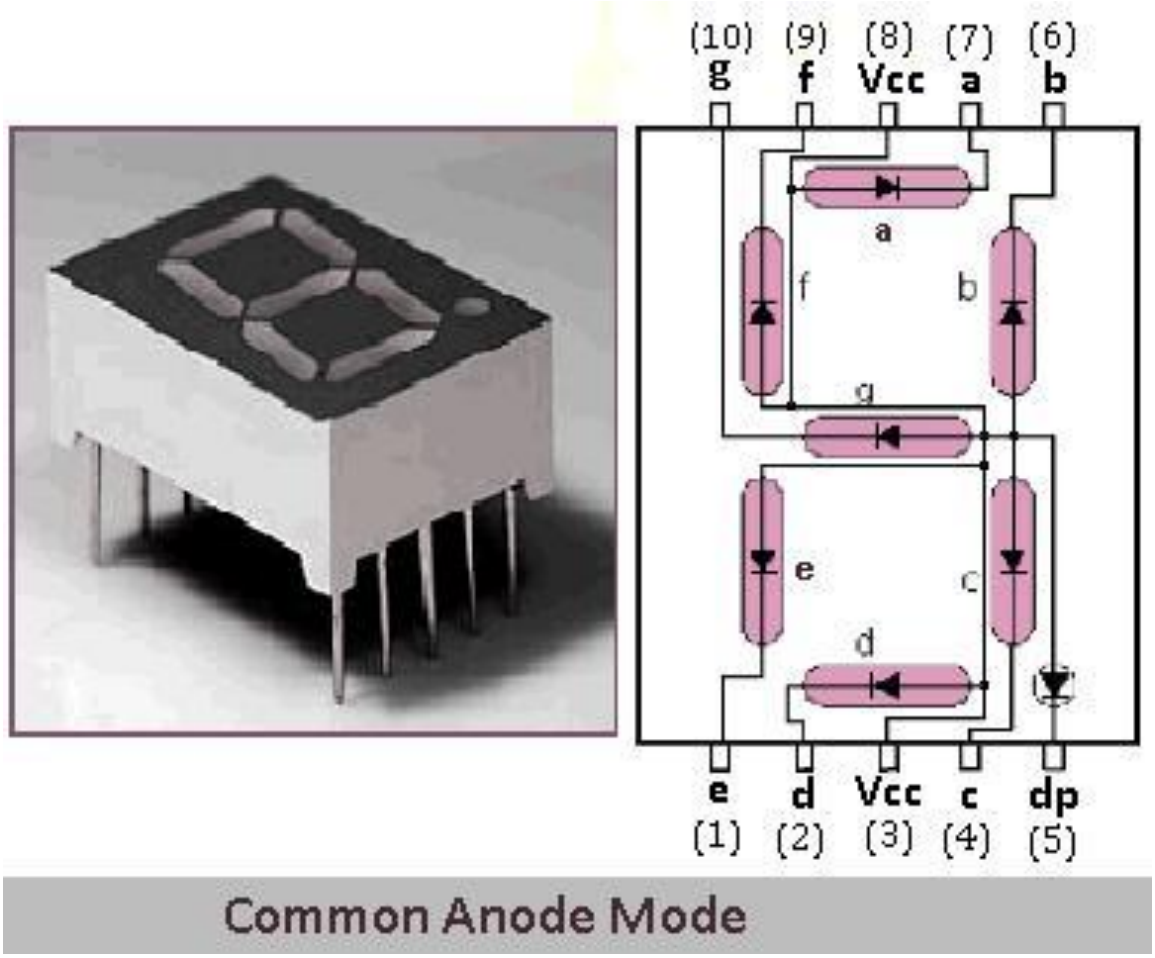


1. Download cpuSevenSegment.v and top_wrapper_cpuSevenSegment.v
2. Fill the missing design parts in cpuSevenSegment.
3. Add cpuSevenSegment.v to project. Add top_wrapper_cpuSevenSegment.v as top wrapper.
4. Run your project.
5. Synthesize your design and take a screenshot of ISE with the warnings tab open.

Submission

- Submit the following files in LMS under the assignment LAB06. Do not zip your files, upload them directly on LMS!
  - fourDigitSevenSegment.v
  - cpuSevenSegment
  - fourDigitSevenSegment.png
  - cpuSevenSegment.png

Common Anode Seven Segment



Common Anode Mode