Lab 7: Calculator

Part 1 – Calculator Implementation

0. Please go to LMS and download calc.v, calc_tb.v, calc.pdf, data, and result files.
1. https://ozu.cloud.panopto.eu/Panopto/Pages/Viewer.aspx?id=2f1c7dcb-f0d2-4d56-ad65-ad14010b3b9f
0. Watch the video linked above up to 12 minutes.
1. Create new project in Xilinx ISE Design Suite and add copy of source project files.
2. Modify your calc.v file as required.
3. Synthesize your design. Make sure your design has no errors or warnings except trivial warning.
4. Take a screenshot of the whole screen with the warnings window open.

Part 2 – Calculator Synthesize and Simulation

0. https://ozu.cloud.panopto.eu/Panopto/Pages/Viewer.aspx?id=2f1c7dcb-f0d2-4d56-ad65-ad14010b3b9f
1. Watch the rest of the video in the link.
2. Data and result files should be copied into the Xilinx project folder.
3. Simulate your design on Xilinx ISE. Make sure your design has no errors in simulation.
4. Take a screenshot of the whole screen with the console window showing the test results.
5. Open Virtual FPGA and add calc.v and top_wrapper files.
6. As you can see in the top_wrapper_calc.v file, reset and validIn buttons are declared as btn[0] and btn[1] respectively.
7. Run the simulation. Check if any of the operations are not working correctly. Correct them if needed.

Submisson: Do not change ".v" file names and do not zip your files. Just submit calc.v and screenshots of synthesis and simulation results.