Lab 10: VSCPU

Part 1 – Completing VSCPU Instruction Set

0. Go to LMS and download InstructionSet.jpg and InstructionSet_README.txt, SRL.jpg and BZJ.jpg
1. Read VerySimpleCPU instruction set again and comprehend it.

Part 2 – VSCPU whole Instruction Set Synthesis and Simulation

0. Watch this video link here: https://ozu.cloud.panopto.eu/Panopto/Pages/Viewer.aspx?id=bbede735-5e27-4ed8-8619-ad3000ef3bad
1. Please go to LMS and download blram.v, program.v, SimpleCPU.v, SimpleCPU_tb.v, and test.asm files.
2. program.v automatically will be included. Do not add manually on ISE. Just add blram.v, SimpleCPU.v and SimpleCPU_tb.v.
3. In the initial design, logic is able to execute BZJi and ADD operations. A logic must be written to execute the test.asm code given to you. Complete all Instruction Set.
4. Modify your SimpleCPU.v file as required.
5. Synthesize and Simulate your design. Be sure your design has no error and warning except trivial warning at synthesis. Also, your design should have no error at simulation part.

Submisson: Do not change .v file names and do not zip your files. Just submit SimpleCPU.v!