Lab 9: VSCPU

Part 1 – Introduction to VerySimpleCPU Design

Please go to:

0. https://ozu.cloud.panopto.eu/Panopto/Pages/Viewer.aspx?id=398ed085-130a-4b0c-9bb8-ad2a00fbf604
1. Watch the video link above up to 11:00.
2. Go to LMS and download Lab 9 documents.
3. Read VerySimpleCPU instruction set again and comprehend it.

Part 2 – VerySimpleCPU Synthesis and Simulation with BZJ and ADD instructions

0. Please go to VerilogTB/lab9_part2 folder and see that you have blram.v, data.v, VSCPU.v, VSCPU_tb.v, and lab9_part2.asm files.
1. https://ozu.cloud.panopto.eu/Panopto/Pages/Viewer.aspx?id=398ed085-130a-4b0c-9bb8-ad2a00fbf604
2. Watch the video link above.
3. data.v automatically will be included. Do not add manually on ISE. Just add blram.v, VSCPU.v and VSCPU_tb.v.
4. In the initial design, logic is able to execute BZJi and ADD operations. A logic must be written to execute the lab9_part2.asm code given below. Add the missing ADDi and BZJ instructions to the VSCPU.v.

```
0: ADD 10 15
1: ADDi 10 20
2: BZJ 3 5
3: 7
5: 0
7: BZJ 3 10
8: BZJi 9 0
9: 8
10: 0
15: 2
20: 3
```

5. Modify your VSCPU.v file as required.
6. Synthesize and Simulate your design. Be sure your design has no error and warning except trivial warning at synthesis. (Note that you will get delay warnings and "(*) More than 100% of Device resources are used" warning). Also, your design should have no error at simulation part.

Part 3 – VerySimpleCPU Synthesis and Simulation with CP and CPi instructions

0. Go into the data.asm file and VSCPU_tb.v file and change the code to the files provided in VerilogTB/lab9_part3 folder.

1. Now your VSCPU design should have ADD, ADDi, BZJ, BZJi instructions implemented. A logic must be written to execute the lab9_part3.asm code given below. Add the missing CP and CPi instructions to the VSCPU.v.

```
0: ADD 12 15
1: ADDi 12 20
2: BZJ 3 5
3: 7
5: 0
7: BZJ 3 12
8: CP 40 50
9: CPi 100 20
10: BZJi 11 0
11: 10
12: 0
15: 2
20: 3
50: 100
100: 200
```

2. Modify your VSCPU.v file as required.

3. Synthesize and Simulate your design. Be sure your design has no error and warning except trivial warning at synthesis. (Note that you will get delay warnings and "(*) More than 100% of Device resources are used" warning). Also, your design should have no error at simulation part.

Submission

- Submit your final VSCPU.v in LMS under the assignment LAB9. Do not zip your file, upload them directly on LMS.