

8.13)

Page size 2KB = 2048 bytes $\Rightarrow 2^{11}$ bytes

a) A conventional, single-level page table

Number of virtual pages = (total virtual memory/page size)

Total addressable virtual memory is 2^{21} bytes

Number of virtual pages $\Rightarrow 2^{21} / 2^{11} \Rightarrow 2^{10} = 1024$ pages

b) An inverted page table

Number of physical frames = (total physical memory/page size)

Total addressable physical memory is 2^{16} bytes

Number of physical frames $\Rightarrow 2^{16} / 2^{11} \Rightarrow 2^5 = 32$ pages

8.16)

Logical address: 32-bit

Page Size = 4KB = 4096 bytes = 2^{12} bytes

Physical memory = 512 MB $\Rightarrow 512 * 2^{20}$ bytes $\Rightarrow 2^{29}$ bytes

a) A conventional, single-level page table

Number of virtual pages = (total virtual memory/page size)

Number of virtual pages $\Rightarrow 2^{32} / 2^{12} \Rightarrow 2^{20}$ pages

b) An inverted page table

Number of physical frames = (total physical memory/page size)

Number of physical frames $\Rightarrow 2^{29} / 2^{12} \Rightarrow 2^{17}$ pages

8.17

a) Paged Memory Reference without TLB

Since each memory access takes 50 nanoseconds, the total time for a paged memory reference would be:

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Total Memory Reference Time=(Time for Page Table Access+Time for Data Access)

Total Memory Reference Time= 50 ns + 50 ns = 100 ns

b) Paged Memory Reference with TLB

TLB Hit Rate: 75% = 0.75

TLB Miss Rate: 25% = 0.25

Effective Memory Reference Time=>

(Time for TLB Hit Scenario* TLB Hit Rate) + (Time for TLB Miss Scenario * TLB Miss Rate)

Time for TLB Hit Scenario = Time to Check TLB+Time for Data Access=>

Time for TLB Hit Scenario = 2 ns + 50 ns = 52 ns

Time for TLB Miss Scenario =>

Time to Check TLB+Time for Page Table Access+Time for Data Access

Time for TLB Miss Scenario = 2 ns + 50 ns + 50 ns = 102 ns

Effective Memory Reference Time=> $52 * 0.75 + 102 * 0.25 = 64.5$ ns

8.20)

a) Logical Address: (0, 430)

Segment: 0

Base: 219

Offset: 430

Length: 600

Since the offset 430 is less than the length 600, this is a valid address.

Physical Address: Base + Offset = 219 + 430 = 649

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b) Logical Address: (1, 10)

Segment: 1

Base: 2300

Offset: 10

Length: 14

The offset 10 is less than the length 14, so this is also valid.

Physical Address: $\text{Base} + \text{Offset} = 2300 + 10 = 2310$

c) Logical Address: (2, 500)

Segment: 2

Base: 90

Offset: 500

Length: 100

The offset 500 is greater than the length 100, making this an invalid address. In typical systems, this would result in a segmentation fault or similar error.

Physical Address: Invalid (offset exceeds segment length)

d) Logical Address: (3, 400)

Segment: 3

Base: 1327

Offset: 400

Length: 580

The offset 400 is less than the length 580, so this is valid.

Physical Address: $\text{Base} + \text{Offset} = 1327 + 400 = 1727$

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e) Logical Address: (4, 112)

Segment: 4

Base: 1952

Offset: 112

Length: 96

The offset 112 is greater than the length 96, another invalid address scenario.

Physical Address: Invalid (offset exceeds segment length)