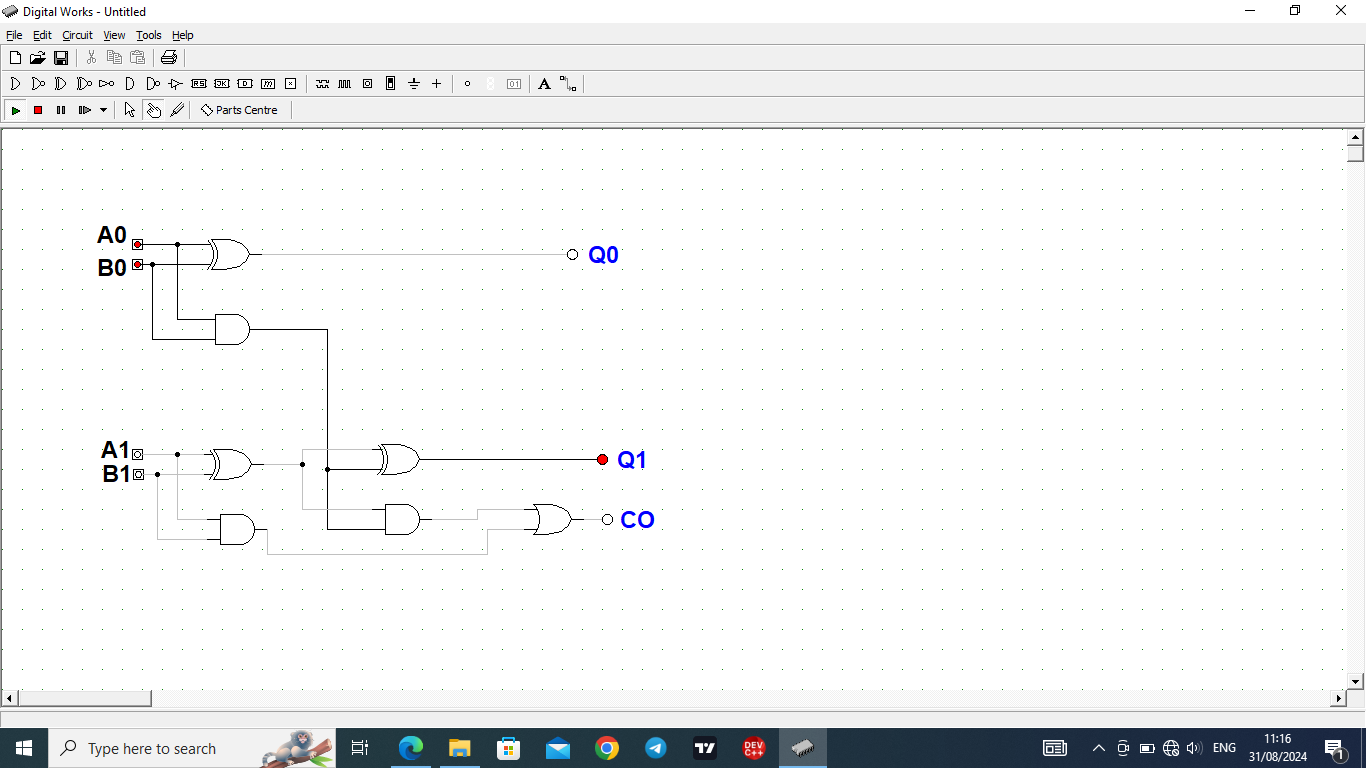
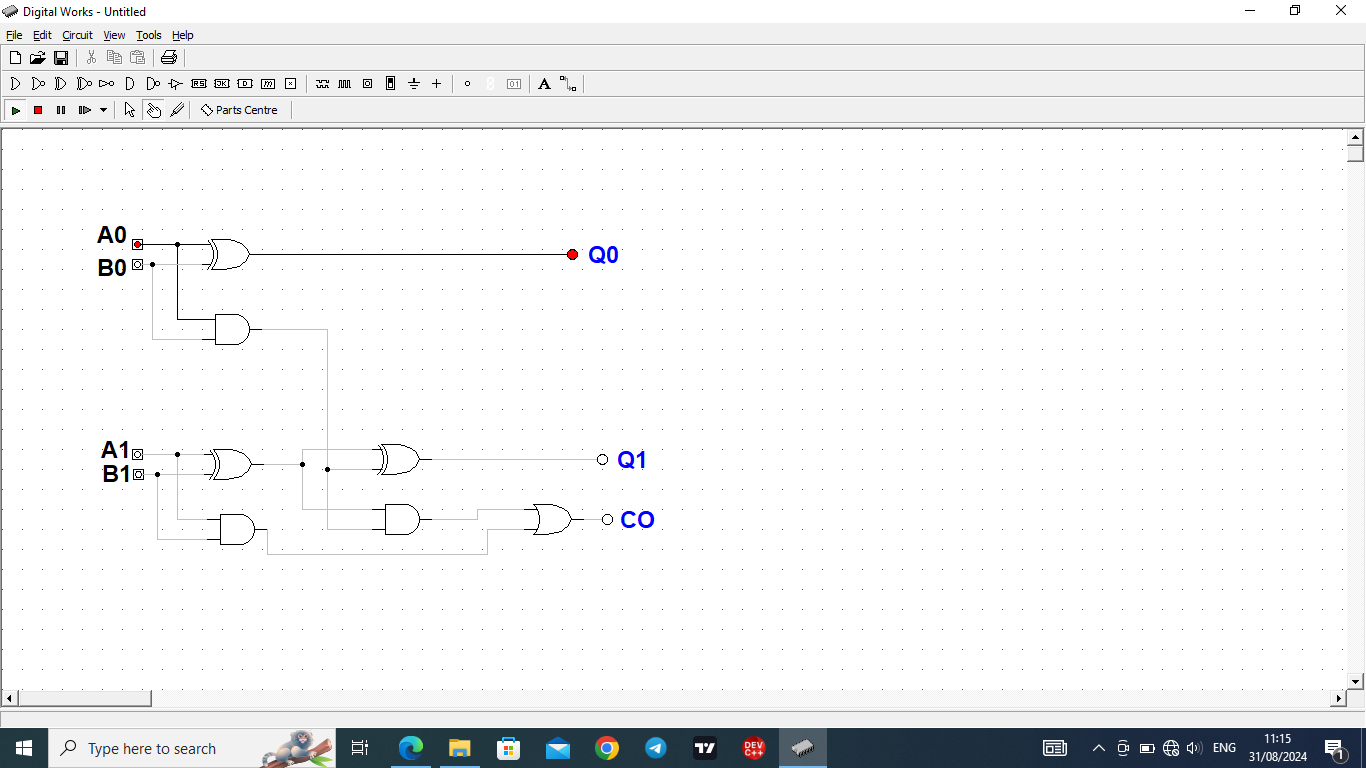
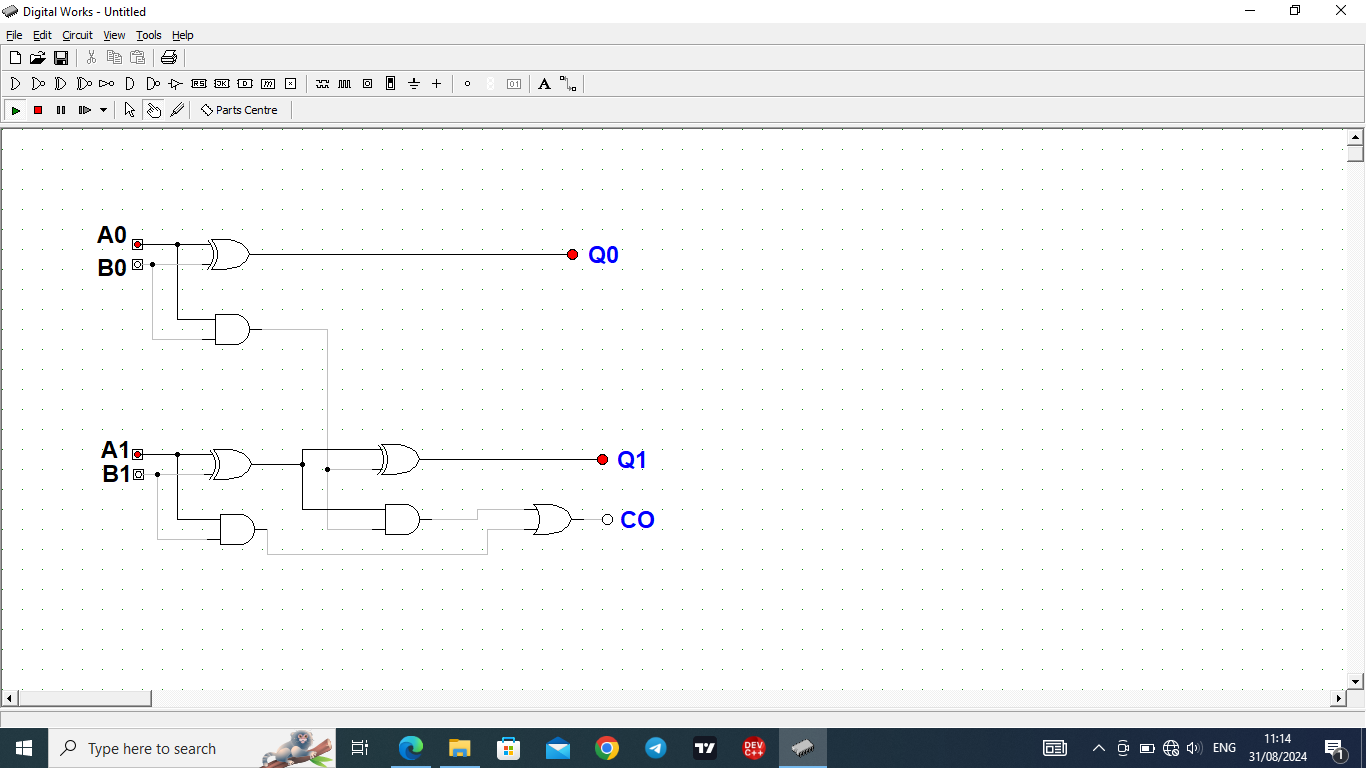
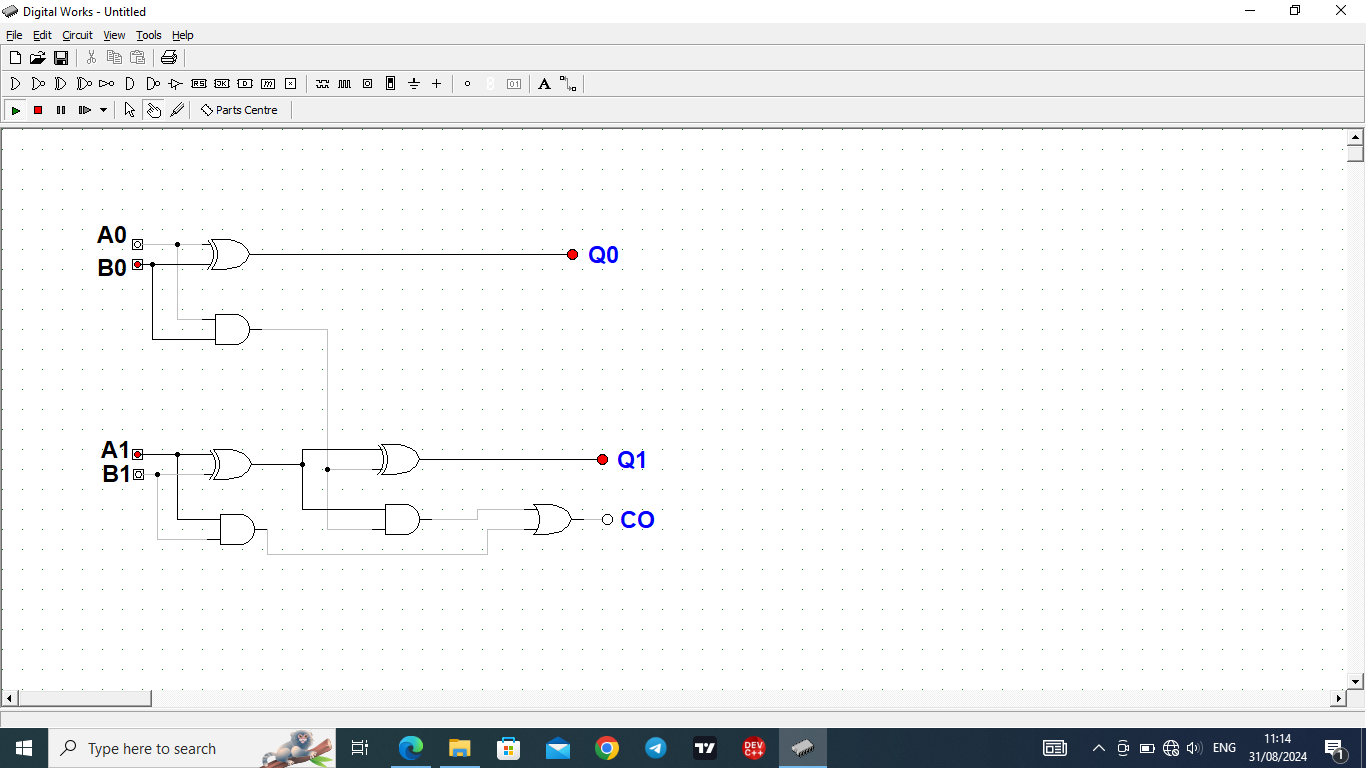
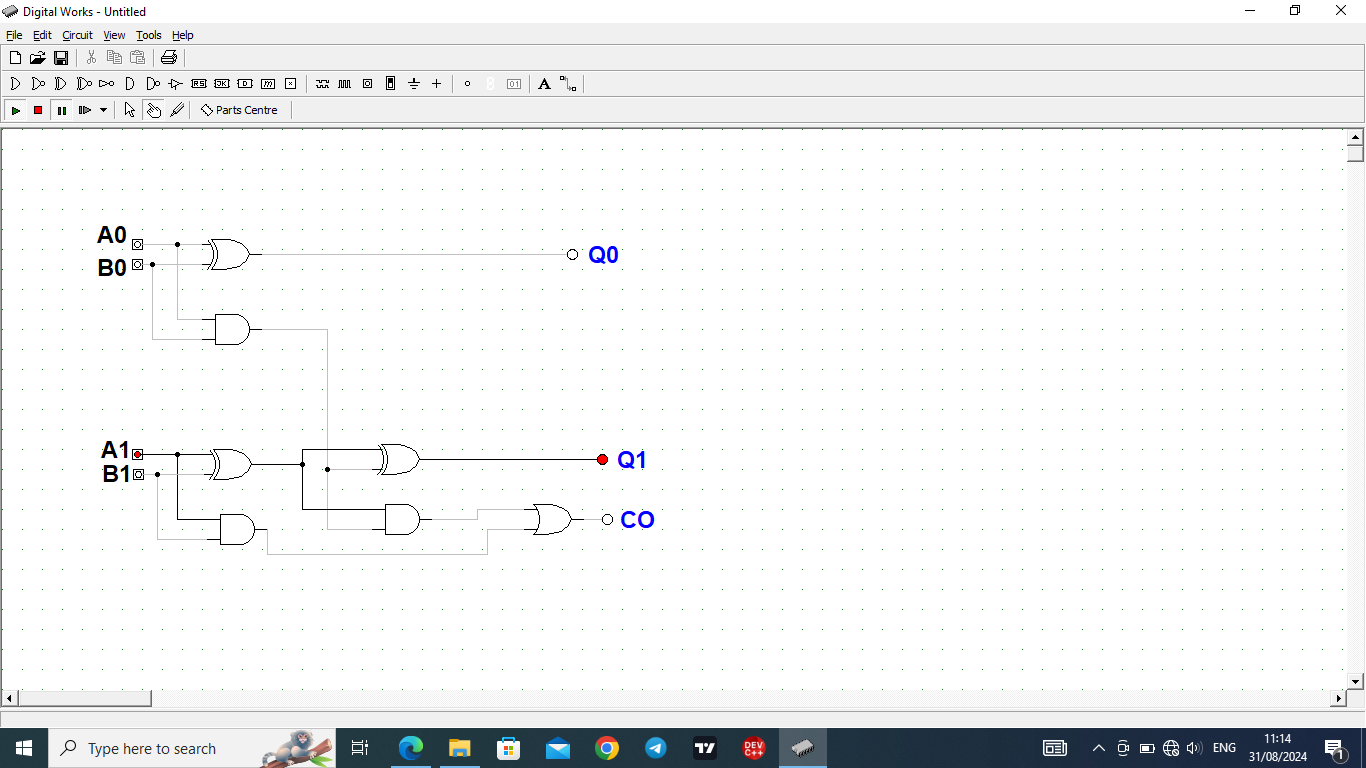
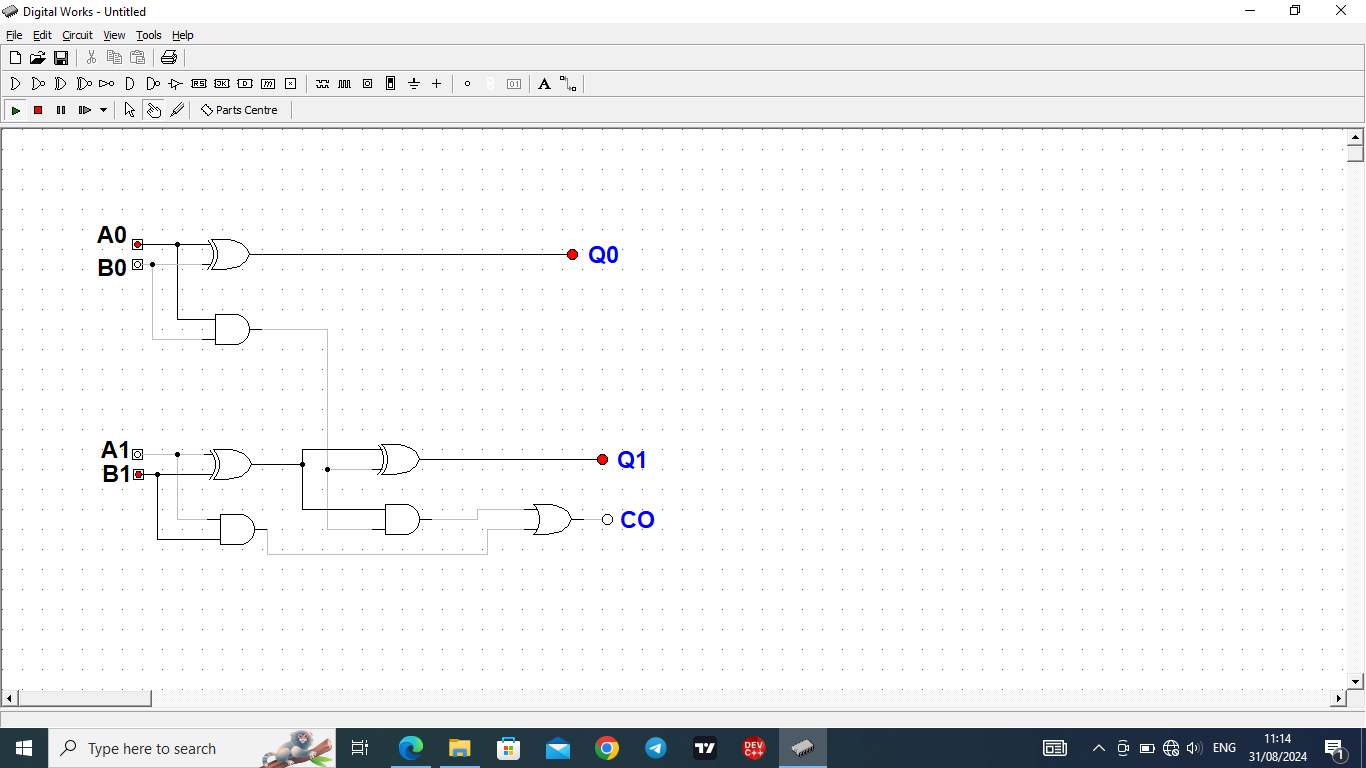
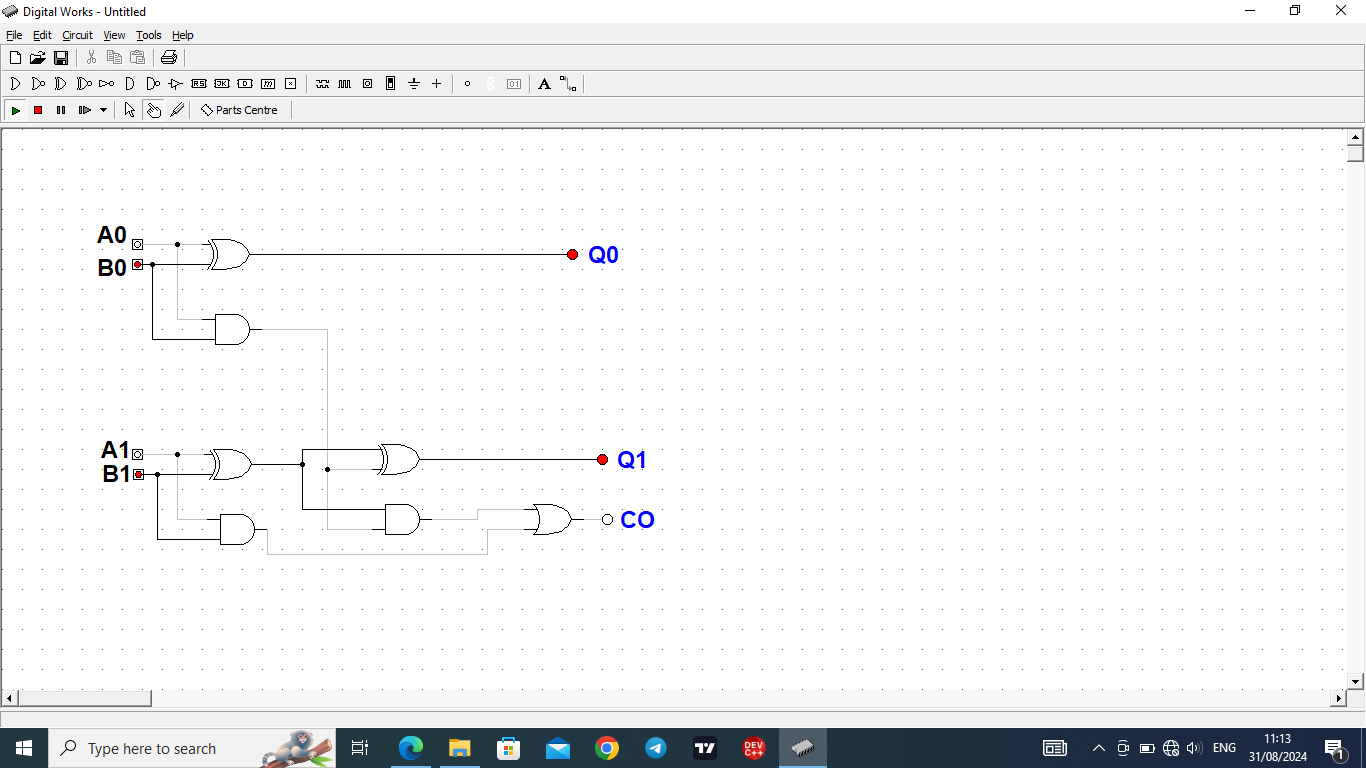
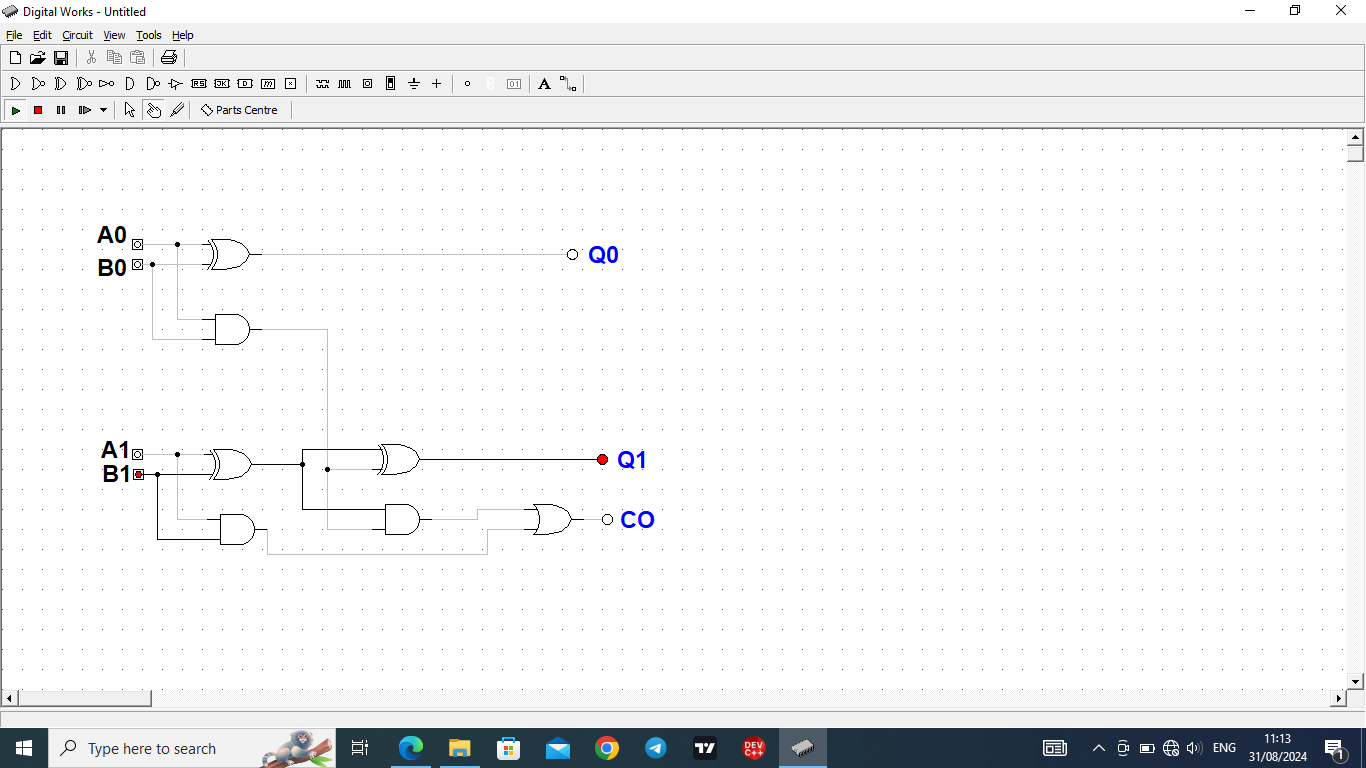
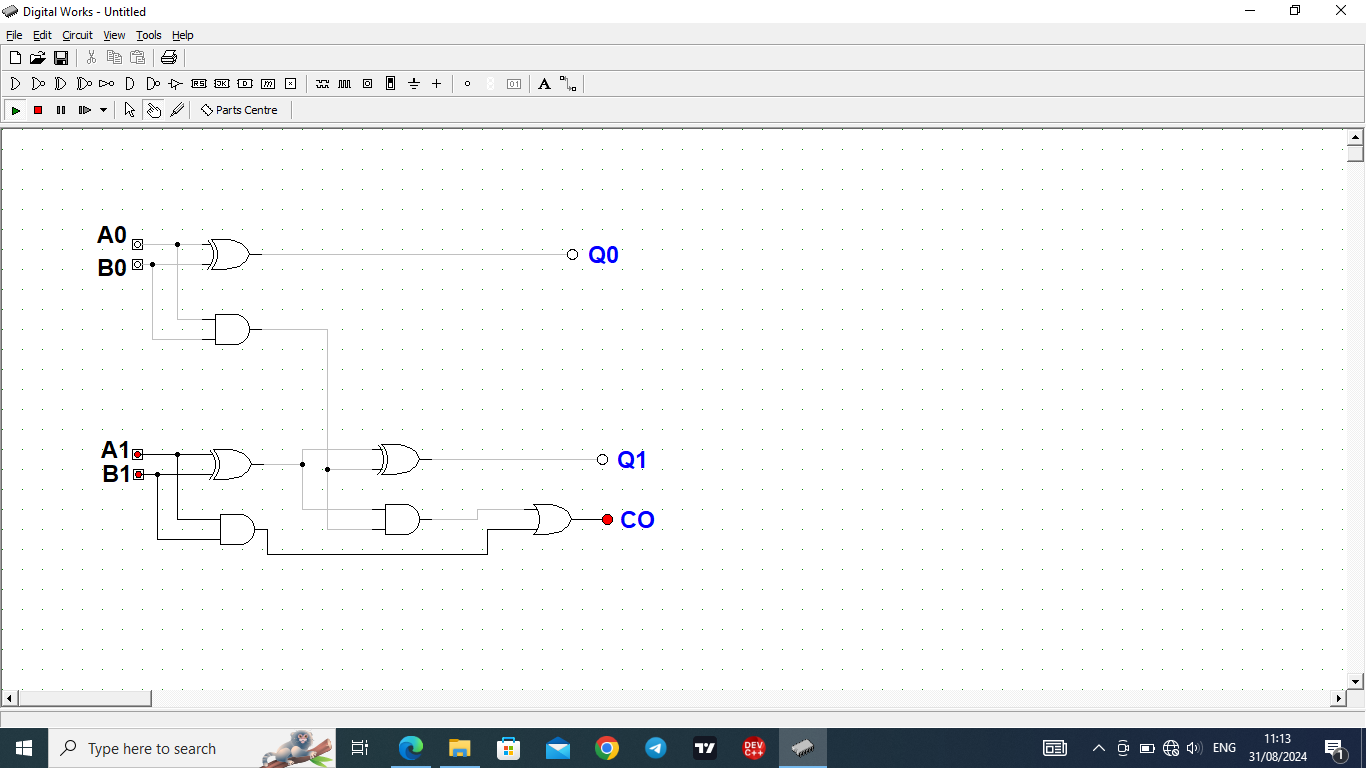
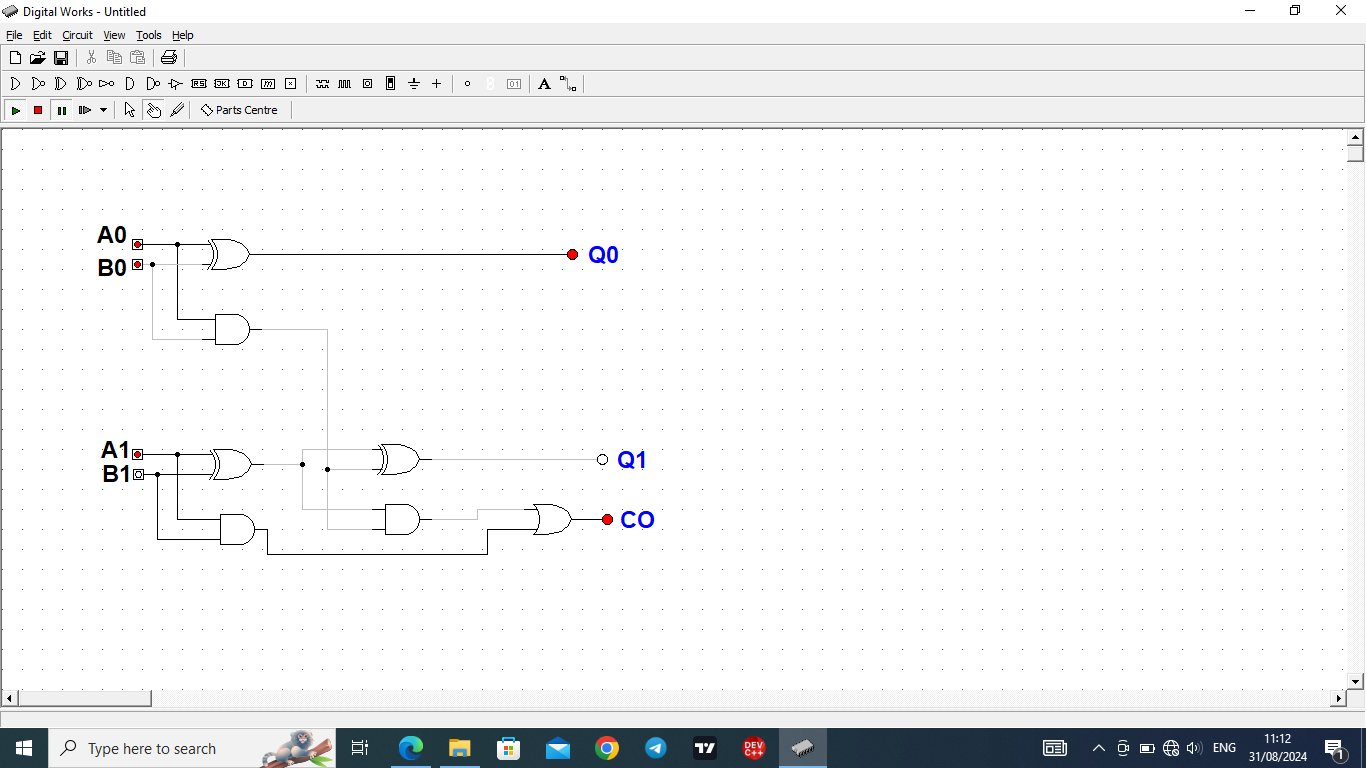
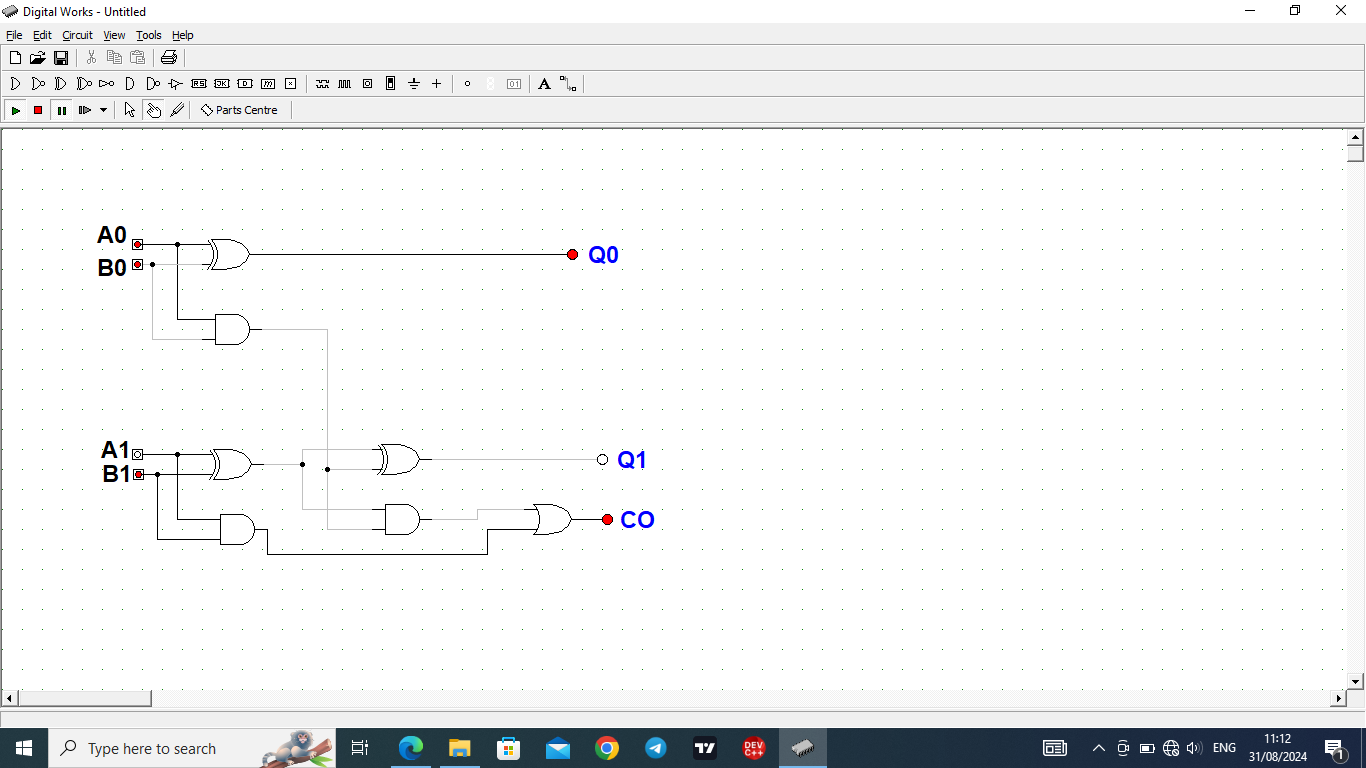
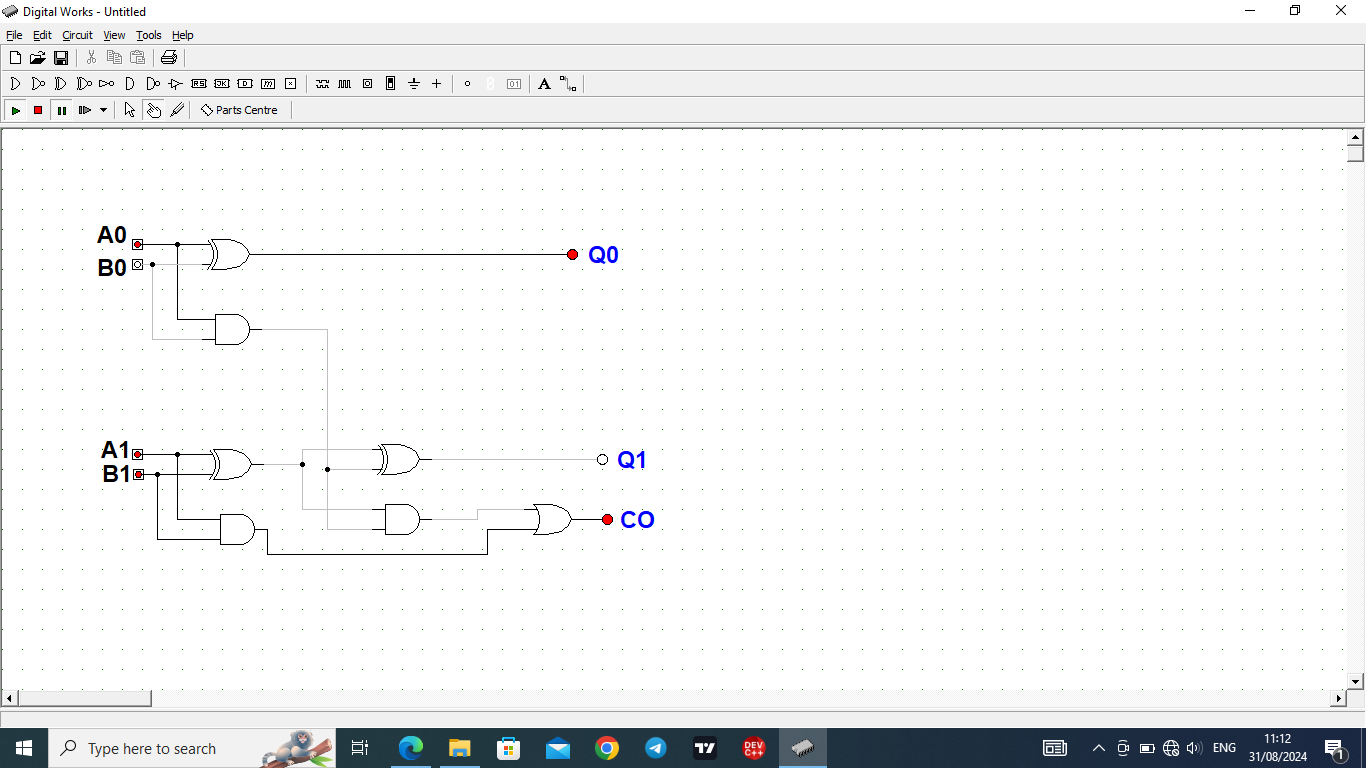
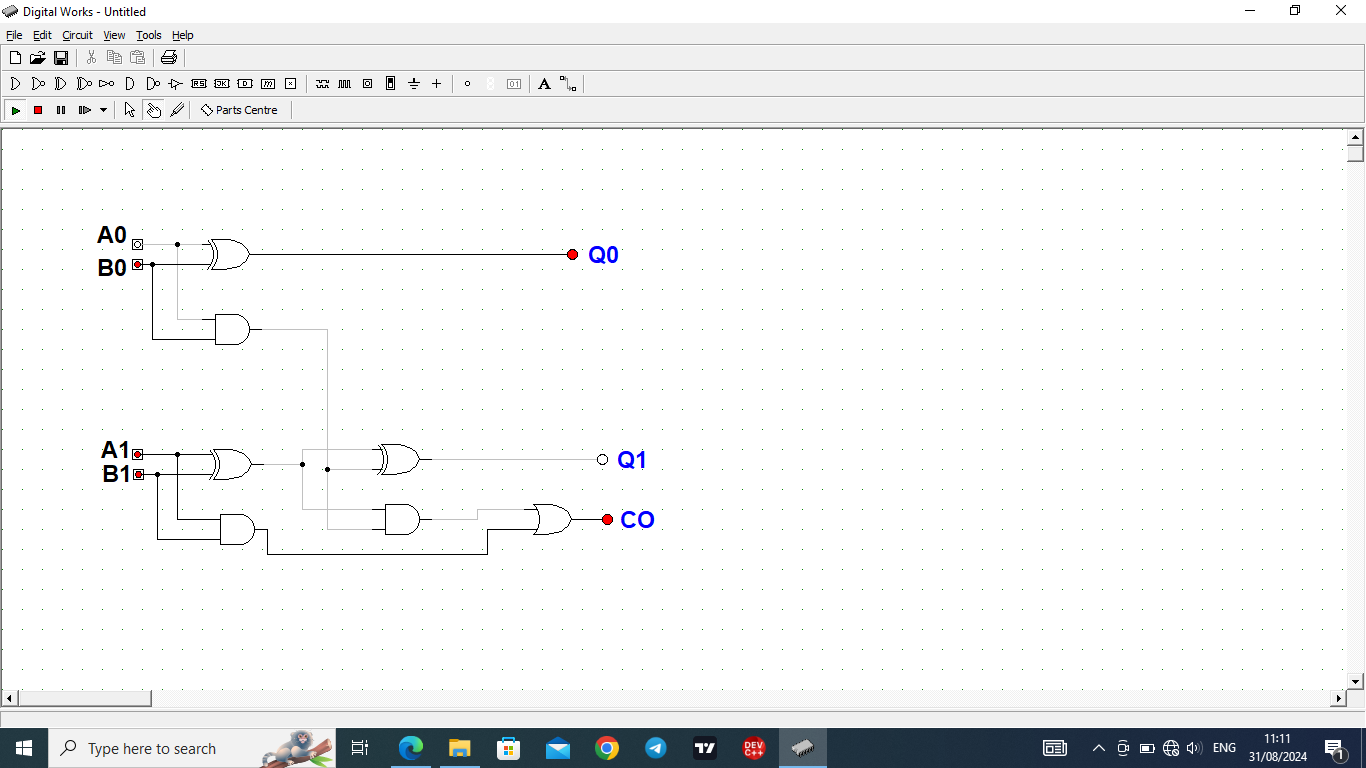
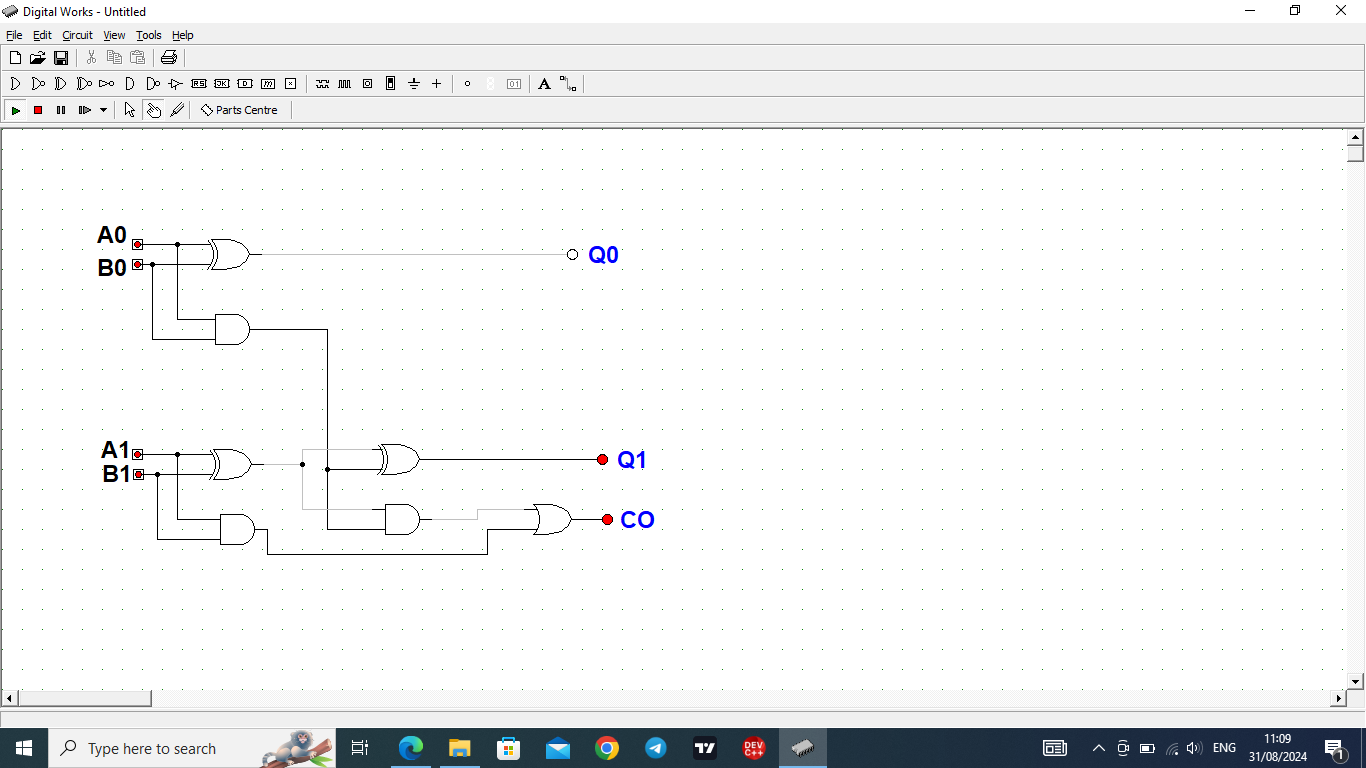
**ASSIGNMENT 0**

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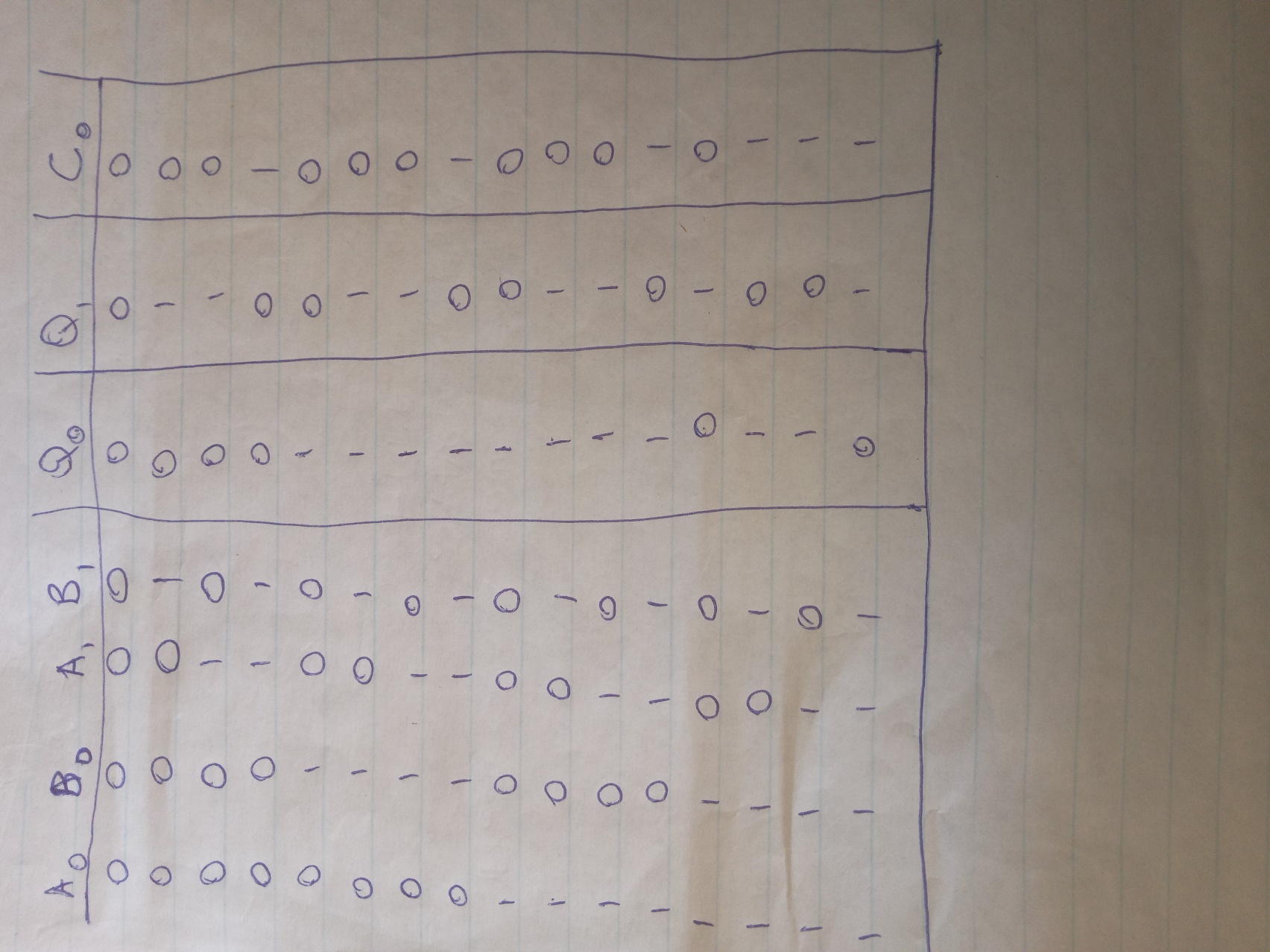


**3.TESTING** Process

We used Digital Works to create and simulate the circuit, and the circuit design was implemented according to the outlined schematic. Every possible combination of the 2-bit binary inputs was applied to the circuit.

For each input combination, we recorded the output sum and carry-out. These outputs were compared against the expected results.

**TRUTH TABLE**



Challenges and Resolutions

We encountered challenges in the carry outputs for some combination because the wiring of the half adders was incorrect, therefore changes were made to ensure proper connections between gates.

Conclusion

The testing process confirmed that the 2-bit binary adder circuit functions correctly across all input scenarios. Every expected output matched the results obtained from the simulation, and the circuit meets the assignment requirements effectively.