CS 223 Digital Design

Bilkent University
Spring 2021/2022

Laboratory Assignment 5
Preliminary Report

Section 2

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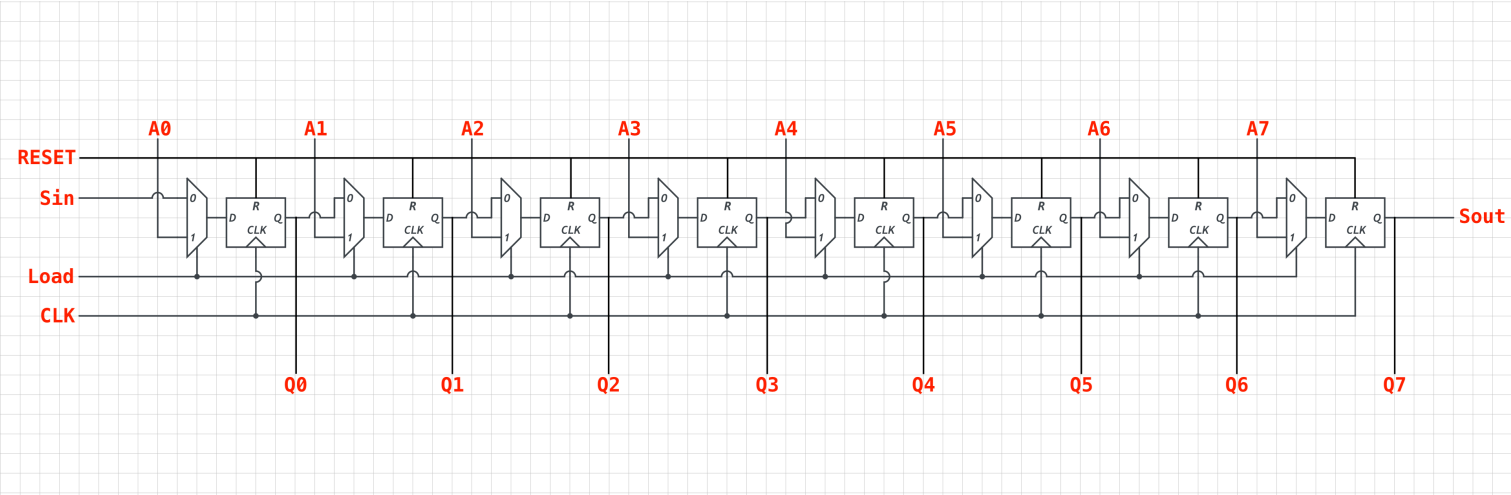
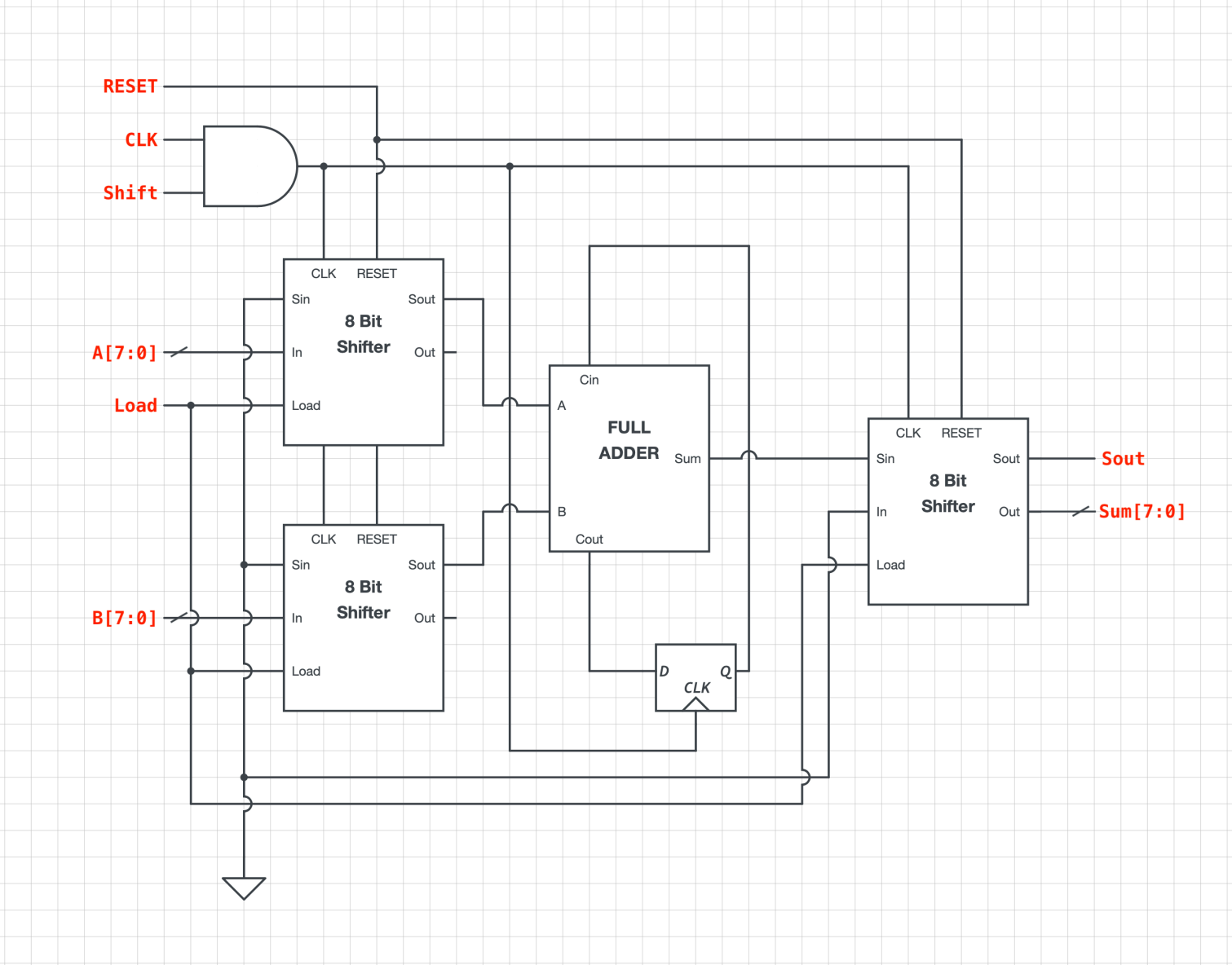
Mon. April 11th, 2022

1 8 Bit Shift Register Circuit Schematic



2 Serial Adder Circuit Schematic



System Verilog Modules

```
//
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// CS223, Section 2
// Lab 5, Preliminary Report
// 11.04.2022, Monday
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//

module ShifterRight(input logic CLK, RESET, Load, Shift, s_in,
[7:0] in,
                    output logic s_out, [7:0] Q);
    always_ff @(posedge CLK, posedge RESET)
        if(RESET)            Q <= 8'b00000000;
        else if(Load)        Q <= in;
        else if(Shift)
        begin
            if(s_in | ~s_in) Q <= {s_in, Q[7:1]};
        end
    assign s_out = Q[0];
endmodule

module SerialAdder(input logic CLK, RESET, Load, Shift, [7:0] A,
                                                              B,
                   output logic [7:0] sum);
    logic [7:0] QA, QB;
    logic a, b, cin, cout, s, x;
    ShifterRight SA(CLK, RESET, Load, Shift, 1'b0, A, a, QA);
    ShifterRight SB(CLK, RESET, Load, Shift, 1'b0, B, b, QB);
    FullAdder FA(a, b, cin, s, cout);
    ShifterRight SS(CLK, RESET, Load, Shift, s, 8'b00000000, x,
sum);
    always_ff @(posedge CLK)
        if(cout) cin <= 1;
        else     cin <= 0;
endmodule
```

Test-benches

```
module shifterRight_testbench();
    logic CLK, RESET, Load, Shift, sout;
    logic [7:0] in, Q;
    ShifterRight dut(CLK, RESET, Load, Shift, 1'b0, in, sout, Q);
    initial begin
        in = 8'b10101010;
        RESET = 0; Shift = 1;
                   Load = 0; #10;
                   Load = 1; #10;
                   Load = 0; #10;
    end

    always
        begin
        CLK <= 0; #10;
        CLK <= 1; #10;
        end
endmodule

module serialAdder_testbench();
    logic CLK, RESET, Load, Shift;
    logic [7:0] A, B, sum;
    SerialAdder SA(CLK, RESET, Load, Shift, A, B, sum);
    initial begin
        Shift = 1;
        RESET = 0;
        A = 8'b00110101;
        B = 8'b10001010;
                   Load = 0; #10;
                   Load = 1; #10;
                   Load = 0; #10;
                             #200; Shift = 0;

    end

    always
        begin
        CLK <= 0; #10;
        CLK <= 1; #10;
        end
endmodule
```