



## EE 445 HOMEWORK #1

**Due date and time**  
**8.November.2017 17:30**

### Introduction

The purpose of this homework is to implement a simple to use door lock system that includes a hex keypad, one push button switch labelled as OK, two on/off switches labelled as PASSWD and RST and three LEDs labeled as green G, red R and yellow Y and one control output LOCKED.

Assume that the keypad used in the system works as follows:

- When a single digit hex number on the keypad is pressed, a DAV (data available) signal goes to high and 4-bit binary value corresponding to hex digit is stored at the outputs of the keypad. DAV signal goes to low when the key is released. Assume that all switches in the system eliminate de-bouncing in hardware. The keypad reads and returns the lowest key value if more than one key are pressed simultaneously.

The specification of the system is as follows:

- It requires the user to enter a pre-determined 4-digit hex key code before unlocking the door.
- It makes consecutive key readings but ignores, if any, those after four until OK button is pressed.
- It compares the user key code entered with the stored code.
- If there is a match, it unlocks the door and makes GR=10 for five seconds.
- Otherwise, makes GR=01 for three seconds and the passage is rejected by keeping the door locked.
- Assume PASSWD and RST switches can only be activated/deactivated by an authorized user.
- Using PASSWD switch it is possible to change the code stored.
- When PASSWD is on, the authorized user is expected to enter the current 4-digit key code. Y starts blinking when correctly entered. While blinking, Y is off for 0.5 seconds and on for 0.5 seconds.
- The supervisor then enters the new 4-digit key code and Y=1 when ready.
- New code is expected to be different than the last three 4-digit key codes used. If it is not, another 4-digit key code must be entered.
- RST initializes the system with the default key code of 1234.
- During normal operation (when not RST and not PASSWD) and except the cases defined above LOCKED=0 and RGY=001.
- The system clock is 1 MHz.

### What to do?

- a) Design the control unit and datapath of the door lock system specified above. For this, draw the ASM chart, form the state table, and give the implementations for both parts.
- b) Design the system and write its Verilog code in behavioral style using Quartus.
- c) Simulate your code in part (b) and functionally verify it using a testbench of your own.

### What to deliver?

- Handwritten document of part (a)
- Source code for your design in part (b)
- Testbench for your simulation in part (c)
- A report containing implementation details and simulation results of your work