Lab 02

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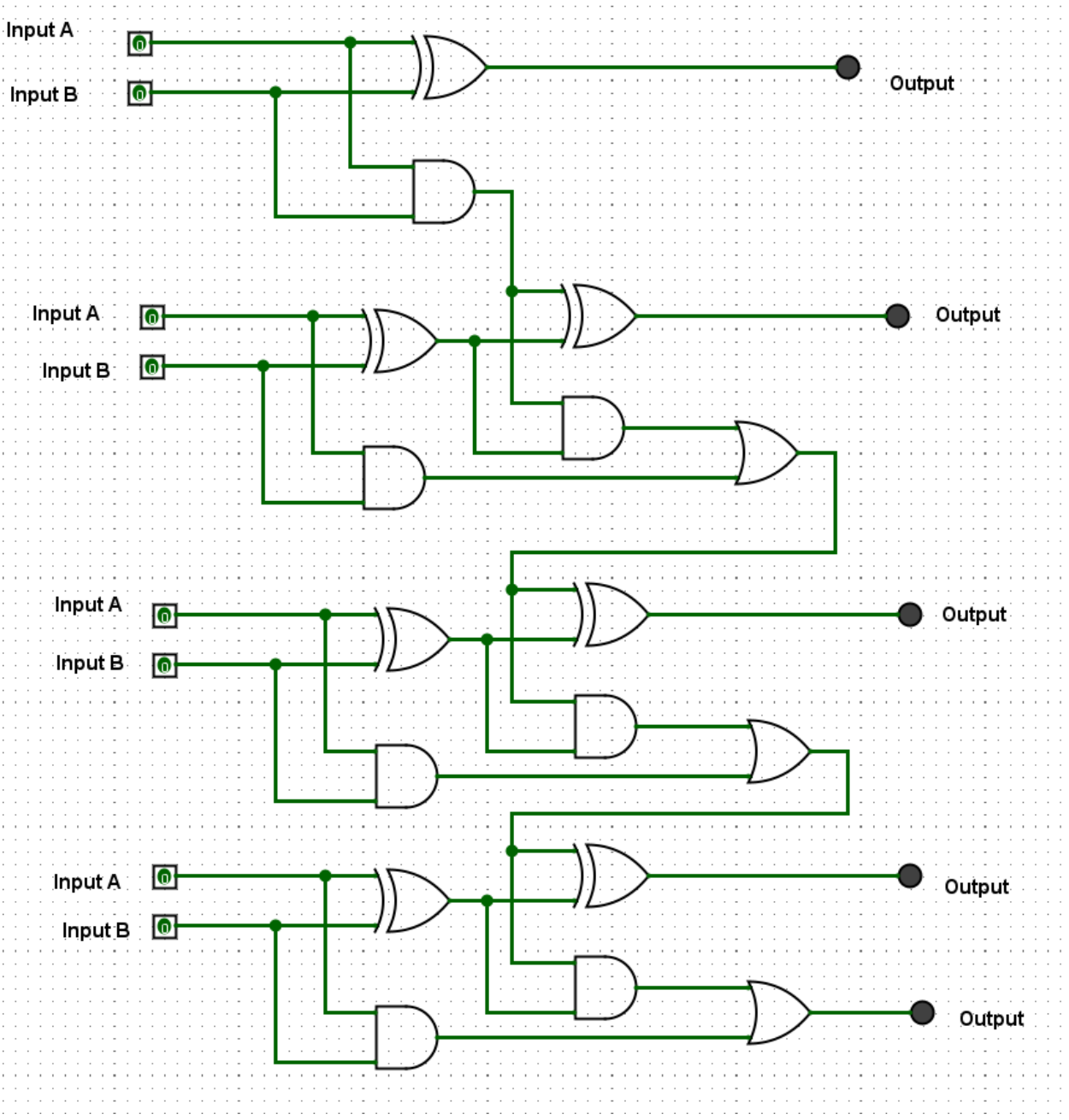
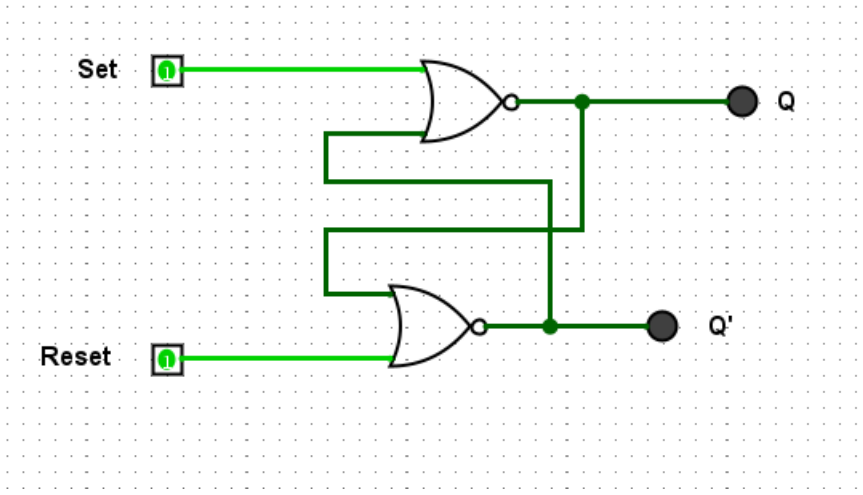
1. 4-bit adder



Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000

0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

2. RS Flip Flop



Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0

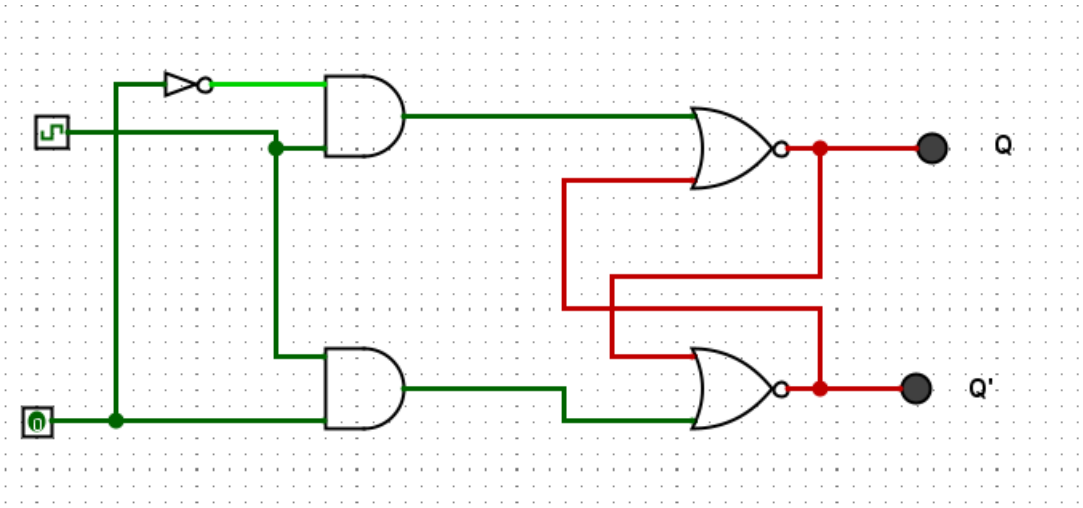
Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

When one of the inputs is 1, the output is unchanged. This is useful as the state of the circuits is stored.

What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design?

When both of the inputs is 1, both of the outputs are 0, which is invalid as Q has to be opposite to Q’, Q and Q’ can’t be on and off at the same time. This is an issue as this is considered as an unstable state.

3. D Flip -Flop



Clock	Pin	Q	Q’
0	0	0	0
0	1	0	0
1	1	0	1
1	0	1	0

Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

- The D flip-flop has only one input, Q is updated to be the same as D when the clock goes active.
- The external D input (Data) internally generate both an R and an S input.
- These are complements so never get both being active at once, avoiding unstable state

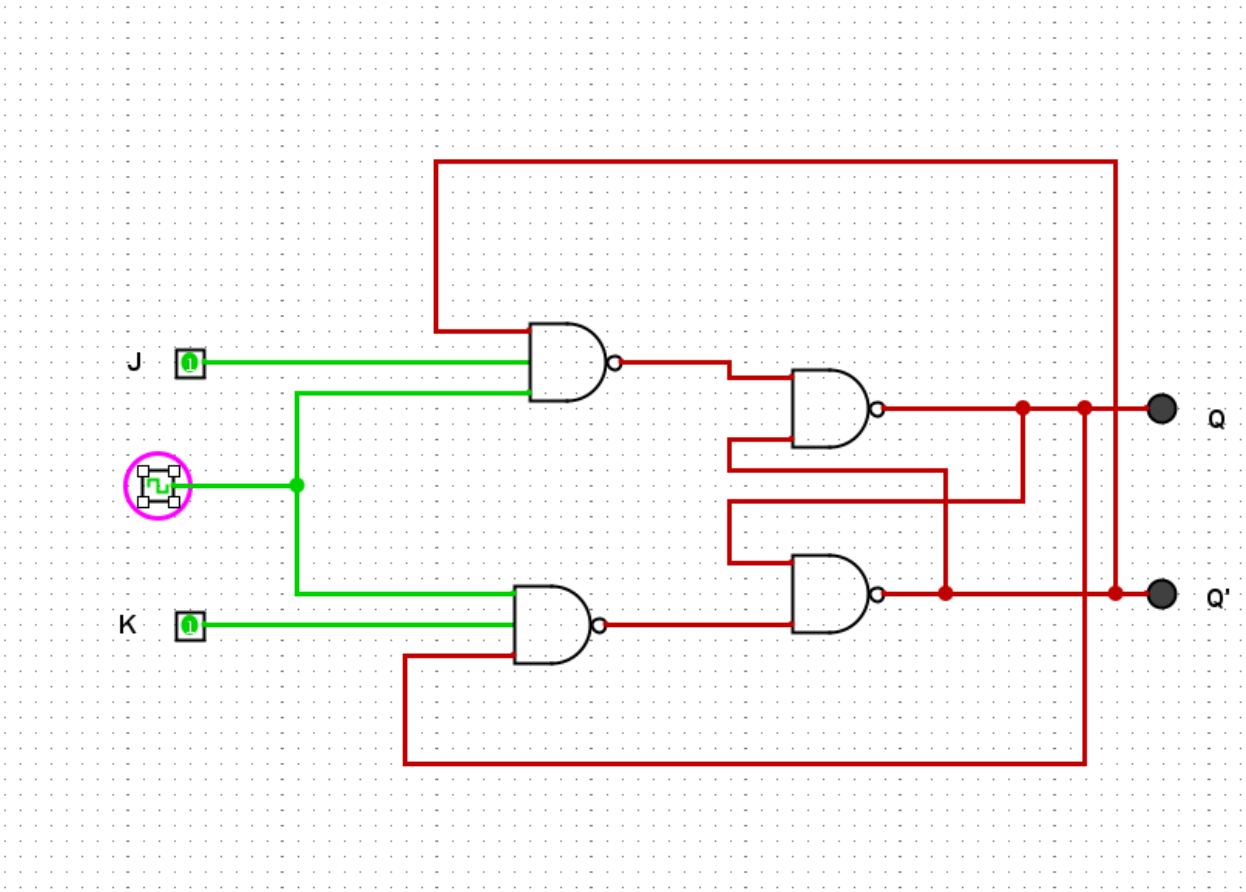
What is the role of the clock? How does it impact the changing of state of Q and Q’?

The clock ensures the data flow is synchronized in a circuit

Why is it generally preferred over the R-S Flip Flop?

There is no illegal state and data can be synchronized

4. JK Flip Flop



J	K	Q (When clocked)	Q’ (When clocked)
0	0	0	1
1	0	1	0
0	1	0	1
1	1	1	1

How can a J-K Flip Flop be made to behave like a D Flip Flop?

A NOT gate can be used

How can a J-K Flop Flop be made to behave like a toggle (T Flip Flop)?

Both inputs are 1, and is clocked