Code No: IT16213S

Max Marks:75

(10)

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (Autonomous) BE(IT) II/IV I Sem (Suppl) Examination May – Jun 2016

Digital Electronics & Logic Design

Time: 3 Hours

Note: Answer all questions from **Section-A** at one place in the same order Answer any five questions from Section-B Section - A (25 Marks) Draw the flow-chart of design flow for logic circuits (3) 1 2 Obtain the minimal sum-of products expression for the function f(x,y,z)=x+y'+x'y'z(2) 3 Draw the structure of CPLD (3)4 Write the truth table of BCD to 7 segment display (2) 5 Differentiate level triggering and edge triggering (2) Develop VHDL code for D Flip-flop (3)6 7 Obtain the state diagram for detecting the sequence "01" (3) 8 Differentiate Mealy and Moore FSM (2) 9 Define set up time and hold time of a flip-flop (2) What is an asynchronous sequential circuit. How the state transition takes place in (3) 10 these circuits. Section - B (50 Marks) (5) 11 (a) Obtain the minimal POS expression for the function $f(a,b,c,d) = \pi M(3,11,14) + D(0,2,4)$. Realize using NOR gates (b) Develop VHDL code for the above function (5) 12 (a) Implement the function $f = x \oplus y \oplus z$ using 4:1 Multiplexer (4) (b) Elaborate the general structure of FPGA (6) 13 (a) Draw the PLA implementation of the combination circuit to implement the function (5) $f_1(x,y,z) = \Sigma(0,3,4,6,7)$ and $f_2(x,y,z) = \Sigma(0,1,2,7)$ (b) Develop VHDL code for a 4-bit shift register (5) 14 (a) Design a sequence detector to detect a serial i/p sequence 1010. It should produce (7) an output 1 when the input pattern has been detected (b) Draw and indicate the elements of ASM Chart (3)15 (a) Analyze D Flip-flop as an asynchronous circuit (b) Construct the state table and draw the FSM model of SR latch (4)16 (a) Find the complement of the function F=x'yz' + x'y'z by finding the dual of the (4) function. (b) Design a 4 to 16 decoder using 3 to 8 decoders. (6)

17 Design a 4-bit synchronous decade counter by making use of JK flip-flops