Asynchronous Seq. Ckt (chap 9)

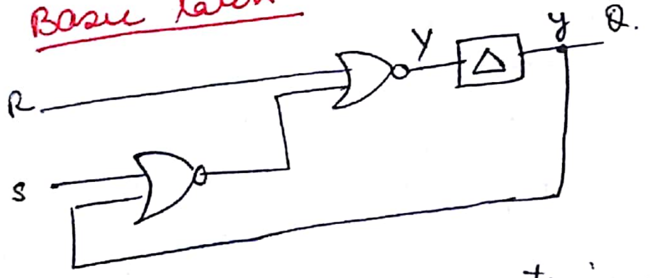
→ do not use F/F

→ do not have clk pulse

→ i/p to the ckt must change one at a time

→ there must be sufficient time b/w the change in i/p signals to allow the ckt to reach a stable state (when all internal signals stop changing)

Basic latch



→ Feedback loop ⇒ req

→ change in either S or R i/p the value of Q ~~with~~ will change after a short propogation time through the NOR gats.

→ The combined propogation delay is rep above by $\boxed{\Delta}$

→ ∴ NOR gates are idle with zero delay.

Q → present state ; y : present state variable   Y :- Next state var.

→ After Δ delay y takes the value of Y.

⇒ State Assignment table

Present	Next SR= 00	01	10	11
y	Y	Y	Y	Y
0	⓪	⓪	1	⓪
1	①	0	①	0

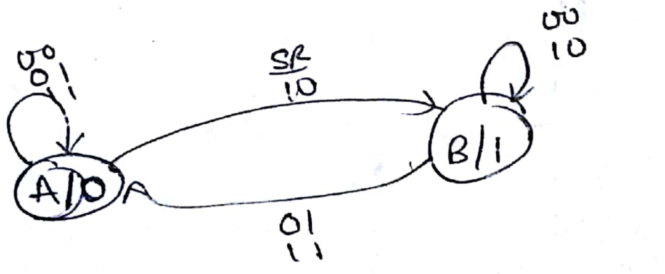
when y = Y the state of the ckt does not ~~chnge~~ change

→ ckt is stable.

⇒ State Table   State A when y=0
B " y=1

o/p depends only on the present state ⇒ Moore type ~~o/p~~ FSM

Prent	Next State SR= 00	01	10	11	Q o/p
A	Ⓐ	Ⓐ	B	Ⓐ	0
B	Ⓑ	A	Ⓑ	A	1



$$\boxed{Y = \overline{R}(S+y)}$$

→ In asyn seq ckt Y is saved in a F/F

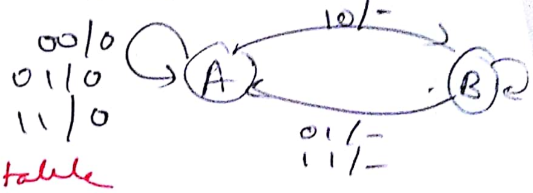
SR latch Mealy Model

		NS		
PS	SR	00	01	10
A	~~B~~	A	A	B
B		B	A	B

→ O/P ~~ckt~~ when ckt is stable are same as for Moore.

→ Suppose SR = 00 state is A o/p = 0 ~~o/p = 1 the~~ now i/p SR change to 10 the state changes to B. When state is B then

→ mealy model change in o/p must at the same time as i/p change ∴ '—' unspecified.

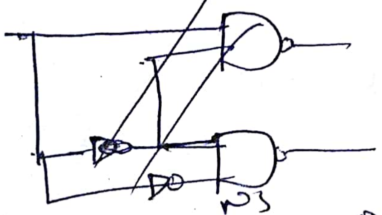


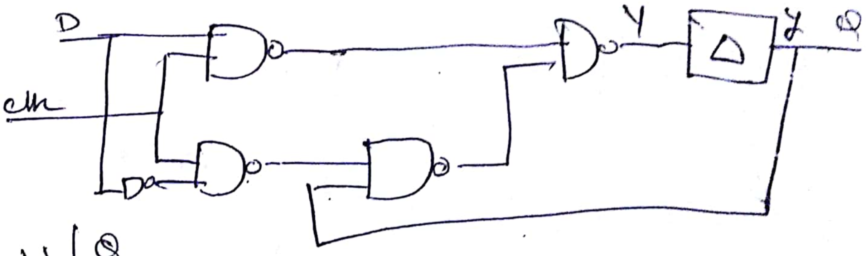
State table called as → flow table
~~state~~

state Assigned table called → transition table or excitation table

ANAYSIS OF ASY SEQ CKT

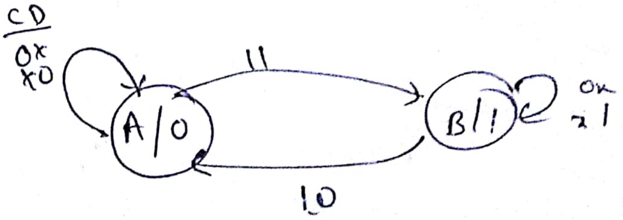
Gated D latch





		NS			
y	CD 00	01	10	11	Q
0	0	0	0	1	0
1	1	1	0	1	1

Excitation table



		NS			
	CD 00	01	10	11	Q
A	A	A	A	B	0
B	B	B	A	B	1

Flow table

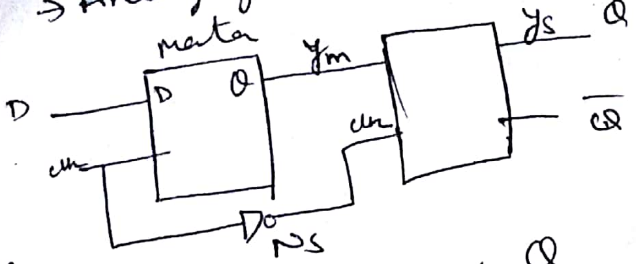
$Y = CD + \bar{C}y$

- 0 | 8
1

Asy Seq Ckt (Analysis) contd :-

Master Slave D F/F

→ Analyzing a ~~seq~~ syn seq ckt as any seq ckt.



	NS				op
PS	CD 00	01	10	11	Q
	Ym	Ys			
00	00	00	00	10	0
01	00	00	01	11	1
10	11	11	00	10	0
11	11	11	01	01	1

	NS				
PS.	CD 00	01	10	11	Q.
S_1	S_1	S_1	S_1	S_3	0
S_2	S_1	S_1	S_2	S_4	1
S_3	S_4	S_4	S_1	S_3	0
S_4	S_4	S_4	S_2	S_4	1

Flow table

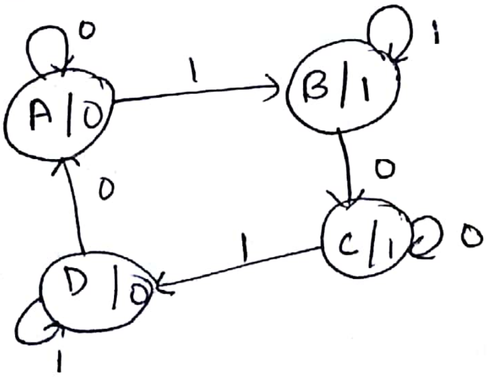
$$Y_m = CD + \bar{C} y_m + y_m D$$

$$Y_s = \bar{C} y_m + C y_s + y_m y_s$$

Synthesis of Asy ckt

Serial Parity generator :-

Design a ckt that has an i/p w & an o/p z, s.t. when pulse is applied to w, the o/p z is = 0 if no of previously applied pulses is even & z = 1 if no of pulses applied are odd.



	NS		op
PS	w = 0	w = 1	z
A	A	B	0
B	C	B	1
C	C	D	1
D	A	D	0

	NS		
	w = 0	w = 1	
$y_2 y_1$	$Y_2 Y_1$		z
00	00	01	0
01	10	01	1
10	10	11	1
11	00	11	0

another state assignment ⟹

	NS		
PS	w = 0	w = 1	z
00	00	01	0
01	11	01	1
11	11	10	1
10	00	10	0

⇓

Prob $y_2 y_1 = 11$ to $y_2 y_1 = 00$

Ⓧ only one should chge at a time
But only one y_2 or y_1 will change first

⇒ when y_2y_1 = 11 & w = 1 NS is 11
change to y_2y_1 = 11 & w = 0 NS is 00

But both y_2y_1 cannot change at the same time (Prop. delay)

a) if y_1 changes first y_2y_1 = 10 & w = 0 NS 10
Then NS remains as 10 which wrong.

b) if y_2 changes first y_2y_1 = 01 & w = 0 NS = 10
requiring both y_2 & y_1 to change simultaneously which not possible
But as we assumed y_2 changes before y_1 then

∴ NS y_2y_1 = 00 which is correct.

∴ D to A xition occurs correctly iff y_2 changes first

Race condition.

→ Can be eliminated by allowing only one var to change at a time A B & D can be 00, 01, 11, 10 resp.

$z = y_1$; $Y_1 = w\bar{y}_2 + \bar{w}y_1 + y_1\bar{y}_2$, $Y_2 = wy_2 + \bar{w}y_1 + y_1y$

Scanned by CamScanner

⇒ when $y_2 y_1$ = 11 & w = 1 NS is 11
change to $y_2 y_1$ = 11 & w = 0 NS is 00
But both $y_2 y_1$ cannot chage at the same time (Prop. delay)

a) if y_1 changes first $y_2 y_1$ = 10 & w = 0 NS 10
Then NS remains as 10 which wrong.

b) if y_2 changes first $y_2 y_1$ = 01 & w = 0 NS = 10
requiring both y_2 & y_1 to change simultaneously which not possible
But as we assumed y_2 changes before y_1 then
∴ NS $y_2 y_1$ = 00 which is correct.

∴ D to A Xsition occurs correctly iff y_2 changes first

Race condition.

→ can be eliminated by allowing only one var to change at a time
A, B & D can be 00, 01, 11, 10 resp.

$z = y_1$; $Y_1 = w\bar{y}_2 + \bar{w}y_1 + y_1\bar{y}_2$, $Y_2 = wy_2 + \bar{w}\bar{y}_1 + y_1 y_2$

Asynchronous S
State Red
→ Re

[illegible]

Asynchronous Seq Ckts

State Reduction

→ Reduces states for simpler implementation.

→ Tables where there is only one stable state for each row, are referred to as. primitive flow tables.

→ State Reduction by partitioning — potentially eq rows bcoz both rows in each pair have same o/p s & don't care entries in the same col.

eg

PS	Next State DN = 00	01	10	11	o/p Z
A	A	B	C	–	0
B	D	B	–	–	0
C	A	–	C	–	1
D	D	E	F	–	0
E	A	E	–	–	1
F	A	–	F	–	1

eg C & F → o/p = 1 ; stable state at 10 unspecified ~~for~~ (01, 11) for both.

A & D :- Stable under DN = 00 o/p = 0 unspe cnt same loc.

B & E :- same unspecified, stable at DN = 01 o/p B = 0, o/p E = 1 } X → cannot be paired

P1 = (AD)(B)(CF)(E)

→ Successor of A & D

	DN 00	01	~~10~~ 10	11
AD	AD	BE	CF	--
CF	AA	--	CF	--

BE not equ
∴ AD also not equivalent.

∴ P2 : (A)(D)(B)(CF)(E)

P3 :

	00	01	10	11
CF	AA	--	CF	--

P3 = P2 (stop)

∴ C,F are equivalent.

eg $x_3x_4 \backslash x_1x_2$ 00 01 11 10

②

∴

	NS DN 00	01	10	11	Z
A	Ⓐ	B	C	–	0
B	D	Ⓑ	–	–	0
C	A	–	Ⓒ	–	1
D	Ⓓ	E	C	–	0
E	A	Ⓔ	–	–	1

II Step Merging using unspecified.

C can be merged with A or E but not both.

if A & C are merged at ~~00~~ DN = 00 stable state

~~01~~ 10 " "

11 same.

$Z_A = 0$ $Z_C = 1$ — Mealy model

alternate

~~A~~ C & E :- DN - 00 A DN = 01 Stable state Ⓔ

DN = 10 stable state Ⓒ. o/p = 1 } moore model

∴ merging C & E.

	00	01	10	11
A	Ⓐ	B	C	–
B	D	Ⓑ	–	–
C	A	Ⓔ	Ⓒ	–
D	Ⓓ	E	C	–

Merging ~~process~~ ~~prod~~ procedure

Two states (rows in a flow table) Si & Sj are said to be compatible if there are no state conflicts for any i/p valuation. Thus, for each i/p valuation, one of the following conditions must be true:.

✓ Both Si & Sj have same successor

✓ both Si & Sj are stable. OR

✓ successor of Si or Sj, or ~~both~~ both, is unspecified.

AND Both Si & Sj must have the same o/p whenever specified.

tate Reduction contd

	NS				O/P
PS	w_2w_1 00	01	10	11	Z
A	Ⓐ	H	B	–	0
B	F	–	Ⓑ	C	0
C	–	H	–	Ⓒ	1
D	A	Ⓓ	–	E	1
E	–	D	G	Ⓔ	1
F	Ⓕ	D	–	–	0
G	F	–	Ⓖ	–	0
H	–	Ⓗ	–	E	0

Moore type merging

A & H are compatable.

A	Ⓐ	H	B	–
H	–	Ⓗ	–	E

B with F & G

C with none

D & E are compatable.

F & G , " "

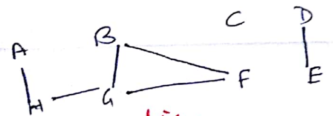
G & H "

B	F	–	Ⓑ	C
F	Ⓕ	D	–	–
G	F	–	Ⓖ	–

comp. Pairs are

(A H) (B F) (B G) (G F)

(D E) (H G)



Merger dig.

A can be merged with H iffo H is not merged with G as

A & G cannot be merged.

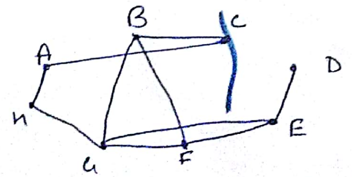
B, F, G are pair wise compatable so can be merged.

but not 'H'. ∴ (A H) (B F G) (D E) (C)

(D E) are merged.

					Z
A	Ⓐ	Ⓐ	B	D	0
B	Ⓑ	D	Ⓑ	C	0
C	–	H	–	Ⓒ	1
D	A	Ⓓ	B	Ⓓ	1

Mealy type



not better

∴ not contd . . .

… y3y4) 00, 01 11 10

Eg pg 548 Fig 9.32

	00	01	10	11	
A	A	G	E	—	0
B	K	—	B	D	0
C	F	C	—	H	1
D	—	C	E	D	0
E	A	—	E	D	1
F	F	C	J	—	0
G	K	G	—	D	1
H	—	—	E	H	1
J	F	—	J	D	0
K	K	C	B	—	0

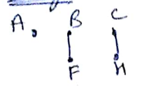
Parti P1 : (A ~~B~~ F K) (B J) (C G) (D) (E) (H)}

o/p same
1 — km " al

AFK	AFK	GCC	EJB
↑ BJ	KF		↑

P2 : (A) (FK) (BJ) (CG) (D) (E) (H)

Merg



Moore

Mealy

azards

The ~~glitches~~ glitches caused by the structure of a given ckt & propogation delays in the ckt are ref. to as Hazard.

Two types

→ Static

→ If a signal is supposed to. remain at a particular logic val when an i/p var changes its val but instead the signal undergoes a momentary change in its required value

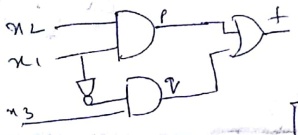
1 → 1 0 → 0.

→ Dynamic

when ~~signal~~ is supposed to change from 1 to 0 or from 0 to 1

If such change involves a short oscillation before the signal settles into its new level.

Static Hazard

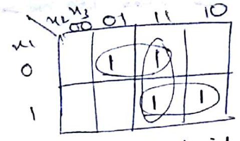


$F = x_1 x_2 + \bar{x}_1 x_3$ glitch

path for 'p' is shorter than for 'q'

$\boxed{f = x_1 x_2 + \bar{x}_1 x_3 + x_2 x_3}$

Hazard can be eliminated



$x_1 \backslash x_2 x_3$	00	01	11	10
0		1	1	
1			1	1

→ A potential hazard exists whenever two adjacent 1's in a k map are not covered by a single product term.

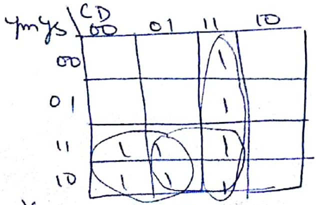
→ Tech for removing hazards is to find a cover in which some product term includes each pair of adjacent 1's.

→ It is not necessary to include 'do'nt' care vertices.

eg Master Slave D F/F.

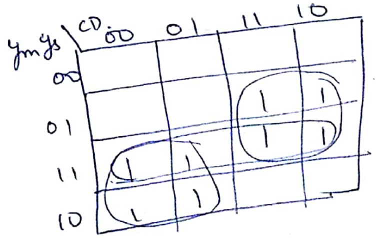
$Y_m = CD + \bar{C} y_m$

$Y_s = \bar{C} y_m + C y_s$



$y_m y_s \backslash CD$	00	01	11	10
00			1	
01			1	
11	1	1	1	
10	1	1	1	

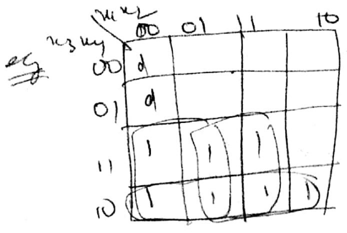
$Y_m = CD + \bar{C} y_m + D y_m$



$y_m y_s \backslash CD$	00	01	11	10
00				
01			1	1
11	1	1	1	1
10	1	1		

$Y_s = \bar{C} y_m + C y_s + y_m y_s$

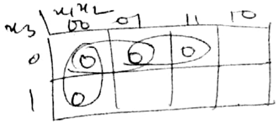
eg



x_3x_4 \ x_1x_2	00	01	11	10
00	d			
01	d			
11	1	1	1	
10	1	1	1	1

$f = \bar{x}_1 x_3 + x_2 x_3 + x_3 \overline{x_4}$

Similarly for POS form also.



x_3 \ x_1x_2	00	01	11	10
0	0	0	0	
1	0			

$f = (x_1 + x_2)(\bar{x}_2 + x_3)(x_1 + x_3)$

Dynamic hazards

→ A dynamic hazard cause glitches on 0→1 or 1→0 transition of an o/p.

→ A dynamic hazard is caused by the structure of the ckt, where there exists multiple paths for a given signal change to propogate along.

→ A ckt that has dynamic haz. must also have a static hazard in some part of it.

→ Dynamic hazards are encountered in multi level ckts.

→ DH can be avoided by using two level ckts & ensuring that there are no static hazards.

Significance of hazards

→ A glitch in an asyn. seq ckt can cause the ckt to enter an incorrect state & possibly become stable in that state.

→ ∴ ckt that generates the next state var must be hazard free.

→ It is sufficient to eliminate hazards due to changes in the value of a single var because ~~the basic~~ in Asy seq ckt both i/p & state var must change one at a time