

DESCRIPTION

The MP1653 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input range. The MP1653 has synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1653 requires a minimal number of readily available, standard, external components and is available in a space-saving SOT563 (1.6mmx1.6mm) package.

FEATURES

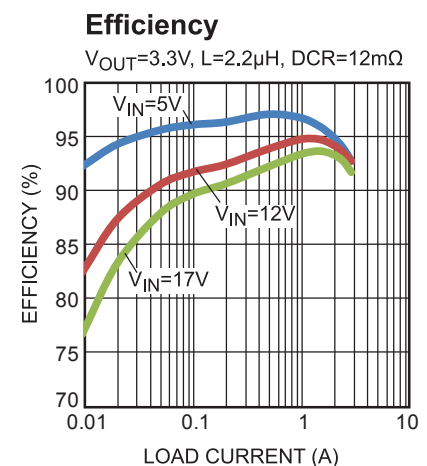
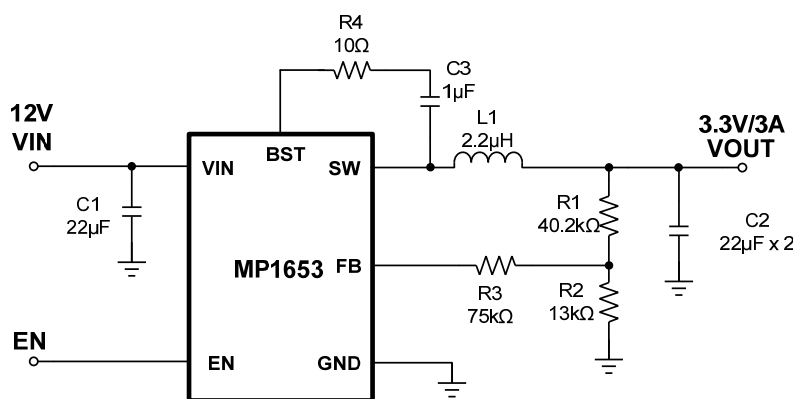
- Wide 4.2V to 17V Operating Input Range
- 70mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 200μA Low I_Q
- High-Efficiency Synchronous Mode Operation
- Power-Save Mode at Light Load
- Fast Load Transient Response
- 800kHz Switching Frequency
- Internal Soft Start
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a SOT563 (1.6mmx1.6mm) Package

APPLICATIONS

- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1653GTF	SOT563 (1.6mmx1.6mm)	See Below

* For Tape & Reel, add suffix -Z (e.g. MP1653GTF-Z)

TOP MARKING

AUCY

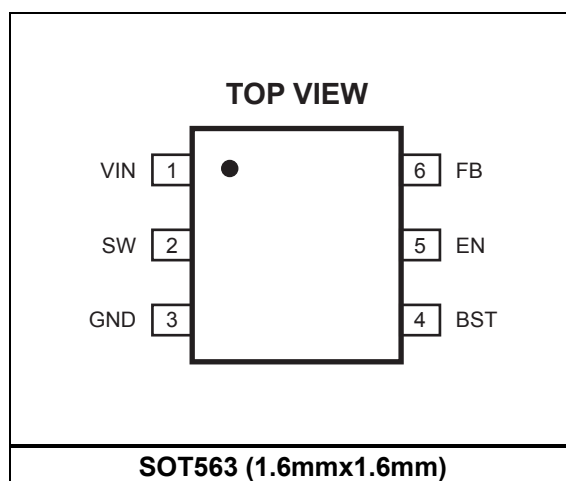
LLL

AUC: Product code of MP1653GTF

Y: Year code

LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V _{IN}).....	-0.3V to 18V
V _{SW}	-0.6V (-6.5V for <10ns) to V _{IN} +0.3V (19V for <10ns)
V _{BST}	V _{SW} + 5V
V _{EN}	-0.3V to 6V ⁽²⁾
All other pins	-0.3V to 5V
Continuous power dissipation (T _A = +25°C) ⁽³⁾	1W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

Recommended Operating Conditions ⁽⁴⁾

Supply voltage (V _{IN}).....	4.2V to 17V
Output voltage (V _{OUT}).....	0.8V to V _{IN} x D _{MAX} or 10V max
Operating junction temp. (T _J)...	-40°C to +125°C

Thermal Resistance ⁽⁵⁾	θ_{JA}	θ_{JC}
SOT563 (1.6mmx1.6mm)	130.....	60... °C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) For details on EN's ABS max rating, please refer to the Enable (EN) section on page 11.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN = 12V, TJ = -40°C to +125°C ⁽⁶⁾, typical value is tested at TJ = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I _{IN}	V _{EN} = 0V			10	μA
Supply current (quiescent)	I _Q	V _{EN} = 2V, V _{FB} = 0.85V	170	200	240	μA
HS switch-on resistance	HS _{RDS(ON)}	V _{BST-SW} = 3.3V		70		mΩ
LS switch-on resistance	LS _{RDS(ON)}			40		mΩ
Switch leakage	SW _{LKG}	V _{EN} = 0V, V _{SW} = 12V			10	μA
Valley current limit	I _{LIMIT}	V _{OUT} = 0V	2.7	4	5.8	A
ZCD	I _{ZCD}	V _{OUT} = 3.3V, Lo = 2.2μH, I _{OUT} = 0A	-250	20	250	mA
Oscillator frequency	f _{SW}	V _{FB} = 0.75V	600	800	1000	kHz
Minimum on time ⁽⁷⁾	T _{ON MIN}			45		ns
Minimum off time ⁽⁷⁾	T _{OFF MIN}			180		ns
Feedback voltage	V _{REF}	TJ = +25°C	790	802	814	mV
Feedback current	I _{FB}			10	100	nA
FB UV threshold (H to L)	V _{UV th}	Hiccup entry		75%		V _{REF}
Hiccup duty cycle ⁽⁷⁾	D _{Hiccup}			25		%
EN rising threshold	V _{EN RISING}		1.14	1.2	1.26	V
EN hysteresis	V _{EN HYS}			100		mV
EN input current	I _{EN}	V _{EN} = 2V		2		μA
VIN under-voltage lockout threshold rising	INUV _{Vth}		3.7	4	4.18	V
VIN under-voltage lockout threshold hysteresis	INUV _{HYS}			330		mV
Soft-start period	T _{SS}		1.6	2.5	3	ms
Thermal shutdown ⁽⁷⁾	TSD			150		°C
Thermal hysteresis ⁽⁷⁾	TSD _{HYS}			20		°C

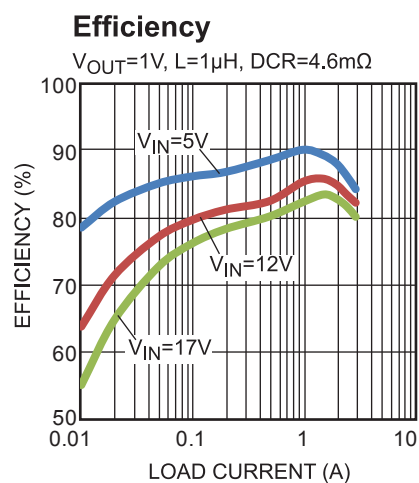
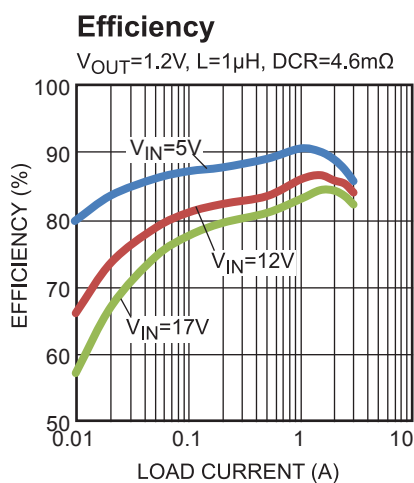
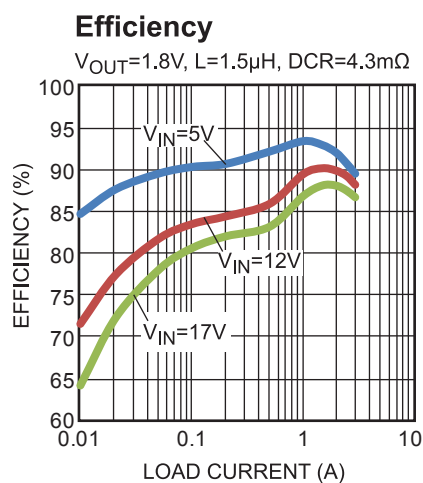
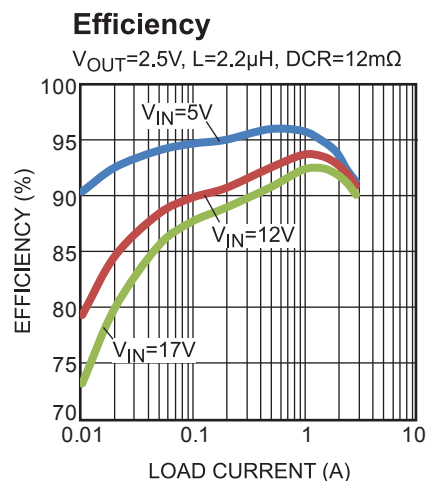
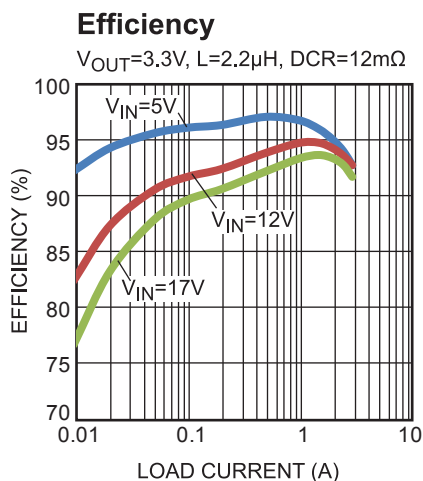
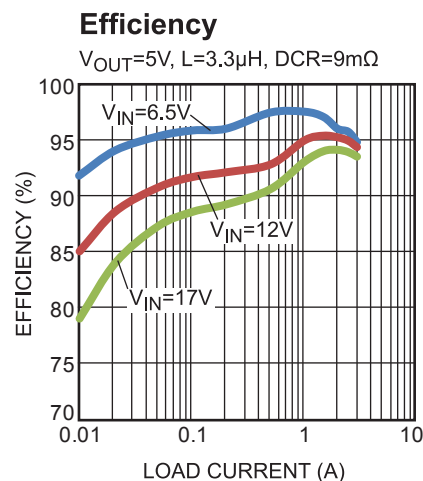
NOTES:

6) Not tested in production. Guaranteed by over-temperature correlation.

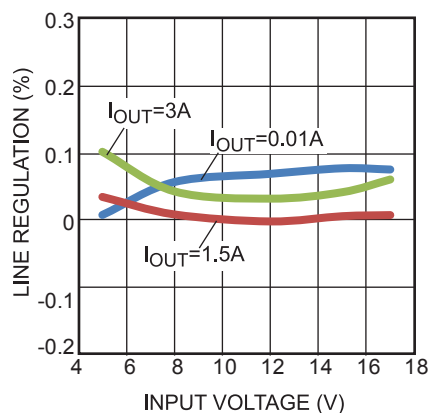
7) Guaranteed by design and engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

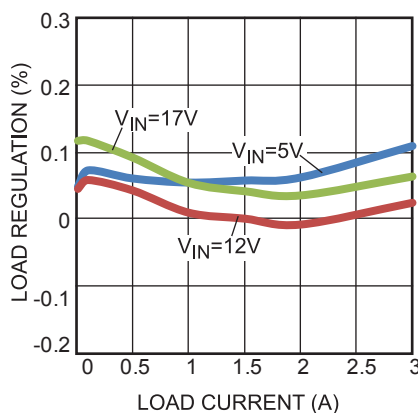
$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $T_A = +25^\circ C$, unless otherwise noted.



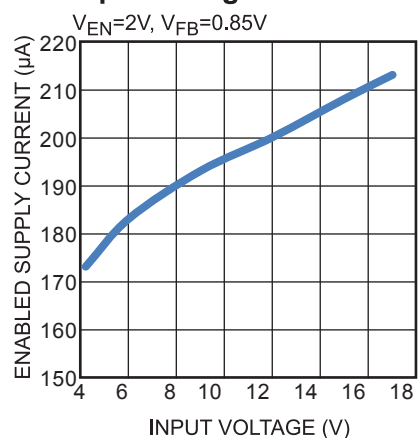
Line Regulation



Load Regulation

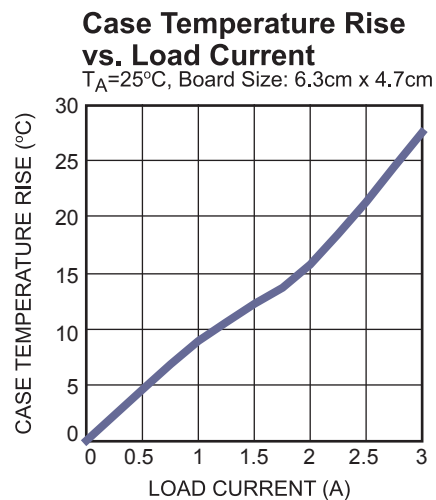
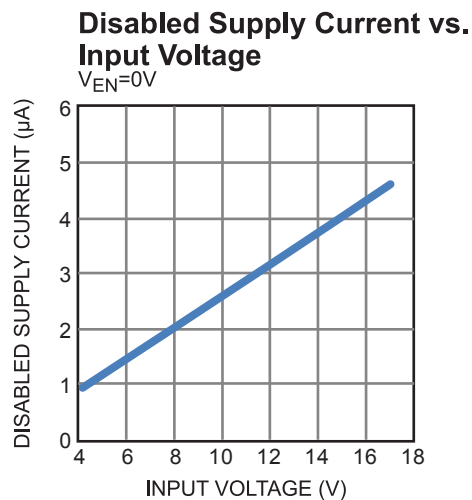


Enabled Supply Current vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

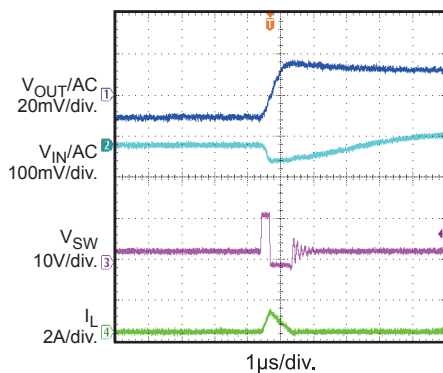


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

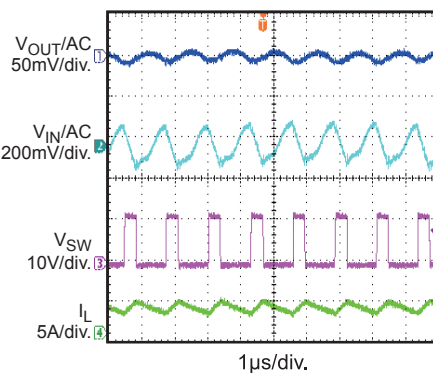
Input/Output Ripple

$I_{OUT} = 0A$



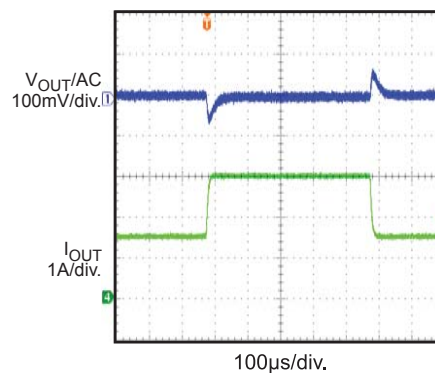
Input/Output Ripple

$I_{OUT} = 3A$



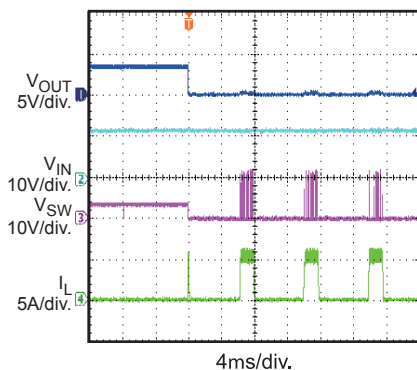
Transient Response

$I_{OUT} = 1.5A$ to $3A$, $2.5A/\mu s$



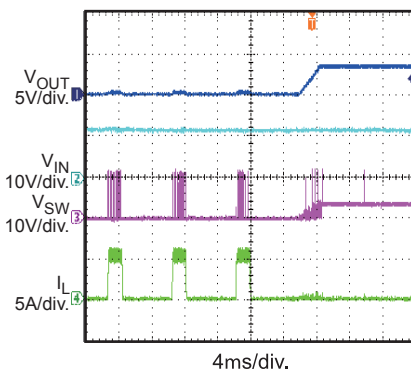
Short-Circuit Entry

$I_{OUT} = 0A$



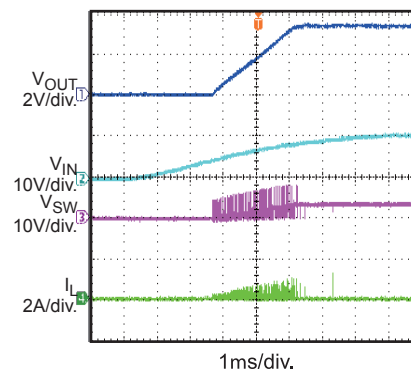
Short-Circuit Recovery

$I_{OUT} = 0A$



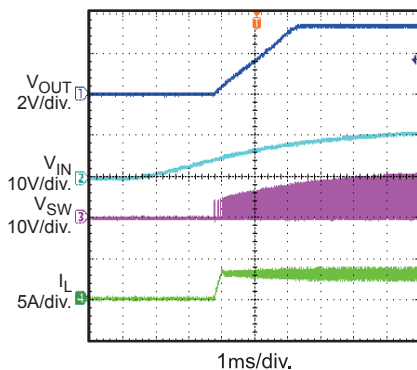
Start-Up through Input Voltage

$I_{OUT} = 0A$



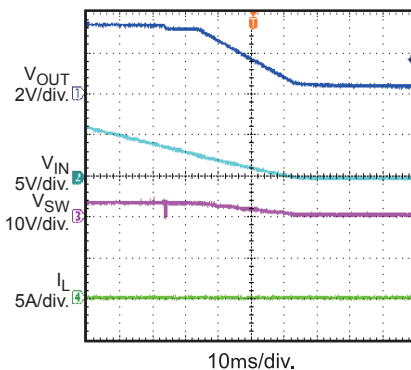
Start-Up through Input Voltage

$I_{OUT} = 3A$



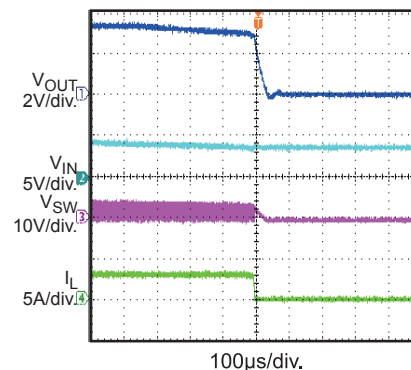
Shutdown through Input Voltage

$I_{OUT} = 0A$



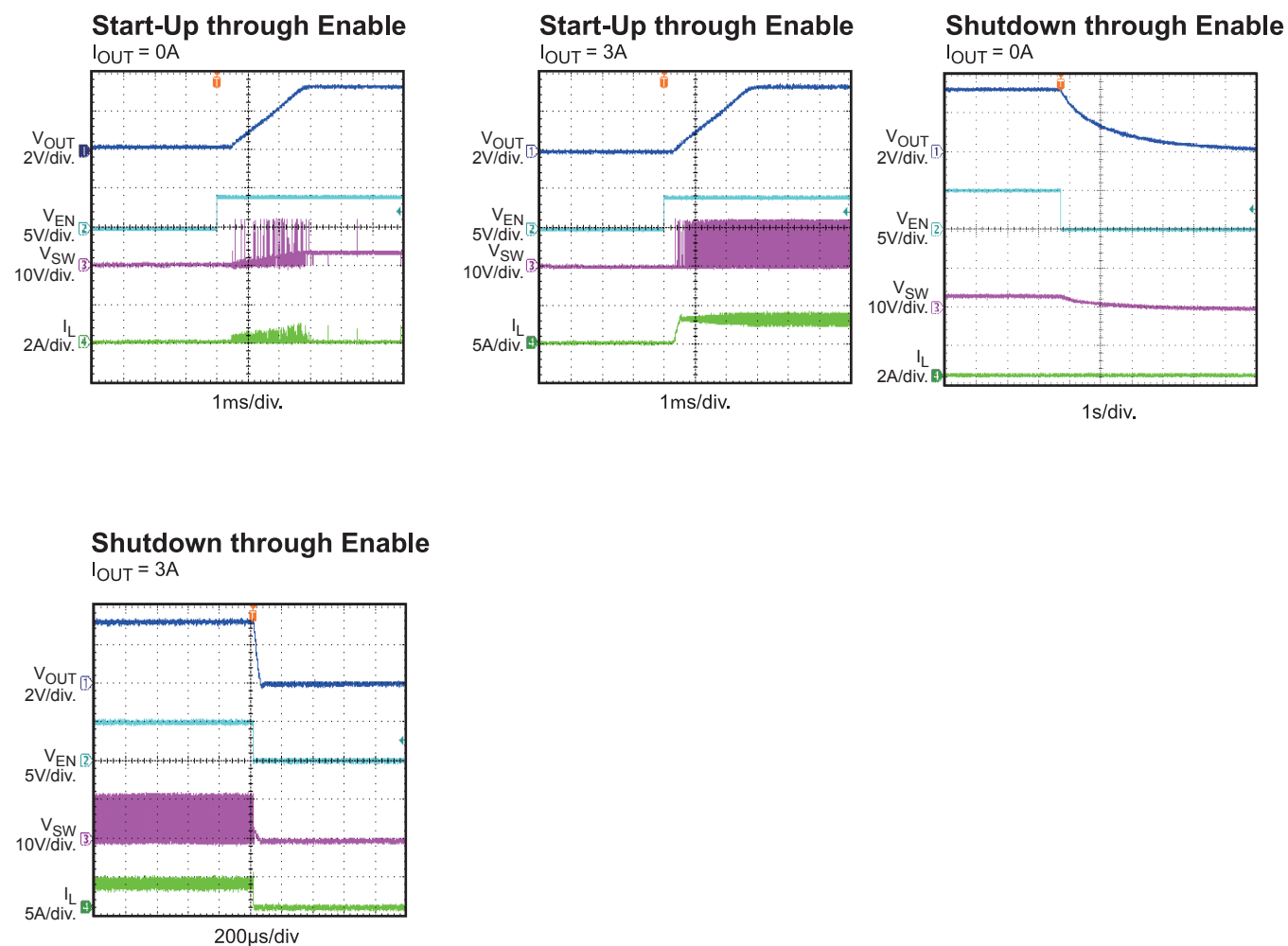
Shutdown through Input Voltage

$I_{OUT} = 3A$



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $T_A = +25^\circ C$, unless otherwise noted.



PIN FUNCTIONS

Package Pin #	Name	Description
1	VIN	Supply voltage. The MP1653 operates from a 4.2V to 17V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	Switch output. Connect SW using a wide PCB trace.
3	GND	System ground. GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND to ground with copper traces and vias.
4	BST	Bootstrap. Connect a 1 μ F BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	Enable. Drive EN high to enable the MP1653. For automatic start-up, connect EN to VIN with a 100k Ω pull-up resistor.
6	FB	Feedback. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 600mV to prevent current limit runaway during a short-circuit fault.

BLOCK DIAGRAM

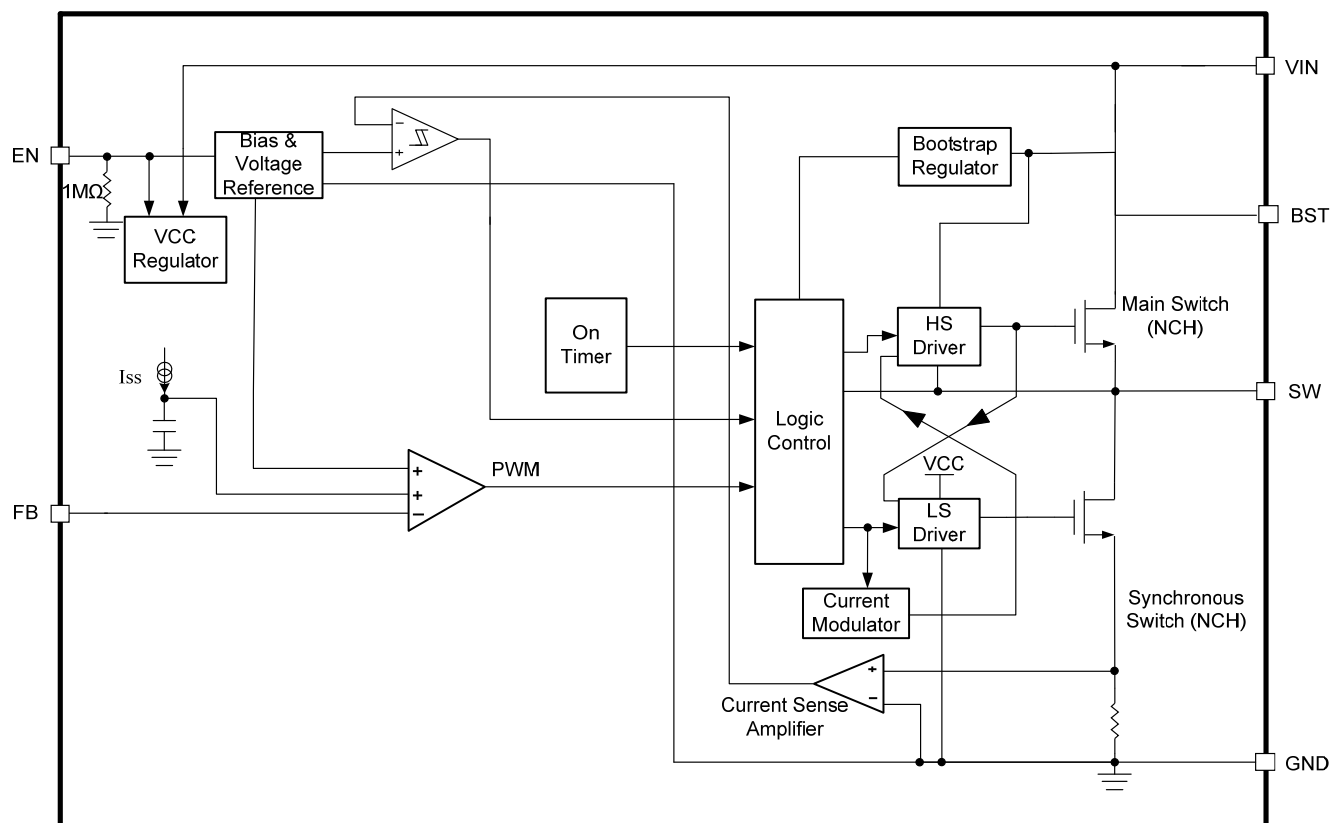


Figure 1: Functional Block Diagram

OPERATION

The MP1653 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off until the next period begins. By repeating this operation, the converter regulates the output voltage.

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps. The low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To prevent a shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

When the MP1653 works in pulse-frequency modulation (PFM) mode during light-load operation, the MP1653 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver enters tri-state (high-Z). The output capacitors discharge slowly to GND through R1 and R2. When V_{FB} drops below the reference voltage, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does in heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter,

and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The MP1653 reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Enable (EN)

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to the voltage on VIN limits the EN input current below 100μA, preventing damage to the Zener diode.

For example, if connecting 12V to VIN, then $R_{PULLUP} \geq (12V - 2.8V) / (100k\Omega + 35k\Omega) = 68\mu A$.

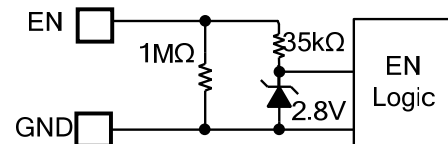


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1653 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4V, while its falling threshold is consistently 3.67V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft start voltage (V_{SS}) that ramps up from 0V to 1.2V. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 2.5ms internally.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP1653 has a valley current-limit control. During LS-FET on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS-FET limit comparator turns over. The device enters over-current protection (OCP) mode, and the HS-FET waits until the valley current limit disappears before turning on again. The output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 75% below the reference). Once UV is triggered, the MP1653 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Pre-Bias Start-Up

The MP1653 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 3). If $V_{IN} - V_{SW}$ exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

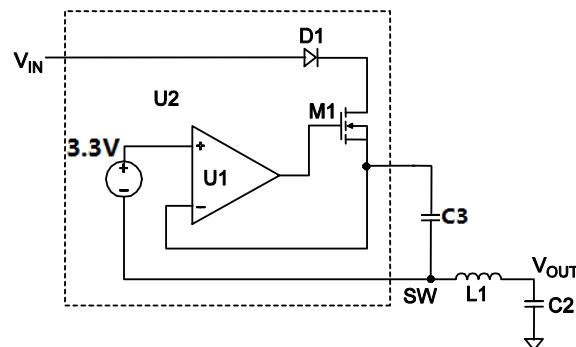


Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The COMP voltage (V_{COMP}) and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. Choose a value for R2 carefully, since a small R2 can lead to considerable quiescent current loss, but a large R2 can make FB noise sensitive. It is recommended for R2 to be between 5kΩ - 100kΩ. Typically, an R2 current value between 5μA - 30 μA achieves a good balance between system stability and no-load loss. R1 can be determined with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

The feedback circuit is shown in Figure 4.

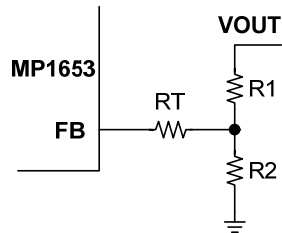


Figure 4: Feedback Network

Table 1 lists the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages ⁽⁸⁾

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
5	40.2	7.68	75	3.3
3.3	40.2	13	75	2.2
2.5	40.2	19.1	100	2.2
1.8	40.2	32.4	110	1.5
1.5	40.2	45.3	147	1.5
1.2	40.2	82	147	1
1	20.5	84.5	249	1

NOTE:

8) For a detailed design circuit, please refer to the Typical Application Circuits on page 16 to page 18.

Selecting the Inductor

An inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining

the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% to 60% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

The output voltage ripple caused by ESR is very small.

In the case of POSCAP capacitors, ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value (C_{O_MAX}) can be limited approximately with Equation (12):

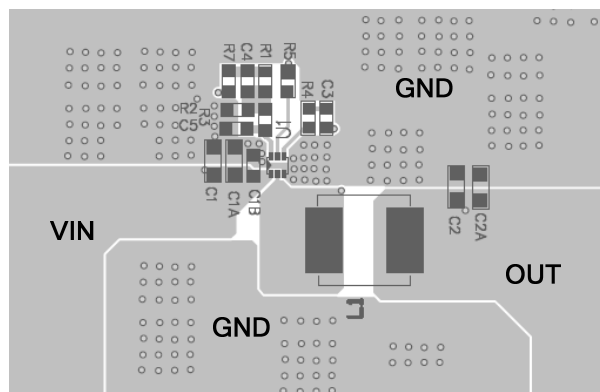
$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{SS} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{SS} is the soft-start time.

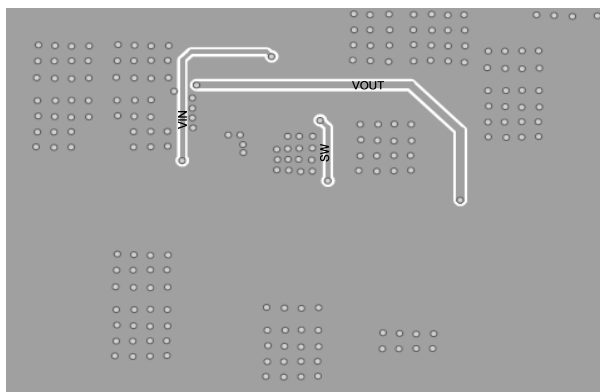
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 5 and follow the guidelines below.

- 1) Place the high current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
- 2) Place the input capacitor as close to IN and GND as possible (recommended within 1mm).
- 3) Place the external feedback resistors next to FB.
- 4) Keep the switching node (SW) short and away from the feedback network.



Top Layer



Bottom Layer

Figure 5: Sample Board Layout

Design Example

Table 2 shows a design example when ceramic capacitors are applied.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	3A

The detailed application schematic is showed in Figure 7. The typical performance and waveforms are shown in the Typical Performance Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

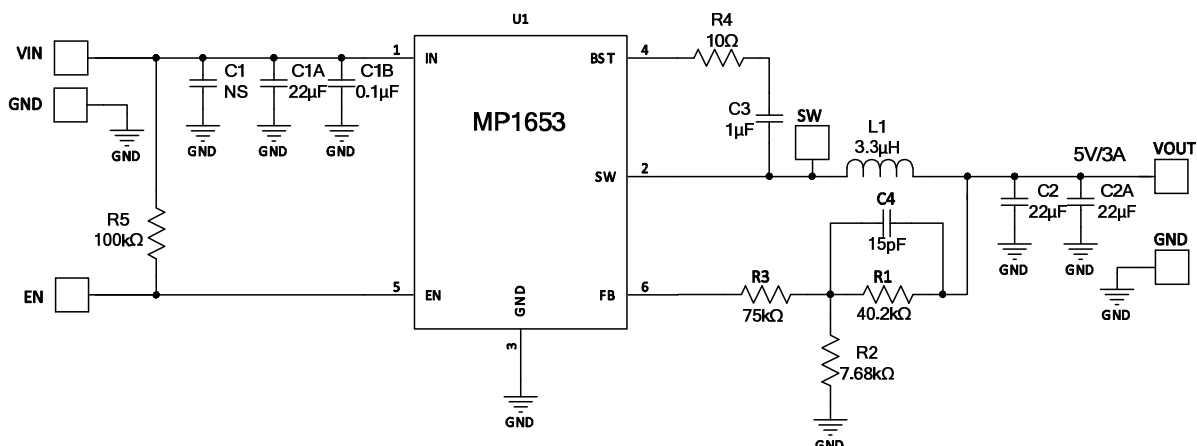


Figure 6: $V_{IN} = 12V$, $V_{OUT} = 5V/3A$

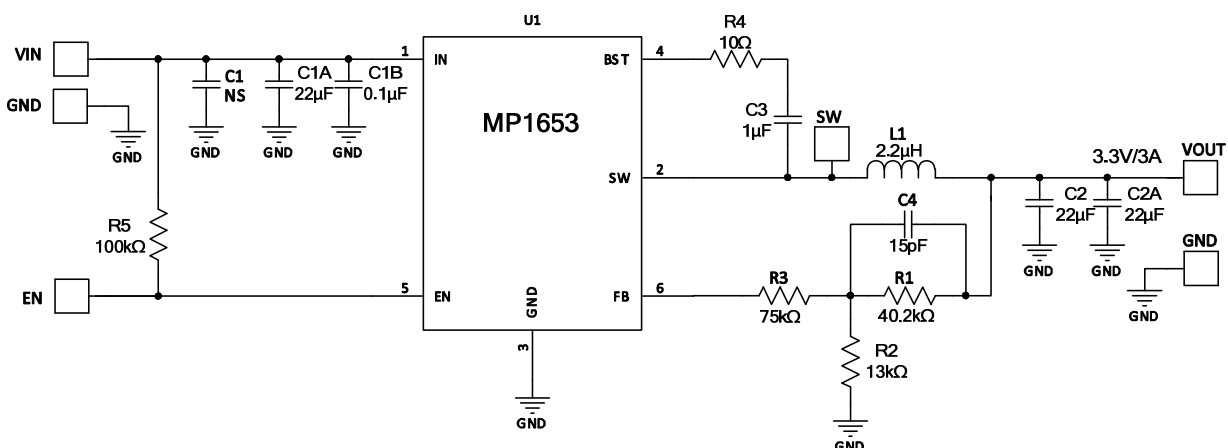


Figure 7: $V_{IN} = 12V$, $V_{OUT} = 3.3V/3A$

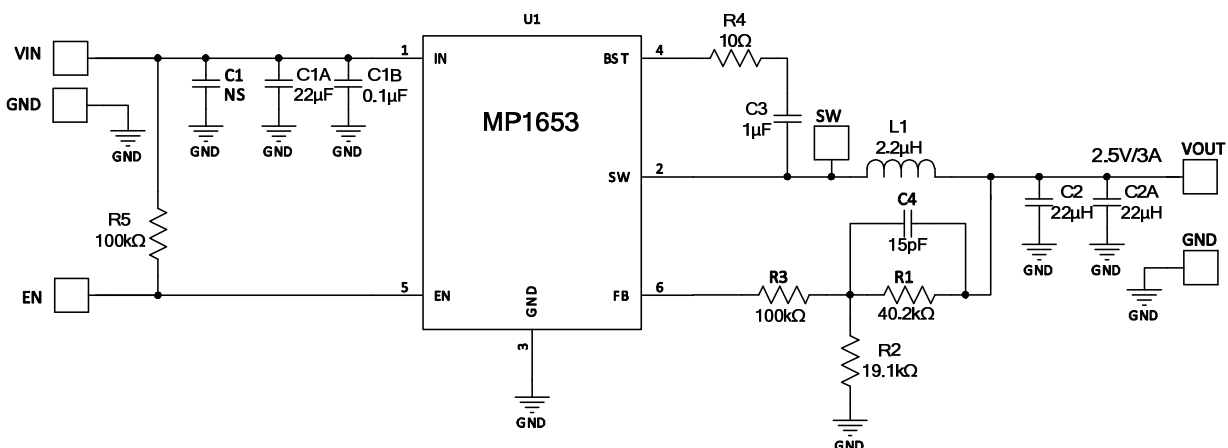


Figure 8: $V_{IN} = 12V$, $V_{OUT} = 2.5V/3A$

TYPICAL APPLICATION CIRCUITS *(continued)*

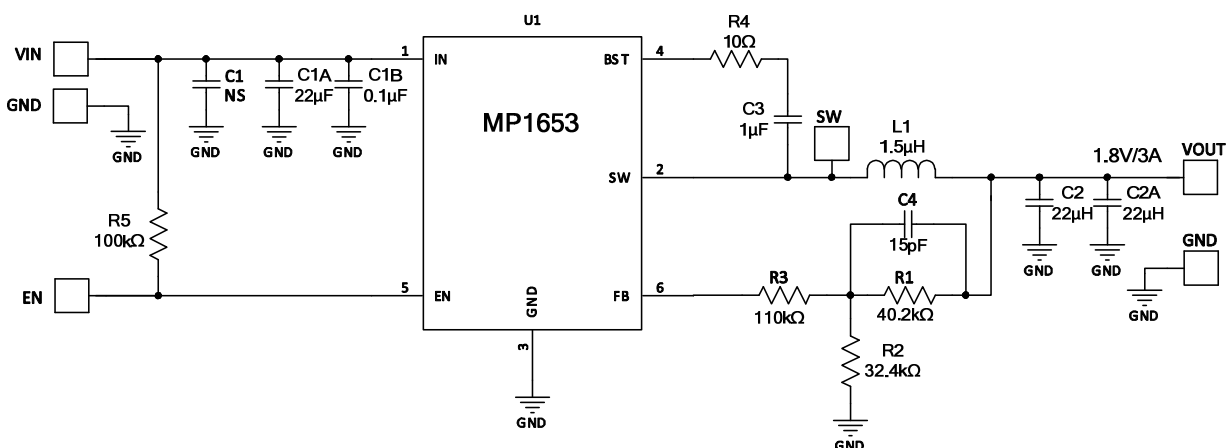


Figure 9: $V_{IN} = 12V$, $V_{OUT} = 1.8V/3A$

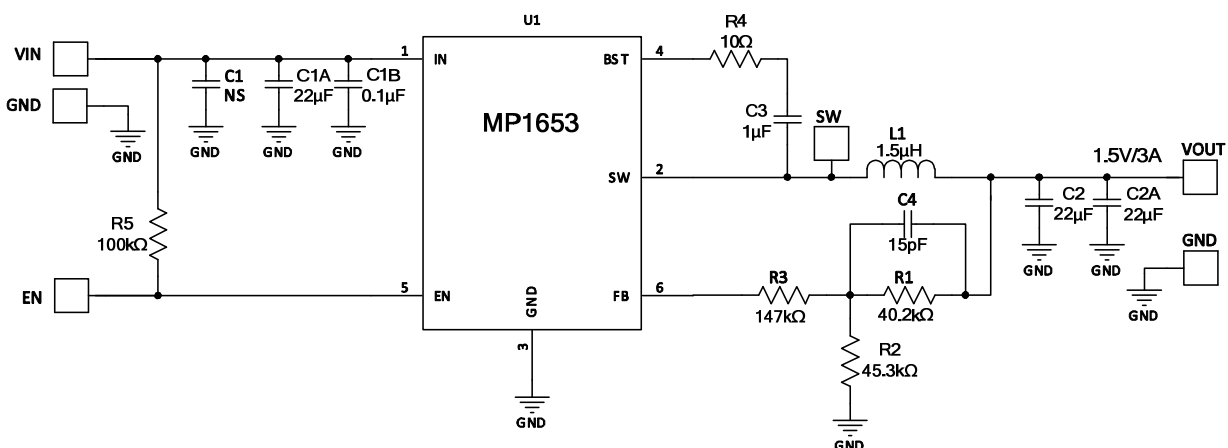


Figure 10: $V_{IN} = 12V$, $V_{OUT} = 1.5V/3A$

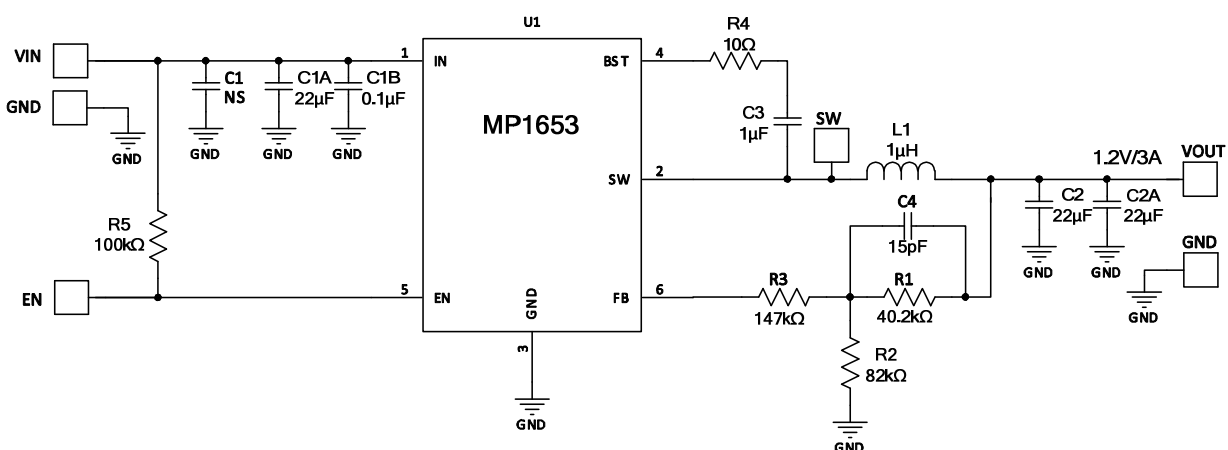


Figure 11: $V_{IN} = 12V$, $V_{OUT} = 1.2V/3A$

TYPICAL APPLICATION CIRCUITS *(continued)*

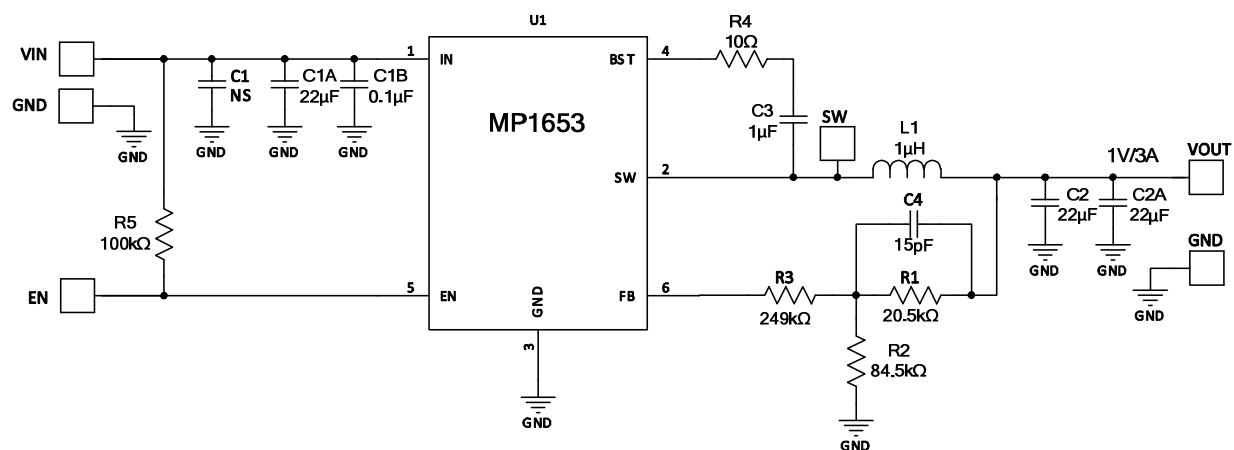
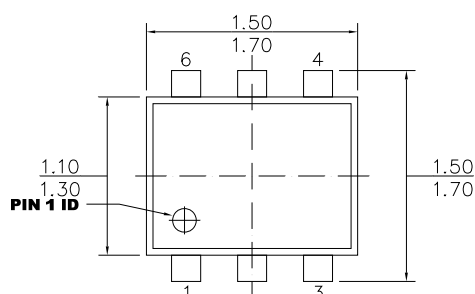


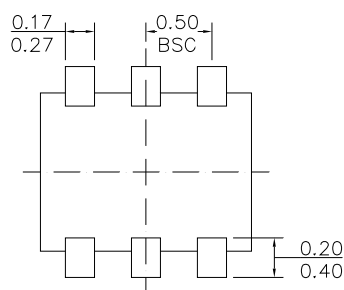
Figure 12: $V_{IN} = 12V$, $V_{OUT} = 1V/3A$

PACKAGE INFORMATION

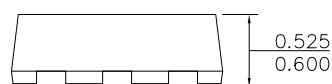
SOT563 (1.6mmx1.6mm)



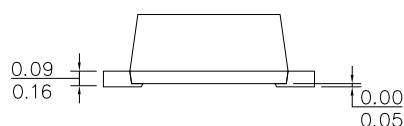
TOP VIEW



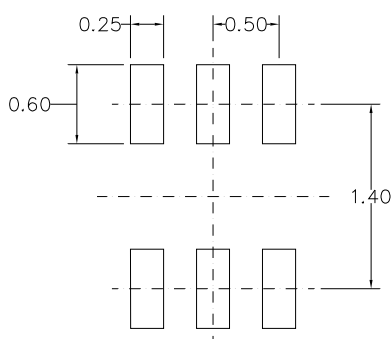
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING IS NOT TO SCALE.

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