

INTEL UNNATI INDUSTRIAL TRAINING SUMMER 2023

PROBLEM
STATEMENT

**DESIGN & IMPLEMENTATION OF SLOW AND
FAST DIVISION ALGORITHM IN COMPUTER
ARCHITECTURE**

NAME

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TEAM NAME

FIXER

TEAM SIZE

1

MENTOR NAME

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FAST DIVISION ALGORITHM

In this method, the quotient is predicted to the closest approximation to the actual quotient, and then the calculation starts. The algorithms for fast division can be done through the methods Newton–Raphson, and Goldschmidt.

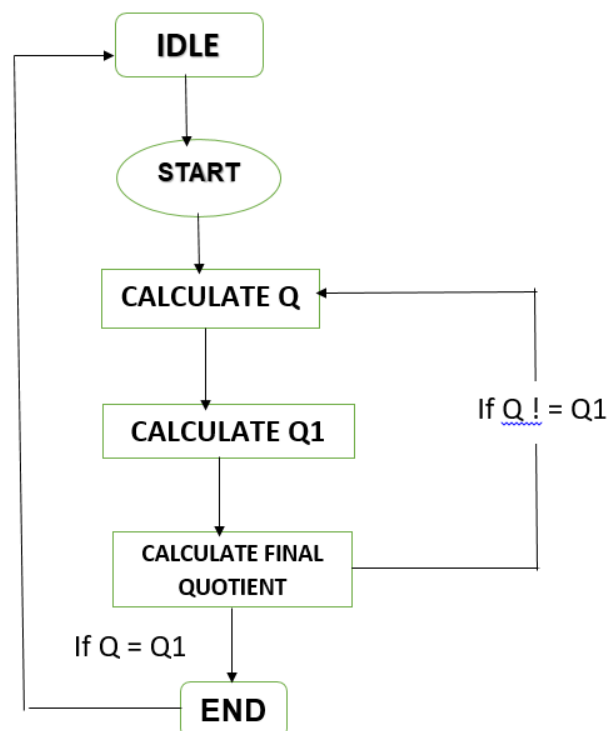
NEWTON-RAPHSON DIVISION ALGORITHM

Newton-Raphson's division algorithm is an iterative method used to approximate the division operation. It is based on finding roots of equations. The algorithm aims to find the reciprocal of the divisor and then multiply it with the dividend to obtain the quotient.

Here are the steps involved in Newton-Raphson's division algorithm:

1. Initialize the reciprocal estimate (Q) to an initial guess, such as $1/\text{divisor}$.
2. Update the reciprocal estimate using the formula:
 $Q1 = Q * (2 - \text{divisor} * Q)$.
3. Repeat step 2 until the reciprocal estimate converges to a desired accuracy (i.e., $Q = Q1$).
4. Calculate the quotient by multiplying the dividend with the final reciprocal estimate (Q1).

MEALY STATE MACHINE



MANUAL CALCULATION

TEST CASE (1)

Dividend = 7 ; Divisor = 2

1) $Q = 1/\text{divisor} = 0.5$

2) $Q1 = Q (2 - \text{divisor} (Q))$
 $= 0.5 (2 - 2 (0.5))$
 $= 0.5$

3) As $Q = Q1$

Final quotient = Dividend * Q1
 $= 7 * 0.5$
 $= 3.5$

TEST CASE (2)

Dividend = 13 ; Divisor = 4

1) $Q = 1/\text{divisor} = 0.25$

2) $Q1 = Q (2 - \text{divisor} (Q))$
 $= 0.25 (2 - 4 (0.25))$
 $= 0.25$

3) As $Q = Q1$

Final quotient = Dividend * Q1
 $= 13 * 0.25$
 $= 3.25$

VERILOG CODE

```
module fast_division1 (
    input wire clk,
    input wire start,
    input wire [3:0] dividend,
    input wire [3:0] divisor,
    output wire [3:0] quotient
);

    reg [10:0] Q;
    reg [10:0] Q1;
    reg [10:0] final_quotient;
    reg [2:0] state;

    always @(posedge clk) begin
        case (state)
            0: begin // Idle state, waiting for start signal
                if (start) begin
```

```

    Q <= 0;
    Q1 <= 0;
    final_quotient <= 0;
    state <= 1;
end
end
1: begin // Step 1:  $Q = (1 \ll N) / \text{divisor}$ 
    Q = ({2'b00, dividend} << 6) / divisor;
    state <= 2;
end
2: begin // Step 2:  $Q1 = Q * (2^N - \text{divisor} * Q)$ 
    Q1 = Q * ({2'b00, 2'b00, 4'b0010} << 6) - divisor * Q;
    if (Q == Q1)
        state <= 4; // Proceed to Step 4 if Q = Q1
    else
        state <= 3; // Repeat Step 2 if Q is not equal to Q1
    end
end
3: begin // Step 2 (repeat):  $Q1 = Q * (2^N - \text{divisor} * Q)$ 
    Q = Q1;
    Q1 = Q * ({2'b00, 2'b00, 4'b0010} << 6) - divisor * Q;
    state <= 2;
end
4: begin // Step 3: Calculate final quotient as dividend * Q1 >> N
    final_quotient = dividend * Q1 >> 6;
    state <= 0; // Return to Idle state
end
endcase
end

assign quotient = {final_quotient[7:4], final_quotient[3]} + (final_quotient[2] ? 1'b1 : 1'b0);

endmodule

```

TEST BENCH

```

module fast_division1_tb;

    reg clk;
    reg start;
    reg [3:0] dividend;
    reg [3:0] divisor;

```

```

wire [3:0] quotient;

fast_division1 DUT (
    .clk(clk),
    .start(start),
    .dividend(dividend),
    .divisor(divisor),
    .quotient(quotient)
);

always begin
    #5 clk = ~clk; // Toggle the clock every 10 time units
end

initial begin
    clk = 0;
    start = 0;
    dividend = 4'b0111;
    divisor = 4'b0010;

    #10;
    start = 1;
    #10;
    start = 0;
    #10;
    $display("Test case 1: dividend = %d, divisor = %d, quotient = %0d.%01d",
dividend, divisor, quotient[3:2], quotient[1]);

    dividend = 4'b1101;
    divisor = 4'b0100;

    #10;
    start = 1;
    #10;
    start = 0;
    #10;
    $display("Test case 2: dividend = %d, divisor = %d, quotient = %0d.%01d",
dividend, divisor, quotient[3:2], quotient[1]);

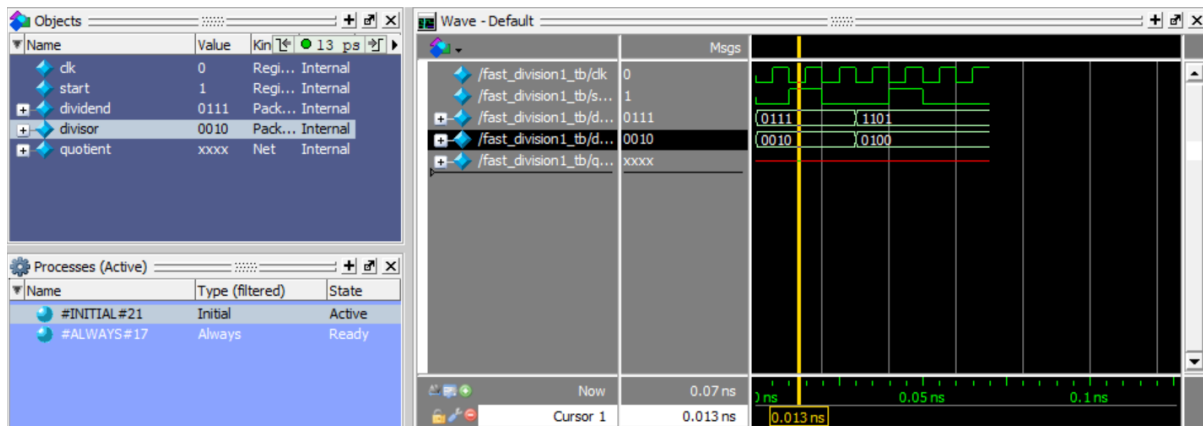
    #10;
    $finish; // End the simulation
end
endmodule

```

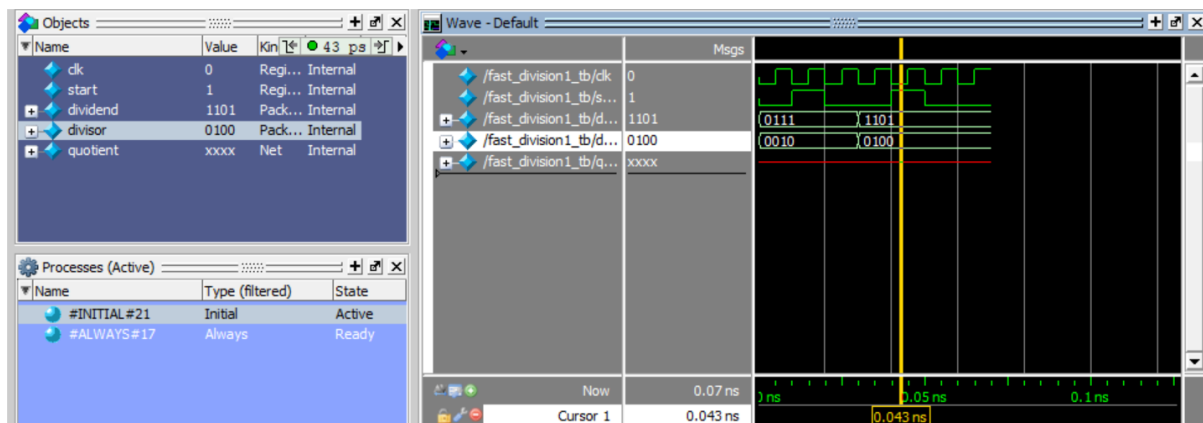
SIMULATION RESULT

```
# .main_pane.objects.interior.cs.body.tree
# run -all
# Test case 1: dividend = 7, divisor = 2, quotient = x.x
# Test case 2: dividend = 13, divisor = 4, quotient = x.x
# ** Note: $finish      : C:/unnati_fastdivision/fast_division1_tb.v(45)
#   Time: 70 ps  Iteration: 0  Instance: /fast_division1_tb
# 1
```

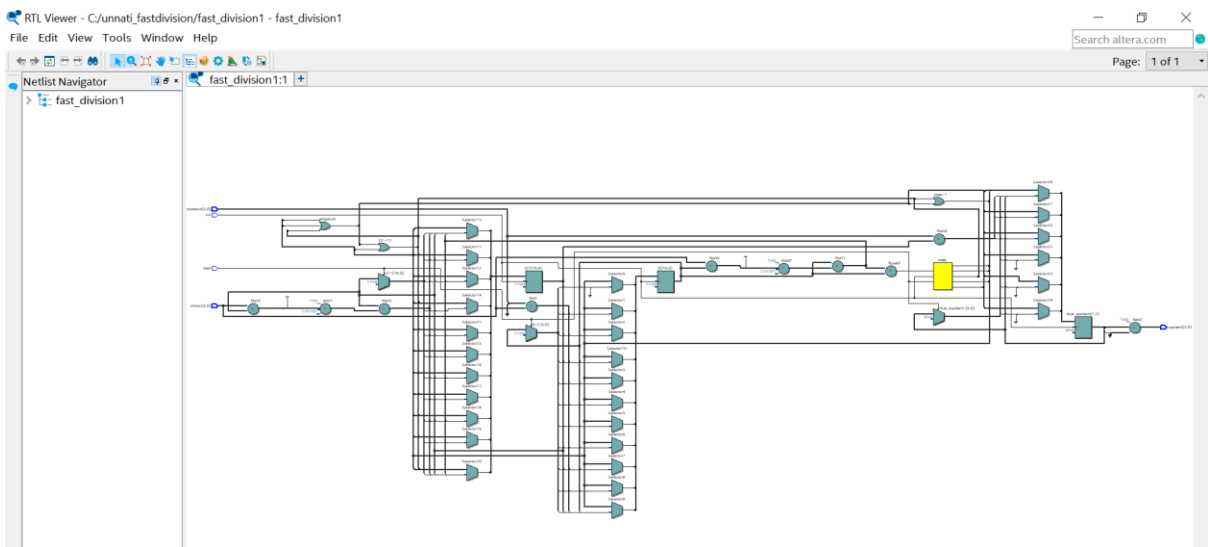
RESULT OF TEST CASE (1)



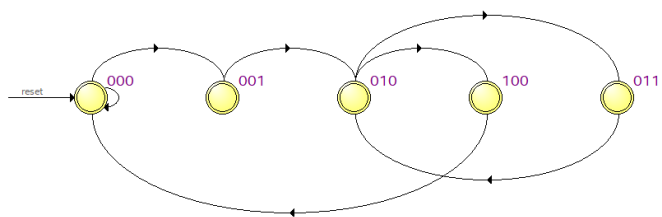
RESULT OF TEST CASE (2)



RTL VIEWER



STATE MACHINE VIEWER



State Table	Source State	Destination State	Condition
	1 000	000	(!start)
	2 000	001	(start)
	3 001	010	
	4 010	011	(!Equal0)
	5 010	100	(Equal0)
	6 011	010	
	7 100	000	

TransitionsEncoding

PIN PLANNER

Pin Planner - C:/unnati_fastdivision/fast_division1 - fast_division1
File Edit View Processing Tools Window Help

Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6

Node Name	Direction	Location	I/O Bank	/REF Group	'O Standar	Reserved	rent Stren	Slew Rate	fferential P	analog Sett	3/VCC_T_Gx	r I/O Pin Tr	ated Refcll	nmon Mod
clk	Input	PIN_AF14	3B	B3B_NO	3.3-...VTTL		16mA...ult							
dividend[3]	Input	PIN_AE11	3A	B3A_NO	3.3-...VTTL		16mA...ult							
dividend[2]	Input	PIN_AC9	3A	B3A_NO	3.3-...VTTL		16mA...ult							
dividend[1]	Input	PIN_AD10	3A	B3A_NO	3.3-...VTTL		16mA...ult							
dividend[0]	Input	PIN_AE12	3A	B3A_NO	3.3-...VTTL		16mA...ult							
divisor[3]	Input	PIN_AF9	3A	B3A_NO	3.3-...VTTL		16mA...ult							
divisor[2]	Input	PIN_AF10	3A	B3A_NO	3.3-...VTTL		16mA...ult							
divisor[1]	Input	PIN_AD11	3A	B3A_NO	3.3-...VTTL		16mA...ult							
divisor[0]	Input	PIN_AD12	3A	B3A_NO	3.3-...VTTL		16mA...ult							
quotient[3]	Output	PIN_Y19	4A	B4A_NO	3.3-...VTTL		16mA...ult	1 (default)						
quotient[2]	Output	PIN_W20	5A	B5A_NO	3.3-...VTTL		16mA...ult	1 (default)						
quotient[1]	Output	PIN_W21	5A	B5A_NO	3.3-...VTTL		16mA...ult	1 (default)						
quotient[0]	Output	PIN_Y21	5A	B5A_NO	3.3-...VTTL		16mA...ult	1 (default)						
start	Input	PIN_AA14	3B	B3B_NO	3.3-...VTTL		16mA...ult							
<<new node>>														

CHIP PLANNER

Chip Planner - C:/unnati_fastdivision/fast_division1 - fast_division1
File Edit View Tools Window Help

Report not available

Coordinate: Editing Mode: ECO - 5CSEMA5F31C6

Layers Settings

Basic

- ☒ Background
- ☐ None
- ☐ Block Utilization
- ☐ Design Partition Planner
- ☒ Logic Lock Regions
 - ☒ User-assigned Logic Lock Re...
 - ☒ Fitter-placed Logic Lock Regi...
- ☒ Clock Regions
- ☒ Overlay Objects
 - ☒ Connection Lines

Layers Settings Color Legend

Device Properties

Selected elements:

General

Device	5CSEMA5F31C6
Family	Cyclone V
Device Extents	90 x 82
ALMs	32070
Total I/Os	457
GPIOs	457
GXB Channel PMA	0
GXB Channel PCS	0

AREA REPORT

fast_division1.v

Compilation Report - fast_division1

fast_division1_tb.v

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Incremental Compilation

Pin-Out File

Resource Section

Resource Usage Sum

Partition Statistics

Input Pins

Output Pins

I/O Bank Usage

Fitter Summary

<<Filter>>

Fitter Status	Successful - Fri Jul 14 15:53:12 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	fast_division1
Top-level Entity Name	fast_division1
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	78 / 32,070 (< 1 %)
Total registers	30
Total pins	14 / 457 (3 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total RAM Blocks	0 / 397 (0 %)
Total DSP Blocks	5 / 87 (6 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

fast_division1.v

Compilation Report - fast_division1

fast_division1_tb.v

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I/O Bank Usage

Fitter Resource Usage Summary

<<Filter>>

	Resource	Usage	%
1	Logic utilization (ALMs needed / total ALMs on device)	78 / 32,070	< 1 %
2	ALMs needed [=A-B+C]	78	
1	[A] ALMs used in final placement [=a+b+c+d]	80 / 32,070	< 1 %
1	[a] ALMs used for LUT logic and registers	10	
2	[b] ALMs used for LUT logic	64	
3	[c] ALMs used for registers	6	
4	[d] ALMs used for memory (up to half of total ALMs)	0	
2	[B] Estimate of ALMs recoverable by dense packing	2 / 32,070	< 1 %
3	[C] Estimate of ALMs unavailable [=a+b+c+d]	0 / 32,070	0 %
1	[a] Due to location constrained logic	0	
2	[b] Due to LAB-wide signal conflicts	0	
3	[c] Due to LAB input limits	0	
4	[d] Due to virtual I/Os	0	
3			
4	Difficulty packing design	Low	
5			
6	Total LABs: partially or completely used	13 / 3,207	< 1 %
1	-- Logic LABs	13	
2	-- Memory LABs (up to half of total LABs)	0	

Fitter Resource Usage Summary			
<<Filter>>			
	Resource	Usage	%
1	-- Logic LABs	13	
2	-- Memory LABs (up to half of total LABs)	0	
7			
8	▼ Combinational ALUT usage for logic	140	
1	-- 7 input functions	0	
2	-- 6 input functions	4	
3	-- 5 input functions	13	
4	-- 4 input functions	25	
5	-- <=3 input functions	98	
9	Combinational ALUT usage for route-throughs	11	
10			
11	▼ Dedicated logic registers	30	
1	▼ -- By type:		
1	-- Primary logic registers	30 / 64,140	< 1 %
2	-- Secondary logic registers	0 / 64,140	0 %
2	▼ -- By function:		
1	-- Design implementation registers	30	
2	-- Routing optimization registers	0	
12			

Fitter Resource Usage Summary			
<<Filter>>			
	Resource	Usage	%
12			
13	Virtual pins	0	
14	▼ I/O pins	14 / 457	3 %
1	-- Clock pins	1 / 8	13 %
2	-- Dedicated input pins	0 / 21	0 %
15			
16	▼ Hard processor system peripheral utilization		
1	-- Boot from FPGA	0 / 1 (0 %)	
2	-- Clock resets	0 / 1 (0 %)	
3	-- Cross trigger	0 / 1 (0 %)	
4	-- S2F AXI	0 / 1 (0 %)	
5	-- F2S AXI	0 / 1 (0 %)	
6	-- AXI Lightweight	0 / 1 (0 %)	
7	-- SDRAM	0 / 1 (0 %)	
8	-- Interrupts	0 / 1 (0 %)	
9	-- JTAG	0 / 1 (0 %)	
10	-- Loan I/O	0 / 1 (0 %)	
11	-- MPU event standby	0 / 1 (0 %)	
12	-- MPU general purpose	0 / 1 (0 %)	

Fitter Resource Usage Summary			
<<Filter>>			
	Resource	Usage	%
23	-- SPI Slave	0 / 2 (0 %)	
24	-- UART	0 / 2 (0 %)	
25	-- USB	0 / 2 (0 %)	
17			
18	M10K blocks	0 / 397	0 %
19	Total MLAB memory bits	0	
20	Total block memory bits	0 / 4,065,280	0 %
21	Total block memory implementation bits	0 / 4,065,280	0 %
22			
23	Total DSP Blocks	5 / 87	6 %
24			
25	Fractional PLLs	0 / 6	0 %
26	Global signals	1	
1	-- Global clocks	1 / 16	6 %
2	-- Quadrant clocks	0 / 66	0 %
3	-- Horizontal periphery clocks	0 / 18	0 %
27	SERDES Transmitters	0 / 100	0 %
28	SERDES Receivers	0 / 100	0 %
29	ITAGs	0 / 1	0 %

POWER REPORT

Run#	ID	Message
218000		Using Advanced I/O Power to simulate I/O buffers with the specified board trace model
334003		Started post-fitting delay annotation
334004		Delay annotation completed successfully
215049		Average toggle rate for this design is 0.000 millions of transitions / sec
215031		Total thermal power estimate for the design is 420.90 mW
0		Quartus Prime Power Analyzer was successful. 0 errors, 6 warnings

TIMING REPORT

Timing Analyzer Summary	
<<Filter>>	
Quartus Prime Version	Version 18.1.0 Build 625 09/12/2018 SJ Lite Edition
Timing Analyzer	Legacy Timing Analyzer
Revision Name	fast_division1
Device Family	Cyclone V
Device Name	5CSEMA5F31C6
Timing Models	Final
Delay Model	Combined
Rise/Fall Delays	Enabled

fast_division1.v Compilation Report - fast_division1 fast_division1_tb.v Power Analyzer Tool

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 - Parallel Compilation**
 - SDC File List
 - Clocks
 - Slow 1100mV 85C Mode
 - Slow 1100mV 0C Mode
 - Fast 1100mV 85C Mode
 - Fast 1100mV 0C Mode

Parallel Compilation

<<Filter>>

	Processors	Number
1	Number detected on machine	4
2	Maximum allowed	2
3		
4	Average used	1.07
5	Maximum used	2
6		
7	▼ Usage by Processor	% Time Used
1	Processor 1	100.0%
2	Processor 2	7.0%

fast_division1.v Compilation Report - fast_division1 fast_division1_tb.v Power Analyzer Tool

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 - Clocks
 - Slow 1100mV 85C Mode
 - Slow 1100mV 0C Mode
 - Fast 1100mV 85C Mode
 - Fast 1100mV 0C Mode

SDC File List

<<Filter>>

	SDC File Path	Status	Read at
1	fast_division1_out.sdc	OK	Fri Jul 14 16:19:00 2023

fast_division1.v Compilation Report - fast_division1 fast_division1_tb.v Power Analyzer Tool

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 - Clocks

Clocks

<<Filter>>

	Clock Name	Type	Period	Frequency	Rise	Fall	Duty Cycle	Divide by
1	actual_clock	Base	20.000	50.0 MHz	0.000	10.000		

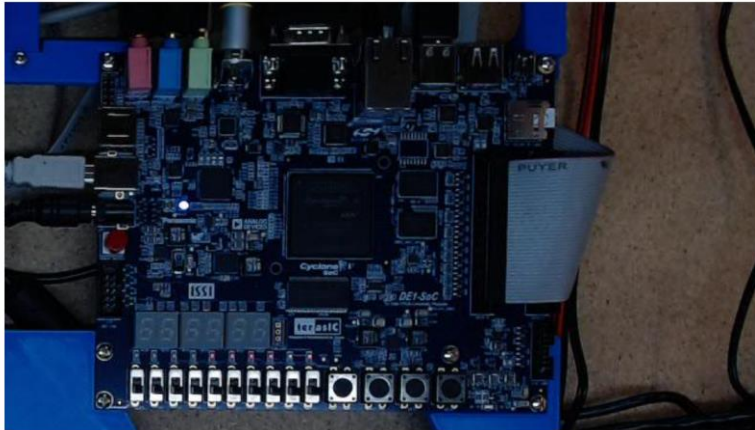
CREATION OF .sof FILE

This PC > Local Disk (C:) > unnati_fastdivision > output_files

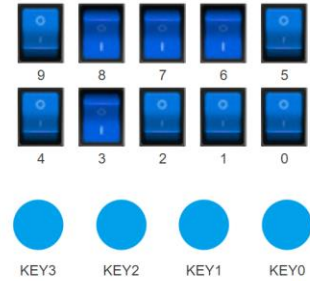
Name	Date modified	Type	Size
fast_division1.asm.rpt	14-07-2023 04:06 PM	RPT File	8 KB
fast_division1.done	14-07-2023 04:06 PM	DONE File	1 KB
fast_division1.fit.rpt	14-07-2023 03:53 PM	RPT File	277 KB
fast_division1.fit.smsg	14-07-2023 03:53 PM	SMSG File	1 KB
fast_division1.fit.summary	14-07-2023 03:53 PM	SUMMARY File	1 KB
fast_division1.flow.rpt	14-07-2023 04:06 PM	RPT File	10 KB
fast_division1.jdi	14-07-2023 04:06 PM	JDI File	1 KB
fast_division1.map.rpt	14-07-2023 03:51 PM	RPT File	35 KB
fast_division1.map.smsg	14-07-2023 03:51 PM	SMSG File	1 KB
fast_division1.map.summary	14-07-2023 03:51 PM	SUMMARY File	1 KB
fast_division1.pin	14-07-2023 03:53 PM	PIN File	104 KB
fast_division1.pow.rpt	14-07-2023 04:04 PM	RPT File	36 KB
fast_division1.pow.summary	14-07-2023 04:04 PM	SUMMARY File	1 KB
fast_division1.sld	14-07-2023 04:06 PM	SLD File	1 KB
fast_division1.sof	14-07-2023 04:06 PM	SOF File	6,534 KB

IMPLEMENTATION ON INTEL FPGA LABORATORY

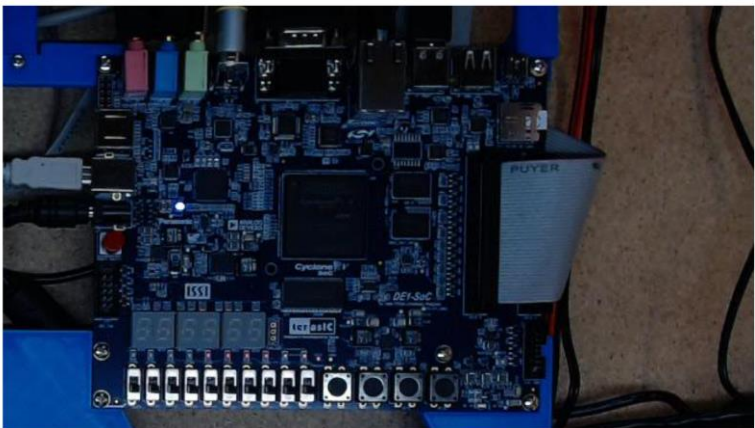
TEST CASE (1)



You are using: uw-2-de1_soc_s6i2. Experiencing any problem with this device? [Let us know](#)



TEST CASE (2)



You are using: uw-2-de1_soc_s6i2. Experiencing any problem with this device? [Let us know](#)

