East West University
Department of EEE

EEE 302: Microprocessors & Interfacing
Semester: Fall 2021
Course Instructor: FMA
Date: November 27, 2021
Section-1
Make up Midterm-1

Time: 80 minutes   **Total Marks: 80**

Answer all the questions. Do not use notes, books and mobiles

1. Suppose, we have the following values: **[10 x 4=40 marks] [CO2/APPLY]**

   For registers,

   [DS] =3E00h [ES] = 22B0h [CS] = 18D0h [SS]= 48C0h

   [BX] = 089Fh [SI] =05AEh

   [DI] = 09EDh [BP]=1BC4h.

   Generate 20-bit physical address for the following commands and

   mention is it aligned or misaligned data transfer for each case.

      (a) MOV CL, 0Eh [BP+SI]

      (b) MOV DX, 32Eh [BX]

      (c) MOV AX, CS: [SI] 11h

      (d) MOV [BP+DI], AX

      (e) MOV DX, ES: [BP] 1033h

      (f) MOV AX, EFh [SI]

      (g) MOV DX, SS: [BX] Ah

      (h) MOV AX, [BX] 09h

      (i) MOV [BP] [DI] 34h, CX

      (j) MOV CX, CS: [BX] [DI] CCh

2. In the following diagram you have the architecture of Intel 8086 microprocessor. Briefly answer the following questions: **[CO1/UNDERSTAND]**

Block Diagram of 8086 Microprocessor

Electronics Desk
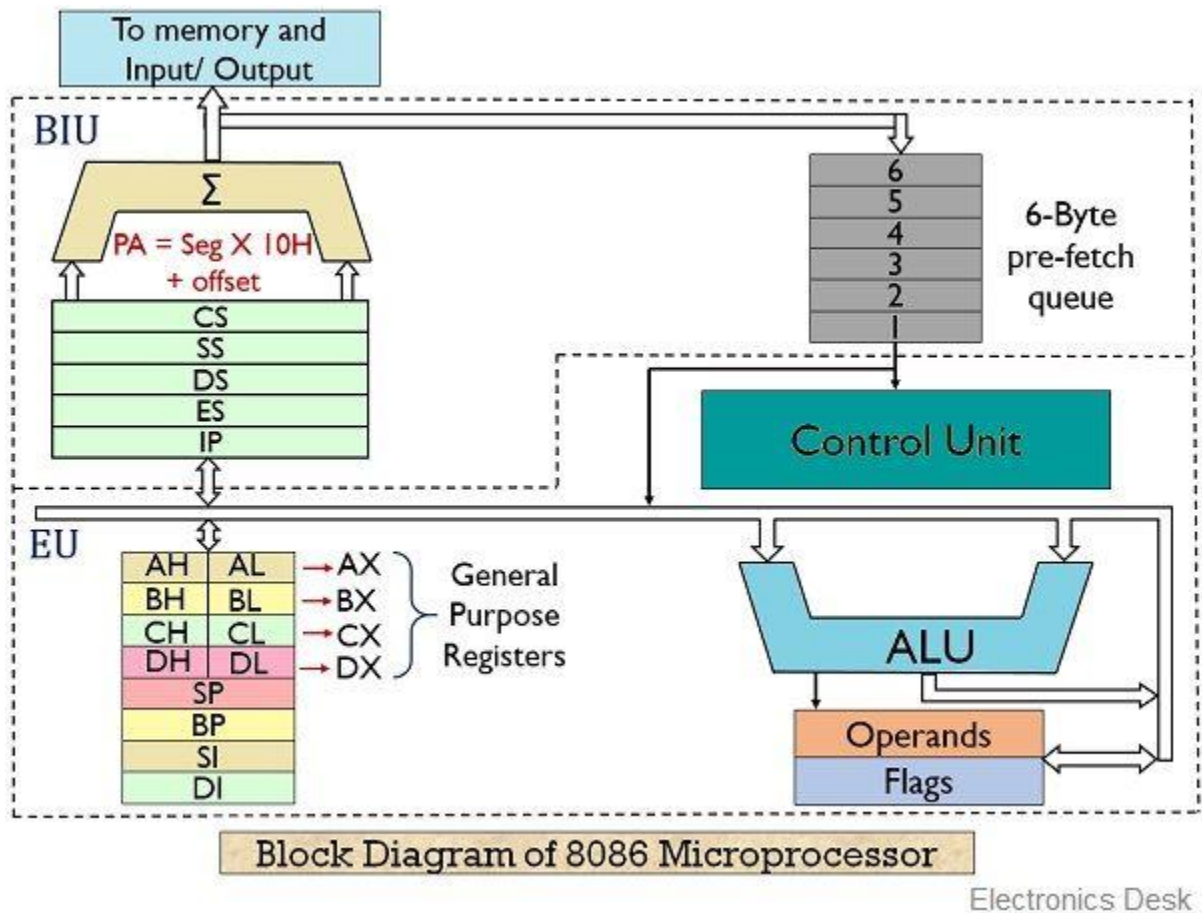
a) What is addressing mode? How many addressing modes are there for Intel 8086 for accessing memory?

b) What is the functionality of address generation circuit? Why it has two inputs and one output line?

c) How many buses are there for Intel 8086? Compare READ and WRITE operation for Intel 8086 microprocessor in terms of bus utilization.

d) What is ALU? Why it is located in execution unit, not in bus interface unit? Justify. **[4x10 =40 marks]**