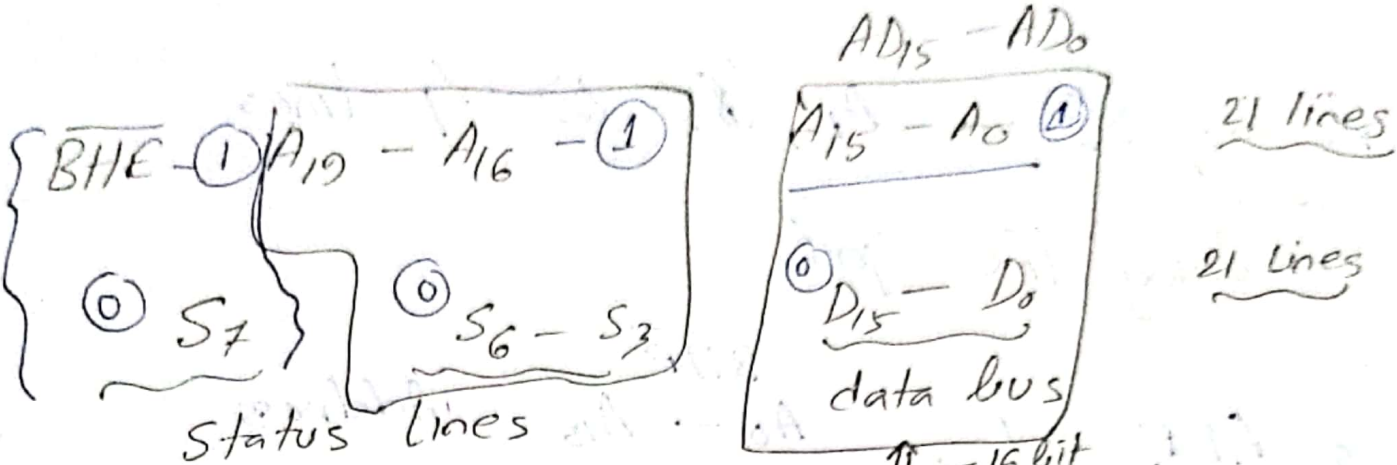


MP indicating segment currently being used.

// S_5 => 0 => IF = 0
1 => IF
} S_5 tells about IF

// S_6 => 0 => 8086 BM
1 => other BM
} indicates who is controlling the bus

// S_7 = Reserved

the one controls the bus is called bus master.

ALE = Address latch Enable

ALE indicates $AD_{15} - AD_0$ lines are carrying data or address.

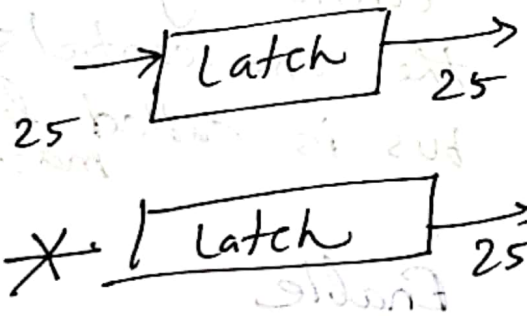
// ALE = 1, the $AD_{15} - AD_0$ bus carrying Add.

// ALE = 0, " " data.

A_{19}/S_6 — A_{16}/S_3 ⇒ 4 lines doing the job

ALE = 1 ;	$\overline{BHE}$	
	$A_0 - A_{15}$	Address
	$A_{16} - A_{19}$	"
ALE = 0 ;	$D_{15} - D_0$	data or status.
	$S_6 - S_3$	
	S_7	

What is latch?



still they will give 25.

For example. AC remote control if we reduce the temp to 21; the latch will still hold the value 21. until you changed it again.

→ A bus just transfers values.

→ Latch holds the values.

→ MP calculates the result.

→ latch that is connected between MP & display will hold the result.

→ $\overline{OE}$ = output enable. ; formality.

STB = Strobbed is a single line.

STB = 1, is allowed to enter to the latch. (Flip-flop inside)

STB = 0, the entry to the latch shuts. the previously stored value will come out.

→ Any cirwit of 8086 will need [3] 8282 latches since we have 21 lines.

→ A buffer. can be enable or disable. When enable it works as a conductor. When disable it goes into a state called high impedance state.

→ i.e. it requires infinite resistance.
that means it works as an insulator.

→ tri-state → i.e. neither at logic 1 nor logic 0.,
where buses carrying nothing.

→ if $\overline{OE}$ permanently grounded,
it will pass both add & data.

→ so, we enable $\overline{OE}$ line only
when $\overline{DEN}$ = data enable ; data has arrived.

$\overline{DEN} = 0$; $\overline{OE} = 0$.

T pin $\begin{cases} T = 1 , \overline{Tx} \\ T = 0 , Rx \end{cases}$ DT/$\overline{R}$

/ ALE = 1

21 lines carries address
Add. will go to 8286. but will do nothing

$\overline{DEN} = 1$. so data will not work.

//

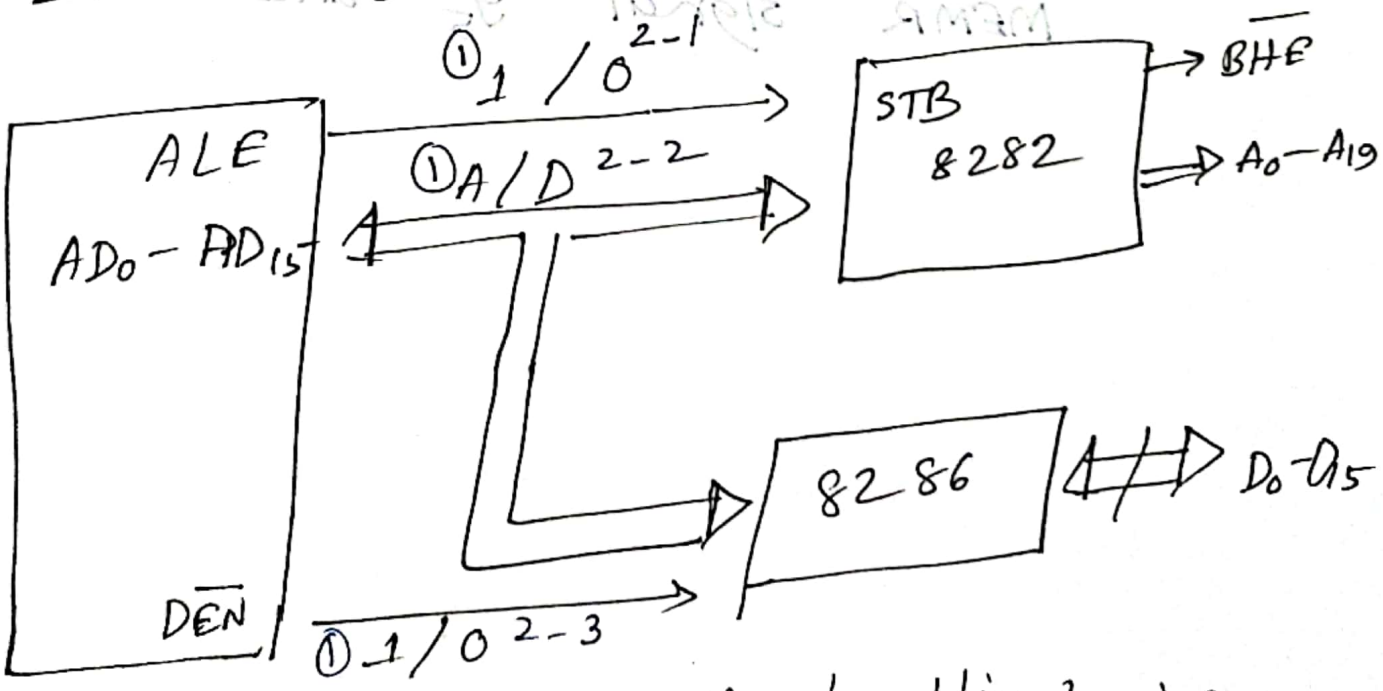
// ALE = 0, $\overline{DEN}$ = 0

. data will go 8286, data enable will be activated, ~~but~~ DT/$\bar{R}$ depends. is it 0/1. But 8282 latch will be shut down.

So, ALE & $\overline{DEN}$ both are same. but their are not the same in timing diagram.

→ The Question is who will change 1st ?

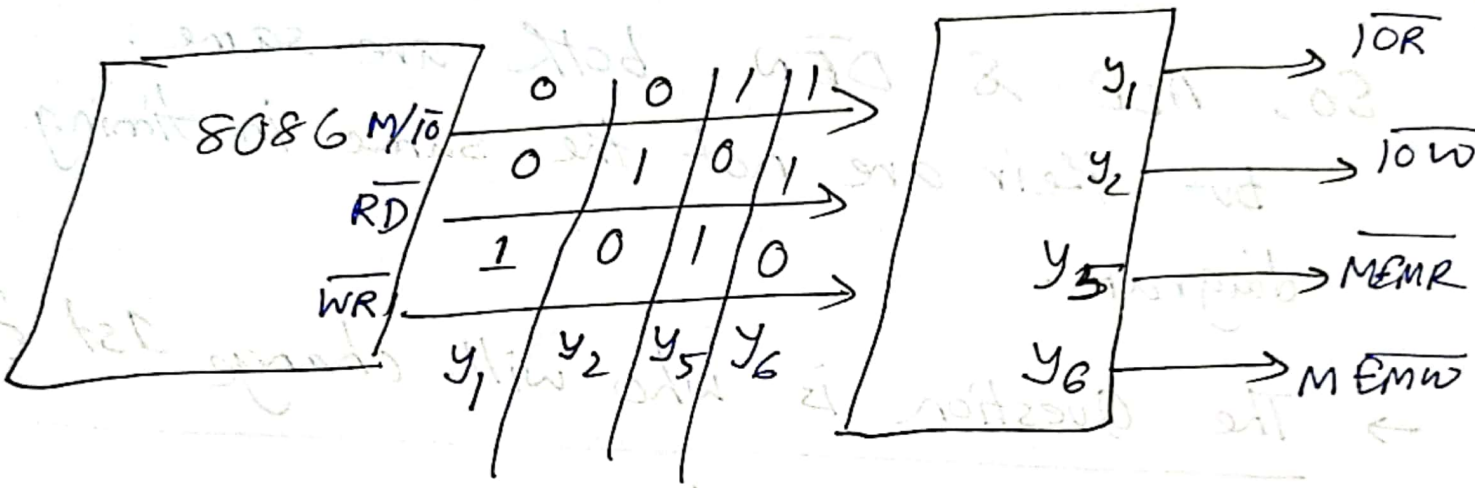
• if $\overline{DEN}$ = 1, 1st, 21 lines carrying the address cannot ~~end~~ do anything inside 8286.



this is the demultiplexing of Add/data lines.

8286 → 2 ~~latches~~

8282 → 3 latches



// RD → 0 1 0 1 only read operation.

// For RAM, we should activate read MEMR signal y_5 line.