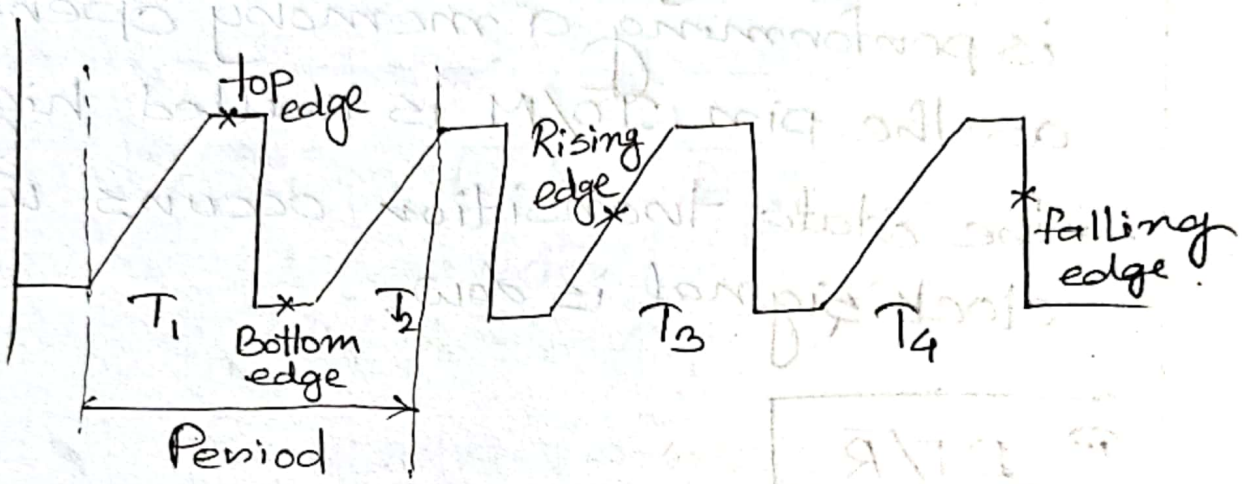
# Intel 8086 Bus timing Diagram

(Parts of a waveform)




## Diagram:

① MN/$\overline{MX}$

→ MN = $min^M$ mode

→ MX = $Max^m$ mode.

→ In the timing diagram here the state transition occurs when the clock signal is low.

→ Also the signal implies that the MPU is operating in $min^M$ mode.

→ If the MPU is operating in $Max^m$ mode, the signal would be at low.

what is happening?
When it is happening? (T1-T4)
How long it is going on? (i.e. 3 clock period/2 clock period/1 clock period?

## (II) $\overline{IO}/M$.

→ Input-output/Memory access.
→ Here the signal implies that the MPU is performing a memory operation as the pin $\overline{IO}/M$ is pulled high.
→ the state transition occurs when the clock signal is low.

## (III) $DT/\overline{R}$

→ $DT/\overline{R}$ stands for data transmit/receive.
→ transmit → WRITE
Receive → READ.
from memory or I/O Port.
→ In this diagram READ is occuring along with the falling edge of the clock period.

## (IV) Top four address Lines:

→ Here, for Intel 8086 $A_{16}$-$A_{19}$ are multiplexed with the status Lines $S_3$ to $S_6$.
→ During $T_1$ period, this set of pins carries address information. $A_{16}$ to $A_{19}$.

→ Subsequently for remaining 2 clock signals.

→ the address pins carries status information, which is used to indicate various operational states of the MPU. In this case $S_5$ memory operation.

(V) $A_0 - A_{15}$ are the bottom 16 bit address lines

→ these address lines are multiplexed with data signals ~~$A_0$ to $A_{15}$~~ D0-D15

→ then there is a tri-state / float condition for 1 clock period.

→ for the remaining 2 clock periods these pins carries data info, where it acts as a data bus.

(VI) Address Latch Enable (ALE)

→ At the falling edge of ALE pin, the MPU guarantees that the address will be valid.

(VII) $\overline{RD}$ → here the MPU is reading info from memory.

→ here the MPU expects external devices to guarantee info on the data bus to read info at the rising edge of $\overline{RD}$ signal.

# DEN - data enable:

→ it is the period during which data is guaranteed by the MPU.

→ external electronic devices, such as memory chips & I/O are designed to match the requirements.

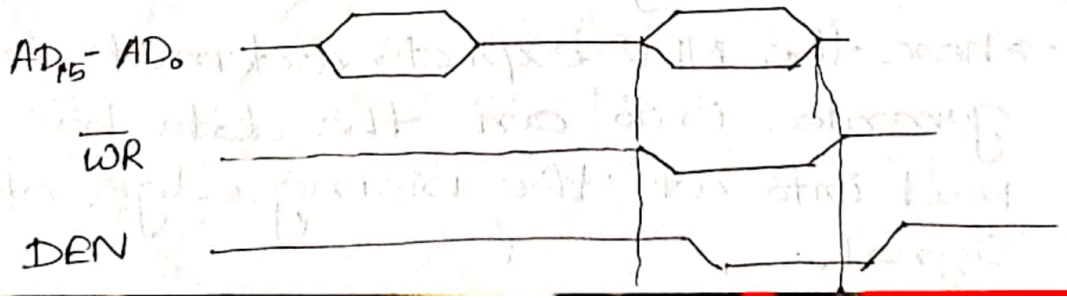
# Ready:

The external peripheral device when slower, pulls the ready line high.

→ Once the ready line is pulled high, the MPU enters in a WAIT State & It will continue to be in WAIT state, till the READY line is pulled ~~high~~ LOW.

⸗ Read pin started when address out is ended.

⸗ float can increase or decrease depends on user ($AD_{15}$ - $AD_0$).



$\overline{RD}/\overline{WR}$ from $T_2$ bottom edge to $T_4$ bottom edge } 2 clock periods.

DEN → $T_2$ → top edge → start
$T_4$ → bottom edge → end } 1.5 clock periods.

## Flowdiagram