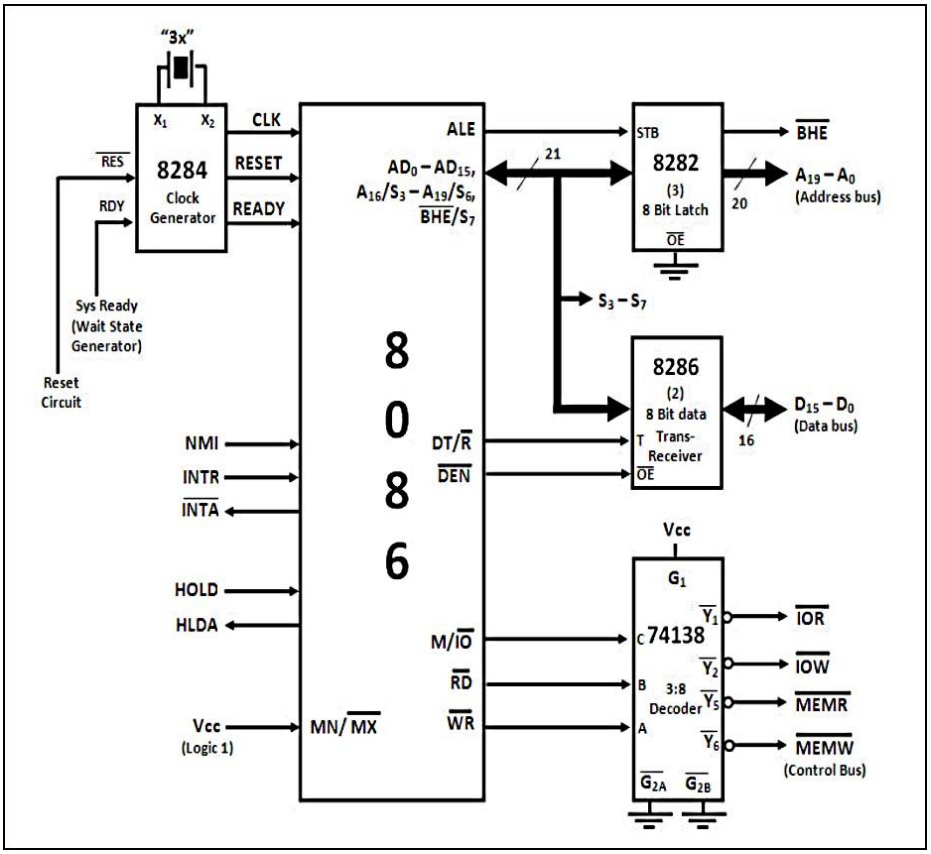
East West University
Department of EEE

EEE 302: Microprocessors & Interfacing
Semester: Spring 2022
Final Examination
Course Instructor: FMA
May 12, 2022
Section-1

Time: 90 minutes **Total Marks: 90**

1. In the following diagram, you have the **minimum mode** configuration. Answer the following questions: CO2/APPLY

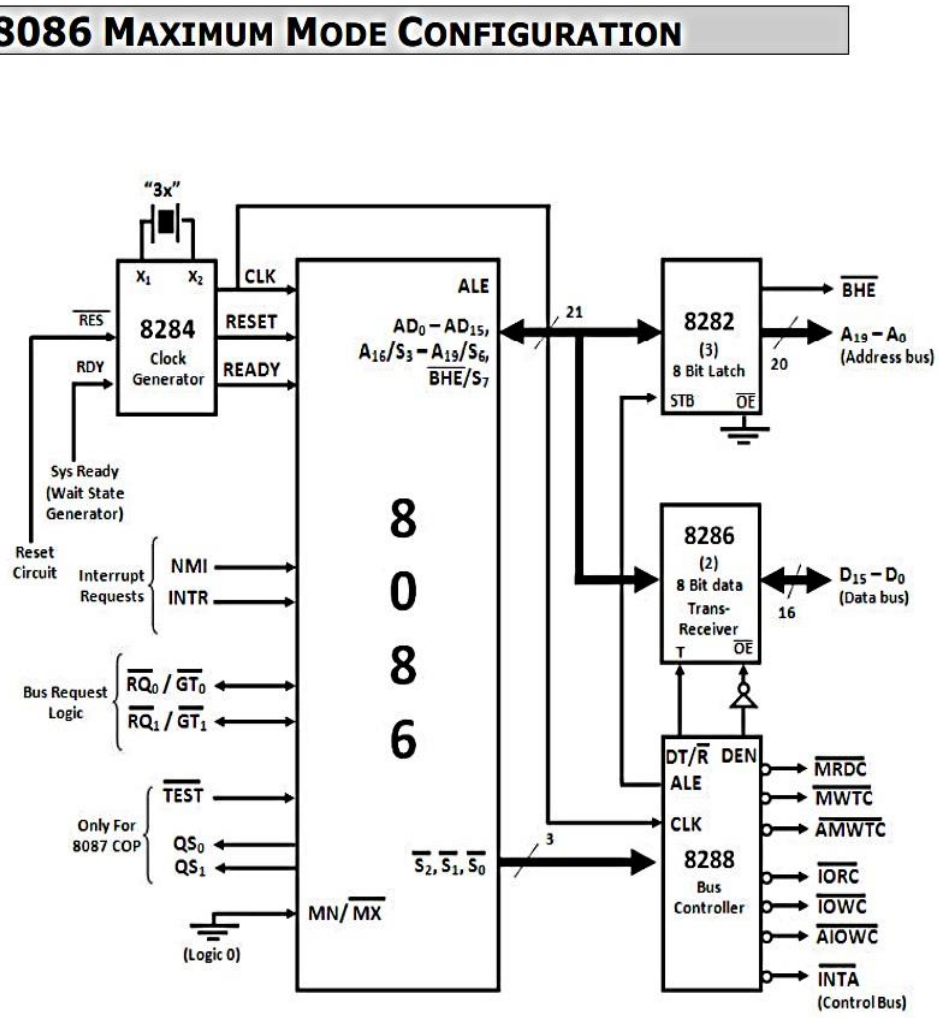


a. How do ALE and DEN pins synchronize together? How does it improve the total performance of the Intel 8086 microprocessor? [10 marks]

b. Explain the generation of control signals preferably via a truth table. What will happen to the unexploited pins for IC 74138? [10 marks]

c. What is the significance of using an 8284-clock generator? Why is it connected to an 18 MHz Oscilloscope? [10 marks]

2. In the following diagram you have the **maximum mode** configuration. Answer the following questions: **CO2/APPLY**

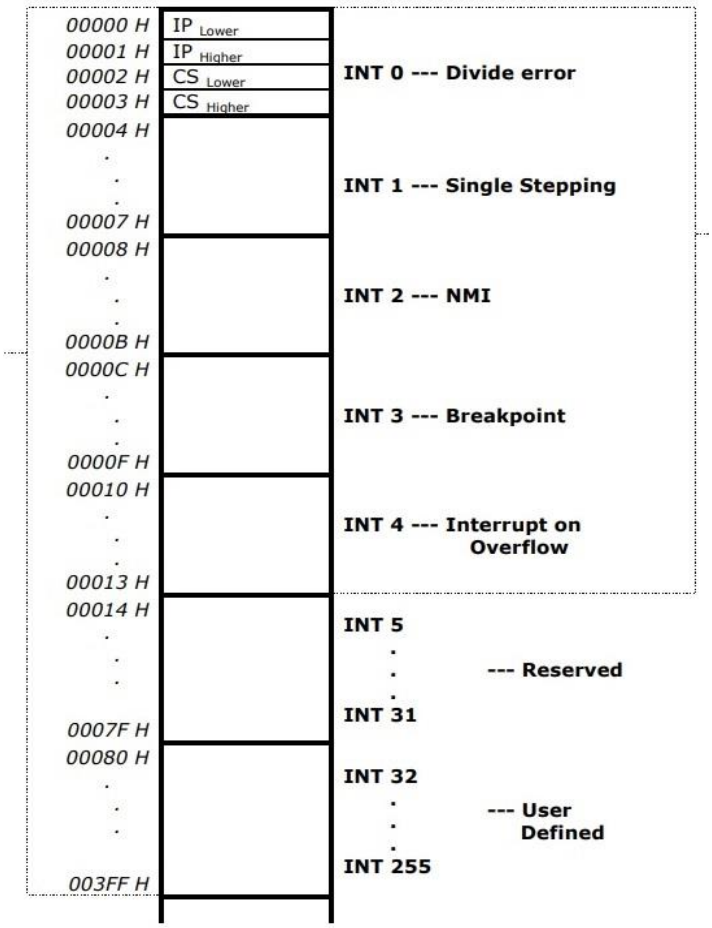


a. How does the bus controller IC 8288 control the IC 8282 and IC 8286 at a given time with the help of a clock generator? Briefly explain.

b. How does Intel 8086 and Intel 8087 coprocessor set up the connection in between?

[10 x 2 =20 MARKS]

3. In the following diagram you have the interrupt vector table of the Intel 8086 microprocessor. Briefly answer the following questions:



a) What is ISR? Where it can be found?

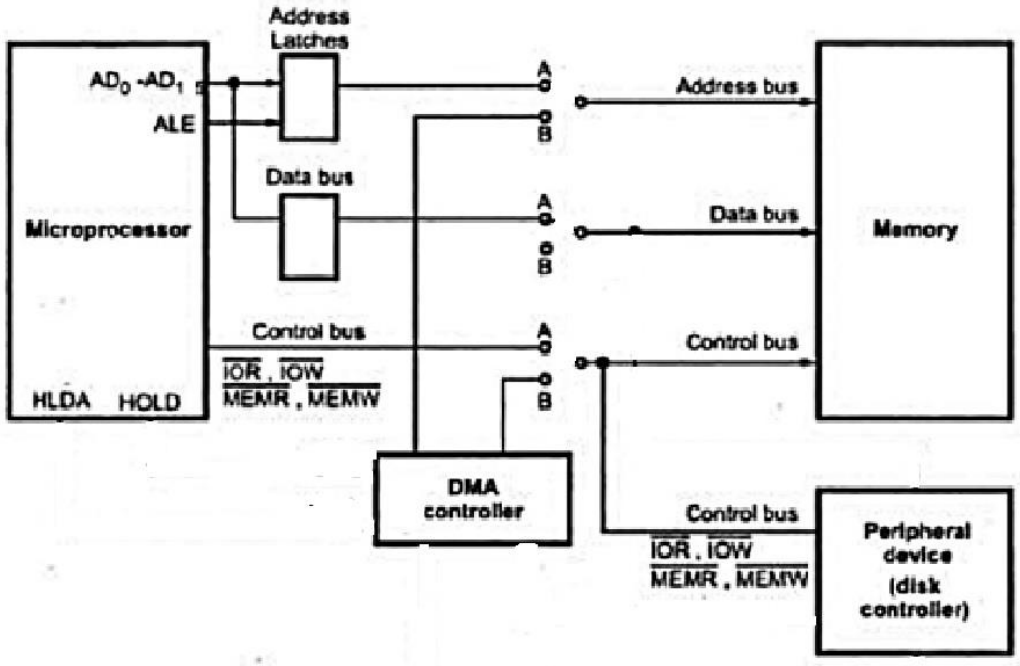
b) Why it is necessary to clear the IF and TF before servicing any ISR?

c) Why Intel 8086 microprocessor go to memory twice whenever it gets an interrupt?

CO1/ Understand [10 x 3 =30 MARKS]

4. In the following diagram, we have the **incomplete** connection diagram of DMA for the Intel 8086 microprocessor. You need to redraw the connection diagram **in the proper direction** and label the connection lines sequentially using numerical numbers only assuming Intel 8086 has responded to the DMA request. **(No explanation required)**

[10 marks] CO2/APPLY


Address Latches
AD0 -AD15
ALE
Microprocessor
HLDA HOLD
Data bus
Control bus
IOR , IOW
MEMR , MEMW
A
B
Address bus
Data bus
Control bus
Memory
DMA controller
Control bus
IOR , IOW
MEMR , MEMW
Peripheral device (disk controller)