

**CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM-II (20 Batch) EXAMINATION '2021**

DEPARTMENT	: ELECTRONICS AND TELECOMMUNICATION ENGINEERING
FULL TITLE OF PAPER	: Electronics-I
COURSE NO.	: ETE 101
FULL MARKS	: 210
TIME	: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- | | | |
|---------|---|----|
| Q.1 (a) | Describe how current is produced in a semiconductor. | 10 |
| (b) | Explain how valance electron determine the electrical properties of a material. | 10 |
| (c) | “Passive components are those that do not have gain or directionality”- Explain with proper example. | 10 |
| (d) | What happens when heat is added to silicon? | 05 |
| Q.2 (a) | Discuss the significance of the knee voltage of the characteristics curve in forward bias. | 05 |
| (b) | Explain how to connect the diodes in a center-tapped rectifier in order to produce a negative going full wave voltage across the load resistor. | 12 |
| (c) | Determine V_o and I_D for the networks of Fig.2(c). | 10 |

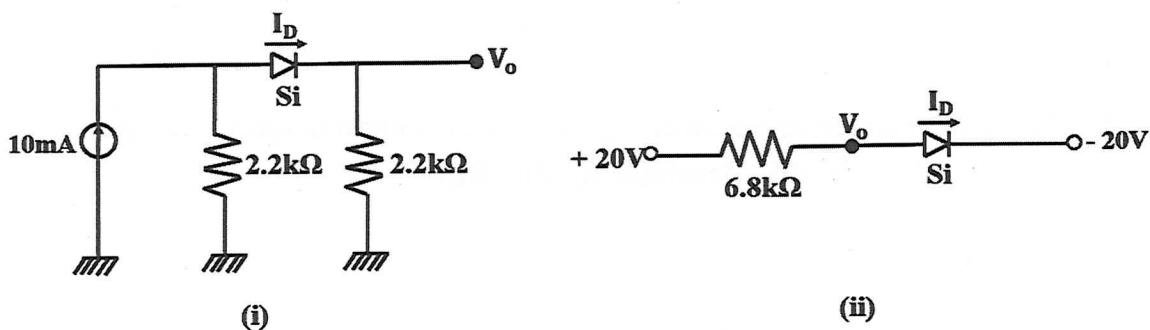


Fig. 2(c)

- | | | |
|---------|--|----|
| (d) | With necessary figures, describe the effects of temperature on the diode characteristics. | 08 |
| Q.3 (a) | In what region of the characteristic curve are zener diodes operated? Explain with figure. | 11 |
| (b) | Why are diodes not operated in the breakdown region in rectifier service? | 10 |
| (c) | Determine V_o and I_D for the networks of Fig.3(c). | 14 |

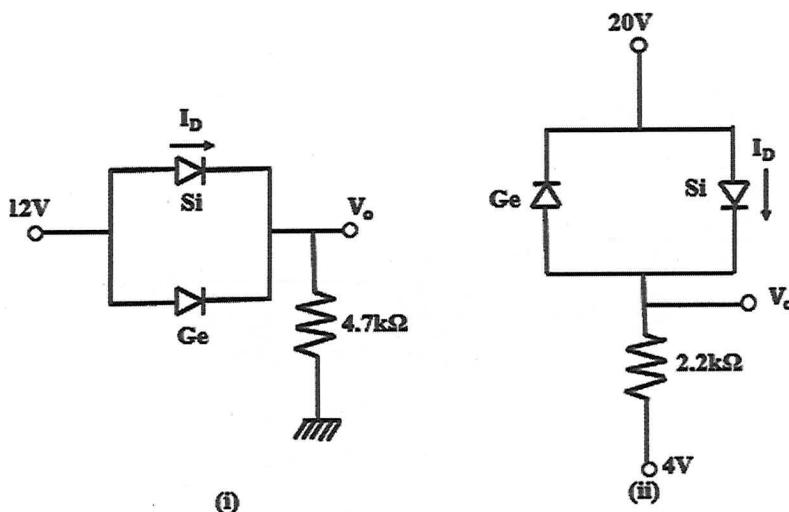


Fig. 3(c)

- Q.4 (a) What is the difference between input (line) regulation and load regulation? 05
- (b) What are the bias condition of the base-emitter and base-collector junctions for a transistor to operate as an amplifier? 10
- (c) What is power supply filter? Explain the importance of power supply filter with necessary diagram. 15
- (d) Discuss how diode limiters and diode clampers differ in terms of their function. 05

Section-B

- Q.5 (a) Explain what causes waveform distortion in BJT. 10
- (b) Determine V_C and V_B for the network of Fig. 5(b) 10

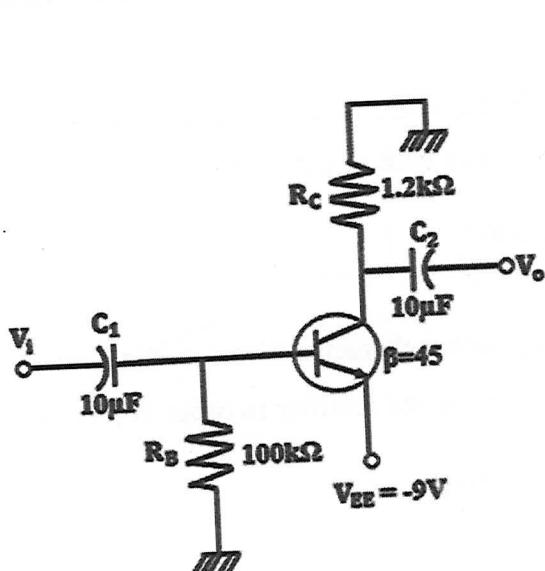


Fig. 5(b)

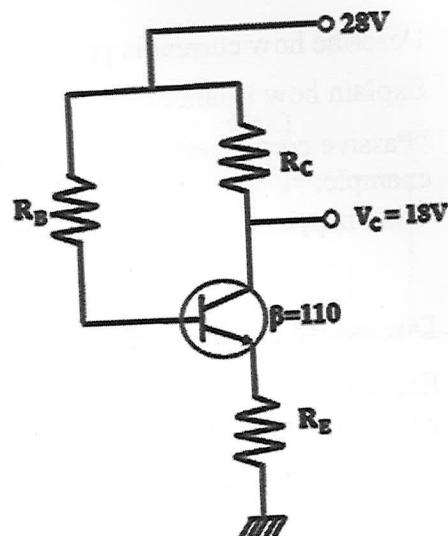


Fig. 5(c)

- (c) The emitter bias configuration of Fig. 5(c) has the following specifications: $I_{CQ} = \frac{1}{2} I_{sat}$, $I_{C_{sat}} = 8\text{mA}$, $V_C = 18\text{V}$. Determine R_C , R_E , R_B . 15

- Q.6 (a) Describe how dc input resistance at the transistor base affects the bias. 10
- (b) Determine the signal voltage at the base of the transistor in Fig. 6(b). 15

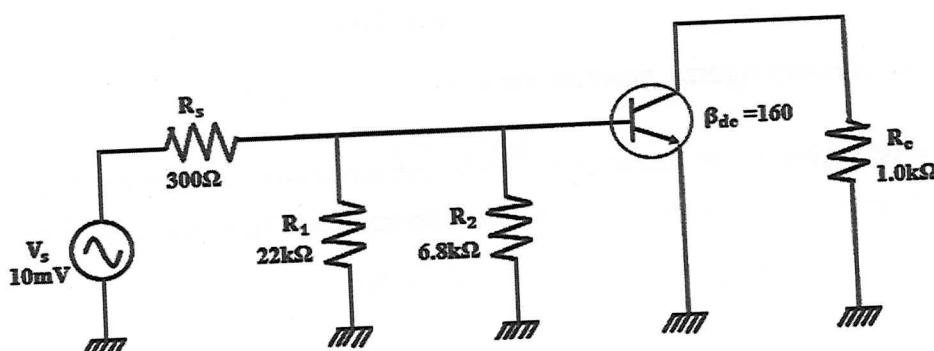


Fig. 6(b)

- (c) For the network of Fig. 6(c) determine i) Z_i ii) Z_o iii) A_v and iv) A_i 10

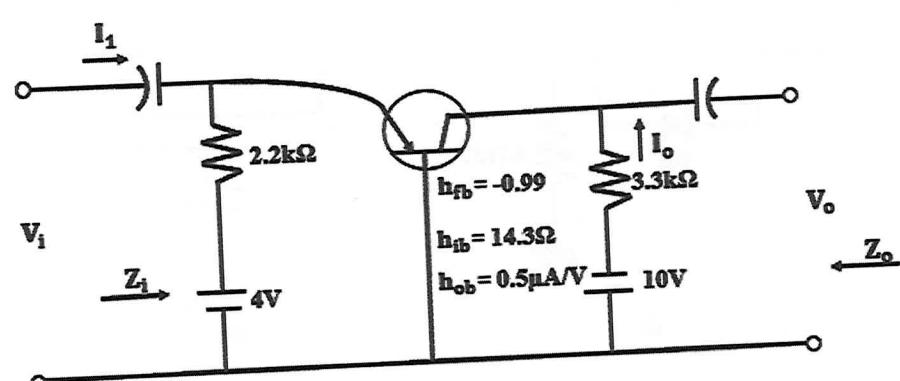


Fig. 6(c)

Q.7 (a) Describe in your own words why I_G is effectively OA for JFET transistor. 09

(b) What happens when gate-to-source voltage in an n-channel E-MOSFET is made more positive - Explain. 10

(c) Determine V_D and V_{GS} for the fixed-bias configurations of Fig. 7(c). 16

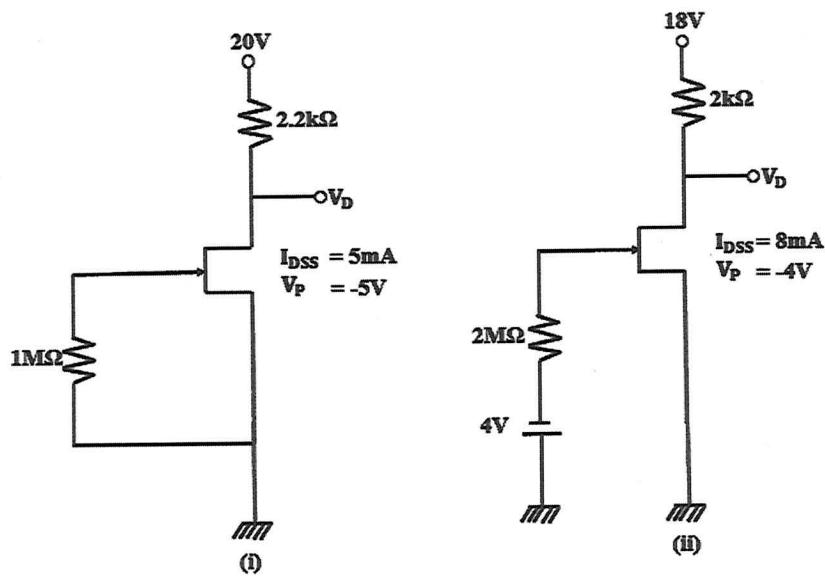


Fig. 7(c)

Q.8(a) What are the major differences between the collector characteristics of a BJT and the drain characteristics of a JFET transistor. 06

(b) For the voltage divider configuration of Fig. 8(b), determine 14

- I_{DQ} and V_{GSQ}
- V_D and V_S

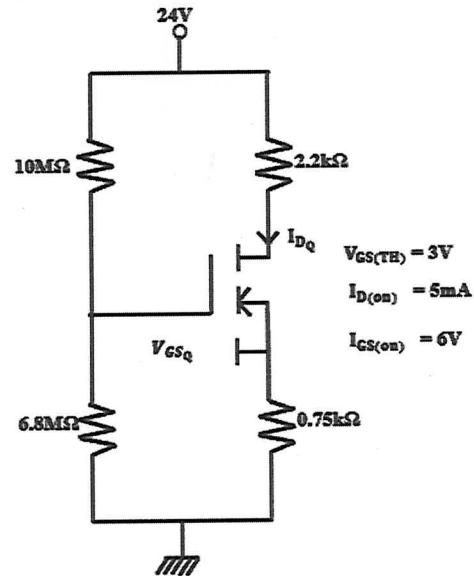


Fig. 8(b)

(c) Design a self-bias network using JFET transistor with $I_{DSS} = 8mA$ and $V_p = -6V$ to have a Q-point at $I_{DQ} = 4mA$ using a supply of 14V. Assume the $R_D = 3R_s$ 15

The End

**CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM-II (19 Batch) EXAMINATION '2020**

DEPARTMENT	: ELECTRONICS AND TELECOMMUNICATION ENGINEERING
FULL TITLE OF PAPER	: Electronics-I
COURSE NO.	: ETE 101
FULL MARKS	: 210
TIME	: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) Distinguish between electrical and electronics with proper example. 06
- (b) What is space charge region? Why is it so called? Briefly explain its formation phenomenon. 10
- (c) What do you understand by the d.c and a.c resistance of a *p-n* diode? How will you determine them from the V-I characteristic of a diode? 10
- (d) Describe the behavior of semiconductor i) at low temperature ii) at room temperature and iii) at increased temperature. 09
- Q.2(a) *n*-type materials has a net negative charge and *p*-type a net positive charge. But this calculation is wrong. Explain why? 10
- (b) Define avalanche effect as applied to diode. When does reverse breakdown occur in a diode? 15
- (c) Semiconductors are different from conductors and insulators-explain with the help of energy band diagram. 10
- Q.3(a) Determine I , V_1 , V_2 and V_o for the series dc configuration of Fig 3(a). 15

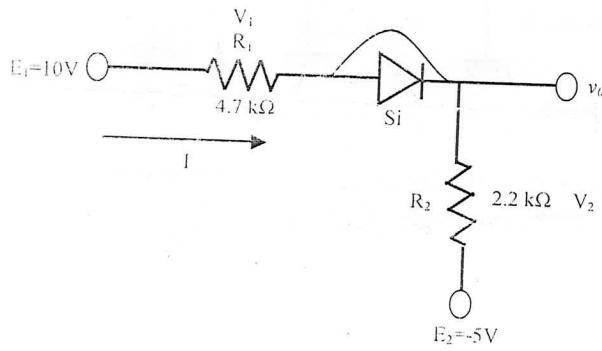


Fig. 3(a)

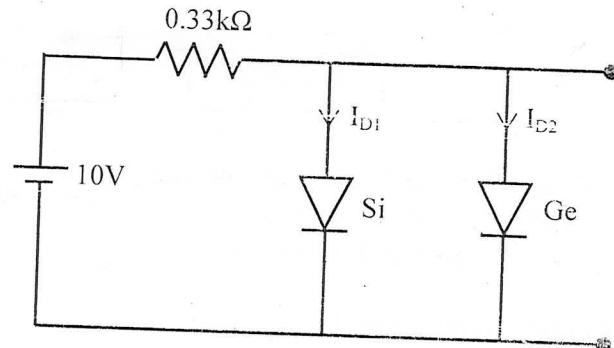


Fig. 3(b)

- (b) Determine I_{D1} and I_{D2} for Fig.3(b). 10
- (c) Write the importance of peak inversion voltage. 05
- (d) Why is output frequency get doubled of input frequency in case of full wave rectifier? 05
- Q.4(a) What is ripple factor? "A capacitor filter can reduce the ripple"-explain. 11
- (b) Draw the output responses of Fig. 4(b). 24

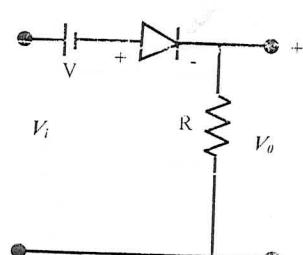
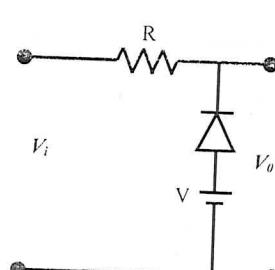
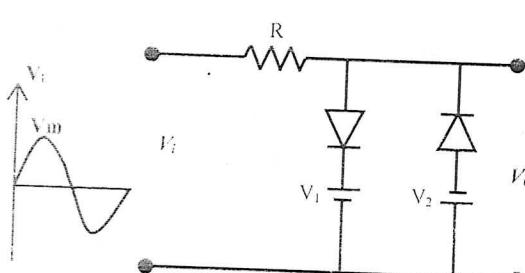


Fig. 4(b)

Section-B

- Q.5(a) With proper diagram, describe ripple voltages for half-wave and full-wave rectifier. 12
 (b) Why Zener diode is used as voltage regulator? 08
 (c) For BJT, describe the effect of an increasing level of R_C on the load line and the Q-point. 15
- Q.6 (a) What is emitter follower? Why it is called so? Write down important characteristics of emitter follower circuit. 12
 (b) How resistor ratio R_B/R_E can effect the stability factor $S(I_{co})$ in an emitter bias configuration-Explain. 10
 (c) For the capacitively coupled multi stage amplifier shown in Fig 6(c). Find 13
 (i) Voltage gain at first stage
 (ii) Voltage gain at second stage
 (iii) Overall voltage gain
 (iv) DC voltage in the capacitively coupled multistage
 $\beta_{DC} = \beta_{AC} = 150$ for Q_1 and Q_2 .

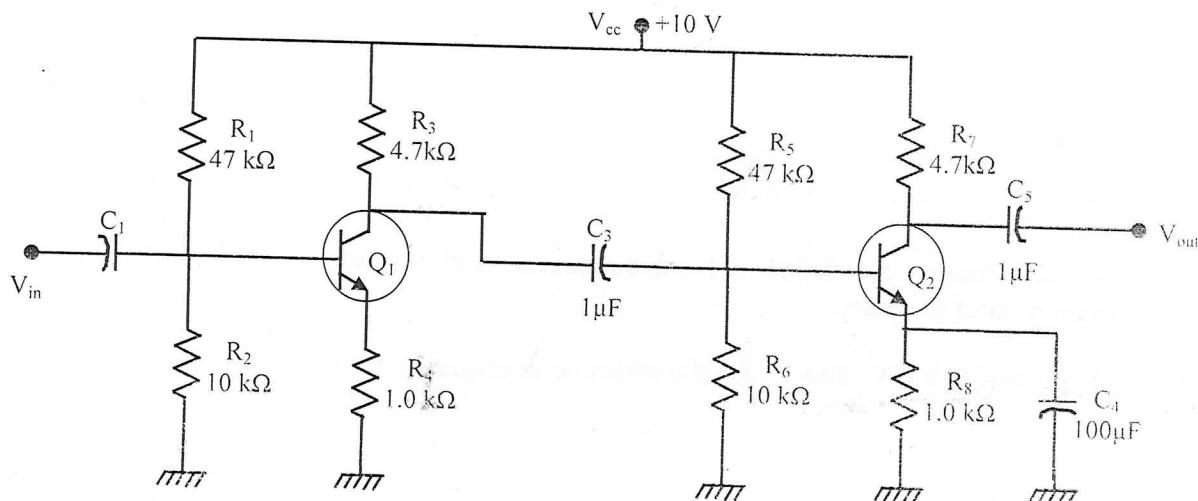


Fig. 6(c)

- Q.7(a) Explain how the ac power output can be greater than the input ac power in transistor. 05
 (b) Draw the re equivalent circuit of Fig. 7(b) and determine i) r_e ii) Z_i iii) Z_o iv) A_v 25
 (c) Write the advantages of hybrid equivalent circuit over re model. 05
- Q.8(a) Why MOSFET is called voltage controlled device? 05
 (b) For FET, compare between pinch-off voltage and cutoff voltage. 10
 (c) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig. 8(c), given that for this particular JFET the parameter values are such that $V_D=7V$. 15
 (d) Write down the comparison between CMOS and Bipolar technology. 05

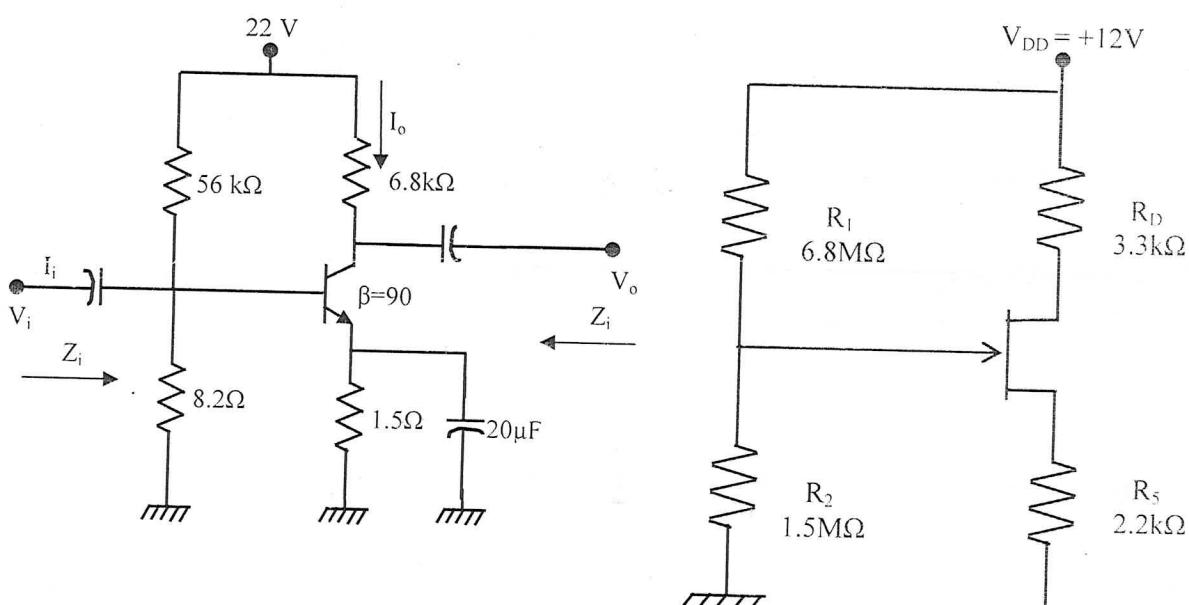


Fig. 7(b)

Fig. 8(c)

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CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM SELF STUDY EXAMINATION '2020

DEPARTMENT	: ELECTRONICS AND TELECOMMUNICATION ENGINEERING
FULL TITLE OF PAPER	: Electronics-I
COURSE NO.	: ETE-101
FULL MARKS	: 210
TIME	: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- | | |
|---|----|
| Q.1(a) Define semiconductor. Mention how the conductivity of a semiconductor is varied? | 10 |
| (b) "A semiconductor is an insulator at ordinary temperature" -Explain. | 10 |
| (c) Explain diffusion and drift current. | 05 |
| (d) What is meant by the a.c. and d.c. resistance of a p-n junction? | 10 |
| Q.2(a) Describe the process of avalanche breakdown in a PN diode. | 10 |
| (b) Describe a complete model of a diode with consisting parameters. | 15 |
| (c) Determine the output of fig 2(c). | 10 |

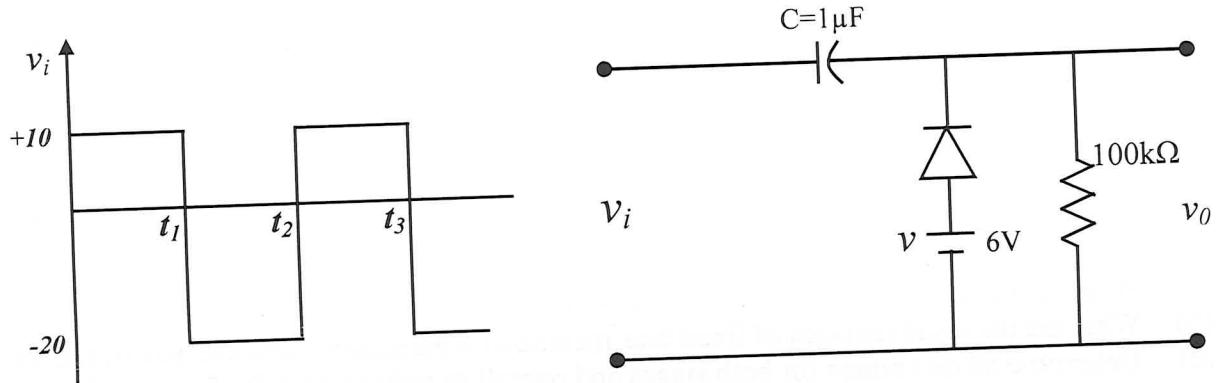


Fig.2(c)

- | | |
|---|----|
| Q.3(a) What is ripple factor? Explain how ripple is reduced by using a capacitor filter. | 08 |
| (b) What is voltage regulation? How does a Zener diode can act as a voltage regulator? | 12 |
| (c) With neat sketch explain the operation of a full-wave bridge rectifier. | 15 |
| Q.4(a) What is transistor biasing? Mention the condition for faithful amplification. | 11 |
| (b) Explain the effect of I_B and V_{CC} on the load line and Q-point with appropriate figure. | 11 |
| (c) For the voltage divider bias configuration of Fig.4(c) determine:
(i) I_{BQ} (ii) I_{CQ} (iii) V_{EC} (iv) V_C (v) V_E (iii) V_B | 13 |

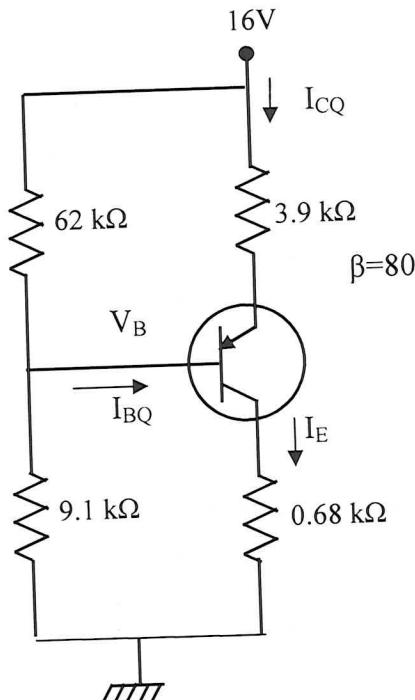


Fig.4(c)

Section-B

- Q.5(a) Determine how much Q point (I_C , V_{CE}) for the circuit in Fig.5(a) will change β_{DC} increase from 17 to 200 when one transistor replaced by another.
- (b) Determine the total input resistance of the emitter-follower in Fig.5(b). Also find the voltage gain, current gain and power gain in terms of power delivered to the load R_L . Assume $\beta_{DC} = 175$ and the capacitive reactance is negligible at the frequency of operation.

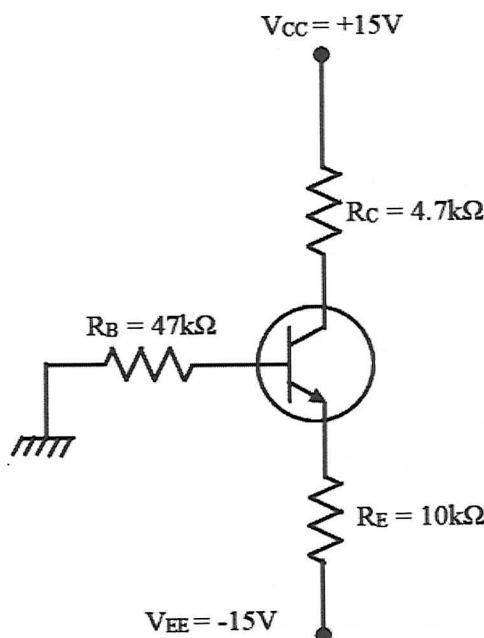


Fig.5(a)

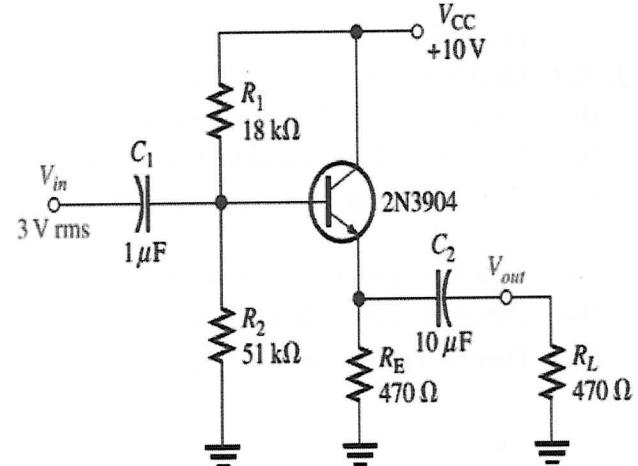


Fig.5(b)

- Q.6(a) What is emitter follower? Why is it called so? 06
 (b) What are the disadvantages of fixed bias method of a transistor? How can you minimize it? 10
 (c) Determine all dc voltage for both stages and overall ac voltage gain for fig 6(c) where $\beta_{DC} = \beta_{AC} = 150$ for Q_1 and Q_2 . 19

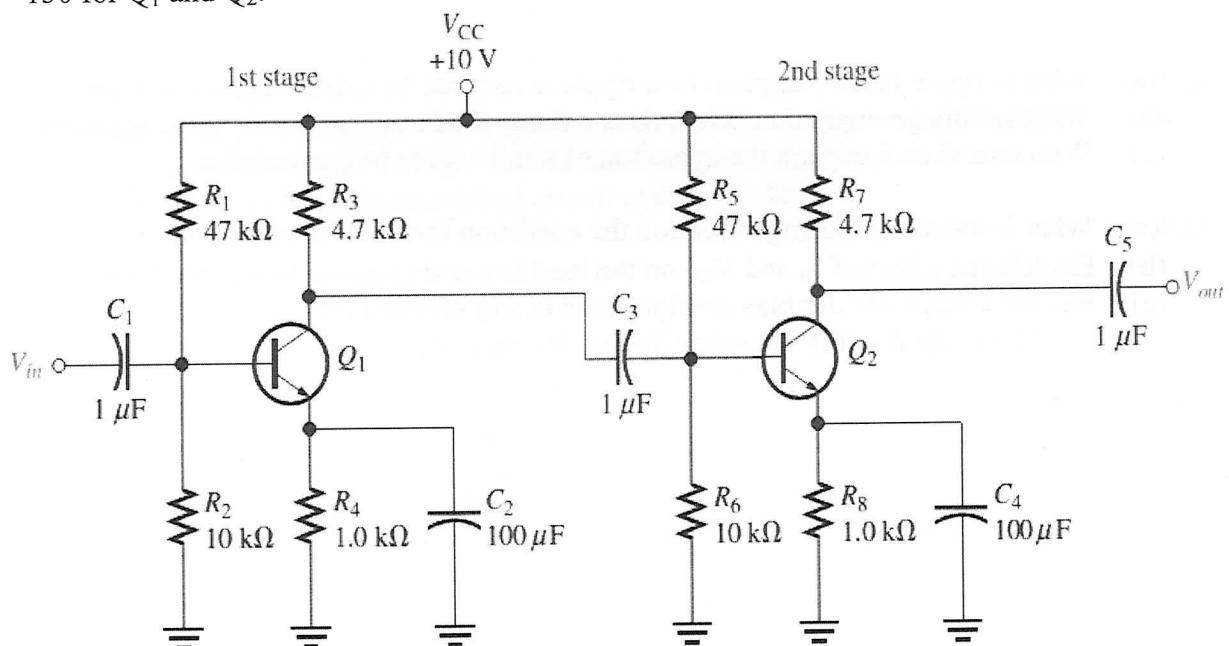


Fig.6(c)

- Q.7(a) Explain how channel is formed in MOSFET. 10
 (b) Compare the frequency response of capacitive coupled and direct couple multistage amplifier. 12
 (c) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig.7(c), given that for this particular JFET the parameter values are such that $V_D = 7V$. 13

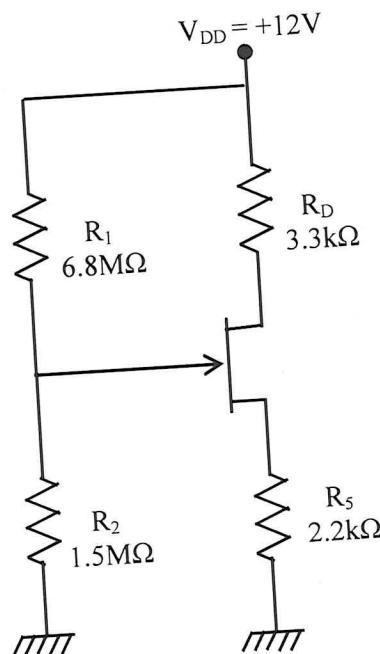


Fig.7(c)

- Q.8(a) "The MOSFET works as a digital switch"- Explain briefly
 (b) Write down the difference between BJT and FET.
 (c) Draw and Explain the basic construction of CMOS.
 (d) Write short note on E-MOSFET and D-MOSFET.

The End

07
08
08
12

CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM-II FINAL EXAMINATION '2019

DEPARTMENT
FULL TITLE OF PAPER
COURSE NO.
FULL MARKS
TIME

: ELECTRONICS AND TELECOMMUNICATION ENGINEERING
: Electronics-I
: ETE 101
: 210
: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) Define semiconductor, resistivity, bulk resistance and ohmic contact. 08
- (b) Write down the basic difference between electrical and electronics. Explain the process of hole conduction. 07
- (c) Describe in your own words the condition established by forward and reverse biased conditions on a p-n junction diode and how the resulting current is affected. 12
- (d) "Semiconductor have negative temperature coefficient of resistance" Explain briefly. 08
- Q.2(a) Describe the ideal diode model, practical diode model and complete diode model. 10
- (b) Describe the effects of temperature on diode characteristics. 10
- (c) Determine the currents I_1 , I_2 and I_{D2} for Fig.2(c) 10

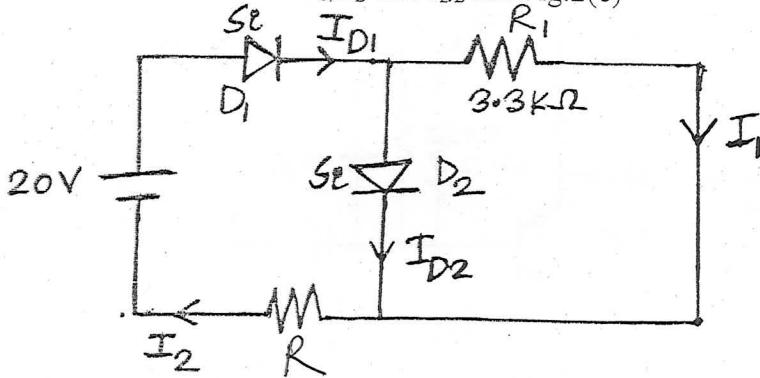


Fig.2(c)

- (d) Compare the depletion regions in forward bias and reverse bias. 05

- Q.3(a) Describe how a bridge full-wave rectifier work. 10

- (b) Determine the output waveform for the sinusoidal input of Fig.3 (b). 10

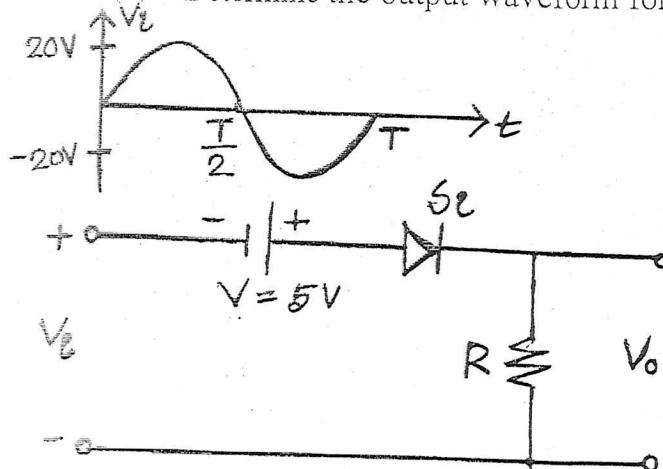


Fig.3 (b)

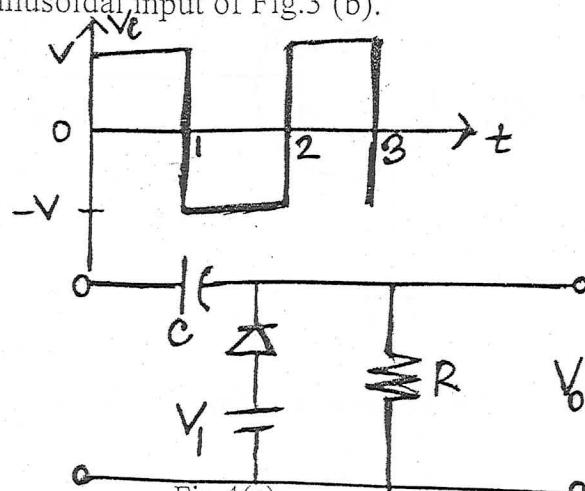


Fig.4(a)

- (c) Explain Zener diode as a voltage stabilizer. 10
- (d) How diode limiters and diode clamps differ in terms of their function? 05

- Q.4(a) Determine the output voltage of Fig.4(a) 10

(b) In what region of their characteristics curve are zener diodes operated? Explain with figure. 10

(c) Why biasing is necessary for a transistor operation? Explain with neat sketch linear, cutoff and saturation region of a transistor operation. 15

Section-B

Q.5(a) Describe the basic structure and operation of the BJT. 15

(b) Write down short notes on : 09
 (i) Coupling Capacitor
 (ii) Bypass capacitor
 (iii) Blocking capacitor

(c) Interpret the transistor collector characteristics curve. 11

Q.6(a) Sketch the characteristics of an n-channel depletion type MOSFET with $I_{DSS}=10\text{mA}$ and $V_p=-4\text{V}$ 10

(b) Determine the dc level of I_B and I_C for the network of Fig. 6(b). 17

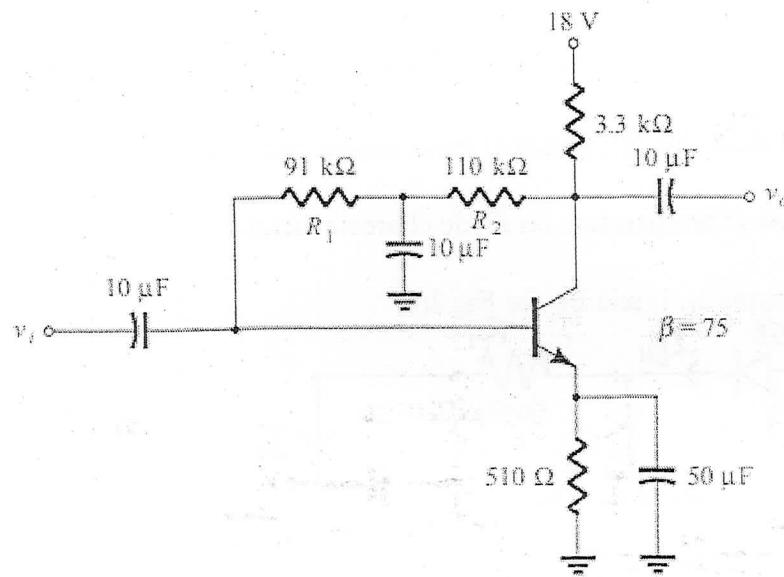
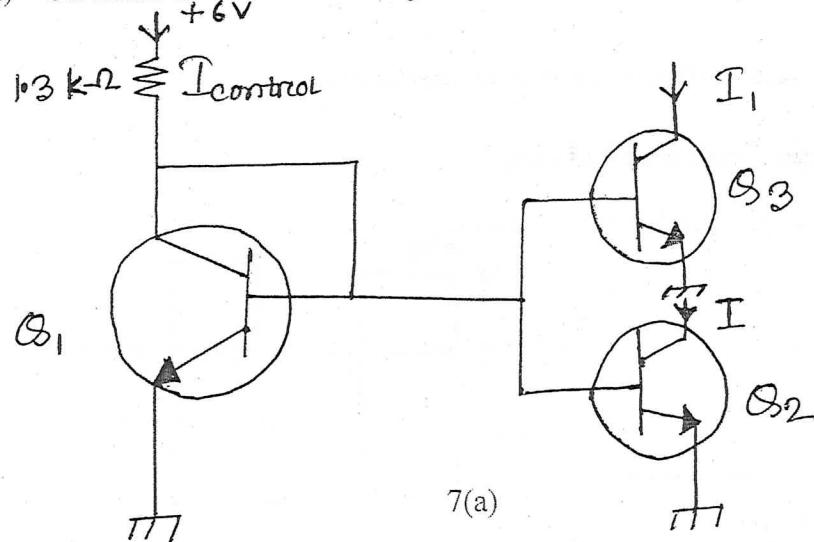


Fig.6 (b).

(c) Define Q-point and describe how it affects the output of an amplifier. 08

Q.7 (a) Calculate the current I through each of the transistor Q_2 and Q_3 in the circuit of Fig.7(a) 13



(b) For the network of Fig.7(b), determine 12

- (i) R_e
- (ii) Z_i
- (iii) Z_0
- (iv) A_v

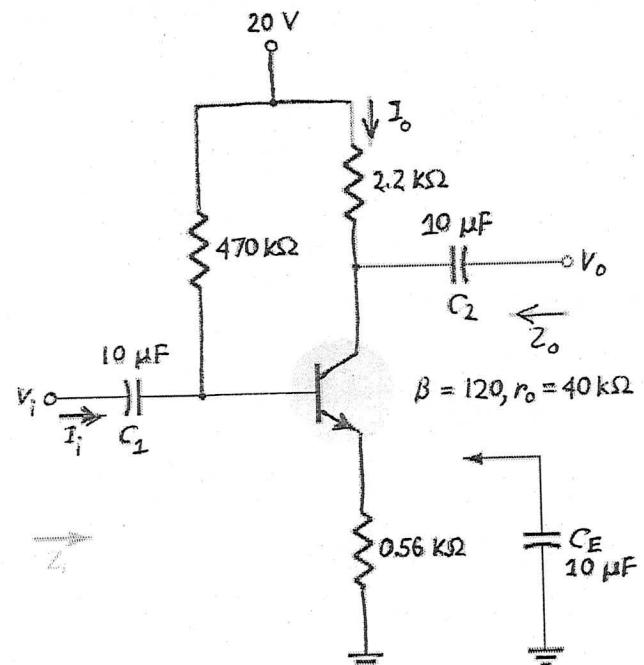


Fig.7 (b).

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- (c) For the network of Fig.7(c) ,find

- (i) Z_i
- (ii) Z_o
- (iii) A_v
- (iv) A_i

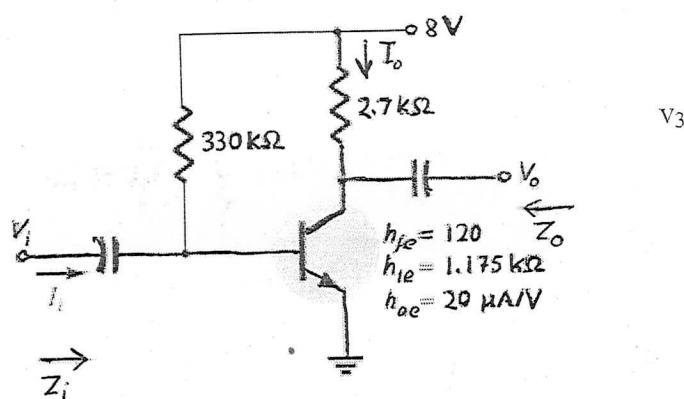


Fig.7(c)

07

- Q.8(a) Explain how gate to source voltage of JFET controls the drain current.

15

- (b) Explain the operating principle of CMOS inverter.

05

- (c) Compare between pinch off voltage and cutoff voltage.

08

- (d) Explain the operation of MOSFETs.

The End

CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM-II (17 BATCH) EXAMINATION '2018

DEPARTMENT
 FULL TITLE OF PAPER
 COURSE NO.
 FULL MARKS
 TIME

: ELECTRONICS AND TELECOMMUNICATION ENGINEERING
 : Electronics-I
 : ETE101
 : 210
 : 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

Q.1(a) Why are free electrons most important for electronics? 10

(b) "Semiconductors have negative temperature coefficient of resistance"-Explain briefly. 10

(c) Explain with the aid of clear sketch showing all current directions, the behavior of a P-N junction diode under forward bias and reverse bias condition. 15

Q.2(a) Can you make a distinction between the breakdown voltage and barrier potential? 10

(b) Find V_0 and I_D in the network at Fig. 2(b). The diodes are silicon diode. 10

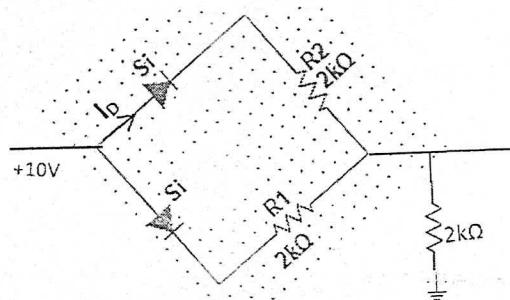


Fig. 2(b).

(c) Determine the output waveform for the network of Fig. 2(c) and calculate the output dc level and the required PIV of each diode. 10

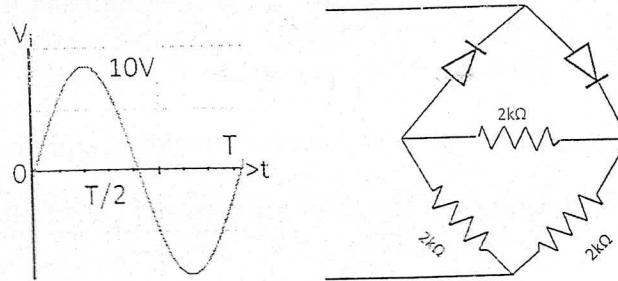


Fig. 2(c).

(d) How does a full-wave voltage differ from a half wave voltage? 05

Q.3(a) Discuss the importance of peak inverse voltage in rectifier service. 10

(b) Determine V_0 for the network of Fig. 3(b). 10

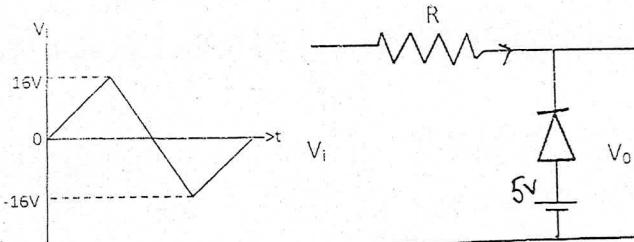


Fig. 3(b).

(c) How can you use Zener diode as a voltage stabilizer? Explain with proper figure. 15

Q.4(a) Why do you think in the saturation region the base-emitter and collector-base junctions are forward-biased? 10

- (b) For the emitter-bias network of Fig 4(b), determine (a) I_B , (b) I_C , (c) V_{CE} , (d) V_C , (e) V_B , (f) V_{BC} .

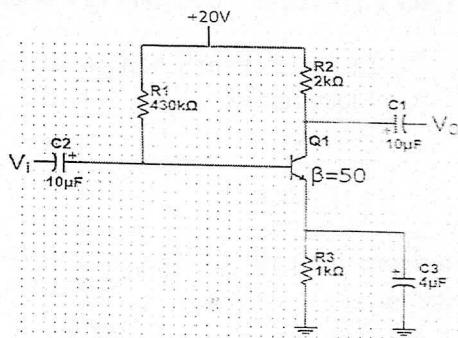


Fig 4(b).

- (c) "Transistor can be used as a switch" – Justify.
 (d) What is emitter follower? Why it is called so?

05

05

Section-B

- Q.5(a) What is the main idea of coupling capacitor.
 (b) Calculate the current I through each of the transistor Q_2 and Q_3 in the circuit of Fig. 5(b).

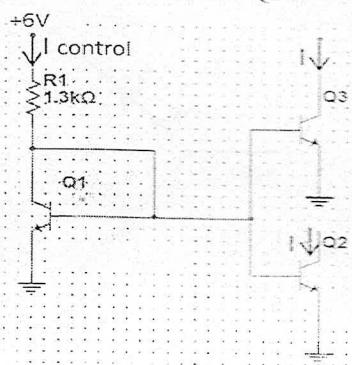


Fig. 5(b).

- (c) For a $0.8\mu\text{m}$ process technology for which $t_{ox}=15\text{nm}$ and $\mu_0=550\text{cm}^2/\text{v-s}$, find c_{ox} , k_n' and the overdrive voltage $V_{or}=V_{GS}-V_t$ required to operate a transistor having $W/L=20$ in saturation with $I_D=0.2\text{mA}$. What is the minimum value of V_{DS} needed?

- Q.6(a) What are the difference between r_e mode and hybrid equivalent circuit?

- (b) Draw the hybrid equivalent circuit of Fig 6(b) and determine Z_i , Z_o , A_v , A_i .

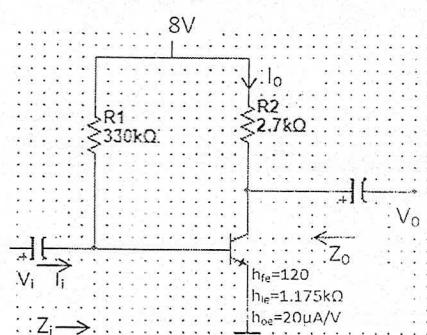


Fig 6(b).

- (c) Determine the following for the network of the Fig. 6(c). V_{GSQ} , I_D , V_{DS} , V_S , V_G and V_D .

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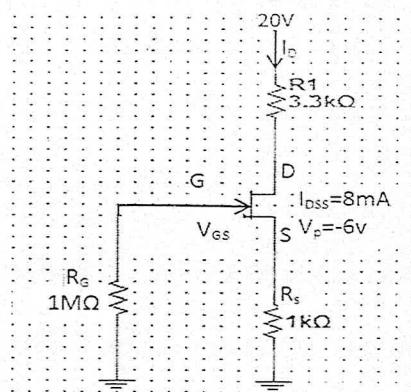


Fig. 6(c).

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15

Q.7(a) Explain how channel is created in depletion type MOSFET.

(b) Write the operating principle of n-channel JFET.

(c) Sketch the transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS}=10\text{mA}$ and $V_p=-4\text{V}$.

Q.8(a) Why a MOSFET is called voltage controlled device? Give a comparison between BJT and MOSFET.

(b) For n-channel type MOSFET of Fig. 8(b), determine I_{DQ} and V_{DS} .

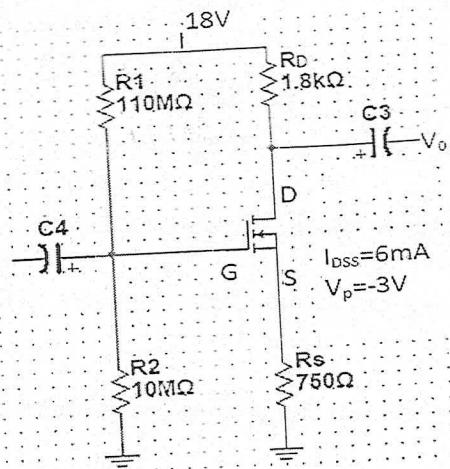


Fig. 8(b).

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(c) How would you summarize BJT, FET and MOSFET.

The End

CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM-II EXAMINATION '2018

DEPARTMENT : ELECTRONICS AND TELECOMMUNICATION ENGINEERING
 FULL TITLE OF PAPER : Electronics-I
 COURSE NO. : ETE 101
 FULL MARKS : 210
 TIME : 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) Classify material in terms of energy band gap. Why conductivity increases in semiconductors with the rise of temperature? 12
- (b) Define dopant, intrinsic and extrinsic material. How p-type and n-type material is formed? 14
- (c) Explain in your own words why study of semiconductor is important for communication engineers. 09
- Q.2(a) With neat sketch and with the help of carrier flow, explain the p-n junction behavior for
 i) Zero bias
 ii) Forward bias
 iii) Reverse bias 18
- (b) Determine current through each diode of Fig.2(b). Assume the diodes are Silicon diode. 08

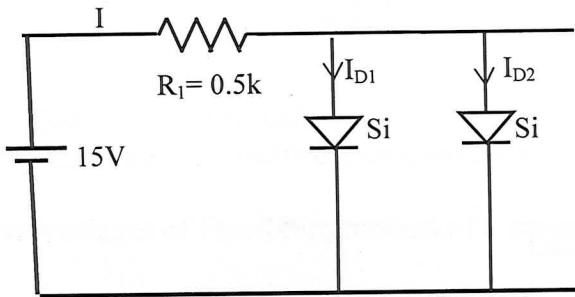


Fig. 2(b)

- (c) With neat diagram, explain the operation of full-wave bridge rectifier. 09
- Q.3(a) What do you mean by ripple factor? How it can be minimized in full-wave rectified output? 10
- (b) Draw the output voltage waveform for following circuit of Fig.3 (b). Consider the diodes are ideal. 10

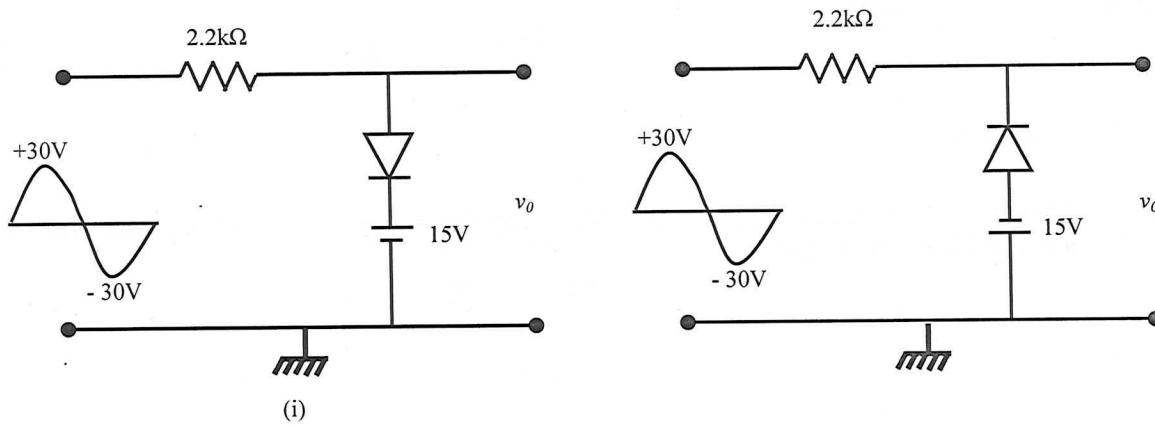


Fig. 3(b)

- (c) Determine I_B , I_C , I_E , V_{BE} , V_{CE} , and V_{CB} for the circuit of Fig.3 (c). The transistor $\beta_{DC}=150$. 15

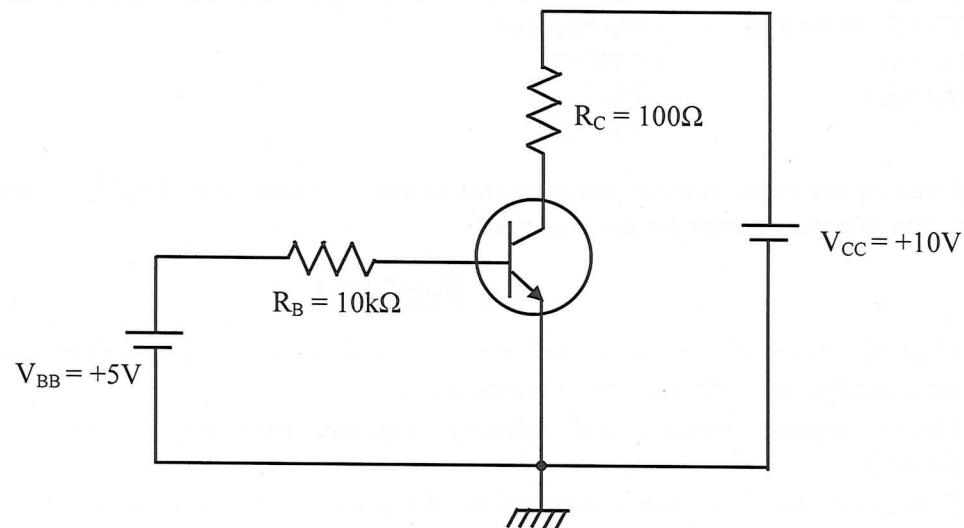


Fig.3(c)

- Q.4(a) Define α and β . Develop a relation between them. 07

- (b) Determine V_{CE} and I_C in the voltage divider biased transistor circuit of Fig.4 (b). Here $\beta_{DC} = 100$. 13

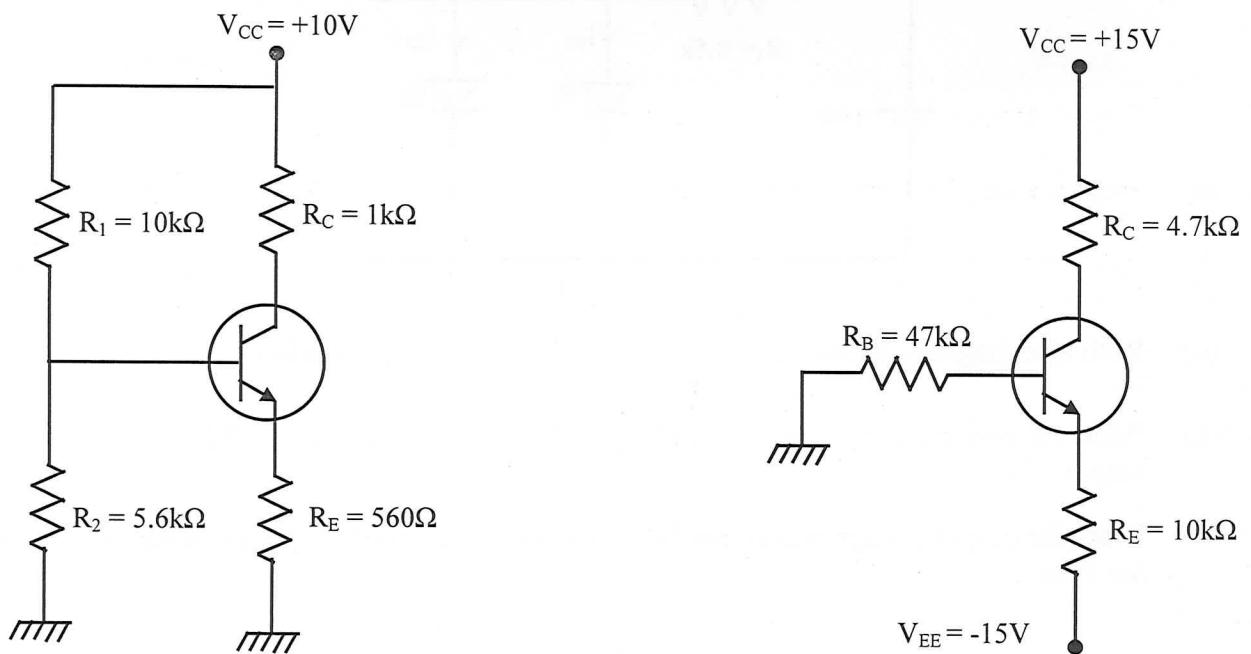


Fig. 4(b)

Fig. 4(c)

- (c) Determine how much Q point (I_C , V_{CE}) for the circuit of Fig.4(c) will change if β_{DC} increases from 100 to 200. 15

Section-B

24

- Q.5(a) For the amplifier of Fig. 5(a)
- Determine dc collector voltage
 - Determine ac collector voltage
- Here $\beta_{DC} = 150$ and $\beta_{ac} = 175$

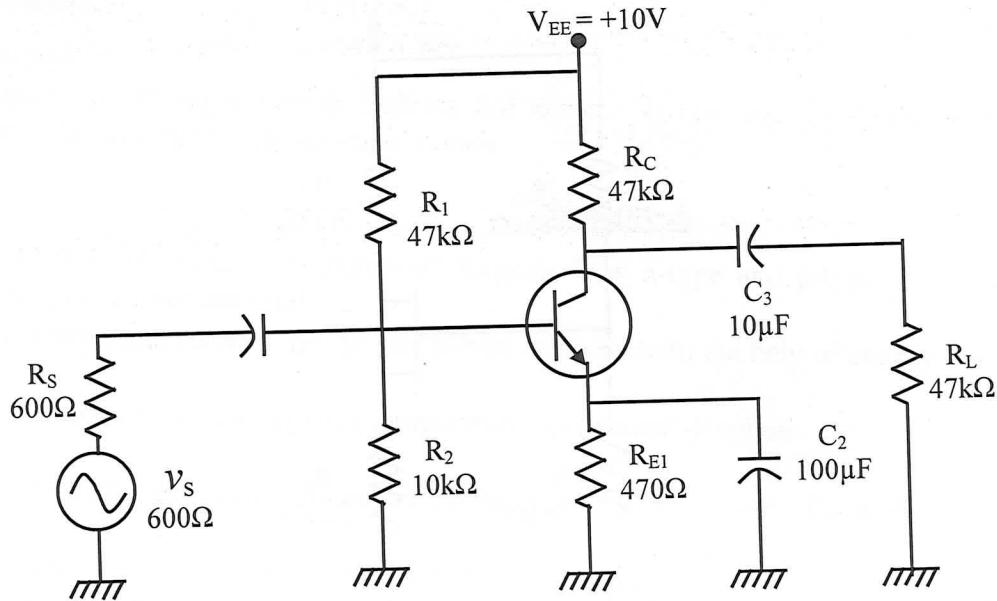


Fig. 5(a)

- | | |
|--|----|
| (b) What is emitter follower? Why is it called so? | 06 |
| (c) Explain frequency response of capacitively coupled amplifier. | 05 |
| Q.6(a) What are the disadvantages of Fixed-bias method of a transistor? How can you minimize it? | 10 |
| (b) Find the input resistance, voltage gain, current gain and power gain for the amplifier in fig 6(b), $\beta_{DC} = 250$ | 16 |

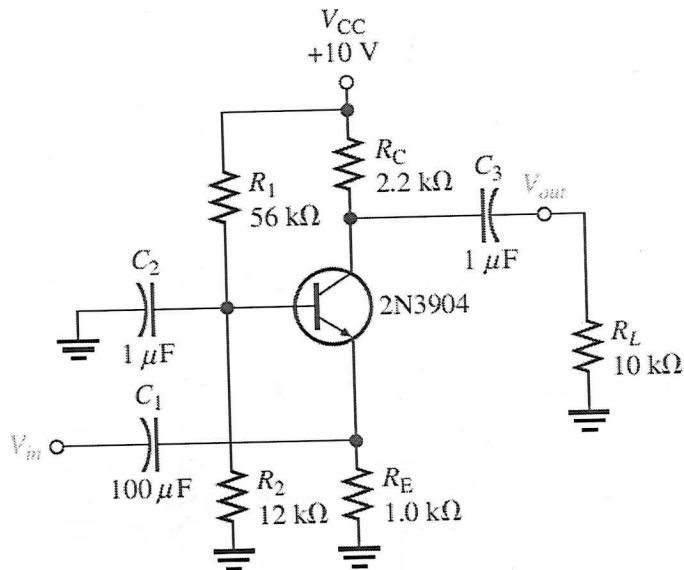


Fig. 6(b)

- | | |
|---|----|
| (c) "Transistor can be used as a switch"- Justify. | 09 |
| Q.7 (a) With neat sketch explain the construction and operation of FET. | 15 |
| (b) Explain how channel is formed in MOSFET. | 10 |

- (c) Explain the construction of Enhancement and depletion type MOSFET. Compare them. 10
- Q.8(a) Write a short note on NMOS, VMOS and CMOS 18
- (b) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig.8(b), given that for this particular JFET the parameter values are such that $V_D = 7V$. 17

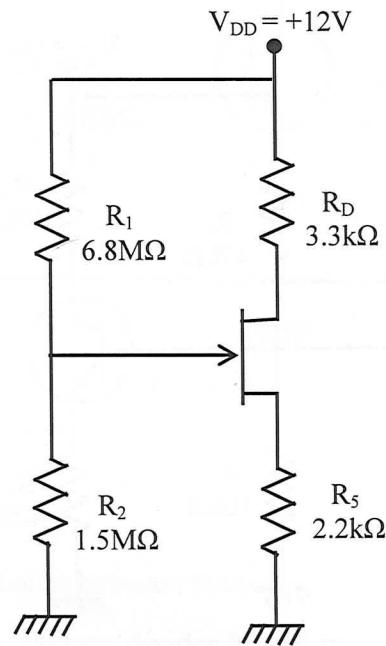


Fig.8 (b)

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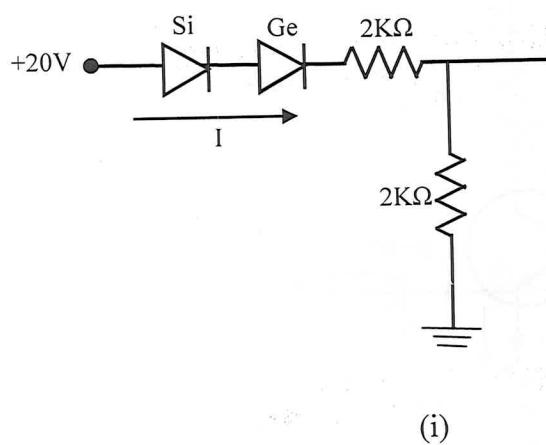
CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY
B.Sc. ENGINEERING LEVEL-I TERM-II EXAMINATION '2016

DEPARTMENT : ELECTRONICS AND TELECOMMUNICATION ENGINEERING
 FULL TITLE OF PAPER : Electronics-I
 COURSE NO. : ETE101
 FULL MARKS : 210
 TIME : 3 HOURS

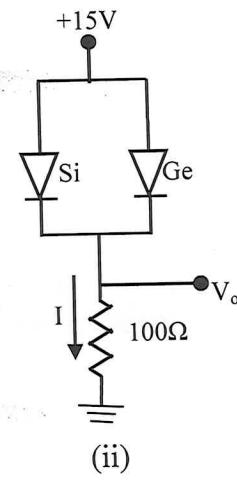
The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) What is semiconductor material? Explain how n-type and p-type material are formed in a semiconductor material. 10
- (b) Differentiate between n-type and p-type material with the help of energy band diagram. 10
- (c) "Semiconductor has negative temperature coefficient"-Explain. 08
- (d) Explain the effect of temperature on the characteristics curve of a diode. 07
- Q.2(a) What is depletion region? What is the effect of reverse bias on depletion layer? Explain with neat diagram. 10
- (b) Determine V_o and I for the circuit in Fig. 2(b) 12



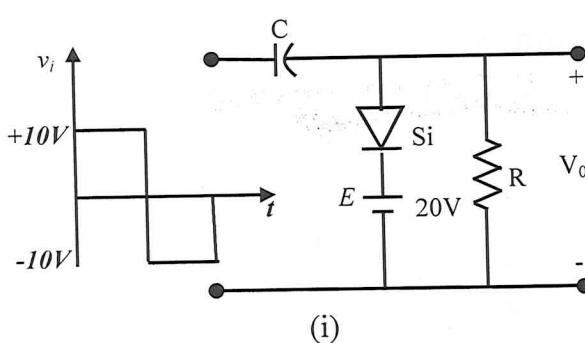
(i)



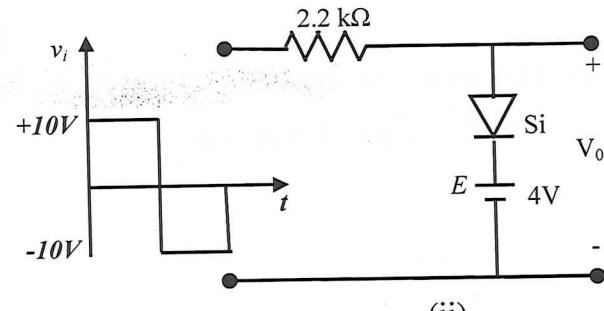
(ii)

Fig. 2(b)

- (c) Sketch V_o for each network of Fig. 2 (c) for the given input. 13



(i)



(ii)

Fig. 2(c)

- Q.3(a) For a zener diode network of Fig. 3(a) determine V_L , V_R , I_Z and P_Z . 12

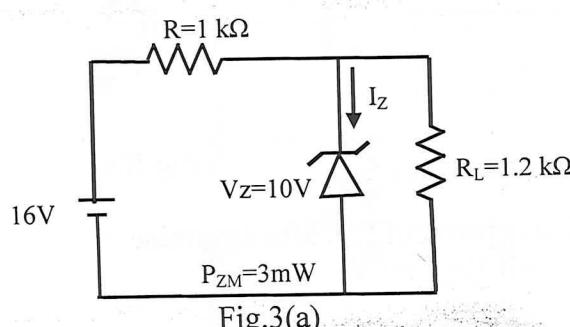


Fig. 3(a)

- (b) Determine I_B , I_C , I_E , V_{BE} , V_{CE} , and V_{CB} in the circuit of Fig. 3(b). The transistor has $\beta_{DC}=150$. 12

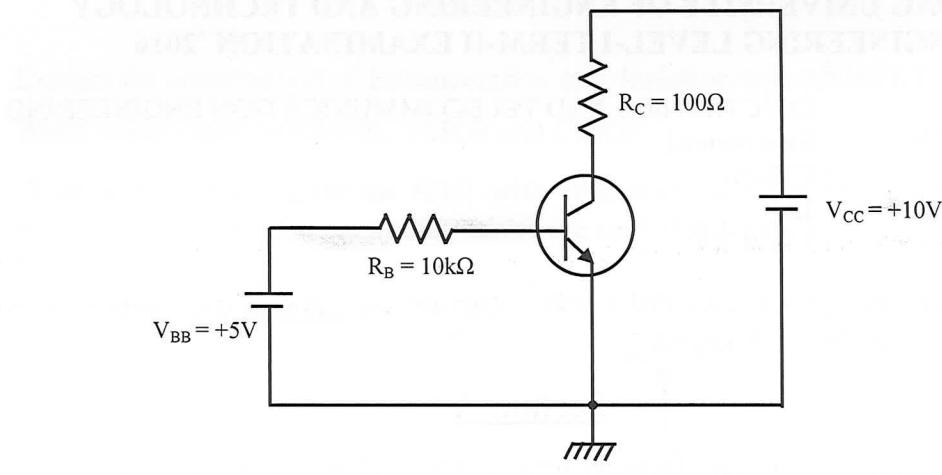


Fig.3(b)

- (c) What is transistor biasing? Mention the condition for faithful amplification. 11
- Q.4(a) Explain the effect of I_B and V_{CC} on the load line and Q-point with appropriate figure. 12
- (b) Explain how transistor act as an amplifier. 10
- (c) For the voltage divider bias configuration of Fig. 4(c), determine:- 13
- I_{BQ}
 - I_{CQ}
 - V_{CEQ}
 - V_C
 - V_E
 - V_B

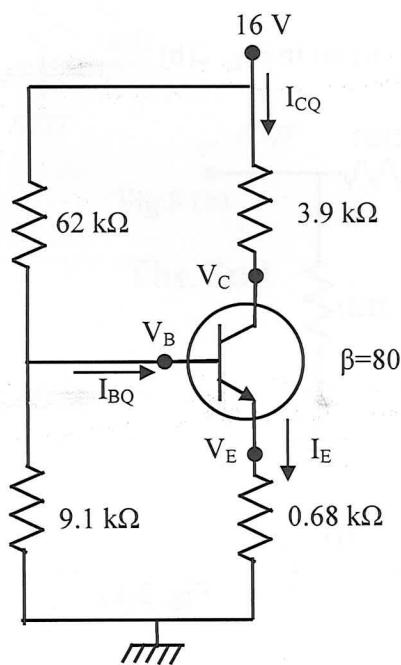


Fig. 4(a)

Section-B

- Q.5(a) Determine the resistance R_B and R_C for the following circuit in Fig. 5(a) so that it can work as a switch. $I_{esat} = 10 \text{ mA}$ 12

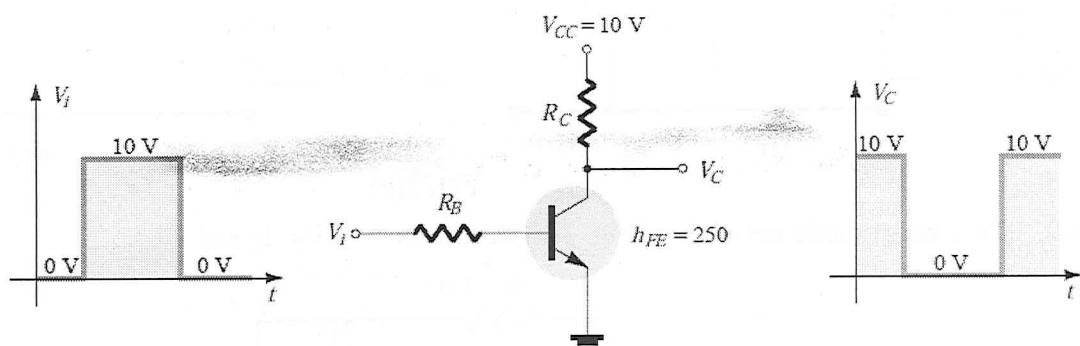


Fig.5(a)

- (b) For the following network of Fig. 5(b) determine 13
- I_B
 - I_C
 - V_{CE}
 - V_C

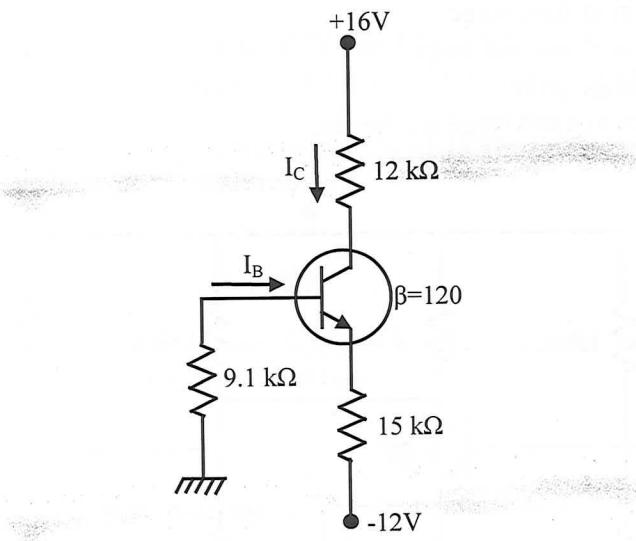


Fig.5(b)

- (c) Explain the effect of the resistor ratio R_B/R_E on the stability factor $S(I_{CO})$ for the emitter-bias configuration. 10
- Q.6(a) Write the important characteristics of a emitter-follower circuit. 05
- (b) Draw the r_e equivalent circuit for the following collector dc-feedback network shown in Fig 6(b) and determine i) r_e ii) Z_i iii) Z_o iv) A_v . 10

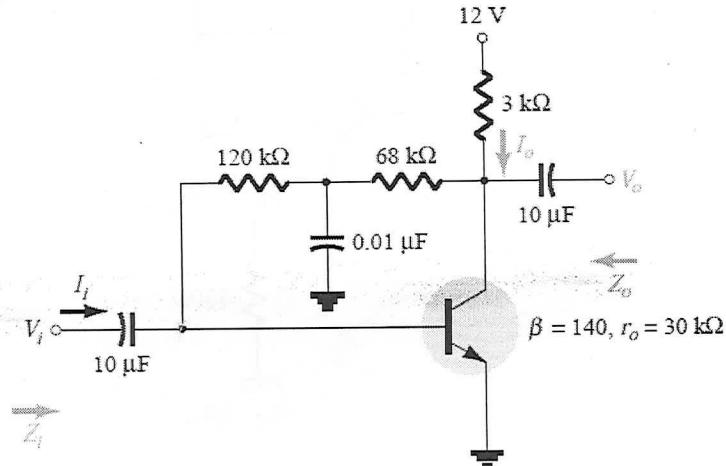


Fig. 6(b)

- (c) For the following voltage divider circuit in Fig. 6(c), determine 13
- r_e
 - Calculate Z_i and Z_o
 - Find A_v
 - Repeat parts (i) and (ii) with $r_o=25\text{k}\Omega$.

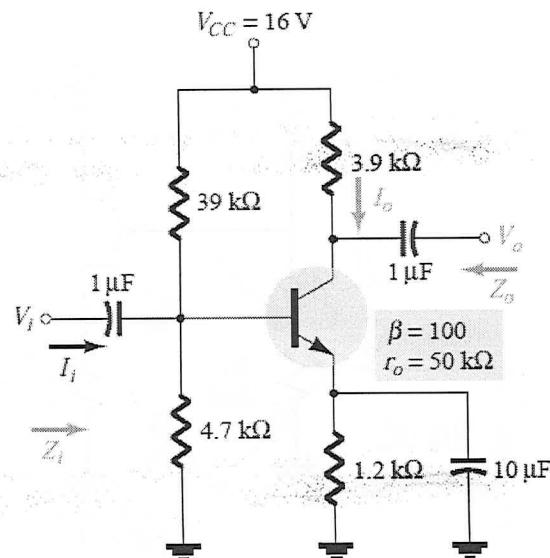


Fig.6(c)

- (d) What is the necessity of bypass capacitor in BJT ac analysis? Explain. 07

Q.7(a) For the capacitively coupled multistage amplifier shown in Fig. 7(a), Find

- Voltage gain at first stage
- Voltage gain at second stage
- Overall voltage gain
- DC voltages at each stage of the ckt.

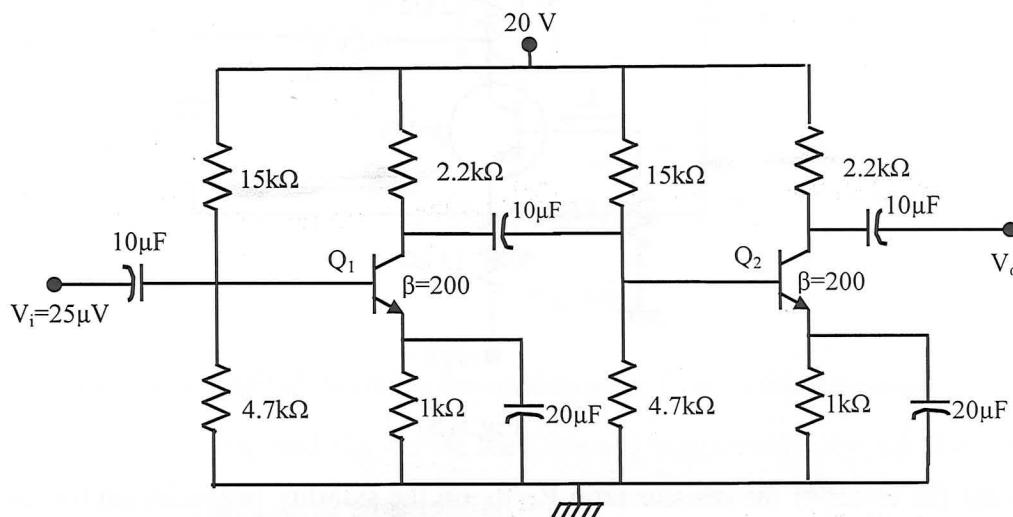


Fig. 7 (a)

(b) Calculate the dc bias voltages and current in the circuit of Fig. 7(b).

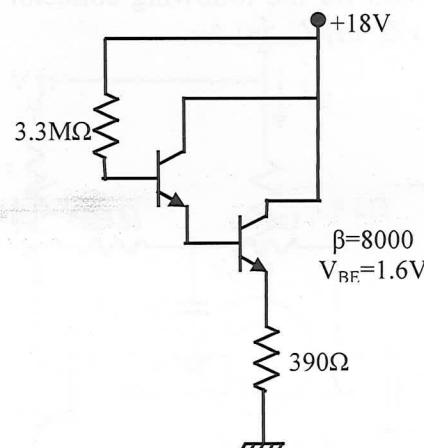


Fig. 7(b)

(c) Why MOSFET is called voltage controlled device? Give a comparison between BJT and 10 MOSFET.

Q.8(a) Explain the operation of a depletion type MOSFET with proper diagram and explain the effect 14 of biasing voltage on it.

(b) Determine I_D and V_{GS} for the JFET with voltage divider bias in Fig. 8(b), given that $V_D = 7V$.

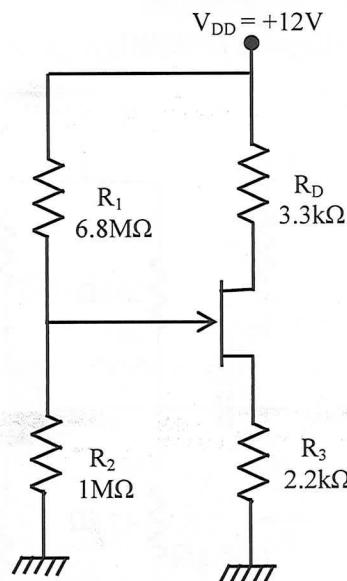


Fig. 8 (b)

(c) Draw and explain the basic construction of CMOS.

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B.Sc. ENGINEERING LEVEL-I TERM-II EXAMINATION '2015

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FULL TITLE OF PAPER	: Electronics-I
COURSE NO.	: ETE101
FULL MARKS	: 210
TIME	: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) Define electron-hole pair. Explain the illustration of the PN junction for the following conditions using the energy diagram: 15
- i) At the instant of junction formation
 - ii) At equilibrium
- (b) State how valence electrons determine the electrical properties of a material. 10
- (c) Differentiate between drift current and diffusion current. 10
- Q.2(a) What do you understand by ac and dc resistance of a pn junction diode? How will you determine them from the V-I characteristic curve? 13
- (b) What is depletion region? How is it formed in P-N junction. 10
- (c) Find V_0 and I_D in the network of Fig. 2(c). The diodes are Silicon diode. 12

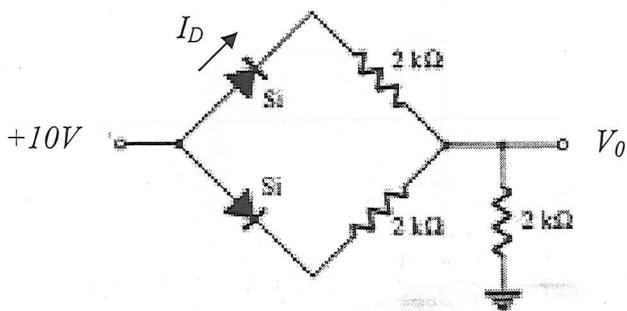


Fig. 2 (c)

- Q.3(a) Why is the output frequency doubled of input frequency in case of full wave rectifier? 08
- (b) What is Ripple factor? Explain how ripple is reduced by using a capacitor filter. 12
- (c) What is voltage regulation? How does a Zener diode can act as a voltage regulator? 07
- (d) For the circuit shown in Fig 3(d), find the output dc voltage 08

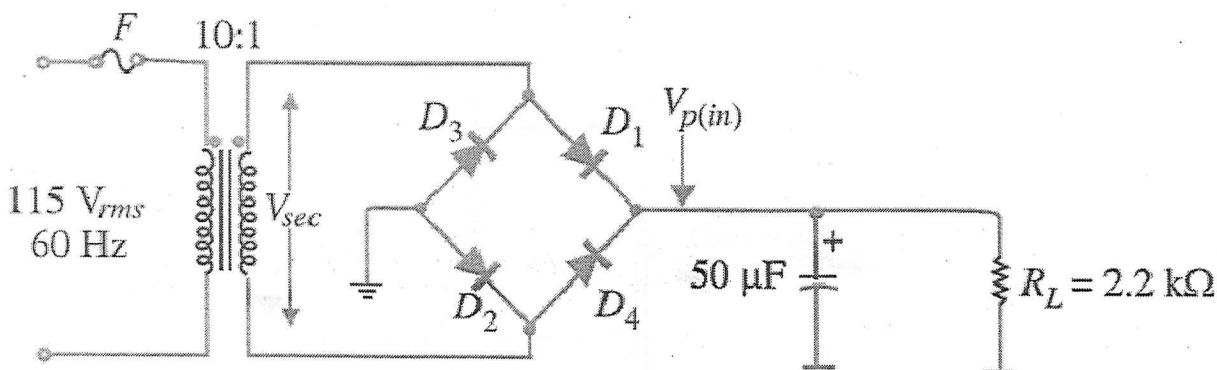


Fig 3 (d)

- Q.4(a) Draw and explain the I-V characteristics of a bipolar transistor. 10

- (b) State the underlying principle of transistor amplifying action. Explain the phenomenon of "Early effect". 10
- (c) The circuit shown in Fig.4(c) provides some information. Find out the value of R_C ; R_E ; R_B ; V_{CE} and V_B . 15

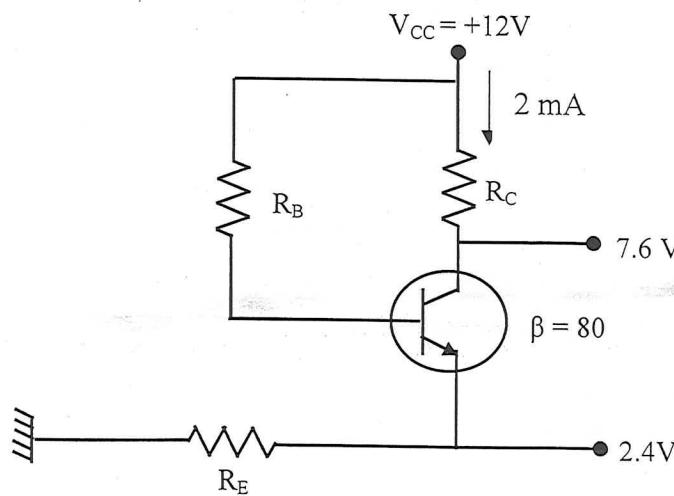


Fig.4 (c)

Section-B

- Q.5(a) Mention the advantages and disadvantages of capacitively coupled amplifier. 07
- (b) What do you mean by "loading effect" in a cascaded amplifier stage? 10
- (c) Fig.5(c) shows a direct-coupled two stage amplifier. Determine 18
- DC voltages for both stages.
 - Voltage gain of each stage.

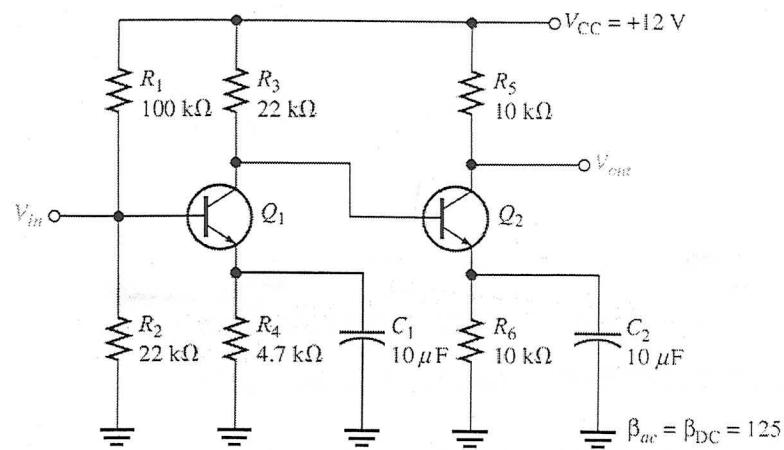


Fig.5 (b)

- Q.6(a) Determine I_C and V_{EC} for the pnp transistor of Fig 6(a). Where $\beta_{DC}=150$. 18

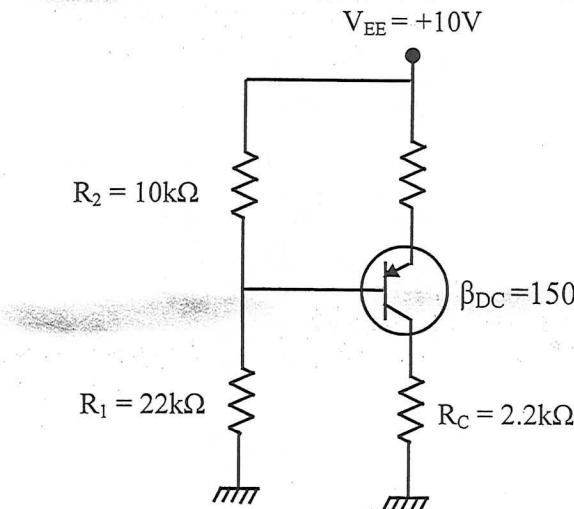


Fig 6 (a)

- (b) Determine how much Q point (I_C , V_{CE}) for the circuit of Fig. 6(b) will be changed if β_{DC} increases from 100 to 200. 17

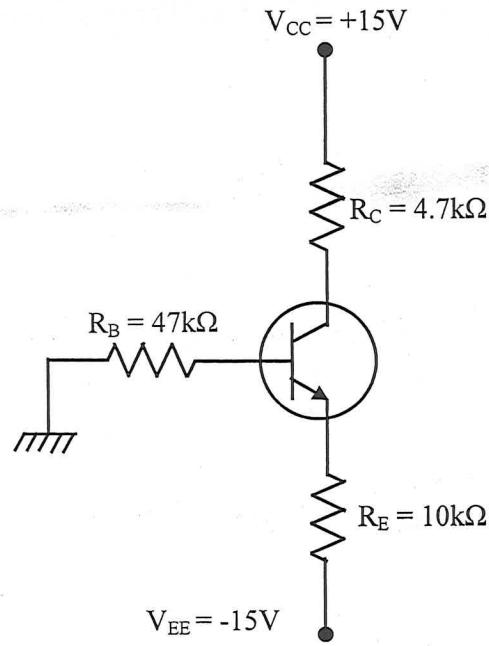


Fig. 6 (b)

- (c) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig. 6(c), given that for this particular JFET the parameter values are such that $V_D = 7V$. 13

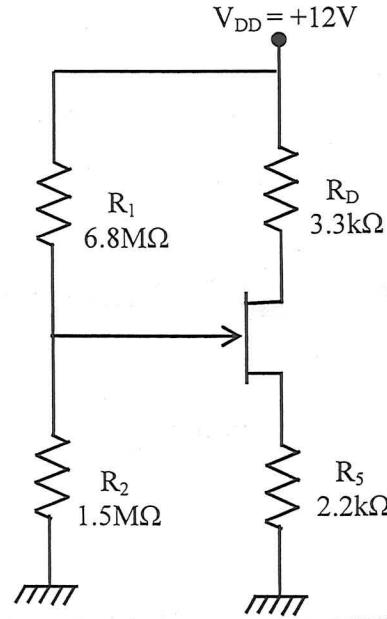


Fig. 6 (c)

- Q.7 (a) How channel is created in the enhancement type MOSFET? Explain in brief. 12
 (b) Calculate I_D and V_{DS} if $K_n=100 \mu\text{A}/\text{V}^2$, $V_{th}=0.6\text{V}$ and $W/L = 3$ for transistor M_1 in Fig. 6(b). 15

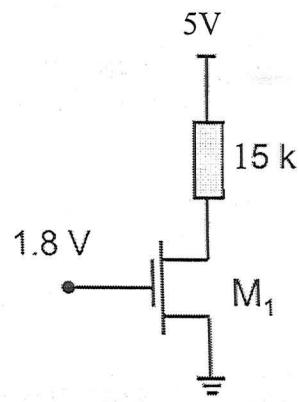


Fig. 6 (b)

- (c) Write down the difference between BJT and FET. 08
- Q.8(a) What is Emitter-follower? Why it is called so? 07
- (b) "The MOSFET works as a digital switch"- justify. 08
- (c) Determine I_D and V_{GS} for the JFET of Fig.8(c). For this particular JFET, the parameter values are such that $V_D=7V$. 10

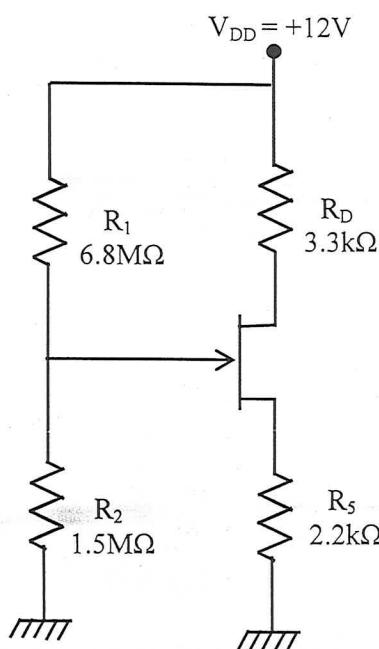


Fig 8 (c)

- (d) Write a short note on E-MOSFET and D-MOSFET. 10

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FULL TITLE OF PAPER	: Electronics-I
COURSE NO.	: ETE101
FULL MARKS	: 210
TIME	: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) With the help of energy band diagram explain the difference between conductors, semiconductors and insulators. 08
- (b) What is space charge region? Why it is so called? Briefly explain its formation phenomena. 10
- (c) Define doping. Explain how n-type and p-type semiconductors are formed. 10
- (d) What is the difference between intrinsic and extrinsic semiconductor. 07
- Q.2(a) With neat sketch clearly explain the behavior of a p-n junction diode under forward biased and reverse biased condition. 15
- (b) Determine I , V_1 , V_2 , and V_0 for the series dc configuration of Fig.2(b) 10

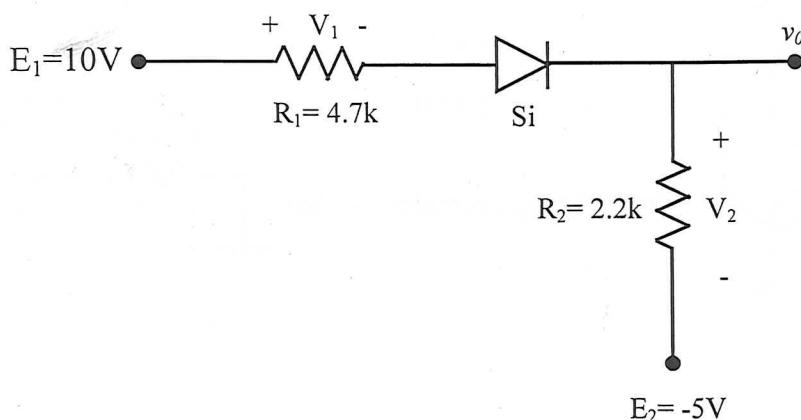


Fig. 2(b)

- (c) What is the ripple factor? Calculate its value for a half wave and full wave rectifier. 10
- Q.3(a) Consider the circuit in Fig 3(a) 18

- What type of circuit is this?
- What is the total peak secondary voltage?
- Find the peak voltage across each half of the secondary
- Sketch the voltage waveform across R_L .
- What is the peak current of each diode?
- What is the PIV of each diode?

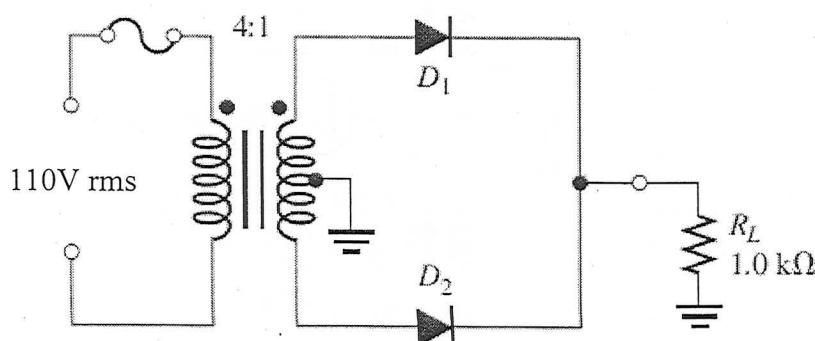


Fig.3(a)

- (b) Determine I_B , I_C , I_E , V_{BE} , V_{CE} , and V_{CB} in the circuit of Fig.3 (b). The transistor $\beta_{DC}=150$. 12

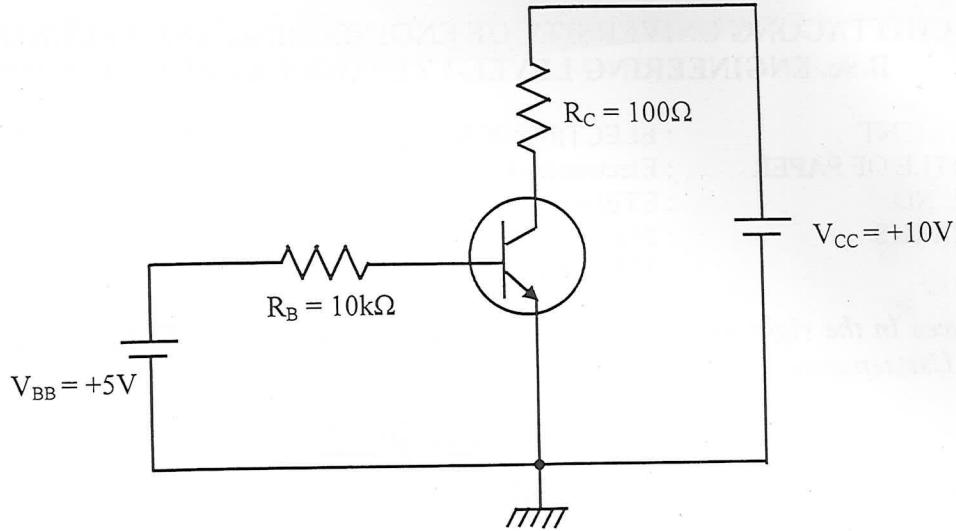


Fig.3(b)

- (c) Why Zener diode is used as a voltage regulator? 05
- Q.4(a) Define α and β . Develop a relation between them. 07
- (b) Determine V_{CE} and I_C in the shift voltage divider biased transistor circuit of Fig.4 (b). 13
Here $\beta_{DC} = 100$.

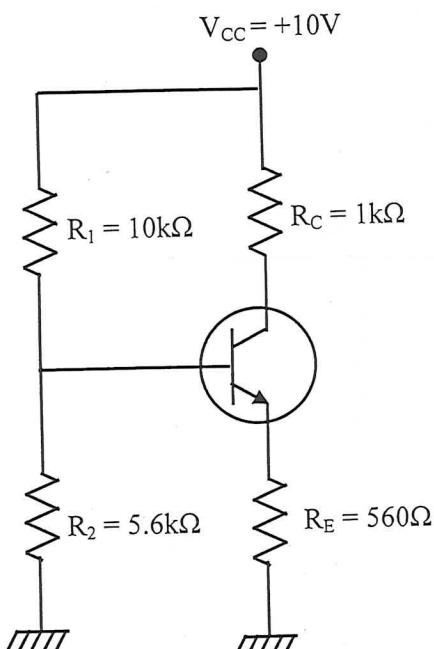


Fig. 4(b)

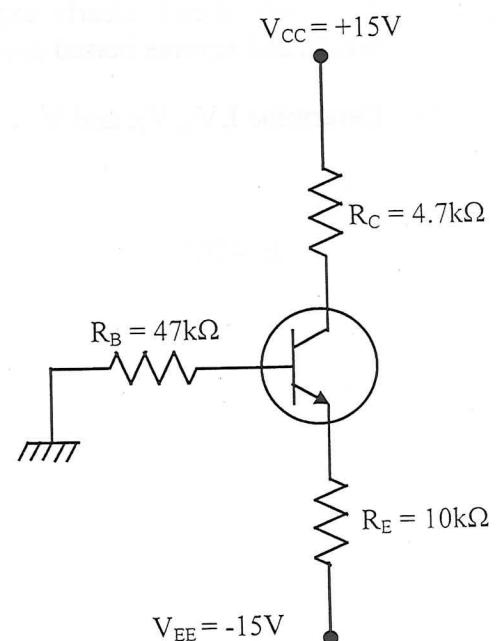


Fig. 4(c)

- (c) Determine how much Q point (I_C , V_{CE}) for the circuit in Fig.4(c) will change β_{DC} 15 when one transistor replaced by another.
increase from 100 to 200.

Section-B

- Q.5(a) Determine the total input resistance of the emitter-follower in Fig.5(a). Also find the 18 voltage gain, current gain and power gain in terms of power delivered to the load R_L . Assume $\beta_{DC} = 175$ and the capacitive reactance is negligible at the frequency of operation.

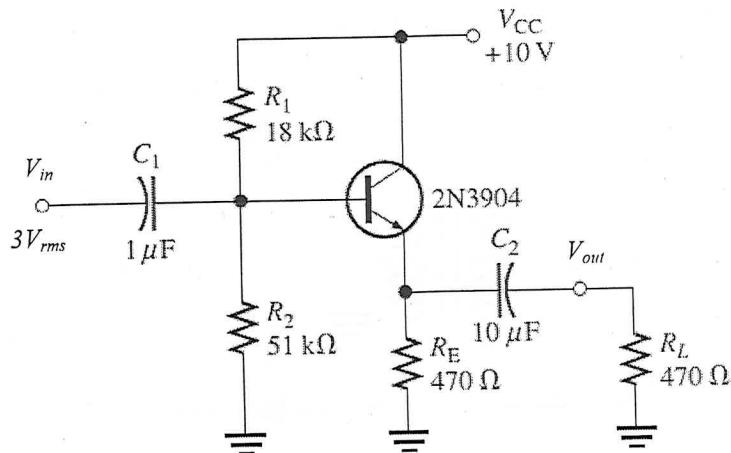


Fig.5(a)

- (b) For the capacitively-coupled multistage amplifier shown in Fig. 5(b), Find

- Voltage gain at first stage
- Voltage gain at second stage
- Overall voltage gain.
- DC voltages in the capacitively coupled multistage amplifier

$$\beta_{DC} = \beta_{AC} = 150 \text{ for } Q_1 \text{ and } Q_2.$$

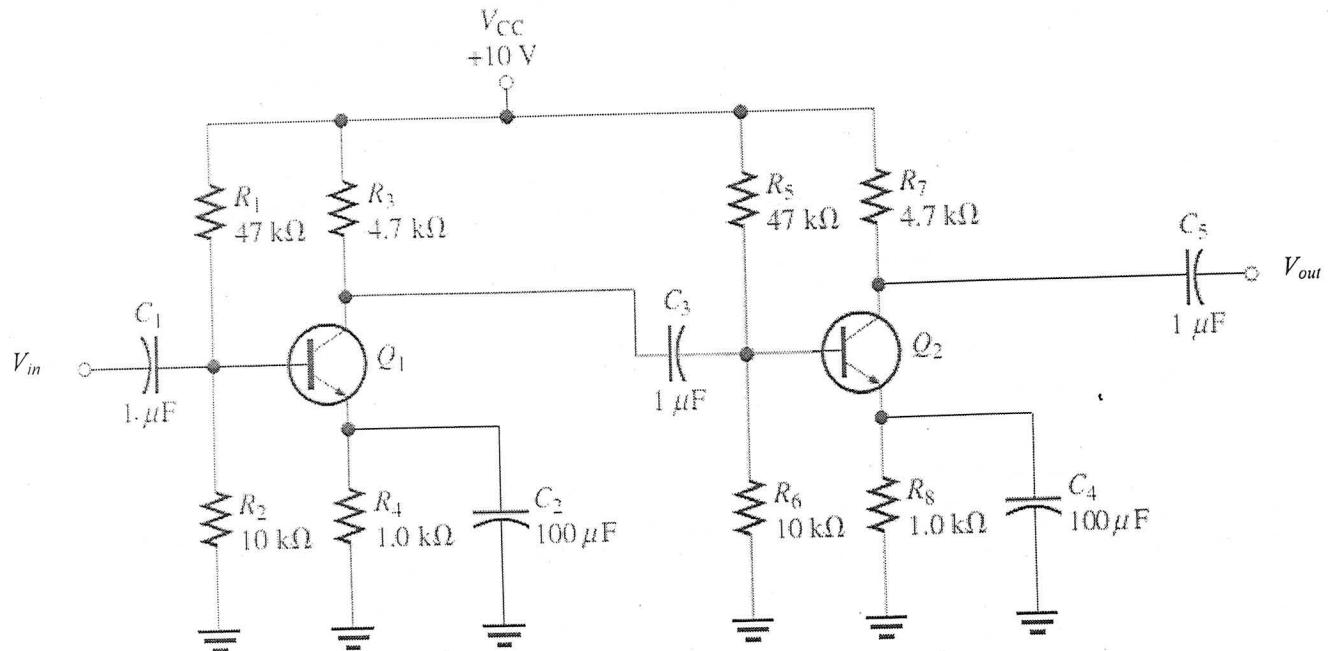


Fig.5(b)

- Q.6(a) Briefly explain the overall frequency response for the coupling and bypass capacitors for 12
an amplifier.
- (b) Explain how channel is created in depletion type MOSFET. 10
- (c) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig.6(c), given that for 13
this particular JFET the parameter values are such that $V_D = 7V$.

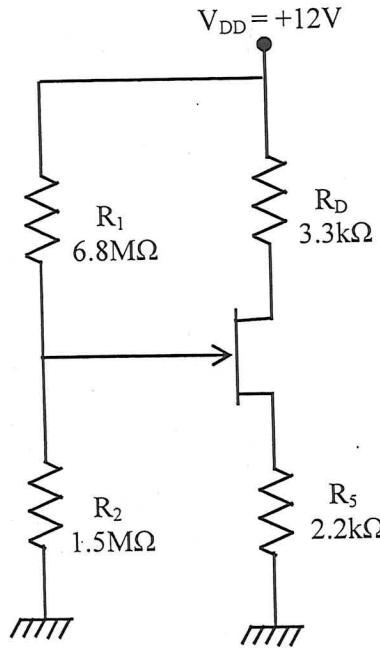
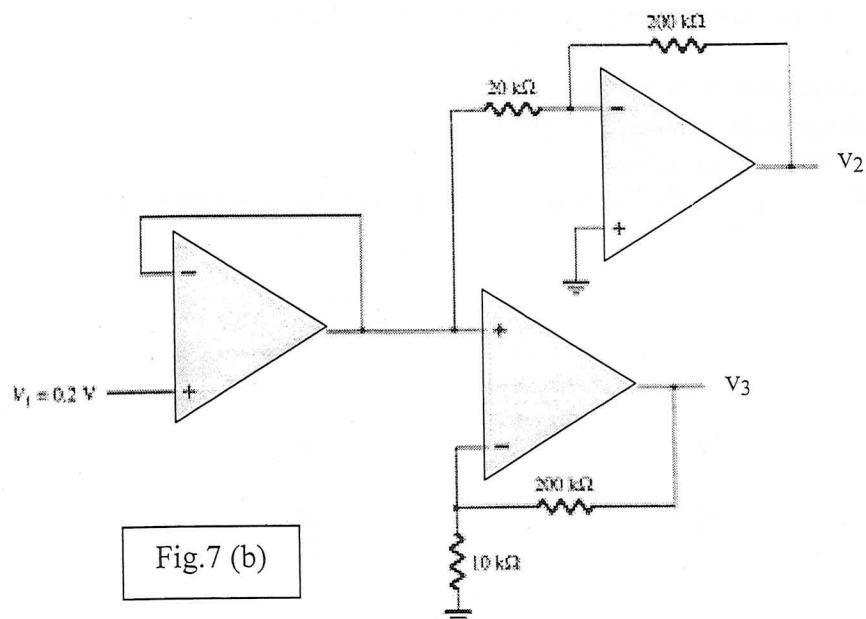


Fig.6(c)

- Q.7 (a) Determine the output voltage of an Op-amp for input voltages of $V_{i1}=150\mu V$, $V_{i2}=140\mu V$. The amplifier has a differential gain of $A_V= 4000$ and the value of CMRR is 100. 13
- (b) Calculate the output voltages v_2 and v_3 for the circuit of Fig.7(b) 12



- (c) Calculate the output voltage using the circuit of Fig.7(c) for resistor component of 10
 $R_f = 470\text{k}\Omega$; $R_1 = 4.3\text{k}\Omega$; $R_2 = 33\text{k}\Omega$ and $R_3 = 33\text{k}\Omega$ for an input of $80\mu\text{V}$

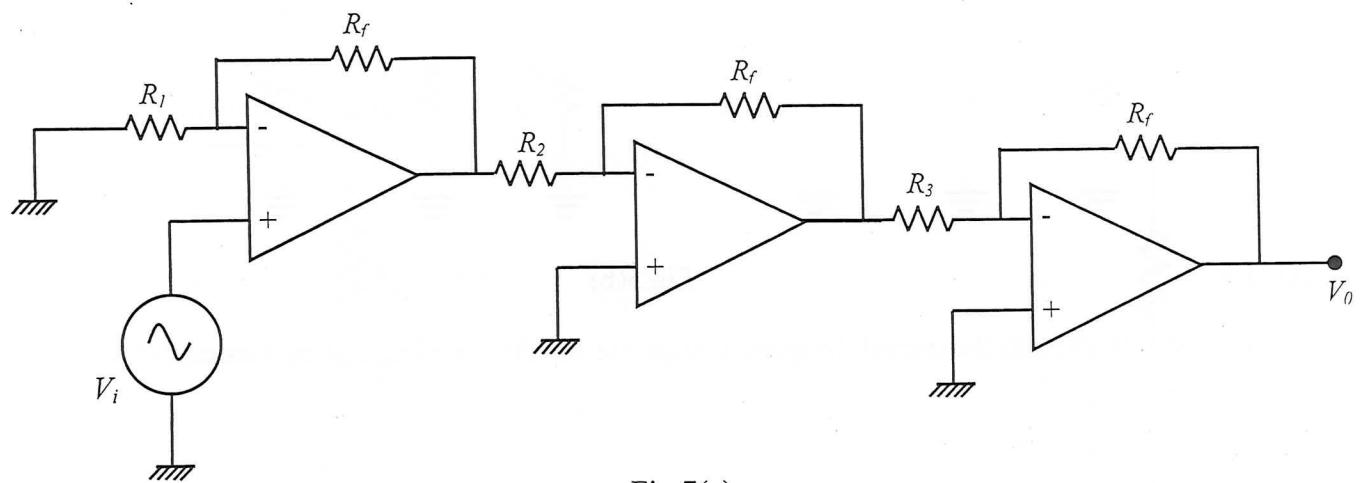


Fig.7(c)

- Q.8(a) Explain the operation of an astable multivibrator using 555 timer with necessary 15
diagram.
- (b) A 555 timer configured to run in the astable mode (oscillator) is shown in Fig.8 (b). 12
Determine the frequency of the output and the duty cycle.

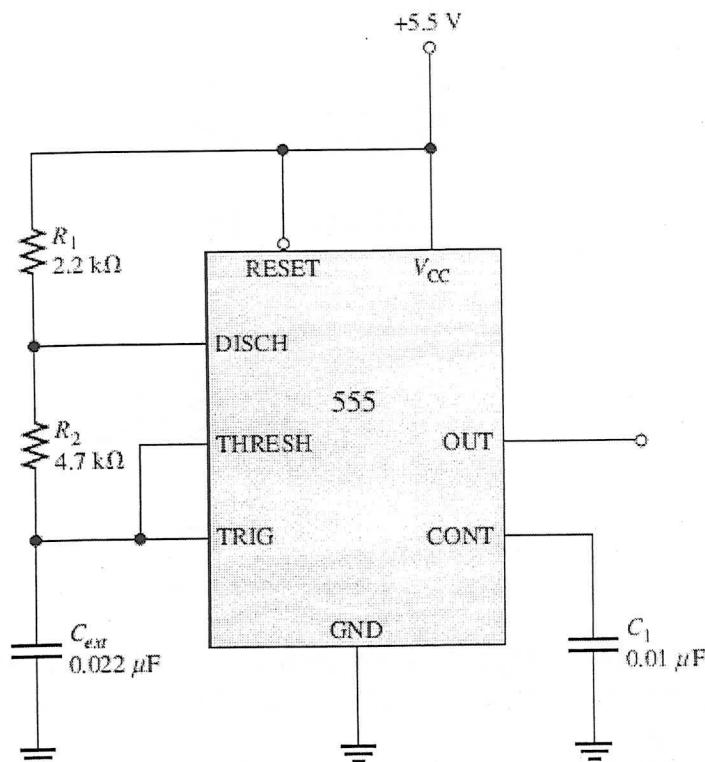


Fig.8 (b)

- (c) Explain in brief on Phase Locked Loop (PLL). 08

The End

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FULL TITLE OF PAPER	: Electronics-I
COURSE NO.	: ETE-101
FULL MARKS	: 210
TIME	: 3 HOURS

The figures in the right margin indicate full marks. Answer any THREE questions from each section. Use separate script for each section.

Section-A

- Q.1(a) What is the difference between a pentavalent and trivalent atom? 10
- (b) Explain how valence electrons determine the electrical properties of a material? What is 12 the difference between donor and acceptor impurities?
- (c) What do you understand by the d.c. and a.c. resistance of a p-n diode? How will you 13 determine them from the V-I characteristics of a diode?
- Q.2(a) With the help of Energy Band Diagram explain how semiconductors differ from 12 conductors and insulators.
- (b) Determine the output voltage waveform for each circuit of Fig.2 (b). Consider the diodes 12 are ideal.

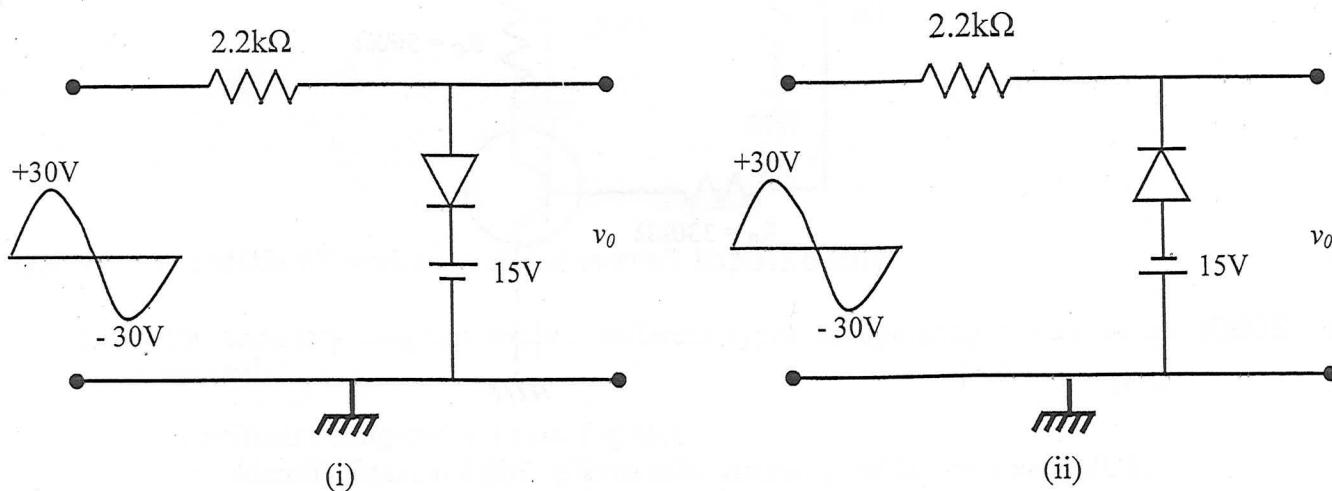


Fig. 2(b)

- (c) What should be the magnitude of R and C in order to design a clamping network? Draw 11 the output voltage v_o for the network of Fig. 2(c) for the input indicated.

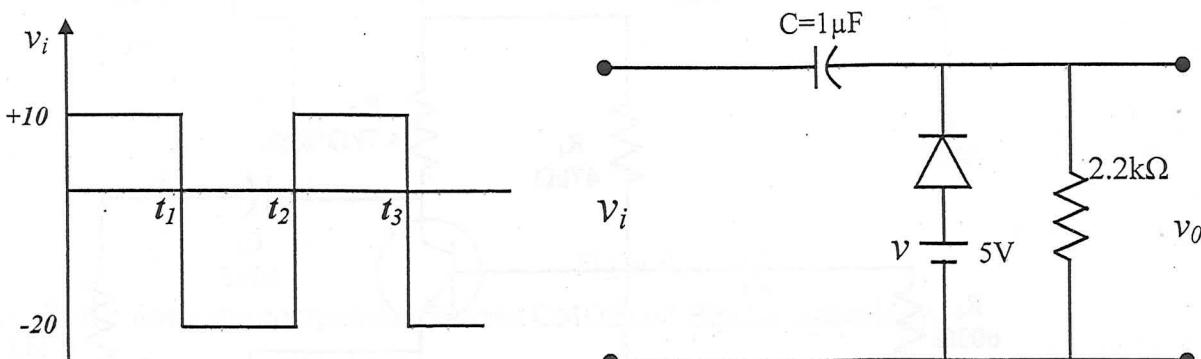


Fig.2(c)

Q.3(a) Find I_C and V_{CE} for the pnp transistor circuit of Fig. 3(a)

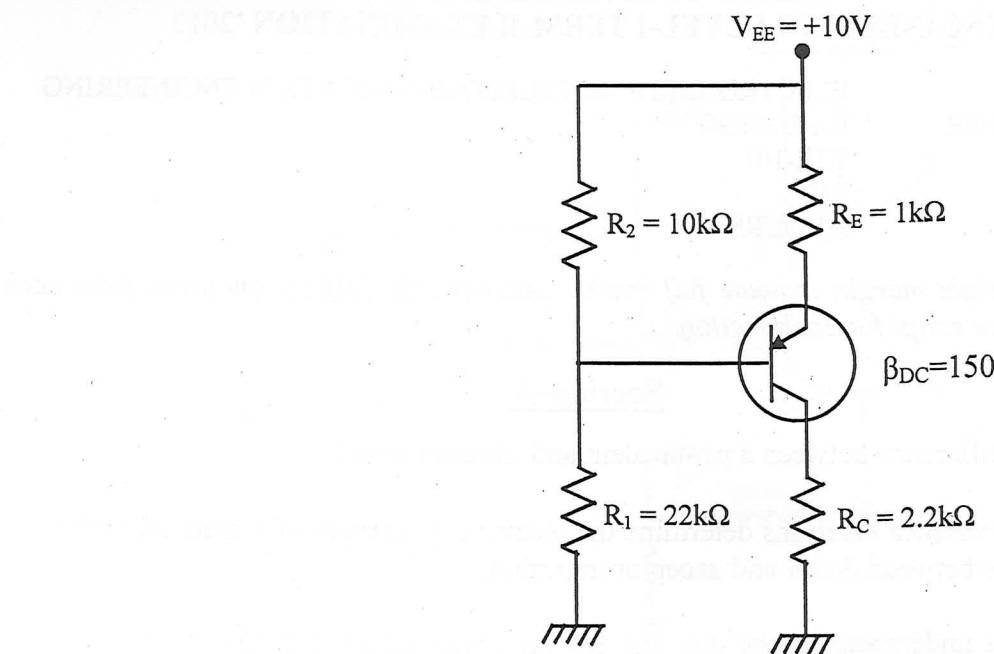


Fig.3(a)

- (b) How much the Q point (I_C , V_{CE}) for the circuit of Fig. 3(b) will change over a 15 temperature range where β_{DC} increases from 100 to 200.

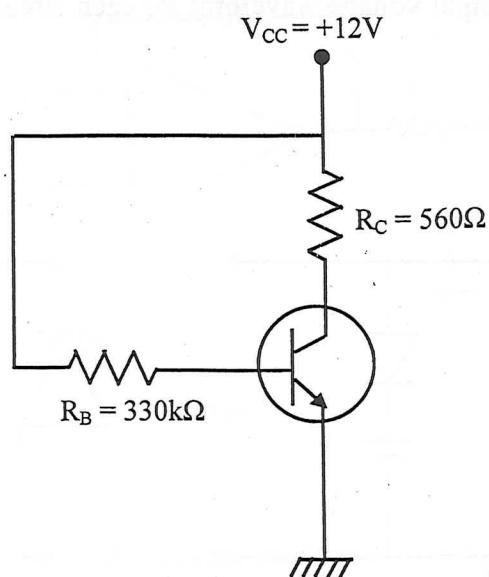


Fig. 3(b)

Q.4(a) For the amplifier of Fig.4(a)

20

- Determine the dc collector voltage
- Determine the ac collector voltage

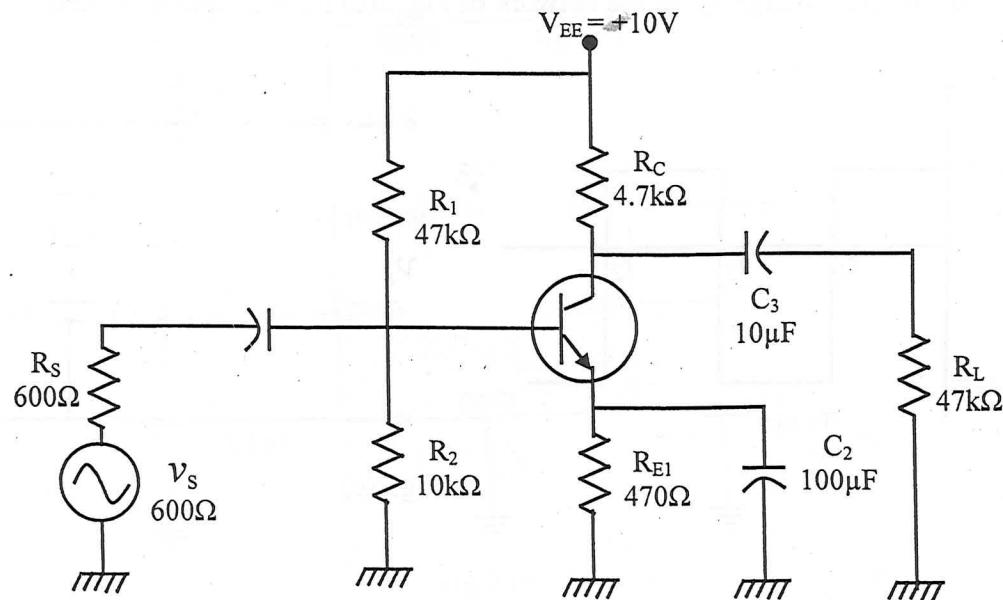


Fig.4(a)

- (b) What is emitter-follower? Why it is called so? 08
- (c) Explain the effect of coupling capacitor and bypass capacitor at lower frequency for BJT and FET amplifier. 07

Section-B

- Q.5(a) Explain the operation of a transistor as an amplifier. 10
- (b) What are the disadvantages of Fixed-bias method of a transistor? How can you minimize it? Explain with circuit diagram. 10
- (c) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig.5(c), given that for this particular JFET the parameter values are such that $V_D = 7V$. 10

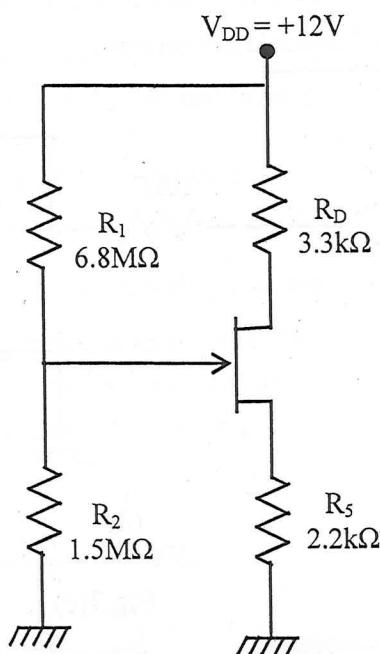


Fig.5(c)

- Q.6 (a) "The MOSFET works as a digital switch"- Explain briefly. 07
- (b) With necessary diagram explain different types of operating modes of an NMOS transistor. 08
- (c) In the circuit configuration below Fig.6(c)
 i) Identify Drain and Source terminals; assuming the device is an NMOS.
 ii) Identify the operating region of each transistor
 iii) Determine the drain current.
 Assume $V_{Dsat} = 1V$; $V_{th}=0.5V$ and $K_n(W/L)=1mA/V^2$; ignore the body effect. 12

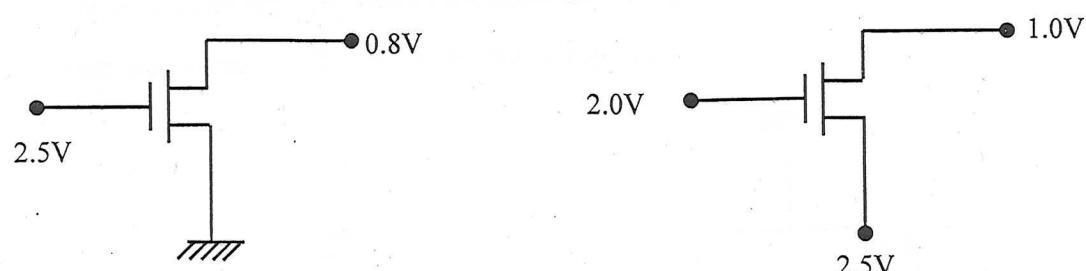


Fig.6(c)

- (d) Write down the comparison between CMOS and Bipolar technology. 08
- Q.7(a) What are the benefits of negative feedback in an op-amp circuit? What mathematical operation can be performed by an op-amp? 10
- (b) Define CMRR and Slew rate for op-amp. 10
- (c) Calculate the output voltage v_o for the circuits of Fig. 7(c) 15

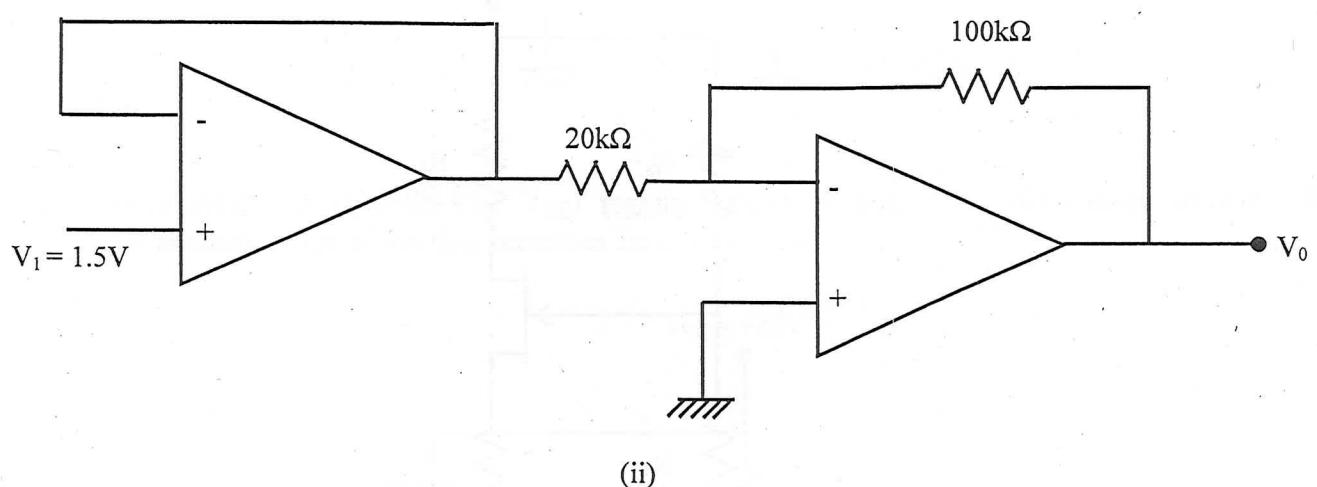
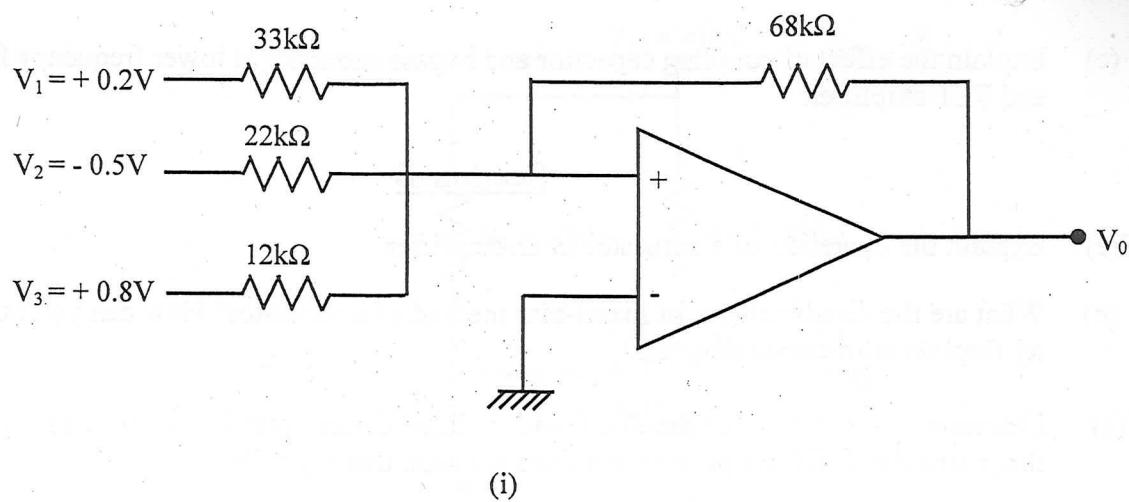


Fig.7(c)

- Q.8(a) Draw the schematic diagram of op-amp connected as i) Integrator ii) Differentiator 15
 iii) Adder, also mention the expression for output voltage.
- (b) What is a Multivibrator? Explain the principle on which it works. What is the basic 10
 difference among the three types of multivibrator
- (c) Sketch the circuit of a 555 timer connected as an astable multivibrator for operation at 10
 350kHz. Determine value of capacitor C, needed using $R_A=R_B=7.5\text{k}\Omega$ where the symbols
 represent their usual meaning.

The End