Experiment 2

Output Characteristics Analysis of Fixed Bias and Voltage Divider Bias

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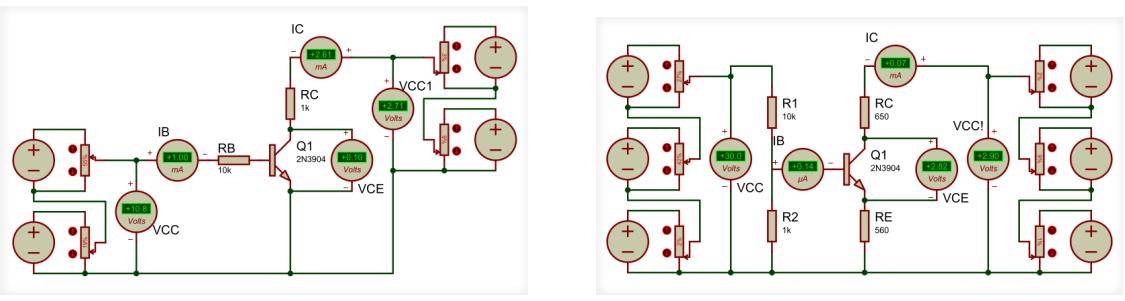
1 Objective

1. To determine the output characteristics of fixed bias configuration
2. To determine the output characteristics of voltage divider bias configuration

2 Apparatus

1. Transistor (2N3904 n-p-n)
2. Resistors ($10k\Omega$, $1k\Omega$, 650Ω, 560Ω)
3. Multimeter
4. Ammeters (mA and μA)
5. Breadboard
6. Wires
7. DC Power Supply (0-30V)

3 Circuit Diagram



(a) Fixed Bias Configuration (b) Voltage Divider Bias Configuration

Figure 1: Circuit Diagrams

4 Data Analysis

4.1 Theoretical Data

4.1.1 Fixed Bias Configuration

$I_B = 0\mu A$			$I_B = 11\mu A$		
V_{CC} (V)	V_{CE} (V)	I_C (mA)	V_{CC} (V)	V_{CE} (V)	I_C (mA)
2.7	2.7	0.0	0.0	0.0	0.0
5.7	5.7	0.0	2.7	1.6	1.1
9.0	9.0	0.0	5.6	4.5	1.1
11.1	11.1	0.0	9.0	7.9	1.1
15.0	15.0	0.0	12.0	10.9	1.1
18.0	18.0	0.0	15.3	14.2	1.1
21.9	21.9	0.0	18.4	17.3	1.1
25.2	25.2	0.0	21.8	20.7	1.1
28.0	28.0	0.0	25.2	24.1	1.1

Table 1: caption

$$I_C = \beta I_B$$
$$V_{CE} = V_{CC} - I_C R_C$$

4.1.2 Voltage Divider Bias Configuration

$I_B = 0\mu A$			$I_B = 0.14\mu A$		
V_{CC} (V)	V_{CE} (V)	I_C (mA)	V_{CC} (V)	V_{CE} (V)	I_C (mA)
0.0	0.0	0.0	0.0	0.0	0.0
3.0	3.0	0.0	3.0	2.9831	0.014
8.0	8.0	0.0	8.0	7.9831	0.014
10.0	10.0	0.0	10.7	10.683	0.014
14.0	14.0	0.0	14.7	14.683	0.014
17.0	17.0	0.0	17.7	17.683	0.014
20.0	20.0	0.0	20.7	20.683	0.014
24.0	24.0	0.0	24.7	24.683	0.014
27.0	27.0	0.0	27.6	27.583	0.014

Table 2: caption

$$I_C = \beta I_B$$
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

4.2 Simulation Data and Practical Data

4.2.1 Fixed Bias Configuration

Simulation Data			**Practical Data**			**Errors**	
$I_B = 0\mu A$							
V_{CC} (V)	V_{CE} (V)	I_C (mA)	V_{CC} (V)	V_{CE} (V)	I_C (mA)	$\%V_{CE}$	$\%I_C$
0	0	0	0	0	0	0	0
2.7	2.7	0	2.7	2.02	0	25.19	0
5.6	5.6	0	5.6	5.01	0	10.54	0
9	9	0	9	8.16	0	9.33	0
12	12	0	12	10.5	0	12.5	0
15.3	15.3	0	15.3	13.9	0	9.15	0
18.4	18.4	0	18.4	17.5	0	4.89	0
21.8	21.8	0	21.8	21.27	0	2.43	0
25.2	25.2	0	25.2	24.3	0	3.57	0
28.2	28.2	0	28.2	27.2	0	3.55	0
$I_B = 11\mu A$							
V_{CC} (V)	V_{CE} (V)	I_C (mA)	V_{CC} (V)	V_{CE} (V)	I_C (mA)	$\%V_{CE}$	$\%I_C$
0	0	0	0	0	0	0	0
2.73	1.86	0.86	2.7	1.56	1	16.13	16.28
5.65	4.74	0.91	5.6	4.2	1	11.39	9.89
8.98	8.01	0.97	9	7.33	1	8.49	3.09
11.9	10.9	1.02	12	10.01	1	8.17	1.96
15.3	14.2	1.08	15.3	13.69	1	3.59	7.41
18.4	17.2	1.13	18.4	16.63	1.1	3.31	2.65
21.8	20.6	1.19	21.8	20.1	1.2	2.43	0.84
25.2	24	1.25	25.2	23.07	1.2	3.88	4
28.2	26.9	1.3	28.2	25	1.2	7.06	7.69

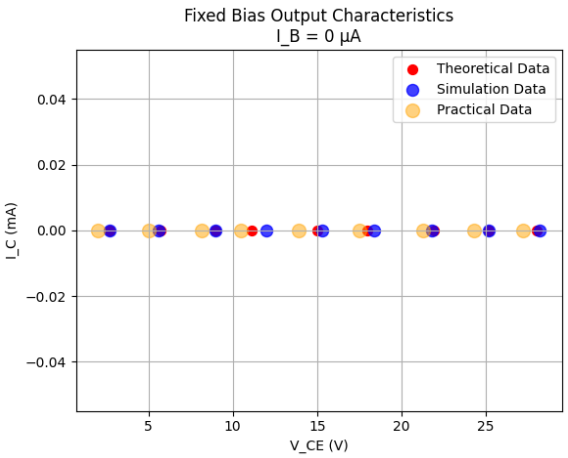
Table 3: Data Analysis for Fixed Bias Configuration

4.2.2 Voltage Divider Bias Configuration

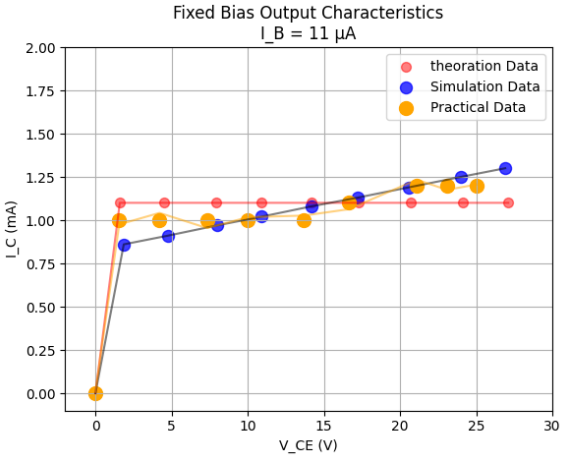
Simulation Data			**Practical Data**			**Errors**	
$I_B = 0\mu A$							
V_{CC} (V)	V_{CE} (V)	I_C (mA)	V_{CC} (V)	V_{CE} (V)	I_C (mA)	$\%V_{CE}$	$\%I_C$
0	0	0	0	0	0	0	0
3	3	0	3	2.7	0	10	0
8	8	0	8	7.6	0	5	0
10	10	0	10	9.3	0	7	0
14	14	0	14	13.87	0	0.93	0
17	17	0	17	16.4	0	3.53	0
20	20	0	20	19.1	0	4.5	0
24	24	0	24	23.6	0	1.67	0
27	27	0	27	26.7	0	1.11	0
$I_B = 0.14\mu A$							
V_{CC} (V)	V_{CE} (V)	I_C (mA)	V_{CC} (V)	V_{CE} (V)	I_C (mA)	$\%V_{CE}$	$\%I_C$
0	0	0	0	0	0	0	0
3	2.91	0.07	3	2.91	0.07	3.09	90
8	7.9	0.08	8	7.9	0.07	1.27	88.57
10.7	10.6	0.09	10.7	10.6	0.07	0.94	87.14
14.7	14.5	0.1	14.7	14.5	0.11	1.38	10
17.7	17.5	0.11	17.7	17.5	0.11	1.14	0
20.7	20.5	0.12	20.7	20.5	0.11	0.98	8.33
24.7	24.5	0.13	24.7	24.5	0.11	0.82	15.38
27.6	27.5	0.14	27.6	27.5	0.11	0.36	21.43

Table 4: Data Analysis for Voltage Divider Bias Configuration

5 Graphs

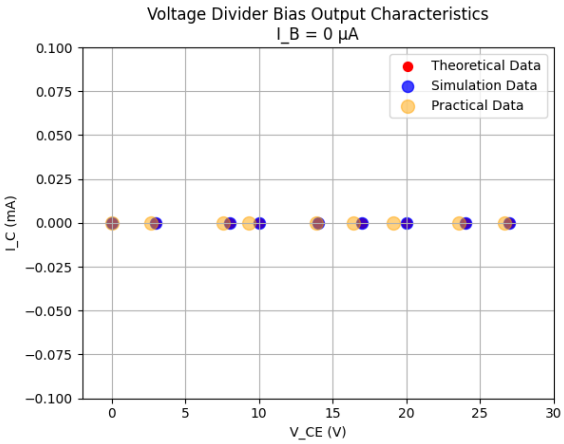


(a) $I_B = 0\mu A$

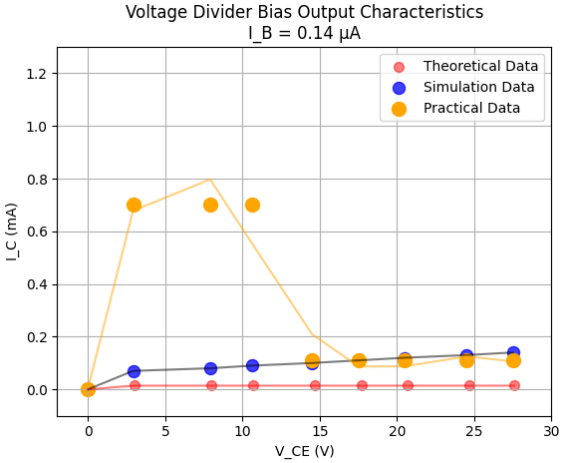


(b) $I_B = 11\mu A$

Figure 2: Output Characteristics of Fixed Bias Configuration



(a) $I_B = 0\mu A$



(b) $I_B = 0.14\mu A$

Figure 3: Output Characteristics of Voltage Divider Bias Configuration

From the graphs, we can see that the theoretical data, the simulation, and the practical data are not exactly equal. This is due to some technical errors and precision errors. From the graph, a connecting line drawn between $V_{CE} = 0$ and $I_C = 0$ will intersect the output characteristic plot at a point called the Q-point or operational point. This Q-point can be modified by varying the values of V_{CC} and R_C.

6 Discussion

(a) The experiment was conducted to learn about the biasing of transistors. Two biasings were analyzed: fixed bias, and voltage divider bias.

(b) All the biases were made using a 2N3904 n-p-n transistor in a common-emitter configuration.

(c) The output characteristics of the two biasing configurations were plotted and analyzed.

(d) The output characteristic graphs for simulation and practical data were plotted and compared.

(e) Error of the practical data from the simulation data was calculated.

(f) The errors were considered to happen due to technical errors and precision errors.

(g) More accurate equipment could be used to reduce the errors.