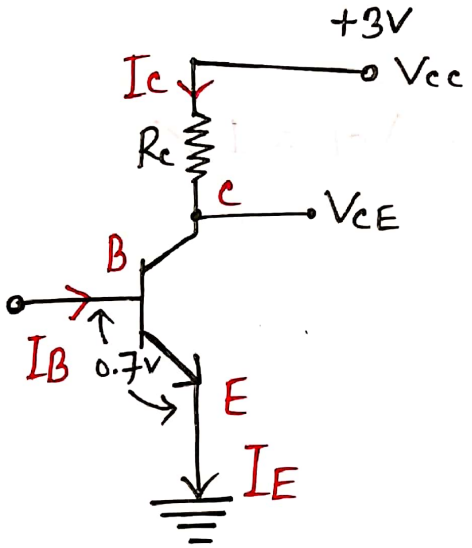
4. Transistor Biasing.



(1) $V_{BE} < 0.7V$: $I_B = 0$

$I_c = 0$

No voltag Drop in Rc, $\therefore V_{CE} = 3V = V_{cc}$ (max)

cutoff

(2) $V_{BE} \geq 0.7 \Rightarrow V_{BE} \simeq 0.7V$

$R_c = 1k\Omega$, $I_B = 10\mu A$

$I_c = \beta I_B \quad \therefore I_c = 1mA$

$V_{Rc} = 1 \times 1 = 1V$

$V_{CE} = 2V$

output current Amplify

Voltage decrease

$I_B = 20\mu A$

$I_c = 2mA$

$\therefore V_{CE} = 1V$

$V_{Rc} = 2 \times 1 = 2V$

$I_B = 30\mu A$ ($V_{CE} = 0$)

$I_B = 40\mu A$ ($V_{Rc} = 4V$) Not possible

Output current will not Increase any more. $I_c = 3mA$

$V_{BE} \simeq 0.7V$

$0 < I_B < 30\mu A$

$I_c = \beta I_B$, $V_{CE} < 0$

Amplify current

Linear Region

$I_B > 30\,\mu A$

$I_c = 3\,mA\,(max)$, $V_{CE} = 0\,(min)$

Saturation

Transistor Biasing (DC)

1. Load line Analysis

- Floyd: Chapter 5: 5-1 (Full)

2. DC Biasing configuration

- Boylestad: Chapter 4: 4.3, 4.4, 4.5, 4.6

4.7 + PNP → Fixed bias configuration.

↳ 4.11 (4.27 example)

See also Floyd.

Maths: Boylestad

DC Biasing – BJTs

$V_{BE} = 0.7\ V$

$I_E = (\beta+1)\, I_B \cong I_C$

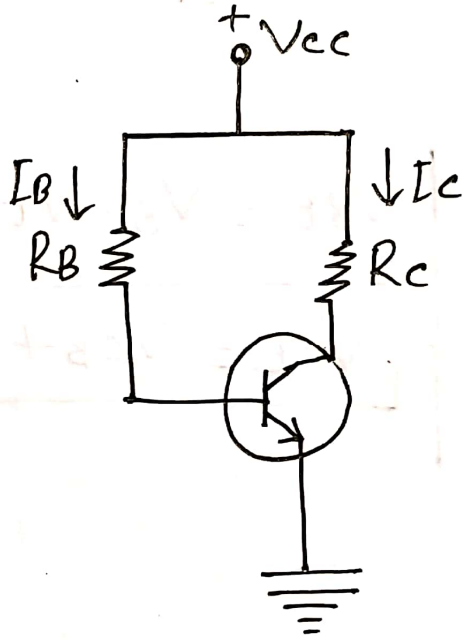
$I_C = \beta\, I_B$

Operating Point / Quiescent point / Q-point

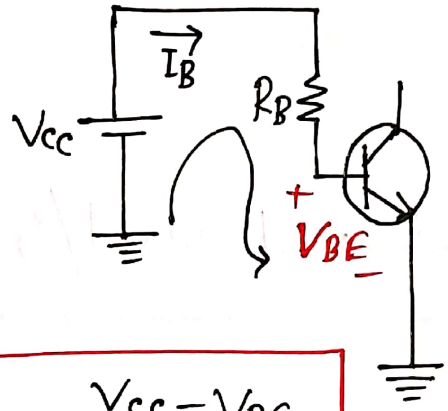
1. Linear: Base-emitter forward
   Base-collector reverse
2. Cutoff: Both reverse
3. Saturation: Both forward

Fixed-Bias Circuit

Circuit



Base-Emitter Loop:



Loop:

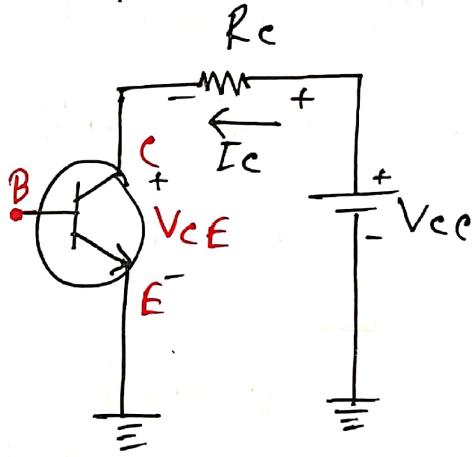
$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

Collector-Emitter Loop:

$$\boxed{I_C = \beta I_B}$$



$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$V_E = 0$

$$\therefore V_{CE} = V_C$$

$$V_{BE} = V_B - V_E = V_B$$

$$\boxed{V_{CE} = V_{CB} + V_{BE}}$$

Transistor Saturation:

→ Maximum I_c

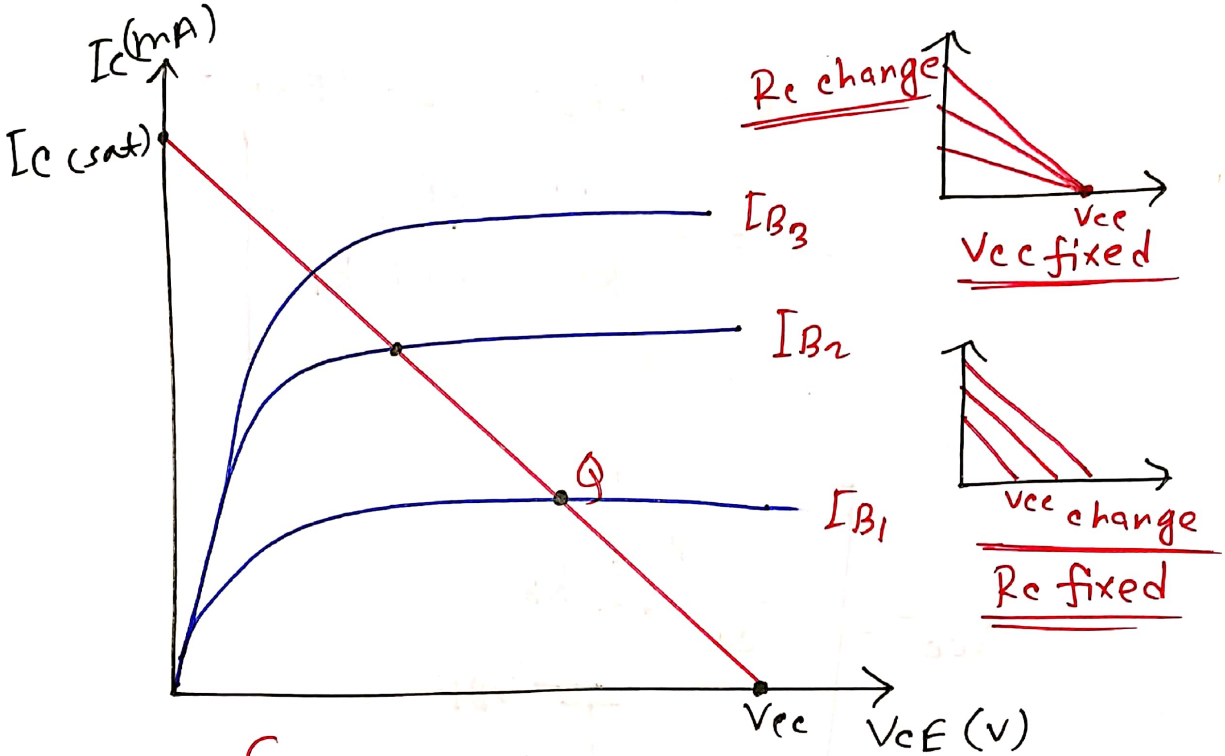
→ Avoided: b-c junction not in reverse, output distorted.

$V_{CE} = 0$ $\quad R_{CE} = \frac{V_{CE}}{I_c} = \frac{0V}{I_{c_{sat}}} = 0\,\Omega$

$$I_{C(sat)} = \frac{V_{cc}}{R_c}$$

Load-Line analysis: Det. Q-point and range

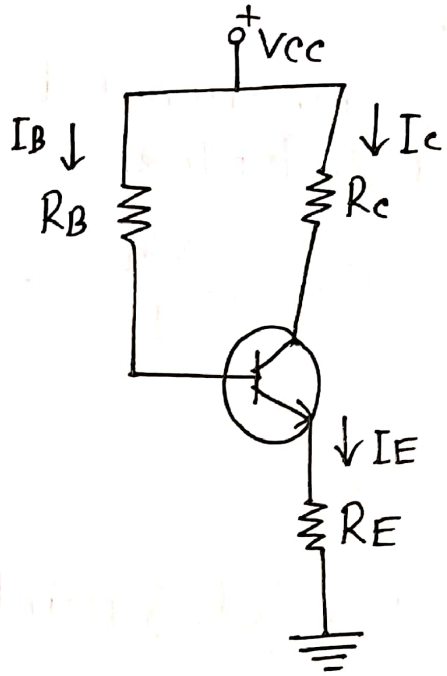
$$V_{CE} = V_{cc} - I_c R_c$$



$$\begin{cases} V_{CE} = V_{cc} \,\big|_{I_c = 0\,mA} \\ I_c = \frac{V_{cc}}{R_c} \,\big|_{V_{CE} = 0V} \end{cases}$$

I_B → change → Q-point change.

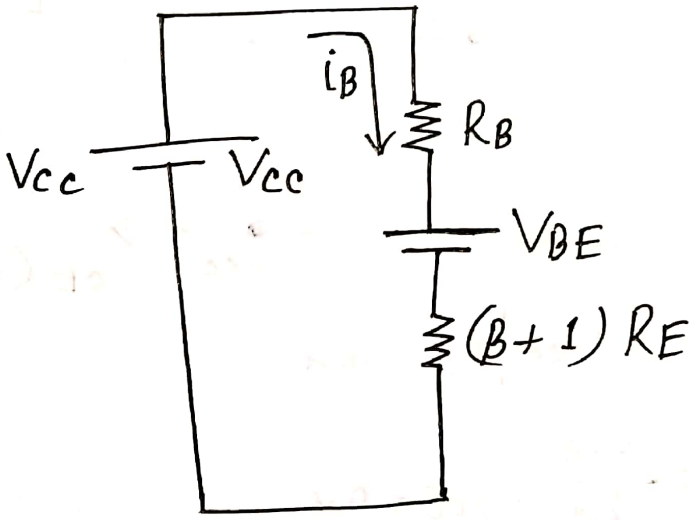
Emitter - Stabilized Bias Circuit



Base emitter Loop:

$$+V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$$

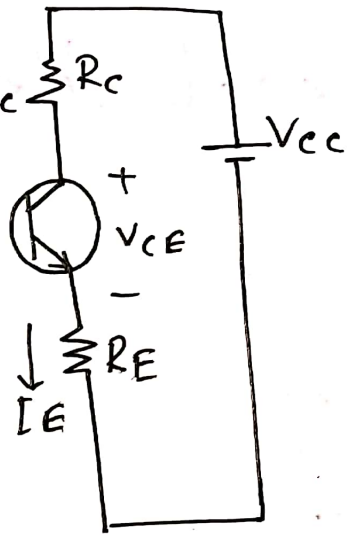
$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E}$$



Collector- Emitter Loop

$$V_{CE} = V_{cc} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{cc} - I_C (R_C + R_E)$$



$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{cc} - I_C R_C$$

Base voltage:

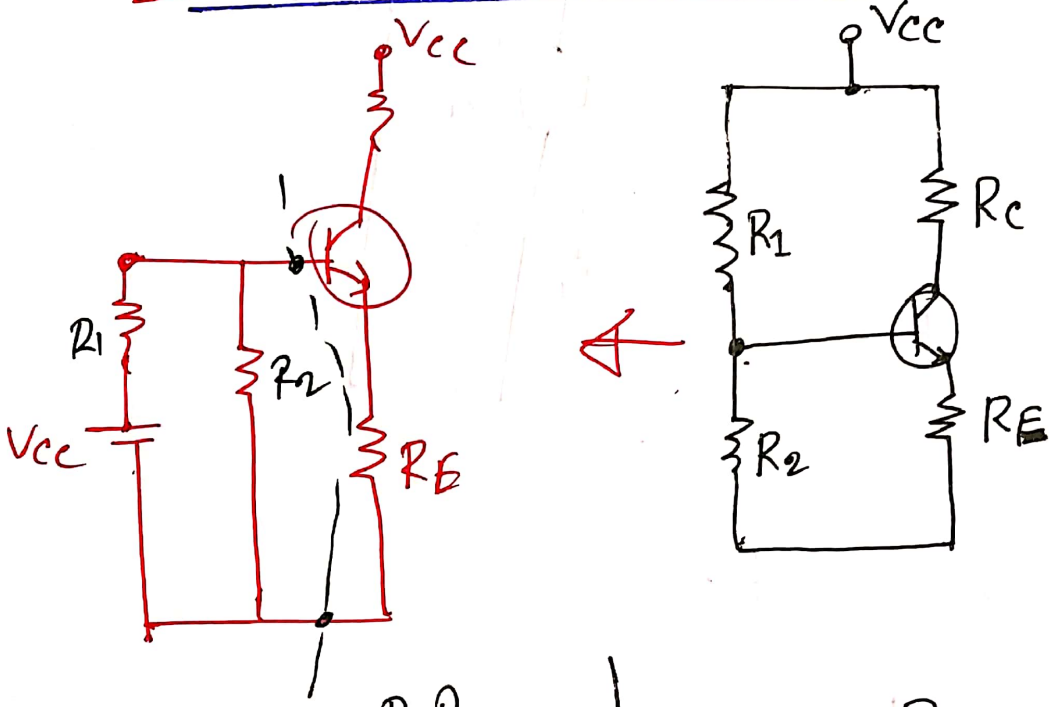
$$V_B = V_{BE} + V_E$$

$$V_B = V_{cc} - I_B R_B$$

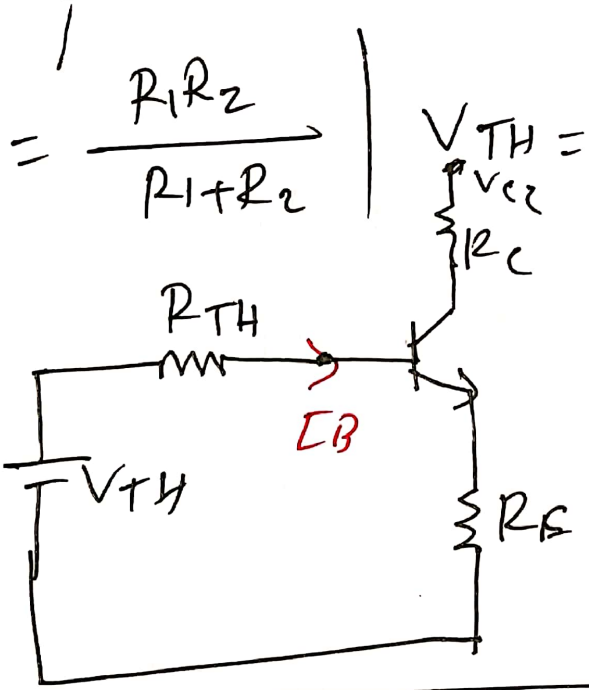
Voltage Divider Bias

β independent

Exact Method:



$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \qquad V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$



$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$

$$V_{CE} = V_{CC} - I_E (R_E + R_C)$$