Slide → 8086 Interfacing Part 1

Define Chip Capacity

Ans:

The number of bits/ bytes that a Semi Conducton memory chip can store is called its chip capacity.

On which thing address space depends

Ans:

The size of the address space depends on the number of address lines of the micro-Processon

* Semi-Conducton memories are used as Primary storage for data & code.

Describe different types of lines & on Connections

Ans:

A memory device on chip must have 4 types of lines on Connections

a. Address Line
b. Data Line
C. Enable Line
d. Control Line

Address Line:

1. The input lines that select a memory location within the memory device
2. De-coders are used, inside the memory chip, to select a specific location
3. The number of address pins on a memory chip specifies the number of memory locations. Number of memory location = 2^n

Data Line:

1. The data pins are bi-directional in read-write memories
2. The number of data pins is related to the size of the memory location. Example: 8 bit wide (byte-wide) memory device has 8 data pins.
3. The number of data lines (m-bits) determines the size of each location in the memory. Memory capacity = $2^n \times m$

Enable Line:

1. All memory devices have at least one chip select ($\overline{CS}$) or chip enable ($\overline{CE}$) input used to select or enable the memory device.
2. $\overline{CS}$ / $\overline{CE}$ input is usually controlled by the micro-processor through the higher address lines via an address de-coding circuit

Control Line:

1. RAM chips have two control input signals that specify the type of memory operation: the Read ($\overline{RD}$) & the Write ($\overline{WR}$).
2. ROM chips can perform only memory read operations

=> Number of memory Location = 2^n

=> Memory Capacity = $2^n \times m$

=> Some RAM chips have a common Read/Write ($R/\bar{W}$) signal.

=> In most real ROM devices the Read signal is called the Output Enable ($\bar{O}E$) signal.

Draw RAM Memory Chip Diagram

Ans:-

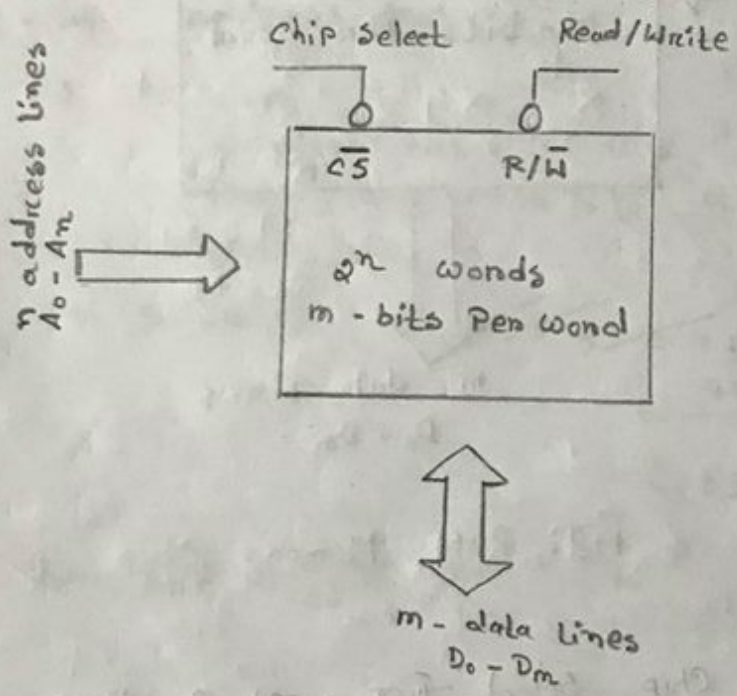


Fig: RAM Memory Chip

Draw ROM memory chip diagram

Ans;

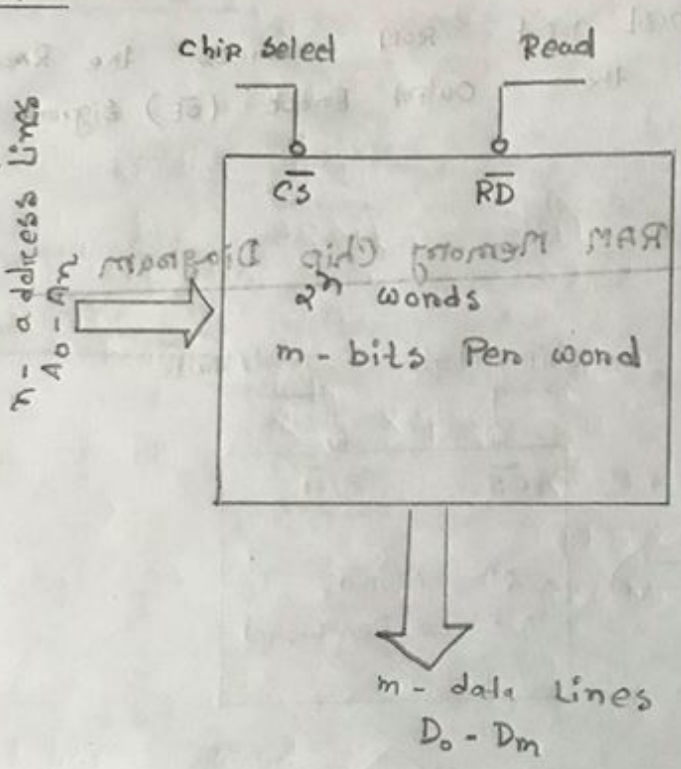
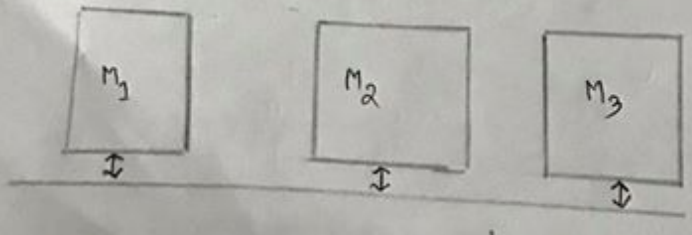


Fig: ROM Memory Chip

* $\overline{CS}$ => Chip Select দিয়ে at a time একটা RAM chip কথা বলে।
* Chip Select ($\overline{CS}$) কে 0 বা low তে Active করে।



	Base 2	Base 10
kilo	$2^{10} = 1024$	$10^3 = 1000$
Mega	$2^{20} = 1048576$	$10^6 = 1000\,000$
Giga	$2^{30} = 1073741824$	$10^9 = 1000\,000\,000$

* RAM Chip ⇒ data lines ⇒ bi-directional
* ROM Chip ⇒ data lines ⇒ single directional [Uni-directional]

RAM → High (Read)
→ Low (Write)

Q. Calculate total addressable memory in a RAM chip where there is a 16 bit data bus & a 32-bit address bus.

Ans:

Given
Address bus = 32 bit
Data bus = 16 bit it means 2 bit address line

So, ~~Therefore~~ ~~$2^{32} \times 2 = 4\,294\,967\,296 \text{bit} \times 2$~~

$= \frac{4\,294\,967\,296}{8} \text{byte} \times 2$

$= 536\,870\,912 \text{ byte} \times 2$

Therefore $2^{32} \times 2 = \frac{2^{32}}{2^{30}} \text{GB} \times 2$

$= 2^2 \text{GB} \times 2$

$= 4 \text{ GB} \times 2$

$= 8 \text{GB}$

Ans -

Calculate total addressable memory in a Rom chip when there is a 32-bit data bus & a 16 bit address bus.

Ans:

Given,

Address bus = 16 bit

Data bus = 32 bit

address lines

Therefore

$$2^{16} \times 4 = \frac{2^{16}}{2^{10}} \text{ KB} \times 4$$

$$= 2^6 \text{ KB} \times 4$$

$$= 64 \text{ KB} \times 4$$

$$= 256 \text{ KB}$$

Ans:

Define word.

Ans:

The number of bits that a CPU can process at one time.

=> 8086 এ 16 bit number নেওয়া যায়, AX এর মাঝে 16 bit.

16 bit = 1 word.

8 bit per word মানে 1 bit address line

Memory Chip

0	1111 - 1111
1	0101 - 1111

16 bits Per word এবং 4 bit address line
(8+8)

Memory Chip.

00	1111	1111 - 0000 - 1000
01	0101	1111 - 1100 - 0001
10	0010	1010 - 0101 - 1111
11	1000	0000 - 1111 - 0000

=> যত বেশি bit তত বেশি address
=> Input line -> Memory কোনটা select করবে।

- Micro - Processor => Volatile Memory.
- ROM Chip => Write signal থাকে না

$\overline{CS}$ = High
$\overline{WE}$ = Low
=> Input Bus [Write করার জন্য]

CS = High
$\overline{WE}$ = High
=> Output Bus [Read করার জন্য]

CS = 0 হলে Read / Write => don't care.

Q Write the main difference between RAM & ROM Chip.

Ans:

RAM is written under normal operation. ROM is Programmed outside the Computer & normally is only read.

RAM Chip Operation

CS	$\overline{WE}$	Mode	Status $D_7 - D_0$	Power
1	X	Not Selected	High Impedence	Stand by
H	L	Write	Acts as input bus	Active
H	H	Read	Acts as output bus	Active

* CS = L
$\overline{WE}$ = X হলে 86% Power reduce হয়
* $A_9 - A_0$ address line হিসেবে কাজ করে।

Q Define Impedence

Ans:

Low Current with high voltage.

RAM দুই ধরনের হয়

RAM
- SRAM
  Example: Micro-Controller
- DRAM
  Example: PC, Laptop, Servers, Mobile.

* Transistor switch এবং Amplifier হিসেবে ব্যবহার করা যায়।

Draw S-RAM Cell

Ans:

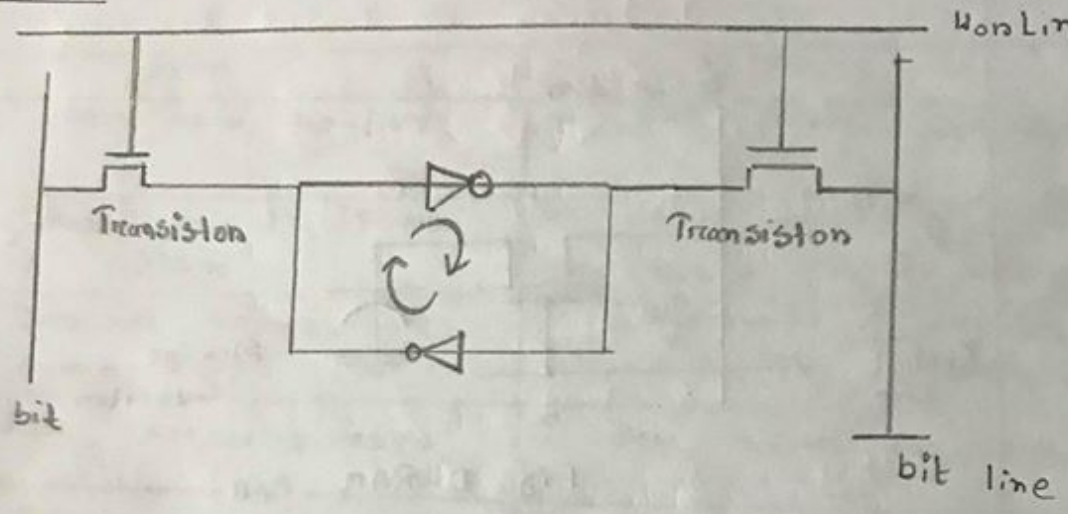


Fig: S-RAM Cell

Draw an inverter Circuit

Ans:

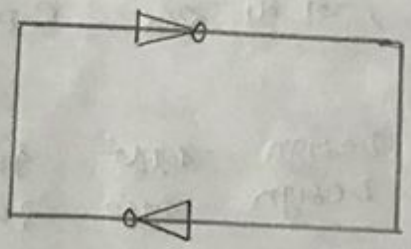


Fig: Inverter Circuit

Draw D-RAM cell

Ans:

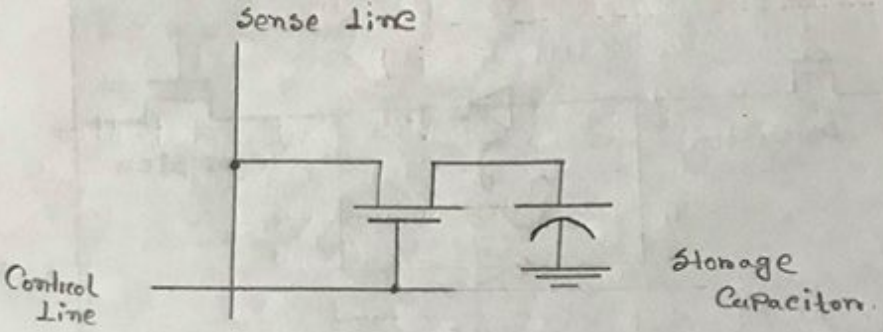


Fig: D-RAM cell

* S-RAM এর Value lock হয়ে যায়, Lock না হওয়া Value Power off / load shedding না হওয়া পর্যন্ত থাকবে,

* D-RAM এর ২-৪ ms পরপর rewritten করা লাগে, তা না হলে Capacitor change হারিয়ে ফেলে,

SRAM Design করতে ৬টা device লাগে
DRAM Design করতে ২টা device লাগে,

Why DRAM is used in servers?

Ans:

DRAM forms the larger system RAM space.

Write differences between S-RAM VS D- RAM

Ans:-

SRAM	DRAM
a. SRAM uses flip-flops	a. DRAM uses Capacitors.
b. Stores data till Power is supplied.	b. Stores data only for few seconds even when Power is supplied
c. Does not refresh the memory cell	c. Continuous refreshing is required to retain data
d. Data access is fasten	d. Data access is slower
e. Consume less Power	e. Consume more Power
f. Less memory Per chip	f. More memory Per chip
g. Cost Per bit is high.	g. Cost Per bit is low.

Define Memory Decoding

Ans:

It is the Process of generating Chip select signals from the address bus for each device in the system.

Why we need memory decoding.

Ans:

All the memory Locations are not implemented. All the address are not used by the memory devices to Select Particular memory locations. The unused lines are used to decode to generate chip select.

Memory Decoding ২ ধরনের হয়।

1. linear or Partial Decoding
2. Absolute or full Decoding

Write the advantages of linear decoding

Ans:

a. Simple
b. Cheap
c. Fast.

Write the disadvantages of linear decoding

Ans:

a. Unutilized space & fold back
b. Bus contention
c. Difficult future expansion.

Define Memory fold back

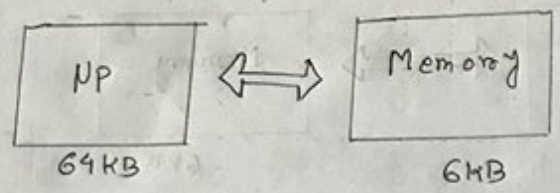
Ans:

Each memory location has more than one address called memory foldback.

Memory Decoding

Draw the diagram of 8-bit microprocessor with 16 bit address bus and 8 bit data bus interfaced with 6KB RAM using linear decoding method. Each RAM chip has 10 bit address bus and 8 bit data bus. Also provide the corresponding address map (starting address and end address) for each RAM chip

Ans:



Given

Address Bus = 10 bit
Data Bus = 8 bit

Memory size of a single RAM chip = $2^{10} \times 8$

$= 8192$ bits

$= \frac{8192}{8}$ bytes

$= 1024$ bytes

$= \frac{1024}{1024}$ KB

$= 1$ KB

Target = 6 KB

Which mean we will need 6 ram chips.

Memory size $\&$/ Capacity of Processor = $2^{16} \times 8$ bit

$= 524288$ bit

$= \frac{524288}{8}$ bytes

$= 65536$ bytes

$= \frac{65536}{1024}$ KB

$= 64$ KB

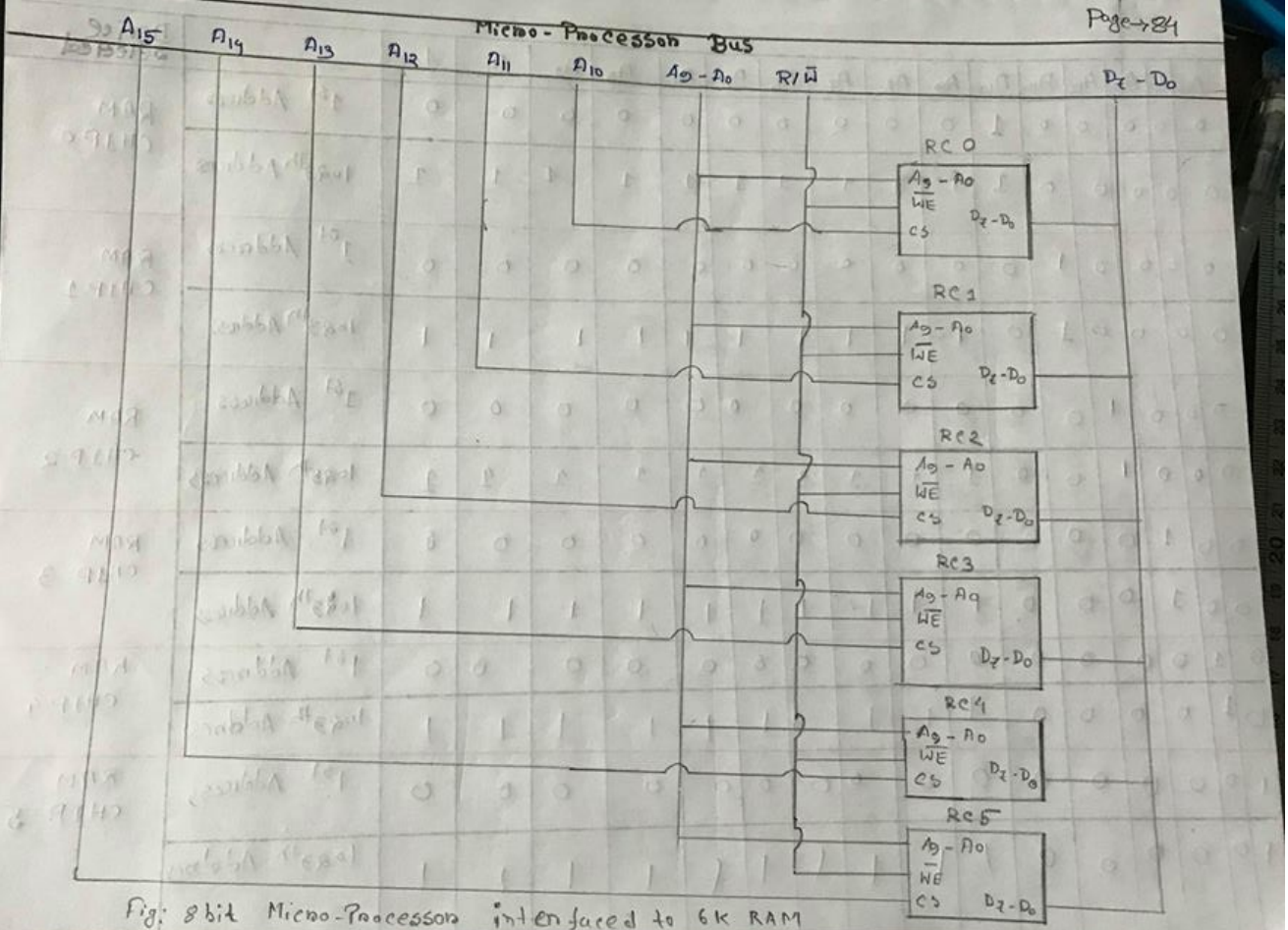


Fig: 8 bit Micro-Processor interfaced to 6K RAM

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Device selected
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1st Address	RAM CHIP 0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1023th Address	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1st Address	RAM CHIP 1
0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1023th Address	
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1st Address	RAM CHIP 2
0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1023th Address	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1st Address	RAM CHIP 3
0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1023th Address	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1st Address	RAM CHIP 4
0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1023th Address	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1st Address	RAM CHIP 5
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1023th Address	

* Address bus এর higher order Pin CS এর আগে দিব,
* Address map continuous হয় না।
* Connection দেওয়া শুরু হয় LSB থেকে
* আগের Page এর Math মতে 64KB Processor 64KB memory তে address করতেছে,
* 64KB Processor 68KB memory তে address করতে পারবে না,