Attion Coulomber I remote - ATTIGA 32 Page -> 3 1. Define Micro Controller Ans: A micro - Controller is a Compact integrated Cincuit designed to govern a specific operation in an embedded system. the block diagram of micro-Controllers 2. Draw Androngonal and HAPP OF SAL Harveryd Architecture. EATHER ATTA SIRMOND CPU Timen RAM Counter managery places & and the base the Michaels bord of the THE day neumann sental Amen Jeolune. Rom Poret. Example : Iriel 8086 X86. 3. Deline Micro - Processon. Ans: हात क्रान्त digital integrated cineuit Capable of executing Program. 4. Unite the differences between Miero Proce ssors & Micho-Controllen. Ans: Miero - Controllen Micro - Processon i. CPU is stand - alone. RAM, i CPU, RAM, ROM, I/O & -limen ROM, I/o, timen and separate are all on a single chip Purpose ii Single PunPose ii. General Typically iii Typically 8/16 bit 32/69 bit ir. High Processing Powers, iv. Low Processing Powers

Callabara Continue of the Cont

2

* Micro - Controller Example - ATMega 32 * Micro - Proosessors Example - Intel, 8086, 8051

and a micro- Controller is a compact integraled Cincuit designed to govern a specific openation

Compiler Anditectione = 43 By base and MicroProcession = 14 - 14 Per - 14 Ast and Hanvand Anchilecture.

Example: ATMega 32, MIPS.

in an embedded agolen

3 Deline Micro-Processon

Assembly Programming Language = 37 370 base 2005.

Microprocessor = 19 type = 10 2161 200 non neumann.

Anchitecture.

Example: Intel 8086 X86.

5. Define Bus

Connects the CPU, memory & the other handware devices on the motherboard.

* The bus is a group of Panallel wines.

Alle nine 2 - les aold information della

* 4 री wine आदा २9=16 है। choice नक्यादन 4

Module 100 Module 2 and applied bus

The devices

the shall be only at all the

and le man 16 to Choice spat

0000 010000 10100 troomer & note experience with the color & memoral input for supput dences

x 69 bit bus Can transfer 8 bytes 6= · 1 byte = 8 bit (and before) and a place = 8x8 pif.

the ward to transfer the addresses of

+ 32 bit bus can transfer 46yles 4 plac = 8x4 pif 1 byte = 8 bit 1.32 billing and along t

acountly & * 16 bit bus can transfer abytes 1 byte = 8 bit byte = 8x2 bit = 16 bit

6. Wreite the types of Bus.

Ans:

There are 3 types bus

a. Additess bus

b. Data bus

Control bus.

a. Address bus:

It is a group of wines that are used to transfer the addresses of Memony on I/o devices.

Plant and the second second b. Data bus: It is used to transfer data within microprocesson & memony input on output devices.

y 64 bit bus can -kanslen 8 byles

C. Control bus: MienoProce sson uses Control bus to Process data, that is what to do with the selected memory location.

* Micro - Processor Ter Up - F Thicks denote to all - px. * Dala bus bidinectional

* Address bus unidirectional

* Address sare Dala bus - - - - mileto - Too - आखि , - अहे Solid Line - मिल्स draw कार्या करेंगे.

* Control bus = - MATUI WATER bit OFF - thin line - मिल्स doaw क्या क्या

* Control bus bidinectional

* Control bus 7 -1 BA fagra Control - 21648

a. MINTE => Memory Write Control
b. MRDE => Memory Read Control

C. 20 WC => I'mput Output Wheite Control

d. Jore => Input Output Read Control.

7. Draw Micro-Computer Structure Ans:

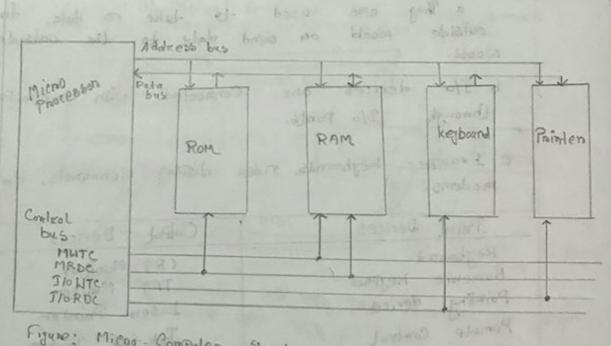


Figure: Micos - Computero Structure Showing different buses

8. Write the Majon Parots of Micro Computer.

Ans:

The major Parols are deland

a . CPU

a. CPU
b. Memoroj
c. I/o cincuitaj
d. Buses. - i. Address bus ii. Dala bus Control bus. 1

9. Wrote note on I/o [Input/output]

Ans:

a. They are used to take in data from outside world on send data to the outside world.

b. I/o derices are Connected with micro-Processon through I/o Porots.

C. Example: keybounds, video display -lenminals, Printers,

Input Devices	Output Devices
Reglocand Numeric Kegrad Pointing derice Pemote Control Jogstick Touch serien Searmore Gircaphics Tablet Microphone Digital Camera Webeans	CRI Monitors TFT Monitors Lasers Prointers Jak jet Prointers Dot Matrix Prointers Speakers Plotters Muttimedia Projectors

10. Write notes on CPU.

Ans:

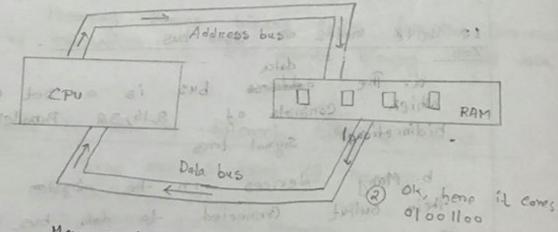
a. It controls the operation of computers.

b. The CPU felches binary coded instructions

C. Decodes the instructions into a senies of Simple actions a color

d. Cannies out these actions in a sequence of Steps of smiles of andrews and

100 1110 110000 100 111110 1100 101



Memory Location ARI PCB THE Location G- FUCHdate à write assit 2001 = 160062 - System Control - Araga Operating System.

* Processon - Com Memory and Registers memory. & Single come Processors to Cache memoral ATR,

11. Write notes on Address bus.

a Address bus is a set of wines

b. It Consists of 16, 20, 29, 32, 00 36

Panallel Unidinectional signal lines.

e. On the lines epu sends out the address of the memory location on Ilo Pont that is to be written to on nead form.

d. The numbers of locations that the court con address is determined by the numbers of address lines.

12. Write notes on Data bus.

a. The address bus is a set of wines which consists of 8,16,32 Panaller bidineeticaal signal lines.

b. Many devices in the System will have their output connected to data bus, but only one device at a time will have it's output enabled.

13. Write moles on Control bus.

a. The control bus is a set of wines which Consists of 4 to 10 Papallel Signal lines.

b. The cpu sends out signals on the Control bus to enable the outputs of addressed memory devices on 1/0 devices.

C. Example of Control signals Memory read, Memory weard, Memory

14. Define Memony

Memony Homes binary codes for the sequence of instructions. It also stones binary coded data. transfer product on stand

16 little the name of different types of memory Ans:

There are 3 types of memory

a-Processon Memony b. Primary on Main Memony

e. Secondary Memory Enomina prompt of

> Processon Memory -> Registers Proimage Memory - RAM, ROM Secondary Memory - + Hard disk

* Volatile Memory => RAM * Non · Volatile Memory = Y ROM

16. Wreile notes on Processors Memory

negisten.

b. Registers are used to had temporary nesults during computation is in Progress.

c. No speed dispanity between hegistens & micro Processon.

17. While notes on Primary Memory

a All Programs une executed. b. MicroProce. Soon can directly access only those items that one stoned in Primary

e. All Programs & data must be within the Proimary memony Proion to execution. d. Example: Rom, RAM

18. Wreite notes on Secondary Memory

Che 3/09

a stones Program & data in access of main

b. Mieno Processon Com not directly execute Programs which are stoned in secondary memory.

c. In order to execute these Programs,
the microprocessor must transfer them to its
main memory by operating system.

the faction of deale to the start to

2. Example: Floppy disk, Hand disk

19. Drouw Micro. Processon interfacing diagram.

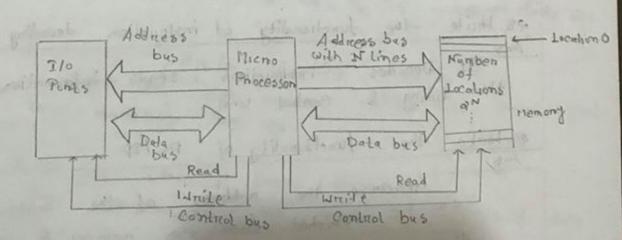


Fig. Micro Processon interlacing with memory & 1/0

20. Write the functionality of ALU.

ALU is an Computational unit. It Personns anithmetic & logic operations.

21. Write the Work Process of Flag Registen.

Various Conditions of the results one stoned as status bits.

Ans:

Internal Storage of data.

is write the Sunctionality of Living & Control unit

Operations of the micro Processon.

It Decodes instructions, sends information to the timing & control unit.

24. Write the functionality of Pe 12P

to be fetched from the memory & send

through address bus to the memory

ogical bit value and the memory

* Logical bit Value offenalion 의 제저 Process
* 8086 대가 → 16 bit Micro- Processon.

Model	Address Bus	Dala Bus
8085	16	8
8086	20	16
8088	20	8

* 8086 - Ga 36 to Pin to data from - 26 data.

- ale 4 to - Fat ager status - care (975),

* Address = Front 20 to - FAR,

HADO - ATS -

00000000000000

The ADO - ADO - ALS -20 Mignito Ao - ALS use - 95.

다 AD Line 가입다 data transmit asgra प्रम 450 - ADO: ADO: ADO: ADO THAT ADORD 15 (15) DO -DO 15 (15) (

The A16/53, A17/64, A18/55, A19/56

THEN multiplex road address bus, status signal

H BHE 157 [Bus High Fnable / Status]
-INT enable data tax most significant half data
bus tra.
BHE; ST GA MICE multiplexed

* MNT/MX [Minimum / Maximum] => gold mode (1 Processor

* Read Pin => 32 number Pin (RD) x Wreite Pin => 29 number pin (WE)

> RD -> Low To active ax MR -> LOW Go active -84.

* TRAIGA SE Operation Total, UR active operation Total inactive - sydala. RD -> Inactive ->2 WR => Active >0

* 8086 tax Execution Unit & Bus Interplace Unit

च यो गी जीवर

Execution Unit

- J. AY LAHTAL
- 2. Bx
- 3. Cx
- 5. Temponany SP [Stack Pointen]
 - 6. 8 BP[Buse Pointer]
 - I. 33 [Sounce Index]
 - 8. DI [Destination Index]
 - 9 Temporarry Registers
 - 10. ALU
 - 11. Flags public \ addition
 - 12. Execution unit Control System.

Bus Interface Unit

- 1. Adden
- 2. C5 [Code Segment]
- 3. DS [Data segment]
 - 4. 55 [Stuck segment]
 - 5. Es [Extra Segment]
- 6. IP [Instruction Pointer]
- 7. Internal Computation Communication Registers
- 8. Bus Control logic
 - 9. Instruction Quele.

Buttile differences between adders & ALU plate but the total date

Adden con add two bits. ALU con Personom runious anithmetic operations.

V Anothmetic Operation -Gaspy noesult change son-

Blurile the features of 8086

Ans:

a. Clock rodes are 5,8,10 MHz b. 16 bit ALU

c. 16 bit data bus

d. 20 bit address bus

=> Execution Unit - capa Bus intendace unit to act Connection - stops 16 bit ALU data bus.

& write differences of Execution unit & Bus interpace unit Execution Unit:

a Executes operation on bytes on 16 bit words b. The nesult is stoned into temp negisters on negisters connected to the internal data bus.

Bus intenface Unit.

- a. Intended to Compute the addresses.
- b. 100 Lemporary registers
- c. foun segment negistens [Ds, cs, ss, Es]
- d Program Counters [IP]
- e. 6 byte Queue buffers.

× 8086 La single Oscillation 4460 3417 → 1 61 Pulse Process 285 16 bit data.

- * Micro Processon Lag memory Costly.
- * 8086 -2- At a lime stil Program Load -24.
 - * 80 286 ca cupyfor negisters 16 bit length.

Ans:

It depends upon number of additess lines in CPU.

Define address Space

Ans:

Set of all Possible addresses that Con

be generaled by epu is called address space.

combba fid og 6

V 8086 - GA address bus as bit, - प्रार्थना किय-२०४१ address line. - भा मिर्प 1 mB memory

* 8086 GRI Memory Size / Capacity and 1 MB

& Calculate the memory size of 8086 MicroProcesson

Address bus = 20 bits
Data bus = 8 bit

Location Marking = 20
= 1048576

Total Memony size = $1048576 \times 8 \text{ bit}$ = 8388608 bit= 8388608 byte [86816]= 1048576 byte= 1048576 byte= 1048576 kB[1646]= 1084 byte= 1084 kB= 1084 kB

to balancina action of attack

Soss Micho Processon

x Address bus : मण्डाका bit, - एण्डाका Combination (विणिता भाग-

The place forestable was

In Calculate the memory size of 8085 microfnocesson

Address bus = 16 bit

Data = 8 bit

Location Marking = 216

= 65536

Total Memony Size = 65536 x8 bit
= 5 24288 bit
= \frac{524288}{8} byte [8 bits = 1 byte]
= 65536 byte
= \frac{65536}{1024} kB [1024 byte = 1kB]
= 64 kB.

8086 Micro Processon

i. Instruction Queue - 211500ii. = 2401140- Processon Supported.

8085 Micro Proceason

i. Instituction Queue Ara
ii. = 440/400 Processon Support vota Ar,

Pamameter 1	8085	
		8086
Size	8 bit Processon	16 bit Processon
Address Bus	16 bits address bus	20 bits address bus
Data Bus	8 bit data bus	16 bit data bus
Memory	64 kB of memony	1 MB of Memony
Instruction	No instruction aneue	It has 6 byte instruction auero.
Pipelining	Pipelining not Supported.	It supports Pipelining anchitecture
110 5	It com address 28=256 I/o Locations	It can address 216=655% I/o Locations
Multiprocessing & upport	No multiprocessing support.	It has multiprocessing support.

HE Write the work of Bos interface unit

Ans

a. It works as the secretary for the Execution

b. It assists the communication between the execution unit & the memory on I/o devices.

C. It transmits address, data, control signals

d. Holds 5 negisters the that stone addresses for memory location.

e. Provides address per relocation.