

Int 0 →

0000	0000
0000	0001
0000	0010
0000	0011
0000	0000

0 → 0H - 3H
 1 → 4H - 7H
 2 → 8H - BH
 3 → CH - FH
 4 → 10H - 13H

Interrupt Vector

- 0-4 are reserved vectors.
 - Some of the vectors are for errors that occur during the execution of software, such as the divide error interrupt.
 - Intel reserves the 5-31 interrupt vectors for the other microprocessor products. The remaining interrupt vectors (32-255) are available for the user.
- | |
|--|
| d. The lower the vector number, the higher the priority. |
|--|
- Interrupt goes to the memory location that is four times the value of the interrupt number.

Math → Calculate the memory address/location for the interrupt INT CH in the interrupt vector table.

Solve!

Given,

INT CH

$$CH \times 4H = 30H$$

Address

33H

32H

31H

30H

CS-H	
CS-L	
IP-H	
IP-L	

i. 0030H & 0031H Location contains IP in the interrupt vector table.

ii. 0032H & 0033H Location contains CS in the interrupt vector table.

Fig: Memory Address/Location for the interrupt INT CH

* 4 address gave - हर एक 4H मिले हुए कड़ी की।
- कारण 4 सब address shift की।

* Physical Address \Rightarrow Interrupt हर first line indicate करे।

Math → Calculate the memory address / location for the interrupt INT 5H in the interrupt vector table.

Ans:

Given

INT 5H

$$5H \times 4H = 14H$$

12H	CS-H
16H	CS-L
15H	IP-H
14H	IP-L

Fig: Memory Address / Location for

the interrupt INT 5H.

i. 0014H & 0015H Contains IP in the interrupt vector table

ii. 0016H & 0017H Location Contains CS in the interrupt vector table

* \Rightarrow Interrupt Active হলে, নতুন CS, নতুন IP,

Main Program এর CS, IP stack এ save করা হবে,

নতুন CS, IP আসবে interrupt এ, ফেরত আসলে, stack এ old value save করে রাখবে।

Micro-Processor দু'টি Mode এ কাজ করে।

a. Real Mode b. Protective Mode.

Q. Write differences between real mode vs Protective mode.

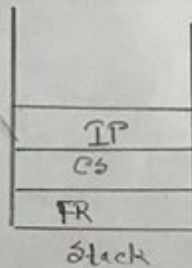
Ans:

Real Mode	Protected Mode
a. Supports Segmentation	a. Supports Segmentation & Paging
b. No Virtual memory support.	b. Support Virtual memory
c. Memory Protection mechanism is not available	c. Memory Protection mechanism is available.

Q. Describe Operation of Real Mode Interrupt

Ans:

- The Contents of the flag registers are pushed onto the stack.
- Both (IF) & (TF) flags are set to 0.
This disables the INTR Pin & the Trap on single step feature.
- The Contents of the Current Code Segment register (CS) are pushed onto the stack.
- The Contents of the Current IP (IP) are pushed onto the stack.
- The interrupt vector Contents are fetched, & then placed into both IP & CS so that the next instruction executes at the interrupt Service Procedure addressed by the interrupt vector.



Stack

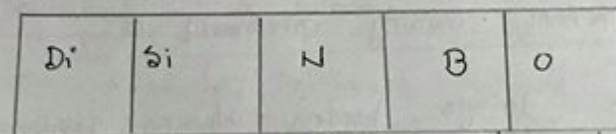
FR → Flag Register
 CS → Code Segment
 IP → Instruction Pointer

Stack → Push register

FR → CS → IP

Stack ← Pop register

IP → CS → FR



Divide By Zero

Single Step

Non Maskable

Break Point

Over Flow

Interrupt Zero:

```

MOV AX, 05
MOV DX, 00
DIV DX

```

Q When interrupt zero occurs?

Ans:

The divide error occurs whenever the result from a division overflows or an attempt is made to divide by zero.

Q What happens during interrupt 0.

Ans:

Three things happen during interrupt 0.

- Flag registers on the stack.
- Reset IF & TF
- Pushes the return address (CS & IP) on stack.
- Gets CS & IP value for the start of the interrupt service procedure from address 0008H & 0000H in the interrupt vector table.

Q When interrupt one occurs?

Ans:

In single step mode a system will stop after it executes its instruction & wait for further direction from the user.

Single-step or trap occurs after the execution of each instruction if the trap (TF) flag bit is set.

Q. What happens during interrupt one.

Ans:

Three things happen.

- Pushes the flag register on the stack.
- Reset IF & TF
- Pushes the return address (CS & IP) on stack.

Get CS & IP value for the start of the interrupt service procedure from address 0006H & 0004H in the interrupt vector table

Q. When interrupt 1 occurs.

Ans:

The non-maskable interrupt occurs when a logic 1 is placed on the NMI input pin to the microprocessor. The input is non-maskable which means that it can not be disabled.

Q. What happens during interrupt two.

Ans:

Three things happen

- Pushes the flag register on the stack.
- Reset IF & TF.
- Pushes the return address (CS & IP) on stack.

Get CS & IP value for the start of the interrupt service procedure from address 000AH & 0008H in the interrupt vector table

Q. Write an example of NMI interrupt.

Ans:

Suppose we have a Pressure sensor on a large system boiler connected to the NMI input. If the Pressure goes above some Preset limit, the sensor will send an interrupt signal to the 8086. Type-2 interrupt service Procedure for this case might turn off the fuel of the boiler, open a Pressure relief valve & sound an alarm.

Q. What's the use of interrupt type 3.

Ans:

The main use of interrupt 3 is to implement a breakpoint function in a system for debugging.

When inserted a breakpoint, the breakpoint features executes all the instructions up to the inserted breakpoint & then stop execution.
--

* INT 3 ; 1 byte instruction.

- 1.
- 2.
- 3.
- 4.
- 5.
- 6.
7. ^{int 3} Mov Ax, Bx

int 3 \Rightarrow debugging

1. Line 6 \Rightarrow line 6 execute হবে, 7 নম্বর line-4-
break point set. তাৎক্ষণিক, wait করবে,

Mov
ADD
SUB } \rightarrow OPCode

Q. What happens during interrupt 3.

Ans.

Three things happen

- a. Pushes the flag register on the stack
- b. Reset IF & TF.
- c. Pushes the return address (CS & IP) on stack.

Get the CS value for the start of the interrupt service procedure from address 000EH in interrupt.

And IP value for the start of the procedure from the address 000CH in the interrupt vector table

Interrupt:

INTO [Interrupt If Overflow]

1. Mov AL, 80H
2. ADD AL, 1H
3. INTO, _____
4. JMP Z,
5. SUB AX, CX
6. _____
7. Mov AX, BX
8. _____

INTO
if (OF == 1)
JMP Z

else do nothing

// Overflow flag high set
JMP Z,

Op Code → 2 byte 20H,

* A special one byte instruction (INT 3) that uses this vector to access its interrupt Service Procedure.

* Int 3 ⇒ halt processor wait,

Q When interrupt - 4 occurs?

Ans. The 8086 overflow flag (OF) will be set if the sign result of an arithmetic operation is too large to be represented in the destination register or memory location.

Q. What happens during interrupt 4.

Ans:

Three things happen

- Pushes the flag registers on the stack
- Reset IF & TF.
- Pushes the return address (CS & IP) on stack

Get the CS & IP value for the start of the interrupt service Procedure from address 0018H & 0010H in the interrupt vector table.

INT n

INT nH

n = interrupt numbers [0 ~ 255]

The int n instruction calls the interrupt service Procedure that begins at the address represented in vector number n.

INTO :

INTO instruction overflow flag check - if OF = 1 then into instruction Procedure call - save the address interrupt vector type number 4 - save - etc.

* INTO Software debugging & test.

IRET:

The interrupt service instruction (IRET) is used only with software or hardware interrupt service Procedure.

Q Write the work of IRET.

Ans.

IRET does three things.

- Pop stack data back into the $\$IP$.
- Pop stack data back into CS
- Pop stack data back into the flag registers.

Q Give an example of Interrupt service Procedure

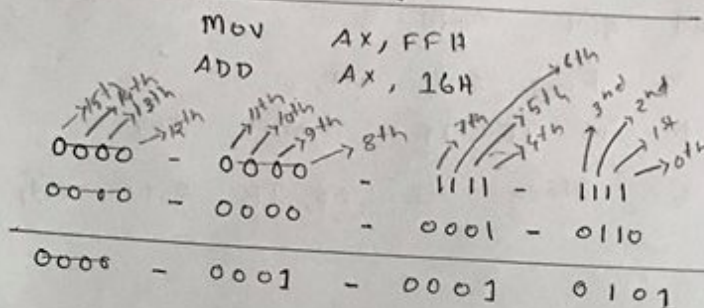
Ans:

```

INTS    PROC    FPR    USES
        ADD     AX, BX
        ADD     AX, BP
        ADD     AX, DI
        ADD     AX, SI
        IRET
INTS    ENDP.
  
```

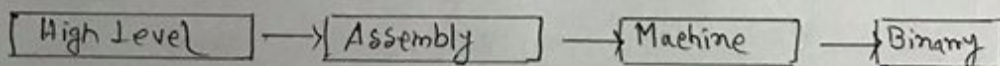

4. Show statuses of flags

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- ZF = 0 [The result is non zero]
 CF = 0 [There is no carry at the MSB (15th bit)]
 AF = 1 [There is carry from 3rd to 4th bit]
 PF = 0 [Odd number of 1's, lower 8 bit]
 SF = 0 [It's a Positive Number]
 OF = 0 [It's within -32768 to 32767. So no overflow]

=> 16 bit का अर्थ PF का अर्थ 8 bit का अर्थ 8 bit का अर्थ 1 का अर्थ 1 का अर्थ



Binary and hex code.

* IRET use કરી આ Return લેવામાં આવે.

* Interrupt બંધ કરવામાં આવે.

a. Flag save કરે,

b. જે TF, IF disable કરે.

c. Stack ની CS, IP save કરે.