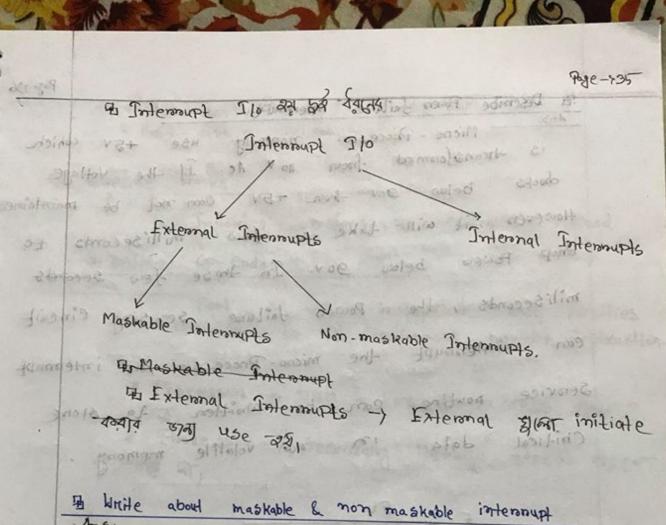
88000000 Page -> 34 Deline intermets. In in-lennupt is used to cause a temporary halt - he execution of Program. * 8086 Microprocesson to intermed Pin onto 30 was the said method for the time Pin 17 => MMI [Non Manable Intermupt] The implication Pin 18 => INTR C DIE NOT 1 Pin 24 => INTA
*NNI Port edge trigg ened inPut. RRRRRRBBBB * INTR and Intermed Request Signal. * JULA ARI and intermet acknowledgement to distribute the threation of BIU # Drogw Micro - Computer Operation timeline Keyboard Internuple Printer Internupt Colonial Ineyboard Symptomy & worker I dota to Thole & memory Internupt Main Brognam Main Prognam Main Rognam Progn Program . first professors white Printer Interrupt funde the standion of Execution smithit Fig: Micro Computer Operation Timeling Showing intermutes b. The exemplian unit executes while next instruction. co ALU of execution and temporary to UIA. a fall and contended losign 2 simpline



I write about maskable & non maskable internut Ans:

There of Therengt The to the

Maskable:

Ar Maskable Internept

enabled on disabled by instructions. Example: Mause-Click

Non maskable

C4 5 =

can not be enabled on disabled by instructions. - Non maskable intermuts

Example: Powers failure intermupt.

* 8086 - Total 256 bil interroupt bronge state ool

1 or eggle complete may aron = 5x10-6 3

eq [

ST.

The Descroibe Powers failure intermupt. - Micro - Processon normally use +54 which is transformed from 110 & Ac. If the voltage drops below 900 - then +50 can not be maintained. However it will take a few milliseconds to Powers below 900. In these few seconds com miliseconds, the Power failure sensing cincuit the micro-Processon An intermupt Service noutine can be written to Chitical data in non volatile memo to stone in non volatile memory

PMC -525

town a stood mastable & many smaller of internation 4.9998 Maskantes 4.9997 Mastrable ist mounts con be boldens 610 boldocità occurred to the standing to C HOL Non inaskable Non maskable Intensi 6 4 ad for mas consider on disabled by instrumetions. Fil! Pewer Failure Homes

· formight

* 8086 => M #2. 366 John 4 2003 *
5×106 Cycle Second 1 or excle complete - maps ATGT = 5x10-63 = 5 PS

* Information - Promany Memory - I Volable Memory * Hand - disk - Non- tob Volatile

DAD daire of DMB Controller To daile # Deline moke. Ams!

Invoking no elens alo calling a method.

12 Deline Op- Code

Ans:

8010969

Parot of the instruction that specifies the operation to be Pendonmed by the instruction. BALLY - BLO IL DEDIE - 2191

memoral access sid,

1 19 Denta * Processon -> RAM & ROM TO access Tolker

* Processon > Secondary Memory access mago नाख् ना,

> FIGH CE-> BOTH OF E

4 Deline DMA

Ans: DMA is a type of I/o lechnique in which data can be transferned between micro-Competer memory & an external device such as the hand disk, without mieno Processor involvement.

* DMA -> DMA Controller Chip 8237 Jaa14 यग्रीय न्यापिन.



Page + 38 ala DND quive memoral a cress roals rin, - Charat - Stated were and we would be well & memoral access Dra Controllers to trace salist memoral access Big1 DMA Controller -> CPU Go TAGE Peromission GA May, Con solo [Controller] and and memony of RAM.

Memory ala RAM.

Micro-Processon idle - algod AT org - Algod memory - shocesson idle - stange AT OIS

* 8086 (44 Pm 30 646 31 Controllers Ga GAJ. DMA

> ←31 Hold → 30 HLDA

BR -> Request Moiss Can be tempton at between mir

menung & on extende donce such as

formarjouri

hand disk, without milero Traceresson

A DIES - BRID CONTROLLED

明年前日 A Drogo Programmed I/o transfer diagram DMA Ansi. CPU Stalem Bus Memory 1/0 Fig. Programmed 110 Transfer 45 Draw DMP diagram. -Hans-Jen Anti DMA Controller CPU System Bus Memory 1/0

Fig: DMA Transfer



Ano: Draw DMA delay diagrages

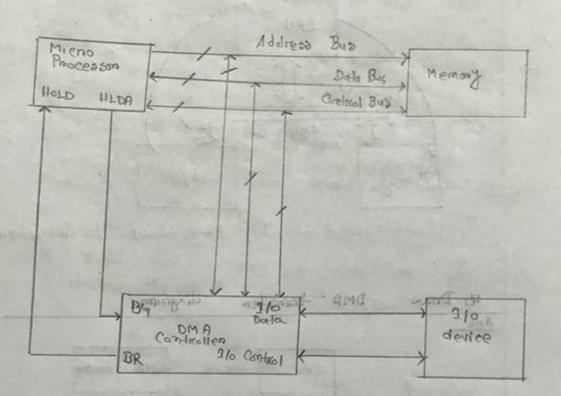


Fig: DMA Controllen Chip 8937

The Describe DMA Operation should

De 3800

a. The Ilo devices heavest oma operation via the DMA negrest: line of the Controllers Chip.

b. The Controller Chip activates microProcesson
HOLD Pin, nequestry the microProcesson to nelease
the bus release

C. The mienoProcession sends HLDA Chold acknowledge) back to the DMA Controller, indicating that the bus is disabled. The DMA Controller Places the memory address of on the address bus & Sends a DMA acknowledgement to the PeriPhenan device.

d. DMA Controller Completes the DMA transfer & release the buses.

* DMA Controller o fact negisten use asta.

=> DMA address register -> Data transfer as only

=> DMA Count negisten -> यळ्याला byte data आधारित

=> DMA control negister - CDU Talgo Command

