✱ Describe DMA operation shortly

Ans:

a. The I/O devices request DMA operation via the DMA request line of the controller chip.

b. The controller chip activates microprocessor HOLD pin, requesting the microprocessor to release the bus.

c. The microprocessor sends HLDA (hold acknowledge) back to the DMA controller, indicating that the bus is disabled. The DMA controller places the memory address on the address bus & sends a DMA acknowledgement to the Peripheral device.

d. DMA controller completes the DMA transfer & release the buses.

✱ DMA Controller ৩ ধরনের register use করে.

=> DMA address register → Data transfer এর জন্য memory address রাখে

=> DMA Count register → কয়টুকু byte data আদান-প্রদান হবে তা রাখে,

=> DMA control register → CPU থেকে command receive করে,

* DMA তিনটা mode -এ কাজ করতে পারে.
  (i) Burst
  (ii) Cycle stealing
  (iii) Transparent

Burst → Total file Transfer না হওয়া পর্যন্ত system bus release করবে না।

* Burst -এ faster transfer হয়, কিন্তু micro-Processor -এর জন্য inefficient হয়।
* Burst -এ I/O slow হয়ে যায়।

* Cycle stealing -এর Mode → Data ~~tranf~~ transfer করবে, then bus release করে দিবে।

* Transparent mode →

Q. When Transparent Mode works?

Ans. The DMA Controller only transfers data when the micro-Processor CPU is Performing operations that do not use system buses.

* DMA operation micro-Processor এর জন্য খুব বিরক্তিকর,
* Transparent mode সব থেকে slow.
* Processor -এর জন্য Transparent mode হল সব থেকে ভাল

* Transparent mode হল → System এর জন্য সর্বনাশক ভাল,

Describe Burst mode.

Ans:

An entire block of data is transfemed in one contiguous sequence. Once the DMA controller is granted access to the system buses by the CPU, it transfers all bytes of data in the memory data block before releasing control of the system bues back to the CPU.

- Burst mode use করে থাকে BG, BR.
- Burst mode use করে Program load করা, data files load করা হয় memory তে.
- Cycle Stealing mode viable alternative use করে থাকে,
- Cycle Stealing mode এ BR দিয়ে BG use হয়,
- Cycle Stealing mode এ CPU is not idled.

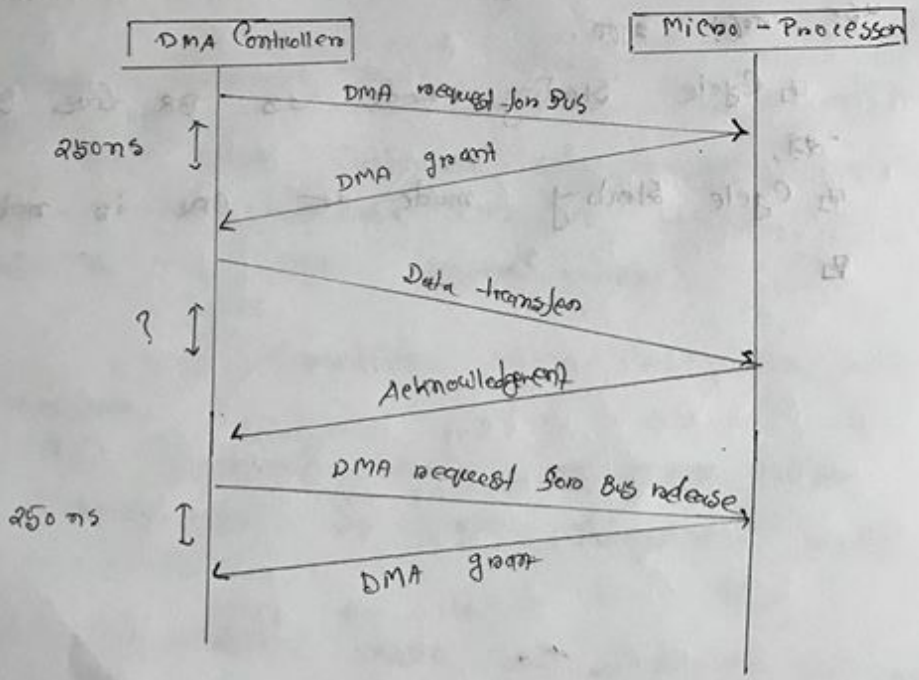
Problem:- Transfer of bus control in either direction, from Processor to device or vice-versa, takes 250ns. One of the IO device has data transfer rate of 15 kB/sec & employs DMA. Data are Data are transferred one byte at a time.

(a) Suppose we employ DMA in a burst mode, How long does it take to transfer a block of 256 bytes.

(b) Calculate the same for cycle stealing mode.

Ans:

(a)



Given

Transfer of bus control from Processor to DMA = 250 ns.

Transferring back bus control from DMA to Processor = 250 ns.

Time taken to transfer 250 Bytes from DMA to memory $= \frac{256}{75 \times 1024}$

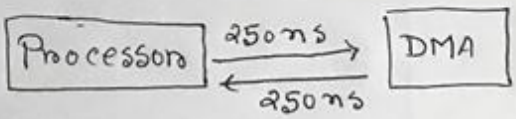
$= \frac{256}{76800}$

$= 3333333.33$ ns

Total = 250 + 3333333.33 + 250

= 3333833.33 ns.

Ans:



(b)

Let

x = Transfer time Processor to DMA [Bus Control]

y = Transfer time of 1 Byte from DMA to memory.

z = Transfer time DMA to Processor [Bus Control]

1 xyz transfers 1 Byte. total time for

1 xyz = 250 ns + 13020.83 + 250 ns.

1 xyz takes total = 13520.83 ns

256 " " " = 13520.83 × 256 ns

= 3461333.33 ns.

13020.83 ns

↘ এর আগে পেয়েছি

75 KB/s data transfer করবে

1 s এ যায় 75 KB

Byte এর হিসেবে 1 s এ যায় $= 75 \times 1024$ Byte

$= 76800$ Byte

76800 Byte যেতে সময় লাগে 1 s

1 Byte যেতে " " $= \frac{1}{76800}$ s

$= 1.3020 \times 10^{-5}$ s

$= 1.3020 \times 10^{-5} \times 10^{-9}$ s

Ans:

Q. Write short description of execution unit

Ans.

a. Execution Unit is a 16-bit arithmetic logic unit.
b. Execution Unit can add, substract, and, or, increment, decrement, Complement. Binary numbers.

c. Execution unit has four 16 bit general Purpose registers, a 16 bit flag register, & a Control unit.

d. Execution unit Contains eight 16 bit registers AX, BX, CX, DX, SP, BP, SI & DI.

e. The general Purpose registers AX, BX, CX, DX can be further divided into two 8 bit registers AH & AL ; BH & BL, & CH & CL, DH & DL.

f. Those registers can store 8 bit or 16 bit data during Program execution.

g. Flag registers have nine flags.

h. Six of those nine flags indicate Condition.

i. Three remaining flags Control Certain operation.

Describe the function of Bus interface unit

Ans:

a. The BIU stores prefetched instruction byte in FIFO registers called queue from memory.

b. Fetching the next instruction while executing the current instruction is referred as the instruction pipeline.

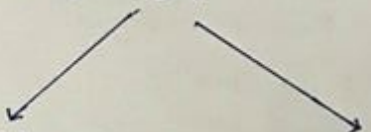
c. BIU has a dedicated adder. It produces 20 bit physical address.

d. Bus control logic unit generates all bus control signals. Example: Read & writes the memory, I/O ports.

e. Four segment registers hold the starting addresses of four memory segments.

f.

Flag Register এর মোট ৩টি



SF → SF = 0 মানে Positive SF=1 মানে negative

ZF → ZF = 0 মানে result non zero, ZF = 1 মানে result zero

CF → CF = 1 মানে Carry আছে, On না থাকলে CF=0

AF → 3 নং বিট থেকে 4 নং বিটে Carry থাকে AF=1 না থাকলে AF=0

PF → জোড় সংখ্যক 1 থাকলে PF=1, বিজোড় সংখ্যক 1 থাকলে PF=0

Even হলে 1's মানে => High
Odd 1's মানে => Low

OF → OF = 1 মানে Overflow হচ্ছে।
Msb 1 মানে overflow তখন OF = 1 হয়।

* দেওয়া আছে
7FH

7F Hexa তে আছে,
Binary তে নিই

0 111 1111

এর সাথে 1 যোগ করি.

```
  0  111  1111
            +1
  ------------
  1000 0000
```

8th 7th 6th 5th 4th 3rd 2nd 1st

```
1  ←0 111   1111
              +1
    -------------
MSB ← 1 000  0000
```

AL = 1000 - 0000 (80H)

CF = 0 [No Carry]

PF = 0 [Odd Number of ones]

AF = 1 [3rd to 4th bit there is Carry]

ZF = 0 [Non zero result]

SF = 1 [Negative Number]

OF = 1 [Overflow]