3lide → Clock Generator 8281

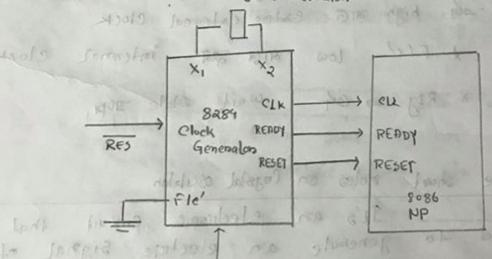
* Clock Signal Chip and 8289

18 White the words of Clock Generator a Reading from memory on Ilo
b. Writing to memory on Ilo

FIRE YAR

Proognammable Persipheral Interspace Clock signal use my AT, distinction and Regulate

Cloth Signal factor space day Py Draw Block diagram of 8289 Clock Constal Ocillaton



Wait State Generator

> Fig. 8284 Block Diagram Interplaced WHY 8086

* RESERT -> Low 60 active 251

* 50 frot Vibrodian 251, Regularo Vibrodian

Clock signal true part and 251,

* Coystal 25 Pieco - Flectrice Modernial

* X1 3 x2 Post Coystal Select infut. The high AGA external Clock

* X1 3 x2 Low and internal clock

RES -> Low to active 231,

X 5 V - Thigh Vibroalism - 231, Regulars Vibroalism

Clock signal - Frequent graphy - days - 221

* Condotal 237 Proper - Electric Material

* Condotal 237 Proper - Electric Material

* F/C' 237 Conjotal Selected Pin.

- 261 high and external clock

* F/C' 1000 AIG 237 internal clock

* F/C' 1000 AIG 237 internal clock

* RDJ => 64 Wait State 2019

Anon It's an electronic cincuit that is used to generale an electrice signal of Proecise frequency

A Wride the advantages of Quartlez Contolal

To see to primary soppe

and much marked top course

ATT THE MENT MENT MENTS (BY)

a Veny Stable signal used in an oscillator b. Low Level of noise for oscillators C. Low cost

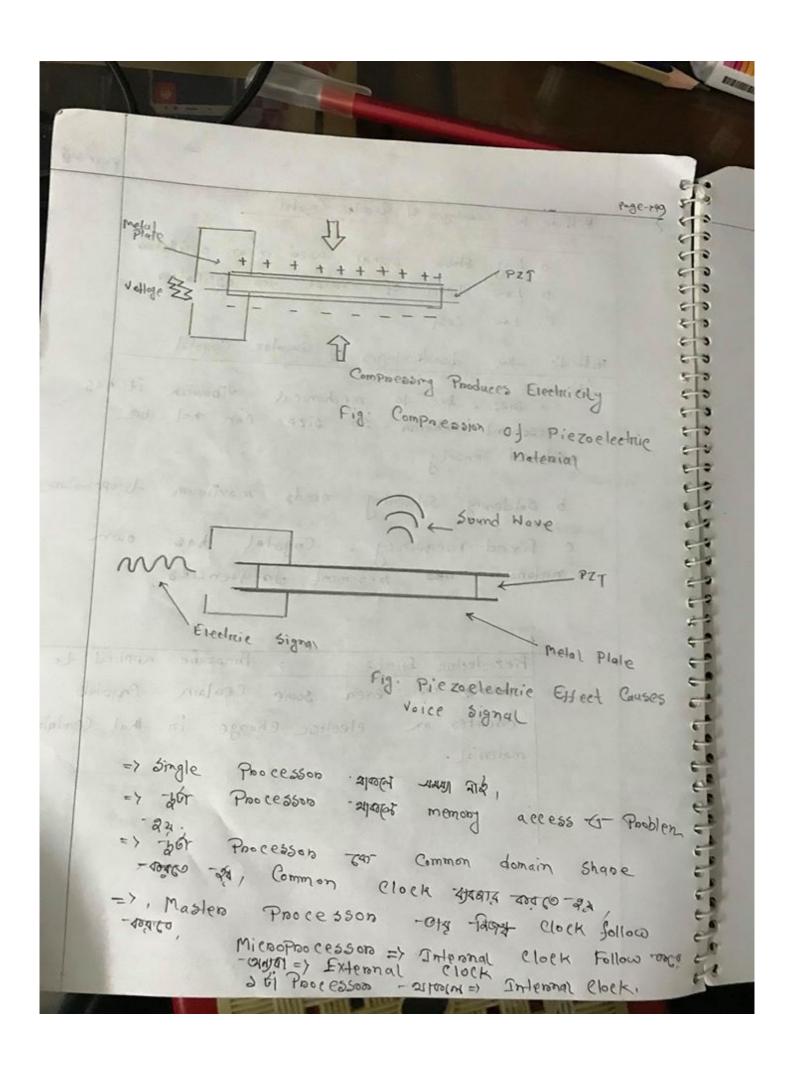
The Write the disadvantages of Quantaz Control

a. Size: Due to mechanical Vibration it has nesonant behavish . so size can not be neduced easily

b. Soldering: Soldering needs maximum temperatures

c. fixed Frequency: (roystal has own natural nes resonant Inequencies.

Prezoelectrice Effect: Pressure applied to quarte on even some Cerolain Crystals croeates an electrice change in that contain material. Fig. Water Idale as 18 parcel of the pr



12 Write the importance of SAP-1

a basic underestanding of how a micro-Processon works, interacts with memory & others Paroto of the System like in Put & outful.

* SAPI BATO design - MOT BIT Academic Purpose

* SAP AM 8 bit anchitecture.

भ 16 x8 memoral आत कर 16 ह। memoral location

* पत निर्वालिय - त्यार्व 5 की instruction.