* SPI → Serial Peripheral Interface
* I_2C → Inter Integrated Circuit

30. Write note on Inter Integrated Circuit.

Ans:

Pronounced eye-two-see or see-on

It's an advanced form of USART. The transmission speeds can be as high as a whopping 400kHz. The I2c bus has two wires. One for clock & the other is the data line.

SPI ত MOSI, MISO, CLK → Common Pin
SS → Unique Pin

I2c ত SCL, SDA → Common Pin

31. Draw I2c Protocol Diagram.

Ans:

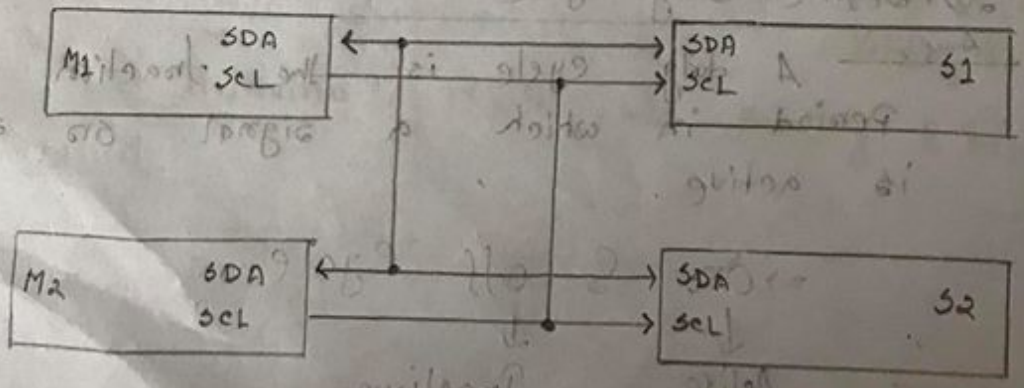


Fig: I_2C Protocol Diagram

32. You are given

$M_1 \longrightarrow S_1$

$M_2 \longrightarrow S_2$

$M_2 \longrightarrow S_3$

Draw I^2C Protocol Diagram with Id.

Ans:

$M_1 \longrightarrow S_1$ (10)

$M_2 \longrightarrow S_2$ (11)

$M_2 \longrightarrow S_3$ (12)

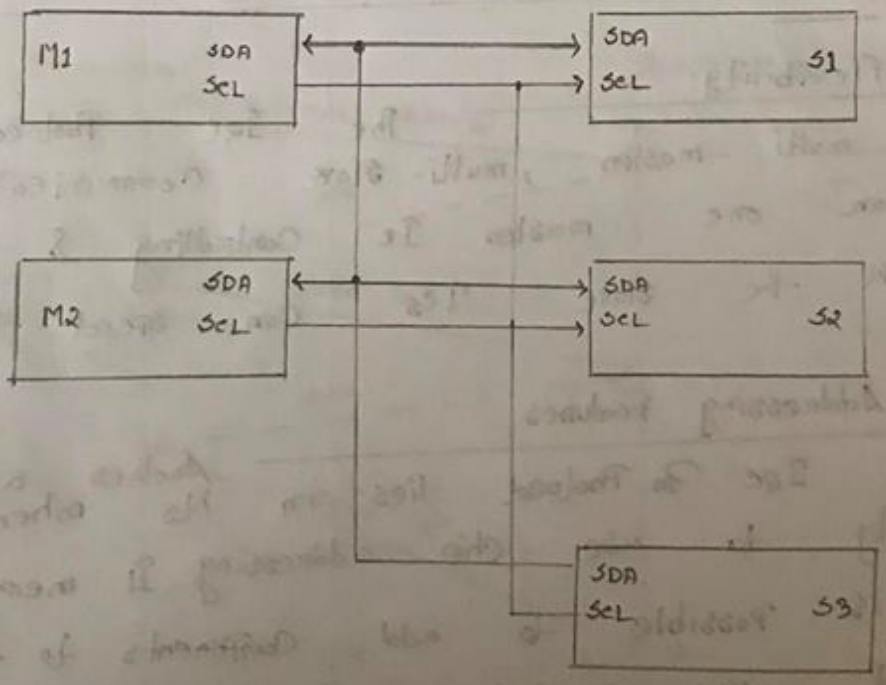


Fig: I^2C Protocol

* SPI তে Master কেন Master?

কারন Master এর কাছে Slave select পিন থাকে, আবার Master এর কাছে Clock signal থাকে,

33. Write the advantages of SPI

Ans:

a. Flexibility:

The I2C Protocol supports multi-master, multi-slave communication. More than one master IC controlling & communicating with the slave ICs can speed things up.

b. Addressing Features:

Another advantages of the I2C Protocol lies in its inherent ability to use chip addressing. It means that it is possible to add components to the bus without any complexity.

C. Simplicity:

I2C Protocol doesn't complicate the design. It requires only two bi-directional signal lines to establish communicating among multiple devices.

34. Draw I²C Protocol sequence diagram (data)

Ans:

START	ADDRESS	W	Ack	DATA	Ack	DATA	Ack	P

Ack → Slave

Fig: Instruction sequence data from master to slave

35. Master (index: 2) wants to send data (Char 'hai') to Slave (index:8). Draw corresponding sequence diagram

Ans:

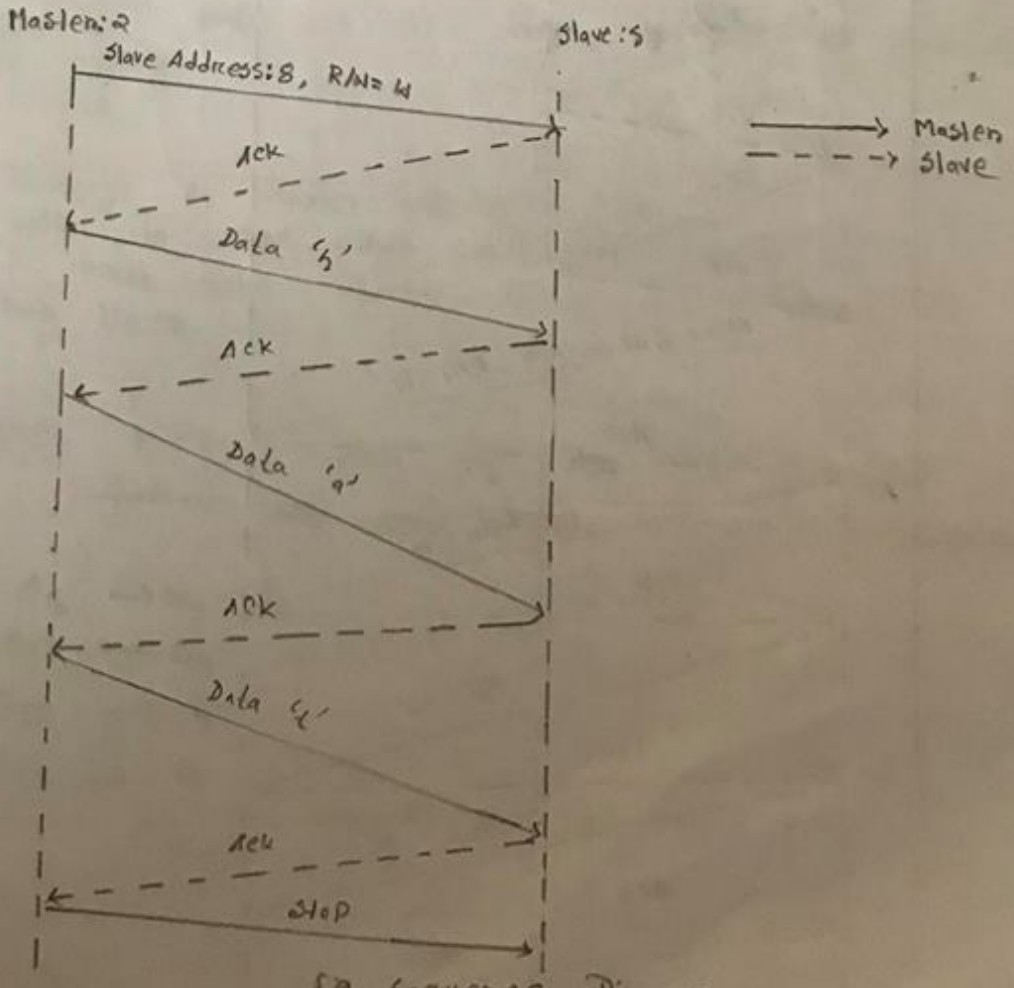


Fig: Sequence Diagram

36. Mast (index:2) wants to send data (char "hat") to slave (index:8) ; (char "Mat") to slave (index:9) ; (char "act") to slave (index:10). Draw the corresponding sequence diagram

Ans.

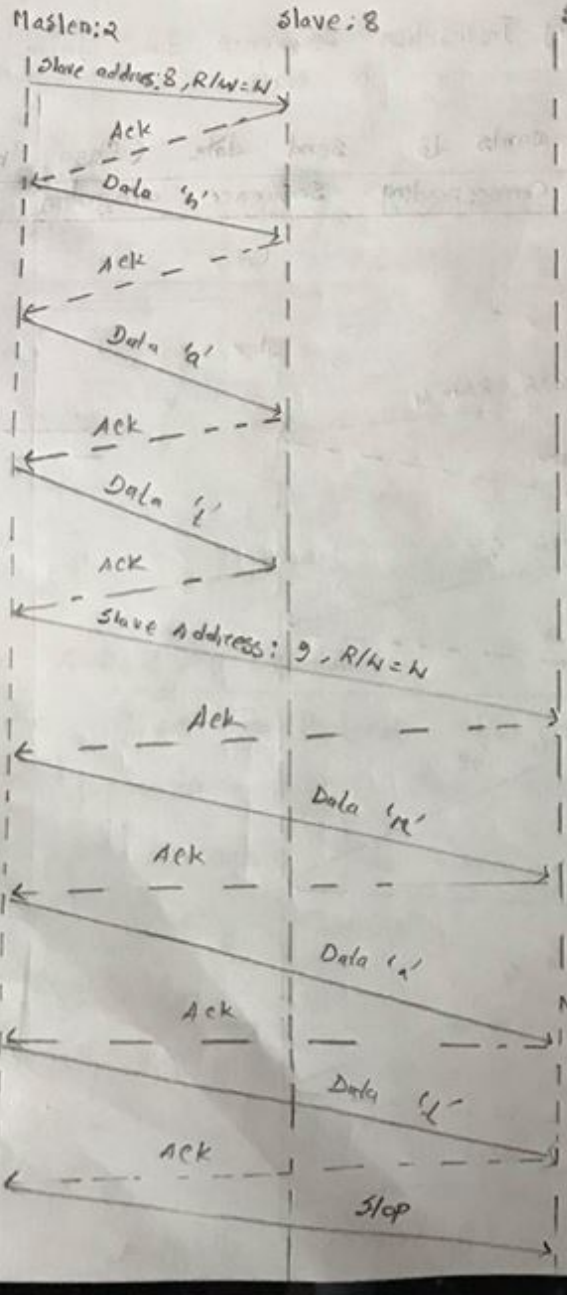


Fig: Sequence Diagram

37. Which Communication Protocol is better for large distributed system. Explain two reasons in two or three sentences.

Ans:

I2c is better. Because the design is simple. There are only two Pins, SDA & SCL. We can interface it easily.

38. Write the advantages of multi master

Ans:

If one master is Corrupted, we still can use the others.

* I2C তে ~~load~~ load ও slave device [with master] সমাধান হয়,

Although the master devices can not talk to each other over the bus & must take turns using the bus lines.

x 8086 Micro Processor -এর AD0 - AD15 Pin গুলো Address এবং data পাঠায়, এগুলো ও Multiplexed.

x A16 → S3
A17 → S4
A18 → S5
A19 → S6

এগুলো হল ৩ bit status Pin.

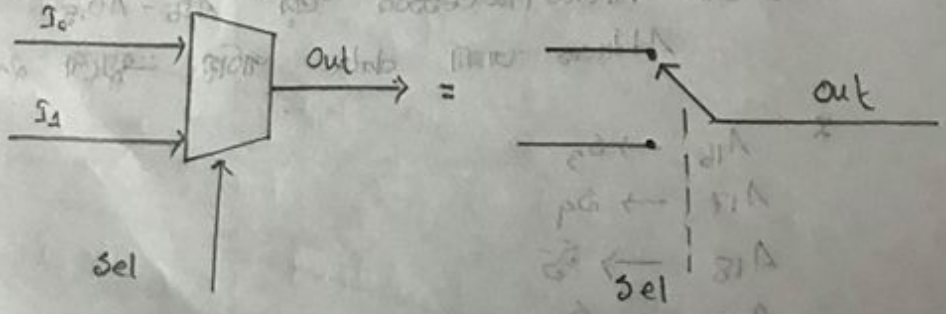
* RD' → Low while reading from memory on Port
* WR' → Low while writing to memory on Port
* ALE → Address latch
* M/IO' → High হলে Memory operation
  Low হলে Data operation

* Pin Description

A_{17}/S_4	A_{16}/S_3	Function
0	0	Extra Segment Access
0	1	Stack Segment Access
1	0	Code Segment Access
1	1	Data Segment Access

39. Draw Multiplexer Diagram

Ans:



Slide → 8086 timing diagram.

40. Why we use timing diagram.

Ans:

It's a graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states.

41. Define instruction Cycle

Ans:

The time required to execute an instruction.

42. Define Machine Cycle

Ans:

The time required to access the memory or input/output devices.

43. Mach Describe Machine Cycle States.

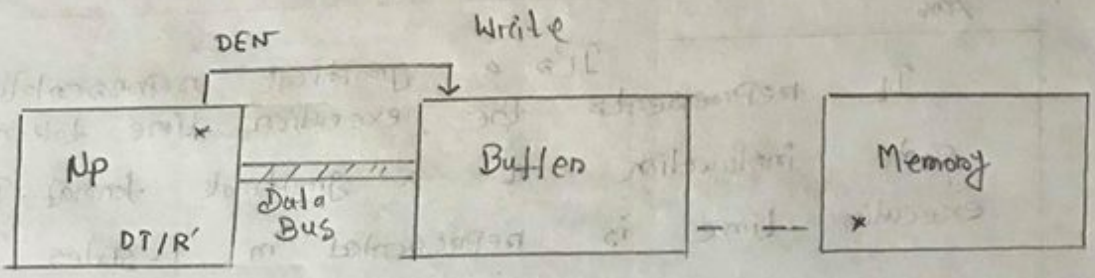
Ans:

T_1: Address is output

T_2: Bus Cycle type [Mem/IO, read/write]

T_3: Data is supplied / Data is received.

T_4: Data latched by CPU, Control signals removed.



MP ⇄ I/O

* DEN মানে = Data Bus Enable [Mainly Databus Buffer Enable]

* Databus activate করলে buffer থেকে memory তে যাবে।

Write Operation এর ধরণ:

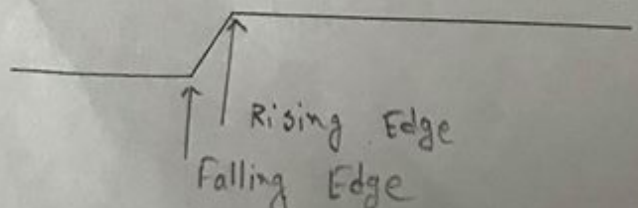
a. Send Address
b. Send data
c. Give Command "Write"

=> 8086 এর Clock rate = 5 MHz
মানে এর একটা Cycle Complete করতে সময় লাগে 0.2 μs.

=> Shutdown মানে high

=> Read মানে Low তে ছিল high হল

=> $\overline{DEN}$ → Buffer to Memory



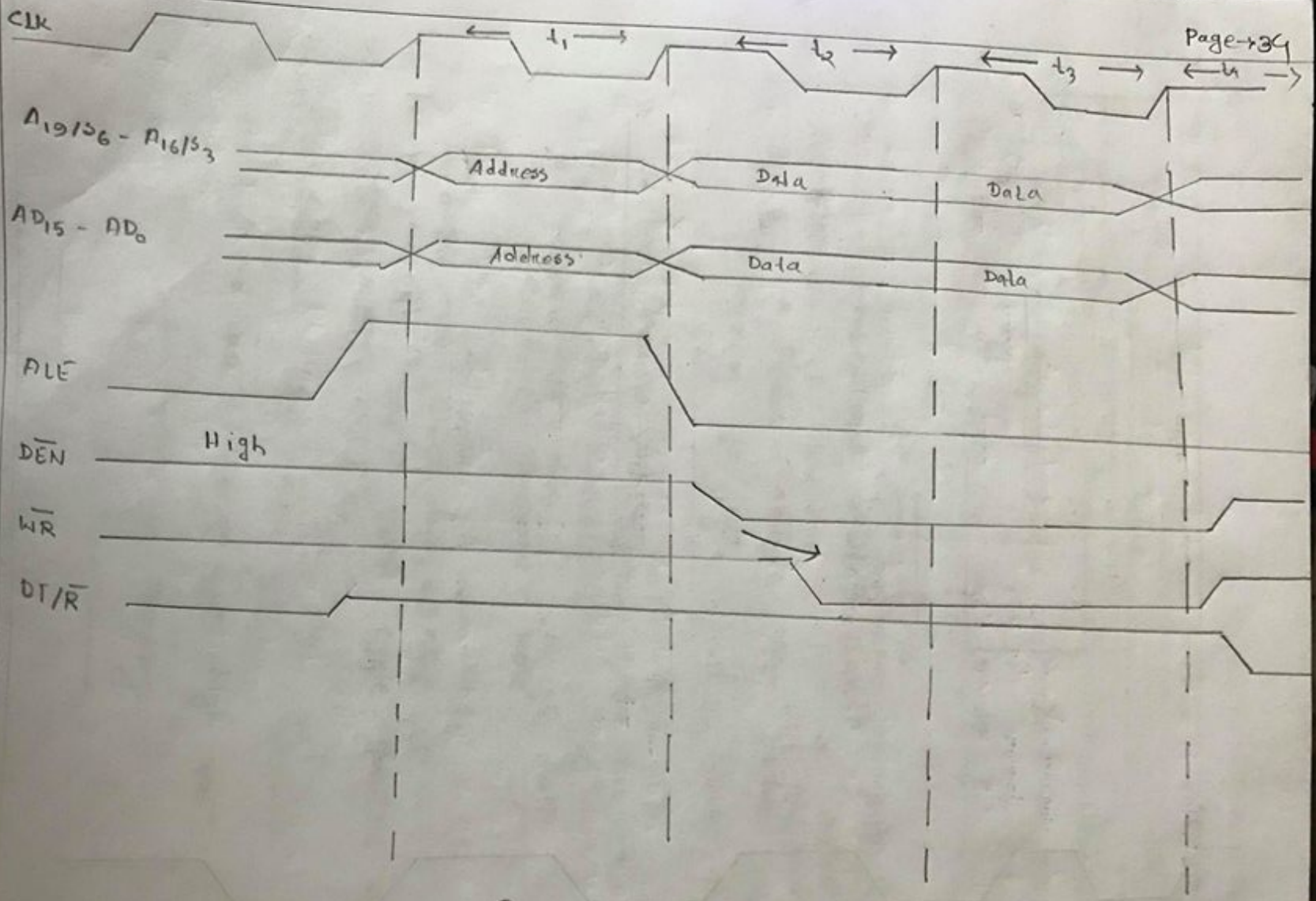


Fig: Bus Timing Diagram for Write Operation

44. Draw Harvard Architecture Block diagram

Ans.

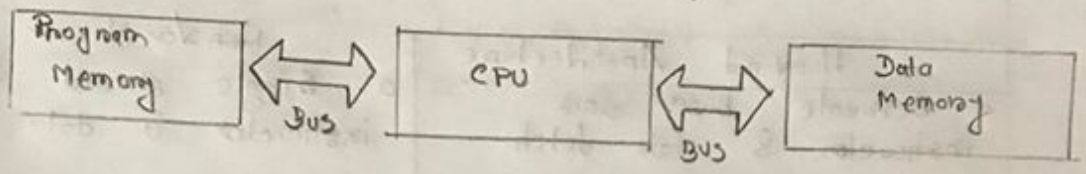


Fig: Harvard Architecture Block Diagram

45. Draw Von Neuman Architecture block diagram

Ans

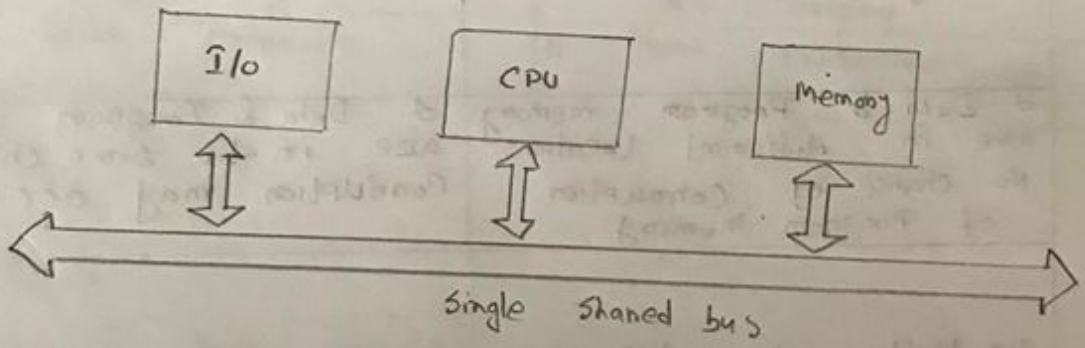


Fig: Von Neuman Architecture Block Diagram

* Harvard Architecture -এর Computer Architecture.
Example: ATMega 32, MIPS.

* Von Neuman -এর Assembly Program -এর জন্য code লাগে।
Example: Intel 8086, x86.

46. Write the differences between Harvard Architecture vs Von Neuman Architecture

Ans:

Harvard Architecture	Non Von Neuman Architecture
a. Separate buses for instruction & data fetch.	a. Single shared bus for instruction & data fetching
b. Easier to Pipeline, so high Performance can be achieved.	b. Low Performance Compared to Harvard Architecture
c. High cost	c. Cheapen.
d. Data & Program memory are in different locations. No chance of corruption of Program memory.	d. Data & Program memory are in the same chip. Corruption may occur.

47. Write the differences between RISC Vs CISC

Ans:

RISC	CISC
a. Instruction Pipelining & increased execution speed	a. No instruction Pipelining feature
b. A large number of registers are available	b. Limited number of general Purpose registers.
c. Single, fixed length instruction	c. Variable length instruction
d. Used with Harvard Architecture.	d. Used with Harvard & Von - neuman architecture

48. What is EEPROM

Ans:

Electrically Erasable Programmable Read Only Memory. It's a type of non volatile memory used in computer.

49. Write the differences between EPROM vs EEPROM

Ans:

EPROM	EEPROM
a. Long time required for erasing	a. Short time required for erasing
b. less expensive	b. More expensive