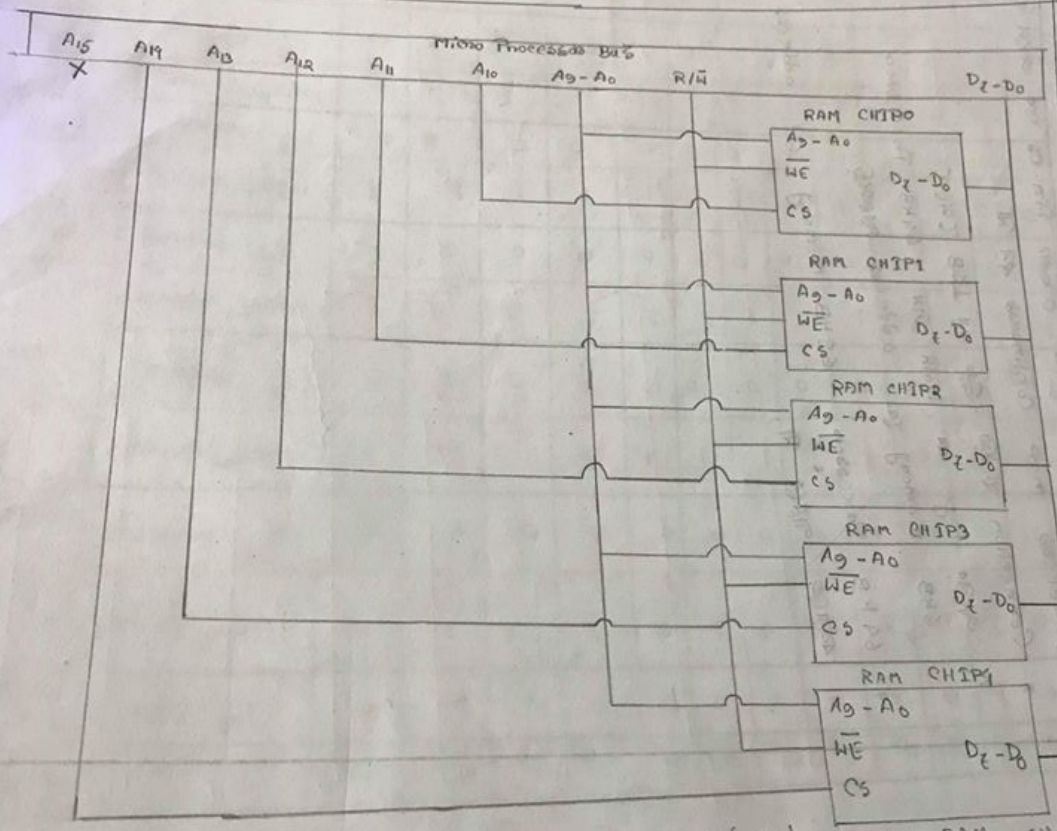


Fig: An 8 bit MicroProcessor interfaced to 8K RAM system

Q) Write the draw back of Linear Decoding

Ans:

a. For 8 bit microprocessor with 16 bit address bus & 8 bit data bus, we have 64KB of RAM memory space.

b. We can't interface with 6KB of RAM memory space where each RAM chip has 10 bit address bus & 8 bit data bus.

c. The address map is not contiguous.

d. If both A_{10} & A_{11} are high at the same time then then a bus conflict occurs.

e. If all unused address lines are not utilized as chip select then total memory size is reduced. It is called memory foldback & it wastes memory space.

* Pin Pin - যদি don't care হয়, তাহলে memory size 6KB থেকে নেমে 5KB হয়, এর ফলে fold back Problem হয়,

Draw the diagram of 8-bit microprocessor with 16 bit address bus interfaced with 9KB RAM using linear decoding method. Each RAM chip has 12 bit address bus and 8 bit data bus. Also provide the corresponding address map for each RAM chip.

Solve:

Given

RAM Chip

Address Bus = 12 bit

Data Bus = 8 bit

Memory Size of a single RAM Chip = $2^{12} \times 8$

$= 4096 \times 8$ bits

$= 32768$ bits

$= \frac{32768}{8}$ bytes

$= 4096$ bytes

$= \frac{4096}{1024}$ KB

$= 4$ KB

Target = 9 KB

Which mean we will need 3 ram chips.

Memory Size/ Capacity of the Processor = $2^{16} \times 8$ bit

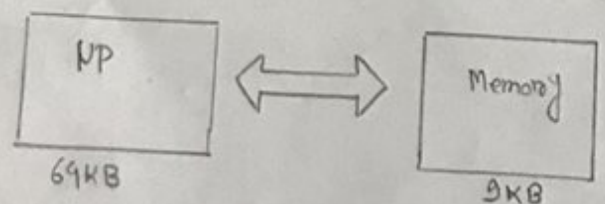
$= 524288$ bit

$= \frac{524288}{8}$ bytes

$= 65536$ bytes

$= \frac{65536}{1024}$ KB

$= 64$ KB



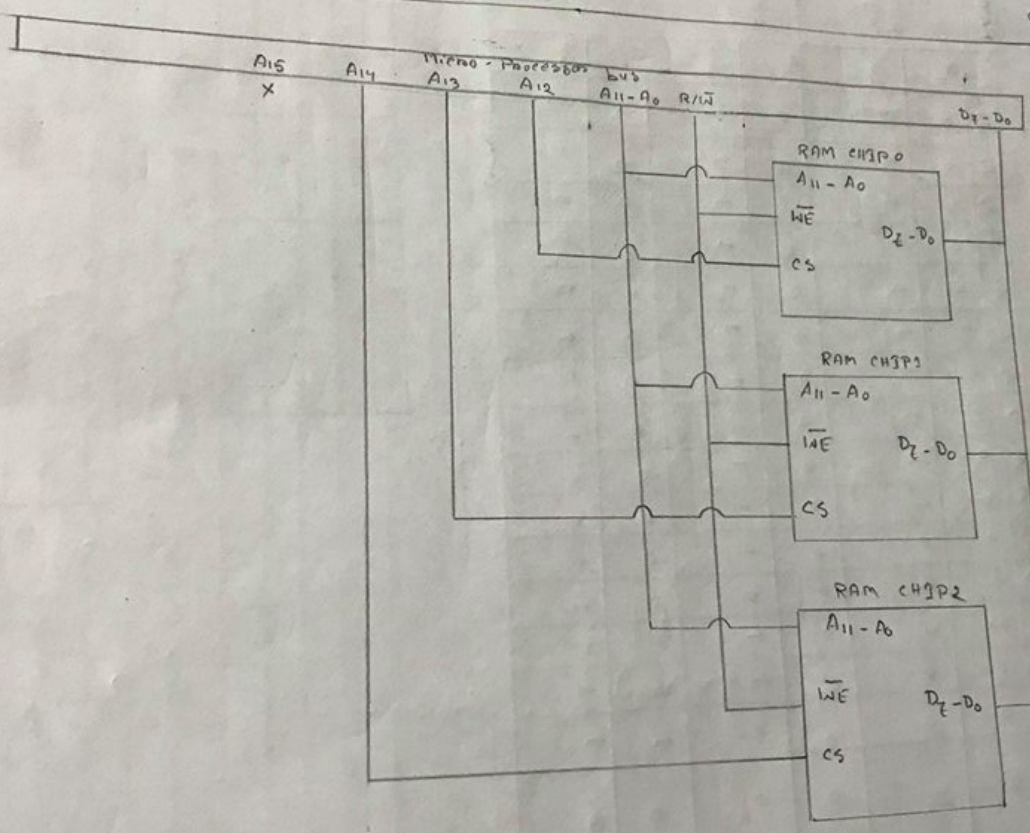


Fig: Micro-Processor interfaced to 9KB RAM

Page 92

* RAM Chip এর Address bus বরাবর বিটের বেস অনুযায়ী A_0 থেকে শিফটিং হবে।

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		RAM CHIP
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1st	RAM CHIP 0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	last	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1st	RAM CHIP 1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	last	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1st	RAM CHIP 2
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	last	

Full Decoding:

→ All of the higher address lines are decoded to select memory chip. The IC chip is selected only for the specified logic levels on these high order address lines.

→ Each memory location has unique address

→ Disadvantages : it needs more hardware for decoding

Decoder Types

i. 2 to 4 decoder
ii. 3 to 8 decoder
iii. 4 to 16 decoder
iv. 5 to 32 decoder
v. 6 to 64 decoder

6 to 64 decoder (max)

AND Gate Truth Table

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND Gate Truth Table

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

* Decoder Low to active হয়,
* 74LS139 এর 2 to 4 Decoder
* RAM chip 0 তে active

Truth Table for 74LS139

G	B	A	Y_0	Y_1	Y_2	Y_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Truth Table For 4 input NAND Gate

A	B	C	D	A.B.C.D
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

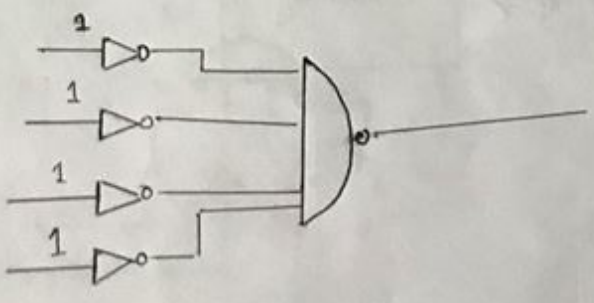
Truth Table For 4 input AND Gate

A	B	C	D	ABCD
0	0	0	0	
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

⇒ AND Gate use করলে, AND gate এগার্ডকে যেতে দিবে।

* 2 to 4 decoder এর জন্য A_{10} এবং A_{11} হল Chip Select.

* A_{15} - A_{12} ⇒ Unused অবস্থিলো সিন হবে 0।



Memory Decoding

Full Decoding

Draw the diagram of an 8-bit microprocessor with 16 bit address bus and 8 bit data bus interfaced to 4KB RAM system using the full decoding method. Each RAM chip has 10 bit address bus and 8 bit data bus. Provide the corresponding address map (starting address and end address) for each RAM chip.

Ans:

Page-07

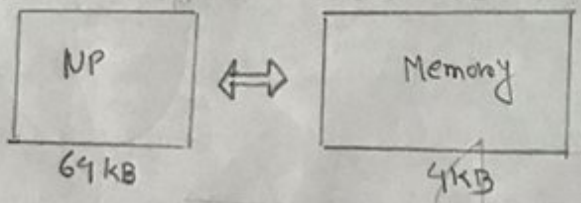
Given,
RAM CHIP
Address Bus = 10 bit
Data Bus = 8 bit

Memory size of a single RAM chip = $2^{10} \times 8$
$= 1024 \times 8$ bits.
$= 8192$ bits
$= \frac{8192}{8}$ bytes
$= 1024$ bytes
$= \frac{1024}{1024}$ KB
$= 1$ KB.

Target = 4 KB.

Which mean we will need 4 ram chips.

Memory Size/Capacity of the Processor = $2^{16} \times 8$ bit
$= 524288$ ~~bytes~~ bits
$= \frac{524288}{8}$ bytes
$= 65536$ bytes
$= \frac{65536}{1024}$ KB
$= 64$ KB



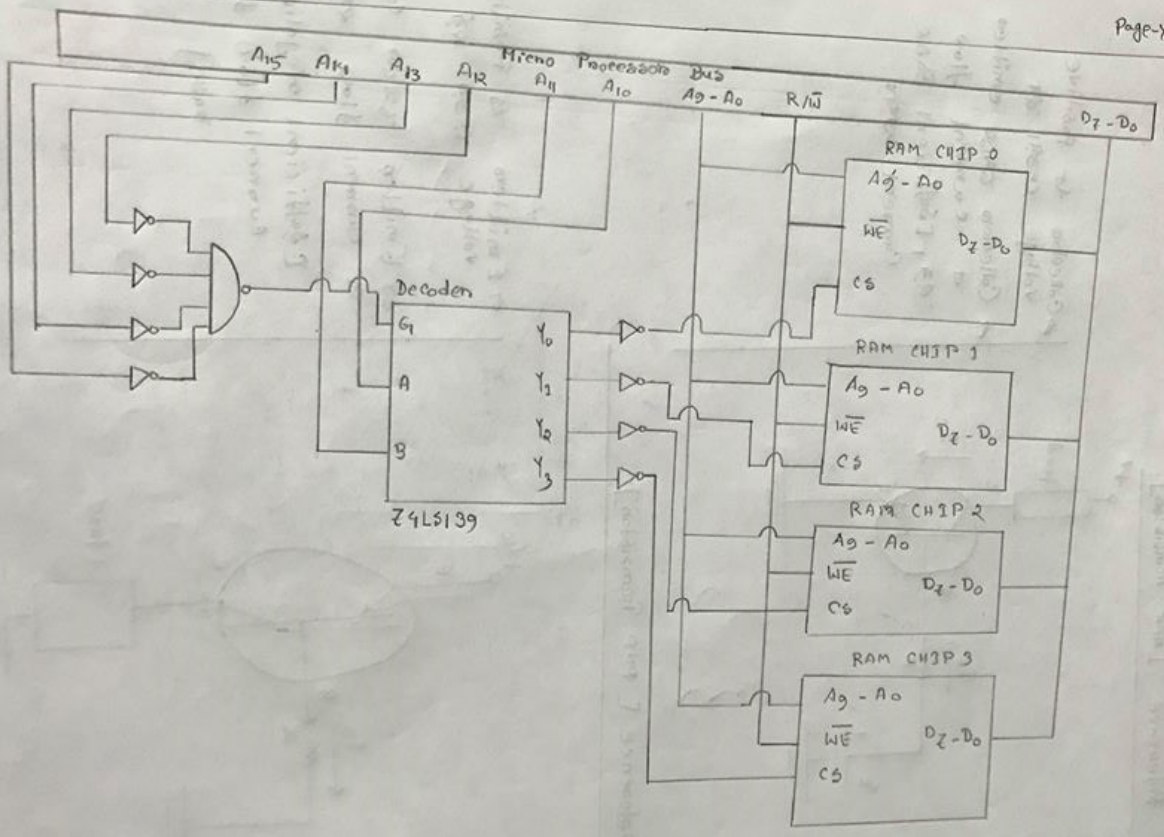
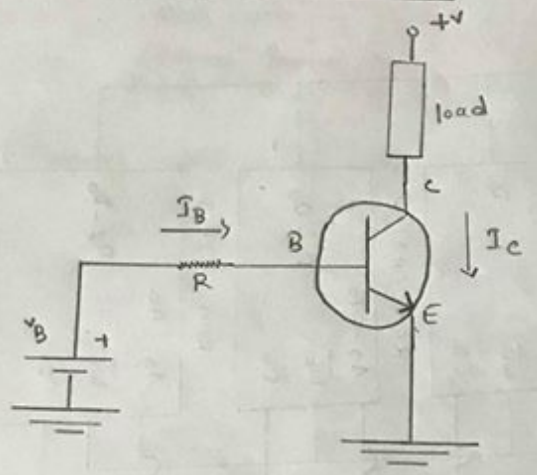


Fig: Full Decoding MicroProcessor interfaced to 4kB

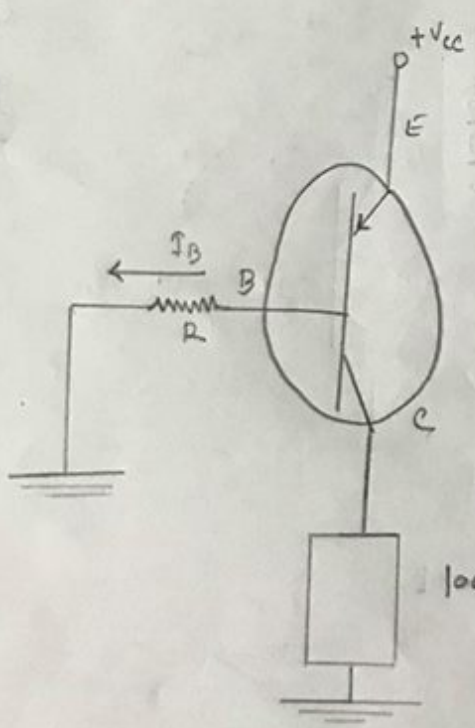
Reference [NPN Transistor]:



→ Collector ↔ Positive voltage দেওয়া হয়

→ Collector থেকে emitter ↔ current flow হয়, [Sufficient Base Current থাকলে।

Reference [PNP Transistor]:



→ Emitter ↔ Positive voltage দেওয়া হয়।

→ Emitter থেকে Collector ↔ current flow হয়, [Sufficient negative current flow from base]