Page-413 Slide + analog - digital 18. Define Senson A senson is an object whose Purpose is to detect events on changes in its environment, & then Provide a Connesponding output. a Suppose a dela a suppose dela Digital Communication Statem rigoro to mitation ind. ADE DAC Complex Treetons Jasolan 319 Mid Digital System . Fit plane , b Micro - Controllen Ndac colombo Palacico 13/2 18 molded Primare

Analog Senson → Theremiston, LDR, Flex

⇒ Digital Senson → PIR Senson, Ultrasenie Senson Page->15 > LDR (Light Dependent Resiston) → Light intensity anget nesistence anger

=> Light Sounce : 754 - 564 - 2160- LDR - (2160-=> 0.76v [VoHage Accross Drop face (732)

22. Desime Pulse Code Modulation Ans:

information signals son electronic data transmission.

=> Pen signal - and senial digital signal

23. Describe Pcm

Ans:

pcm works at 3 steps

a. sampling:

i. Sample is a single measurement of amplitude. in The larger sumpling roate, the betters accuracy of Convension

b. Quartization

the loss of information. The quality of a quantized output depends upon the number of quaralization levels used.

Page-716

ii. The difference between an input & it's quantized value is called quantization

C. Encoding:

level is reprocessed using binary numbers.

x Quantization is neproesenting the sampled values of the amplitude by a simile set of levels.

samples signale son electronic data

* Quantization Innon - Cas Totalet accurate signal

* Anduino - Ga Ao - A5 - 2 A Analog to
Digital

24. Define Quantization Innon

Ano.

Nature l'its quantized value is called a quantization ennon.

=> ADes Can vary greatly between micro-Controller meaning it has the ability to delect 1024 (210) number of discrete levels. Some microControllers have 8-bit ADES (28 = 256 disente levels) & some have 16-bit ADC 5 (a16 = 65535 dischete levels)

=> The ADE neports a ratio-metric value. This means that the ADE assumes 50 is 1023 & anything tess than so will be a ratio between 5v & 1023

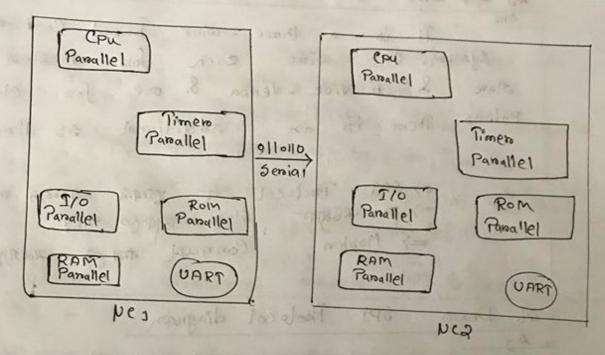
Vollage	Digit Value
5	→ 1023
a.5v	→ 512
2-12 V	→ 439
le over the park and	

ADE reading Resolution of the ADC System Voltage

Page -718 Question. The so bit ADE of the Andrino on a Sv System. If the analog voltage is a py them what will be the ADE report as a value gody (4) mumbers of discocie level Resolution of ADC = ADC Reading System Vollage Analog Vollage Measured => 1023 5.00 × 2.12 => 5.00 x = 1023 x 2.12 => 5.00 x = 2168.76 -> x = 2168.76 → x = 433. 752 => ADC reading fraction allowed of.

-> Ceiling / Aoro Floon Value - Fro area within 0-1 GAZ,

M



* Toogs Panallel

* Trois Senial

-> UART ZA Conventers Prodocol

=> Seroial. begin (3600); and ant seroial Communication

=> R5 232 - Thick Seroial Data Transfer 27.

-> Servial Communication Prootocol STAT got

a. Etheronet

b. USB

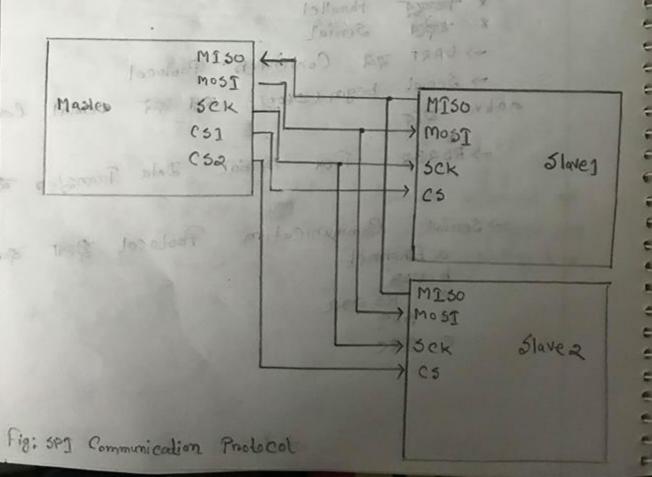
C. R5 232

d. 5PT

e. Tre

Bge-120 6 25. Descroïbe SPI Prodocol Aná It is a three - wine based Communication ayatem. One wine each son master to slave & # Vice - Versa & one for clock Pulses. There is an additional so line. of SPI Prolocal -6- grand = 40.574 master => क लहभीय- श्रायत - भारत आदि । => Massen Connupt or of water,

SPI Proole col diagraph 26. Droaw Ag.



MISO - [Masters In Stave Out] => Stave line Jons Page-721 sending data to the master. MosI -> [Masters Out Slave In] => Masters line for sending data to the Persipherals. sek → [Seroial Clock] => Clock Pulses synchronize data transmission. Jenerated by the master. 35 -> [Slave Select] => Master can use to enable & disable specific devices.

27. Write différences between 5PI 15 Jac Ans:

SPI MAN Tac a Servial Persitheral Interspace a Interpreted Circuit b. sek, moss, miso, ss b. SOR Pins Pins Pins c. Asyr chronous c. Synchronous d. One or more than d. Only one master one masters e. Complex handwane e. simple handware

Page-122

28 Hrite the Advantages & Disadvantages of SPI

Advantage ([] stold to askall] + I wolf

a The neceiver / sender handware can be a simple shift negister.

b. It supposts multiple slave

Disadvanlage 1307 (= 1 159/36 34/37

a. Masters must control all Communications b. Requires separate so lines to each slave.

voltage - aller 1 miles almina Galy ano CHE,

* 16 MH 2 \sim 16 Cycle 5-1

16 X106 Cycle > 15 4-7

16 X106

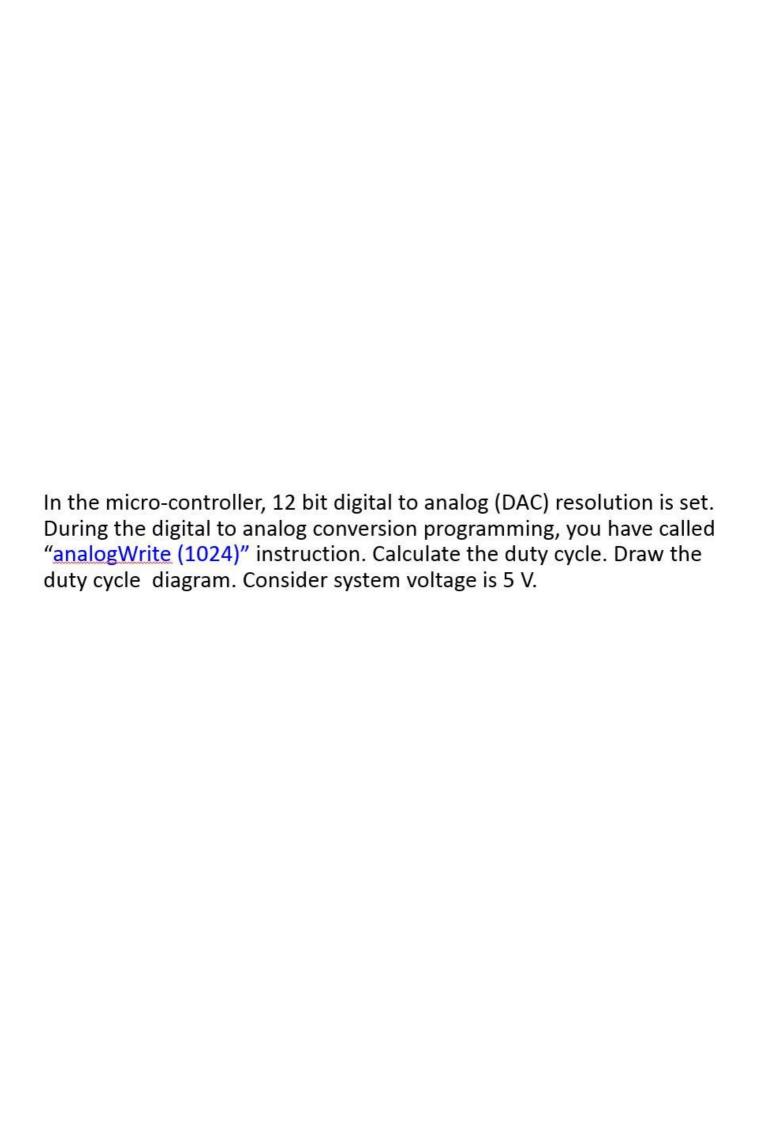
16 X106

□ 16 N5

=> Anduino board - Go Noth -> 10 biz [0-1025]

Analog to digital

=> Anduino digital to Analog 8 bit



Guiren 12 bit digital to Analog 50 212 = 4096

analogibrate (1024)

Fig. Duly Cycle GRAPH

Any: A duly eyele is the traction of one period in which a signal on system is active.

=>000 & o-sf eyele L Adive Inactive