

## HOMEWORK 2

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1- Assume for a particular year that a particular size chip using state-of-the-art technology can contain 1 billion transistors. Assuming Moore's Law (doubling each 18 months) holds, how many transistors will the same size chip be able to contain in ten years?

According to Moore's Law capacity doubling about every 18 months

So ten years  $10 \text{ years} * 12 \text{ months} = 120 \text{ months}$

$120 \text{ months} / 18 \text{ months} = 6.667 \text{ doublings}$

$1 \text{ billion} * 2^{6.667} = 101.617 \text{ billion}$

2- Evaluate the boolean equation  $F = (a \text{ AND } b) \text{ OR } c \text{ OR } d$  for the given values of variables  $a, b, c$  and  $d$ :

a.  $a=1, b=1, c=1, d=0$

$$\begin{aligned} F &= (1 \text{ AND } 1) \text{ OR } 1 \text{ OR } 0 \\ &= 1 \text{ OR } 1 \text{ OR } 0 \\ &= 1 \end{aligned}$$

b.  $a=0, b=1, c=1, d=0$

$$\begin{aligned} F &= (0 \text{ AND } 1) \text{ OR } 1 \text{ OR } 0 \\ &= 0 \text{ OR } 1 \text{ OR } 0 \\ &= 1 \end{aligned}$$

c.  $a=1, b=1, c=0, d=0$

$$\begin{aligned} F &= (1 \text{ AND } 1) \text{ OR } 0 \text{ OR } 0 \\ &= 1 \text{ OR } 0 \text{ OR } 0 \\ &= 1 \end{aligned}$$

d.  $a=1, b=0, c=1, d=1$

$$\begin{aligned} F &= (0 \text{ AND } 0) \text{ OR } 1 \text{ OR } 1 \\ &= 0 \text{ OR } 1 \text{ OR } 1 \\ &= 1 \end{aligned}$$

3- For the function  $F = a + a'b + acd + c'$

a) List all variables

4 variables:  $a, b, c, d$

b) List all literals

7 literals:  $a, a', b, a, c, d, c'$

c) List all product terms

4 product terms:  $a, a'b, acd, c'$

4. Convert the function  $F$  shown in the truth table in the table to an equation. Don't minimize the equation.

a	b	c	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$F = a'b'c + a'bc' + a'bc + ab'c + abc' + abc$$

5. Use algebraic manipulation to minimize the equation in Exercise 4

$$F = a'b'c + a'bc' + a'bc + ab'c + abc' + abc$$

$$F = a'(b'c + bc' + bc) + a(b'c + bc' + bc) \quad (\text{Associative})$$

$$F = (a' + a)(b'c + bc' + bc) \quad (\text{Distributive})$$

$$F = b'c + bc' + bc \quad (\text{Complement})$$

$$F = b'c + b(c' + c) \quad (\text{Associative})$$

$$F = b'c + b \quad (\text{Complement})$$

b. Determine whether the boolean functions  $F = (a+b)' * a$  and  $G = a + b'$  are equivalent

a) Algebraic manipulation

$$F = (a+b)' * a$$

$$F = a'b'a = 0$$

$$G = a + b'$$

$$G = a(b' + b) + b'(a + a')$$

$$G = ab' + ab + ab' + a'b'$$

$$G = a'b' + ab' + ab$$

F and G

are not

equivalent

b. Truth tables

F	a	b	a+b	(a+b)'	(a+b)'a	F
	0	0	0	1	0	0
	0	1	1	0	0	0
	1	0	1	0	0	0
	1	1	1	0	0	0

G	a	b	b'	a+b'	G
	0	0	1	1	1
	0	1	0	0	0
	1	0	1	1	1
	1	1	0	1	1

7. Using the combinational design process, create a 4-bit prime number detector. The circuit has 4 inputs,  $N_3, N_2, N_1$  and  $N_0$  that corresponds 4-bit number ( $N_3$  most significant bit) and one output  $P$  that is 1 when the input is a prime number and that is 0 otherwise.

Step 1: Capture behavior

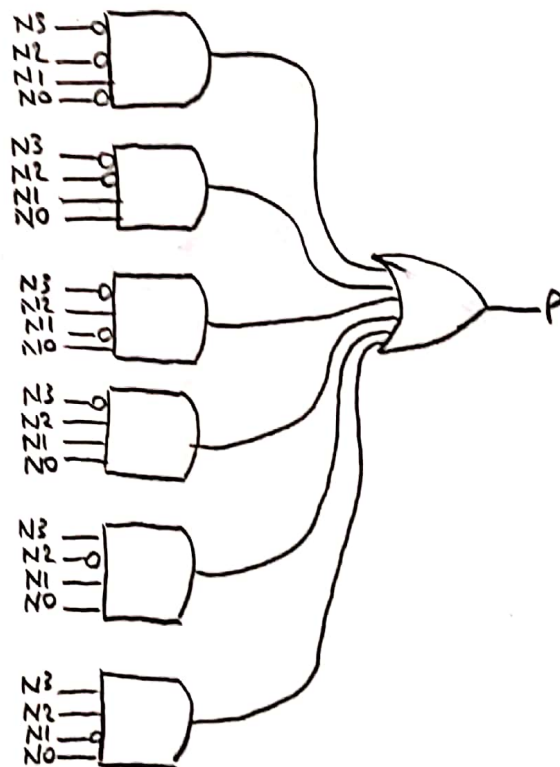
Prime numbers between 0 and 16 are 2, 3, 5, 7, 11 and 13. In these numbers,  $P$  must be 1

$N_3$	$N_2$	$N_1$	$N_0$	$P$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Step 2A: Create equations

$$P = N_3'N_2'N_1N_0' + N_3'N_2'N_1N_0 + N_3'N_2N_1'N_0 + N_3'N_2N_1N_0' + N_3N_2'N_1N_0' + N_3N_2N_1'N_0$$

Step 2B: Implement as a gate-based circuit



8. A network router connects multiple computers together and allows them to send message to each other. If two or more computers send messages simultaneously, the messages "collide" and the messages must be resent. Using the combinational design process 2.5 Table, create a collision detection circuit for a router that connects 4 computers. The circuit has 4 inputs labeled  $M_0$  through  $M_3$  that are 1 when corresponding computer is sending a message and 0 otherwise. The circuit has one output labeled  $C$  that is 1 when a collision is detected and 0 otherwise.

Step 1 - Capture Behavior

$M_3$	$M_2$	$M_1$	$M_0$	$C$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Step 2A - Create an equation

As you can see, there is 15 more than 0s. So we can write an equation that inverse of it

$$C' = M_3 M_2 M_1 M_0 + M_3 M_2 M_1 M_0' + M_3 M_2 M_1' M_0 + M_3 M_2' M_1 M_0 + M_3' M_2 M_1 M_0$$

Step 2B: Implement as a gate-based circuit

