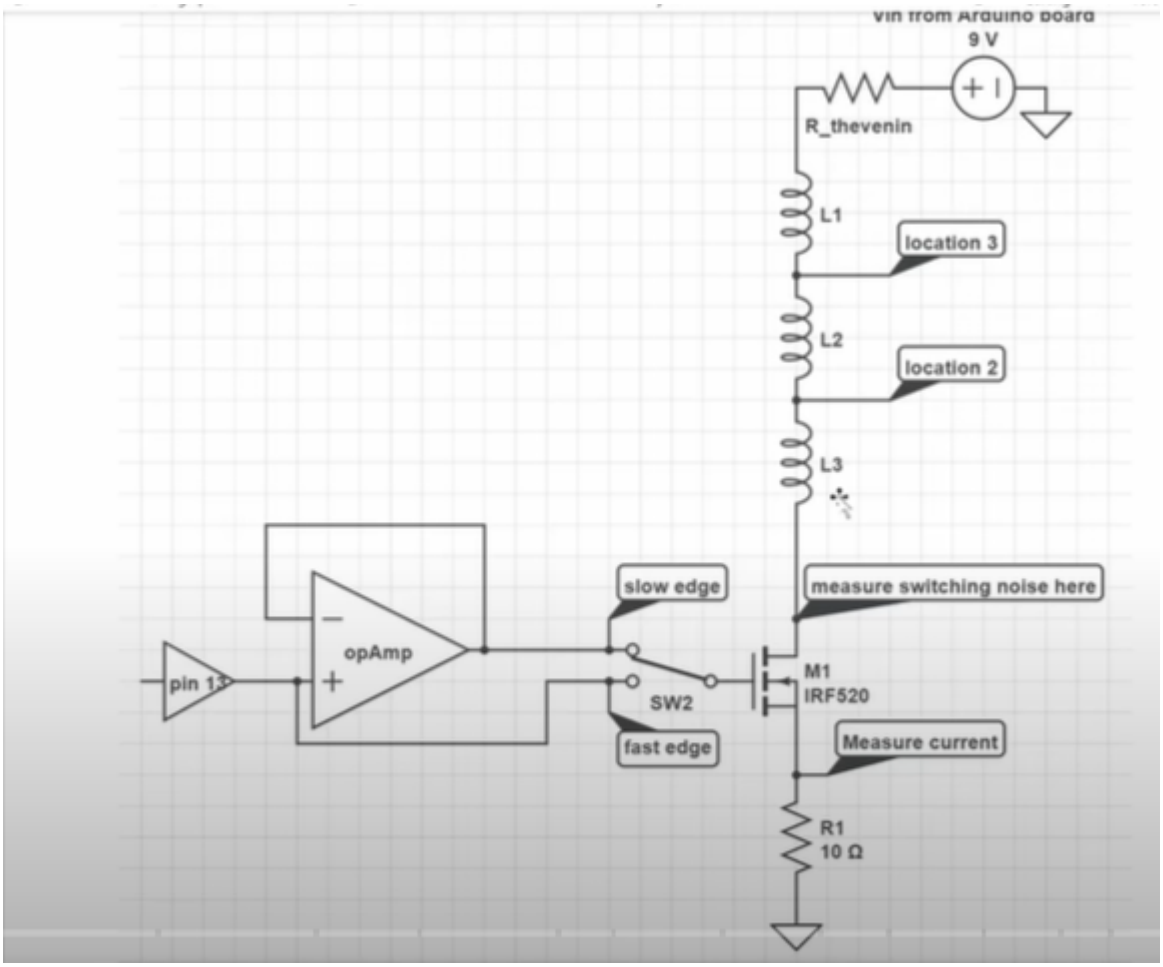
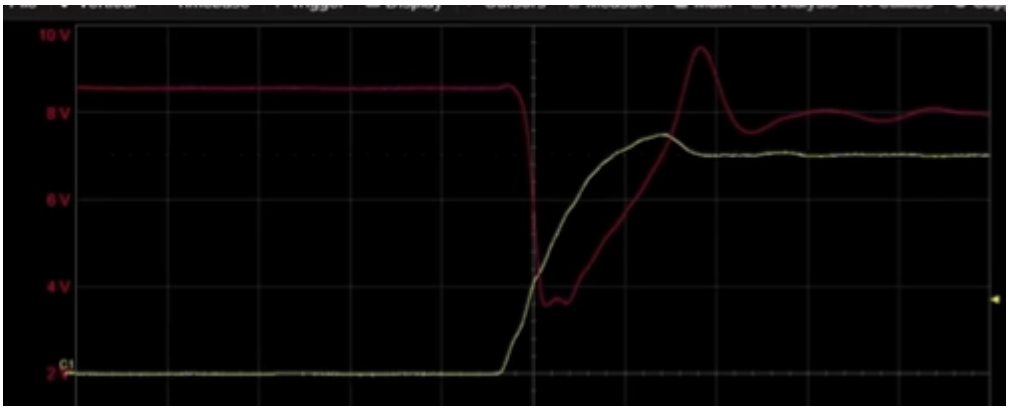
# Decoupling capacitors

It prevents quick changes in the voltage, protecting the system or IC by providing a proper DC supply. The decoupling capacitor is **connected in between the power supply and load/IC in parallel**. To inhibit the voltage disturbances for each IC, they must be placed locally, i.e., as close as possible to the IC.




Pin 13 is a pin from the arduino which is supplying a voltage to switch on the CMOS, an opamp is used in between for greater rise time ie. the rise time of a pin in arduino(from 0 to 5V or whatever voltage) is going to be 2-5 nanoseconds, and when you have an op amp in between the rise time is going to change to 1-10 microseconds, this means the rise time has increased

why care about the rise time?
The voltage in the power rail drops significantlt from 9V to 3.5 V if the rise time is shorter




The red signal is the voltage measured from the power rail and the yellow signal is the voltage measured from the source of the input signal(directly from the arduino pin or from the op amp, in this case we are having the pin13 directly connected to the mosfet gate..)



$$\frac{dV}{dt} = \frac{1}{C} \times I$$

If the current is 0.4 A and the C = 1000 uF, the dV/dt = 400 V/sec or 0.4 V/msec. How does your estimate of the slope of the voltage droop match what you actually measure?

During the time of the rising or falling edge, dt, when there will be inductive switching noise, we want all of the I to come from the capacitor, so none of it has to flow through the rest of the inductance of the power rail. But, this current only has to flow during the rising or falling edge. If we want to limit the voltage drop or droop, during the dt time, to 0.4 V, for example, how much capacitance do we need? Assuming the rise time is 1 usec, the capacitance we need to limit the voltage droop to 0.4 V is:

$$C = \frac{I \times dt}{dV} = \frac{0.4 \times 1u\,sec}{0.4V} = 1uF$$