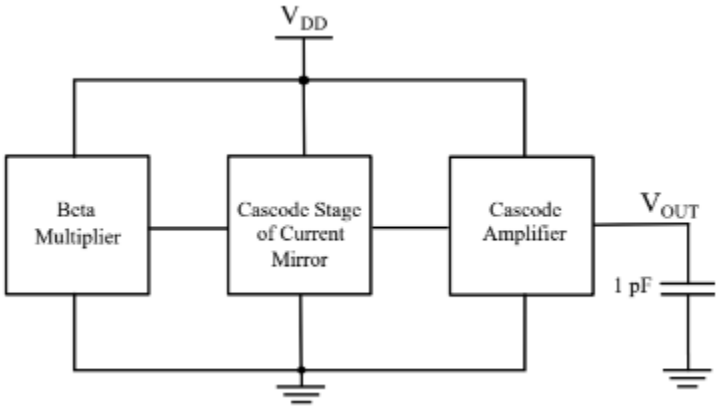
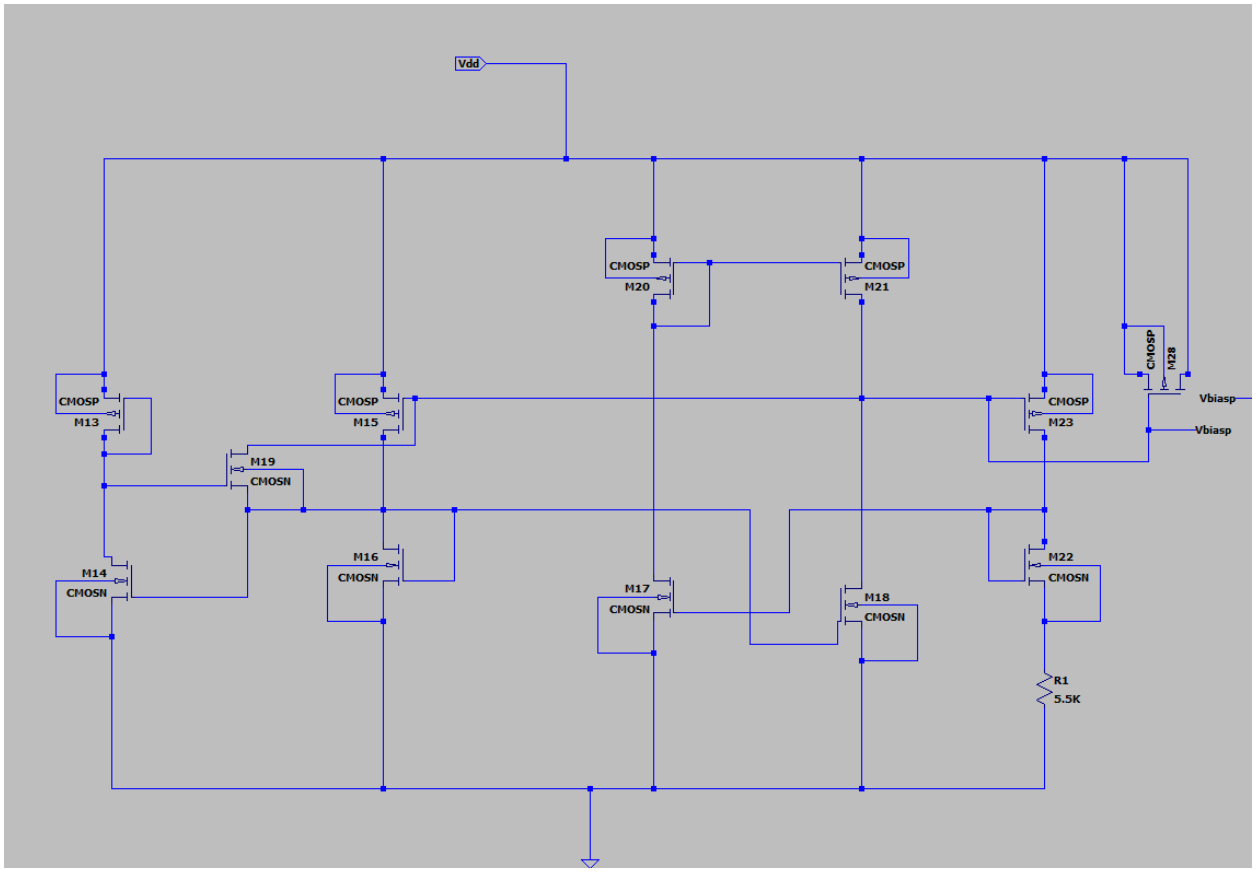
Aim:

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice or Cadence and Magic/Cadence tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

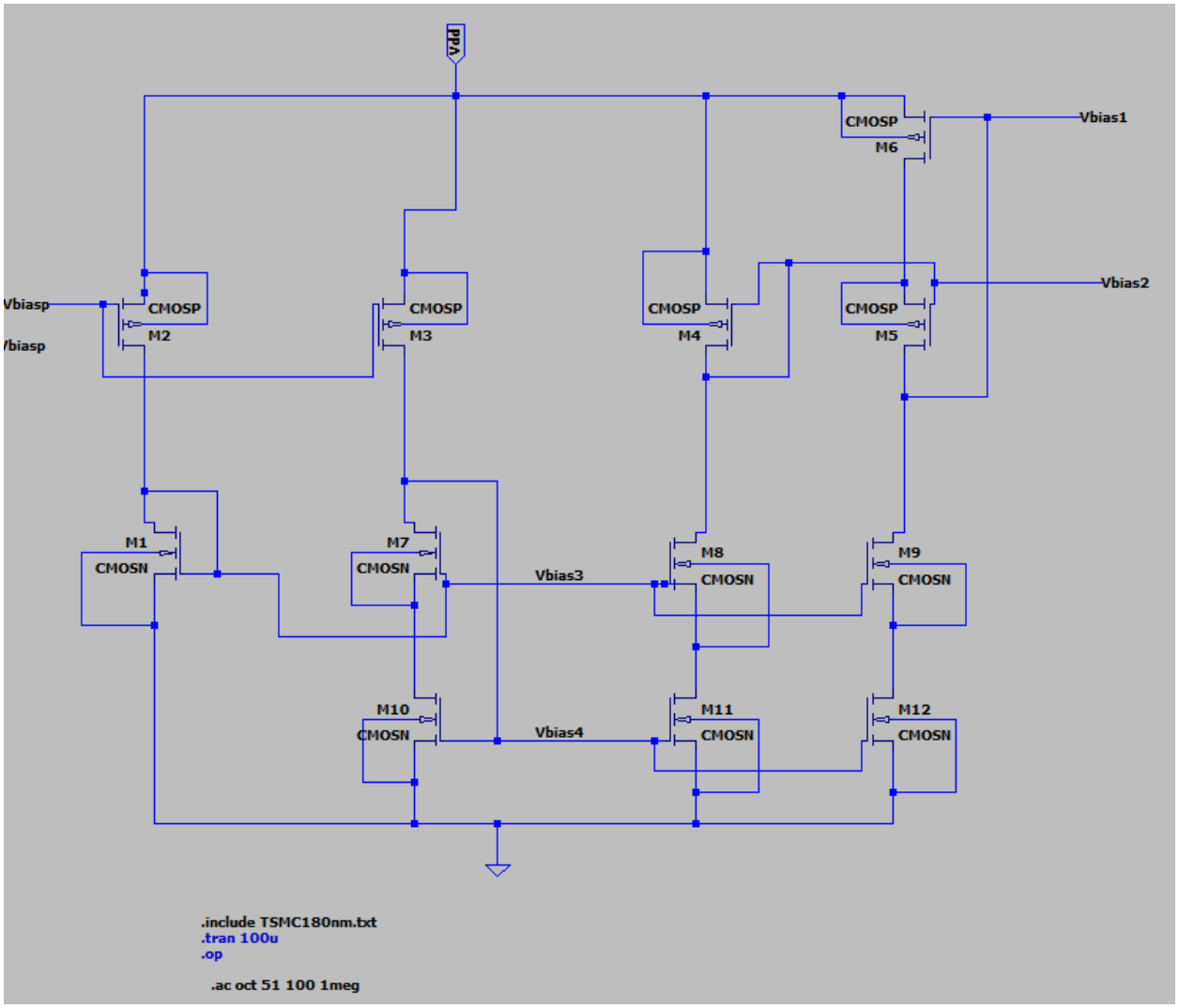
LtSpice Simulation:
The overall block diagram of cascode amplifier with other blocks:



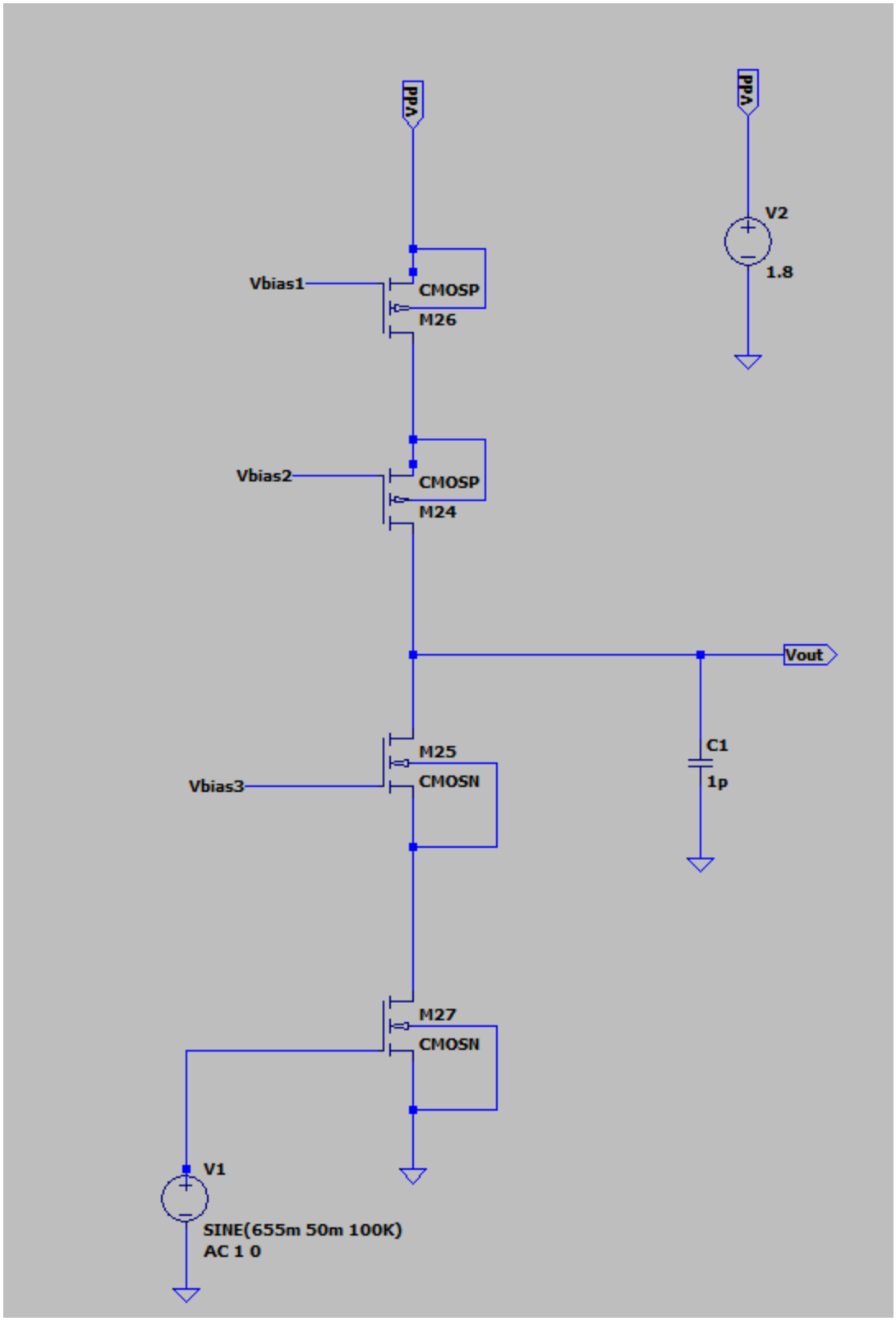
A) 180 nm Technology:
Simulation The following images show circuits made in LtSpice for Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (180nm). W/L were set according to the given values in Beta Multipier and Cascode Current Mirror. For Cascode Amplifier, this ratio was found by calculations shown in next section.



Beta Multiplier



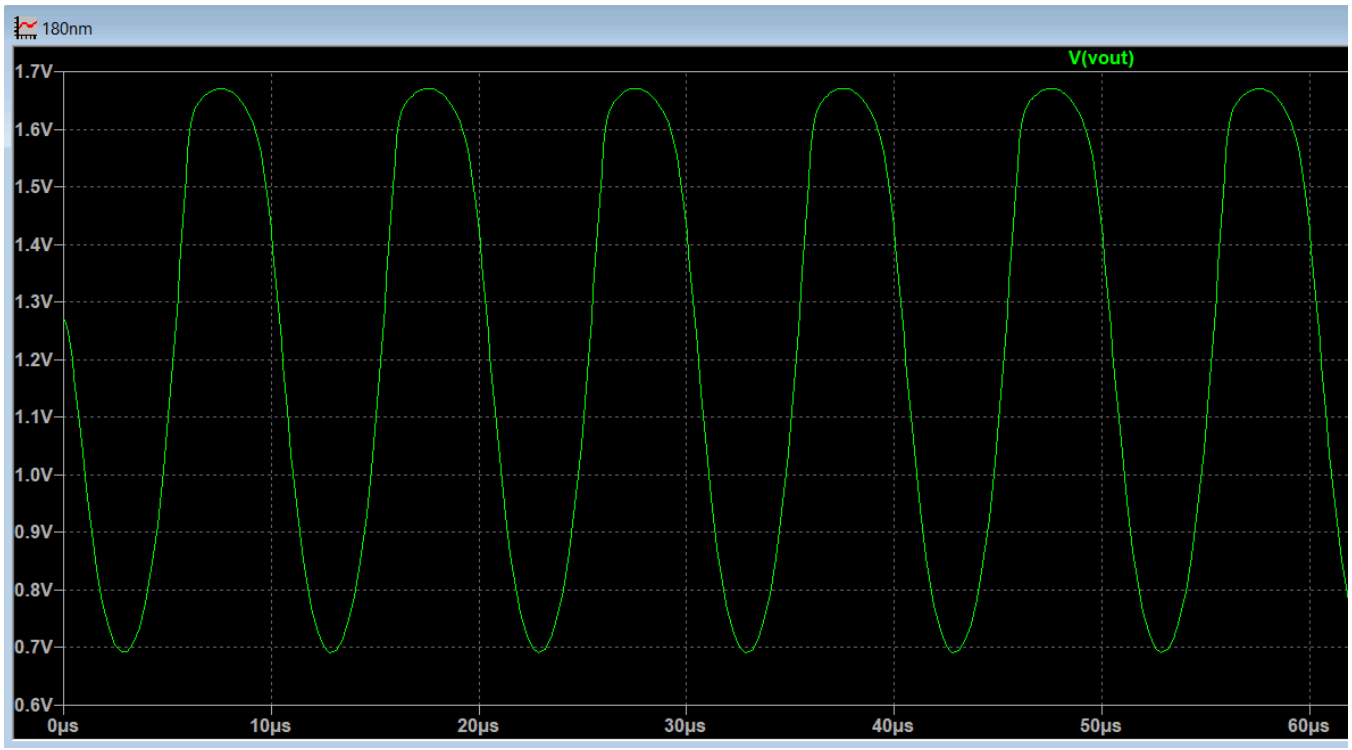
Cascode Current Mirror



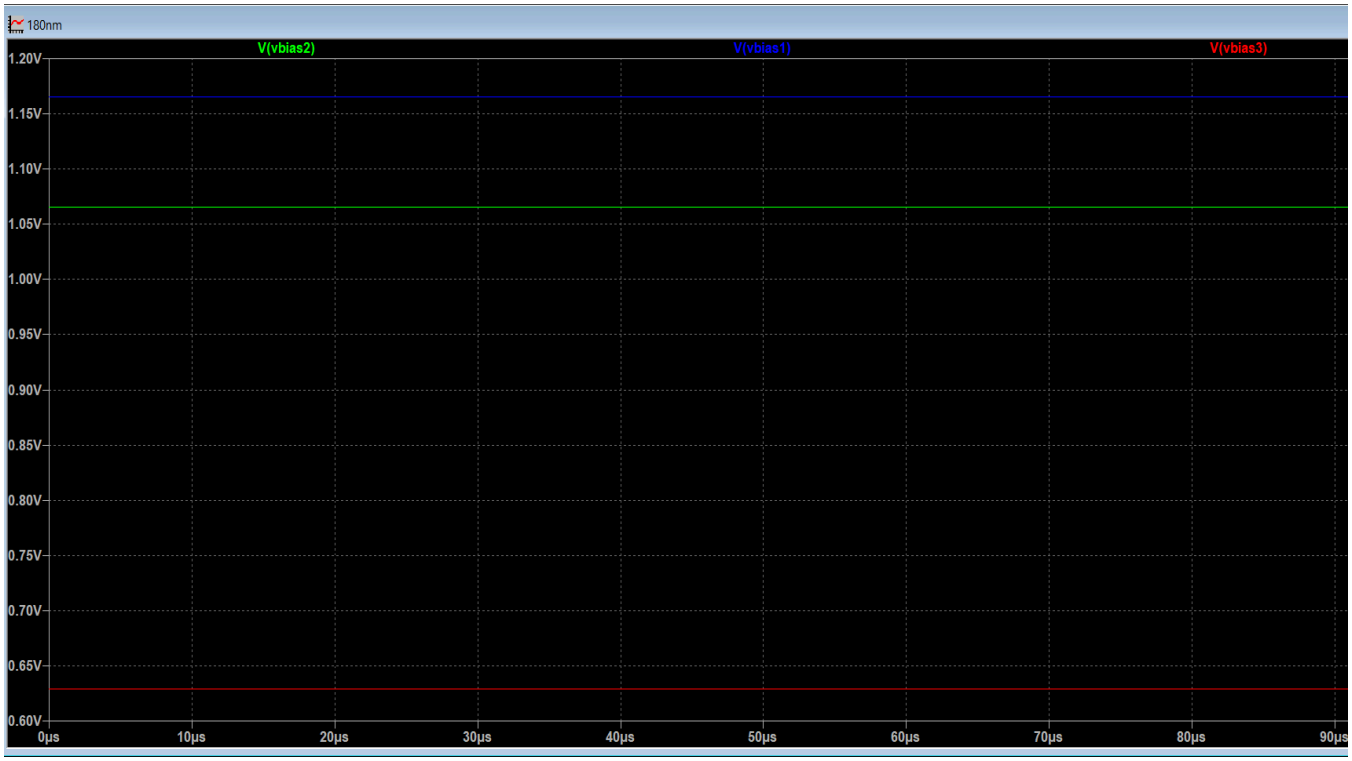
Cascode Amplifier

Output

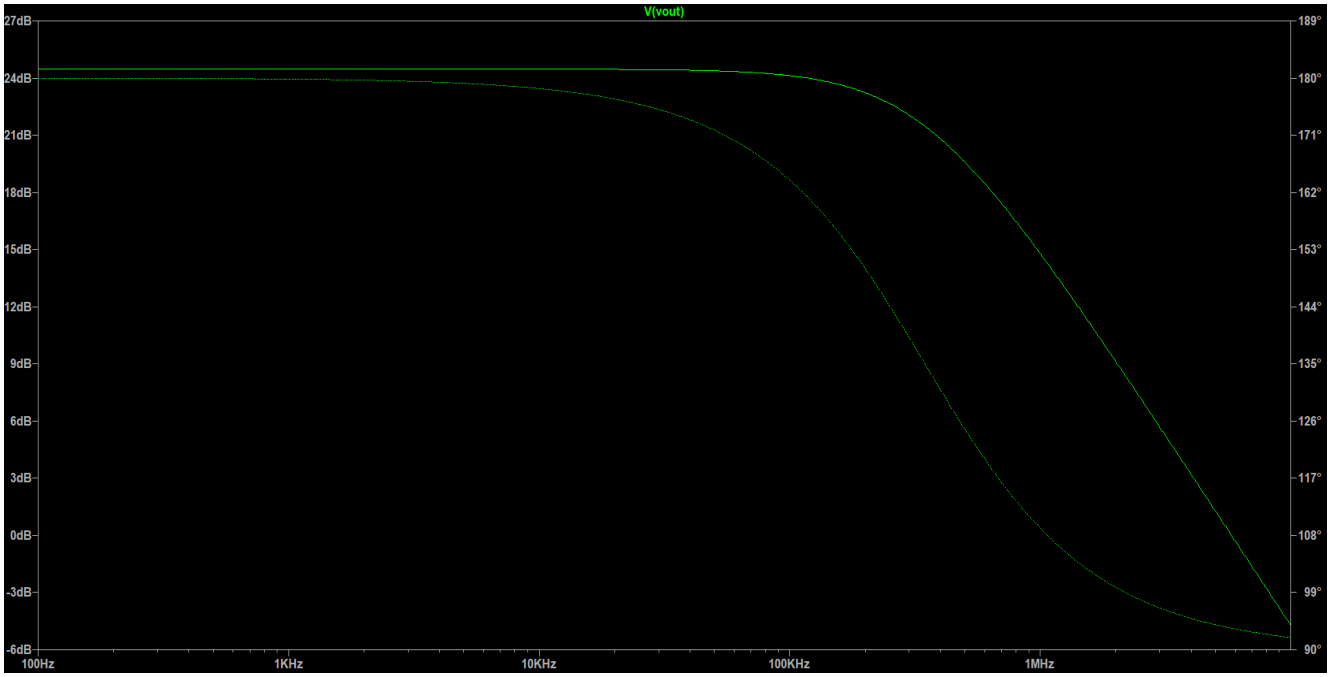
The Simulation outputs obtained were:



Output Waveform



Vbias Values



Frequency Response

Calculations:

For 180nm technology

$A_V = 20\ V/V$

Power Dissipation $< 5mW$

Unity Gain Bandwidth $> 500KHz$

$V_{DD} = 1.8V$, $\lambda = 0.09$

$\frac{1}{2}\mu_n C_{ox} = 175.4\ \mu A/V^2$, $V_{th_n} = 0.50V$

$\frac{1}{2}\mu_p C_{ox} = 35.6\ \mu A/V^2$, $V_{thp} = -0.51V$

Calculations.

Considering the frequency pole location at.

$f_p = 1.5\ MHz$

(Bandwidth $> 500KHz$

We know $R_o = \frac{1}{2\pi f_p C_L}$

$R_o = \frac{1}{2 \times \pi \times 1.5 \times 10^6 \times 10^{-12}}$

$R_o = 106103.29\ \Omega$

Now $|g_m R_o| = Gain = 20.$

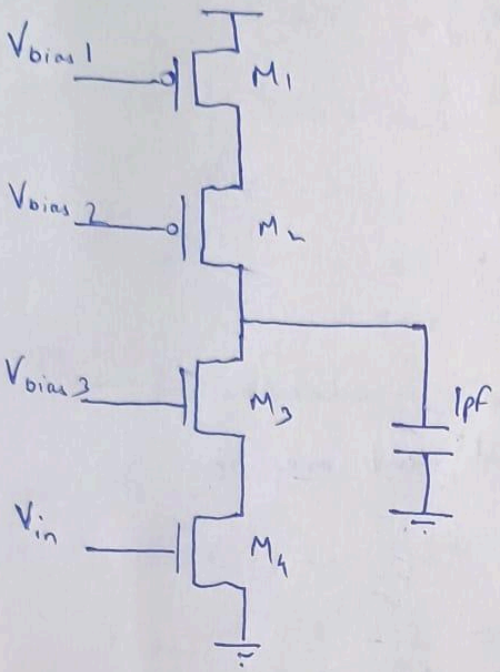
$g_m = \frac{20}{106103.3} = 1.8 \times 10^{-4} S$

- All mosfets are in saturation and same current flows through all of them, and also because the circuit is cascode amplifier.

$V_{DS} = V_{GS} - V_{th} = V_{ov}$

From Industrial standards.

Drop across each MOSFET = 0.2V — (1)



For M_4

$V_{DS} = V_D - V_S = 0.2$ (from 1)

$V_D = 0.2V$

Since MOSFET in saturation

$V_{DS} = V_{GS} - V_{th} = V_{OV}$ — (2)

$V_{GS} = V_{OV} + V_{th}$

$V_G = 0.2 + 0.5$

$= 0.7V$

This is the input biasing cond^n

i.e $V_{GS} \leq 0.7V$

For M_3

Again $V_{DS} = 0.2V = V_{OV}$

$V_D = 0.2 + 0.2 = 0.4V$

From (2)

$V_{GS} = V_{OV} + V_{th}$

$V_G = V_{OV} + V_{th} + V_S$

$= 0.2 + 0.5 + 0.2$

$= 0.9V$

This is the biasing condition for M_3, i.e $V_{bias3} < 0.9V$

Calculating $\frac{W}{L}$

$$g_m = \mu_N C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{th})$$

$$\left(\frac{W}{L}\right)_n = \frac{g_m}{\mu_N C_{ox} (V_{GS} - V_{th})}$$

$$\left(\frac{W}{L}\right)_n = \frac{1.8 \times 10^{-4}}{2 \times 175.4 \times 0.2 \times 10^{-6}}$$

$$\left(\frac{W}{L}\right)_n = 2.6$$

Since all MOSFETs are cascoded and are in saturation,

$$I_{D1} = I_{D2} = I_{D3} = I_{D4}$$

$$I_D = \frac{1}{2} \mu_N C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

$$I_D = \frac{1}{2} \cdot 175.4 \times 10^{-6} \times 2.6 \times (0.2)^2 \times (1 + 0.09 \times 0.2)$$

$$I_D = 18.2416 \times (1 + 0.018)$$

$$I_D = 18.57 \ \mu A$$

Calculating $\left(\frac{W}{L}\right)_p$, for M_3 & M_2

$$\left(\frac{W}{L}\right)_p = \frac{I_D}{\frac{1}{2} \mu_p C_{ox} (V_{GS} - V_{th})^2 \cdot (1 + \lambda V_{DS})}$$

$$\left(\frac{W}{L}\right)_p = \frac{18.57 \ \mu A}{35.6 \ \mu A \times (0.2)^2 \cdot (1 + 0.2 \times 0.09)}$$

$$\left(\frac{W}{L}\right)_p \simeq 13$$

For M_2

$V_S = 1.6V$ & $V_D = 1.4V$

i.e $V_{SD} = 0.2V$

$V_{SG} = V_{SD} + |V_{thp}|$

$V_S - V_{SD} - |V_{thp}| = V_g (= V_{bias\,2})$

$V_{bias\,2} = 1.6 - 0.2 - 0.51$

$= 0.89\,V$ V_{bias}

Thus for saturation, $V_{bias\,2} \geq 0.9\,V$

For M_1

$V_D = 1.6V$, $V_S = 1.8V$

$V_{bias\,1} = 1.8 - 0.2 = 0.5$

$= 1.1V$

For Power Dissipation

$P.D = V_{DD} \times I_D$

$= 18.57 \times 1.8$

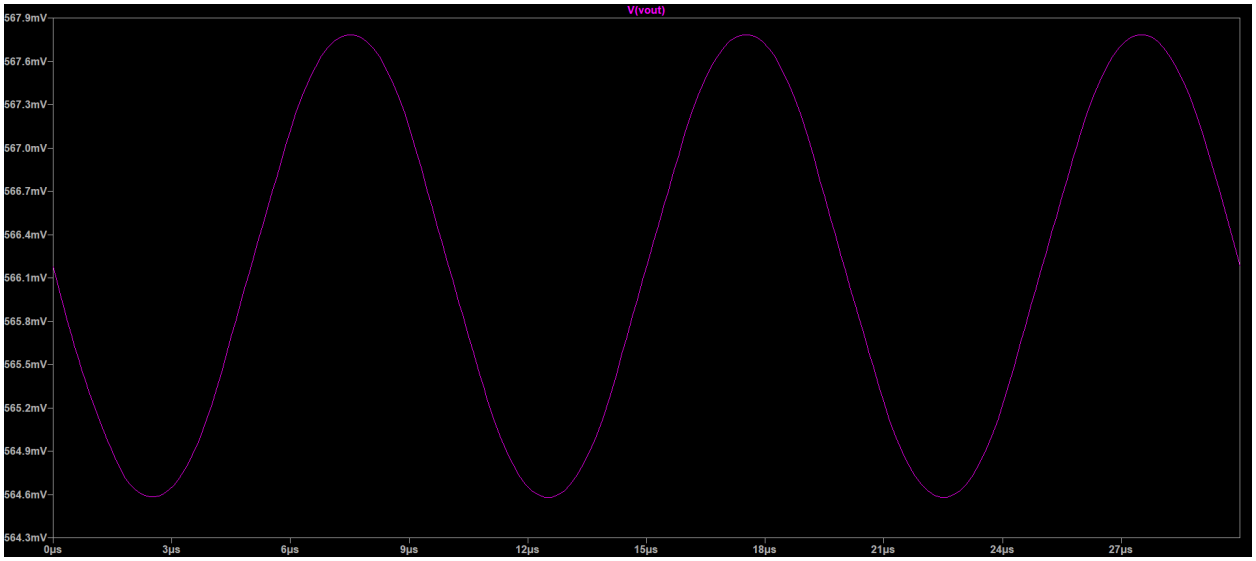
$= 0.029\,mW < 5mW$

Comparing Simulation and Spice results:

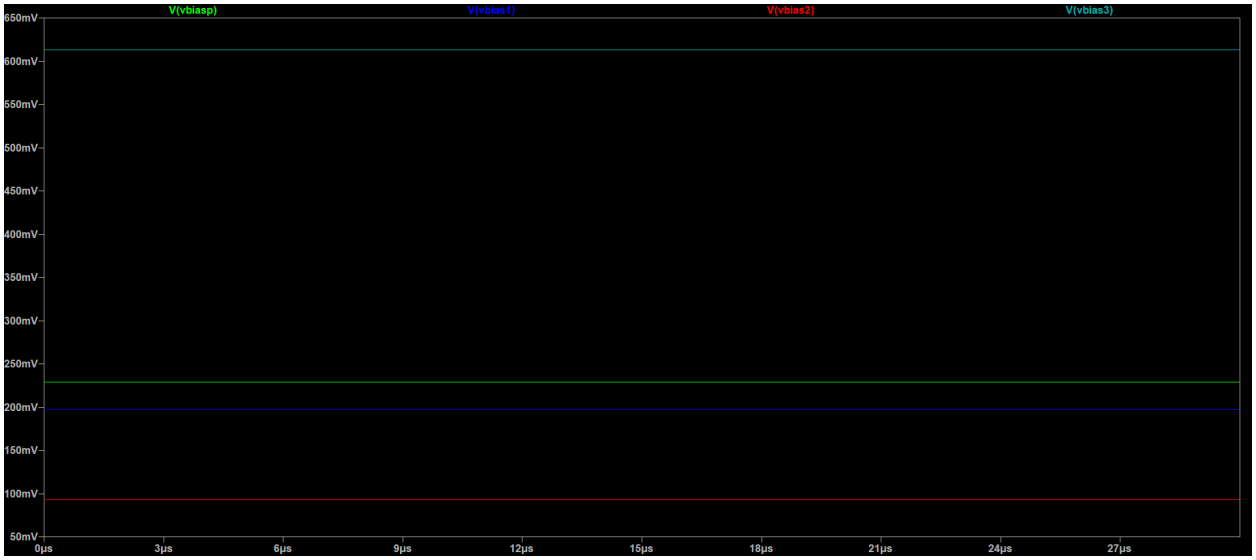
	Theoretical Values	Simulation Results
V_{biasp}	—	1.196 V
V_{bias1}	$\geq$ 1.1 V	1.16 V
V_{bias2}	$\geq$ 0.9 V	1.06 V
V_{bias3}	$\leq$ 0.9 V	0.66 V
V_s(dc)	0.7 V	0.655 V
I_D	18.57 uA	9.8 uA
Av	26 dB	25.1 dB
PD	< 5 mW	0.0176 mW

22 nm Technology:

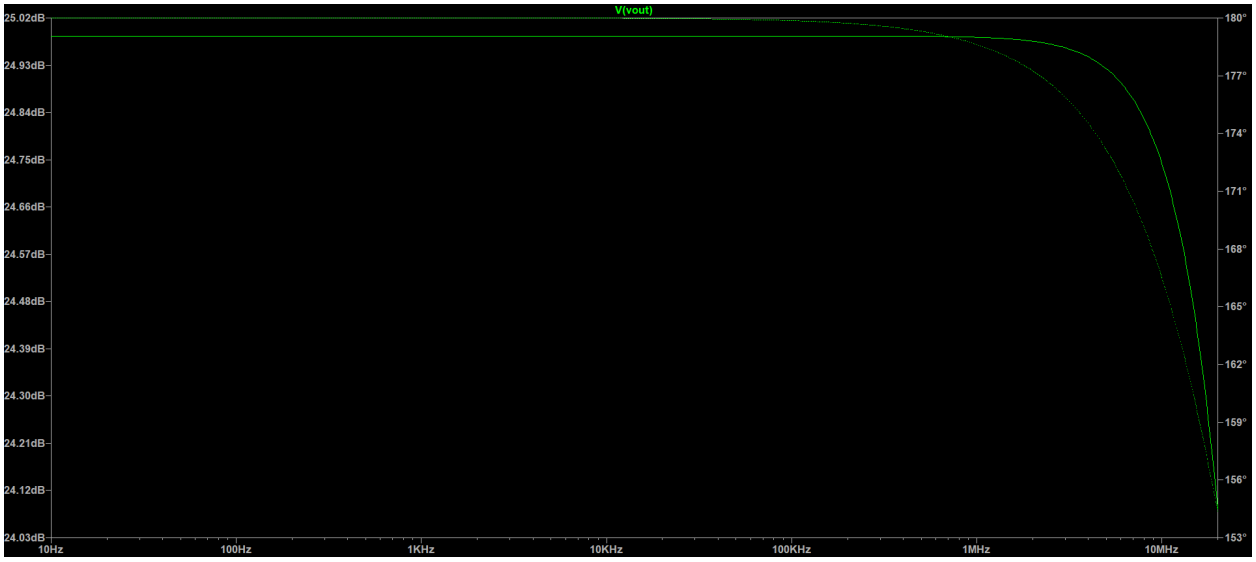
Output
The Simulation outputs obtained were:



Output Waveform



Vbias Values



Frequency Response

Calculations

For 22nm technology:

Given,

$A_V = 20 V/V$ | Power Dissipation $< 5 mW$

$V_{DD} = 0.8V$ | UGB $> 500 KHz$

$C_L = 1pF$ | $\lambda = 0.09$

$V_{thn} = 0.50308V$ | $\mu_n C_{ox} = 100 \mu A/V^2$

$V_{thp} = -0.4606$ | $\mu_p C_{ox} = 50 \mu A/V^2$

Calculations:

Considering the frequency pole location at $1.5 MHz$

$$R_{out} = \frac{1}{2 \times \pi \times 1.5 \times 10^{6} \times 10^{-12}} = 106103.3$$

$$|g_m R_o| = 20$$

$$g_m = \frac{20}{106103.3} = 1.885 \times 10^{-4}$$

$V_{DS} = 0.2V$ (Industrial standard)

$V_{DS} = V_{GS} - V_{th} = V_{ov} = 0.2V$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 (1+\lambda)$$

$$\frac{2 I_D}{V_{ov}} = \mu_n C_{ox} \left(\frac{W}{L}\right) V_{ov} (1+\lambda)$$

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right) V_{ov} (1+\lambda)$$

$$1.885 \times 10^{-4} = 100 \times 10^{-6} \times \left(\frac{W}{L}\right)_N \times 0.2 \times 1.01$$

$$\left(\frac{W}{L}\right)_N = \frac{1.885}{0.2} = 9.425$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 (1+\lambda V_{DS})$$

$$I_D = \frac{1}{2} \times 100 \times 10^{-6} \times 9.425 \times (0.2)^2 \times (1.018)$$

$$I_D = 19.18\ \mu A$$

→ for cascode connection and MOSFET in saturation, same current flows through pMOS as well

$$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p (V_{ov})^2 \times (1+\lambda V_{DS})$$

$$\underset{\times 10^{-6}}{19.18} = \frac{1}{2} \times 50 \times 10^{-6} \times \left(\frac{W}{L}\right)_p \times (0.2)^2 \times (1.018)$$

$$\left(\frac{W}{L}\right)_p = \frac{2 \times 19.18 \times 10^{-6}}{50 \times 10^{-6} \times 0.04 \times 1.018}$$

$$\left(\frac{W}{L}\right)_p = 18.84$$

- Finding ranges of V_{bias1}, V_{bias2}, V_{bias3}, & V_1

Since all mosfets are at the edge of saturation when $V_{DS} = 0.2V$

① M_1

$V_{DS} = 0.2\ V$

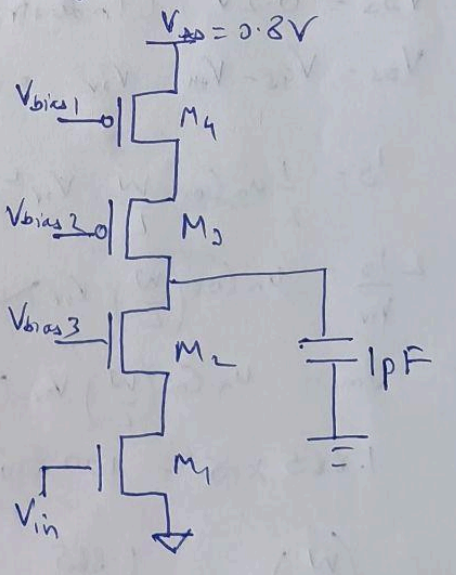
$V_D = 0.2V$ as $V_S = 0V$

$V_{DS} = V_{GS} - V_{th}$

$V_G = V_{in} = V_{OV} + V_{th}$

$= 0.2 + 0.3$

$= 0.5V$



② for M_2

$V_D = 0.4V$

$V_{DS} = 0.2V$ as $V_S = 0.2V$

$V_{DS} \geq V_{OV}$ or $V_{OV} = V_{GS} - V_{th}$

$V_{bias\,3} = V_{OV} + V_{th} + V_S$

$= 0.2 + 0.3 + 0.2$

$= 0.7V$

$V_{bias\,3} = 0.7V$

③ for M_3

~~$V_{DS} = 0.2V$~~ $V_{SD} = 0.2V$

$V_S - V_D = 0.2V$

$V_S = 0.2V + 0.4 = 0.6V$

$V_{SD} = V_{SG} - |V_{thp}| = V_{OV}$

~~$V_G = V_D - |V_{thp}|$~~

$V_S - V_G - |V_{thp}| = V_{OV}$

$V_S - |V_{thp}| - V_{OV} = V_G$

$V_G = 0.6 - 0.3 - 0.2$

$V_G = 0.1V$

$V_{bias\,2} \geq 0.1V$

④ for M_4

$V_{SD} = 0.2V$

$V_S = 0.2 + 0.6 = 0.8V$

$V_S - V_G - |V_{thp}| = V_{OV}$

$V_G = V_S - |V_{thp}| - V_{OV}$

$V_G = 0.8 - 0.3 - 0.2$

$V_G = 0.3V$

$V_{bias\,1} \geq 0.3V$

Power Dissipation:

$P.D = V_{DD} \times I_D$

$= 0.8 \times 19.18\,\mu A$

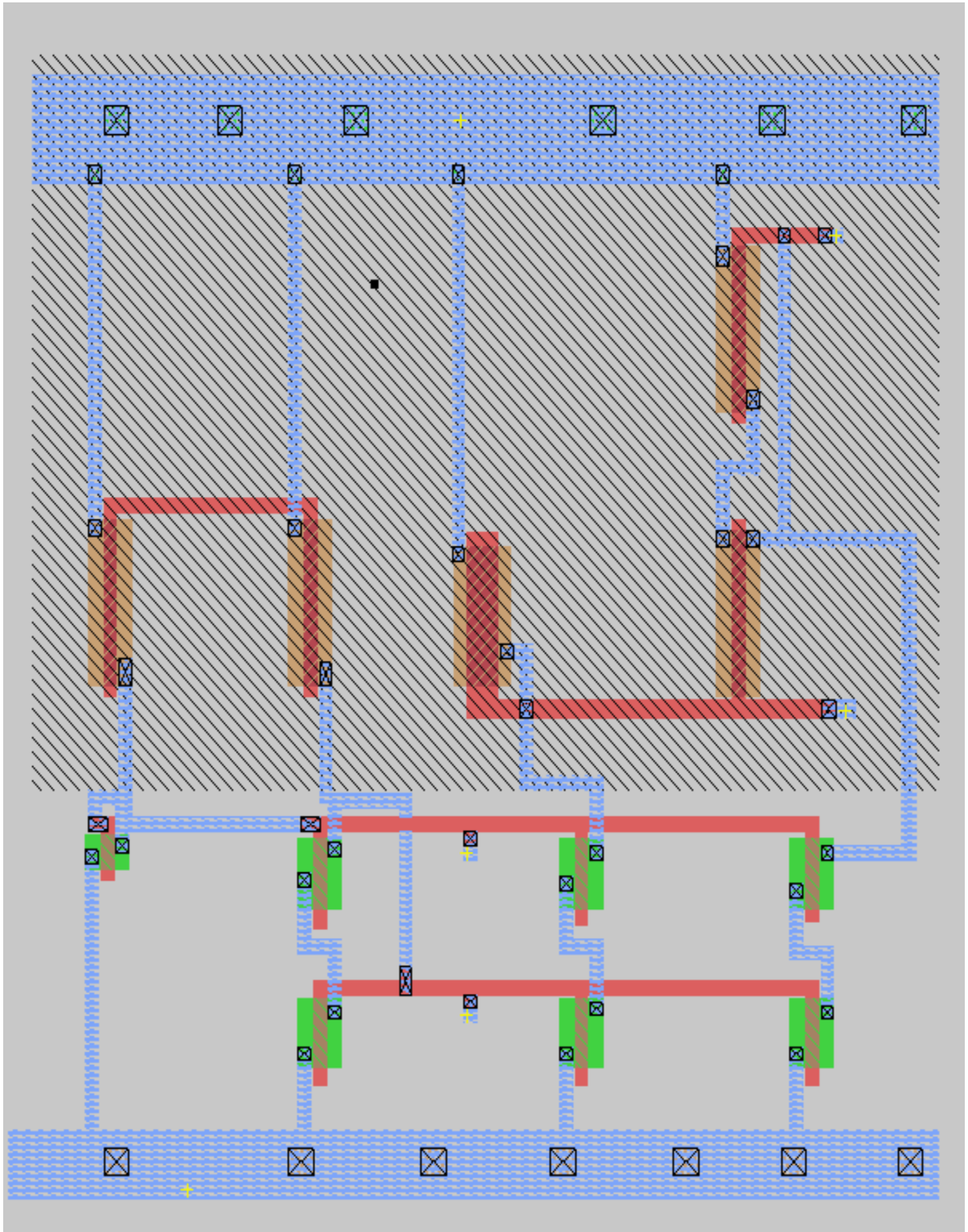
$= 15.344\,\mu W$

$= 0.015\,mW \quad < 5\,mW$

Comparing Simulation and Spice results:

	Theoretical Values	Simulation results
$V_{bias\,p}$		0.24 V
$V_{bias\,1}$	≥ 0.2 V	0.20 V
$V_{bias\,2}$	≥ 0.1 V	0.11 V
$V_{bias\,3}$	≤ 0.7 V	0.24 V
$V_{s(dc)}$	0.5 V	0.58 V
I_D	19.18 uA	28.191 uA
A_V	26 dB	25 dB
P.D	< 5 mW	0.0648 mW
UGB	> 500 KHz	2.1 MHz

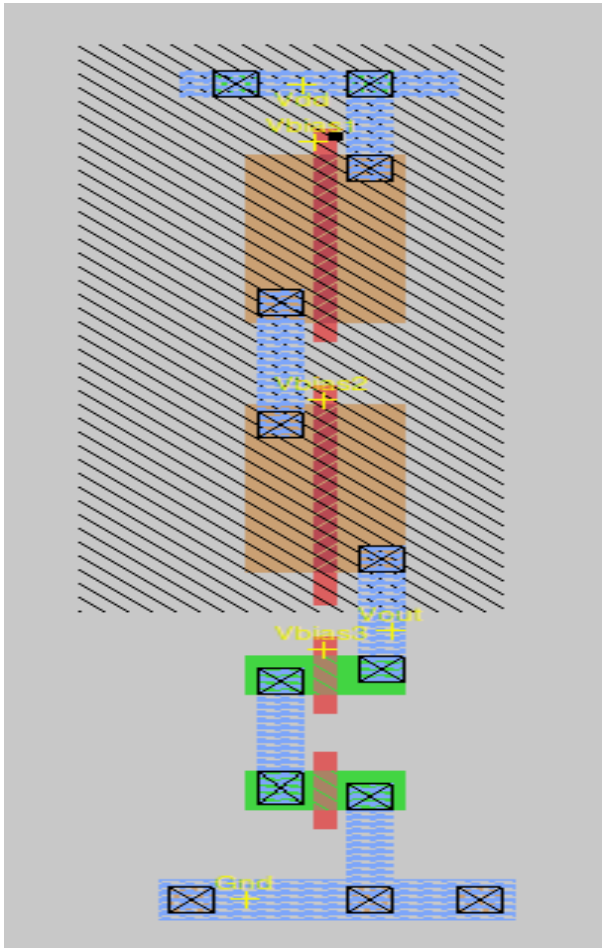
LAYOUT
Current Mirror



NGSpice results :

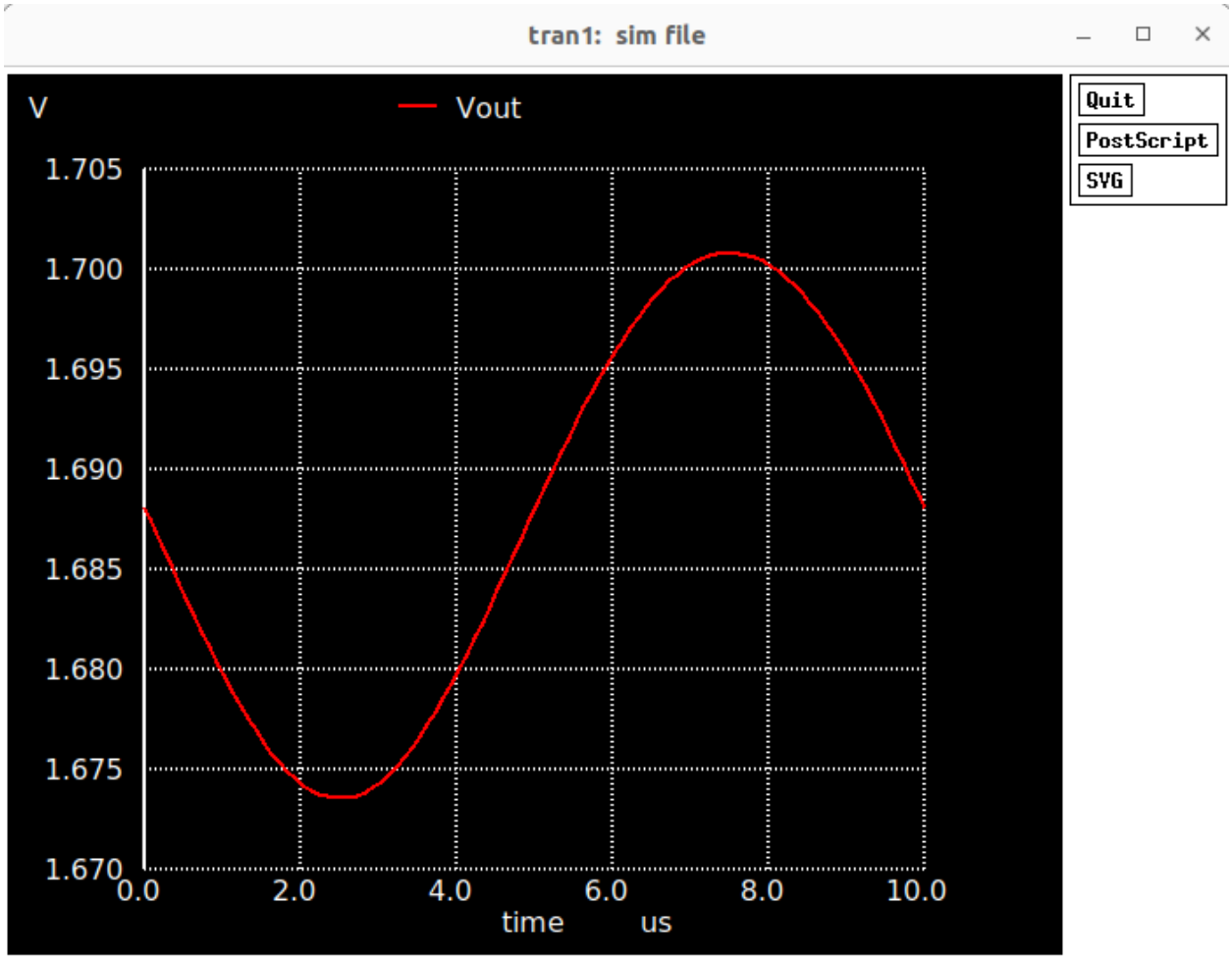
```
Node                                   Voltage
----                                   -------
vbias1                                 1.31368
vdd                                        1.8
vbias3                                0.478804
vbias4                                0.486818
vbias2                                 1.32635
vbiasp                                   1.196
v2#branch                                    0
v1#branch                          -2.25629e-06

 Reference value :  0.00000e+00
No. of Data Rows : 59
ngspice 2 ->
```

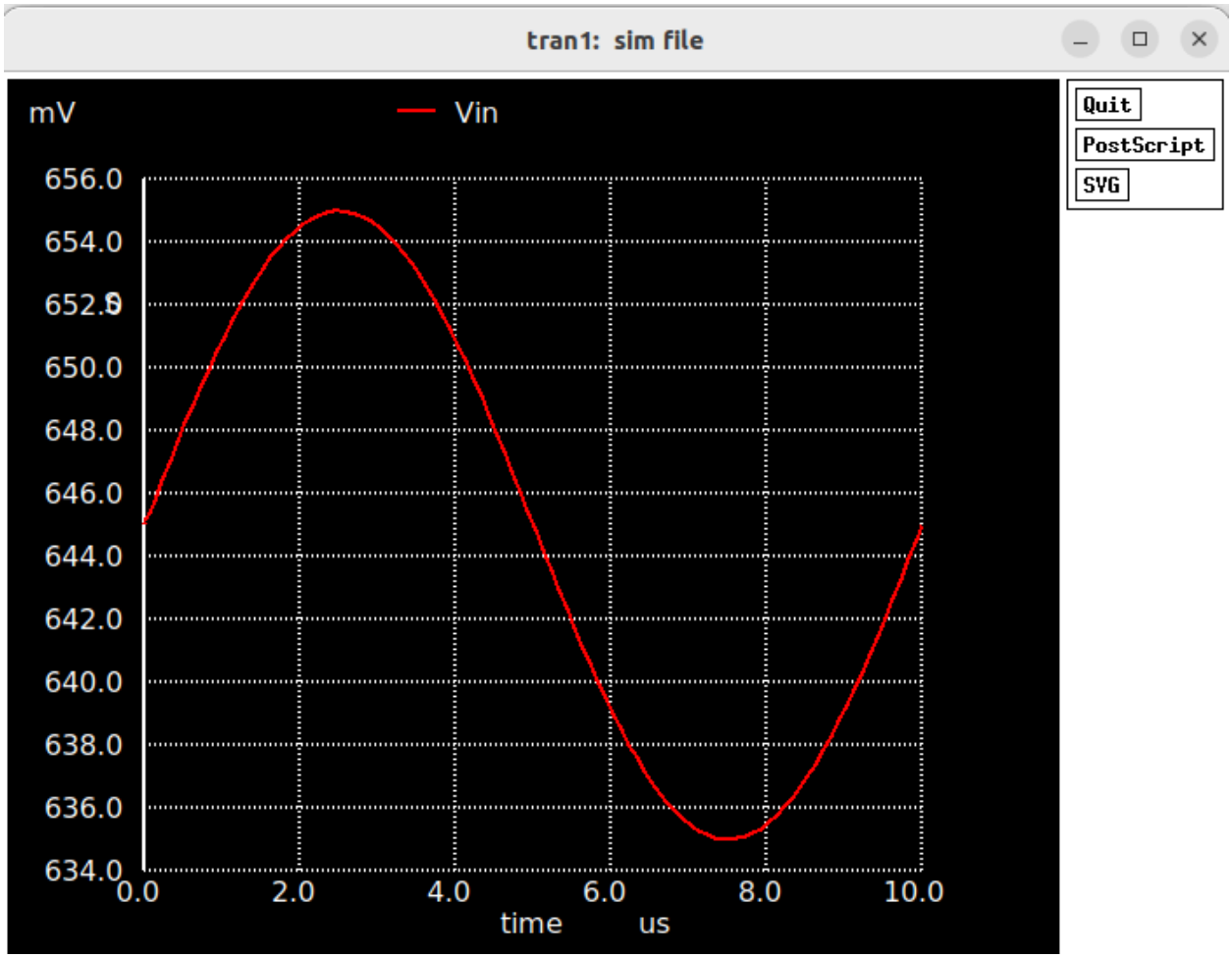
Current Amplifier



NGSpice results :

Node	Voltage
vdd	1.8
vbias1	1.12685
vout	1.68806
vbias2	1.07917
vbias3	0.650134
vin	0.645
v5#branch	0
v4#branch	0
v3#branch	0
v2#branch	0
v1#branch	-6.7261e-06


tran1: sim file
V
Vout
1.705
1.700
1.695
1.690
1.685
1.680
1.675
1.670
0.0
2.0
4.0
6.0
8.0
10.0
time
us
Quit
PostScript
SVG



Observed difference between 180nm and 22nm Technology:

- In general, all the Vbias values and current is lower for 22nm Technology. Thus the Power consumed by 22nm Technology is less than 180nm Technology.
- The Unity gain Bandwidth and hence cut-off frequency of 22nm is higher.
- Since 22nm mosfets are small (8 times smaller than 180nm), they can be packed closer on layout and more transisters can be placed on a chip. This leads to improved performance.
- Howerver due to small size, 22nm mosfet layouts are difficult to design, and this might increase its cost.

Conclusion:

Thus we simulated Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (for both 180nm and 22nm Technology) on LtSpice. The simulation results obtained were close to the theoretical ones and satisfied all the required performance specifications. We also designed the layout for Cascode Current Mirror and Cascode Amplifier on Magic (only for 180nm Technology). Finally, we compared both 180nm and 22nm Technology based on LtSpice Simulation and Magic Layout.