A General Overview of Memristor Devices

Faten OUAJA RZIGA
Micro-optoelectronic & Nanostructures Lab.
Dep. of Physics,
Univ. of Monastir
Monastir Tunisia
faten_ouaja@yahoo.fr

Khaoula MBAREK
Microelectronics & Instrumentation Lab.
Dep. of Physics,
Univ. of Monastir
Monastir Tunisia
Khaoula_mbarek@yahoo.fr

Sami GHEDIRA
Microelectronics & Instrumentation Lab.
Dep. of Physics,
Univ. of Monastir
Monastir Tunisia
ghedirasam@yahoo.fr

Kamel BESBES
Center for Research in Microelectronics & Nanotechnology Sousse Technology Park,
Microelectronics & Instrumentation Lab,
Dep. of Physics, Univ. of Monastir,
Monastir Tunisia
beskamel@gmail.com

***Abstract*—The nanoscale memristive devices will contribute to the development of new applications in the field of micro and nanoelectronics. Indeed, these nanodevices can bring new architectures and configurations, through their sizes, consumptions, functioning and their electronic properties, which differ considerably from the old devices.**

In 1971, Prof. Leon Chua of UC Berkeley has claimed that a fourth passive device should exist, which holds the relationship between magnetic flux and electric charge. In addition, this device named "memristor" was only manufactured in 2008 by HP Lab team. He also proved that the behavior of the memristor should complement the functions of the other three passive elements by bringing a new dynamic. The aim of this paper is to understand the memristor's operation, to introduce and to model its operation for new electronic functions, essentially nonlinear, and to reinforce its integration with other architectures such as CMOS.

Keywords—Nanodevices; Memristor; I-V characteristics; Pinched hysteresis loops.

I. Introduction

Memristor is introduced and proposed by Chua in [1], he claimed that besides the resistor, the capacitor, and the inductor, there should be a fourth basic circuit element: the memristor. According to Chua [1] and Joglekar [2], a memristor can be defined by the relation between the charge q and the flux φ as:

$$d\varphi = M(q(t))\,dq \tag{1}$$

And M(q(t)) is called the memristance.

Hence, the voltage and current relationship of a memristor is described by:

$$V(t) = M(q(t))\,i(t) \tag{2}$$

A useful physical model is proposed by HP Lab team in [3], it is described by a thin film semiconductor sandwiched between two metal contacts.

The film consists of two regions: a doped region (with low resistance R_{ON}) and an undoped region (with much higher resistance R_{OFF}). The illustration of this two terminal electrical device can be seen in Fig. 1.

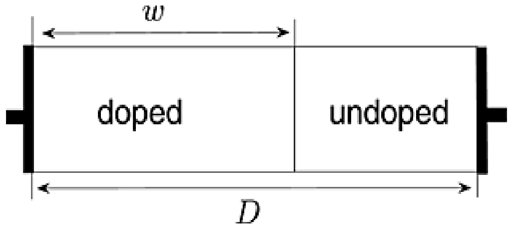


Fig. 1 Illustration of the physical model proposed in [3]. The thickness of the doped region and the undoped region changes under applied input signal.

The nanoscale device shows a great potential in many applications [4]. Assuming the thickness of the film is D, and the thickness of the doped region as w (t) ∈ [0, D]. According to Joglekar [2] and Strukov [3], the simplest model of the device (for the simplest case of ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility μ_v) is the linear drift model:

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \tag{3a}$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t), \tag{3b}$$

As shown in [3], from (3b), the following relation of w(t) and q(t) can be obtained in (4):

$$w(t) = \mu_v \frac{R_{ON}}{D} q(t), \tag{4}$$

Then for $R_{ON} \ll R_{OFF}$, the memristance M(q(t)) (in the memristor definition (1),(2) of the linear-drift model is:

$$M(q(t)) = R_{OFF}\left(1 - \frac{\mu_v R_{ON}}{D^2} q(t)\right) \tag{5}$$

One of the resulting properties of the memristor device is its current-voltage characteristic, the existence of a hysteresis effect [1, 2]. The zero crossing between the current and voltage signals makes it a passive device. It shows that a memristive system do not store electrical energy, unlike capacitance or inductance.

Another property of memristor described in Fig. 2, the pinched hysteresis loop narrows by increasing the excitation frequency. Indeed, when the excitation frequency increases to a higher value the memristor behaves like a linear resistor.

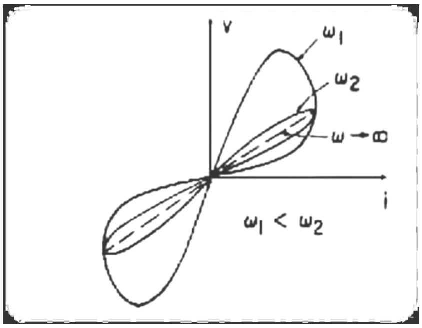


Fig. 2 Memristor hysteresis loop submitted under a periodic input with different frequencies.

Furthermore, a significant interest has been placed on the development of memristor-based systems, which was physically recognized in 2008 by the HP Laboratory [2-3], which is a non-volatile, nanoscale device with variable resistance.

This paper provides a study of a different memristor models that have been proposed since the first physical memristor devices.

So, our aim is to understand the memristor's operation, to introduce its analytic and physical functions, to model its behavior for new electronic functions, essentially nonlinear.

II. Review of Memristor Models

Several SPICE models of the memristor have been studied in [5-8], are based on equation (5). The main differences are displayed in the implementation of the equation of the state variable defined as x=w/D, in particular at the boundaries (minimum and maximum conductance points).

Under the DC voltage application, the devices studied in [7-9] show that the surface of the hysteresis loop decreases as the conductivity of the hysteresis loop increases. The memristor models based on the equations studied in [10] show the inverse effect, with a very large loop near the maximum conductivity. A comparison of those models is presented in Fig. 3 and Fig.4. Fig. 3 shows that the variation of the hysteresis loops is inversely proportional to the conductivity of the memristive device. On the other hand, we found the inverse phenomenon of the switching operation in Fig.4.

Indeed, the accumulation of the current at each pulse of the voltage makes it possible to obtain the various states of resistance, hence it demonstrates the memory effect of a memristive device.

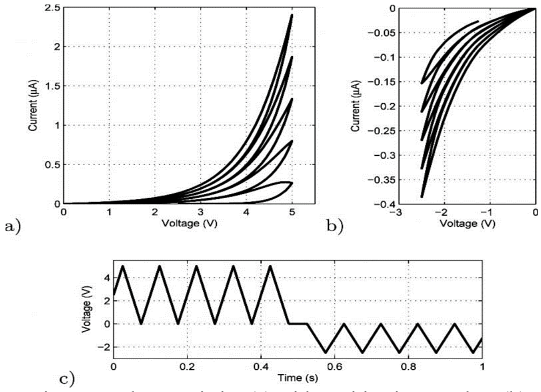


Fig. 3 Memristor I-V characteristics (a) with positive input pulses (b) with negative input pulses. (c) the repetitive sweeping voltage applied across the memristor [9].

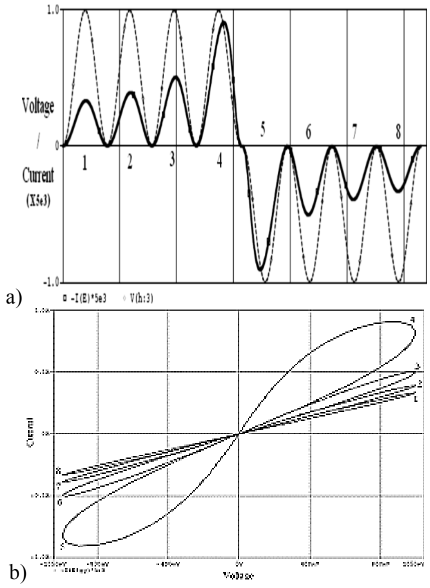


Fig. 4 I-V characteristics of the memristor, a) the input voltage (dashed line) and the resulting current (solid line), b) the pinched hysteresis loops corresponding to the eight positive and negative input voltage [10].

A. Linear ionic drift model

The behavior of this model is presented in Table 1, it is characterized by a pinched hysteresis loop. However, this model has disadvantages that must be fixed. For example, the state variable x is not bounded by the limits 0 and 1, which is physically impossible to pass them. Therefore, this model does not take into account the non-linearity of a strong electric field inside the memristor [3, 6].

B. Nonlinear ionic drift model

A more advanced model shown in Table 1 is the nonlinear model. This memristor model solves the problem at the boundary levels of the linear ionic drift model by multiplying a nonlinear function f (x), named a window function, in the state variable function. This model also assumes an asymmetric switching behavior displayed on the I-V characteristics with different window functions (Strukov, Joglekar, Biolek ...) presented in Table 1.

C. *Exponential model*

The nonlinear model does not yet hold the nonlinearity of the large electric field in a memristor. The exponential model takes this effect into account, Yang *et al.* propose an example of this model in [11] which uses the following equation:

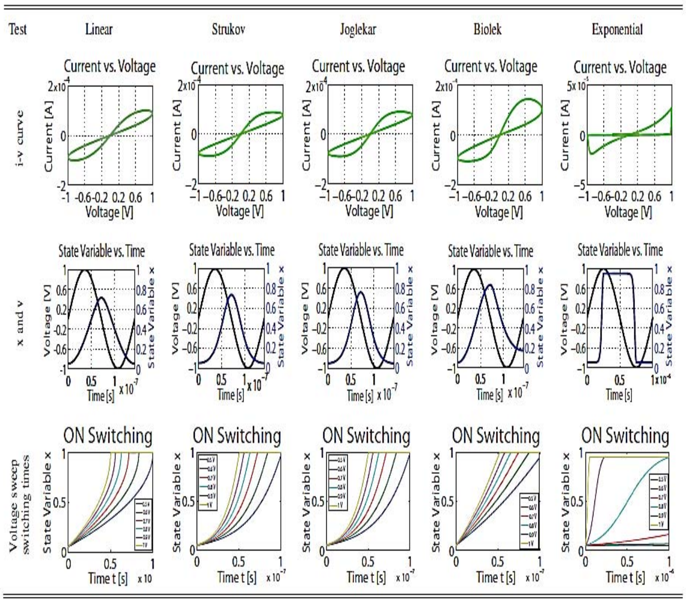
$$I = w^n \beta \sinh(\alpha V) + \chi(\exp(\gamma V) - 1) \quad (6)$$

Where α, β, χ and γ are adjustment constants and n is a free parameter.

The advantage of this model is that in the OFF state the I-V characteristic behaves as a PN junction (the second term of equation (6)), while in the ON state the I-V characteristic follows a tunneling process (the first term of equation (6)). However, the equation of the state variable will be modeled by the following non-linear equation [11], note that f (x, i) is the window function:

$$\dot{X} = a \sinh(bv)\, f(x, i) \quad (7)$$

Table 1 Comparison of memristor models [12].



A summary of these various models and simulation tests is given in Table 1. The results show that all models can operate at high frequency (~ MHz), compatible with the specifications of a memory.

The results also show that the switching time in the first two models, linear and nonlinear, is not sensitive to the voltage level.

The exponential model is more sensitive to the voltage level as its switching time is highly dependent on the voltage level. The reason behind this rapid response in this model is that the drift equation of this model is highly nonlinear to the bias voltage.

Thus, the exponential model presents a more reasonable description of a functional memristive device. The fact that this model is more sensitive to the voltage level gives it the flexibility to reconcile fast and stable ON / OFF switching in the memristor operations.

D. *Improved window functions*

According to Strukov [3], (4) is only valid for values of w(t) in the interval [0, D]. Nonlinear drift, when w is close to zero or D, is not considered in the linear drift model. Because small voltages can yield to a huge electric fields in nanoscale devices, there will be significant nonlinearities in ionic transport [3]. Thus, to model the boundary condition and the nonlinear drift, when *w* is close to zero or D, a window function F(w) is often multiplied to the right-hand side of (3b).

As w(t) is close to 0 or D, the window function F(*w*) in (3b) will tend to 0. Therefore, dw(t)/dt will also tend to 0, according to (3b). And this will keep w(t) in [0, D].

One commonly used window function is given in [2]:

$$F_p(w) = 1 - \left(\frac{2w}{D} - 1\right)^{2p}, \quad (8)$$

Where parameter p is a positive integer. Particularly, the p=1 case was first proposed in [3], together with the linear drift model. It is easy to verify that Fp (0) = 0, Fp (D) = 0 and Fp (w) <1, ∀ w ∈ [0, D].

Note that, $\lim_{p\to\infty} F_p(w)=1$, ∀ w ∈ (0, D), which implies that equation (3) with $F(w)=F_p(w)$ behaves like the linear drift model when w is around D/2 [2]. Letting, w(t)=w(t)/D, (8) can be written as: $F_p(\varpi(t))=1-(2\varpi(t)-1)^{2p}$.

Because window functions are nonlinear, multiplying a window function to the right-hand side of (3b) may make the new model more complex than the linear drift model. For example, consider equation (3) with F(w)=Fp(w). For p>1, to our best knowledge, no explicit relation between *w*(*t*) and q(t), like (4) for the linear drift model, can be calculated [2]. Therefore, for p>1, explicit memristance expression M(q(t)) in the memristor definition (1), (2) cannot be delivered.

III. SIMULATION RESULTS

We have discussed the functioning of some models of SPICE memristor, of different structures and subjected to various polarization voltage.

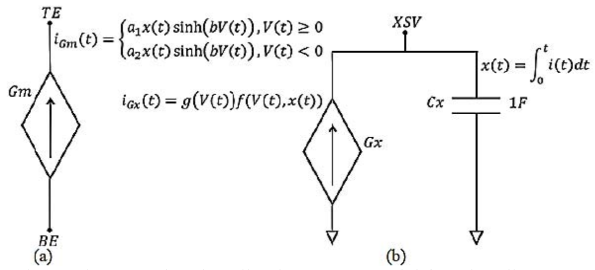
Several memristor models have been proposed, but so far no model has yet been correlated and adapted to different memristor characterization data subjected to various polarization voltage and composed of different physical structures.

We examine the characteristics of I-V of a generic memristor model which adapts to the characterization data of different memristive devices subjected to different types of polarization voltage. The polarization voltages studied are either repetitive sinusoidal or repetitive pulses whose purpose is to present the intermediate levels between the minimum and maximum resistances of the memristors.

A. *Modeling of the memristor in SPICE*

Modelgni the electrical characteristics of the memristor, SPICE would be the most appropriate way to describe the actual operation of the memristor. Using the model as a subcircuit can show a reasonable flexible and high development functions. We will then study the model proposed by C. Yakopcic in 2013 in the paper [20] studied at the University of Dayton, this device has been quantitatively correlated to several memristive devices for two sinusoidal and repetitive sweeping voltage.

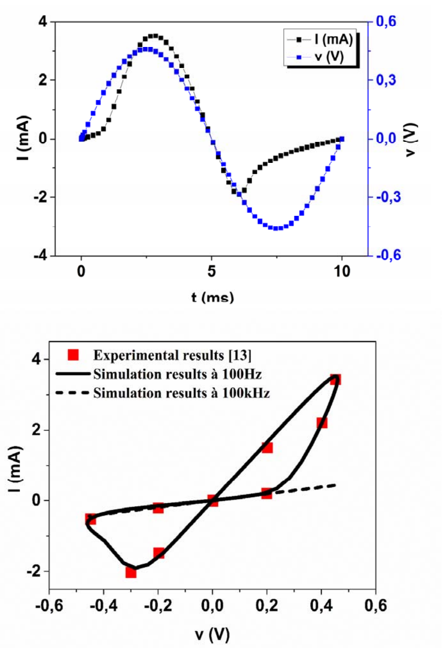
This model has been developed according to the diagram of Fig 5 proposed by Yakopcic [20], which represents a two-terminal subcircuit with two parts (a) and (b). Fig. 5 (a) shows a voltage-controlled current source Gm, it maintains the I-V relationship of the device. The TE and BE electrodes represent the upper and lower electrodes of the memristor. Fig 5 (b) responsible for determining the state variable, using another current source Gx and a capacitor Cx. The capacitor Cx is used to integrate the current generated by Gx to produce the value of the state variable. This technique is similar to those proposed in other SPICE memristor models [21, 22]. The XSV electrode is used to provide a convenient method to draw the internal state variable.



(a) (b)

Fig. 5 Diagrams that describe the SPICE model functionality [21].

The Fig 6. shows the simulation results of the model proposed by Yakopcic [20], (a) shows the voltage and current applied to the memristor terminals, (b) the resulting hysteresis at 100Hz and 100kHz where the Hysteresis shrinks to become linear.



(a)

(b)

Fig. 6 (a) Voltage and current curve applied to the memristor terminals, (b) The resultant hysteresis loop at 100Hz and 100kHz where the deviates linear.

B. Analytical context

This model is based on three different characteristics observed in the memristive devices: a metal-insulator-metal junction presented in equation (9), a voltage threshold for the motion of the state variable shown in equation (10), and a drift function of the dopants shown in equations (11) and (12).

The generalized I-V relation by this model can be seen in the following equation [20, 23]:

$$I(t) = \begin{cases} a_1 x(t)\sinh(bV(t)), V(t) > 0 \\ a_2 x(t)\sinh(bV(t)), V(t) < 0 \end{cases} \qquad (9)$$

This equation is based on a hyperbolic sinusoid which serves to increase the conductivity beyond a threshold voltage value. The parameters a_1, a_2 and b are used to adjust this equation to the different structures of the memristive devices. a_1 and a_2 are two amplification or attenuation parameters which depend on the polarity of the input voltage. The adjustment parameter b used to control the conductivity of the device.

The variation of the state variable x (t) is based on two functions g (V(t)) and f (x(t)).

The function g (V(t)) is responsible for the implementation of the threshold voltage which must be exceeded in order to induce a change in the value of the state variable.

$$g(t) = \begin{cases} A_p\left(e^{V(t)} - e^{V_p}\right), & V(t) > V_p \\ -A_n\left(e^{-V(t)} - e^{V_n}\right), & V(t) < -V_n \\ 0, & -V_n \leq V(t) \leq V_p \end{cases} \qquad (10)$$

$$f(x) = \begin{cases} e^{-\alpha_p(x-x_p)} w_p(x,x_p), & x \geq x_p \\ 1, & x < x_p \end{cases} \qquad (11)$$

$$f(x) = \begin{cases} e^{\alpha_n(x+x_n-1)} w_n(x,x_n), & x \leq 1-x_n \\ 1, & x > 1-x_n \end{cases} \qquad (12)$$

While,

$$w_p(x,x_p) = \frac{x_p - x}{1-x_p} + 1$$

$$w_n(x,x_n) = \frac{x}{1-x_n}$$

The amplitudes A_p and A_n represent how the state changes once the voltage threshold is exceeded. The variation of the state variable on the function f (x (t)) remains constant up to the points x_p ou x_n and is limited by two factors of amplification or attenuation α_p or α_n. The parameters x_p, x_n, α_p and α_n are necessary for this model to be able to match the dynamics of several devices.

C. physical concept

This memristor is based on three main characteristics, the tunnel effect of electrons shown in the current equation by the hyperbolic sine function, the nonlinear drift shown in the ionic drift equation f (x (t)). And a voltage threshold is shown in the voltage equation g (t).

The memristor model described by C. Yakopcic has been correlated to present the I-V characterization data of the memristive devices [22- 28].

The next simulation results reveal the richness of circuit's dynamical behavior confirming the usefulness of the specific design approach.

The Fig. 7, shows the linear allure of the flux and charge curve.

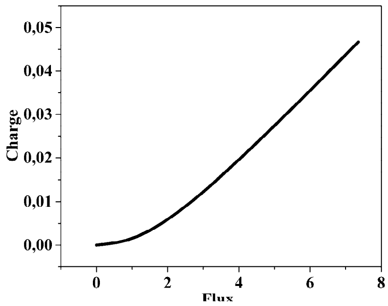


Fig 7. The relationship between the charge and flux.

The effect of memristive switching is inspected by varying the implemented parameters of the model such the magnitude of input voltage V, initial charge q, state variable, etc. may change the operating regime so the memristance value may not remain constant and the memristor operates in different segments or takes different memristance values. This sudden jump of memristance is called as "memristive switching" or "resistive switching".

In this case, memristive switching depends on the bias of the applied voltage across the device which is represented in Fig. 8, the curve of the state variable motion at memristor boundaries. We consider the memristor in an Off state, as an initial state of the device, switching the device to On state, requires a positive bias across the device. While switching to Off state requires negative bias.

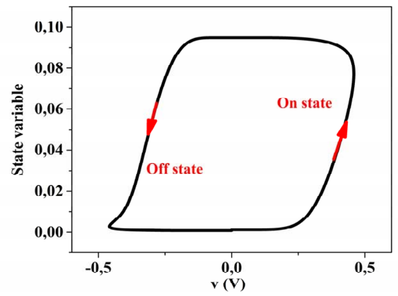


Fig. 8 The state variable motion at memristor boundaries according to the applied voltage.

The Fig. 9 represents the curve of the memristance or the resistance of the memristor on the On and Off state. From this results, Ron and Roff's value estimated by 1.3kΩ and 1.1kΩ respectively.

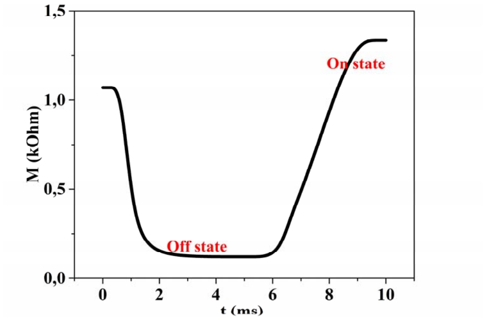


Fig. 9 The memristance as a function of Time.

IV. CONCLUSION

In this paper, we point out for an appropriate model that can be used in the circuit design of memory cell utilizing memristor as a storage element. The model is tested for different conditions and parameter's values and its dynamic behavior clearly fulfills the memristive fingerprints. We prove that the SPICE memristor model is a reliable and flexible memristor model. This memristor model will bring a new perspective for the study of the dynamical behavior of memristive neural network.

REFERENCES

[1] L. Chua, "Memristor-the missing circuit element." IEEE Transactions on Circuit Theory, vol. 18, no 5, pp. 507–519, September 1971.

[2] Y. Joglekar, S. Wolf, "The elusive memristor: properties of basic electrical circuits." European Journal of Physics, vol. 30, no 4, pp. 661–675, May 2009.

[3] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams. "The missing memristor found." Nature, vol. 453, pp. 80–83, May 2008.

[4] R. S. Williams. "How we found the missing memristor." IEEE Spectrum, vol. 45, no 12, pp. 28–35, December 2008.

[5] J. J. Yang, M. X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro1, R. S. Williams, "High switching endurance in TaOx memristive devices." Applied Physics Letters, vol. 97, no 23, pp. 232102, November 2010.

[6] C. Merkel, "Thermal profiling in CMOS/memristor hybrid architectures." theses New York, pp. 94, May 2011.

[7] T. Chang, S. H. Jo, K. H. Kim, P.Sheridan, S. Gaba, W. Lu, "Synaptic behaviors and modeling of a metal oxide memristive device. " Applied physics A, vol. 102, no 4, pp. 857-863, March 2011.

[8] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems". Nano letters, vol. 10, no 4, p. 1297-1301, March 2010.

[9] M. Laiho, E. Lehtonen, A. Russel, P. Dudek, "Memristive synapses are becoming reality." The Neuromorphic Engineer, November 2010.

[10] M. J. Sharifi, Y. M. Banadaki, "General spice models for memristor and application to circuit simulation of memristor-based synapses and memory cells." Journal of Circuits, Systems, and Computers, vol. 19, no 02, pp. 407-424, September 2010.

[11] J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices". Nature nanotechnology, vol. 3, no 7, pp. 429-433, June 2008.

[12] H. Elgabra, I. A. Farhat, A. S. Al Hosani, D. Homouz, B. Mohammad, "Mathematical modeling of a memristor device." In: Innovations in Information Technology (IIT), 2012 International Conference on. IEEE, pp. 156-161, 01 June 2012.

[13] L. Chua, S. Kang, "Memristive devices and systems." Proceedings of the IEEE, vol. 64, no 2, pp. 209–223, Feb. 1976.

[14] L. Chua, A. C. Deng, "Canonical piecewise-linear modeling." IEEE Transactions on Circuits and Systems, vol. 33, no 5, pp. 511–525, May 1986.

[15] L. Breiman, “Hinging hyperplanes for regression, classification, and function approximation.” IEEE Transactions on Information Theory, vol. 39, no 3, pp. 999–1013, May 1993.

[16] S. Wang, X. Huang, K. M. Junaid, “Configuration of continuous piecewise-linear neural networks.” IEEE Transactions on Neural Networks, vol. 19, no 8, pp. 1431–1445, Aug. 2008.

[17] L. Chua. “Resistance switching memories are memristors.” Applied Physics A: Materials Science & Processing, vol. 102, no 4, pp. 765–783, 2011.

[18] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, R. S.Williams, “Switching dynamics in titanium dioxide memristive devices.” Journal of Applied Physics, vol. 106, no 7, pp. 508–074, July 2009.

[19] S. Kvatinsky, E. G. Friedman, A. Kolodny, U. C. Weiser, “Team: threshold adaptive memristor model.” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no 1, pp. 211–221, November 2012.

[20] C. Yakopcic, T. M. Taha, G. Subramanyam, R. E. Pino, “Generalized memristive device SPICE model and its application in circuit design”. IEEE Transactions on, Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no 8, pp. 1201-1214, Aug. 2013.

[21] T. Chang, S. H. Jo, K. H. Kim, P. Sheridan, S. Gaba, W. Lu, “Synaptic behaviors and modeling of a metal oxide memristive device.” Applied Physics A: Materials Science & Processing, vol. 102, no 4, pp. 857-863, March 2011.

[22] D. Biolek, V. Biolkova, Z. Biolek, “SPICE model of memristor with nonlinear dopant drift”. Radioengineering, vol. 18, no 2, pp. 210-214, June 2009.

[23] C. Yakopcic, Ph.D. thesis, University of Dayton, Dayton, Ohio 2011. “Memristor Devices: Fabrication, Characterization, Simulation, and Circuit Design”. Ph.D. thesis, University of Dayton 2011.

[24] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, “Nanoscale memristor device as synapse in neuromorphic systems.” Nano letters. vol. 10, no 4, pp. 1297-1301, March 2010.

[25] F. Miao, J. P. Strachan, J. J. Yang, M. X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, R. S. Williams, “Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High□Performance Memristor.” Advanced materials, vol. 23, no 47, pp. 5633-5640, November 2011.

[26] A. S. Oblea, A. Timilsina, D. Moore, K. A. Campbell, “Silver chalcogenide based memristor devices”. in: 2010 International Joint Conference on Neural Networks (IJCNN), pp.1-3, 14 October 2010.

[27] S. H. Jo, W. Lu, “CMOS compatible nanoscale nonvolatile resistance switching memory.” Nano letters, vol. 8, no 2, pp. 392-397, January 2008.

[28] K. J. Miller. “Fabrication and modeling of thin-film anodic titania memristors.” 2010.