A Memristor-based 6T1M Hybrid Memory Cell without State Drift during Successive Read

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Abstract—**This research proposes a new 6T1M memory structure, which is designed using 6 transistors and a single memristor. The proposed cell is capable of storing data in bidirectional fashion. This memory model is not only space efficient but also operates faster than other conventional structures. It does not require any refresh operation as it prevents state drift during successive read operation. Extensive simulation results by employing LTspice demonstrates the excellent performance and competency in terms of write time, read time and power dissipation of the proposed model .**

***Index Terms*— Memristance; Hybrid; Bidirectional; State Drift**; **Precharge.**

I. INTRODUCTION

CMOS based conventional memory technologies have reached its zenith to achieve higher density with the continuous constriction in nano scale regime [1-3]. Moore scaling will be difficult to meet as the end of scaling paradigm is imminent with the current shrinking rate of CMOS. Very recently, a highly capable despite of its infinitesimal size has been demonstrated which is the first physical realization of the elusive fourth fundamental circuit element, memristor. Because of the less power consumption along with the occupation of less die area, memristor has got the potential to supplant CMOS transistors in next generation computers [4-5]. Memristor has got some fascinating features like non volatility, nonlinearity at the boundaries, high packing density in crossbar arrays which have spurred extensive attention to the researchers to design memristor based nonvolatile memory arrays. Moreover, fabrication compatibility of memristor with CMOS technology boosted the hybrid approach of designing nonvolatile memory.

A novel 6T1M hybrid memory cell is proposed in this research. This model is the modified version of our previously proposed 7T1M [6] memory cell. The passive two terminal memristor is employed in this research to hold data in terms of resistance. The proposed circuit stores data bidirectionally and also does not require any refresh operation while successive read operation is performed. The main hindrance to design memristor based nonvolatile memory is the state drift phenomena in successive read which is referred to the change in memristor state from R_{OFF} to R_{ON} or vice versa. In the proposed cell, only one memristor is utilized to store data (0 or 1). So, there is a possibility to affect either a "0" or a "1" while retrieving data depending on the read pattern. If the read pattern is like the write 0 (1) pattern, stored 1 (0) can be affected after each read pattern and state drift phenomena can be occurred after some successive read operation. A new approach is provided to eradicate the state drift phenomena in this paper. The proposed circuit also outperforms some recently developed memristor based memories [7-11] in terms of die area, write and read times.

II. BACKGROUD

The missing memristor was first postulated by Chua [12] in 1971 based on the circuit theoretical reasonings. Memristor is considered as the so called fourth fundamental circuit element because of its canonical nature [13] (i.e., missing static relationship between flux and electric charge). The missing relationship between flux and electric charge having memristance M of the memristor is $d\varphi=Mdq$, where φ and q are the flux and electric charge respectively. The resistance of the memristor which is the so called memristance does not change even if the supply voltage is removed. The physical model of memristor (see fig. 1) presented in [14] is composed of a two layer of TiO_2 thin film which is sandwiched between the top and bottom electrodes. The physical structure of the two electrodes is basically metal nanowires on platinum. State of the memristor can be changed according to the direction of current through the device or applied biasing (i.e., forward or reverse). R_{ON} and R_{OFF} state can be achieved by applying positive and negative voltage to the top electrode respectively. Oxygen vacancies drift from the doped (TiO_{2-x}) to the undoped (TiO_2) region or vice versa while the state of the memristor gets to the ON or OFF state respectively. The total resistance of the memristor is given by

$$M(t)=\left\{R_{ON}\frac{w(t)}{D}+R_{OFF}\left(1-\frac{w(t)}{D}\right)\right\} \quad (1)$$

Where R_{ON} and w(t) are the resistance and width of the completely doped region while R_{OFF} is the resistance of the

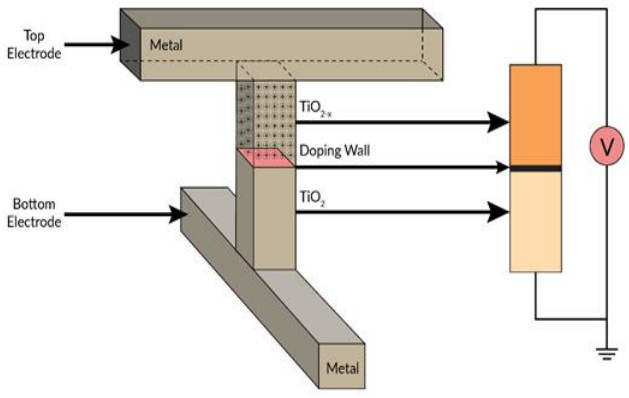


Fig. 1. Physical structure of memristor

completely undoped region. The parameter D denotes the thickness of TiO_2.

III. PROPOSED MEMORY CIRCUIT

The proposed bidirectional memory cell (see Fig. 2) which is hybrid in nature is composed of only six transistors for switching purpose and one memristor as a nonvolatile storage element. Among the six transistors used to design the bidirectional memory cell, two of them are PMOS transistors and the rest of them are NMOS transistors like the conventional 6T SRAM cell. But the operation of the proposed memory circuit is different from the conventional SRAM cell and does not need standby power to hold the binary data like the SRAM cell. In case of data extraction from one memristor, state drift phenomena is the main hindrance to design a stable hybrid memory cell. The bidirectional binary data storing of the proposed memory circuit is rapid and also prevents state drift for repetitive read.

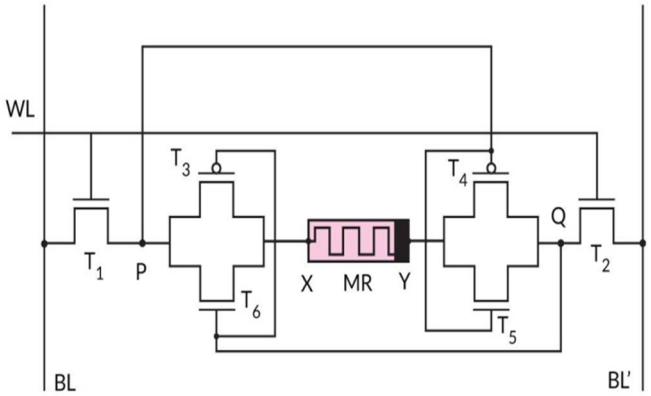


Fig. 2. Proposed 6T1M memory cell

A. Write Operation

The nonvolatile memristor gets the raw data to store through the bit line (BL) and inverse bit line (BL'). The word line (WL) selects the memory cell during data storing and extraction operation. The word line (WL) is set to high (VDD) to send the binary data to the memristor through the access transistors T_1 and T_2 for storing.

1. Write a "0"

When the bit line (BL) and inverse bit line (BL') are set to high and low respectively, current flows from node P to node Q that means from the undoped to the doped region of the memristor. Transistor T_3 and T_5 will be ON during this biasing. So, there will be a positive voltage from the undoped to the doped side of the memristor ensuring the full enhancement of the boundary of the undoped region over doped region. Thus, maximum memristance value will be achieved (i.e., R_{OFF} state) and a "0" will be written in the cell.

2. Write a "1"

The current flow during a write "1" operation is opposite to the one of writing a "0" operation as inverse biasing of writing a "0" needs to apply to get minimum memristance value. The memristor will be forward biased as the bit line (BL) and the inverse bit line (BL') are set to low and high respectively. Transistor T_4 and T_6 will be ON while storing a "1". The presence of negative voltage from the undoped to the doped side of the memristor will ensure the complete enhancement of the boundary of the doped region over the undoped region. Thus, minimum memristance value will be achieved (i.e., R_{ON} state) and a "1" will be stored in the cell.

Hence, bidirectional write operation is performed by the proposed circuit. The write time for the proposed memory circuit is determined by taking the time to change the memristance value from minimum (R_{ON} state) to maximum (R_{OFF} state) or vice versa.

B. READ OPERATION

Read operation starts by precharging the bit line (BL) and the inverse bit line (BL') to high (VDD) and low (GND) respectively. The biasing to extract binary data is identical to the one of writing a "0". This biasing to retrieve binary data eradicates the state drift problem during successive read operation. If the write "1" biasing would have been applied to retrieve the binary data, only "0" would get affected and R_{OFF} state would shift towards the R_{ON} state after every read pattern is applied. This is because there will be a large positive voltage to the doped region of the memristor which will enhance the boundary of the doped region after every read operation. But when write "0" biasing is applied to retrieve the data, a large positive voltage is present to the undoped region (i.e., X terminal) of the memristor which will not cause any state change. If a "1" is stored in the cell, the memristance can be changed while retrieving the "1" because of the opposite directional current flow through the memristor. But the memristance (R_{ON}) is constant as a result of the quick isolation from the bitline while retieving the data. Because of this quick isolation from the bit line (BL), there will not be enough voltage across the memristor to bias it to the R_{OFF} state. This isolation was done by adding a transistor in 7T1M cell [6] which can cause state drift during repetitive read. Detailed explanation of the read operation is carried out next.

As mentioned earlier, the bit line (BL) and the inverse bit line (BL') are precharged to VDD and GND respectively during read operation. So, the transistor T_3 and T_5 will be ON and the transistor T_4 and T_6 will be OFF while the read pattern is applied. Though, the PMOS transistor, T_3 gets OFF just after the starting of read operation and isolates the circuit from the bit line (BL) as the transistor T_6 is already OFF. If a "1" is stored in the memory cell, the voltage at node Q rapidly increases from zero to a large positive voltage as the memristance is lower. So, the source to gate voltage, Vsg of the PMOS transistor, T_3 becomes lower rapidly. The PMOS transistor, T_3 gets OFF as $Vsg < |Vt|$. Here, the threshold voltage $|Vt|$ is 0.16V. As a result of the isolation of the circuit from the bit line (BL), almost zero current flow through the memristor will be achieved. While retrieving a "0", same phenomena is noticed. But the time to have almost zero current through the memristor is higher than retrieving a "1". This is because of the larger memristance value which prevents the rapid increment of voltage at node Q. Fig. 3 depicts that the source to drain voltage (Vsg) of the PMOS transistor, T_3 gets lower as the read operation proceeds. It is also clearly depicting from Fig. 4 that the circuit gets isolated from the bit line (BL) during data retrieving operation. The stored data is detected by the disparate bit line voltage differences ($V_{BL-BL'}$) for "0" and "1".

The voltage difference across the memristor plays an important role in determining state change during repetitive read operation. Fig. 5 demonstrates the voltage difference across the memristor while extracting a "1" is much lower in comparison with the voltage difference across the memristor

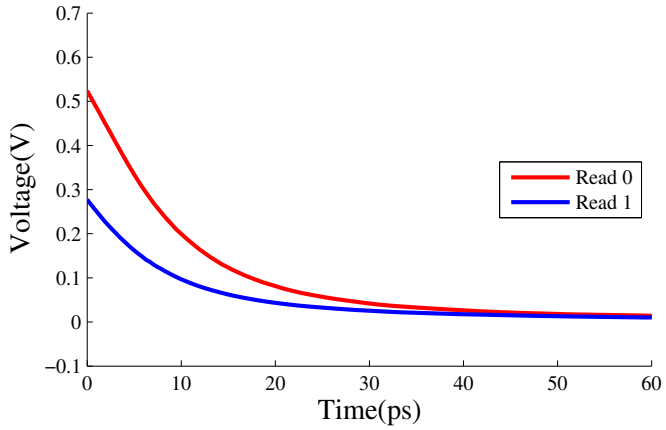


Fig. 3. Source to gate voltage of the transistor, T_3 during read operation

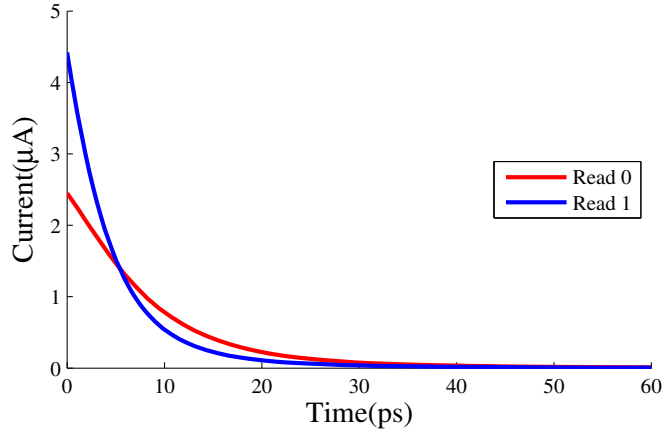


Fig. 4. Current through the memristor (undoped to the doped region of fig. 2) during read operation

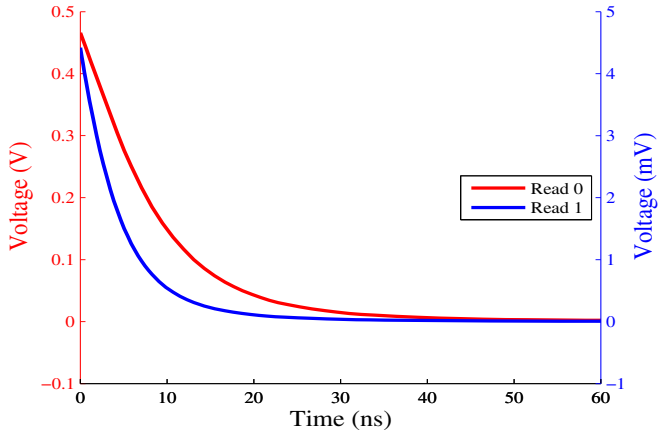
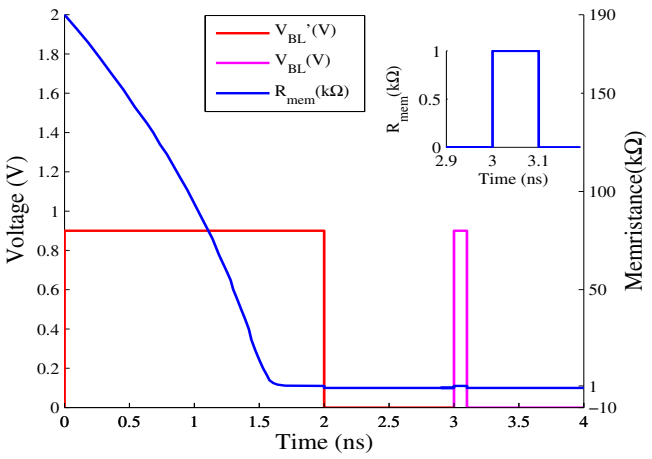


Fig. 5. Voltage across the memristor (V_x-V_y) during read operation

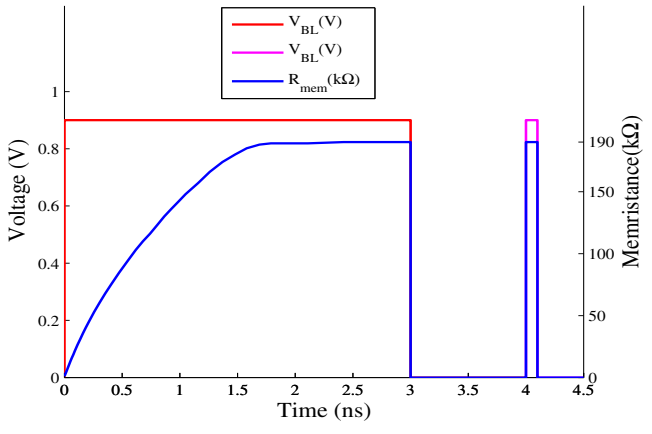
for "0". Moreover, the voltage drop across the memristor for a "1" extraction falls to almost zero abruptly after the starting of read operation. As mentioned earlier, zero will not get affected while the read pattern is identical to wrote "0" pattern. Despite having a high voltage drop across the memristor while retrieving a "0", the boundary of the undoped region cannot move further as it has already been enhanced to the highest level. Now, the negligible voltage drop across the memristor for a "1" extraction cannot change the memristance value. Thus, memristor state will not be perturbed ensuring the prevention of state drift phenomena.

Fig. 6 (a) & (b) delineates that change in memristance is absent for the proposed memory circuit by applying the read pattern hich is identical to write "0" pattern. In fig. 6 (a) the inverse bit line (BL') is high for 2 ns and a "1" is written in the cell as the memristor is biased to the R_{ON} state. From 2ns -3ns, both the bit line (BL) and the inverse bit line (BL') are set to low (i.e., no read or write pattern is given). From 3 ns-3.1 ns, read pattern is given to precharge the bitline to VDD. It is unequivocal from fig. 6(a) that no change in memristance is present while extracting a stored "1" which eradicates the state drift phenomena. The memristance of the memristor before and after the read pattern is applied while retrieving "1" is shown in the inset fig. 6(a). Fig .6 (b) shows the storing and retrieving a "0" in the proposed memory cell. It can also be seen from fig. 6 that zero standby power is required to hold the binary data as the oxygen vacancies get completely immobile when there is no pulse[12],[15]. This unique characteristic will cause a significant reduction of power dissipation in the proposed memory cell in comparison with the conventional SRAM cell and recently developed flash memories.

As mentioned earlier, the stored binary data is detected by the disparate bit line voltage difference for "0" and "1". Fig. 7 depicts the variation of bit line voltage difference for "0" and "1". The reason behind this dissimilar bit line voltage difference is the dissimilar memristance value for "0" and "1" (i.e., R_{OFF} and R_{ON}). If a "1" is already in the cell, the lower memristance value influences rapid voltage transfer from the bit line (BL) to the inverse bit line (BL'). On the other hand, sluggish transfer of voltage from the bit line to inverse bit line is noticed if a "0" is in the cell. From fig. 7, it is unequivocal



(a)



(b)

Fig. 6. Read and Write pattern and memristance for (a) "1" (b) "0"

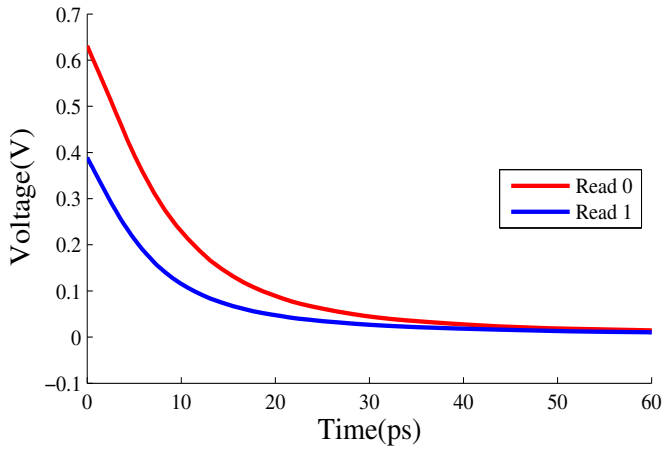


Fig. 7. Bitline voltage difference ($V_{BL-BL'}$) for retrieving "0" and "1"

that the bit line voltage difference for "0" is larger than "1" which is because of the sluggish abatement of the bit line voltage for a "0" extraction than a "1" extraction. The bit line voltage difference for retrieving "0" and "1" are 254 mV and 129 mV while the read time is 9 pS. The difference in voltage between the bit lines for "0" and "1" gets smaller if the read time is taken high.

IV. SIMULATION RESULTS AND COMPARISON

By employing LTspice as a simulation tool, extensive simulation experiments have been carried out to evaluate the competency of the proposed memory cell. 32 nm [16] feature size of CMOS technology has been employed by setting L_{eff} = 12.6 nm, T_{ox} = 1nm, VDD = 0.9 V and threshold voltage of PMOS and NMOS are -0.16 V and 0.16V respectively. Highly scalable memristor model of [17] having the R_{OFF}/R_{ON} ratio of 190 (i.e., R_{OFF} = 190 K and R_{ON} = 1K) and x_0 =0.4, a=50, p=10 are employed to exploit the characteristics of the proposed memory cell. Other parameters [18] used for simulations are: D= 1 nm, μ_v = 1e-7($m^2 s^{-1} V^{-1}$).

TABLE I

COMPARISON OF THE PROPOSED CELL WITH RECENTLY DEVELOPD MEMRISTOR BASED MEMORY CELL

	Proposed Cell	**Ambipolar based memory[7-8]**	**MCAM [10]**
Write '0'	2.189 ns	219 ns	201 ns
Write '1'	1.7 ns	219 ns	201 ns
Read	9.00 ps	1.095 ns	12 ns
Supply Voltage	0.9 V	0.9 V	0.9 V

The proposed 6T1M memory cell does not only require refresh operation but also capable of rapid bidirectional storage operation. Recently developed memristor based memory cells such as Ambipolar based memory [8] requires large number of transistors to perform various operations and also refresh operation is required for repetitive read. The MCAM [10] cell requires search operation to match the stored data which causes high read time. Though the memory cell of [7] does not require any refresh operation, large die area is required to perform the bidirectional storage operation. On the other hand, if the threshold voltage of the ambipolar transistor in [7] is taken high, erroneous read operation can be occurred due to the belated switching and turning off the PMOS and ambipolar transistor respectively. The proposed circuit does not suffer the problem of erroneous read operation while varying the threshold voltage of the PMOS transistor. Though the memory cell of [10] does not require any refresh operation, higher supply voltage is needed to operate the cell because of the use of diode. This is the reason of higher dynamic power consumption for the 2M1D cell [11]. A comparison of the proposed memory cell and other recently developed memristor based memory cells [7-10] is shown in Table 1.

V. CONCLUSIONS

A new type of memristor based compact memory cell is proposed. This hybrid model used only 4 NMOS and 2 PMOS transistors along with a memristor and stores data from both directions. As the model does not need refresh during successive read operation, so less amount of power is required and the operating time becomes shorter than ambipolar based structure. The proposed model can be widely used due to its superior performance and linearity.

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