Cell Design and Comparative Evaluation of a Novel 1T Memristor-Based Memory

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***Abstract*— CMOS is expected to soon meet the end of the Semiconductor Industry Technology Roadmap. This paper investigates the memristor as a post-CMOS component for memory design. The proposed cell requires one transistor and one memristor (i.e. 1T1M); this cell employs novel read and write mechanisms for improved performance. Initially, it is shown that differently from previous designs, the proposed scheme accomplishes a read operation that does not affect the memory state; this cell is assessed with respect to different parameters as related to its design (such as applied write voltage, memristor range and size). It is shown that at array-level, the write operation may still incur in a state change due to voltage degradation. A detailed assessment of the relationship between a linear array size (as dimension of a square memory array) and the cell parameters, is pursued. Moreover, a comparison with a DRAM cell (i.e. 1T1C) in CMOS is pursued; the advantages and disadvantages of DRAM versus memristor based arrays are then presented.**

***Keywords*— Memristor, DAC, nanotechnology, DRAM, flux/charge.**

I. INTRODUCTION

The Memristor is a basic circuit element that was first postulated in 1971 [1]; due to the inability in its fabrication, the memristor was not investigated for more than three decades till researchers at HP Labs disclosed [2] [3] the discovery of the so-called "missing" element (i.e. the memristor) in 2008. HP Labs have provided a full device characterization inclusive of basic theory and fabrication; this has therefore opened new avenues of research by which novel circuits can be implemented to exploit the operational characteristics of this circuit element [3].

This is particularly relevant today, as CMOS is expected to meet the end of the Semiconductor Industry Technology Roadmap. Over the last thirty years, CMOS has been the dominant technology with a steady shrinking in feature size [4]. However, the quantum effects at such reduced feature size and the limitations in fabrication technology present serious hurdles in the nano ranges; new active devices such as Carbon Nano Tube FETs, Quantum-dot Cellular Automata (QCA) and Single Electron Transistors (FETs) have been proposed as emerging technologies [6].

The memristor is considered as a very promising emerging technology (mostly for switching) due to its excellent characteristics. Implementations have been proposed for binary and multi-valued memories as a memristor can be programmed at intermediate levels for a fine resolution in programmable resistance [4]. Therefore, this feature makes the memresistor a good candidate for circuit design. There are several additional advantages of using memristors when designing high performance circuits. One of the most important and obvious advantages is that while still at an early stage of development, the memristor has a nanometric dimension; it is projected that within the next few years, fabrication methods may yield memristors of 5nm size. Moreover as memristors are not fabricated on a single crystal, they can be stacked and used in 3D architectures [8] and when used with CMOS devices, they provide an opportunity to design hybrid nanoelectronic circuits .

The application of memristors to semiconductor memory technology has been widely advocated in the technical literature [11]. Memory cells that utilize different schemes have been proposed; these circuits have shown that memristor-based cells have a significant potential for new memory architectures in the nanometric ranges [11]. Memristor-based memories can be used for multi-level operation to exploit the switching features of the memristance. However, the limitation imposed by the disturbance due to the read operation must be considered in the design.

This paper addresses the fundamental circuit-level characterization of a memory consisting of the simplest cell configuration, i.e. one transition and one memristor (1T1M). A novel scheme is employed in the cell to avoid the loss of data due to the read operation; this scheme employs a pulse based signal as input to the 1T1M cell. The performance of the 1T1M cell is extensively evaluated and compared to a CMOS DRAM cell (i.e. 1T1C); extensive simulation results for cell operation under the variation of different parametric features are presented, so that a comparative assessment can be made. Array-level design issues are also considered; it is shown that features such as memristor size, the applied voltage and the voltage across the memristor can be used to achieve an increase in memory array dimension when considering the write 1

operation (as incurring in a degradation of the voltage across the memristor when a state change occurs in the stored data).

II. Review

The four circuit variables that define circuit theory, are charge, flux, current and voltage; these four variables account for the six possible (two-variable) combinations, out of which only five of them (as relations) are known and well understood. However, there is no circuit element that defines the relation between charge and magnetic flux. Chua theorized this fourth fundamental element in 1971 [1]; he named this element *memristor*, i.e the memory resistor. This element completes the missing circuit analogy, such that a memristor is characterized by its *memristance function* (M) given by the ratio of the change of flux to the change of charge, i.e.

$$d\phi = M*dq \quad (1)$$

From Faraday's law of induction, the magnetic flux is a time integral of the voltage and the charge is the time integral of the current. Thus, a memristor is a charge/flux dependent element that exhibits a hysteresis behavior. Scientists at HP Labs have achieved the first physical realization of a memristor; this memristor consists of a titanium dioxide film sandwiched between two platinum electrodes [2] (Figure 1).

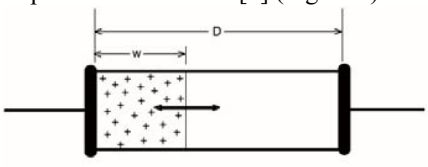

Figure 1: TiO_2 film sandwiched between two Pt electrodes

In the HP implementation, there are two layers of film, one has a slight depletion of oxygen atoms. The oxygen vacancies act as charge carriers, i.e. the depleted layer has a significantly lower resistance than the non-depleted layer. When an electric field is applied, the oxygen vacancies drift in the direction of the field, changing the boundary between the high-resistance and low-resistance layers. The application of a positive voltage at one end moves the oxygen ions to the other end of the film, thereby shifting the boundary between the doped and undoped film regions; however, the application of a voltage with opposite polarity reverses this phenomenon, thereby making this device to behave as a nanoscale potentiometer. Thus, the resistance of the film is dependent on the charge that has passed through it in a particular direction; this process can be reversed by changing the direction of the current. Based on the ionic mobility and the thickness of the thin film, the HP memristor is characterized by the following equations [3]

$$v(t) = \left\{R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right\} i(t) \quad (2)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \quad (3)$$

$$w(t) = \mu_v \frac{R_{ON}}{D} q(t) \quad (4)$$

where w denotes the length of the doped region (as function of time), D is the total length of the titanium dioxide layer, the off and on resistances are the extreme values of the memristor resistance. The range of memristor operation is therefore defined in terms of the location of the TiO_2 boundary [5], because the memristance depends upon the areas of the depleted and non-depleted regions in the film. The mobility depends on the applied electric field; once the electric field is not applied, then the boundary retains its state, thus fixing the areas and in turn defining the memristance at a particular state.

The conductivity of a memristor depends on the length of the doped region; if a sufficiently high charge/flux is passed through the memristor, then the oxygen ions spread over the entire film, the resistance decreases and the memristor is said to be in the ON state (with resistance given by Ron). The application of a different polarity voltage can reverse this phenomenon and if no doped region is present, then the memristor is in the OFF state with a high impedance (Roff) [3]. The boundary position in the TiO_2 film depends on the amount of charge flown through the memristor; this in turn depends upon the applied voltage and the frequency of operation. When the memristor is operated by gradually shifting the TiO_2 boundary, then it is said to be in the *active region* of operation. In the active region, the boundary is slowly drifted towards the saturation state and the memristor can be programmed as a fine programmable resistor. When the frequency and the magnitude of the voltage applied to a memristor drastically change the TiO_2 boundary across the ends of the film, then the memristor is said to be operating in the *saturation region*. As the boundary fluctuates between 0 and the full length of the memristor, the resistance varies from Ron to Roff. The values over which the resistance varies define the so-called *range of the memristor*, i.e. larger the film length or lower the conductivity of the non-depleted region are, greater is the range.

The memrisistor has received considerable attention over the last few years. For circuit design, the memristor has been widely advocated as a memory element [11], also for multi-level storage operation [12]. This is accomplished by using a reference (resistive) array, whose resistance values are predetermined and fixed. In this design, a comparator is used to compare the resistance of the memristor with a resistor in the array. As a memristor can attain a very high resistance, the required resistive array may cause a large power dissipation; moreover, the provision of a comparator in the cell may result in a considerable area overhead. In [11], the fundamental electrical properties of a memristor are encapsulated into a set of compact closed-form expressions for characterizing a non-volatile memory. Moreover, the design, basic (read and write) operations, data integrity and noise-tolerance of these memory circuits are also established. In the design of [11], a memristor is read or written by directly forcing the input voltage source into the memristor itself and comparing it with the reference; so, this ternary memory requires three voltage levels (0, V_{DD}, and $V_{DD}/2$) and therefore, an additional voltage line is needed, i.e. area and power dissipation are considerably increased.

III. Proposed Memory Cell

By exploiting the memristor scheme presented in [11], the novel design of a memristor cell (consisting of a single

memristor and a single transistor) is shown in Figure 2. This memristor cell design is analogous to a CMOS DRAM cell; it consists of a transistor and a memristor as memory element (in place of the capacitor of a DRAM). A *read terminal* (readIN) is attached to one side of the memristor; this terminal is utilized by a novel read mechanism (as described later). The memristor is the memory element; the gate of the transistor is connected to the write_select (wordline) terminal, while the drain is connected to the bitline. The source of the transistor is connected to one side (terminal) of the memristor; the other side of the memristor is connected to the readIN signal for the control of the read operation, hence this is a 1T1M cell.

Figure 3 shows n 1T1M memory cells (C0, C1…..Cn) in a linear array (with control circuitry). M1 and M2 are the write and read drivers which connect the bitline to the write and read buffers respectively. During the write operation, the write buffer is activated and the data corresponding to the desired memory state is placed on the bitline. The wordline of the memory cell is held high to write the value on the bitline to the memristor in the selected cell. The read driver is off during the write operation, so disconnecting it from the array. Vread_in (Figure 3) is also held low during a write operation.

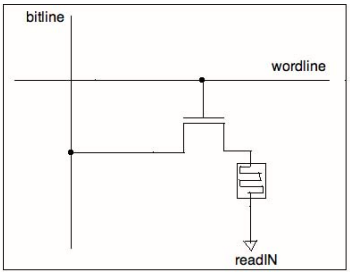

Figure 2: Proposed Memory Cell (1T1M)

The read operation executes by disconnecting the input buffer from the bitline (i.e. WR of the driver M1 is low). The read driver is then activated and Vread_in is applied to the cell selected to be read. The output voltage depends on the resistance across the selected memristor, which indicates the state of the memristance (Ron and Roff) that it holds.

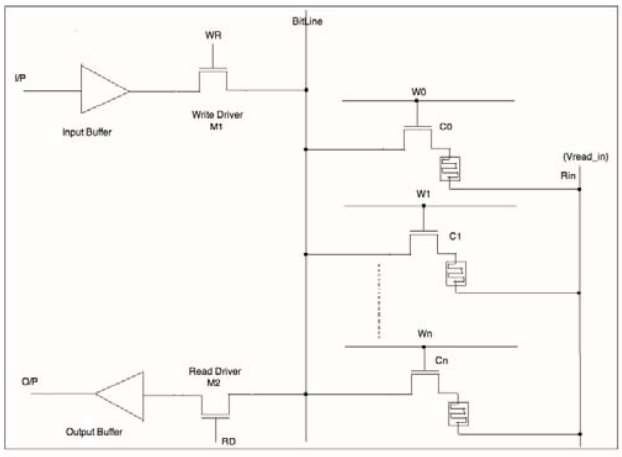

Figure 3: Memristor memory Array

As shown in Figure 3, the bitline is connected to the write and read drivers (i.e. transistors M1 and M2); hence, the input and output are buffered. The read operation is executed by applying the Vread_in input to the Rin terminal of the selected memristor cell.

To simulate a memristor and to validate its functionality, different SPICE-based models have been proposed in the technical literature [5][9][10]. These SPICE models are based on different window functions for behavioral simulation as the physical model of a memristor is only partially understood. In this paper, simulation is performed by HPSICE with the macromodel for a memristor of [5]; this macromodel has been shown to closely resemble the HP memristor parameters [3]. Unless specified otherwise, when simulating the read (write) operation, the following default values are applicable to the 1T1M cell: Roff/Ron = 10k/100 = 100, Vdd = 1v, 32 nm feature size, the input signal Vin has a frequency of 1 MHz (100MHz) for the write (read) operation.

A. Write operation

Assume that the memristor is initially in the Roff state (State 0); to perform a write operation, the write driver is activated by biasing, while an input signal is provided via the (input) buffer. During this operation, the bitline is high; the wordline of the selected memory cell is also high, then a current flows. When the transistor of the selected memory cell is in the saturation region, then the current flows through the source. The memristor conducts in the active region of operation (by selecting an appropriate frequency and voltage level for the input). So at completion of the write 1 operation, the memristor is placed in the Ron state (State 1). The same process is carried out for the write 0 operation. Figures 4 and 5 show the write operations of 1 and 0 respectively (assuming the memristor is initially in State 0): in both these figures starting from the top, the timing diagrams show the voltage across the memristor (Vmem), the wordline (Wi) of the selected cell, the applied input voltage (given by Vin at a frequency of 1Mhz and with a high pulse of width W) and WR.

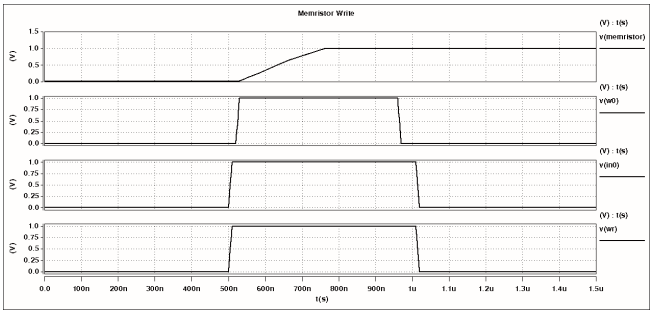

Figure 4: Write Operation (1)

B. Read operation

The read operation for the proposed memory is different from a conventional DRAM memory cell (in which the state is stored as a voltage in the capacitor); in the CMOS case, the bitline is precharged to read the DRAM cell. Charge sharing between the capacitor and the bitline is used to detect the state of the memory cell. However, a memristor stores the memory

state in form of a memristance (as determined by the voltage across the memristor, Vmem). In the proposed cell, the Rin terminal (connected to Vread-in at array-level) is used for the read operation, i.e. to read the state of the memristor, a read input pulse must be applied. The application of this signal changes the state of the memristor; the state can be retained if the flux flowing into the memristor is equal to the flux flowing out of the memristor [19]. This can be achieved by applying two consecutive pulses (one of negative polarity, the other of positive polarity), as part of the reading process for the memristor.

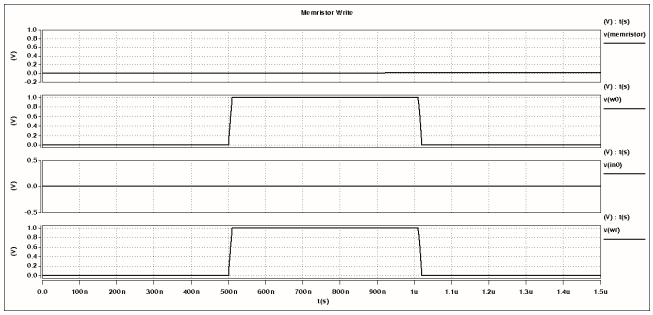

Figure 5: Write Operation (0)

For the read operation, the cell is selected by holding the wordline high and activating the read driver and output buffer. The write driver is off; so, it disconnects the input buffer from the bitline. Vread_in (consisting of two pulses) is applied to the Rin terminal of the selected cell as shown in Figures 6 and 7. In each of these figures, three timing diagrams are shown corresponding (from the top) to the output signal (at a frequency of 100MHz), Vread_in and Vmem. The negative pulse on Vread_in changes the state of the memristor; however, this effect is fully counterbalanced by the applied positive pulse (second timing diagram); hence, the original memristor state is preserved. This is an alternative arrangement to the traditional refresh mechanism commonly used in a CMOS DRAM cell.

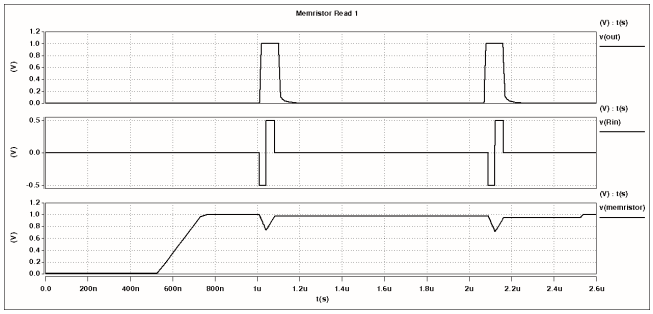

Figure 6: Read Operation (1)

Figure 6 (7) shows two consecutive read 1 (0) operations when Vread_in is applied for the cell of Figure 2. In both Figures 6 and 7, the threshold voltage is 0.5v; so a voltage below (above) 0.5v is considered to be 0 (1). As the read driver and the output buffer are enabled, an output is provided as state of the memory cell. This type of read operation is *functionally* equivalent to probing the voltage across the memristor, so it can be performed at a relatively higher frequency than the write operation. Moreover as the threshold voltage is given by 0.5v (i.e. equal to Vdd/2), the voltage levels of the two pulses of Vread_in are given by +0.5v and -0.5v respectively.

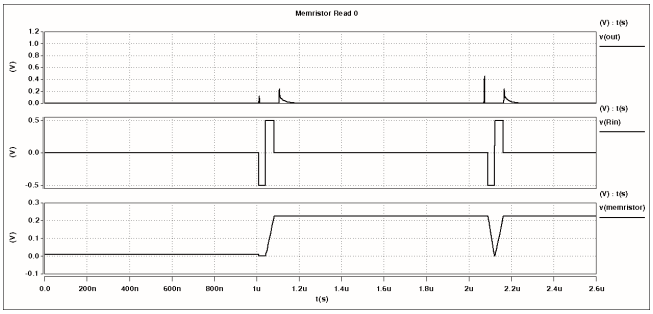

Figure 7: Read Operation (0)

Two types of delay could be evaluated for the above described read scheme. The first delay is the time elapsed between the application of Vread_in and the output of the read buffer; this is usually referred to as the read (or *access*) time of the memristor cell. The second delay is the time taken by the memristor to return to its original state. The second delay is not of significant importance because it is accomplished by Vread_in when reading the state of the memristor (and remaining at its original value). i.e. it is already included in the access time. Hence, only the read (access) time is considered in more detail hereafter.

IV. EVALUATION OF 1T1M CELL

In this section, the evaluation of the proposed memory cell (1T1M) is pursued. Simulation has been performed using a CMOS 32nm process with the memristor model of [5] at Vdd=1v. Unless otherwise specified the following default values have been used: Roff=10k , Ron=100, Roff/Ron (α) = 100 (memristor range ratio), memristor length (D) of 10nm, CMOS transistor sizing (β) = 2.5, Vin = 1v=Vdd, room temperature (27 ^{0}C).

A. Design parameters

Figures 8, 9 and 10 show the write and read times (in ns) on the y-axis by varying Vin, the driver width size ratio (M1/M2) and the feature size on the x-axis respectively. Figure 11 shows the write time (y-axis) by varying the memristance ratio (i.e. Roff/Ron (α)). The write/read times show a nearly inverse linear relationship with the applied voltage (i.e. Vin=Vdd) and the driver width and a linear relationship with feature size. Moreover as expected, the read time substantially increases with an increase in the memristor range ratio (i.e. as result of an increase in Vmem).

B. PVT variations

PVT (Process, Voltage,Temperature) variations affect the performance of the proposed memory cell (read and write times); Monte Carlo simulation has been used to assess their impact. A Gaussian distribution with 3 sigma variation of 5% (positive and negative) is used for the three parameters from

the previously specified nominal values. Simulation has found that there is no significant change in read/write times due to temperature variation. Figures 12 and 13 show the effects of process and (input) applied voltage variations on the read and write times of the memory. Among these variations, the most significant one is caused by the applied voltage, i.e. an increase (decrease) in voltage results in a decrease (increase) in operational performance (in terms of percentage, the write time is more affected due to the input voltage dependency on Vdd).

V. CELL-LEVEL COMPARISON

This section presents a detailed comparison between the proposed memristor-based memory cell (1T1M) and a CMOS DRAM cell (1T1C, as shown in Figure 14). It should be pointed out that comparisons for area and power are not presented; both the 1T1M and the 1T1C utilize one transistor (with equal characteristics) and [11] [19] have shown that a memristor requires less area and dissipates less power than a capacitor (at the values considered hereafter).

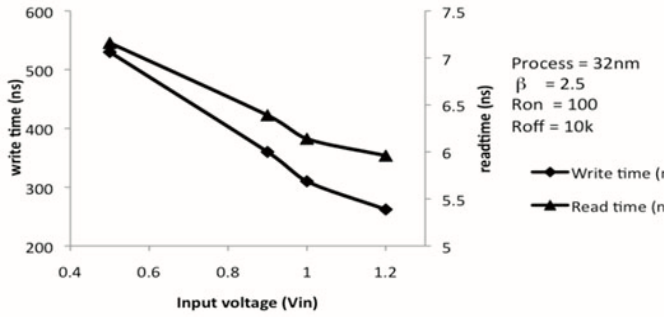

Figure 8: Applied voltage Vs Read/Write time

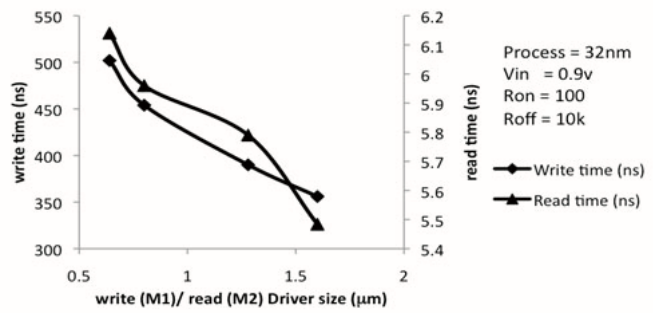

Figure 9: Driver width Vs Read/Write time

Figure 10: Feature size Vs Read/Write time

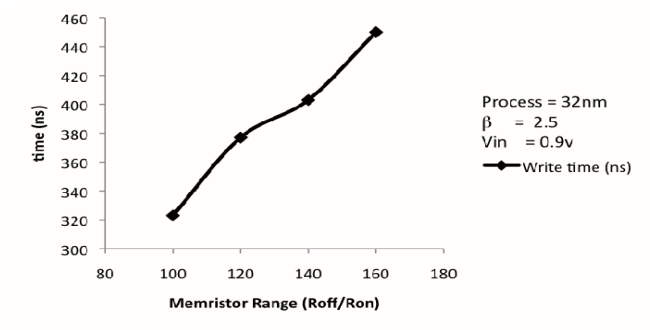

Figure 11: Memristance range Vs Write time

Figure 12: PVT (Process) variation

Figure 13: PVT (Applied Input Voltage) Variation

Table I shows the simulated results for the read/write times of the 1T1C DRAM at different feature sizes using the Predictive Technology Models of [7]; the 1T1C cell (Fig 14) is simulated with a load capacitance of 10fF as representative of today's memory products .

1) Read/Write times

The write time of a memristor-based memory is higher than CMOS. During the write operation, the oxygen vacancies in the film are moved depending upon the applied voltage. The doped region has a low resistance Ron (100) and the undoped region has a high resistance Roff (10k); the Roff-Ron ratio (100) is large and so, considerable amount of time is required for writing; this is particularly severe when a state change occurs. (A) For a 1T1C memory the write operation requires to charge the capacitor, this is faster than the resistive-based process of the 1T1M. (b) For the read operation, the 1T1M has the highest performance, i.e. at 32nm ~ 6 ns compared to ~ 27ns for the 1T1C. Hence, the proposed 1T1M should be used for memories in circuit applications in which read operations

are more frequent than write operations, such as FPGA and flash memories.

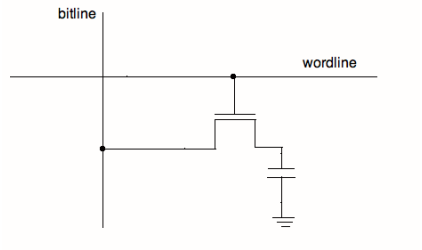

Figure 14: 1T1C DRAM Cell

TABLE I. DRAM CELL (1T1C) READ/WRITE TIMES

Process	Write Time (ns)	Read Time (ns)
16nm	76	23
32nm	80	27
45nm	83	31
65nm	87	34

2) Read stability

Read stability is defined as the feature by which the state of a memory can be correctly retained following multiple read operations. The logic value of a memristor-based memory is based on the memristance and its range. This depends on the ON or OFF state of the memristor. Reading the 1T1M cell can be achieved by probing the state of the memristor through the output buffer; this operation retains the memristor state using the proposed mechanism of two consecutive pulses on Vread_in. In CMOS, the usually small and weak signal on the capacitor must be probed by large and relatively high current drivers to produce an output signal. Being a slowly destructive process (due to leakage), the read operation requires refresh capabilities [8]. Also due to the large memresistance ratio, 1T1M offers a better read stability than a CMOS DRAM because a CMOS DRAM has a very weak signaling due to the small charge stored in the capacitor.

3) Endurance

Endurance is the characteristic that relates to the total lifetime of a memory i.e. the duration for which the memory can be repeatedly and reliably used for read/write operations. Memristors are not still functionally reliable; [2] has reported that a memristor can operate only up to 10^{10} write cycles. This remains a major concern as the long viability of a memristor-based memory (also compared with existing CMOS DRAMs) requires endurance when used at high operational frequencies [8].

4) Retention time

Retention time is defined as the time for which the memory cell holds the correct stored value once written. Memristors are non-volatile and therefore they exhibit long retention times. HP has reported that its fabricated memristor is capable to keep the memory state for several years [3]. Figure15 shows the simulation results of a 1T1C DRAM (using 32nm feature size and a capacitor value of 10fF). The 1T1C cell is first charged to 1V (i.e. Vdd); the voltage across the capacitor is then monitored to ensure state retention. Figure 16 shows the simulation results for the 1T1M cell at 32nm feature size and memristor size of 10nm; it can be clearly seen that under this performance metric, the 1T1M cell has superior performance compared with the 1T1C DRAM cell.

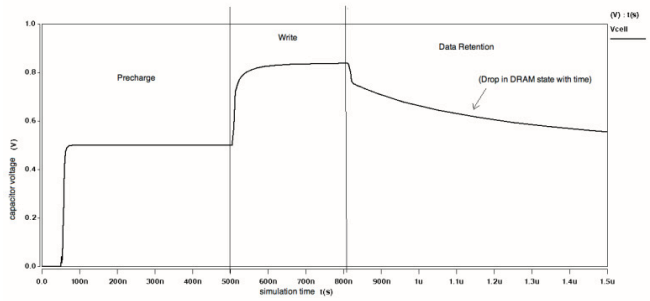

Figure 15: Data Retention of 1T1C

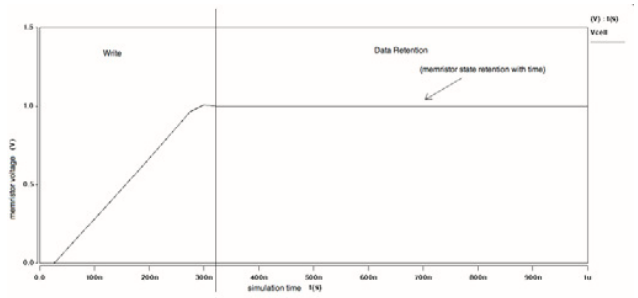

Figure 16: Data Retention of 1T1M

5) Capacity and area efficiency

One of the most important advantages of memristor-based memories is the higher density that can be achieved for design. At the end of the ITRS roadmap, a 16nm half-pitch CMOS DRAM cell is expected by 2019. At the early stages of development, the memristor size is 10nm and it is expected to reduce to 5nm by 2015. So considering the best and expected area efficiency for CMOS, the density of the memory array (so without support circuitry) is at most 44GB per square centimeter. However for memristors the density of the memory array is 466GB [8] per square centimeter, i.e. nearly 10 times better.

VI. ARRAY-LEVEL ANALYSIS

Next, the performance evaluation of the1T1M cell is extended by considering a linear memory array. This array (corresponding to a row or column of a square memory) has N memory cells; however, a large value of N can negatively affect the operation of the array. As shown before, the write operation has a considerably lower frequency than the read operation (1 MHz versus 100 MHz). As the read operation does not affect the memory state (accomplished by Vread_in in Figure 3), an array-level analysis must consider in more detail the write operation. Due to the change in memristance, only the write operation that changes the content of the 1T1M cell, is considered (i.e. the two cases in which the write operation results in no change, are of no significance); so for consistency with the results reported previously, the write 1 case is analyzed (i.e. assuming that the cell initially stores a 0). The write 0 case (i.e. assuming that initially the 1T1M cell stores a 1) is equivalent, because the value of the threshold voltage is assumed to be half of the supply voltage, i.e. Vdd/2.

Consider an array with N 1T1M cells (under the same conditions presented in Section IV at 32nm); Table II shows that when writing state 1, the memristor voltage Vmem of the selected cell decreases with array size and it falls below the 0.5v value of the threshold voltage when N=8.

TABLE II. MEMRISTOR ARRAY EVALUATION: WRITE 1

N	Memristor VoltageVmem
1	1
2	1
3	1
4	0.83
5	0.68
6	0.57
7	0.51
8	*0.44 (< 0.5v) Error*

So, simulation results show that the memristor state of a 1T1M cell can be correctly written up to N=7, i.e. at N=8 this voltage is 0.44 and the array operates incorrectly. So, the size of the *operating array* (i.e. an array operating correctly with Vmem higher than the threshold voltage for writing a 1) is given by N=7. To increase the size of the operating array (i.e. N>7), a possible design solution is the insertion of repeaters to provide a larger driving/restoring capability. However, this is not a viable solution, because it accounts to a significant area overhead. To increase the size of the operating array, different parameters as related to the memristor in each 1T1M cell (such as D) and the input signal (in terms of the pulse width W and the applied voltage), are analyzed next.

1) Memristor size (D)

The operation of the 1T1M cell is dependent on the size of the memristor. So to increase N beyond the value shown in Table II (i.e. 7), the memristor length can be changed (while keeping all other parameters constant). Figure 17 shows the values of operating array size (N) for the correct operation of the 1T1M cells.

2) Pulse width (W)

The pulse width of the input signal (denoted by W) significantly affects the amount of flux flowing into the memristor of a 1M1T cell; note that in this case, only W is changed, while the write frequency is kept constant to the default value. Figure 18 shows the plot of W versus the size of the operating array, confirming the strong effect of the pulse width at array-level operation.

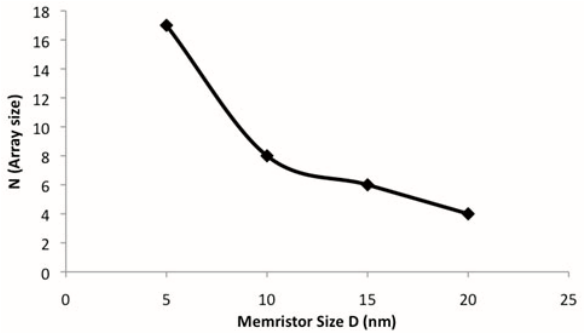

Figure 17: Memristor size (D) vs Operating Array Size (N)

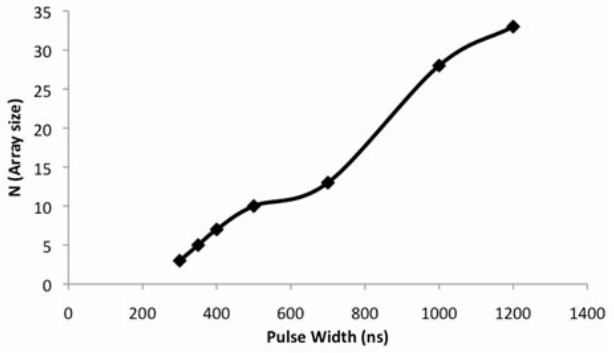

Figure 18: Pulse Width (W) vs Operating array size (N)

3) Applied voltage of write input

As the flux depends on the write input, a change in the applied voltage Vin (equal to Vdd and related to the threshold voltage given by Vdd/2) affects the performance of the memory array. Figure 19 shows the plot of the applied voltage versus the size of the operating array; while a stronger dependence on W is found, it is also evident that by raising the value of the applied voltage (and therefore the threshold voltage), the operating array size can be increased too. So while D is technology dependent, W and the applied voltage are cell parameters that can be changed for improved array operation.

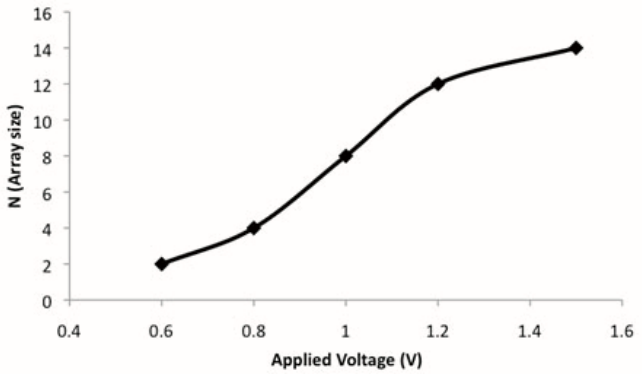

Figure 19: Applied voltage (V) vs Operating array size (N)

Therefore, Figures 17, 18 and 19 show that the performance of a memory array made of 1T1M cells largely depends on memristor size, W and the applied voltage: as the memristor size increases, N decreases, while by increasing W or the value of the applied input voltage, N is increased.

Table III shows these three parameters when optimized for 4, 8, 16 and 32 bit (linear array) sizes and their impact on the operation of the overall memory; this table has been generated by considering the memristor design parameters established throughout this section at a feature size of 32nm. Therefore, the increase in the size of an operating linear array requires technology advances (i.e. a decrease in the size of the memristor) as well as appropriate design considerations (i.e. the applied voltage and the pulse width of the write signal) for the 1T1M cell itself.

TABLE III. MEMORY ARRAY DESIGN, WRITE OPERATION

Operating Array Dimension (N)	D (nm)	W (ns)	Applied voltage (v)
4	15nm	250ns	0.7v
8	10nm	400ns	1v
16	10nm	800ns	1v
32	5nm	1000ns	1.2v

VII. CONCLUSION

This paper has presented the design and assessment of a memory cell consisting of one memristor and one transistor (i.e. 1T1M). The proposed memory cell utilizes a circuit arrangement that differently from previous schemes, it allows the read operation to retain unaltered the stored data. It has been shown that to improve performance, the write operation of the proposed 1T1M cell must be carefully considered. The scenario in which the stored data is changed as result of a write operation, has been analyzed; a parametric analysis (dealing with memristor size, memristance range and applied voltage) has been pursued to show that the write time has a proportional dendepency with the memristor range ratio and the feature size of the transistor. Table IV shows a comparative analysis with a CMOS DRAM cell (i.e. 1T1C) at 32nm feature size; the major drawback of memristor technology is the slow write time and endurance. However with the extensive research in memristor technology and the use of different materials for fabrication, these parameters are bound to improve in the future and a memristor memory can be seen as a competitor to existing DRAM memories at the end of the Technology Roadmap.

TABLE IV. MEMORY CELL COMPARISON AT 32NM

Feature	1T1C	1T1M	Advantage
Read Access	27ns	6ns	***1T1M***
Write	80ns	300ns	***1T1C***
Read Stability	-	+	***1T1M***
Endurance	+	-	***1T1C***
Retention Time	-	+	***1T1M***
Capacity/Area Efficiency	44GB/cm^2	466GB/cm^2	***1T1M***
Non-Volatile Operation	-	+	***1T1M***

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