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Gate Controlled 3-Terminal Metal Oxide Memristor

Eric Herrmann, Andrew Rush, Tony Bailey, Rashmi Jha

***Abstract*—We discuss the theory, design, fabrication, and testing of a three-terminal memristor based on thin film metal oxides. The fabricated device modifies a traditional $SrTiO_3$ thin film memristor to include a third control terminal. The results show the device conductance is continuous over three orders of magnitude, with significant retention and endurance, and comparatively low set and reset currents. The gate allows for continuous conductance state tuning, and allows for flexible architectures compared to traditional two terminal memristors by separating the read and write terminals.**

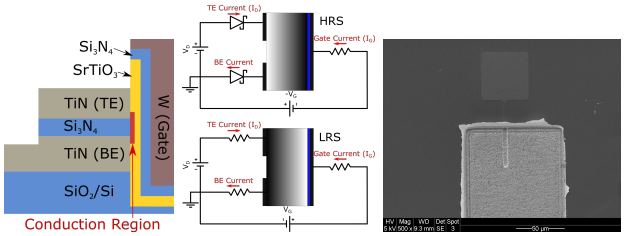
***Keywords*—Thin film devices, Memristors, Nonvolatile memory, Resistive RAM, Neuromorphics, Thin film transistors**

I. Introduction

Traditional two terminal (2T) Resistive Random Access Memory (RRAM) memristive devices based on thin film metal oxides (MO) have shown promise for non-volatile memory (NVM) applications as well as in neuromorphic architectures [1]. These 2T devices use the same terminals to read and configure the device, by keeping the read voltage below a threshold to retain device state. This approach makes multiple state devices and continuous resistive-state (RS) tunable devices hard to implement [2], [3]. One approach is to read and then program the RRAM repeatedly until the desired state is achieved [3], which has to be done sequentially in 2T RRAM. Additionally, setting and resetting these devices is more power consuming due to the device structure. In this work, we report our studies on 3-terminal (3T) RRAM devices that attempt to address these problems by using a third terminal to set and reset, allowing for a structure similar to the already popular flash architecture for NVM. Addition of a third terminal in RRAM also allows for much more versatile architectures in neuromorphic and other integrated-memory system applications.

II. Theory of Operation

One of the more popular theories of conduction mechanisms in MO is the movement of oxygen ions (O^{2-}) through the material, creating oxygen vacancies (V_O^{2+}). In the case of $SrTiO_3$ (STO), this behavior has been shown to explain the change in conductance in thin film memristors [4]. In the proposed device, a third terminal (referred to as gate) is used to apply a lateral electric field to modulate the V_O^{2+} concentration in the conduction region, changing the device state. Since the change in state is achieved by field-controlled modulation of the V_O^{2+} gradient in STO, programming current can be minimized with a gate insulator, allowing for reduced programming energy.



(a) (b) (c)

Fig. 1: (a) Device design cross-section. The leftmost TiN layers are the two read electrodes, and the W layer on the right is the device gate. (b) Diagram of the device operation. In the high-resistance state (HRS), the conduction region is depleted of V_O^{2+}, and the contacts are schottky. In the low-resistance state (LRS), the conduction region is saturated with V_O^{2+}, and the contacts are ohmic. (c) SEM image of 3μm interface device. Bright region is the W gate, light square at the top is the TiN top electrode (TE), and surrounding area is the TiN bottom electrode (BE).

The proposed device design cross-section can be seen in Fig. 1(a). The switching layer is STO, and the top and bottom electrodes (TE and BE) are TiN. STO was chosen for its generally accepted V_O^{2+} mobility [4], and TiN was chosen because it is relatively resistant to oxidation compared to other common electrode metals [5]. The STO region between the TE and BE is the conducting interface of the device. The W gate is parallel to the interface, and applies a field laterally to move V_O^{2+} in and out of the conduction region. The purpose of the Si_3N_4 layer between the gate and the STO is to reduce the gate (a.k.a write/erase) current. Ideally, the gate current should be minimal, and the STO should act as a slowly polarizing dielectric between the gate and the TE/BE. The depth of the largest fabricated device in this work is 100μm.

Fig. 1(b) shows the simple circuit diagram in the theorized high and low resistance states (HRS and LRS). Assuming that STO acts as a wide bandgap semiconductor with mobile V_O^{2+} [4], and that all contacts are non-reactive to STO, the change in the conductivity between the TE and BE can be achieved by two mechanisms. The first is an increase (decrease) in conductivity in the conduction region with higher (lower) V_O^{2+} concentrations due to mechanisms such as trap assisted tunneling, ohmic [4], or mixed-ionic electronic conduction. The second is an increase (decrease) in Schottky contact conductivity between TE/STO and BE/STO interfaces by accumulation (depletion) of V_O^{2+}. The control of oxide/metal contact resistivity by modulation of V_O^{2+} at metal interfaces has been well-explored in prior works for similar MO such as TiO_2 [6].

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III. Experimental Procedure

To fabricate the devices, 50 nm of TiN, 20nm of Si_3N_4, and 40nm of TiN were deposited sequentially onto an oxidized 4-inch p-Si substrate using RF magnetron sputtering. Using conventional photolithography and reactive ion etching (RIE) with CF4/O2 plasma, the top 2 layers were removed over most of the wafer. The protected top layer of TiN will be hereafter called the top electrode (TE), and the exposed TiN layer beneath will be called the bottom electrode (BE). A second aligned photolithography and subsequent RIE on the edge of the TE region exposed the silicon substrate. 40nm of STO, 20nm of Si_3N_4, and 40nm of W were then sequentially deposited using RF magnetron sputtering. These layers were made thicker to ensure thick enough sidewall deposition. The area outside of the etched region was then removed using photoresist liftoff. The sidewall of the etched region is the active area, and the W region defines the gate of the device. An SEM image of the fabricated device can be seen in Fig. 1(c). Several device sizes were fabricated, from 100μm interface width to 3μm interface width. All testing was done on a 100μm device. The vertical electrode separation was 20nm with a 40nm electrode height, meaning the cross-sectional contact from the electrode to the STO is 40nm$\times$100μm=4μm^2. Devices were measured in a Cascade Microtech MPS150 probe station using a Keithley 4200 Semiconductor Characterization System, fitted with a 4225 Pulse Modulation Unit.

IV. Results and Discussion

The fabricated devices were characterized for set and reset characteristics, state retention, endurance, and parasitic conductance. All measurements were taken at room temperature (RT) with 100μm interface devices. For all experiments, the BE was the reference ground.

Due to the low V_O^{2+} mobility at RT [7], it was anticipated that the device RS would vary in time. Therefore, the DC and transient V_G-I_D characteristics were measured by changing the gate voltage (V_G) at different rates. Fig. 2(a) shows the DC and transient characteristics, measured by sweeping V_G from -5V to 5V, with a constant read voltage (V_D) of 2V across the TE and BE, and measuring the corresponding read current (I_D). The final set state of the device at DC is fairly linear after it passes a threshold, resembling an n-channel MOSFET V_G-I_D characteristic, although unlike a MOSFET the conduction state is non-volatile. The fitted threshold voltage (V_T) from the linear region is 0.788 V with a linear transconductance of 2.96 nA/V beyond V_T. The transient curve has a higher V_T and nonlinear response indicating that the polarization state of the MO is lagging behind V_G. Fig. 2(b) shows the corresponding V_D-I_D curve of the device. Since there is no intentional body biasing in this device, the body is biased by the TE and BE, which in this test are V_D and 0V respectively. This can be seen in Fig. 2(b), where I_D rolls over with a higher V_D, presumably due to the lower net field across the STO with a positive V_D, causing unidirectional saturation.

A good demonstration of the non-volatile operation of the

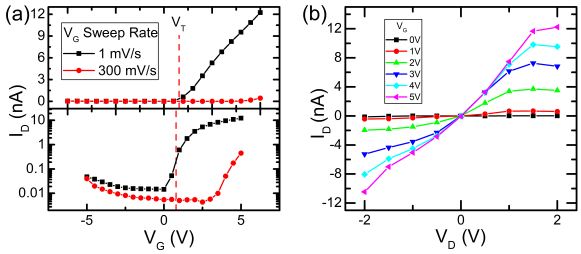

Fig. 2: (a) The DC and transient device current. This was taken by sweeping V_G at different rates (1mV/s and 300mV/s respectively), and measuring with a constant V_D of 2V. (b) I_D over V_D for several gate voltages, taken at DC (1mV/s).

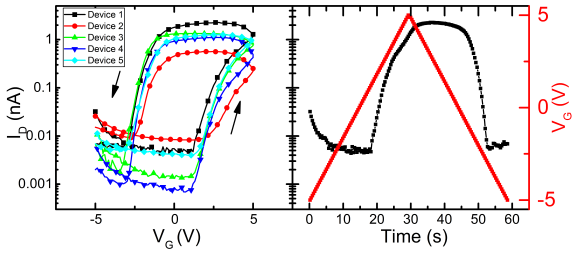

Fig. 3: The set/reset cycle of the device, with a 1V fixed V_D. The left plot is the V_G-I_D curve for 5 devices, and the right side is I_D and V_G over time of device 1.

device can be seen when sweeping the V_G more rapidly. In Fig. 3, V_G is swept from -5V to 5V, then back with a constant V_D of 1V, over the course of a minute on five 100μm devices. There is high variability between devices, the cause has been identified and will be fixed in future fabrications. On all devices, significant hysteresis in I_D was observed with a forward and backward V_G sweep. At V_G=0V, the low to high conductance ratio was as high as 1093, large enough to distinguish several unique resistance states. The small increase in current when the V_G approaches -5V is due to gate leakage (I_G). However, this current is small compared to the high-conductance state (LRS) current of the device. This test shows that the device exhibits continuous states, with programming done simultaneously while reading. The slow set rates can be attributed to the low mobility of V_O^{2+} at RT. This could be improved in future devices by maximizing the field in the STO either by minimizing the MO and gate insulator thickness or using a high-k gate insulator. This could also be achieved by modifying STO's properties through doping, annealing, or different deposition conditions, or using a different MO.

The device was characterized for power consumption and set/reset rates. Fig. 4(a) shows I_D and I_G over time with different V_G. In the I_D curves the device reaches its LRS state quickly, and then retains the state due to the persistent gate voltage. For low V_G, the current falls after reaching its peak. This is likely due to the complex fields in the STO, removing V_O^{2+} from the TE region due to a positive V_D. From the lower plot, we can see higher I_G when the device approaching its LRS, which is presumably due to the STO polarizing. The current falls once the device reaches equilibrium, this baseline current is then the gate leakage. From this data, the energy was calculated over the time it takes the conductance to change one order of magnitude, and is shown in Table 1.

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TABLE I: For different V_G, the maximum LRS and set times/energies for a 10× I_D change from HRS with V_D=1V, corresponding to Fig. 4(a)

V_G (V)	1	2	3	4	5
Max. LRS (pS)	55.8	141	659	1960	3560
Set Time (s)	26.9	5.33	4.79	3.72	1.68
Set Energy (pJ)	1.16	81.8	279	1480	3820

The corresponding reset measurements were also taken, with similar times and energies for a 10× change from LRS. With a -5V V_G, reset energy and time was measured as 1920pJ over 1.076s. Note that these energy measurements are inflated due to the large gate probe pad (capacitance) and leakage.

The state retention/decay of the device was tested by applying a 500ms, 5V pulse to configure the LRS, and a 500ms, -5V pulse to configure to the HRS. After each pulse, the gate terminal was left open, and the state was read over 140 seconds using a -1V and +1V V_D. As shown in Fig. 4(b), a positive V_D reinforces the HRS, while a negative V_D reinforces the LRS. State decay can be explained by two phenomena. The first is V_O^{2+} diffusion, which could naturally reset the device over time due to the induced V_O^{2+} concentration gradient. The second is V_O^{2+} drift, which is due to the intrinsic field in the STO generated by polarizing the STO when programming. Furthermore, the constant 1V V_D will pull O^{2-} back into the conduction region, increasing resistance. Conversely, a -1V V_D will reinforce the LRS and decay the HRS, by pulling V_O^{2+} back into the conduction region continuously. This property of the device is not desired, and could be improved by using reactive electrodes (instead of TiN), or using an MO with higher O^{2-} activation energy. Nevertheless, the non-volatile characteristics are evident in this experiment.

The endurance of the device can be seen in Fig. 4(c). This was taken by repetitive setting and resetting with 10V and -10V, 100ms V_G pulses, respectively for 128 cycles. The state was then read with a V_D of 1V. The device is able to switch reliably for these 128 cycles, and shows little degradation in the separation of states over this span.

The lower range of states shown in the above two experiments can be explained by the short pulsing, which is not long enough to span the full range of device states.

The last set of measurements were designed to quantify the effect of the I_D and I_G on device state. The fabricated device had a relatively leaky gate insulator, likely due to the Si_3N_4 layer between the W gate and STO being too thin. The I_G component is shown in Fig. 1(b) which consists of leakage through the gate insulator to the TE and BE. In future fabrications, this layer could be thicker to minimize I_G. Still, as can be seen in Fig. 5(a), the I_G to the TE ($-I_D$) is in the range of hundreds of pA, smaller than the I_D for this device. This leakage can also be observed in Fig. 3(a) at low V_G.

The TE to BE conductance with V_G=0V acts similarly to a traditional 2T metal/oxide/metal memristor [6], as would be expected. As can be seen in Fig. 5(b), the response is nonlinear and there is significant hysteresis, but it is important to note that the change in conductance is much less than is seen when configuring using the gate, even though V_D is being swept over the same range. Still, this effect is currently a drawback of the device since reading the device will affect the device state over time. This issue may be solved by reducing V_D. However, our device's characteristics with smaller read voltages could not be tested in this work due to low conductance of the device, which could not be read reliably with our measurement unit. Device conductance needs to be increased to make this solution plausible. Future work will attempt to solve this problem.

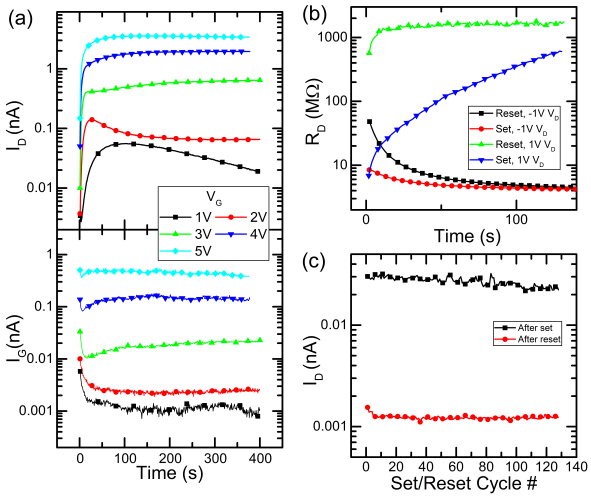

Fig. 4: (a) I_G and I_D over time with a constant V_D=1V, after set into HRS. (b) State retention for device following 5V, 500ms pulse for configuring to LRS, and -5V,500ms pulse for configuring to HRS. A constant V_D=1V/-1V applied to measure the state. (c) The set and reset states over 128 cycles of set/reset using a 10V/-10V, 100 ms pulse to V_G at each step, with V_D=1V.

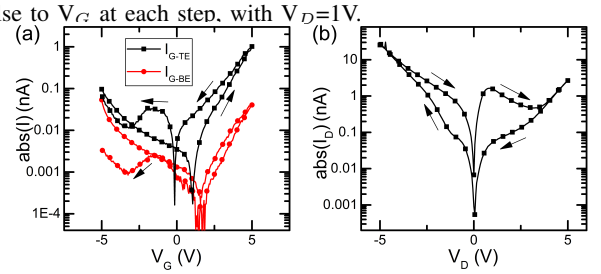

Fig. 5: (a) Current from the gate to the TE and BE with the TE/BE grounded, and V_G swept from -5V to 5V and back. (b) I_D with V_D swept from -5 to 5V and back, with V_G=0V.

V. Conclusion

A gated metal oxide RRAM device was fabricated with promising characteristics. The device exhibits continuous conductance states over 3 orders of magnitude controllable with a 5V gate voltage. Reading the device state can be done independently of programming, which gives designers the ability to obtain a resistive state with high accuracy. This could potentially allow for many-state memory, since the resistance state is easily tunable. This is also very useful for neuromorphic architectures.

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