# New Design of A Three-terminal Memristor Emulator

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***Abstract*—An emulator circuit is newly designed in this paper by making use of common off-the-shelf active devices for mimicking the dynamic behaviors of the three-terminal memristors (3T-MRs). The theoretical calculation shows that the equivalent memductance of the 3T-MRs emulator can be flexibly controlled by imposing excitation voltage with different amplitude, frequency and duty cycle on the third terminal. For the purpose of testing the controllability and emulation performance of the proposed emulator, simulation investigation is carried out based on PSpice software. The simulation results show good agreement with theoretical analysis, which confirms that the memductance of this 3T-MRs emulator can be conveniently controlled and can be utilized for further investigating the dynamic behaviors of 3T-MRs.**

***Keywords—Memristor; Three-terminal; Memductance; Emulator***

## I. INTRODUCTION

Memristive systems [1] were proposed in 1976 by Leon Chua and Sung Mo Kang defined as two-terminal passive nonlinear dynamical systems which possess the ability to record historical information by means of memductance. The main fingerprint which can be used for distinguishing the memristive systems [2] from other dynamical non-linear systems is the unique pinched hysteresis loops, which reflects the variable resistance called memductance dependent on the quantity of charge passed through.

It has been reported that memristors have high potentials to structure new functional devices as used industrial applications. A resistive random-access memory (RRAM) which can be switched between two different resistance states by applying proper terminal voltages is in fact a memristive system. RRAM is also identified as one of the emerging research devices (ERD) in the International Technology Roadmap for Semiconductors (ITRS) [3]. Technologically, memristors have been widely utilized for memory device [4-13], and many other applications in signal oscillators [14-17], logic and arithmetic circuits [18, 19], programmable analog circuits [20, 21], and emulation of dynamic neuron behaviors [22,23].

As highlighted in [24], over the past 50 years, many 3-terminal non-passive dynamical devices have been confirmed to show the memory effects which is in similarity to the memristive system. The gated three-terminal memristors based on TiOx [25] and Cu2-αS [26] have been developed and tested. The programming and erasing abilities of these gated memristors can be controlled by imposing proper voltage to the gate. The dynamic behaviors and control performance of three-terminal memristor is also a very attractive research topic recently emerging in neuron networks. In [27], a synapse chip of the neural network is formed by stacking CMOS circuits and three-terminal ferroelectric memristors (3T-FeMEMs). In [28], a supervised learning model is proposed, which enables the error back propagation for spiking neural network to suit the hardware implementation, of which the 3T-FeMEMS is used as an electric synapse device to store the analog synaptic weight. The results presented in [29] show that, the conductance of the biologically-inspired learning device can be modulated by the gate voltage regardless of the signal flow through the channel, and these characteristics can simultaneously realize pattern recognition and pattern learning like a brain. However, due to the lack of a practical 3T-MRs, researches related to the 3T-MR emulator are mainly carried out on the basis of theoretical analysis [24].

In this paper, a new emulator circuit is proposed to mimicking the dynamic behaviors of the 3T-MRs. By adjusting the amplitude, frequency, and duty cycle of the excitation voltage imposed on the third terminal, the memductance can be easily controlled on purpose.

## II. DESIGN OF THE 3T-MR EMULATOR

The new emulator of the 3T-MR is designed based on off-the-shelf electronic components. As shown in Fig.2, three op amps, one multiplier and four current feedback op amps (CFOA) are necessarily required for building this new 3T-MR emulator. The proposed emulator circuit can be divided into three parts, as enclosed by three dotted frames. The circuit inside the lower left frame is operated as an integrator and inside the right dotted frame there is an inverting adder circuit (IAC) structured by an op amp. The circuit inside the red upper frame can be operated as a two terminal equivalent flux controlled memristor emulator by connecting the output terminal of U6 to the terminal y of the CFOA U4. According to the operational function of CFOA (AD844), the voltage of terminal $x$ is equal to the voltage of terminal $y$. The following equation holds,

$$v_{u1} = \frac{R_2}{R_1} v_{AB} . \quad (1)$$

Based on the inherent input-output current performance of AD844, we have $i_x=i_z$, and $v_{u3}$ can be expressed by

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$$v_{u3} = -\frac{\varphi_{AB}}{C_1 R_1}, \tag{2}$$

where $\varphi_{AB}$ is the time integral of $v_{AB}$. In fact, U2 and capacitor $C_1$ are together operated as an integrator circuit. Generally, a resistor is connected with $C_1$ in parallel to eliminate the DC offset.

Op amp U5 is introduced to realize the Inverting Adder Circuit (IAC). By referring to the configuration of AD844, voltage of terminal $z$ is equivalent to the output voltage of terminal $p$. Hence, the output voltage of U5 can be described by

$$v_{u5} = \frac{R_5}{R_1 R_3 C_1}\varphi_{AB} - \frac{R_5}{R_4} v_s, \tag{3}$$

where $v_s$ is an adjustable DC current voltage.

By referring to the input-output function of AD633JN, the output voltage of terminal $w$ of AD633 can be given by

$$w = \frac{(x_1 - x_2)(y_1 - y_2)}{10} + z. \tag{4}$$

Hence, $v_{u6}$ can be further mathematically derived by

$$v_{u6} = \frac{R_6 + R_7}{10 R_6} v_{u1} v_{u5}. \tag{5}$$

Based on the actions of U2 and U4, the current $i_{MR}$ going through terminals A and B can be in fact decided by $v_{u8}$. Therefore, we have

$$i_{MR} = \frac{v_{u8}}{R_{13}}. \tag{6}$$

Also, $v_{u7}$ can be calculated by

$$\frac{v_C}{R_8} = -\frac{v_{u7}}{R_9} - C_2 \frac{dv_{u7}}{dt}. \tag{7}$$

Since the initial value of $v_{u7}$ is equivalent to 0, with respect to (7), $v_{u7}$ can be deduced by

$$v_{u7} = -\frac{R_9 v_C (1 - e^{-\frac{t}{C_2 R_9}})}{R_8}, \tag{8}$$

U8 is introduced to also realize an IAC, hence $v_{u8}$ can be expressed by

$$\frac{v_{u7}}{R_{10}} = -\frac{v_{u6}}{R_{11}} - \frac{v_{u8}}{R_{12}}. \tag{9}$$

By combining (5), (8) and (9), $v_{u8}$ can be further calculated by

$$v_{u8} = \frac{R_{12} R_9 v_C (1 - e^{-\frac{t}{C_2 R_9}})}{R_8 R_{10}} - \frac{R_{12} v_{u6}}{R_{11}}. \tag{10}$$

Based on (6) and (10), we have

$$i_{MR} = \frac{v_{u8}}{R_{13}} = \frac{R_9 R_{12} v_C (1 - e^{-\frac{t}{C_2 R_9}})}{R_8 R_{10} R_{13}} - \frac{(R_6 + R_7) R_2 R_{12} v_{AB}}{10 R_1 R_6 R_{11} R_{13}} \left(\frac{R_5}{R_1 R_3 C_1}\varphi_{AB} - \frac{R_5}{R_4} v_s\right), \tag{11}$$

Hence, the voltage-controlled memductance $W$ can be derived based on (11) by

$$W(v_{AB}, v_C) = \frac{i_{MR}}{v_{AB}} = \frac{R_9 R_{12} v_C (1 - e^{-\frac{t}{C_2 R_9}})}{R_8 R_{10} R_{13} v_{AB}} - \frac{(R_6 + R_7) R_2 R_{12}}{10 R_1 R_6 R_{11} R_{13}} \left(\frac{R_5}{R_1 R_3 C_1}\varphi_{AB} - \frac{R_5}{R_4} v_s\right) \tag{12}$$

It can be deduced from (12) that, for the special case of $t > 2.31 C_2 R_9$, the condition of $1\text{-}\exp[-t/(C_2 R_9)] > 0.9007$ is satisfied and $\exp[-t/(C_2 R_9)]$ is close to 0 with the increment of time $t$. Therefore, the memducance $W(v_{AB}, v_C)$ can be easily adjusted by tuning the input voltage of terminal $C$.

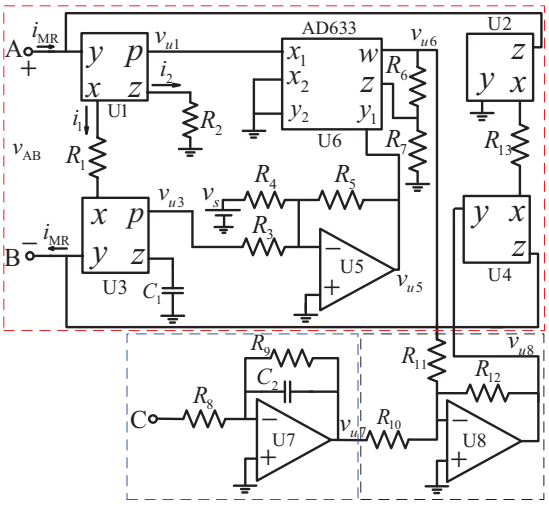


Fig. 1. Circuit schematic of the 3T-MR emulator

## III. Simulation Analysis

In order to validate the theoretical calculation and control performance of the 3T-MR emulator, the simulation circuit is built and tested by PSpice. This 3T-MR emulator possesses an extra controllabel electrode terminal C which can be used to adjust the memductance between the other two terminals of A and B. In order to comprehensively test the controllability and emulation performance of the emulator, the input voltage $v_{AB}$ with different shape and parameters are imposed on terminal AB, namely, the sinusoidal voltage, isosceles triangular voltage and the square voltage, respectively. At the same time, the input voltage $v_C$ is configured by the pulse voltage with different amplitudes to control the memductance and correspondingly verify the controllability performance of the terminal C. The parameters used for simulation testing are configured as $R_1$=51kΩ, $R_2$=$R_3$=$R_4$=100kΩ, $R_5$=10kΩ, $R_6$=100kΩ, $R_7$=91kΩ, $R_8$=100kΩ, $R_9$=1MΩ, $R_{10}$=15kΩ, $R_{11}$=1kΩ, $R_{12}$=1kΩ, $R_{13}$=1kΩ, $C_1$=100nF, $C_2$=470nF.

Firstly, a sinusoidal voltage of $2\sin(20\pi t)$V is used as the input excitation voltage. In addition, the pulse voltage $v_C$ with 10Hz frequency and 50% duty cycle are adopted to excite terminal C. when the amplitude $V_{Cm}$ are configured as 1V, 3V and 5V, respectively. The three Lissajous curves of $i_{MR}$ versus $v_{AB}$ are displayed in Fig.3, from which we can see that the pinched hysteresis loops (PHLs) behave as an inclined '8' and

are together passing through origin. Also, the PHLs can be comparatively shrunk by the diminution of $v_C$ amplitude. The amplitudes of $i_{MR}$ are measured as 0.0011, 0.00113 and 0.00117A, respectively, correspondingly to these three control amplitudes and can be further increased also by the increment of the amplitude of $v_C$. Note that, the phase error can be observed as shown in the dotted circle of Fig.3. As compared with that of Fig.4(b), the variation error of the PHLs can be attributed to the out-of-phase output of U8 due to the resistor $R_9$ connected with $C_2$ in parallel.

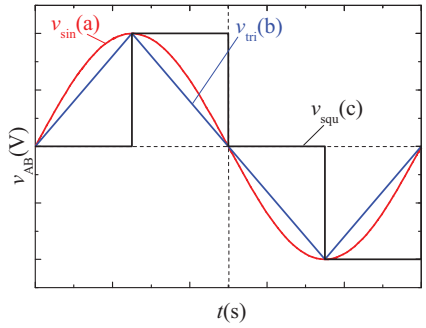


Fig. 2. Curves of input excitation voltages

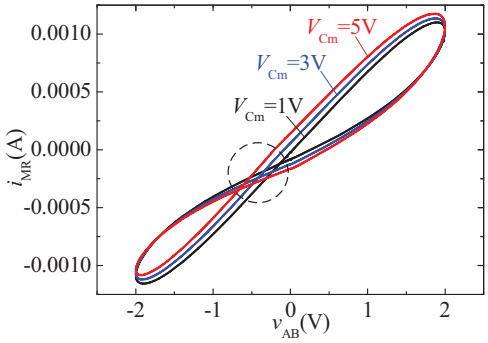


Fig. 3. The PHLs of the 3T-MR emulator excited by sinusoidal voltage

Likewise, three PHLs of $i_{MR}$ versus $v_{AB}$ under the condition of isosceles triangular excitation voltage $v_{AB}(t)$ across A and B are exhibited in Fig.4. The isosceles triangular voltage $v_{AB}(t)$ is configured by 10Hz frequency and 2V amplitude to testify the memductance behavior of the 3T-MR emulator and control performance of terminal C. The pulse voltage of $v_C$ with 10Hz frequency and 50% duty cycle is adopted to control the memductance via terminal C. The simulation results in terms of three different amplitudes $V_{Cm}$=1V, 3V and 5V are taken for demonstration to show the controllability of this emulator as shown Fig.4. It can be seen that, the triangular excitation voltage could lead to sharp terminals of the PHLs and the PHLs are inclined to $x$ axis by the decrement of control amplitude. The amplitudes of $i_{MR}$ are measured as 0.986, 0.940 and 0.899mA corresponding to these three amplitudes and can be further reduced also by the amplitude diminution of $v_C$.

When the input voltage $v_{AB}(t)$ is a square voltage with 10Hz frequency, 2V amplitude, and 25% duty cycle of high level and low level respectively, the curves measured as shown in Fig.5 clearly show the memory effect of the 3T-MR emulator. Three different amplitudes of the impulse voltage $v_C$ with 10Hz frequency and 50% duty cycle are adopted to test the controllability of the memductance. It can be seen that, for each given terminal voltage value $v_{AB}(t)$, two possible current values could be measured from the memristor emulator. The current $i_{MR}(t)$ could be abruptly changed and intensity of the variation is in fact dependent on the memductance value 'remembered' by the 3T-MR emulator. The amplitudes of $i_{MR}$ are measured as 0.00157, 0.00147 and 0.00139A respectively corresponding to $V_{cm}$ equal to 5, 3 and 1V. The current amplitude can be further reduced by decreasing the amplitude of $v_C$. Evidently, the PHLs are shrunk by reducing the amplitude of $v_C$. Simulation errors are observed as enclosed by the dotted circle and could be attributed to the phase error caused by the integrator circuit.

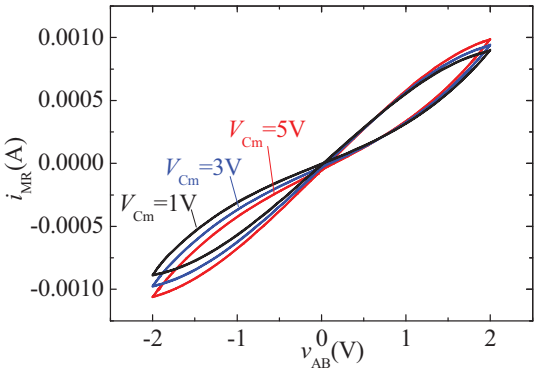


Fig. 4. The 3T-MR emulator excited by an isosceles triangular wave

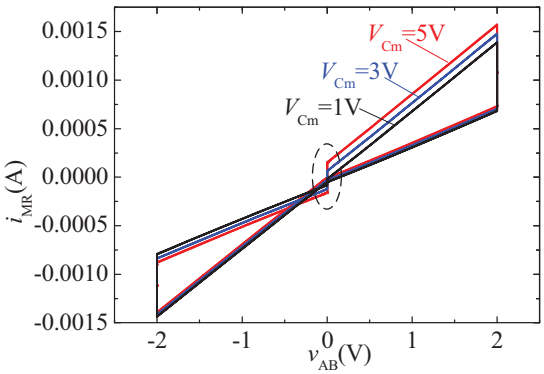


Fig. 5. The 3T-MR emulator excited by a square wave

For the purpose of further verifying the control performance of the terminal C, a narrow pulse voltage with different amplitudes, a narrow pulse voltage with 10Hz frequency and 2% duty cycle is adopted to excite terminal C, while terminal AB is excited by a sinusoidal wave. The amplitude of the excitation voltage $v_C$ is varied from 0V to 10V to test the memductance variation of the memristor emulator. In this section, the memductance related to the maximal positive value of excitation voltage is calculated based on measured data to reveal the behaviors of memductance variation, as shown in Fig.6. Evidently, along with the amplitude increment of $v_C$ from -10V to 10V with step 1V, the memductance can be decreased from 0.64 to

0.50mS. From this control process, it can be derived that the memductance can be easily controlled to the required value by adjusting the amplitude value of the pulse voltage of terminal C.

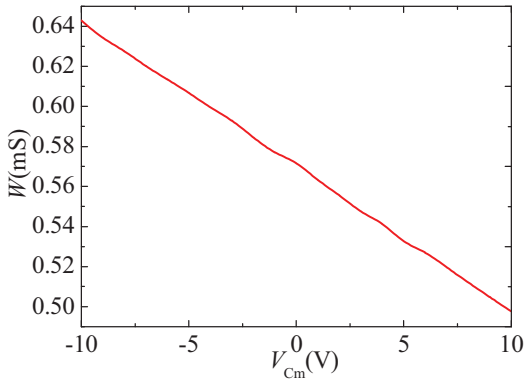


Fig. 6. Memductane versus the amplitude of pulse voltage $v_C$

A square voltage with amplitude of ±1V and 50% duty cycle and changeable frequency is employed for further testing the control performance of this emulator, while an unaltered sinusoidal wave is introduced to excite terminal AB. The variation curve of memductance corresponding to excitation frequencies from 4 to 20Hz is shown in Fig.7. It can be seen that the memductance can be decreased by the frequency increment of the pulse voltage $v_C$. Hence, the control performance and dynamic behaviors of the 3T-MR can be mimicked by this emulator circuit via properly configuring the circuit parameters. It is worth noting that, distortion can be observed when the frequency is further increased beyond 29Hz. This unexpected result can be attributed to the output saturation of the integral chips of either U3 or U7.

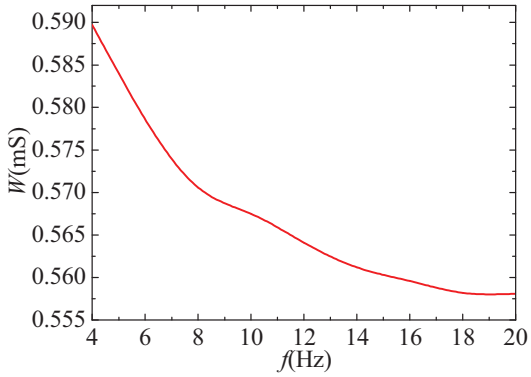


Fig. 7. Memductane versus different frequency

Likewise, the duty cycle of the voltage imposed on the terminal C is taken into account to test the dynamic behaviors of this 3T-MR emulator. The voltage $v_C$ is configured with the high level of 1V and the low level of 0V. The curve of memductance corresponding to high level of $v_C$ varied along with the increment of the pulse width from 0.001 to 0.099s is displayed in Fig.8. It can be seen that, the memductance can also be reduced by the increment of the pulse width.

All the above simulation results show that, by tuning the parameter of the control voltage applying to the terminal C, the memductance of this 3T-MR emulator can be regulated on purpose. Hence, the control performance of the 3T-MR device can be emulated by this new designed circuit.

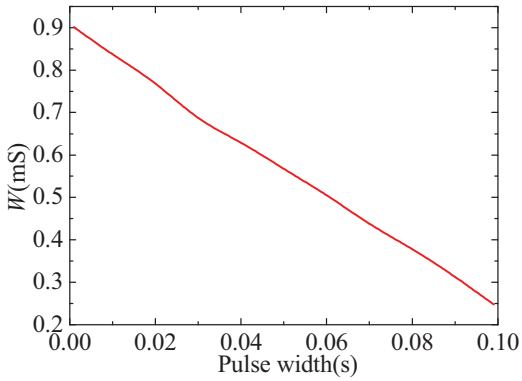


Fig. 8. Memductane versus the duty cycle of thh pulse voltage

## IV. Conclusion

A 3T-MR emulator is newly proposed and theoretically analyzed in order to show the memductance controllability of the three terminal memristors. By adjusting the frequency, amplitude, duty cycle of the excitation voltage imposed on the third terminal C, the equivalent memductance of the proposed 3T-MR emulator can be controlled. The simulation results related to different system parameters are measured and discussed, and show good agreement with the theoretical analysis. The dynamic behaviors of this new 3T-MR emulator deserve further research attention in consideration of wide potential applications of 3T-MR devices.

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