Welcome To My Presentation

My Presentation Topics is

Flip Flops & The Practical use Cases

Presented By

Tushar Sarkar

Student ID : 18CSE035

Second Year Second Semester

Department of CSE, BSMRSTU.

Content

- What is Flip flop?
- Types Of Flip Flop
- SR Flip Flop
- D Flip Flop
- JK Flip Flop
- T Flip Flop
- The Practical Uses of Flip Flop

What is Flip Flop?

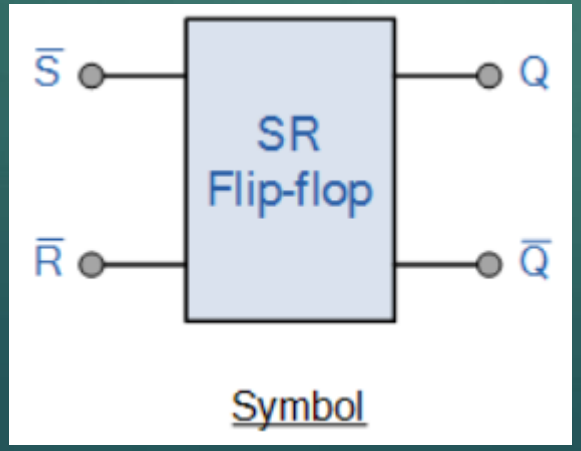
- A flip flop is an electronic circuit with two stable states that can be used to store binary data, bit 1 or bit 0.
- The stored data can be changed by applying varying inputs.
- The designing of the flip flop circuit can be done by using logic gates such as two NAND and NOR gates.
- Each flip flop consists of two inputs and two outputs, namely set and reset, Q and Q’.
- This kind of flip flop is stated to as an SR flip flop.

Types of Flip Flop

- Flip flop circuits are classified into four types based on its use, Namley-
  - SR-Flip Flop
  - D Flip Flop
  - JK Flip Flop
  - T Flip Flop

SR Flip Flop

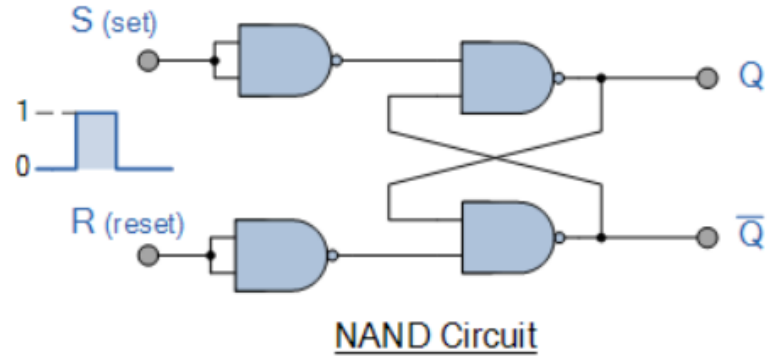
- The SR-flip flop is built with two AND gates and a basic NOR flip flop.
- The o/ps of the two AND gates remain at 0 as long as the CLK pulse is 0, irrespective of the S and R i/p values.
- When the CLK pulse is 1, information from the S and R inputs permits through the basic FF.
- When S=R=1, the clock pulse occurrence roots both the o/ps go to 0.
- When the CLK pulse is detached, the state of the FF is unstated.



Symbol

SR Flip Flop

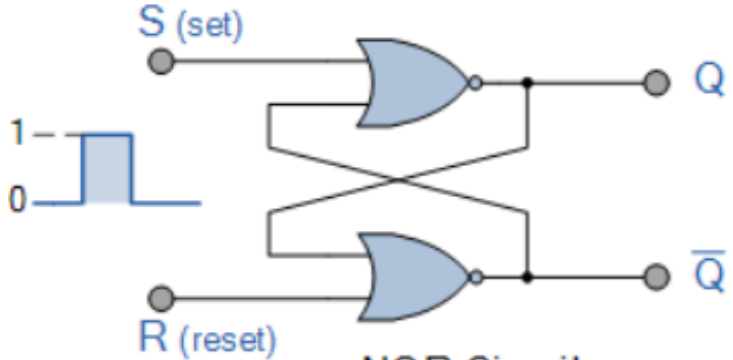
NAND Gate SR Flip-flop :



NAND Circuit

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	X (Invalid)	X

NOR Gate SR Flip-flop

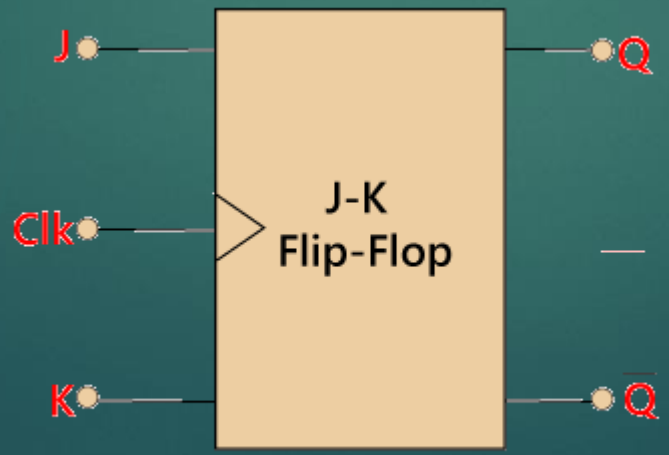


NOR Circuit

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	1	0
1	0	0	1
1	1	X (Invalid)	X

JK Flip Flop

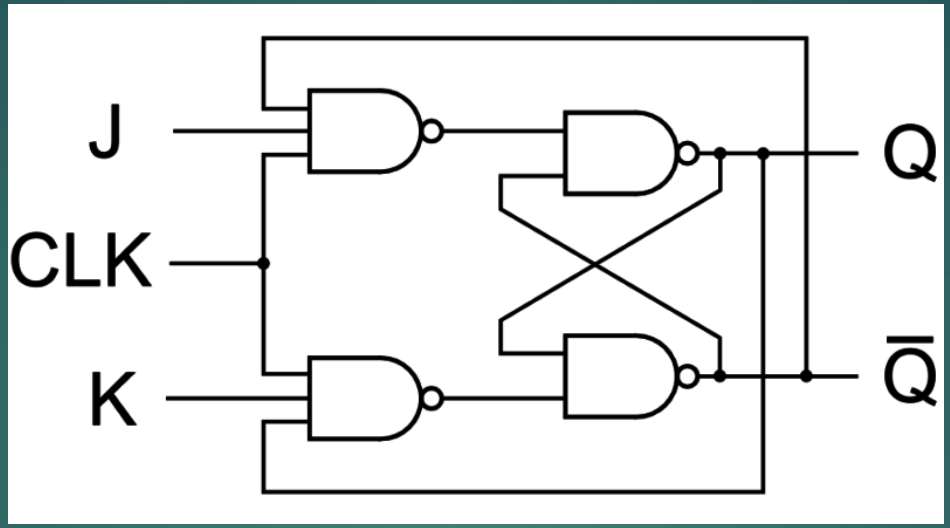
- A JK-FF is a simplification of the SR-flip flop. The inputs of the J and K flip flops behave like the inputs S & R.
- When input 1 is applied to both the inputs J and K, then the FF switches to its complement state. The designing of the JK FF can be done in such a way that the o/p Q is ANDed with P and.
- This procedure is made so that the FF is cleared during a CLK pulse only if the output was previously 1. In the same way, the output is ANDed with J & CP so that the FF is cleared during a CLK pulse only is Q' was previously 1.



Symbol

JK Flip Flop

JK flip Flop Logic Diagram:

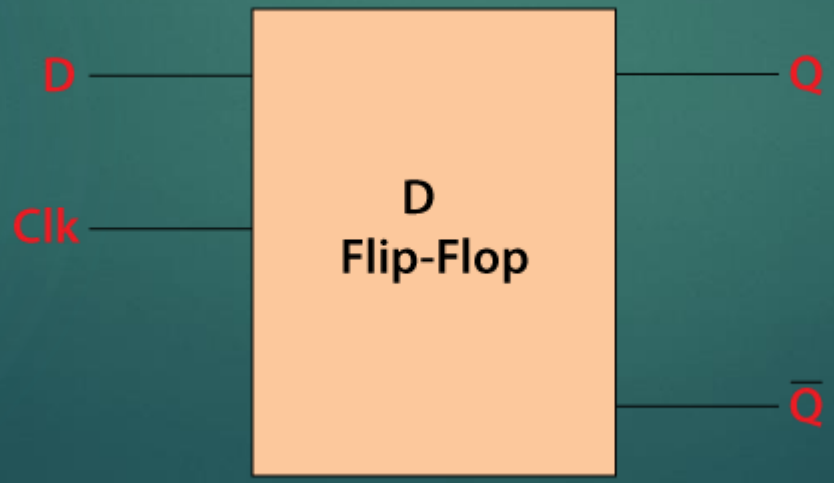


Truth Table for JK Flip Flop :

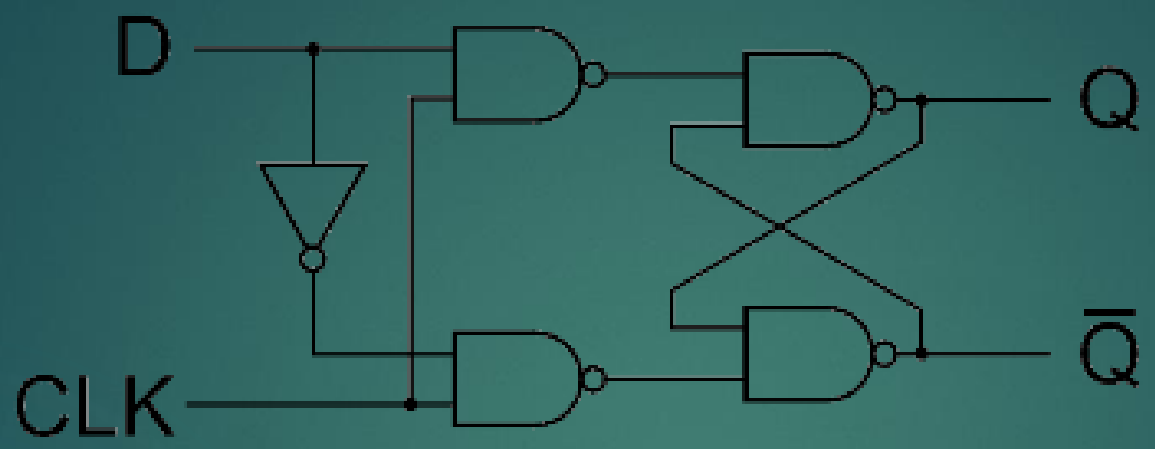
Input			Output		
Clk	J	K	Q	Q’	Status
↑	0	0	Q	Q’	No Change
↑	0	1	1	0	Reset
↑	1	0	0	1	Set
↑	1	1	Q’	Q	Toggle

D Flip Flop

- D Flip Flop also known as Data Filp Flop
- The D-input is sampled throughout the existence of a CLK pulse.
- If it is 1, then the FF is switched to the set state.
- If it is 0, then the FF switches to a clear state.
- The D flip flop will act as a storage element for a single binary digit (Bit)



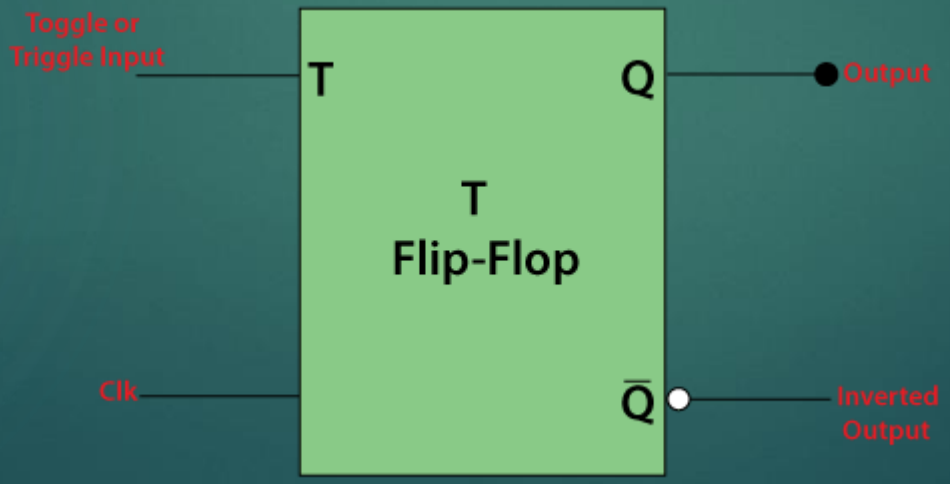
D Flip Flop



Input		Output	
Clk	D	Q	Q’
↓ >> 0	0	0	1
↑ >> 1	0	0	1
↓ >> 0	1	0	1
↑ >> 1	1	1	0

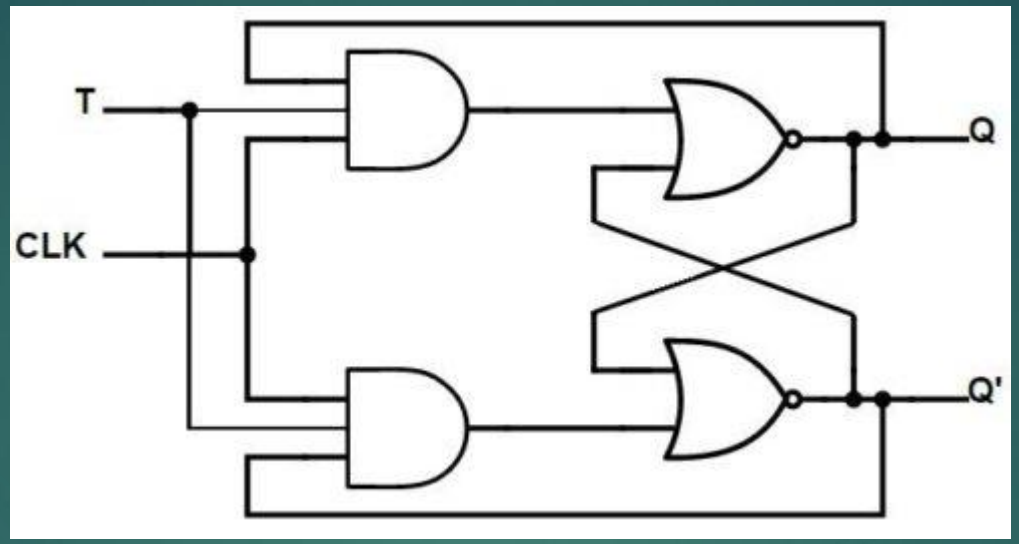
T Flip Flop

- The T-flip flop or toggle flip flop is a single i/p version of the JK-flip flop.
- The working of this FF is as follows: When the input of the T is ‘0’ such that the ‘T’ will make the next state that is similar to the current state.
- That means when the input of the T-FF is 0 then the present state and the next state will be 0.
- However, if the i/p of the T is 1 then the present state is inverse to the next state. That means, when T=1, then the present state =0 and next state =1).



T Flip Flop

T flip Flop Logic Diagram:



Truth Table for T Flip Flop :

Input		Output		
T	Clk	Q	Q’	Status
0	↑	Q	Q’	Hold
1	↑	Q’	Q	Togol

The Practical Uses of Flip Flop

- Counters-
  - Asynchronous counter
  - Modulo – n – counter
  - Synchronous counter
  - 2 – Bit synchronous counter
  - Applications of Counters
- Registers.
- Frequency Division.
- Data Transfer.

Thank You