Sinulator Code: C/C++/Assembly

 # MIPS-5-Stage-Pipelined-Processor

1.Fetch (IF):fetches an instruction from instruction memory. Updates PC.

2.Decode (ID/RF): reads from the register RF and generates control signals required in subsequent stages. In addition, branches are resolved in this stage by checking for the branch condition and computing the effective address.

3.Execute (EX): performs an ALU operation.

4.Memory (MEM): loads or stores a 32-bit word from data memory.

5.Writeback (WB): writes back data to the RF.

Instruction supported by MIPS processor:

1. add
2. addu
3. addiu
4. sub
5. subu
6. xor
7. mul
8. mulu
9. div
10. divu
11. beq
12. bne
13. beqz
14. bnez
15. lw
16. sw
17. move
18. nop