Tushar Malakar

Prof: Soumik Dey

CSCI 260.0001

June 6, 2018

Assignment 1

1. A) Performance

Instruction count = 500,000

CPI for A, B, C, D are 1, 2, 3, 4 respectively

Clock rate =

CPU clock cycle = instruction count \* CPI

CPU clock cycle A = (500,000 \* 30% + 500,000 \* 40% + 500,000 \* 20%) \* 1= 450,000

CPU clock cycle B = (500,000 \* 20% + 500,000 \* 20% + 500,000 \* 10%) \* 2 = 500,000

CPU clock cycle C = (500,000 \* 40% + 500,000 \* 20% + 500,000 \* 30%) \* 3 =1,350,000

CPU clock cycle D = (500,000 \* 10% + 500,000 \* 20% + 500,000 \* 40%) \* 4 =1,400,000

Total CPU clock cycle =3,700,000

CUP execution time = CUP clock cycle \* Clock Rate

= 3,700,000 \*

= 3,700,000 \* \* 10-9

= 1.057\*10-3 ms

So, Performance = = \*10-3 = 945.98 Seconds

We know that performance is 1/execution time, and to figure out the execution time the we are given the number of instructions count, CPI, and clock rate.

B) Performance = CPU speed \* CPU instruction per cycle \* CPU cores

Performance of T1 = 3.5 GHz \* (1/ (0.30\*500,000 + 0.2\*500,000 + 0.4\*500,000 + 0.1\*500,000)) \* 300

= 3.5 GHz \*(1/1,150,000) \* 300

= 9.13 \* 10-4 GHz

Performance of T2 = 3.5 GHz \* (1/ (0.40\*500,000 + 0.2\*500,000 + 0.2\*500,000 + 0.2\*500,000)) \* 200

= 3.5 GHz \*(1/1,100,000) \* 200

= 9.55 \* 10-4 GHz

Performance of T3 = 3.5 GHz \* (1/ (0.20\*500,000 + 0.1\*500,000 + 0.3\*500,000 + 0.4\*500,000)) \* 300

= 3.5 GHz \*(1/1,450,000) \* 300

= 7.24 \* 10-4 GHz

2. A.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Clock | CPI | Instructions |
| P1 | 4 GHz | 0.90 | 5.0E9 |
| P2 | 3 GHz | 0.75 | 1.0E9 |

Execution, P1 = = 1.125 sec.

Execution, P2 = = 0.25 sec.

Performance, P1 = = = 0.88

Performance, P2 = = = 4.00

Clock rate of p1> clock rate p2

But performance of p1 < performance p2

So, we can conclude that bigger clock not necessarily is going to better performance.

B.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Clock | CPI | Instructions |
|  |  |  |  |
| P1 | 4 GHz | 0.90 | 1.0E9 |
| P2 | 3 GHz | 0.75 | ? |

Performance, P1 = = 0.225 second

Instruction needs for p2 = = 9\*109 = 9.0E9 instruction

The fallacy is wrong that the larger numbers of instructions needs larger CPU time, Because p2 has more instructions.

C. Mips P1(millions of instructions per seconds) = = 4,444.44 = 4.44 \* 103

Mips P2(millions of instructions per seconds) = = 4,000.00= 4.00 \* 103

Mips P1  > Mips P2

D. MFLOPS (millions of floating-point operations per second) = No. FP operations / (Execution time \* 1E6)

MELOPS, P1 = 0.5 \*109 \* 4 \* 0.9

= 1.8 \* 109

MELOPS, P1 = 1.0 \*109 \* 0.75

= 2.28 \* 109

Performance, P1 = = 1.128 second

Performance, P2 = = 0.28 second

Mips, P1 = = 1.6\* 103

Mips, P2 = = 9\* 103