

# All-Digital Delay-Locked Loop-based Frequency Multiplier Operating from 4.0GHz to 5.6GHz

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**Abstract**—In this paper, a high speed, small area and highly reliable frequency multiplier based on an all-digital delay-locked loop (ADDLL) implemented with TSMC 65nm CMOS technology is proposed. A comparison between the two multiplication factors of 40 and 20 for the proposed edge combiner is also presented. The proposed ADDLL uses a 5-bit up/down counter to control the digital delay line. The delay difference is achieved with 3ps in the proposed design based on a post layout simulation. The simulated operating frequency range is between 100MHz to 140MHz for a multiplication factor of 40; and 220MHz to 240MHz for the multiplication factor of 20. The output signal in a frequency range from 4.0GHz to 5.6GHz can be generated. Based on the simulation results peak-to-peak jitter is 28.2ps and 22.2ps for the output signal with a frequency of 4.88GHz and 4.5GHz while the DLL operates at 122MHz and 225MHz, respectively.

**Keywords**—All-digital delay-locked loop, minimised jitter, broad frequency range, diminished design size.

## I. INTRODUCTION

With taking advantage of improvement in semiconductor process, the microprocessors and system on chips (SoC) have been more complex in recent days. Maintaining these devices in optimum conditions gets more challenging. To achieve reliable performance for the SoC, multiple frequency generating blocks are required to drive the low oscillating frequency. Therefore, a phase-locked loop (PLL) is utilised to generate the required clock in order to alter the output frequency. Conventional PLL suffers from multiple issues including structural complexity, large area, huge power dissipation and high peak-to-peak jitter. An alternative solution to PLLs is provided by delay-locked loops (DLL) which can overcome the drawbacks of the PLL. DLL does not suffer from stability issue as it is first order system. It brings multiple advantages such as power consumption and chip size occupation as well as low design complexity [1], [2]. DLL can be used in many applications such as buffer deskewing, delay compensation, clock and data recovery systems, frequency synthesiser and multiple applications which are related to integrated circuits (IC) [3]. DLLs have two sub-groups which are analogue and digital DLLs. Both types share the similar blocks like phase

detector (PD), delay line, and its dedicated controller. The conventional analogue DLL has a voltage-controlled delay line (VCDL) which can be used to generate high output frequency via multi-phases signal by delaying input clock. On the other hand, digitally-controlled delay line (DCDL) is used in digital DLL [4]. The analogue DLL provides lower jitter compared to the digital DLL, at the expense of higher current drawing, larger design size and extended locking time.

The Digital DLLs are splitted into four categories: register-controlled DLL (RDLL), time-to-digital converter (TDC)-based DLL, counter-controlled DLL (CDLL), and successive-approximation register (SAR)-controlled DLL. RDLL adjusts the delay time by utilising shift registers which can shift the control bit in two directions [5]. RDLL can easily track any pressure, voltage and temperature (PVT) variation as it is a closed-loop system. However, it requires a long locking time, large design size, and larger power dissipation. A time-to-digital converter (TDC)-based DLL also occupies large size and draws high current due to the structural complexity [6]. CDLL is a closed-loop system [7], where elements of the delay line are designed in binary-weighted method, and up/down counter is placed as a controller. Compared to RDLL, CDLL achieves a better delay resolution with smaller number of delay cells.

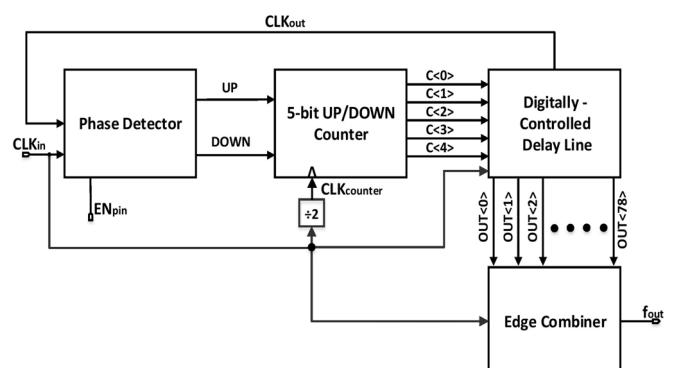


Fig. 1. The proposed ADDLL-based frequency multiplier.

Therefore, it also leads to a lower power dissipation. The SAR-controlled DLL is an open-loop system and it cannot follow PVT variations after the correct locking is found [8],[9].

A fully digital architecture for a DLL is proposed in this paper for the application in a frequency multiplier. This ADDLL design features a short locking time, high operating frequency, and small on-chip area. The proposed ADDLL is implemented as a counter-controlled DLL to alter delay time of the DCDL.

## II. ADDLL ARCHITECTURE

In this section the proposed ADDLL architecture is described. Fig. 1 presents the general structure of the proposed ADDLL. It consists of phase detector (PD), 5-bit up/down counter, DCDL, and an edge combiner. Once the input clock signal  $CLK_{in}$  rises, the phase inequality between  $CLK_{out}$  and  $CLK_{in}$  is determined by the PD. It generates UP and DOWN signals after getting a signal from  $CLK_{out}$ . The results are then sent to the 5-bit up/down counter to generate a control word C<0>to C<4> which changes the state of the DCDL. All 80 or 40 equidistant phases are fed to the edge combiner where the multiplication happens, and high output frequency can be achieved. In the following, the functional units of the frequency multiplier DLL are described in detail and then, the complete circuit is elaborated.

### A. Phase Detector

The PD can be performance limiting component in any type of DLL as it regulates the complete phase resolution of the system. Thus, the special attention has been considered to achieve enough resolution. As shown in Fig. 2, the PD uses two typical Yuan-Svensson D flip-flop (DFF), in addition to the reset pin ( $EN_{pin}$ ). True-single-phase-clocking (TSPC) are used in various designs [9]. The output of DFF is determined based on its clock signal and the data. It can detect the difference in range of couple of pico-seconds when different states of data or clock signal occurs for a short duration. Addition of the enable pin ( $EN_{pin}$ ) in the design allows activation or deactivation of the proposed PD. The PD consists of two DFFs, referred to as DFF1 and DFF2. In principle, if  $CLK_{out}$  leads to  $CLK_{in}$ , DFF1 generates an UP signal which is logic “1” whereas DFF2 generates the DOWN signal which is logic “0”. In the opposite case, DOWN and UP signals become logic “1” and “0”, respectively.

### B. Digitally-controlled delay line

Delay line is the most important component of the proposed DLL in terms of designing. It comprises of 80 or 40 delay cells depending on the multiplication factors which provide equidistant phases to the edge combiner for the generation of high frequency signals. The delay cell schematic is given in Fig.3. It consists of 5 digital inputs, which are binary weighted. In Fig. 3, M1 to M5 are controlling transistors whereas M8-M9 as well as M4a are current mirror transistors, M1a to M6a are the main elements of the delay line which are connected to the inverters.

This DCDL, with its 32 delay steps provides a good tradeoff between linearity and range of the delay characteristics for a single delay cell. It is worth noting that the parasitic capacitance at the source of M3a and M5a are the same for each input combination of (C<0>to C<4>) so that the values are monotonically varied with respect to the input combinations. To maintain a similar rising and falling edge, M9, M8 and M7 are featured in the design to control the current.

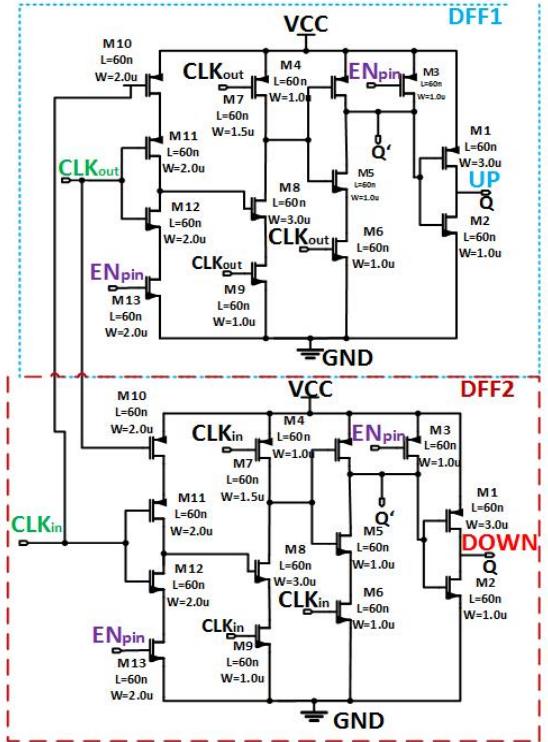


Fig. 2. Schematic of the proposed phase detector.

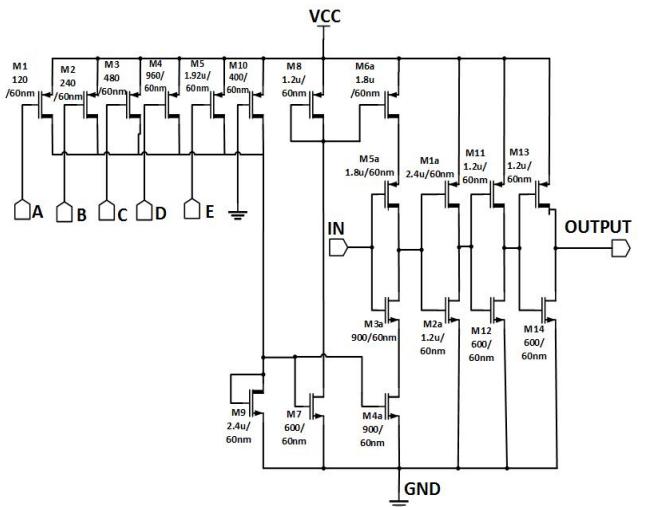


Fig. 3. Schematic of the proposed digitally-controlled delay cell.

### C. 5-bit Up-Down Counter

XOR-based up-down counter is the main regulator in the given ADDLL. The total delay time of the DCDL is controlled by UP and DOWN signals. The schematic is shown in Fig.4.

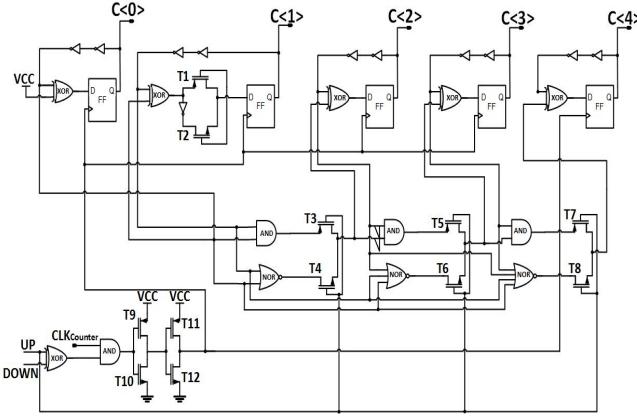


Fig. 4. Schematic of the proposed 5-bit up/down counter.

The up-down signals are sent to the counter once the phase detector is enabled. The phase difference between  $CLK_{in}$  and  $CLK_{out}$  determines the state of these two signals. The control bits from  $C<0>$  to  $C<4>$  are connected to DFF, and it can be toggled for every  $CLK_{counter}$  cycle. A synchronic operation of the system can be guaranteed by this approach. The operation of the phase detector is stopped when the phase difference between the clock signals of  $CLK_{in}$  and  $CLK_{out}$  is too small. It forces to stop the up-down counter by sending up and down signals at either 1 or 0. Thus, following XOR gate gives logic 0 at the output. Then, output of the AND gate pulls to ground and  $CLK_{counter}$  cannot be sent to the DFFs which means that locked state is achieved.

#### D. Edge Combiner

The proposed edge combiner consists of NAND and AND gates, with an addition of 2 stage and 3 stage inverters, which are used to generate multiplied falling and rising clock signals without affecting the synchronisation of the digital outputs from the DCDL. The edge combiner is fed by 80 or 40 output clock signals as it is used to combine the digital outputs of different phase clocks and generates a higher frequency output signal. The multiplied frequency depends upon the phase difference of the input clocks. The multiplication factor of 40 is achieved by different phase signals generated by 80 delay cells as shown in Fig.1. Each delay cell in the DCDL delays  $CLK_{in}$  by 1/2 and the number of generated phases N as,  $CLK_{out} = CLK_{in} (N/2)$ .

### III. SIMULATION RESULTS

The proposed design is tested with the input clock frequencies of 122MHz and 225MHz. The entire circuit is implemented using TSMC 65nm CMOS technology with Cadence Virtuoso. Fig. 5 illustrates the layout of DCDL inherits 80 cells organized in 8 rows and 10 columns occupying approximately  $56\mu m^2 \times 70\mu m^2$  of area. The proposed layout is designed in a matrix form so that each cell can be controlled with minimum mismatch between each other. Fig.6 shows the delay characteristics of the proposed DCDL based on post layout simulations operating at the input frequency of 122MHz. Its range can be varied from 5.8ns to 9.8ns constituting a wide operating frequency range. Fig. 7 shows the layout of XOR 5- bit up/down counter, each device is represented by a different colour.

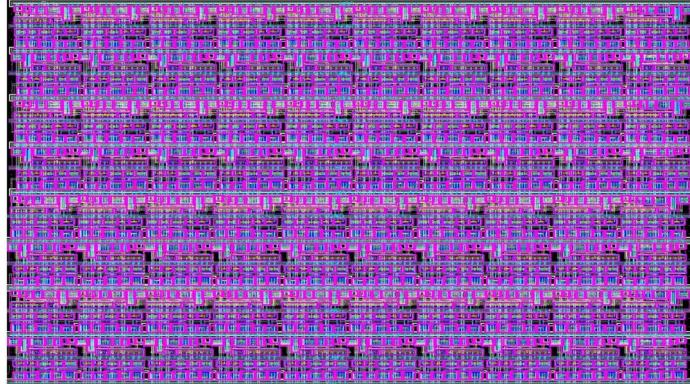


Fig. 5. Layout of the design DCDL.

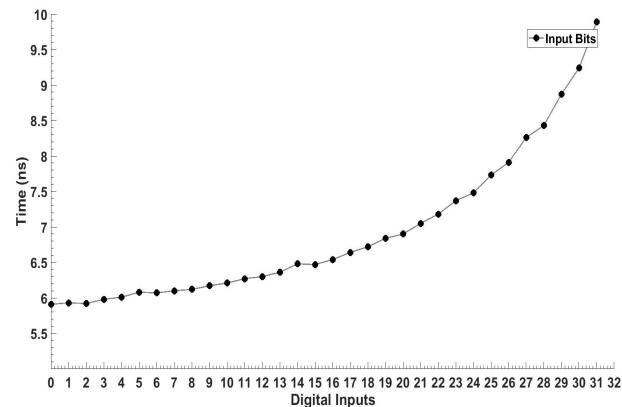


Fig. 6. Simulated delay characteristic of the designed DCDL.

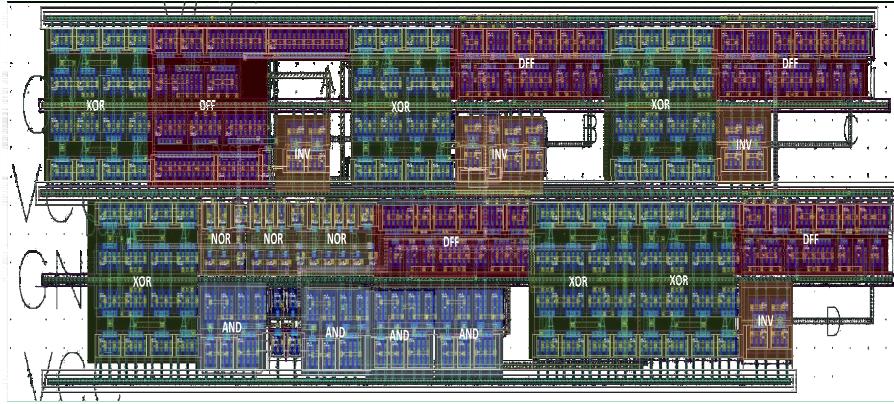


Fig. 7. Layout of the designed XOR-based 5-bit Up/Down counter.

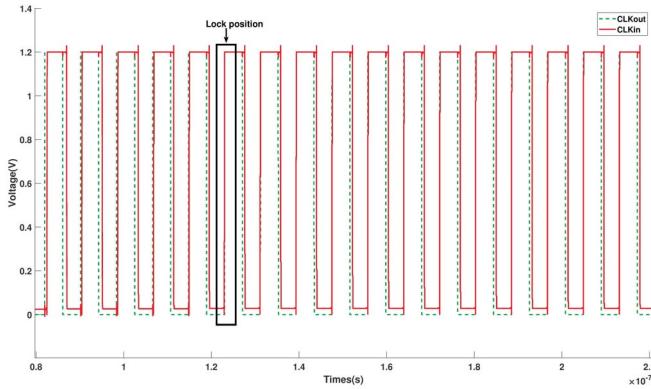


Fig. 8. Locking state of the input and output signal at 122MHz.

The behaviour of the control bits from  $C<0>$  to  $C<4>$  shows that the locking stage of up/down is reached at 130ns. In this case, the counter generates the control word of 10110 and the counter cannot respond anymore so that the difference between up/down signals becomes 0. In contrast, the locking state of the DCDL with 40 cells is reached at 40ns. Fig. 8 illustrates the simulation results for  $CLK_{in}$  and  $CLK_{out}$  during the locking process for a larger size of DCDL with 80 cells.

The simulated waveform of the clock signal  $f_{out}$  generated by the edge combiner with a period of 205ps. The delay line consists of 80 cells with 102.5ps delay (half of the total period) produced by each cell. The duty cycle of  $f_{out}$  is close to 50%. Fig. 9 presents the spectrum of generated  $f_{out}$  at 4.88GHz. It provides 25dB spurious free dynamic range (SFDR) within a 244MHz bandwidth around generated tone of 4.88GHz.

Fig. 10 shows the jitter performance of  $f_{out}$  at 4.88GHz with a multiplication factor of 40, the jitter is 28.2ps. Similarly, the performance of jitter  $f_{out}$  is 22.2ps while the edge combiner operating at 4.5GHz with a multiplication factor of 20. Comparing the jitter performance between two different sizes of the edge combiners, the one with smaller

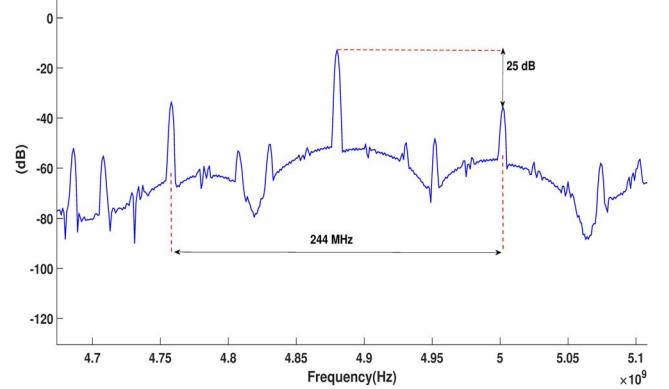


Fig. 9. Spectrum of the generated clock  $f_{out}$  operating at 4.88GHz.

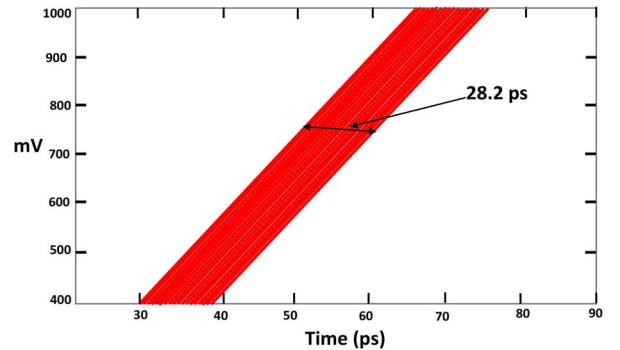


Fig. 10. Peak-to-peak jitter of generated clock  $f_{out}$  operating at 4.88GHz.

multiplication factor provides a superior peak to peak jitter performance.

Table I presents a comparison between the state-of-the-art and this work. The proposed DLL offers higher multiplication factor and wider operating frequency range. It provides a good jitter performance for a high multiplication factor. The power consumption is also reasonable with respect to the high output frequency.

TABLE I. PERFORMANCE AND COMPARISON

	[10]	[11]	<b>Proposed</b>	<b>Proposed</b>
<b>Process</b>	0.35μm	0.18μm	0.065μm	0.065μm
<b>VCC</b>	3.3V	1.8V	1.2V	1.2V
<b>Architecture</b>	EC	EC	DLL+FM	DLL+FM
<b>Max. Multi. Ratio</b>	N/A	N/A	40	20
<b>Power consumption</b>	86.6mW@ 1.3GHz	54mW@ 3.4GHz	54.6mW@ 4.88 GHz	25.7mW@ 4.5 GHz
<b>Jitter</b>	13.2ps@ 1.3GHz	N/A	28.2ps@ 4.88 GHz	22.2ps@ 4.5 GHz

## IV. CONCLUSION

The proposed an all-digital delay-locked loop (ADDLL)-based frequency multiplier implemented in TSMC 65nm CMOS technology is presented in this paper. The design proposed offers superior performance in terms of locking time, jitter, and power consumption. The multiplication factor can be varied in a short locking time. The architecture occupies a much smaller area and inherits less design difficulties compared to PLLs with their stability issues of a higher-order system and a trade-off between good phase noise performance and short settling time. A comparison is done with similar work in terms of multiplication factor and size of DCCL. A new type of delay cell can be designed, or the multiplication factor can be decreased to minimise the overall power consumption.

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