Why Glass? Advantages and Applications of Glass Substrates for Advanced Packaging

Partho Bhoumik	ASU ID: 1229999006
Joshua Jimenez	ASU ID: 1218712547
Tyler Kirby	ASU ID: 1223213862
Adam Paredes	ASU ID: 1212356819
Tushar Vishwanath	ASU ID: 1227565302

Introduction

Glass substrates are an emerging advanced packaging technology that could replace traditional substrates in the next generation of electronics. Recently, resources in industry and academia have been invested to research and develop glass substrate technology. The material properties of glass are advantageous in the mechanical, thermal, and electrical considerations of substrate design. Additionally, glass substrates allow for manufacturing processes and applications that other substrate materials are constrained by. Along with the numerous advantages, glass substrates have some inherent disadvantages and challenges that still need to be addressed. We investigated glass substrates through research papers, articles, and analytical comparisons of different physical properties with other materials. This methodology is justified because glass substrates are a new technology and are protected intellectual property. After conducting thorough research and a literature review, we examined the research question regarding substrates in semiconductor packaging, Why Glass?

Mechanical & Thermal Characteristics

One of the clearest and easiest to see benefits of glass substrates is their similar coefficient of thermal expansion (CTE) to silicon (see figure 1). The CTE of glass falls between 4-6 ppm/K and the CTE of silicon falls between 3-5 ppm/K. This overlap allows for significantly higher temperatures before suffering the same stress from thermal expansion. The delta between CTE's is often referred to as "CTE Mismatch". With copper having a CTE of 17 ppm/K, the mismatch between a copper core and silicon is ~12-14 ppm/K. FR4 is even worse with a CTE of 18-20 and a mismatch of 13-17 ppm/K. With a glass, we would see a max CTE of 3 ppm/K and in some cases, we would even have a 0 mismatch. Since strain $\boldsymbol{\gamma}=(L/H)\ *\ \Delta CTE\ *\ \Delta T$, we can see that the strain for both FR-4 and copper will be a minimum of 4+ times bigger and could even have a 0 strain condition if we get the glass and silicon properties aligned. However, that isn't the only improvement from a lower CTE mismatch.

One of the biggest plagues on the semiconductor industry is substrate warpage. It is a problem that is universal to all packaging companies and with glass substrates, we can greatly reduce it. Since we have seen that the CTE mismatch can already be as little as 0 (thus eliminating warpage) and a maximum of 3, worst case glass substrate warpage results are only ⅓ of organic substrates from changing nothing but CTE and Modulus (see example in appendix).

Aside from these improvements, there are a handful of other benefits that come into play when using glass. In Intel's slide deck during the announcement of glass substrates, they boasted that glass substrates could increase package size capabilities of up to 240mm x 240mm and with larger die complexes [12]. Along with the large size, Intel also states that the glass substrates will have "ultra low flatness", "dimensional stability", and "high assembly yields" [12].

Electrical Characteristics

Glass substrates provide numerous electrical benefits over traditional substrates. First, glass substrates are a thin-film substrate technology with high interconnect density. The interconnect density on glass is similar to that of silicon interposers [2]. This interconnect density is achieved through manufacturing processes that are perfectly suitable for glass. With high interconnect density, packages can be produced with high I/O which allows for the next generation of electronics, especially with new AI and server hardware being developed. Another advantage of glass is its dielectric properties. The dielectric constant of glass varies based on the specific design and composition of the glass. In semiconductor applications, glass variants are designed for manufacturing properties and the dielectric constant [1]. Typically, glass dielectric constants range from 3.7-10. The lower end of this range is on par with traditional substrate materials, such as organics. This low dielectric constant enables quicker signal transmission and minimizes losses. This is an important electrical characteristic, especially in high speed applications such as RF or high speed digital.

Properties	Ceramics		Organics		Glass	Silicon	Metal
	Alumina	Silicon carbide	Epoxy polymer	FR-4 laminate	Borosilicate glass	Single crystalline	Copper
Electrical							
Dielectric constant @ 1 MHz	9.5	9.5–10	3–4	4.5–4.8	4.6	11.9	—
Resistivity (Ω·m)	$>10^{10}$	Variable (depends on grades)	$>10^{10}$	$>10^{10}$	$>10^{10}$	0.02–10 (typically doped)	2×10^{-8}
Thermal							
Coefficient of thermal expansion (ppm/K)	7.5–8.5	4	45–65	18–20	3.3	2.6–3.0	17
Thermal conductivity (W/m·K)	20–40	50–300	0–1	0–1	1.1–1.2	100–150	350–400
Mechanical							
Young's modulus (GPa)	300–400	400–500	0–2	10–20	60–80	130	110–120

Figure 1: Substrate Material Properties (from lecture 11 slides)

Glass wafers have already been extensively used for manufacturing passive devices. Through glass vias (TGVs) introduced in glass substrate technology, passive devices can be manufactured on both sides of the substrate material [1]. Also, the dielectric properties of glass allow for antennae integration since losses are low and signal quality can be maintained [1]. Integration of passive devices and antennae is one of the huge electrical benefits that glass substrates provide. An additional benefit of passive device integration is that the technology and reliability for the manufacturing of these devices on glass are already proven. Given the many benefits of glass substrates, there are still some challenges and disadvantages that affect their electrical performance. One major challenge is that the number of layers is limited with glass. Silicon substrates and laminates allow for many layers on the top, bottom, and inside of the substrate. At the moment, glass substrates are constrained in that they cannot have internal layers and the interconnects on the top and bottom are limited in layer count [2]. This limited layer count can bottleneck high density interconnect designs due to routing challenges. Innovative solutions must be created to improve this current drawback of glass substrates. Another disadvantage of glass is that the manufacturing technology is still not mature. Fortunately, these challenges and disadvantages can be addressed and improved, making glass a very competitive material for future substrates. The next section will discuss the manufacturing processes for glass substrates.

Manufacturing Processes

In semiconductor manufacturing, glass substrates are considered to play a huge role in the future, especially in advanced packaging technologies [3]. Fabricating a glass substrate involves several steps to ensure that it meets the required dimensions, flatness, and electrical properties for semiconductor devices. These steps include melting, shaping, cutting, and polishing to produce glass sheets or wafers. Techniques like photolithography and etching are then used to add features such as embedded trenches or vias, just like how it is done on wafers. Glass substrates offer benefits like excellent thermal stability, customizable coefficients of thermal expansion (CTE), and electrical insulation, making them ideal for reliable thermal management. However, intricate features may require special equipment and skills, which can increase manufacturing costs.

The embedded trench process involves carving narrow channels or trenches into glass substrates for semiconductor packaging. It begins with defining precise patterns using photolithography and etching. Trenches are then created using wet or dry etching techniques and filled with materials like dielectric insulators or conductive metals. These trenches serve as pathways for electrical connections and thermal management in semiconductor devices.

Semi-additive processes selectively deposit and pattern metal traces onto glass substrates for semiconductor packaging. After preparing the substrate, a thin metal layer is deposited using techniques like sputtering. Photolithography defines precise patterns for the metal traces, followed by selective etching to remove unwanted metal. This process creates complex metal structures, including interconnects and bond pads, essential for semiconductor device functionality.

Challenges in glass substrate manufacturing include achieving precise dimensional control and uniformity, overcoming glass etching difficulties, ensuring proper adhesion and metallization, managing thermal conductivity limitations, preventing substrate cracking, and maintaining compatibility with packaging materials and processes [7]. Addressing these challenges requires advanced technologies and collaboration across the supply chain to ensure the reliability and performance of glass substrates in semiconductor packaging.

State of the Art

Intel has been exploring the use of glass core substrates in its semiconductor manufacturing processes as part of its ongoing efforts to enhance performance and efficiency according to its Industry 2.0 guidelines. Glass core substrates offer several advantages over traditional silicon substrates, including improved thermal management, higher electrical insulation, and potential cost savings. Intel has been researching various techniques to integrate glass core substrates into its semiconductor devices, such as incorporating them into advanced packaging technologies or utilizing them as interposers for 3D integration. By leveraging glass core substrates, Intel aims to achieve higher performance, lower power consumption, and increased functionality in its semiconductor products. Not much is known about Intel's use of glass core technology specifically, but they have repeatedly confirmed that they will change their supply to use this technology for chips in the future [13].

Applications

For data-intensive applications such as artificial intelligence (AI), the organic substrates in use today face limitations. Power delivery, design rules, signaling speed, and package stability are all essential areas where glass is the preferred material. It would allow more chips to be packed into a smaller footprint while improving performance and lowering costs and power usage. “Glass substrates can tolerate higher temperatures, offer 50% less pattern distortion, and have ultra-low flatness for improved depth of focus for lithography, and have the dimensional stability needed for an extremely tight layer-to-layer interconnect overlay. As a result of these distinctive properties, a 10x increase in interconnect density is possible on glass substrates” [3]. The tolerance to higher temperatures can also make it easier to integrate optical interconnects and embed inductors and capacitors into the glass. While it can run at higher temperatures, it also expands at the same rate as silicon to avoid mechanical failures. The stability of glass is also an advantage. As the number of holes in the substrate increases, warping becomes more of an issue as it can cause loss of contact in some areas. However, glass does not warp due to its rigidity. This trait also allows for more finely cut pathways for data. “The stability of glass allows for up to a 10x increase in routing and signaling wires, allowing wires to be smaller and closer together, which will let Intel reduce the number of metal layers involved. More signaling allows more chiplets to be stacked onto the package, and the glass's thermal stability will allow more power to go to the chiplets instead of getting lost in the interconnects” [10].These benefits bring the industry closer to being able to scale 1 trillion transistors on a package by 2030 and make glass substrates a big part of the new and larger data centers and AI chips working with them.

Glass substrates are also important in MEMS applications such as pressure sensors, optical MEMS, acceleration sensors, and gyroscopes. These devices have fragile moving structures that need to be protected from the environment to ensure reliable functionality. Encapsulation is therefore needed to hermetically seal them, which is usually done using glass. It often serves as a cap substrate to create a highly vacuum-sealed environment through anodic bonding, direct bonding, or metal bonding. Glass’s strong chemical and temperature resistance is needed to withstand harsh environments, which include conditions such as corrosion. This makes glass preferable for many applications, such as in the automotive and medical fields, since durability and high reliability in the long term are required. Not only does glass have good sealing performance, it also provides good electrical isolation and minimizes parasitic

capacitance in regards to the electrical interconnects [9]. Glass is also good for optical sensors due to its optical transparency over infrared and visible spectra. These properties make glass an important component of the packaging process, which is an essential part of MEMS sensors.

With the continuing growth of 5G, high frequency signals are also of great importance. With glass being an insulator, it is a great choice for this application due to its very low electrical loss. “Compared to the state of the art, it increases the functionality that can be integrated through various waveguide concepts, high-density micro-wiring and hermetic encapsulation. In addition, it enables applications up to 300 GHz thanks to its high levels of accuracy and material quality. This is achieved with glass, a single system material, which allows, among other things, excellent waveguiding properties and high-precision micro-machining“ [8].Other advantages to using glass for high frequency applications include the ability to form fine-pitch metal lines and spaces, the machinability to create micro-size TGVs, high dimensional stability, its closely matched CTE to silicon dies, and its productivity in thin and large panels.

Glass substrates are also helping the advancement of the heterogeneous era the semiconductor industry is in, which includes integrating multiple chips in a package. An example of this is the heterogeneous integration of electronic integrated circuits and photonic integrated circuits onto a common package substrate, which reduces the electrical interconnect loss by decreasing the required distance. “The single layer provides simpler fabrication and assembly compared to a 2.5D silicon interposer on an organic substrate or an embedded multi-die interconnect bridge configuration and, as such, has the potential for lower overall packaging cost” [11].This is another application area that benefits from the many properties of glass such as its ability to allow low loss and power efficient high-speed electrical interconnects, thermal management of the high power consumption of electrical ICs combined with temperature sensitive photonic ICs, low warpage, and high electrical reliability.

Challenges and Potential Solutions

Given the comprehensive analysis of glass substrates in advanced packaging so far, including their advantages and applications, it is evident that this technology can be the driving force of semiconductor manufacturing technology in the upcoming years. However, there still remain some challenges and we will discuss them along with some potential solutions.

First, this new fabrication technology is susceptible to defects due to its higher sensitivity to mechanical stress and can form cracks and damage inside the core [14]. Although conducting material research on glass compositions and proper testing and diagnosis, these failure issues can be narrowed down through yield learning, and eventually, just like other technologies, we can reach the bottom of the "Bathtub Curve". Second, the lower thermal conductivity, while advantageous in terms of tolerance, can become problematic for high-power applications where it may struggle to dissipate heat according to Fourier's law. This issue can be readily overcome by deploying high-end cooling solutions or integrating other materials with glass to find a sweet spot for thermal conductance that facilitates the best of both worlds. Third, the layer limitations that have already been discussed are also present. This problem also needs to be addressed with proper research on advanced layering techniques such as ultra thin layering and/or 3D stacking. Fourth, fragility, lack of adhesion to metal wires, and measurement accessibility, due to the high level of transparency and differing reflective indices compared to silicon, can play a critical role in determining the integrity of the chip being manufactured [2]. Material engineering, incorporating an adhesive layer or atomic layer deposition techniques, and testing and measurement aware design considerations can be explored to address these issues as well.

It is true that there are a number of limitations to this technology but it is also evident from the discussion that there is infinite potential to solve these problems too.

Conclusion

A new technology is always full of challenges; even the silicon devices we are currently using have come to this point after a plethora of research and development. The exploration of glass substrates in advanced semiconductor packaging represents a pivotal shift towards meeting the evolving demands of the electronics industry. The journey of silicon-based technologies has been monumental, setting a high benchmark for reliability, efficiency, and innovation. However, the inherent limitations of silicon substrates, particularly in terms of thermal management, interconnect density, and scaling capabilities, have necessitated the search for alternatives. This is where glass substrates, with their superior thermal stability, lower dielectric constant, and potential for high interconnect density, step into the limelight. Despite the challenges—ranging from mechanical fragility and thermal conductivity issues to the complexities of layer limitations

and adhesion concerns—the discussion about glass substrates focuses not on the hurdles but on the solutions and the promise they hold.

Therefore, answering the research question, "Why Glass?"—glass is not just being developed as a future substrate material out of necessity but out of a vision for the future. A future where the limitations of today become the stepping stones for tomorrow's innovations. A future where glass substrates enable the semiconductor industry to meet the increasing demands for higher speed, lower power consumption, and greater functionality in ever-smaller (and bigger) packages. As we embark on the journey of material science and engineering, it becomes clear that the question is no longer "Why Glass?" but "How far can glass take us?"

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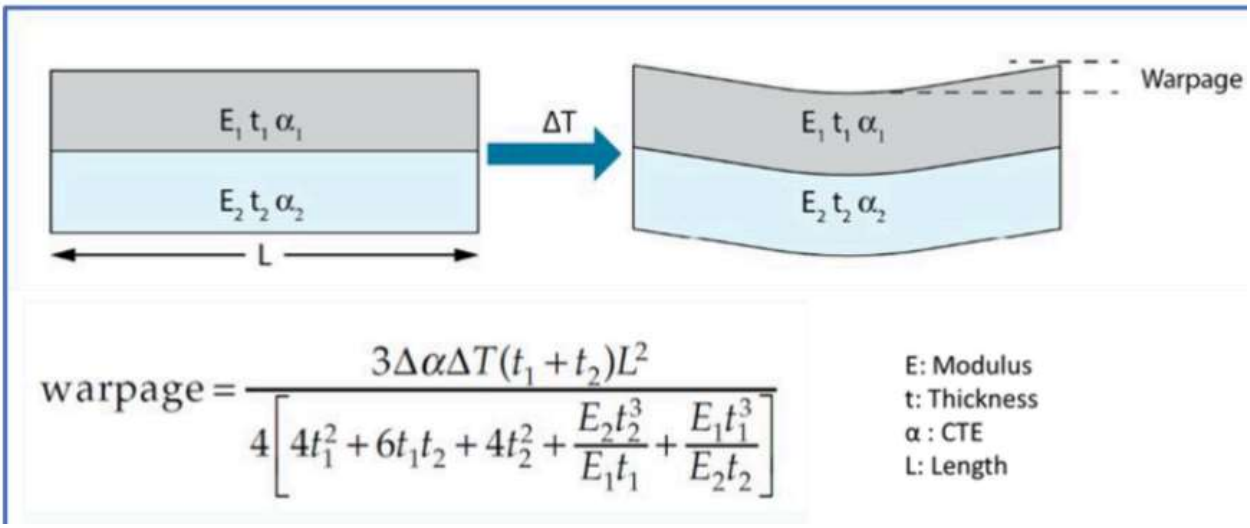
Appendix:

Example calculations for Warpage (referenced from in class example)



$$\text{warpage} = \frac{3\Delta\alpha\Delta T(t_1+t_2)L^2}{4\left[4t_1^2+6t_1t_2+4t_2^2+\frac{E_2t_2^3}{E_1t_1}+\frac{E_1t_1^3}{E_2t_2}\right]}$$

E: Modulus
t: Thickness
α : CTE
L: Length

CTE1	0.000003
CTE2	0.000006
Thickness 1	0.001
Thickness 2	0.001
Length	0.05
E modulus 1	1.5E+11
E modulus 2	70000000000
Temp 1	273
Temp2	373

Warpage of Glass substrate(m)
6.77322E-05

CTE1	0.000003		Warpage of Organic Substrate (m)		
CTE2	0.000015				
Thickness 1	0.001				
Thickness 2	0.001		0.00022314		
Length	0.05				
E modulus 1	1.5E+11				
E modulus 2	25000000000				
Temp 1	273				
Temp2	373				
			warpage in organic sub is	3.294451	times bigger
			That means glass only warps	30.35407	% of organic