

# VHDL 1: WRITE A VHDL CODE FOR AND GATE.

The screenshot shows the EDA playground interface. On the left, the sidebar includes options for Testbench + Design (VHDL), Libraries (None, OVL, OSVVM), Top entity (tb\_ANDgate), Tools & Simulators (GHD3L 3.0.0, Import Options, Make Options, Run Options, Simulator Options), and Examples (using EDA Playground, VHDL, Verilog/SystemVerilog, UVM, EasierUVM, SVA/Unit, SVUnit, VUnit (Verilog/SV)).

The main area has two tabs: 'testbench.vhd' and 'design.vhd'. The 'testbench.vhd' tab contains the following VHDL code:

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity tb_ANDGate is end;
architecture sim of tb_ANDGate is
begin
  uut: entity work.ANDgate port map(A, B, Y);
end;
process
begin
  A <= '0'; B <= '0'; wait for 10 ns; report "A=0 B=0 => Y='0'" &
  STD_LOGIC''image(Y);
  A <= '0'; B <= '1'; wait for 10 ns; report "A=0 B=1 => Y='0'" &
  STD_LOGIC''image(Y);
  A <= '1'; B <= '0'; wait for 10 ns; report "A=1 B=0 => Y='0'" &
  STD_LOGIC''image(Y);
  A <= '1'; B <= '1'; wait for 10 ns; report "A=1 B=1 => Y='1'" &
  STD_LOGIC'image(Y);
  wait;
end process;
end sim;

```

The 'design.vhd' tab contains the following VHDL code:

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity ANDgate is
  Port (A, B : in STD_LOGIC; Y : out STD_LOGIC);
end ANDgate;
architecture beh of ANDgate is
begin
  Y <= A AND B;
end beh;

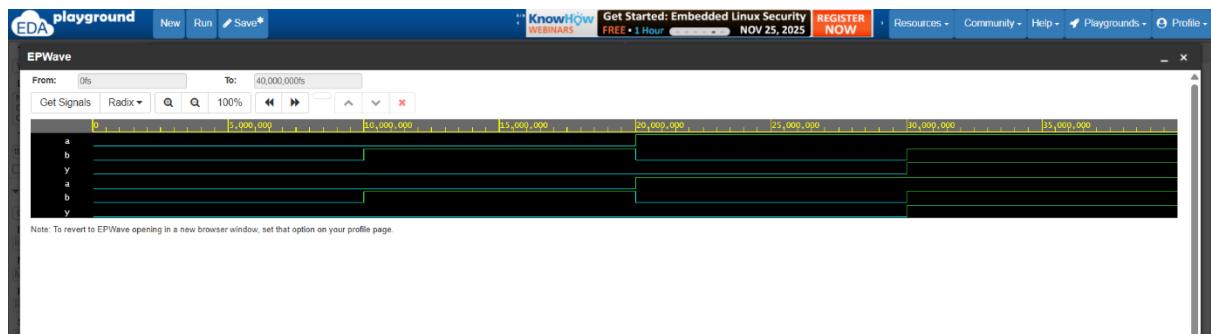
```

Below the tabs, a log window shows the command-line output of the simulation:

```

[2025-11-09 14:41:12 UTC] ghd1 -t design.vhd testbench.vhd && ghd1 -n tb_ANDgate && ghd1 -r tb_ANDgate --vcd=dump.vcd
analyze design.vhd
analyze testbench.vhd
elaborate tb_andgate
testbench.vhd:13:41:@10ns:(report note): A=0 B=0 => Y='0'
testbench.vhd:14:41:@20ns:(report note): A=0 B=1 => Y='0'
testbench.vhd:15:41:@30ns:(report note): A=1 B=0 => Y='0'
testbench.vhd:16:41:@40ns:(report note): A=1 B=1 => Y='1'
Finding VCD file...
./dump.vcd
[2025-11-09 14:41:13 UTC] Opening EPWave...
Done

```



# VHDL 2: WRITE A VHDL CODE FOR OR GATE.

The sidebar and tabs are identical to the first screenshot, showing the same options and files.

The 'testbench.vhd' tab contains the following VHDL code:

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity tb_ORGate is end;
architecture sim of tb_ORGate is
begin
  uut: entity work.ORGate port map(A, B, Y);
end;
process
begin
  A <= '0'; B <= '0'; wait for 10 ns; report "A=0 B=0 => Y='0'" &
  STD_LOGIC''image(Y);
  A <= '0'; B <= '1'; wait for 10 ns; report "A=0 B=1 => Y='1'" &
  STD_LOGIC''image(Y);
  A <= '1'; B <= '0'; wait for 10 ns; report "A=1 B=0 => Y='1'" &
  STD_LOGIC'image(Y);
  A <= '1'; B <= '1'; wait for 10 ns; report "A=1 B=1 => Y='1'" &
  STD_LOGIC'image(Y);
  wait;
end process;
end sim;

```

The 'design.vhd' tab contains the following VHDL code:

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity ORGate is
  Port (A, B : in STD_LOGIC; Y : out STD_LOGIC);
end ORGate;
architecture beh of ORGate is
begin
  Y <= A OR B;
end beh;

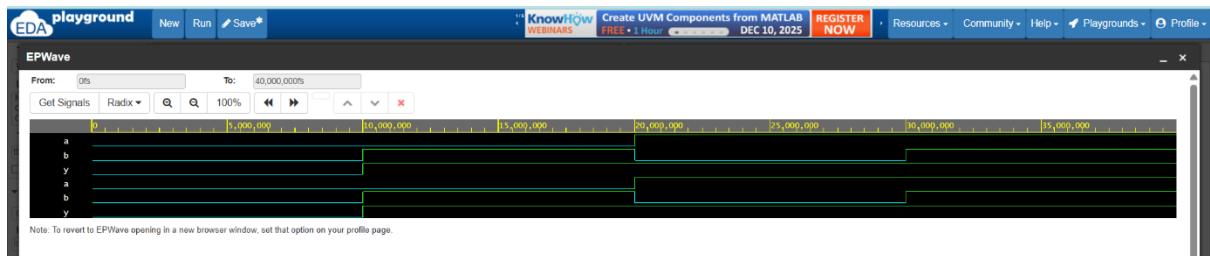
```

The log window shows the simulation results:

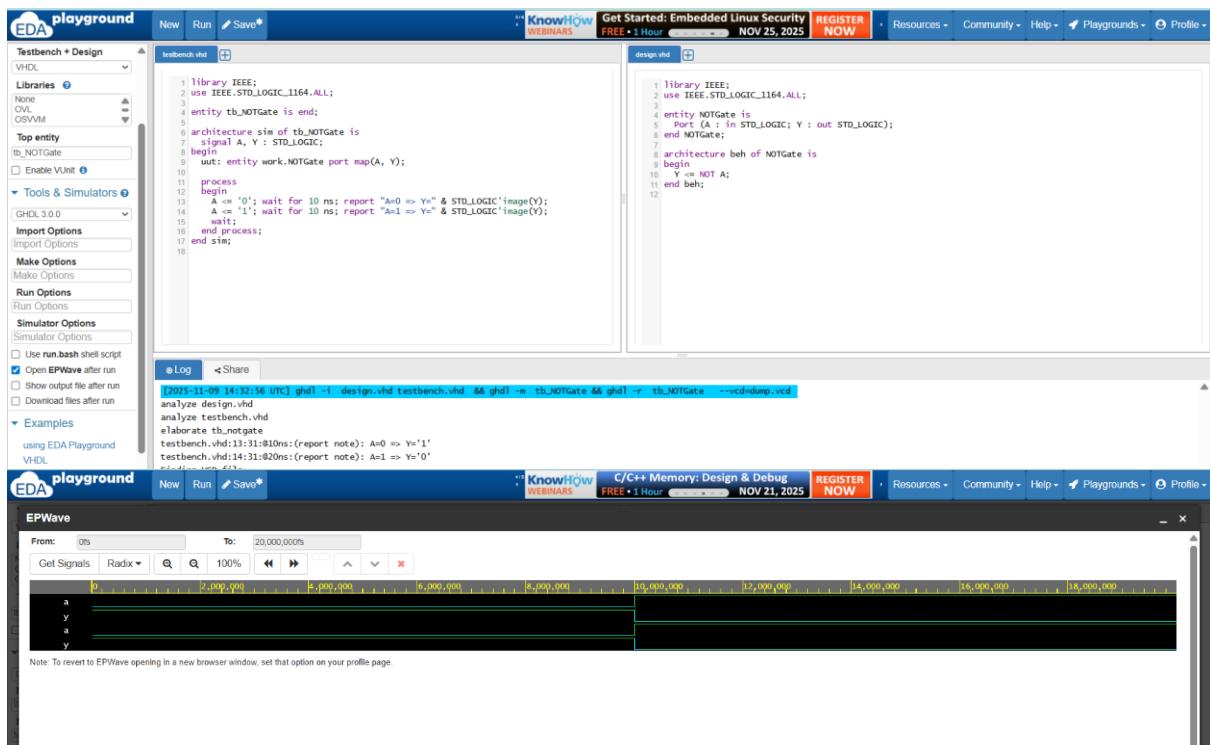
```

[2025-11-09 14:41:24 UTC] ghd1 -t design.vhd Testbench.vhd && ghd1 -n tb_ORGate && ghd1 -r tb_ORGate --vcd=dump.vcd
analyze design.vhd
analyze testbench.vhd
elaborate tb_orgate
testbench.vhd:13:41:@10ns:(report note): A=0 B=0 => Y='0'
testbench.vhd:14:41:@20ns:(report note): A=0 B=1 => Y='1'
testbench.vhd:15:41:@30ns:(report note): A=1 B=0 => Y='1'
testbench.vhd:16:41:@40ns:(report note): A=1 B=1 => Y='1'
Finding VCD file...
./dump.vcd
[2025-11-09 14:41:26 UTC] Opening EPWave...
Done

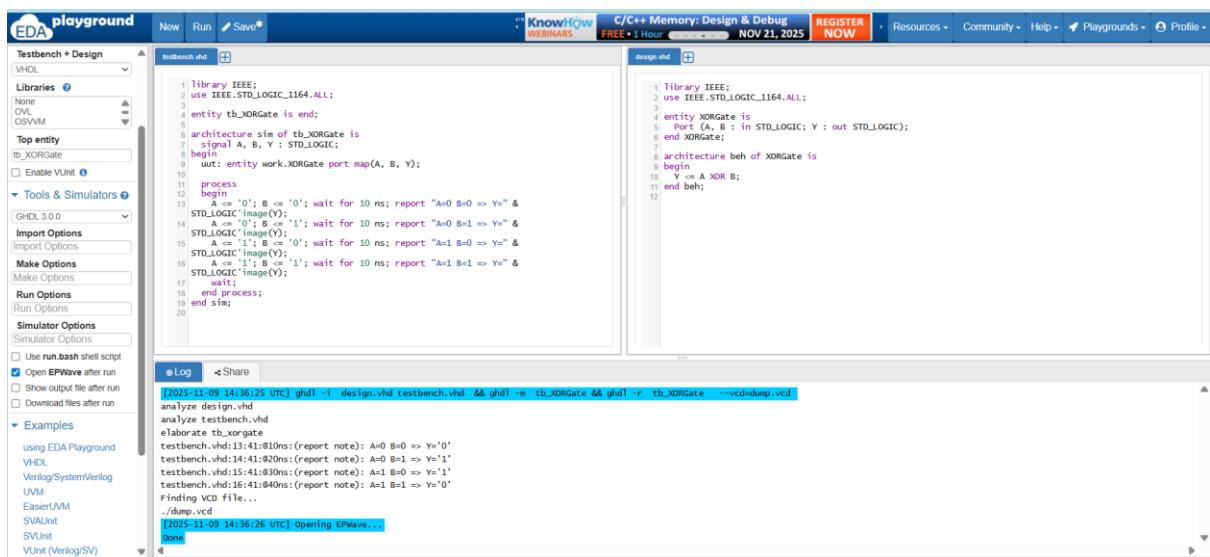
```

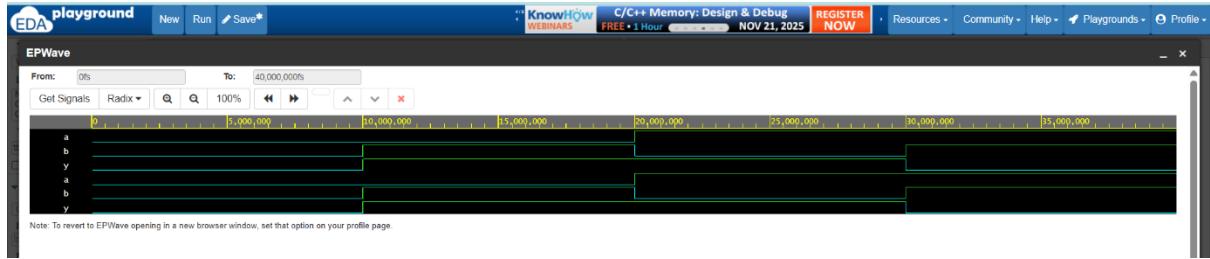


## VHDL 3: WRITE A VHDL CODE FOR NOT GATE.

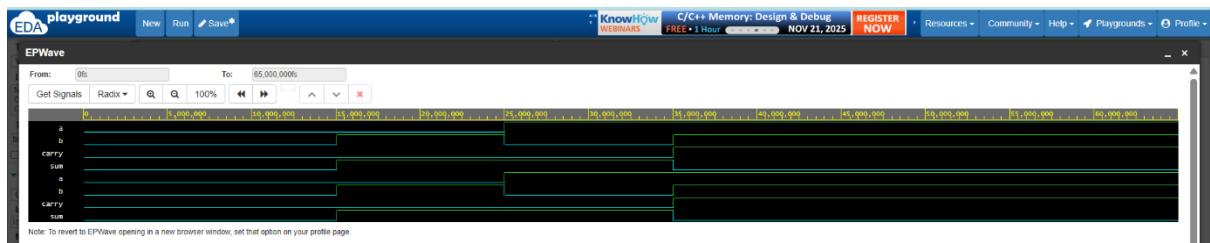
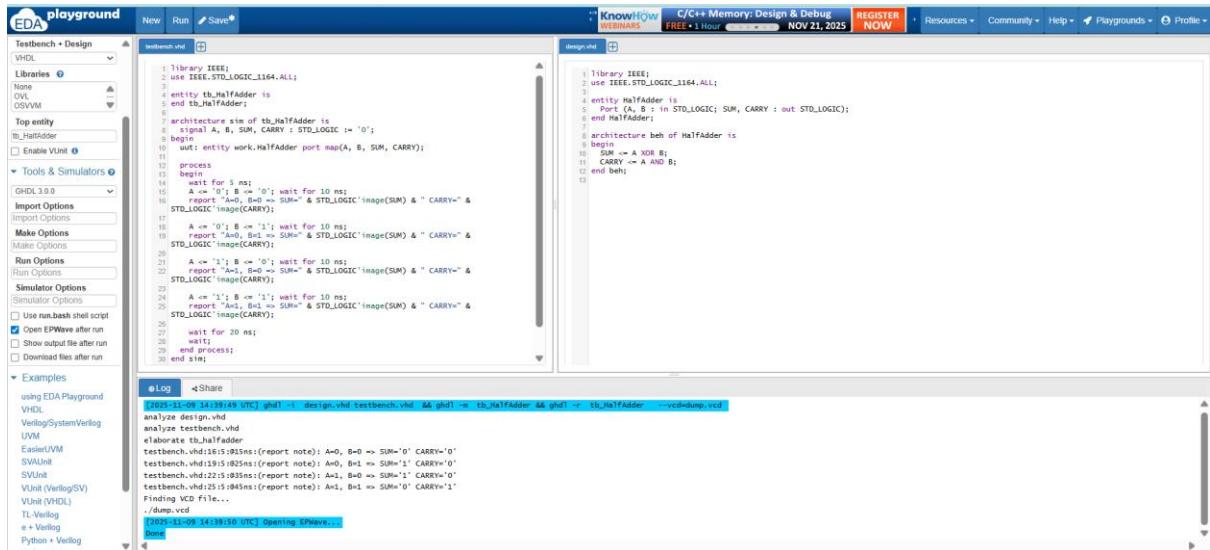


## VHDL 4: WRITE A VHDL CODE FOR XOR GATE.





## VHDL 5: WRITE A VHDL CODE OF HALF ADDER CIRCUIT.



## VHDL 6: WRITE A VHDL CODE FOR FULL ADDER CIRCUIT.

