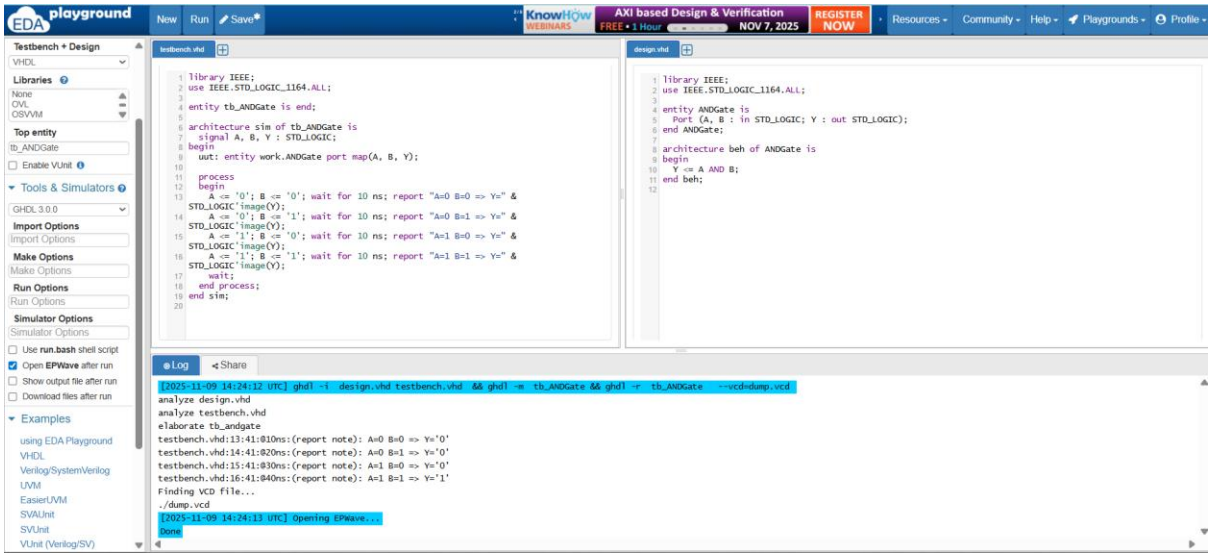
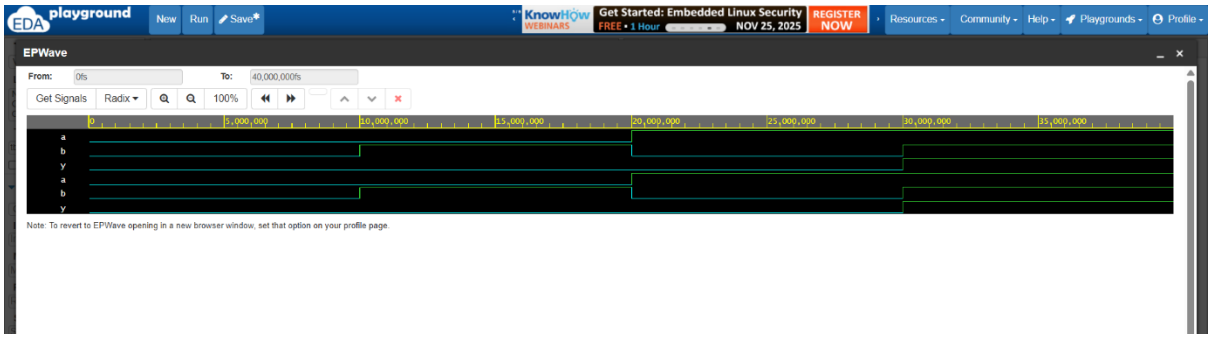
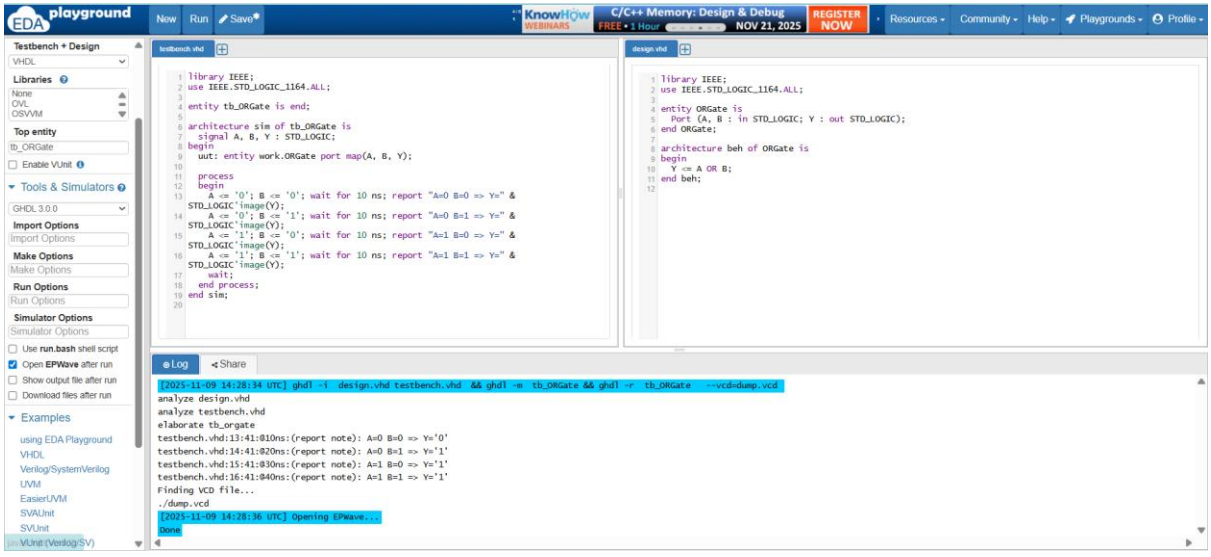
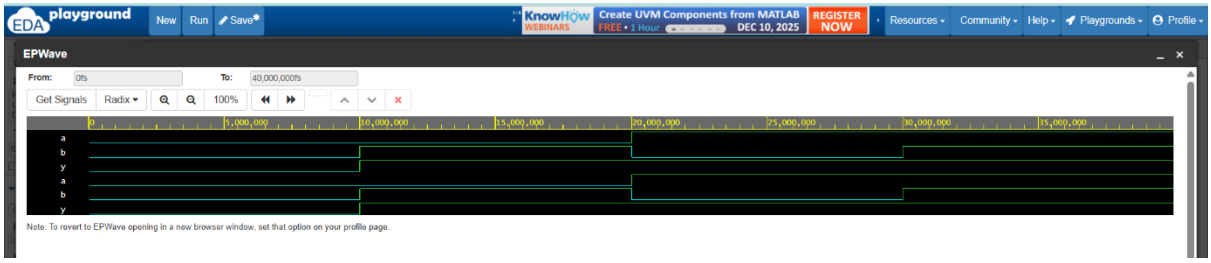
VHDL 1: WRITE A VHDL CODE FOR AND GATE.



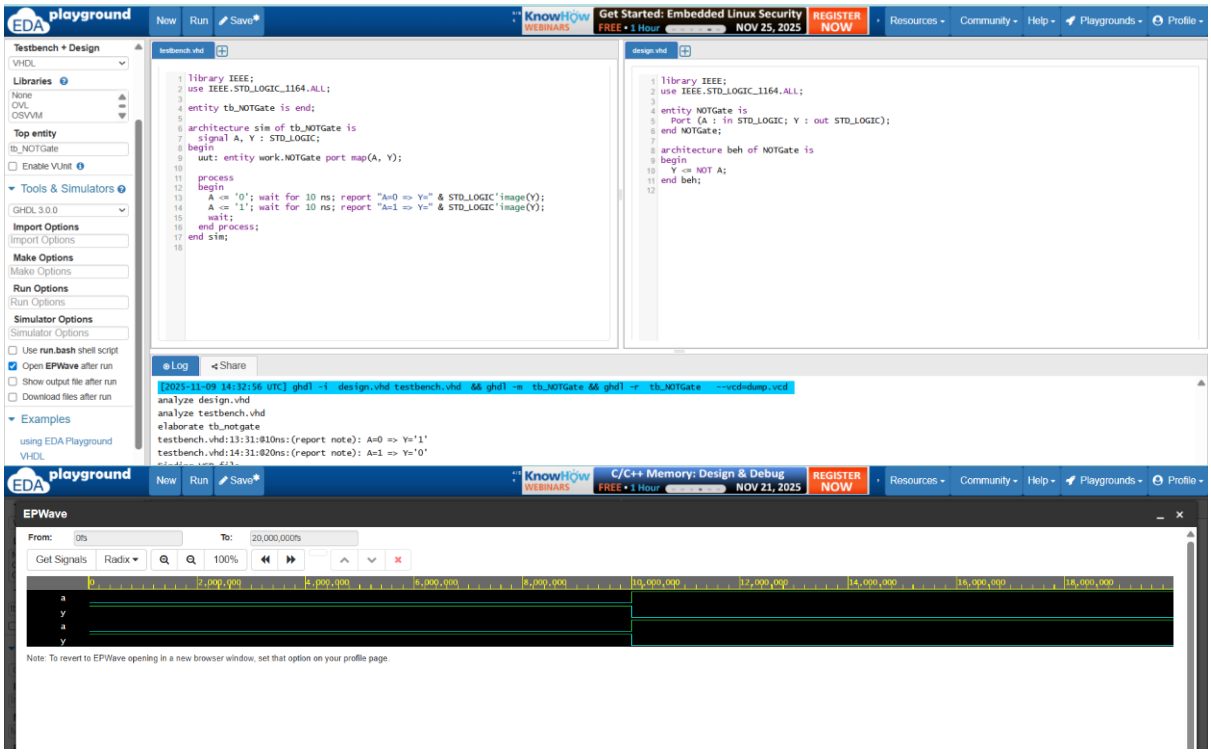


VHDL 2: WRITE A VHDL CODE FOR OR GATE.

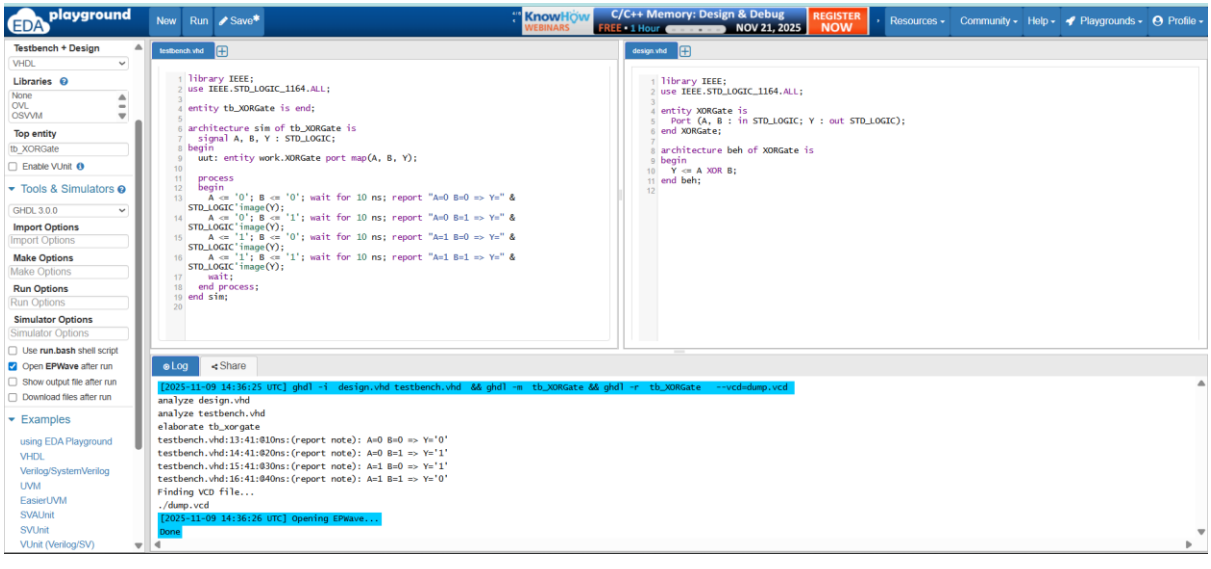


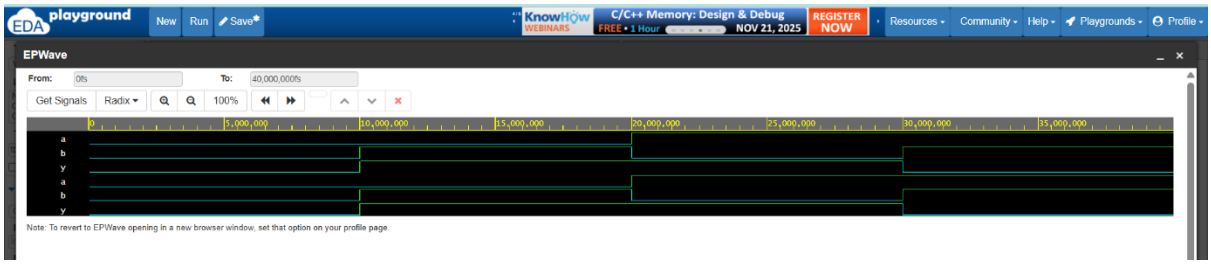


VHDL 3: WRITE A VHDL CODE FOR NOT GATE.

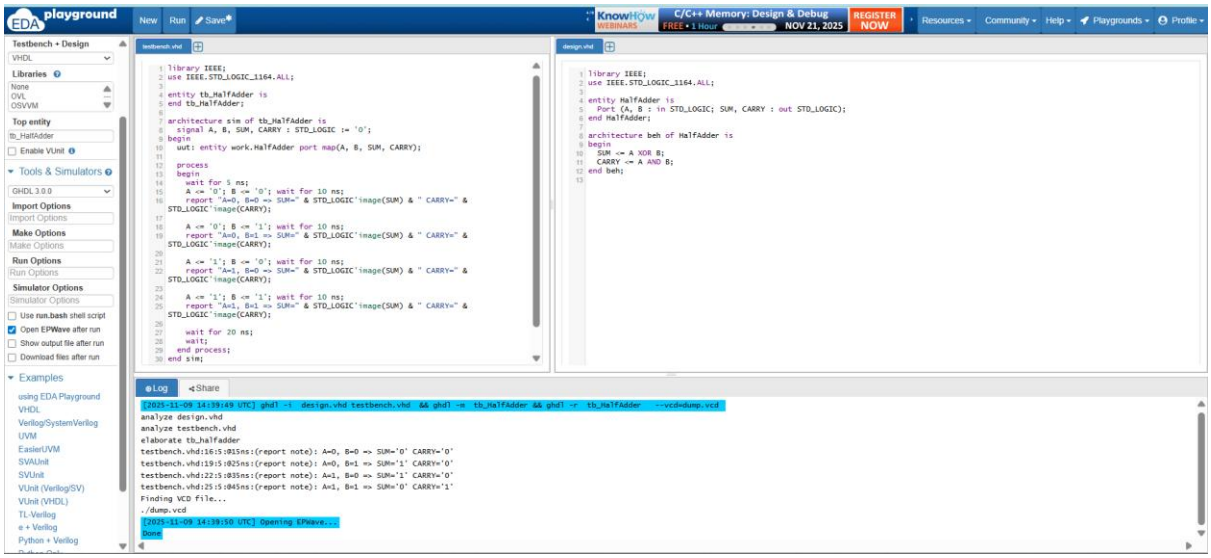


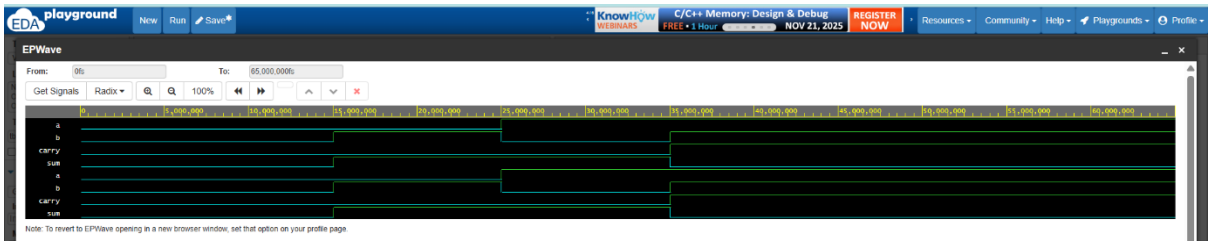
VHDL 4: WRITE A VHDL CODE FOR XOR GATE.



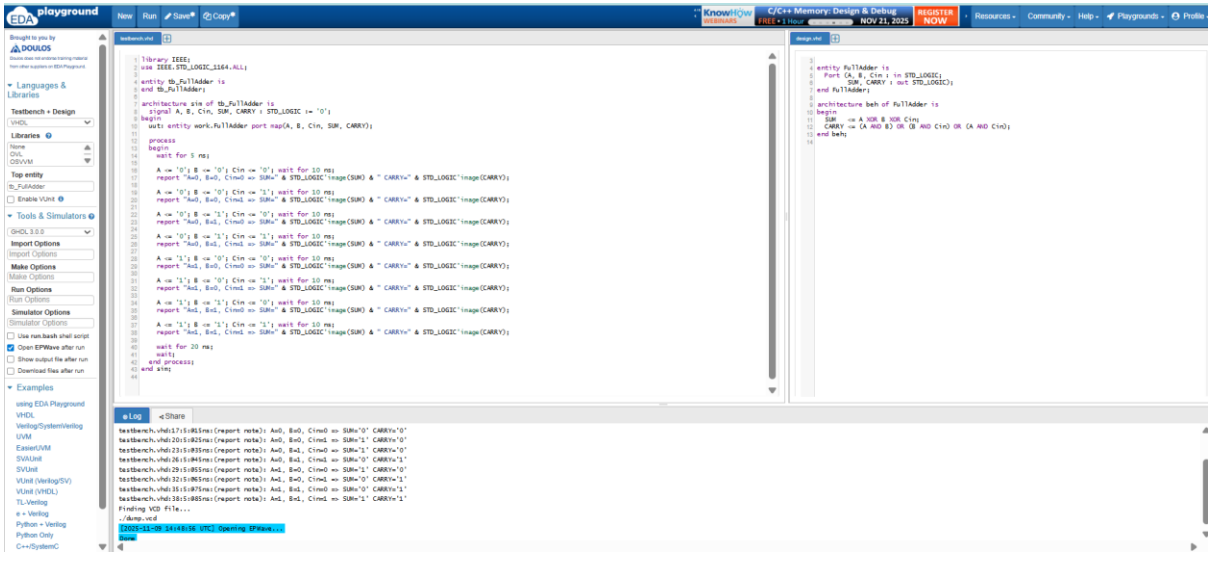


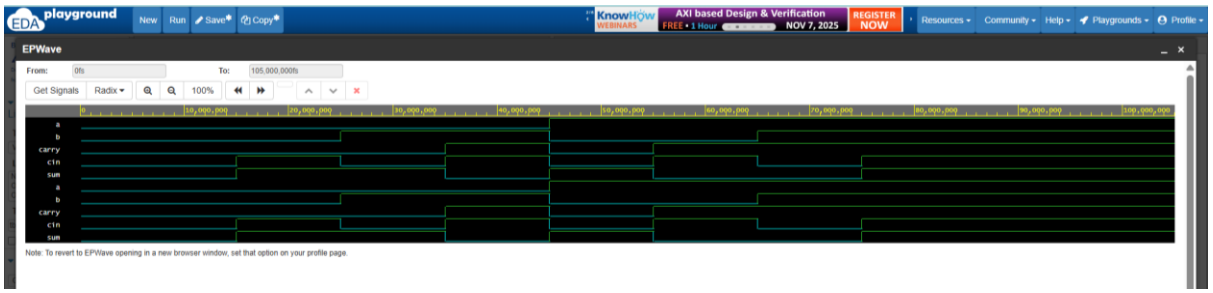
VHDL 5: WRITE A VHDL CODE OF HALF ADDER CIRCUIT.





VHDL 6: WRITE A VHDL CODE FOR FULL ADDER CIRCUIT.

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Note: To revert to EPWave opening in a new browser window, set that option on your profile page.