

Tran Van Tu

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Education

Danang University of Technology
Computer Engineering. GPA: 3.24/4.00

Da Nang
August 2021 – Present

Research

Integrating MotionAGFormer and STEP for Emotion Recognition from Human Gait Mar. 2025 – Aug. 2025
Advisor: Dr. Tran Thi Minh Hanh | Team size: 3 | [\[paper\]](#)

- Integrated 3D human keypoint extraction model with emotion classification model to recognize emotions from human gait videos.
- Evaluated model performance using quantitative methods (accuracy, confusion matrix) and by comparing it with other emotion recognition models.

Experience

Embedded Intern – Naicorp Robotics

June 2025 – October 2025

- Developed a video playback system streaming RAW data from SD card to dual GC9A01A 240×240 LCDs on STM32F411 (HAL/LL, C).
- Implemented and optimized GC9A01A driver with DMA-based rendering, rotation, scrolling, and text/graphics.
- Designed a high-speed SPI/DMA pipeline with chunking and double buffering, reducing CPU load and RAM usage.
- Achieved smooth 240×240 RGB565 playback at ~25–30 fps (up to 100% faster than baseline).

Hardware/PCB Design Intern – Naicorp Robotics

May 2025 – June 2025

- Designed a breakout board for ATmega32U4 with USB-TTL CP2102.
- Created schematic and 2-layer PCB layout using Altium Designer & KiCad.
- Applied high-speed design techniques: differential pair routing (USB), impedance control, length matching.
- Performed EMC/EMI reduction: power distribution, decoupling, and ground plane optimization.
- Generated Gerber/BOM files and supported prototype bring-up/testing.

Skills

Programming: C/C++, Python (scripting/automation), Dart/Flutter.

Embedded Systems: STM32 (F103/F411), ESP32-C3, Arduino; HAL/LL, CMSIS, FreeRTOS.

Interfaces: GPIO, SPI, I2C, UART, CAN, DMA, PWM, ADC/DAC; PID control.

Networking & Protocols: TCP/UDP Socket, MQTT, Wi-Fi, HTTP/HTTPS, REST API.

Hardware & PCB: Schematic reading, basic PCB design/testing (Altium, Proteus).

Tools: STM32CubeMX/IDE, ESP-IDF, Git.

Strengths: Fast learner of datasheets/documentation; skilled in low-level optimization & debugging under RAM/CPU constraints.