AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH

Faculty of Engineering

Laboratory Report Cover Sheet

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Laboratory Title: Study of Different Flip-Flops

Experiment Number: 06 Due Date: 21-04-24 Semester: Spring 23-24

Subject Code: 0067 Subject Name: **Digital Logic And Circuits Lab** Section: R

Course Instructor: Md. Ashiquzzaman Degree Program: CSE

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Title: Study of Different Flip-Flops.

Introduction:

The basic building blocks of combinational logic circuits are gates. In particular, AND, OR, and NOT gates (however, there are also, XOR, NAND, NOR, XNOR gates too).
The basic building blocks of sequential logic circuits are flip flops. Flip flops are devices that use a clock. Each flip flop can store one bit. There are different types of flip-flop. D flip-flop, T flip-flop, J-K flip-flop etc.

Theory and Methodology:

Basically, a flip flop has two/three inputs. One input is a control input. For a D flip flop, the control input is labeled D. For a T flip flop, the control input is labelled T. For J-K flipflop the control inputs are J and K.The other input is the clock.

The clock input is usually drawn with a triangular input. These flip-flops are *positive edge- triggered flip flops*. This means that the flip flops can only change output values when the clock is at a positive edge. There are also negative edge triggered flip flops, which change on a negative edge. In this theory section, we consider only positive edge-triggered flip flops.

When the clock is not at a positive edge, then the output value is held. That is, it does not change.

A flip flop also has two outputs, **Q** and **Q'**. The output is really the bit that's stored. Thus, the flip flop is always outputting the one bit of information.

But one might wonder "Doesn't it have two bits of information? **Q** and **Q'**?" If we have two bits, we have four possible values. However, **Q'** is the negation of **Q** which means you only have two possible outputs: **Q = 0, Q' = 1** or **Q = 1, Q' = 0**. Since the second output is always negated from the first, you don't get any additional storage. But what is the necessity of the negated output? Actually, the design of flip-flop gives **Q'**basically for free, so that's why flip flops have both the regular output and the negated output.

D Flip-Flop:
In a positive edge triggered D flip-flop, the output **Q** samples the input **D** and becomes **Q = D** only at the positive edge of the clock and it does not change during the whole clock cycle even if the input changes.
Sometimes flip flops often have two additional inputs called *clear*and*preset*. Conventionally they are drawn at the top and bottom of the flip flop respectively. 'Preset' and 'Clear' can be either active low or active high. If the preset is active, the output will be 1 no matter what are the conditions of D or clock. But 'clear' is of two types. Asynchronous clear and synchronous clear.If the asynchronous clear is activated, it causes **Q** to be automatically set to 0. It does this, even if the clock has not reached a positive edge. That is, it sets Q to zero as fast as it can. The asynchronous clear is often used to reset flip flops to some initial value. But for synchronous clear, **Q** will be 0 if the clear is active when the clock is in a positive edge.

There are different ways to design a D flip-flop. In this lab sheet, only one way is shown. Students will be familiar about other ways in their theory class.

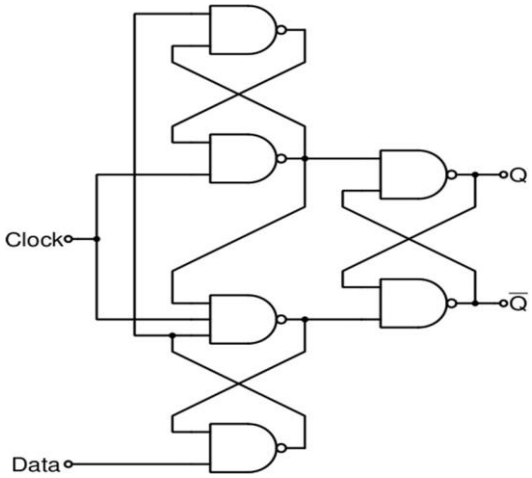

Figure1: Logic circuit a positive edge triggered D flip-flop without preset and clear capability.

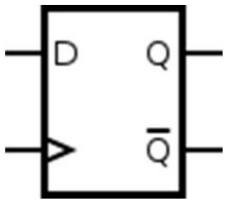

Figure 2: Graphical Symbol of a positive edge triggered D flip-flop without preset and clear capability.

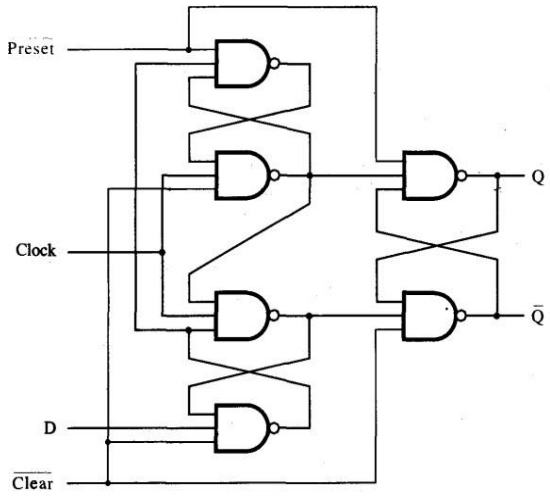

Figure3: Logic circuit a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

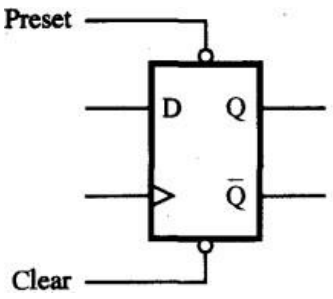

Figure4: Graphical symbol of a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

J-K Flip Flop:

In a J-K flip-flop, there are two control input labeled as J and K and a clock input. It has two outputs Q and Q' as usual. In a positive edge triggered J-K flip-flop, output only changes at the positive edge of the clock depending on the values of J and K. If J=1 and K=0, Q is set to 1. If J = 0, K=1 then Q is set to 0. If J = 0 and K = 0 then Q remains unchanged. If J = 1 and K = 1 then Q changes from its former value, which we can say the output toggles.

We can show the characteristics of a J-K in a table given below.

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	~ Q(t)

J-K flip-flop can be designed easily using D flip-flops.

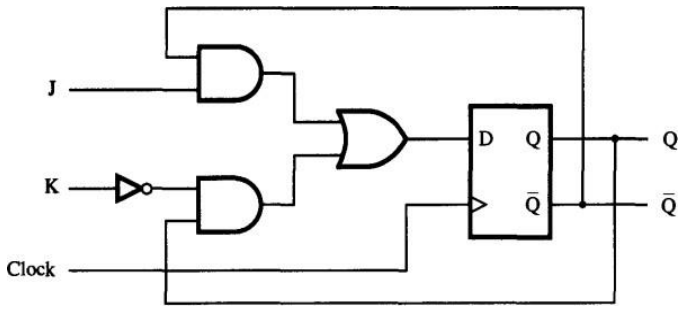

Figure 5: J-K flip-flop using D flip-flop

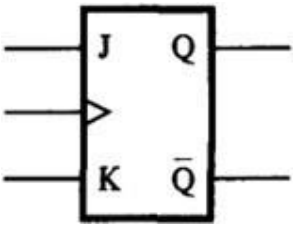

Figure 6: Graphical Symbol of J-K flip-flop.

T Flip-Flop:

A T flip-flop has a control input labeled as T and a clock. The characteristic of a T flip-flop is such that the output toggles at the positive edge of the clock if T is 1. But if T is 0, the output remains unchanged even at the positive edge of the clock.

A T flip-flop can be designed easily by making J and K short of a J-K flip flop.

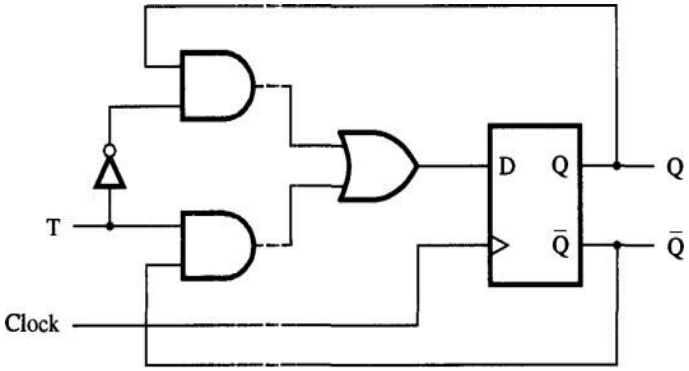

Figure 7: T flip-flop using D flip-flop

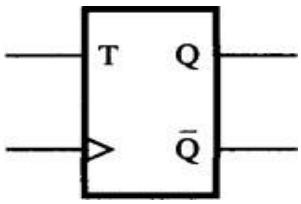

Figure 8: Graphical Symbol of T flip-flop.

There are built-in ICs for D flip-flop and J-K flip-flop. IC-7474 contains 2 D flip-flops and IC-7476 contains 2 J-K flip-flops. The pin configuration of IC-7474 and IC 7476 are given below.

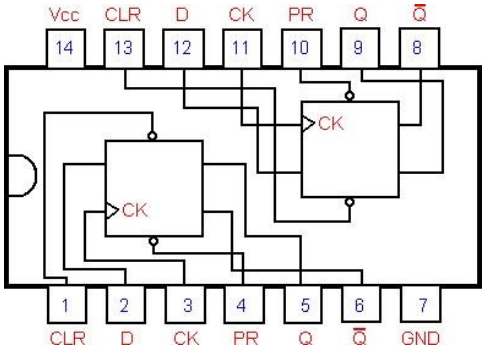

Figure 9: IC-7474

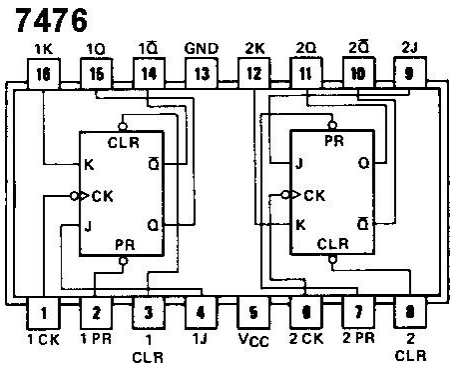

Figure10: IC-7476

Apparatus:

SL	Apparatus	Picture	Quantity	Remarks
1.	Digital trainer board.		1	Good condition
2.	Integrated Circuits (ICs) 7400 (NAND Gate) 7404 (NOT Gate) 7408 (AND Gate) 7432 (OR Gate))		 6 1 2 1	Good condition
3.	7474 (D flip-flop)		1	Good condition
4.	7476 (J-K flip-flop)		1	Good condition
5.	Connecting wires		15	Good condition

Precautions:

It is imperative to ensure that the 'Preset' and 'Clear' functions are not activated at a time. Failure to adhere to this precautionary measure may result in erroneous outcomes.

Experimental Procedure:

The circuits depicted in figures 1, 3, 5, and 7 are to be implemented on the trainer board. The input-output characteristics of these circuits are to be observed. A pulse switch is to be utilized as the clock signal. Following the implementation, timing diagrams shall be generated to illustrate the behavior of the implemented circuits.

Hardware Setup:

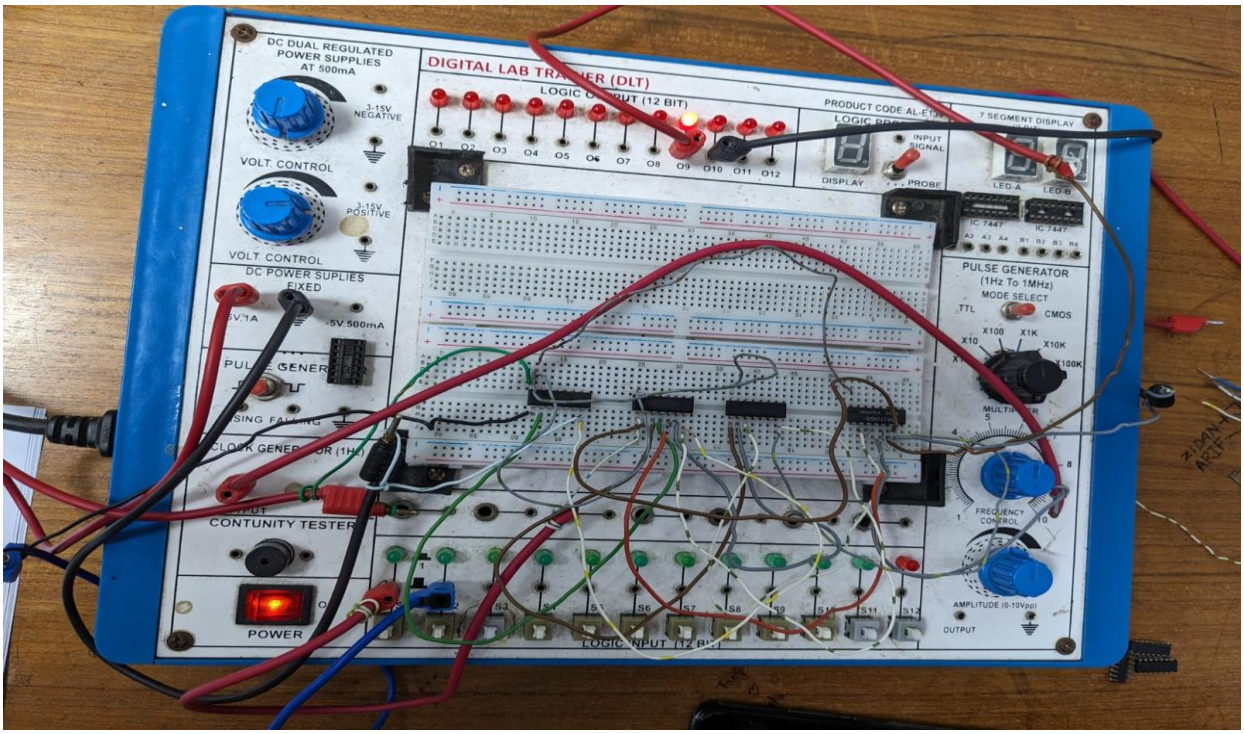

Figure11: J-K flip-flop when input 0 and 0

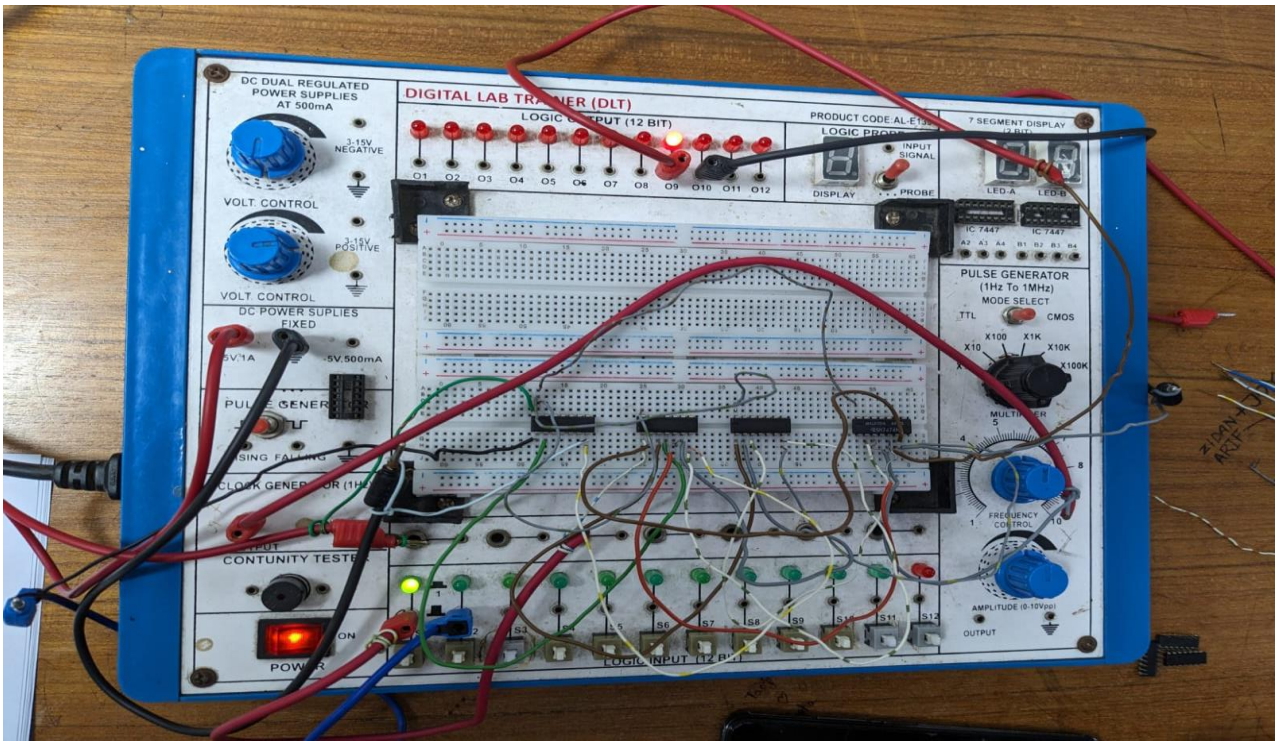

Figure12: J-K flip-flop when input 1 and 0

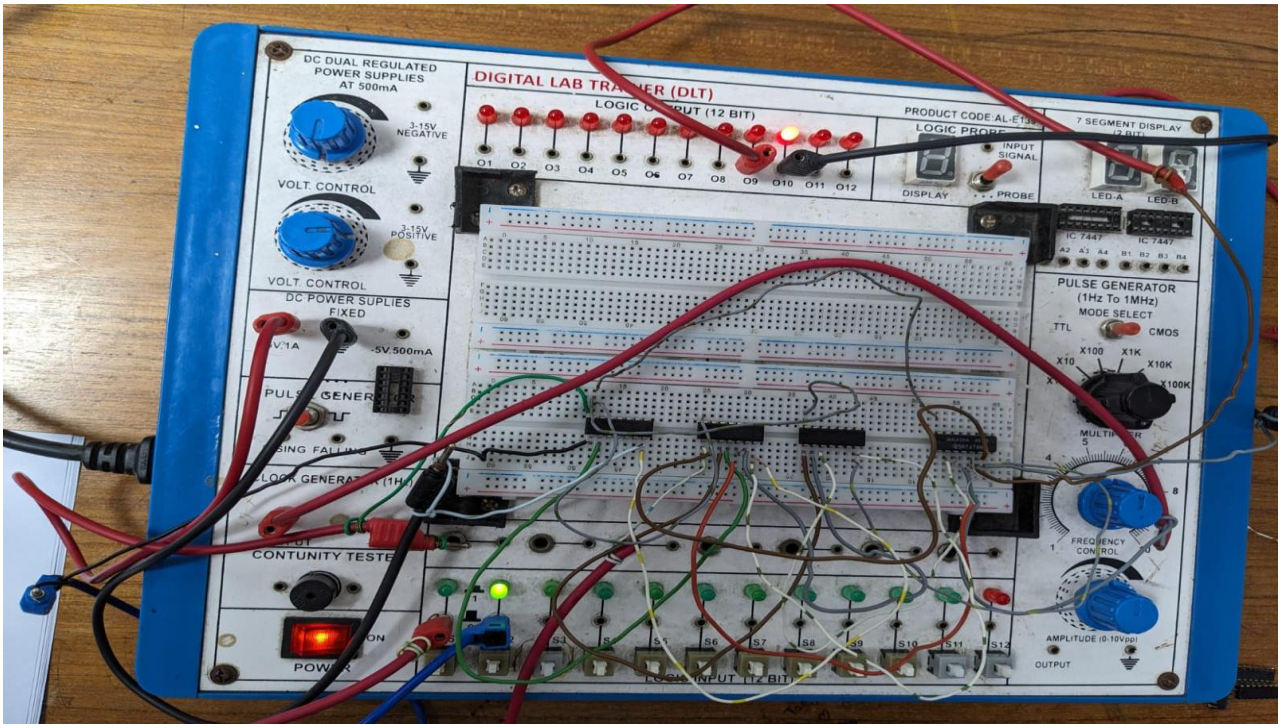

Figure13: J-K flip-flop when input 0 and 1

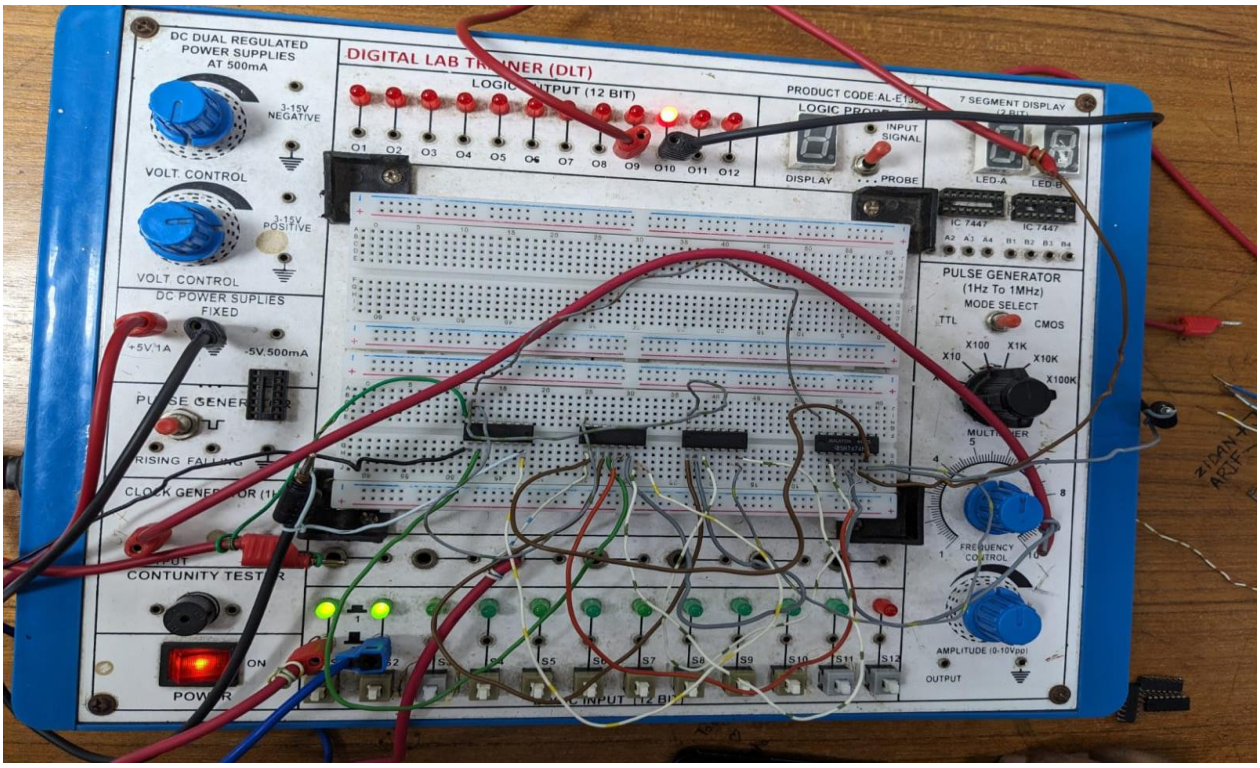

Figure14: J-K flip-flop when input 1 and 1

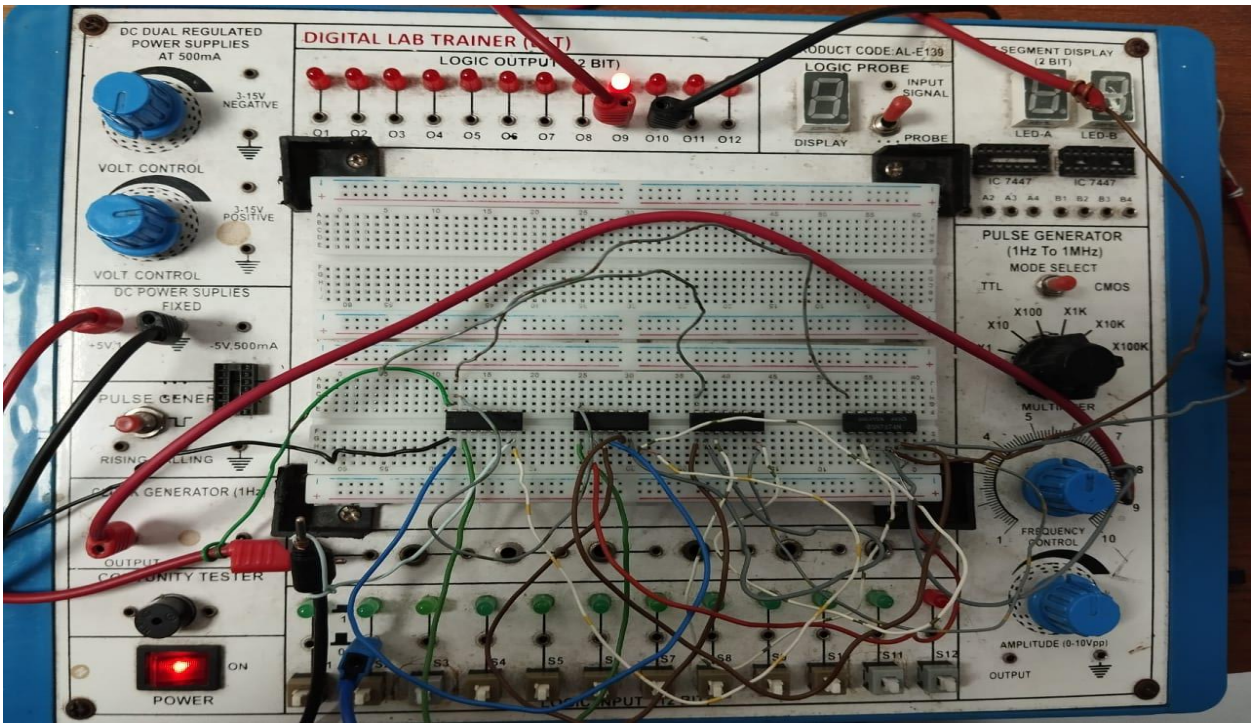

Figure15: T flip-flop when input 0

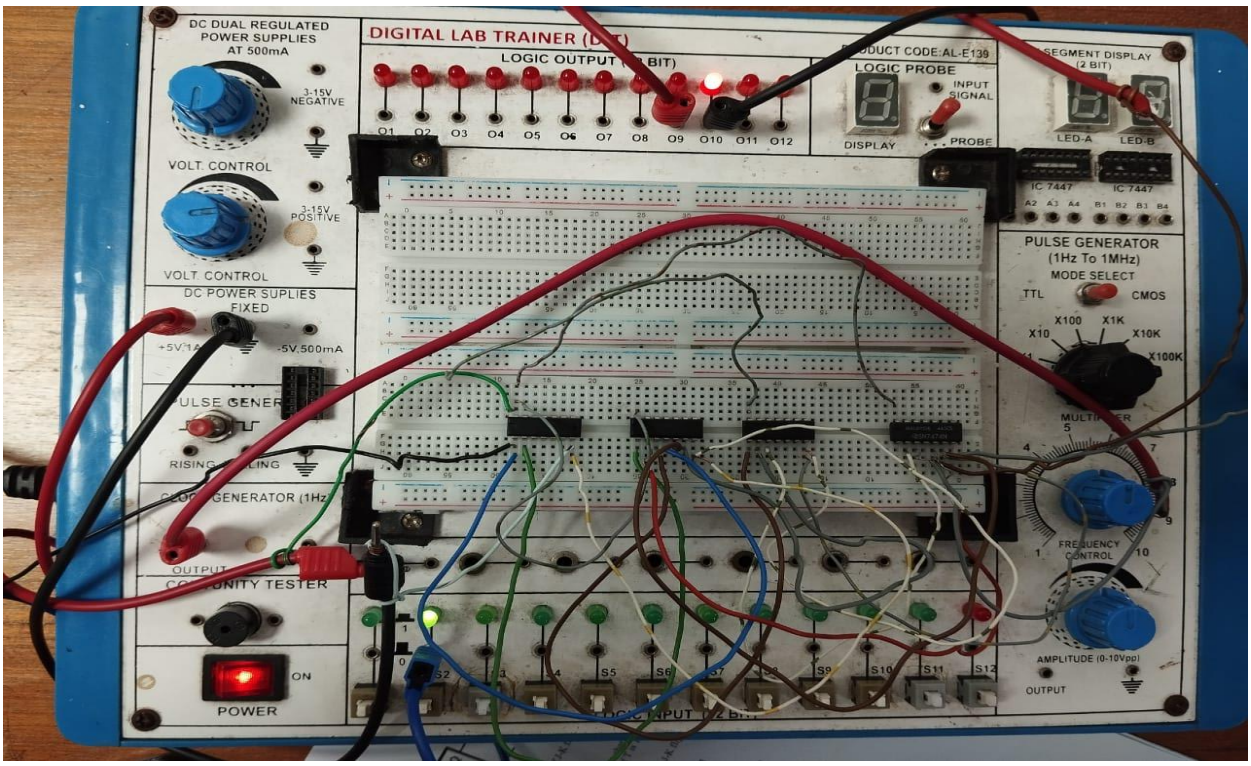

Figure16: T flip-flop when input 1

Simulation and Measurement:

Timing Diagram of a positive edge trigged D flip-flop without 'Preset' and 'Clear' capability:

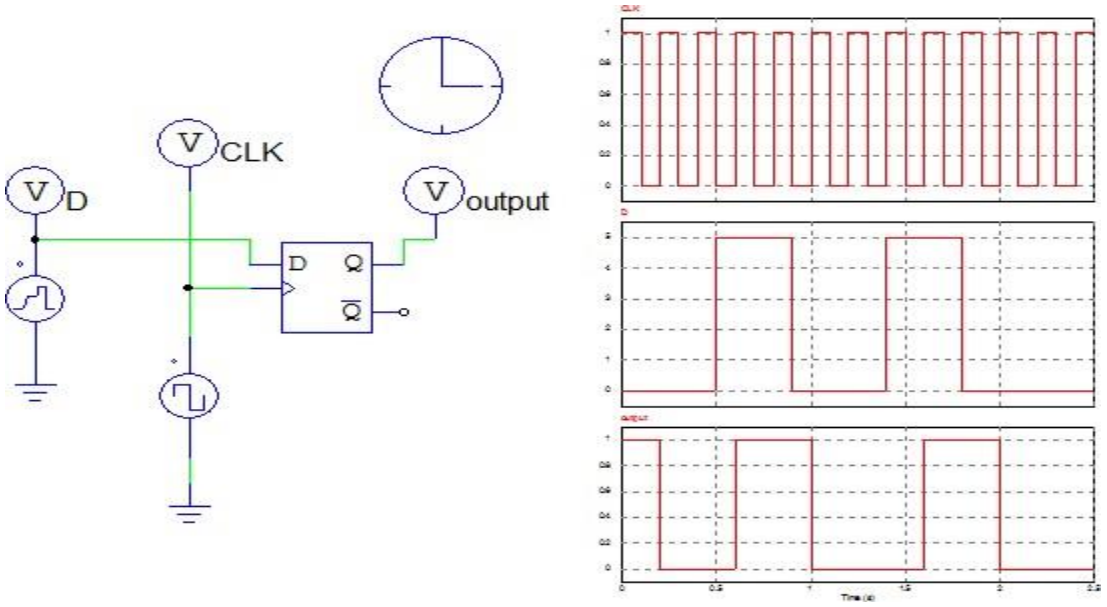

Figure17: Timing Diagram of a positive edge triggered D Flip-Flop without preset and clear capability. Output only samples the input when the clock has a positive edge and remains unchanged for the next positive edge.

Timing Diagram of a positive edge trigged J-K flip-flop:

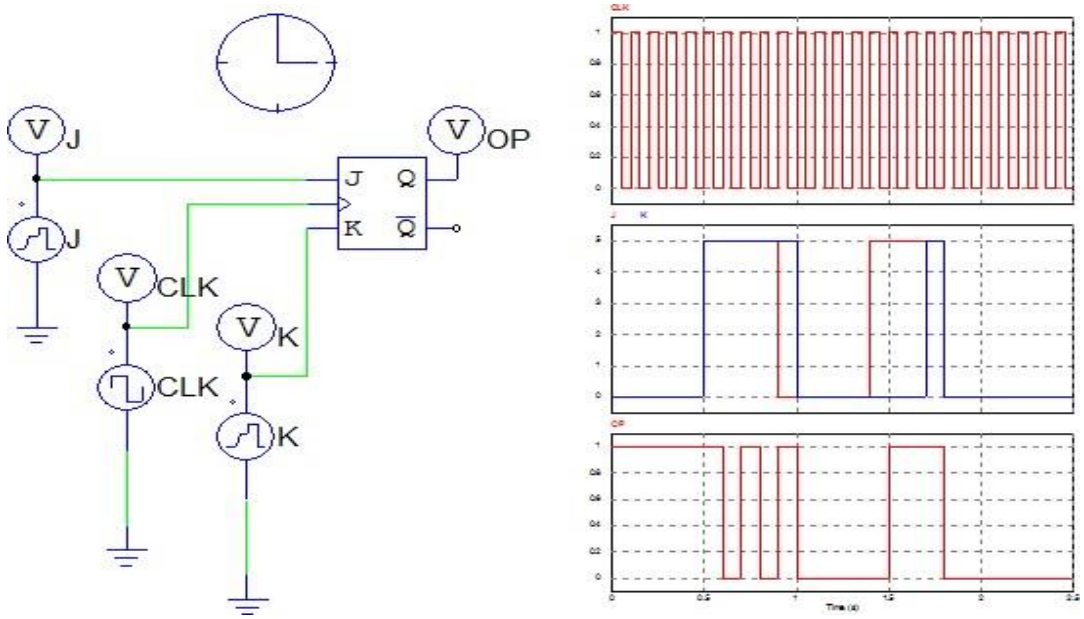

Figure18: Timing Diagram of J-K Flip-Flop

Timing Diagram of a positive edge trigged T flip-flop:

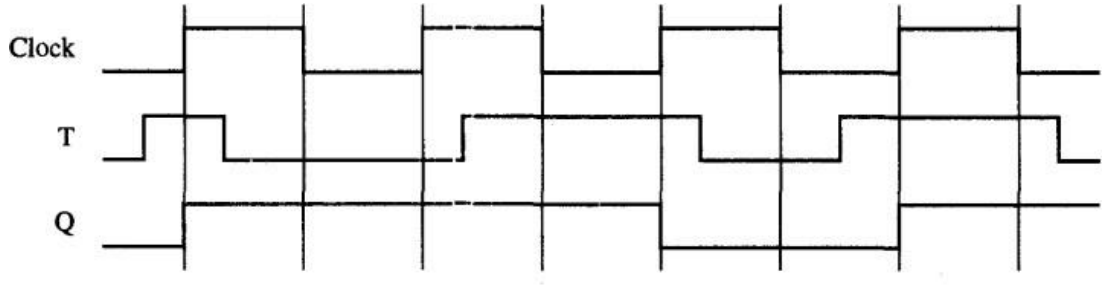

Figure19: Timing Diagram of T-flip-flop

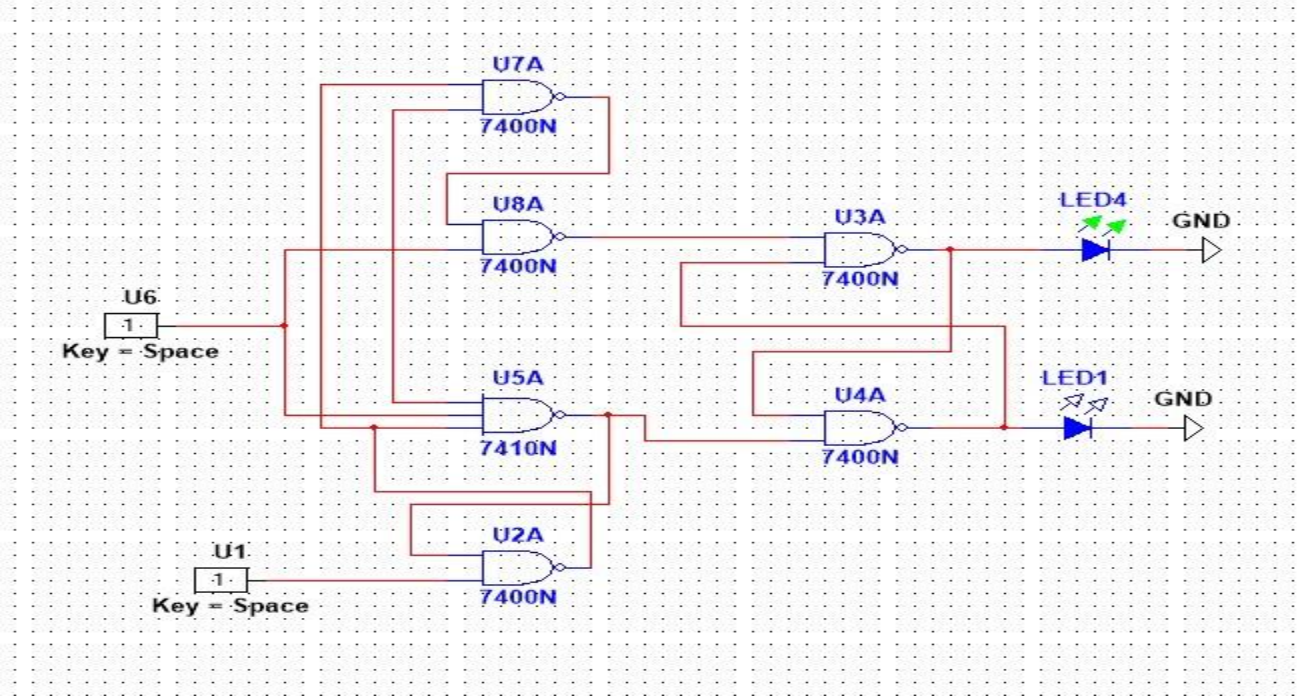

Figure 20: D flip-flop

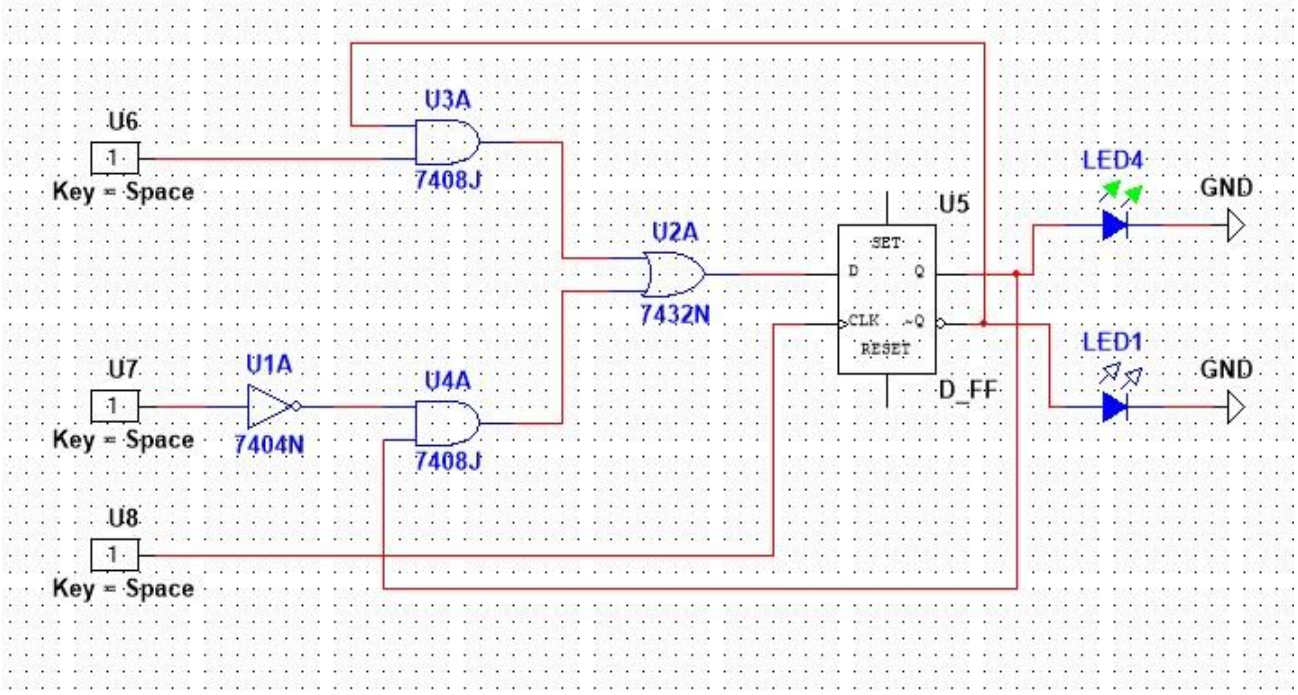

Figure 21: J-K flip-flop using D flip-flop

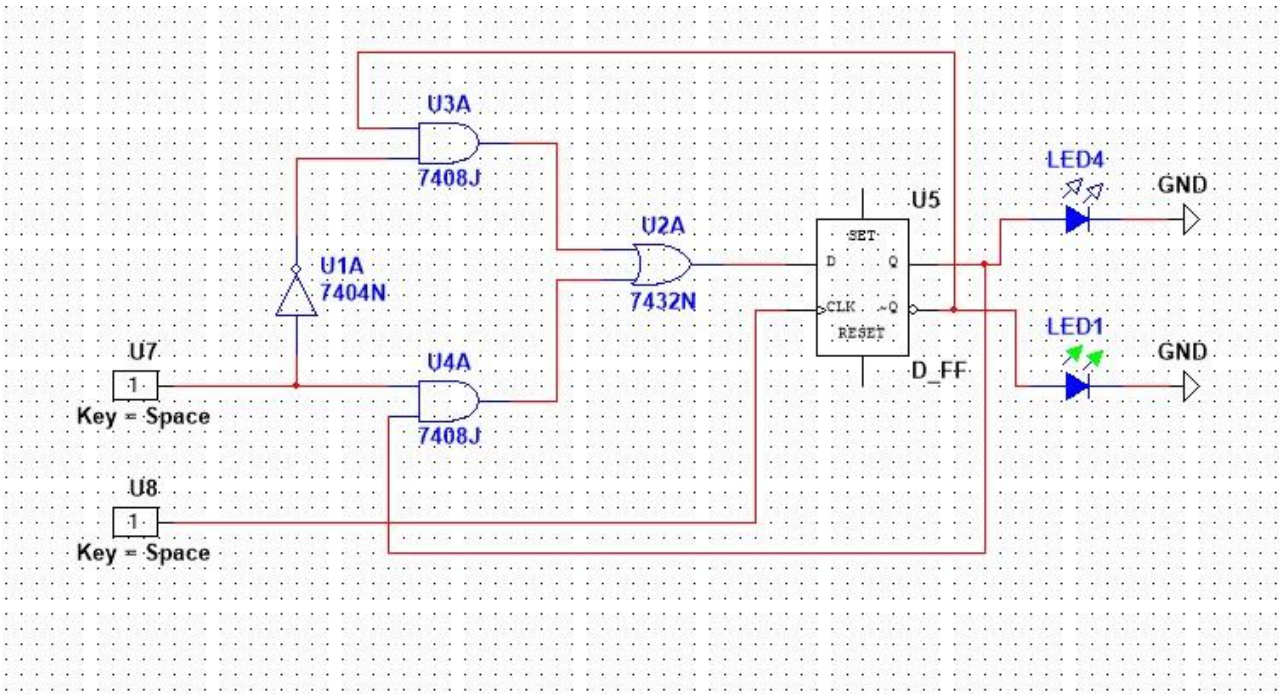

Figure 22: T flip-flop using D flip-flop

Discussion:

During the experiment, we investigated various types of flip-flops, including D, J-K, and T flip-flops, using a pulse switch as the clock signal. We observed distinct characteristics and responses to different input configurations for each type of flip-flop. The D flip-flop stores and outputs the logic level applied to its data terminal when the clock input is high. We also examined the design of positive edge-triggered D flip-flops with and without 'Preset' and 'Clear' capabilities, J-K flip-flops, and T flip-flops, gaining insight into their applications and suitability for different digital circuit designs. Throughout the experiment, we encountered no difficulties, and all tasks proceeded smoothly. NI Multisim version 14.0 software was employed for simulation purposes.

Conclusion:

Upon completion of the experiment, valuable insights were acquired regarding the design and behavior of various flip-flops utilized in digital electronics. Emphasizing a comprehensive understanding of flip-flop functionality as crucial for dependable circuit design, analysis of timing diagrams enriched comprehension of their practical applications. Future applications aim to streamline complex system design and troubleshoot flip-flop-related issues. Further experimentation with different flip-flop types is expected to deepen understanding of digital circuit design principles.

References:

[1] “Fundamentals of Digital Logic with verilog design” by – Brown &Vranesic
[2] www.wikipedia.org
[3] http://www.cs.umd.edu/class/spring2003/cmsc311/Notes/Seq/flip.html
[4] American International University–Bangladesh (AIUB) Digital Logic And Circuits Lab Manual.