Title: Design of adder, subtractor and comparator circuits.

Abstract:

The purpose of this experiment is to learn the design and behaviour of adder, subtractor andcomparator logic circuits. Adders and subtractors are the most basic and most important partof digital electronics.

Part I (Adder and Subtractor):

Adders and subtractors are digital circuits which are capable of adding and subtracting binarydigits. They are the most important part in the design of Arithmetic Logic Unit (ALU). In thisexperiment different types of adders and subtractors will be designed and their behavior willbe observed.

Theory and Methodology:

An adder or summer is a combinational circuit that adds binary numbers. There are mainly two kinds of adders, half adder and full adder. The half adder can add only two single bits ofbinary digit and outputs the sum of the bits and a carry which is the overflow of the sum. A full adder can add two single bit digits and one carry bit which is the overflow of the sum ofthe previous stage of addition and outputs the sum and the carry.

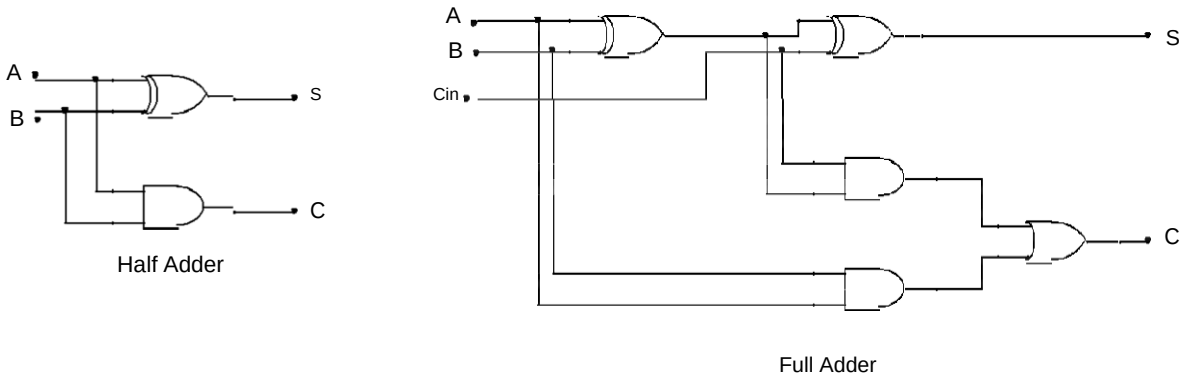


Fig.1.1: Schematics of Half Adder and Full Adder

The Boolean expression for half and full adder is given below –

Half Adder –

$S = A \oplus B$

$C = AB$

Full adder –

$S = A \oplus B \oplus Cin$

$Cout = Cin\ (A \oplus B) + AB$

Truth table for half adder –

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table for full adder –

A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A subtractor is also a combinational circuit that calculates the difference of two binary digits.This is done by taking the two's complement of the subtrahend and then adding it with the minuend. So the subtractor circuit can be designed with the help of adder circuits. Like adders, there are two types of subtractor circuits, half subtractor and full subtractor.

A half subtractor performs a subtraction between two single bits and produces their difference and another output called borrow. A full subtractor performs a subtraction two single bits, taking into account a borrow bit. It outputs the difference of the subtraction and aborrow bit.

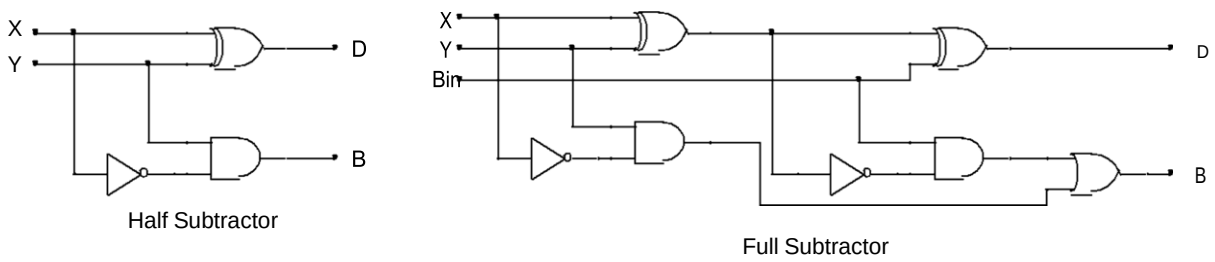


Fig.1.2: Schematics of Half Subtractor and Full Subtractor

The Boolean expressions for half and full subtractor are given below –

Half subtractor –

$D = X \oplus Y$

Bout = X'Y

Full subtractor –

$D = X \oplus Y \oplus Bin$

Bout = X'Y + X'Bin + YBin

Truth table for half subtractor –

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth table for full subtractor –

X	Y	Bin	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Using Full Adder blocks for addition of n- bit systems:

Full adder blocks can be connected for summation of n-bit systems. To design a 2 bit full adder, two 1 bit full adders are connected in parallel connection as shown in the figure below. The same process can be used for designing n-bit Full Adder for addition of words having a length of n-bits.

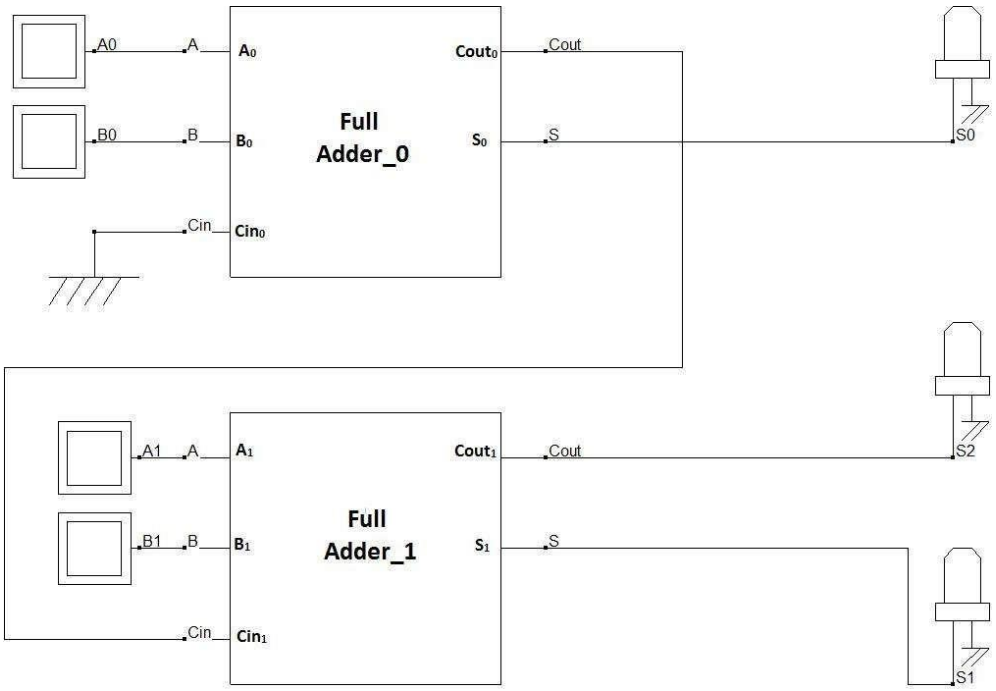


Fig. 1.3: 2-bit Full adder design using 1 bit full adder blocks

Here, the LSB of both word A and B (A0 and B0) are connected in the first stage full adderblock and Cin of this block (Cin0) is connected to ground (as there is no carry in available atthe initial stage). The MSB of both word A and B (A1 and B1) are connected in the first stagefull adder block and Cin of this block (Cin1) is connected to the previous stage Cout (Cout0).Summation output for the LSB is available from the first stage Sum (S0). The next stage block outputs Sum (S1) and Carry out (Cout1) provide the MSBs for the next stage output (S1 and and S2).

Part II (Comparator):

A magnitude comparator is a device that takes in two sets of inputs in its input and compares them to provide an output, if they are equal, greater than or less than the other. Inthis experiment 1-bit comparator will be designed at first and using the 1-bit comparator block, 2-bit comparator will be designed.

Theory and Methodology:

Magnitude Comparators are combinational logic circuits that take 2 sets of data as its inputs and tests whether the value represented by one binary word is greater than, less than, or equal to the value represented by another binary word.

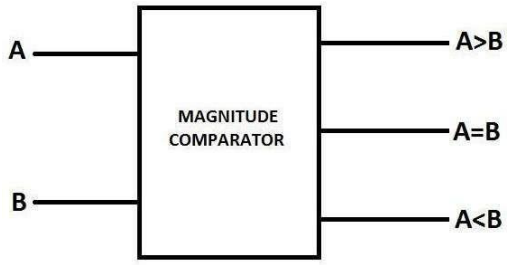


Fig.2.1: Block Diagram of 1 Bit Magnitude Comparator

Depending on the input combination for a 1-bit magnitude comparator, following behavior table can be developed using the logic expressions.

A=B if, A=B=0 or A=B=1;
A>B if A=1 and B=0;
A<B if A=0 and B=1;

		A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

The SOP expressions for the output lines can be written as

(A=B) = A'B'+AB;
(A<B)= AB';
(A>B) =A'B;

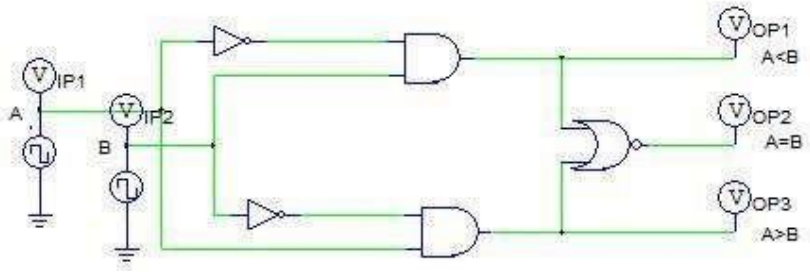


Fig.2.2: 1-Bit Comparator

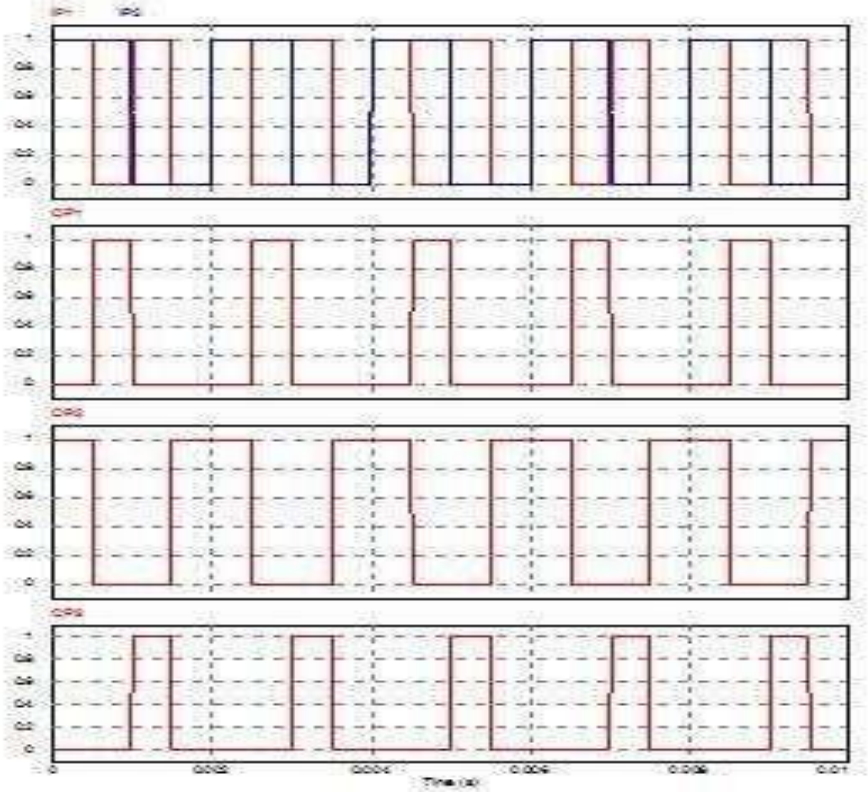


Fig.2.3: Timing Diagram for 1-Bit

Comparator **2 Bit Comparator design using 1 bit block:**
Using 1-bit blocks, n-bit Magnitude comparator can be designed.

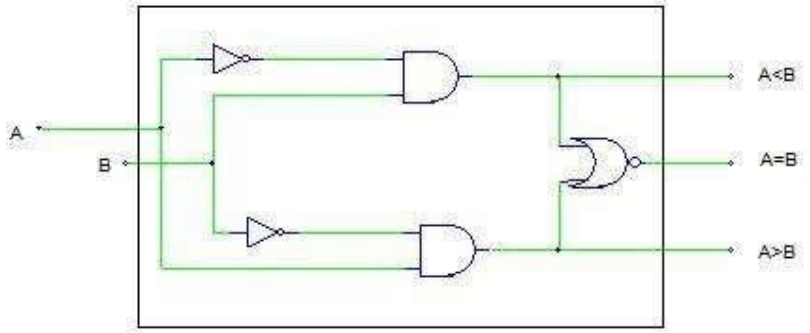


Fig.2.4: 1-Bit Comparator Block

Designing a 2-bit comparator using 1-bit blocks:

Let us consider 2 words,

Word A -> A_1A_0
Word B-> B_1B_0

For comparing, the following process is used as writing the logic equations.

For A=B,
If (A1=B1) & (A0=B0), then (A=B);

For A>B,
If (A1>B1) then (A>B) or
if (A1=B1) & (A0>B0), then (A>B);

For A<B,
If (A1<B1) then (A<B) or
if (A1=B1) & (A0<B0), then (A<B)

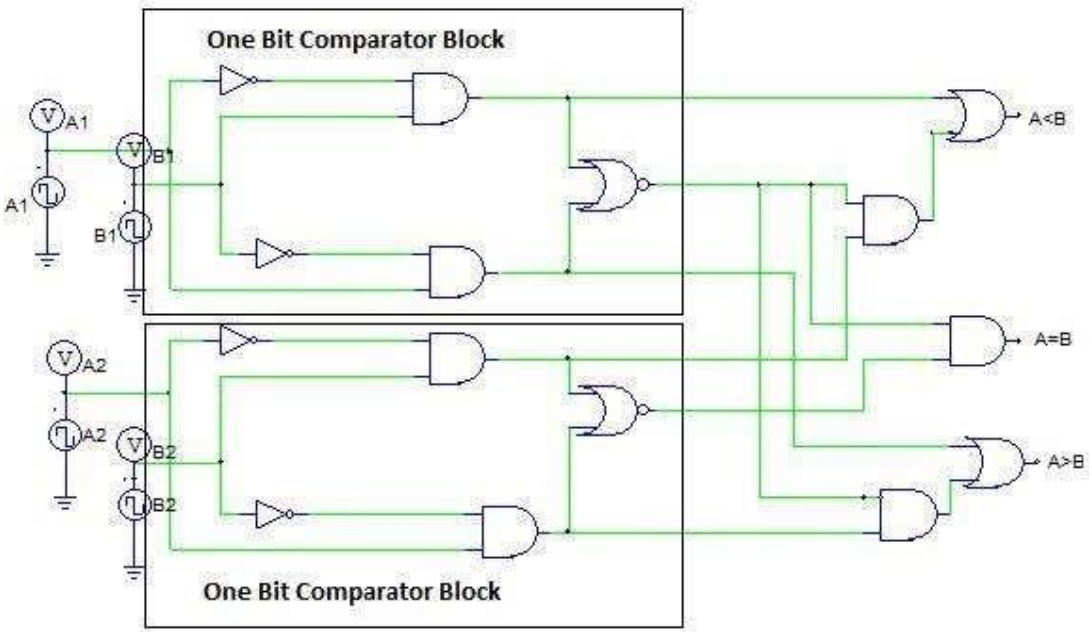


Fig.2.5: 2-Bit Comparator using 1_bit Comparator Block

For designing a 2-bit comparator using 1-bit comparator block, 2 1-bit comparator block, 3 AND gateand 2 OR gate is needed as shown in Fig.4.

Apparatus:

SL	Apparatus	Picture	Quantity	Remarks
1.	Digital trainer board.		1	Good condition
2.	Integrated Circuits (ICs) 7400 7402 7404 7408 7432 7486		 1 1 2 2 2 2	Was not in good condition. Had to change it.
3.	Power Supply		1	Good condition
4.	Connecting wires		multiple	Good condition

Precautions:

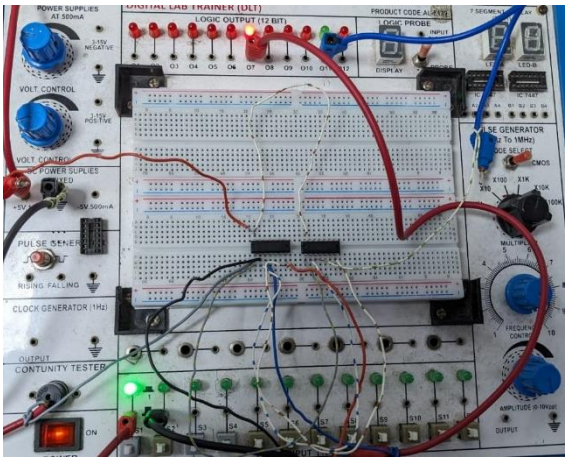
1. All LEDs and toggle switches of the trainer board were ensured to be working properly.
2. Connections were not shorted, as short connections can produce heat due to high current flow, which is harmful to the components.

Experimental Procedure:

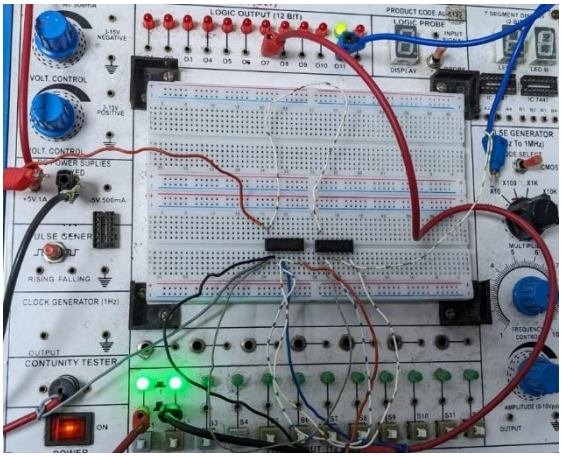
1. The output and truth tables of the logic circuits for full adder and half subtractor provided in the theory and methodology section were determined.
2. The necessary gates and their quantities were determined, and all the IC numbers were checked and identified.
3. The ICs were carefully placed on the Trainer Board and biased by connecting them to the +5 volt DC supply and ground.
4. The ICs were connected using wires according to the logic diagram, and the outputs were connected to the LEDs.
5. The outputs were checked and recorded by providing different inputs in accordance with the derived truth table.
6. A 4-bit full adder was designed using IC 7483, and its operation was verified.

Simulation and Measurement:

Experimental Setup:

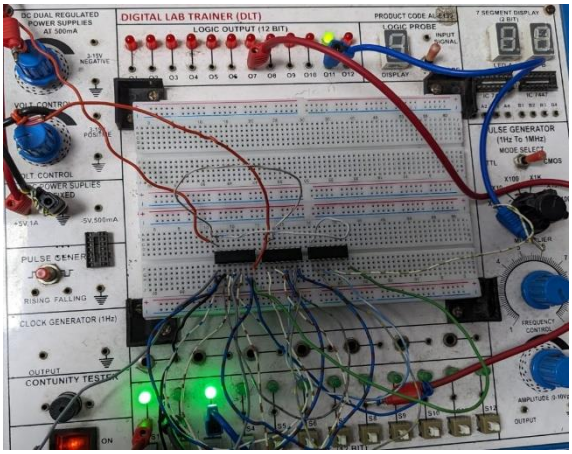


a) For A=1, B=0 output S=1, C=0.

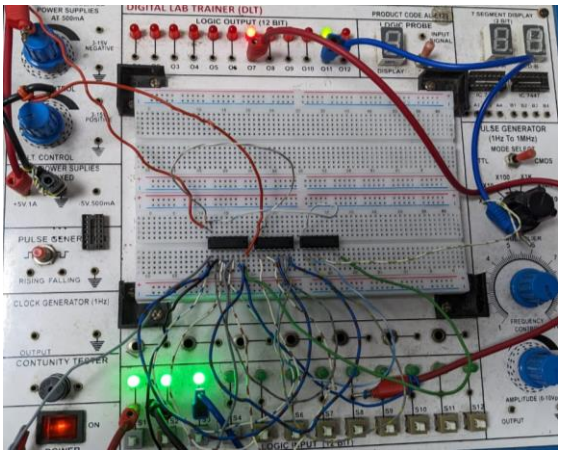


b) For A=1, B=1 output S=0, C=1.

Fig-03: Implementing Half Adder Circuit

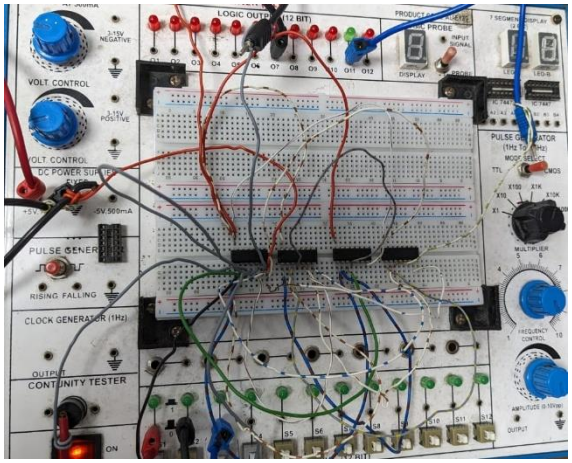


a) For A=1, B=0 & C_{in}=1 output S=0, C=1.

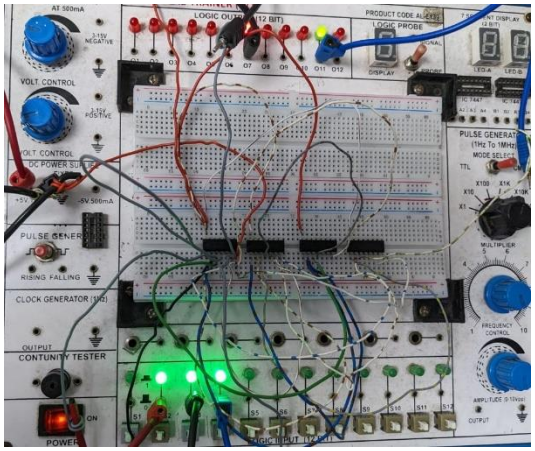


b) For A=1, B=1 & C_{in}=1 output S=1, C=1.

Fig-04: Implementing Full Adder Circuit

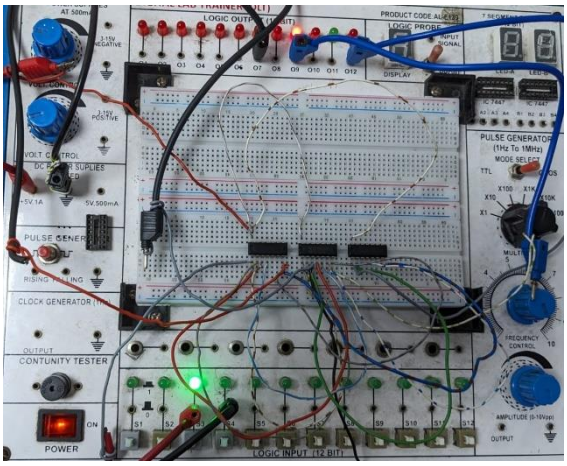


a) For A=0, B=0 & B_{in}=0 output D=0, B=0.

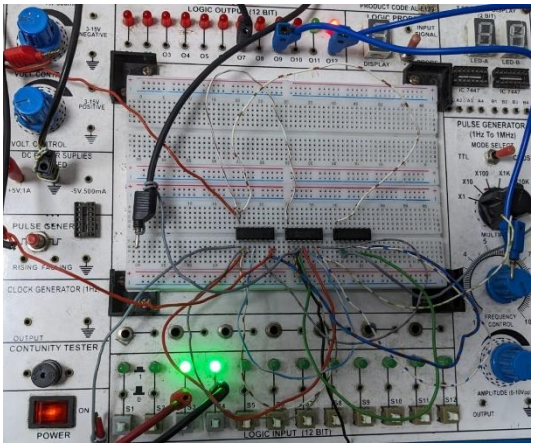


b) For A=1, B=1 & B_{in}=1 output D=1, B=1.

Fig-05: Implementing Full Subtractor Circuit



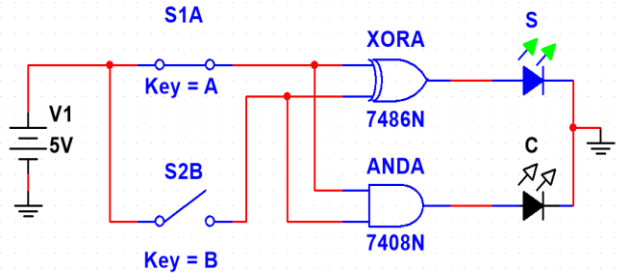
a) For A=1, B=0 output A>B.



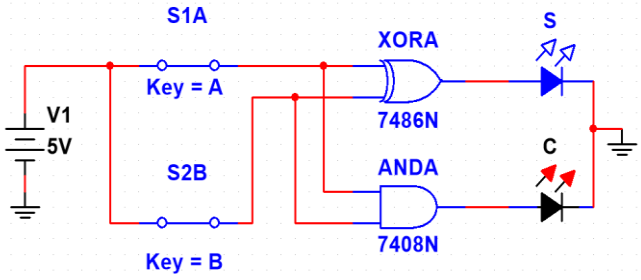
b) For A=1, B=1 output A=B.

Fig-06: Implementing 1 bit comparator Circuit

Simulations:

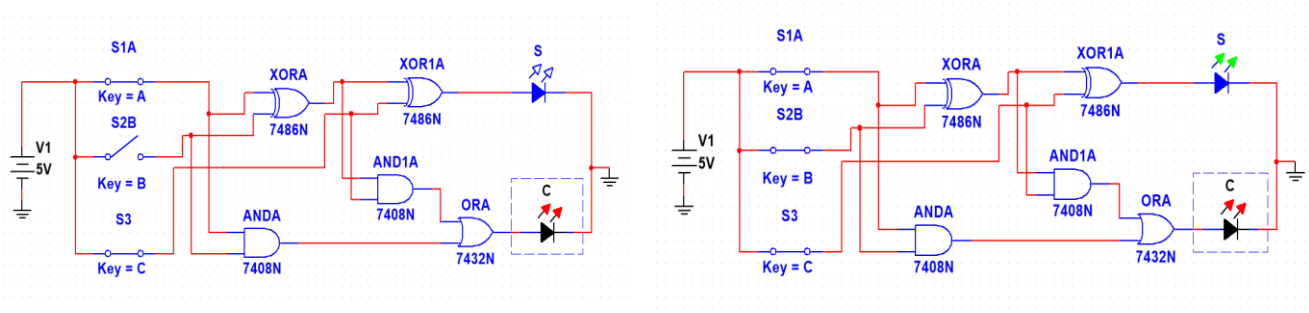


a) For A=1, B=0 output S=1, C=0.



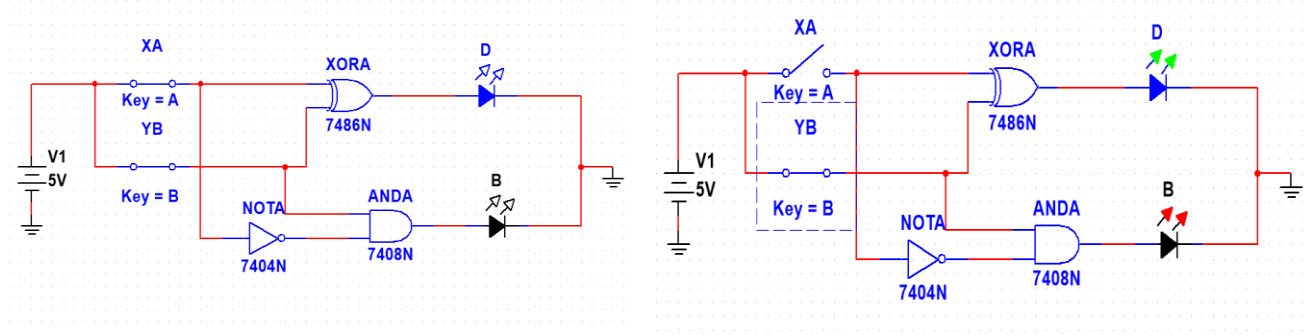
b) For A=1, B=1 output S=0, C=1.

Fig-07: Implementing Half Adder Circuit



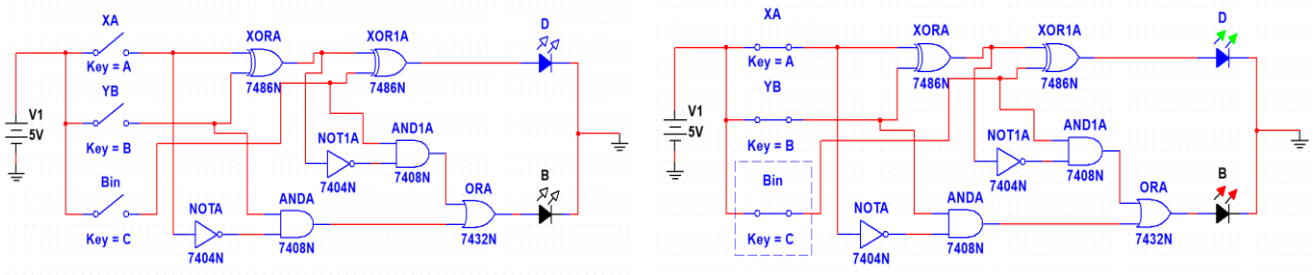
a) For A=1, B=0 & C_{in}=1 output S=0, C=1. b) For A=1, B=1 & C_{in}=1 output S=1, C=1.

Fig-08: Implementing Full Adder Circuit



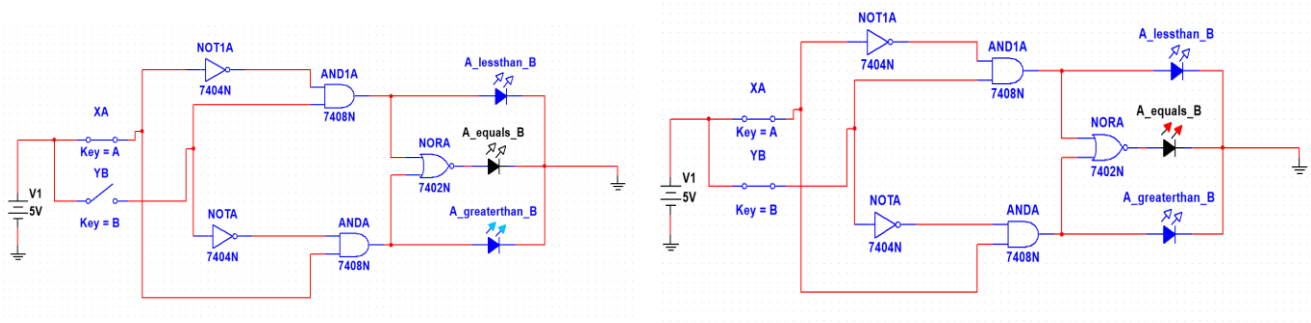
a) For A=1, B=1 output D=0, B=0. b) For A=0, B=1 output D=1, B=1.

Fig-09: Implementing Half Subtractor Circuit



a) For A=0, B=0 & B_{in}=0 output D=0, B=0. b) For A=1, B=1 & B_{in}=1 output D=1, B=1.

Fig-10: Implementing Full Subtractor Circuit



a) For A=1, B=0 output A>B. b) For A=1, B=1 output A=B.

Fig-11: Implementing 1 bit comparator Circuit.

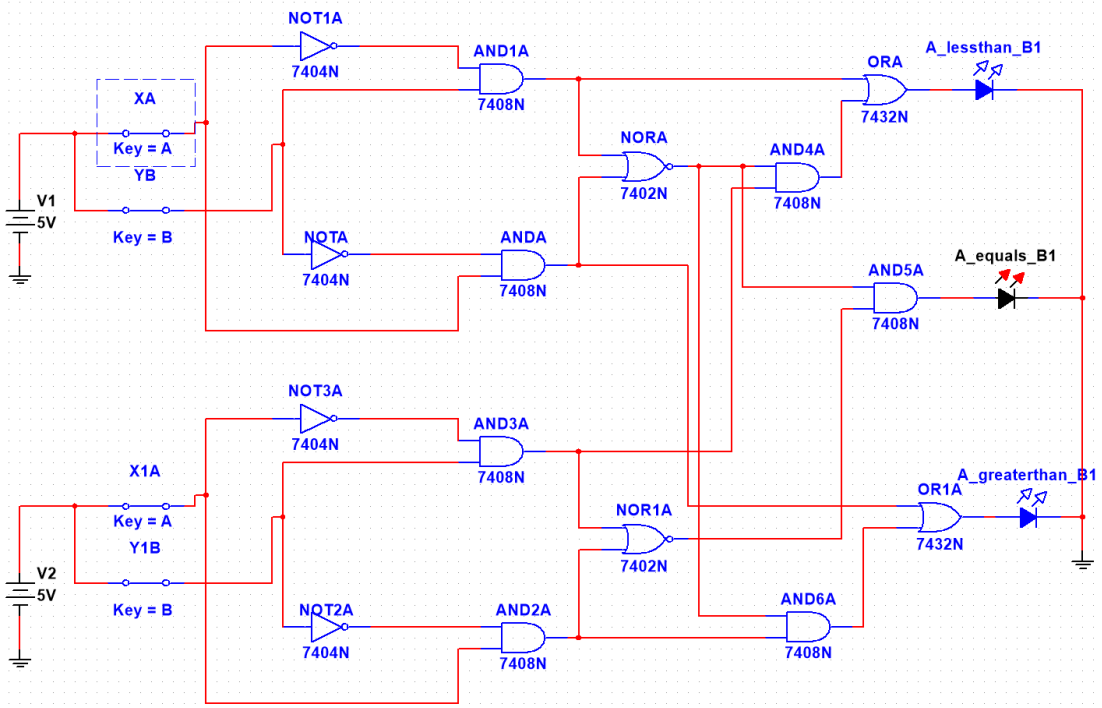


Fig-12: Implementing 2-bit comparator circuit using 1_bit comparator block.

Questions with answers for report writing:

1. Design a full adder circuit for performing 3-bit binary addition.

   Ans: Figure 11 shows the 3-bit full adder circuit.

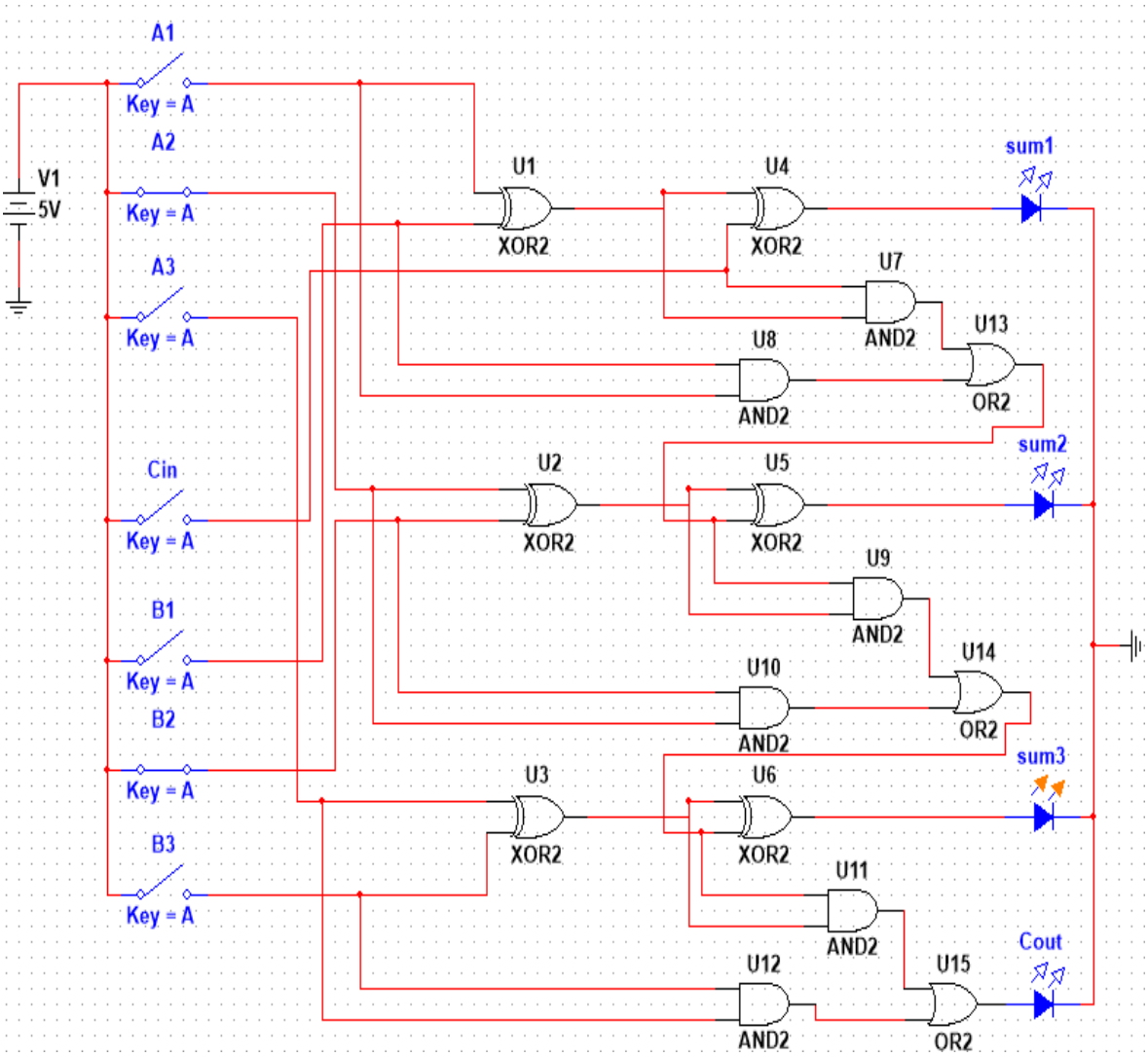


Figure 13: 3-bit full adder circuit

2. Design a full subtractor circuit for performing 3-bit binary subtractor.

   Ans: Figure 12 shows the 3-bit subtractor circuit.

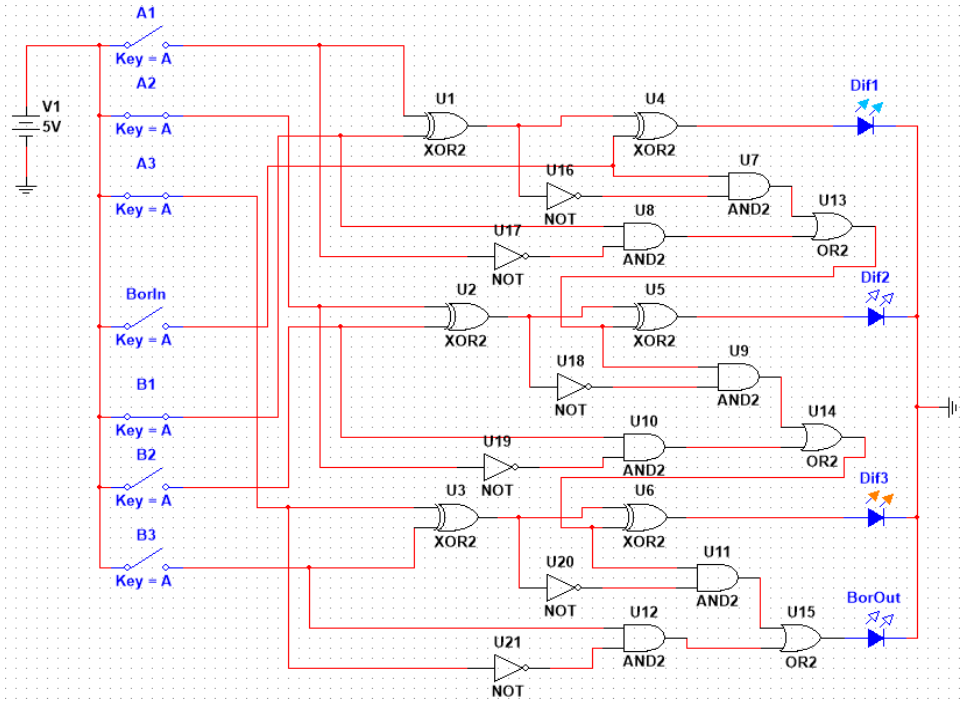


Figure 14: 3-bit full subtractor circuit.

3. Design an 8-bit full adder using 4-bit full adder IC 4008 from PSIM.

   Ans: An 8-bit full adder was designed and shown in figure 13 using two 4-bit adder IC using Multisim.

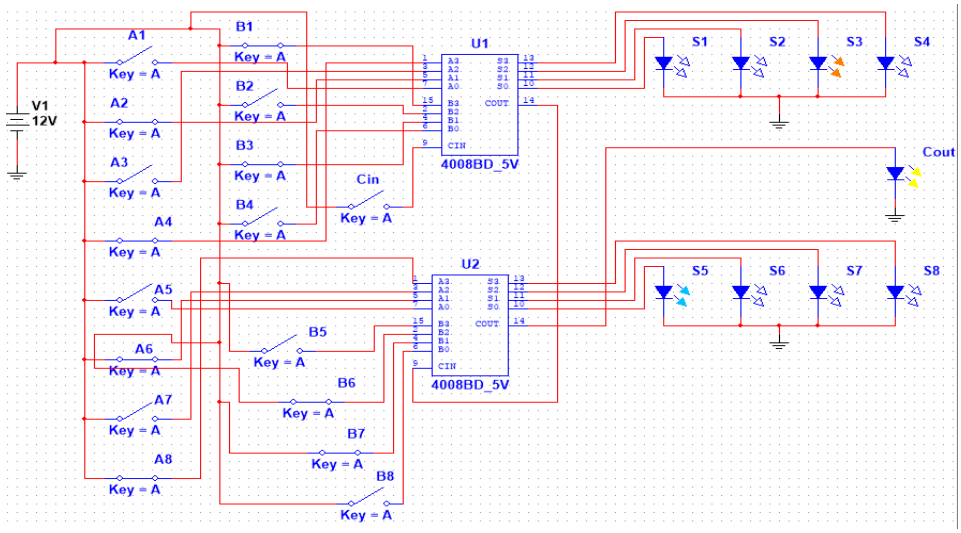


Figure 15: 8-bit full adder circuit using two 4-bit adder IC.

4. Design a comparator circuit for comparing two words, each of 3 bits of input using 1 bitblock.
   Ans: The comparator circuit is given in figure 14. The 7485N 4 bit comparator IC was used with its last remaining pins being disconnected.

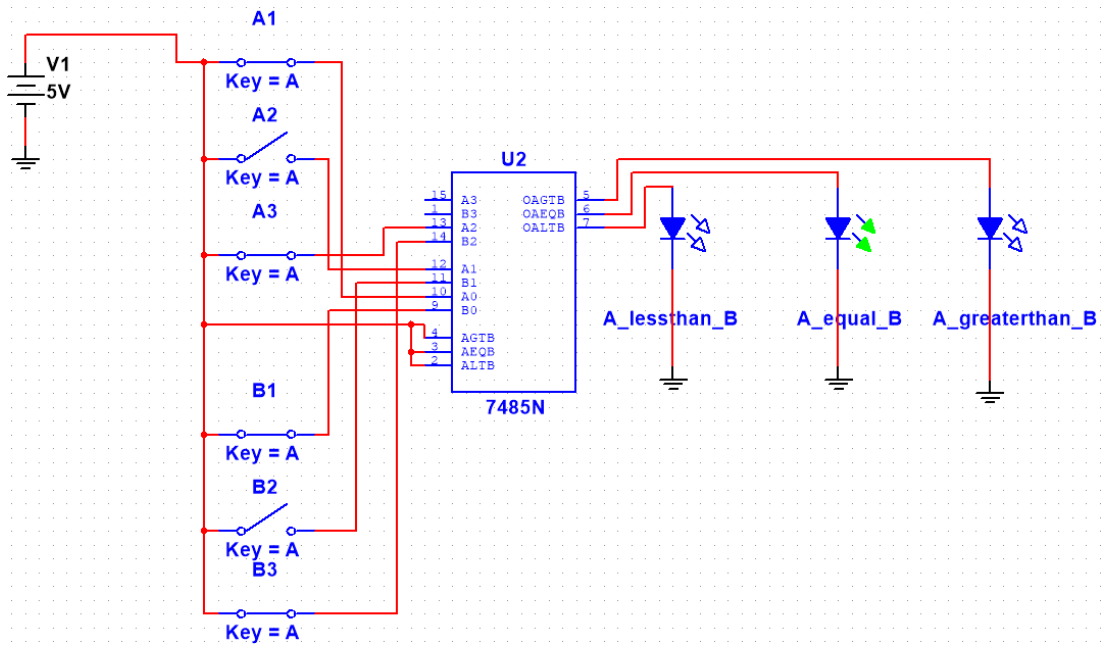


Figure 16: Simulation and design of a 3-bit comparator circuit using 7485 N IC.

Discussion:

With the guidance of our lab teacher, the construction of the half adder, full adder, full subtractor, and 1-bit comparator was successfully completed on the breadboard during our experiment. The process proceeded smoothly without any errors, making it easy to follow. Our work was double-checked by verifying the truth table, and it matched perfectly, confirming the accuracy of our circuit. NI Multisim version-14.2 software was utilized for simulation, and No issues with the circuit design was found through simulations.

Conclusion:

Upon completion of the experiment, a comprehensive understanding of half adder, full adder, full subtractor, and 1-bit comparator has been acquired. The simulation process has provided practical insights into the functioning of these circuits. Through simulation exercises, hands-on experience has been gained, enabling observation of the correlation between theoretical truth table concepts and actual results. This experience has significantly improved understanding of truth table construction and interpretation.

References:

[1] www.tutorialspoint.com
[2] www.electronics-tutorials.ws
[3] faculty.kfupm.edu.sa
[4] “Digital Fundamentals” by Thomas L. Floyd
[5] American International University–Bangladesh (AIUB) Digital Logic And Circuits Lab Manual.

Appendix:

Pin configuration of IC 74LS83

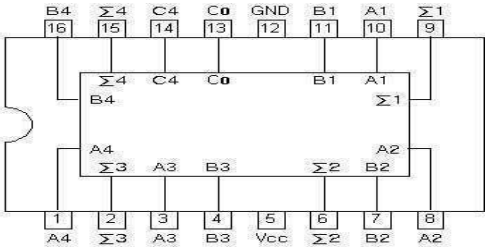


Fig. : 4-bit Full Adder IC pin configuration

Pin configuration for IC-74LS85