AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH

Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Laboratory Title : Implementation of Asynchronous and synchronous counters using flip-flops.

Experiment Number: 7 Due Date: 28-04-24 Semester: Spring 23-24

Subject Code:0067 Subject Name: **Digital Logic And Circuits Lab** Section: R

Course Instructor: Md. Ashiquzzaman Degree Program: CSE

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American International University-Bangladesh
Department of Electrical and Electronic Engineering
EEE 3102: Digital Logic & Circuits Laboratory

Title: Implementation of Asynchronous and synchronous counters using flip-flops.

Introduction:

Counters are combinations of flip-flops arranged so that they can remember how many clock pulses have been applied over some specified interval. The flip-flops are often interconnected so that only a portion of their available binary states can be supported. If there are N flip-flops being used in a counter, the number of states available is 2N. If the counter proceeds cyclically through K of these states, where $K \leq 2N$, it is said to be a modulo K (or MOD K) counter. Some applications will require a separate output to indicate each of the counters states, alternatively, other applications may require only one output pulse every Kth state.

Counters are classified into two broad categories according to the way they are clocked: **asynchronous and synchronous.** In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip flop is clocked by the output of the preceding flip-flop. In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.
The objective of this experiment is designing of the following counters using J-K Flip-Flops (IC 74LS76)
(a) n-bit Binary Asynchronous Counter
(b) n-bit Binary Synchronous Counter

Theory and Methodology:

Asynchronous counter

A three-bit asynchronous counter is shown in the figure 9.1. The external clock is connected to the clock input of the first flip-flop (FF0) only. So, FF0 changes state at the falling edge of each clock pulse, but FF1 changes only when triggered by the falling edge of the Q output of FF0. Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF0 can never occur at exactly the same time. Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation.

Figure 9.1 gives a three-bit counter capable of counting from 0 to 7. The clock inputs of the three flip-flops are connected in cascade. The T input of each flip-flop is connected to a constant 1, which means that the state of the flip-flop will be reversed (toggled) at each positive edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary input called Clock. Thus the clock input of the first flip-flop is connected to the Clock line. The other two flip-flops have their clock inputs driven by the Q output of the preceding flip-flop. Therefore, they toggle their state whenever the preceding flip-flop changes its state from Q = 1toQ = 0, which results in a positive edge of the Q signal.
Figure 9.1 shows a timing diagram for the counter. The value of Q0 toggles once each clock cycle. The change takes place shortly after the positive edge of the Clock signal. The delay is caused by the propagation delay through the flip-flop. Since the second flip-flop is clocked by Q0, the value of Q1 changes shortly after the negative edge of the Q0 signal. Similarly, the

value of Q2 changes shortly after the negative edge of the Q1 signal. If we look at the values Q2Q1Q0 as the count, then the timing diagram indicates that the counting sequence is 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, and so on. This circuit is a modulo-8 counter. Because it counts in the upward direction, we call it an up-counter.

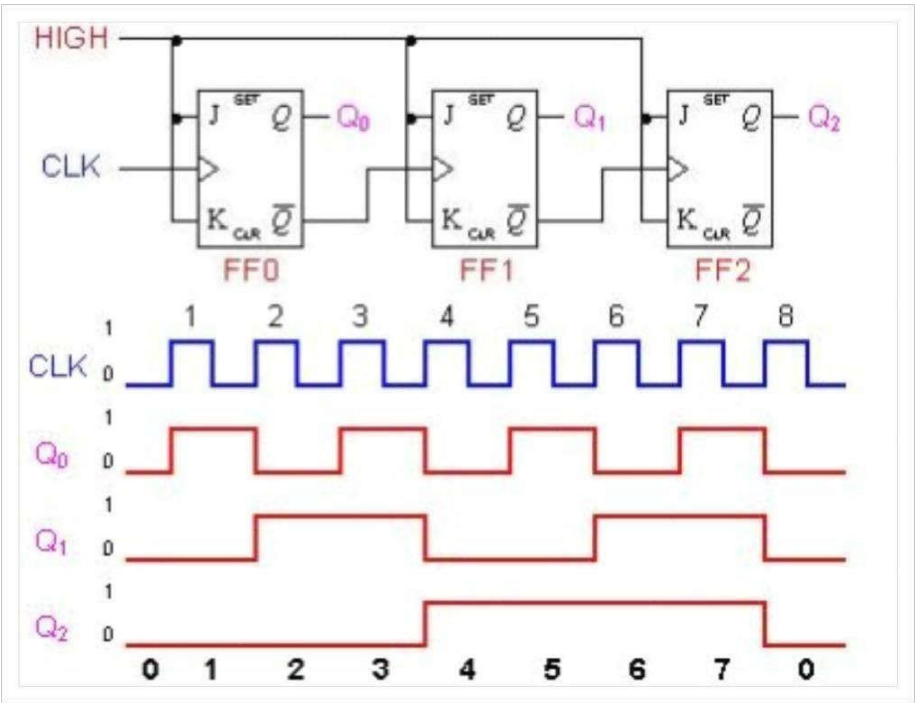

Figure 9.1: 3 bit Asynchronous counter and its timing diagram

Synchronous counter

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The most important advantage of synchronous counters is that there is no cumulative time delay because all flip-flops are triggered in parallel. Thus, the maximum operating frequency for this counter will be significantly higher than for the corresponding ripple counter.

Table 9.1 shows the contents of a four-bit up-counter for eight consecutive clock cycles, assuming that the count is initially 0. Observing the pattern of bits in each row of the table, it is apparent that bit Q0 changes on each clock cycle. Bit Q1 changes only when Q0 = 1. Bit Q2 changes only when both Q1 and Q0 are equal to 1. In general, for an n-bit up-counter, a given flip-flop changes its state only when all the preceding flip-flops are in the state Q = 1.

T0 = 1

T1 = Q0
T2 = Q0Q1
T3 = Q0Q1Q2
T4= Q0Q1Q2Q3
.
.
.
Tn = Q0Q1 ⋯Qn−1

Clock cycle	Q_2 Q_1 Q_0
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1
8	0 0 0

Q_1 changes

Q_2 changes

The Circuit diagram of a four-bit counter based on these expressions is given in Figure 9.2a. Figure 9.2b gives a timing diagram. It shows that the circuit behaves as a modulo-16 up-counter. Because all changes take place with the same delay after the active edge of the Clock signal, the circuit is called a synchronous counter.

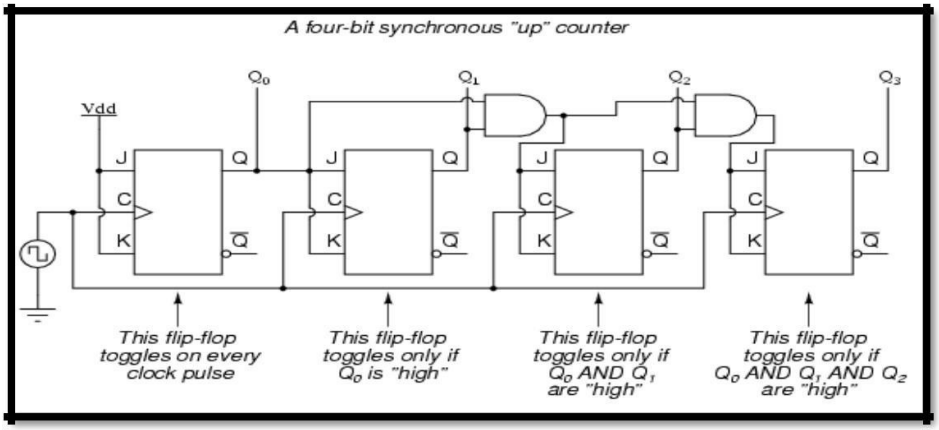

Figure 9.2a: A four-bit Synchronous Up Counter

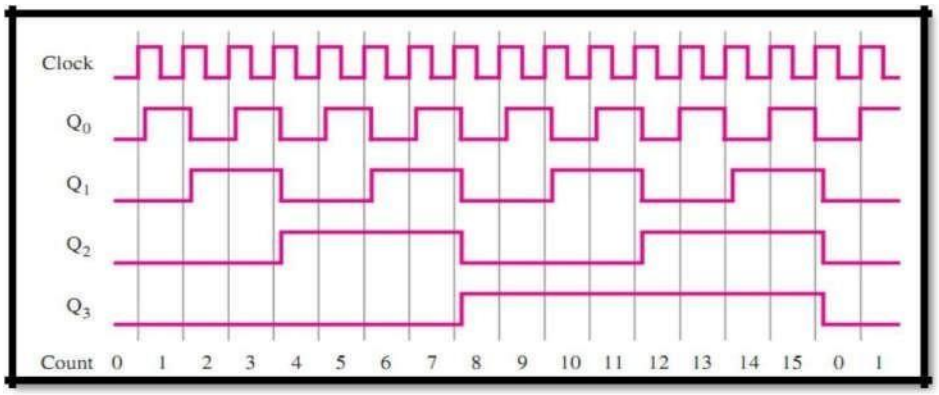

Figure 9.2b: The timing diagram of a four-bit Synchronous Up Counter

Pin Configuration of 74LS76 and 7408

There are 2 J-K Flip Flops in one IC. Here is the pin configuration of the IC 74LS76:

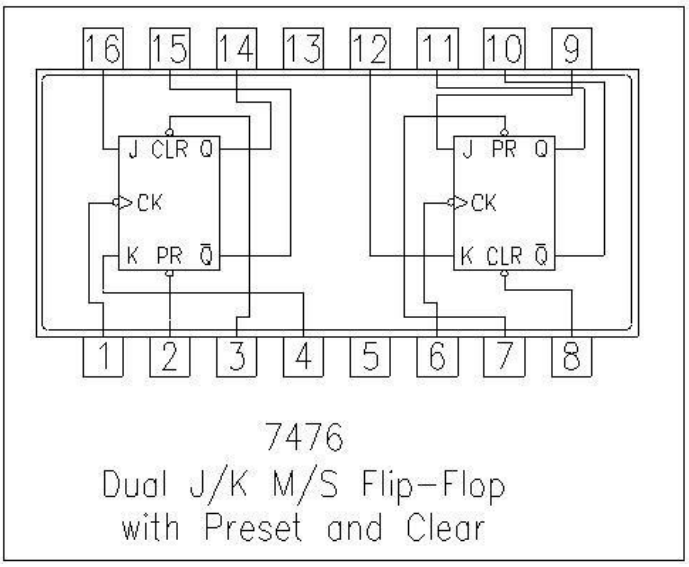

Figure 9.3: IC 74LS76

IC 7408 contains 4 AND gates in it. The pin configuration is shown below:

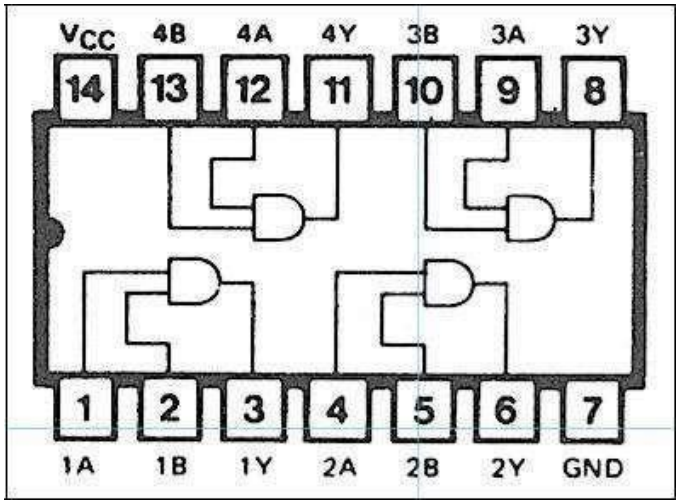

Figure 9.4: IC 7408

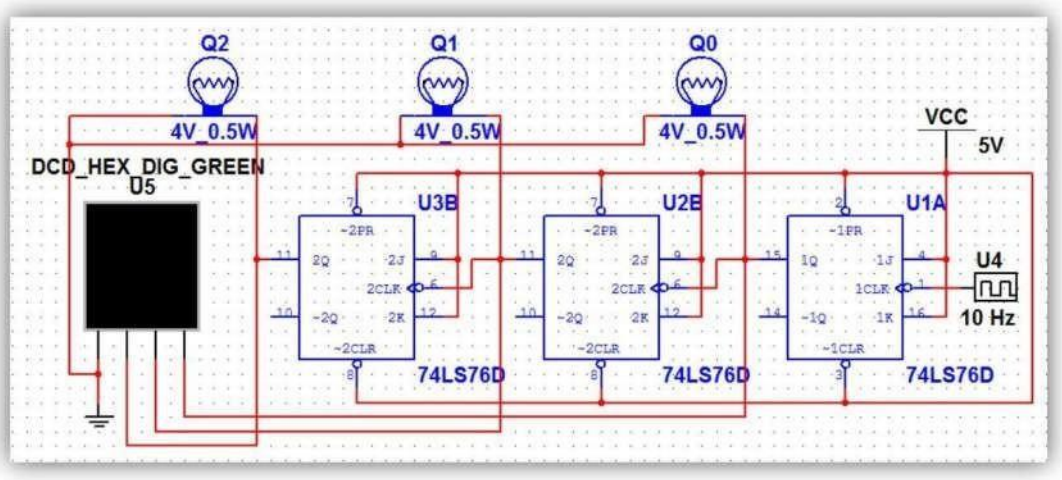

Fig 9.5: 3 bit Asynchronous Counter

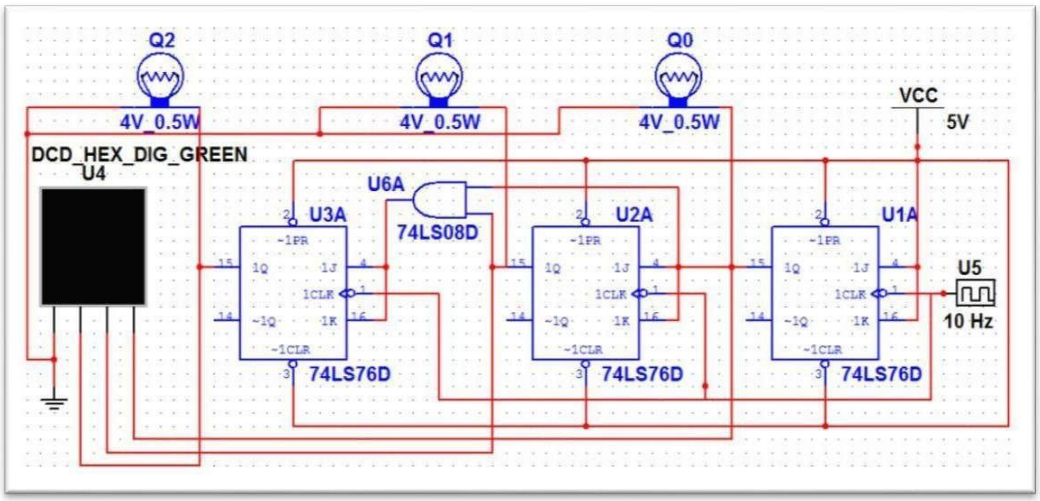

Fig 9.6: 3 bit Synchronous Counter

Apparatus:

SL	Apparatus	Picture	Quantity	Remarks
1.	Digital trainer board.		1	Good condition
2.	Integrated Circuits (ICs) And Gate(7408)		1	Was not in good condition. Had to change it.
3.	Power Supply		1	Good condition
4.	Connecting wires		multiple	Good condition
5.	IC 74LS76 (JK Flip Flop)		4	Good condition
6.	LED Display		1	Good condition

Precautions:

• Before circuit preparation, all ICs (74LS76 & 7408) was checked to ensure their proper functioning.
• The connection of preset and clear pins to Vcc was ensured.
• Efforts were made to minimize the use of wires and ensure the absence of loose connections.
• An LED display is utilized for proper biasing.
• The trainer board's analog signal generator was used for Clock pulse generation, with lower frequencies being used to facilitate slow changes, enabling the observation of outputs and the taking of readings.

Experimental Procedure:

Part 1: 3 bit Asynchronous Counter

1. Designed the circuit on the bread board as shown in Figure 9.5.
2. Used the trainer board's signal generator for the clock pulse and power supply forbiasing the Flip Flops.
3. The output can also be viewed in oscilloscope, just connect the outputs to the different channels of the oscilloscope.
4. Observed the output results, recorded them and also took pictures for labreport.

3 bit Synchronous Counter

1. Designed the circuit on the bread board as shown in Figure 9.6.
2. Used the trainer board's signal generator for the clock pulse and power supply forbiasing the Flip Flops.
3. The output viewed in oscilloscope, just connected the outputs to the differentchannels of the oscilloscope.
4. Observed the output results and too pictures lab report.

Hardware Setup:

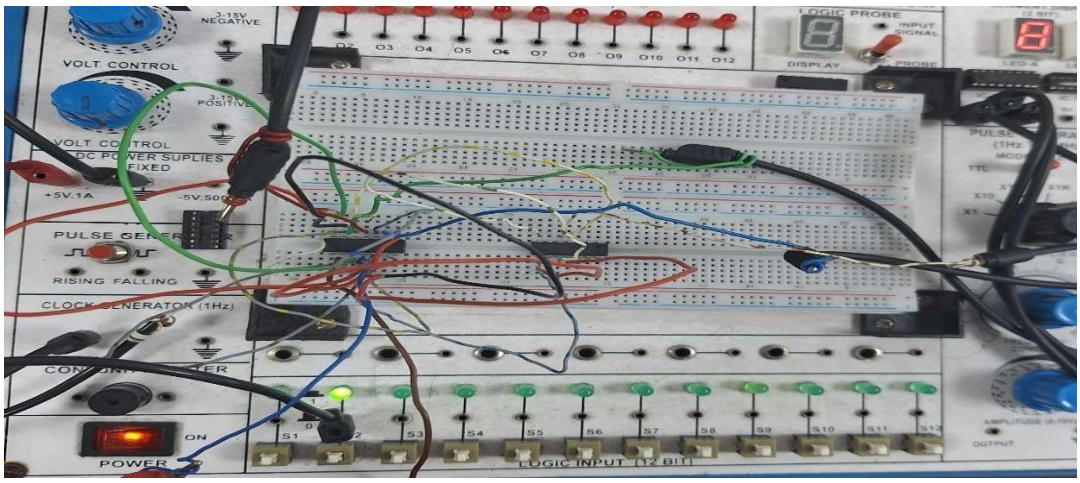

Fig 10: 3-bit Asynchronous Counter

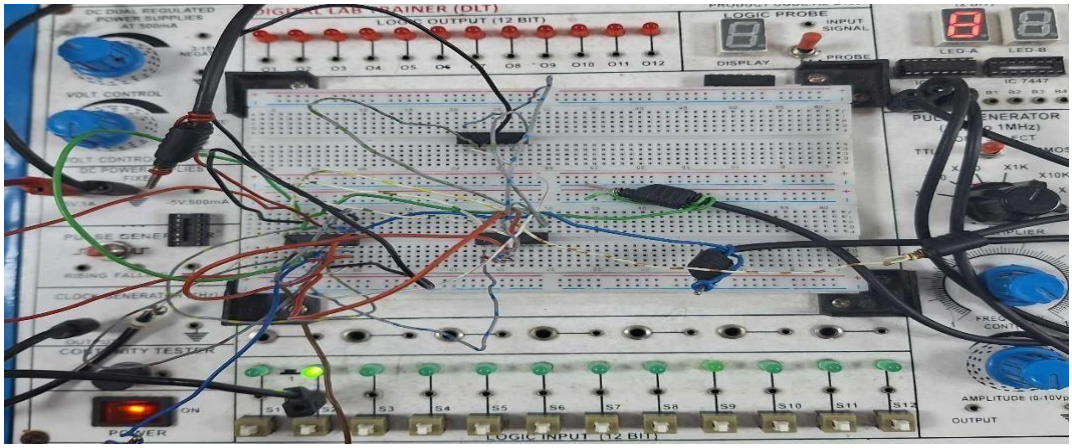

Fig 11: 3-bit Synchronous Counter

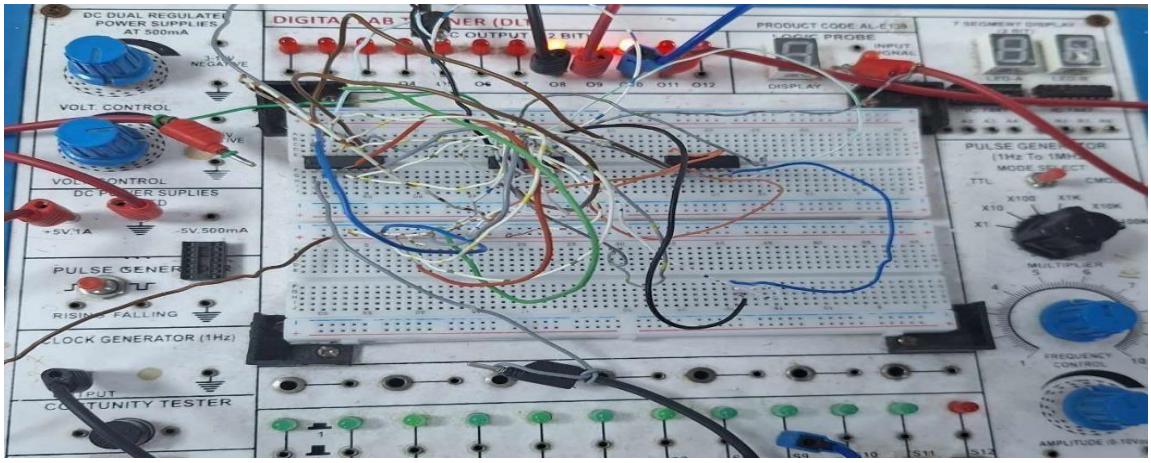

Fig 12: 4 bit Synchronous Counter

Simulation and Measurement:

Red: Clock, Yellow: Q0(X1), Green: Q1(X2), Blue: Q2(X3)

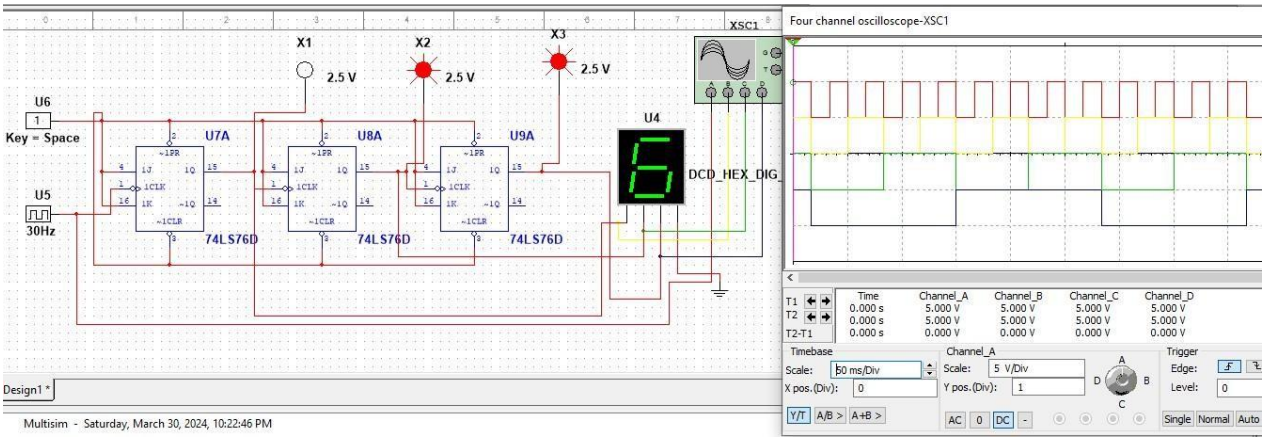

Fig 13: 3-bit Asynchronous Counter

Red: Clock, Yellow: Q0(X1), Green: Q1(X2), Blue: Q2(X3)

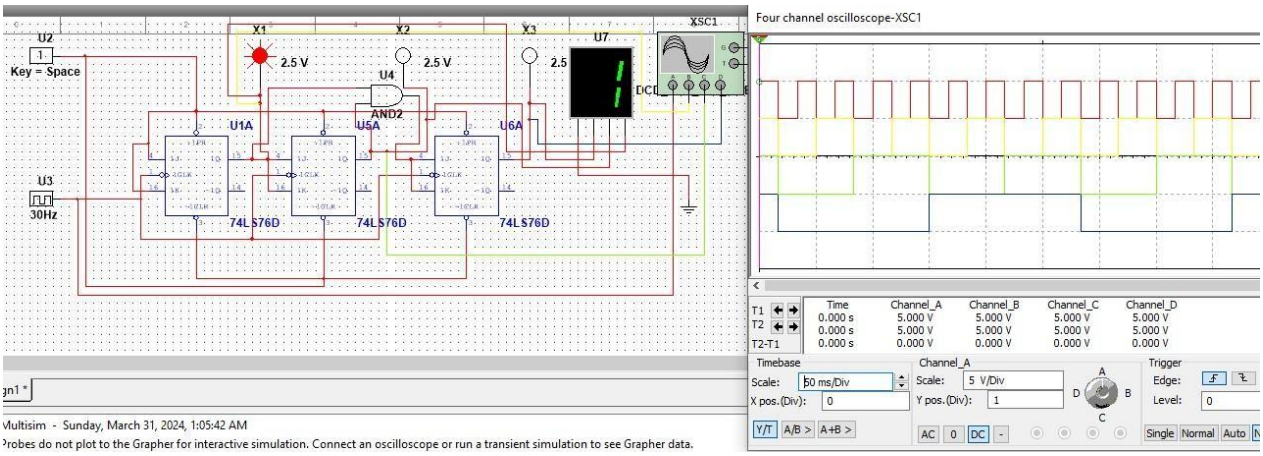

Fig 14: 3-bit Synchronous Counter

Questions with answers:

1. Design of a 4-bit Asynchronous Up- Counter.

Red: Q0(X1), Green: Q1(X2), Yellow: Q2(X3), Blue: Q3(X4)

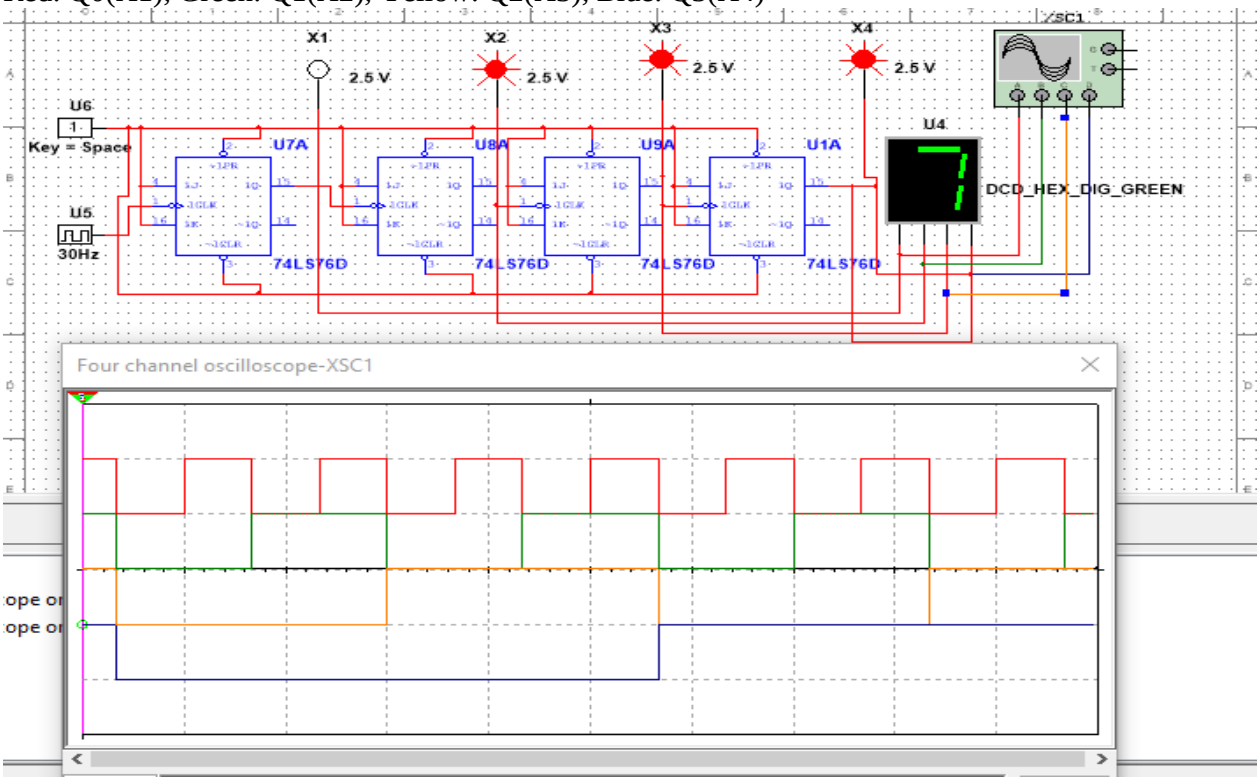

Fig 15: 4-bit Asynchronous Counter

2. Design of a 4 bit Synchronous Up- Counter.

Red: Q0(X1), Green: Q1(X2), Blue: Q2(X3), Yellow: Q3(X4)

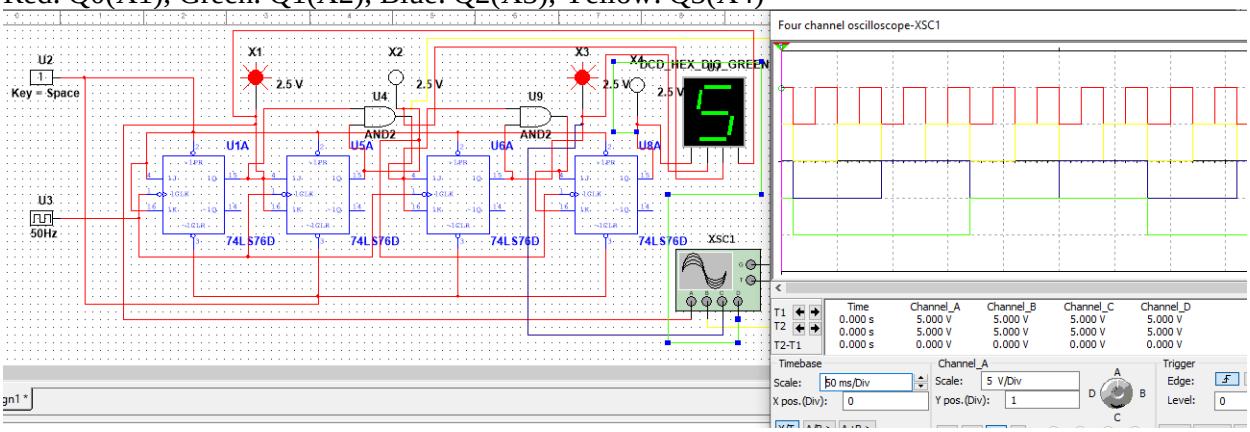

Fig 16: 4-bit Synchronous Counter

Bonus Mark:

1. Design a 3 bit Asynchronous down counter.

Red: Clock, Yellow: Q0(X1), Green: Q1(X2), Blue: Q2(X3)

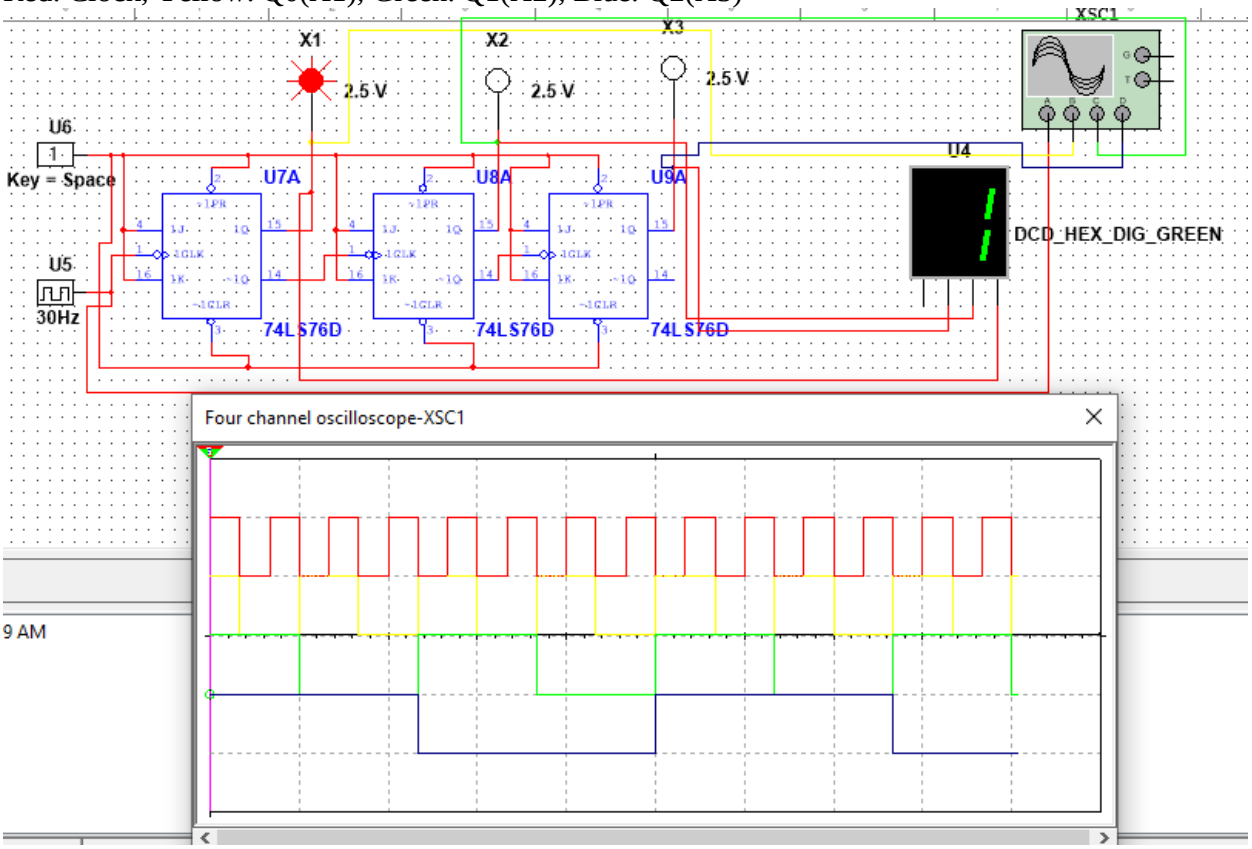

Fig 17: 3-bit Asynchronous Down Counter

2. Design of a Mod 10 Synchronous up counter.

Red: Q0(X1), Yellow: Q1(X2), Green: Q2(X3), Blue: Q3(X4)

Fig 18: 10 MOD Synchronous Counter(1-5)

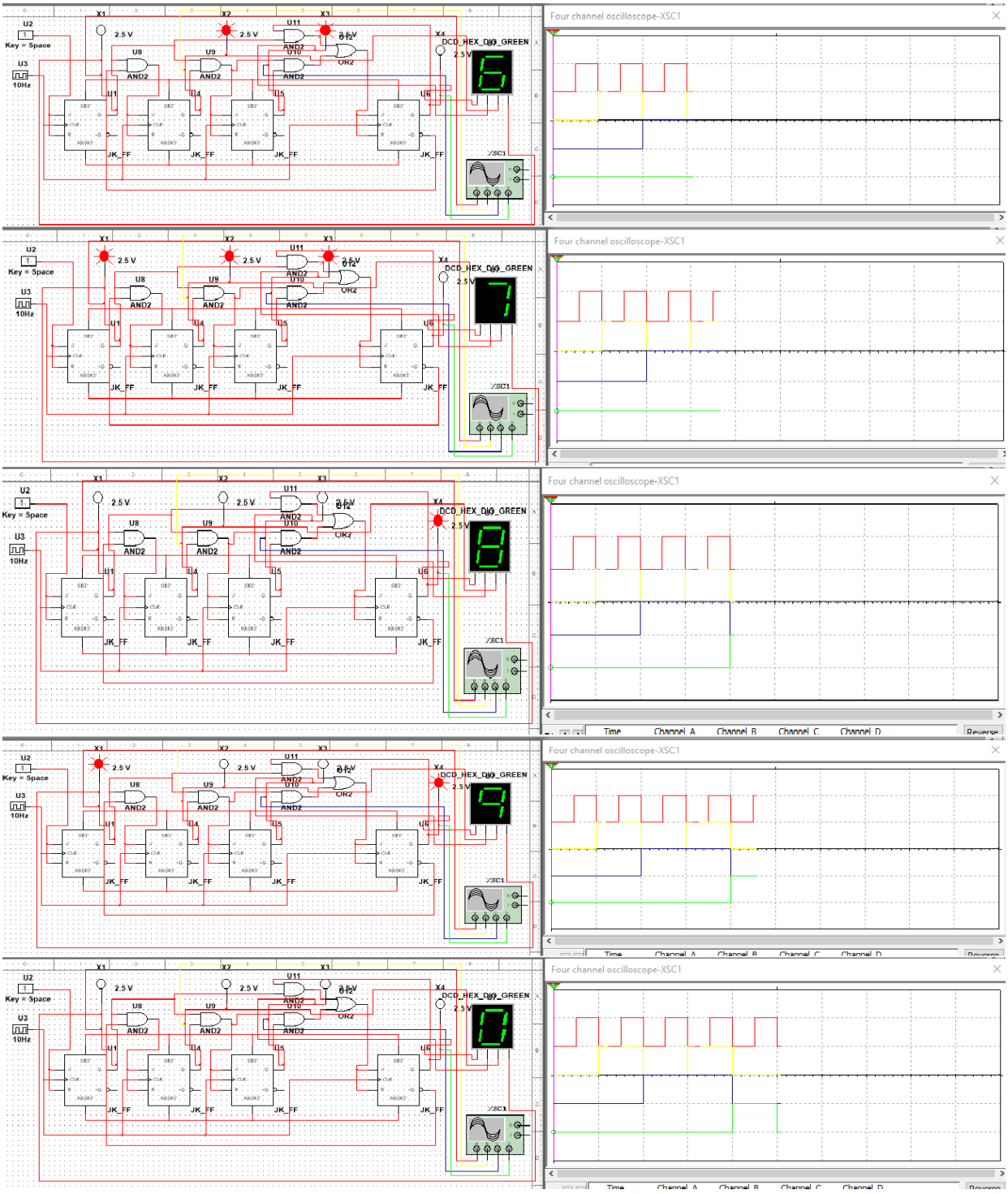

Fig 19: 10 MOD Synchronous Counter(6-0)

Discussion

The experiment aimed to compare asynchronous and synchronous counters using JK flip-flops. Setting up the 4-bit asynchronous counter proved challenging, highlighting its complexity. In contrast, synchronous counters were successfully demonstrated, showing simultaneous flip-flop activation and superior performance. Discrepancies in outputs were noted, possibly due to component tolerances and wiring errors. The simulations were conducted using Multisim NI Version 14.

Conclusion

In conclusion, the experiment illuminated the operational disparities between asynchronous and synchronous counters. Despite encountering difficulties with the 4-bit asynchronous counter setup, participants gained valuable insights into the challenges associated with its sequential operation. Successful setup of synchronous counters underscored their advantages, highlighting the significance of meticulous setup procedures and precise measurement techniques. Further refinement may be required for asynchronous counters, but overall, the experiment served as a valuable learning experience in digital circuit design with JK flip-flops.

References:

[1] www.tutorialspoint.com
[2] www.electronics-tutorials.ws
[3] faculty.kfupm.edu.sa
[4] "Digital Fundamentals" by Thomas L. Floyd
[5] American International University–Bangladesh (AIUB) Digital Logic And Circuits Lab Manual.