AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH

Faculty of Engineering

Laboratory Report Cover Sheet

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Laboratory Title: Construction Logic Gates using various MOS transistors

Experiment Number:_____ Due Date: 21-04-24 Semester: Spring 23-24

Subject Code:0067 Subject Name: **Digital Logic And Circuits Lab** Section: R

Course Instructor: Md. Ashiquzzaman Degree Program: CSE

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American International University- Bangladesh
Department of Faculty of Engineering
EEE 3102: Digital Logic & Circuits Laboratory

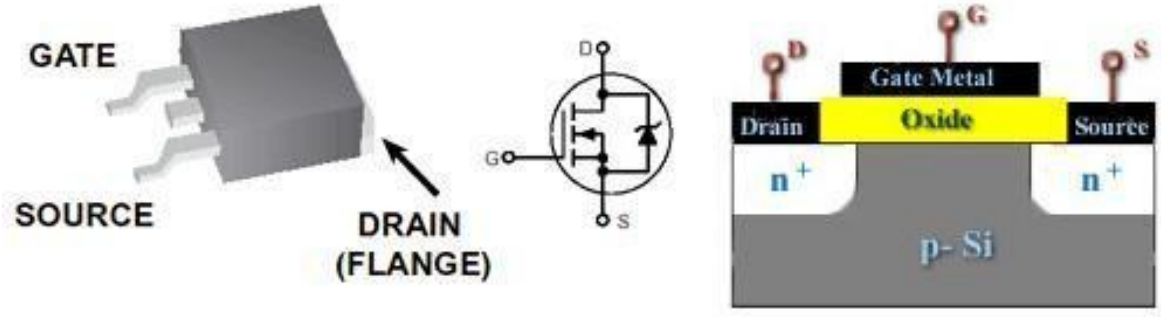
Title: Construction Logic Gates using various MOS transistors

Part I: Construction of MOSFET Logic Gates

Introduction:

MOSFET:
Pronounced MAWS-feht. Acronym for metal-oxide semiconductor field-effect transistor. These are used in many scenarios where you want to convert voltages. On your motherboard for example to generate CPU Voltage, Memory Voltage, AGP Voltage etc. Mosfets are usually used in pairs. If you see six mosfets around your CPU socket you have three-phase power.

Technical Info
MOSFETs come in four different types. They may be enhancement or depletion mode, and they may be n-channel or p-channel. For this application we are only interested in n-channel enhancement mode MOSFETs, and these will be the only ones talked about from now on. There are also logic-level MOSFETs and normal MOSFETs. The only difference between these is the voltage level required on the gate.



Unlike bipolar transistors that are basically current-driven devices, MOSFETs are voltage-controlled power devices. If no positive voltage is applied between gate and source the MOSFET is always non-conducting. If we apply a positive voltage UGS to the gate we'll set up an electrostatic field between it and the rest of the transistor. The positive gate voltage will push away the 'holes' inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source and drain electrodes. This produces a layer just under the gate's insulator through which electrons can get into and move along from source to drain. The positive gate voltage therefore 'creates' a channel in the top layer of material between oxide and p-Si. Increasing the value of the positive gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result we find that the size of the channel we've made increases with the size of the gate voltage and enhances or increases the amount of current which can go from source to drain- this is why this kind of transistor is called an enhancement mode device. Hence the operation of a p-channel MOSFET is just the opposite of an n-channel MOSFET.

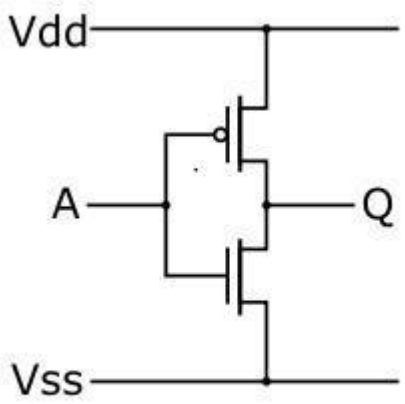
MOSFET testing

Get a multimeter with a diode test range. Connect the meter negative to the MOSFET's source. Hold the MOSFET by the case or the tab if you wish, it doesn't matter if you touch the metal body but be careful not to touch the leads until you need to. Do NOT allow a MOSFET to come in contact with your clothes, plastic or plastic products, etc. because of the high static voltages it can generate. First touch the meter positive on to the gate. Now move the positive meter probe to the drain. You should get a low reading. The MOSFET's gate capacitance has been charged up by the meter and the device is turned on. With the meter positive still connected to the drain, touch a finger between source and gate (and drain if you wish, it doesn't matter). The gate will be discharged through your finger and the meter reading should go high, indicating a non-conducting device.

MOS:

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963 (US patent 3,356,858).

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.



CMOS inverter

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

Some advantages of CMOS over TTL are:

- CMOS gate inputs draw far less current than TTL inputs, because MOSFETs are voltage- controlled, not current-controlled, devices.

- CMOS gates are able to operate on a much wider range of power supply voltages than TTL: typically 3 to 15 volts versus 4.75 to 5.25 volts for TTL
- CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors.

In this experiment, we will first look at some logic circuit designs using NMOS. Then we will implement the same logic circuits using CMOS and try to identify the potential design advantages of CMOS over NMOS.

Theory and Methodology:

NMOS Inverter with Ohmic/ Resistive Load:

Considering an ideal scenario, when a HIGH (+5V) is applied to the input, the NMOS transistor turns ON and current flows from Vdd to ground; thus output voltage, Vo= 0V.
Similarly, if a LOW (0V) is applied to the input, the NMOS remains in its OFF state. As a result, the current from Vdd has no path to ground. The output voltage is +5V

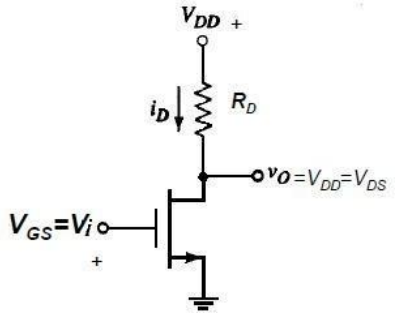


Fig.1: NMOS Inverter with Ohmic/Resistive Load

NMOS Inverter with NMOS Enhancement Transistor load:

One disadvantage of designing NMOS logic circuits with ohmic load is that even when the NMOS is OFF, there is static power dissipation due to the resistor. A better design is to use an enhancement-type NMOS as load. They are "*normally-off"* devices and it takes an applied voltage between gate and drain of the correct polarity to bias them *on*. Thus static power consumption is avoided

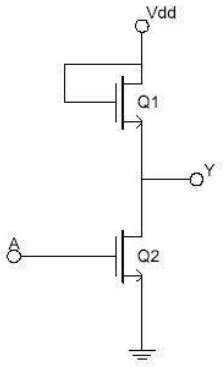


Fig.2 NMOS Inverter with NMOS Load

NMOS NAND Gate:

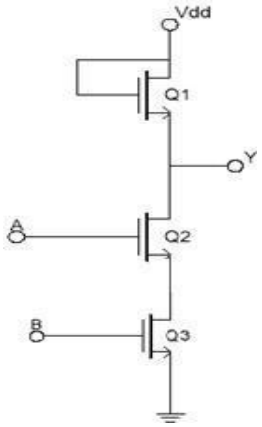


Fig.3 NMOS NAND Gate

NMOS NOR Gate:

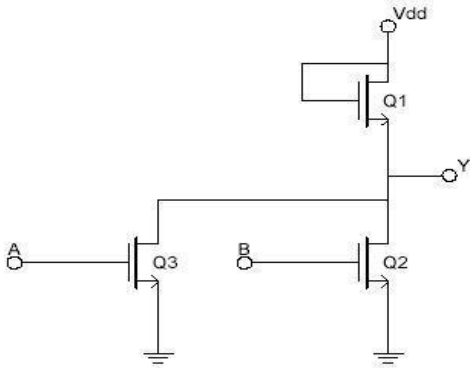


Fig.4 NMOS NOR Gate

MOS Logic:

CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications.

CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When OFF, their resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

CMOS Inverter:

When the input is grounded (logic 0), the N-channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground. At the same time, the P-channel MOSFET is forward biased, so it has a channel enhanced within itself. This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the output up to +V (logic 1).
When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

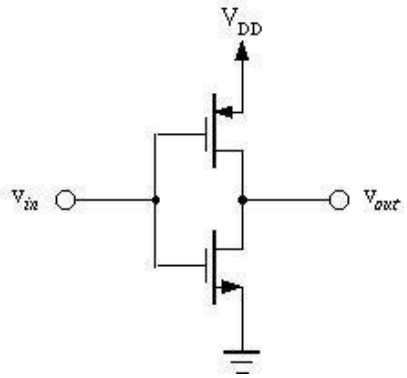


Fig.5 CMOS Inverter

CMOS NAND Gate:

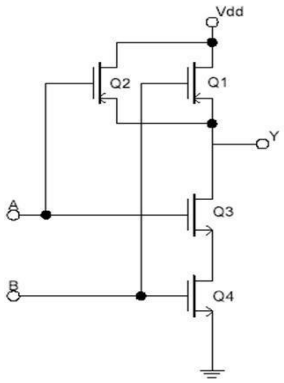


Fig.6 CMOS NAND Gate

CMOS NOR Gate:

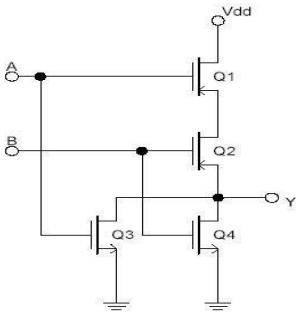
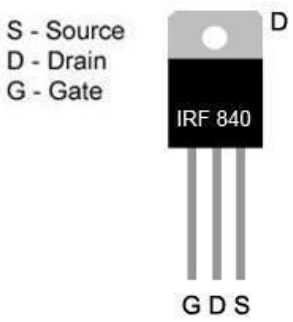


Fig.7 CMOS NOR Gate

MOSFET pin configuration:



Apparatus:

SL	Apparatus	Picture	Quantity	Remarks
1.	Digital trainer board.		1	Was not in good condition.
2.	Cmos - Pmos Nmos		2 2	Good condition
3.	Connecting wires		Multiple	Good condition

Precautions:

Checked all connections after you are done setting up the circuit and made sure that applied only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

1. Set upped the circuit to build NAND gate using Cmos

2. For each input combination, fond the output and place them in a Truth Table. The Truth Table should have two sets of outputs- one ideal and one experimental.
3. Repeated steps 1 and 2 for each circuit set-up for Fig.1

Hardware Implementation

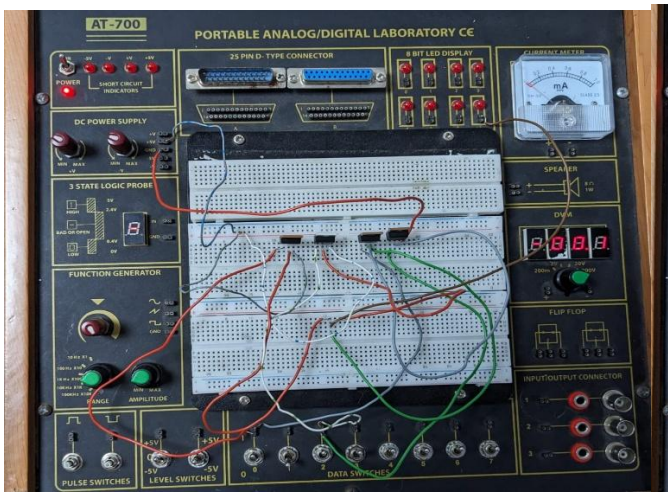


Fig.1: NAND gate using Cmos

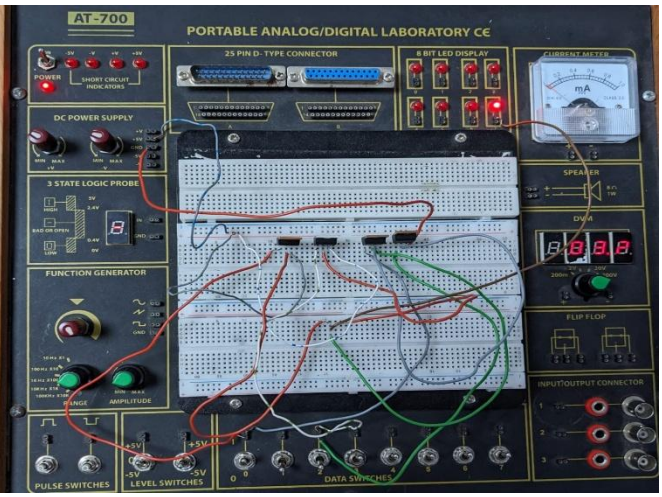


Fig.2: NAND gate using Cmos.

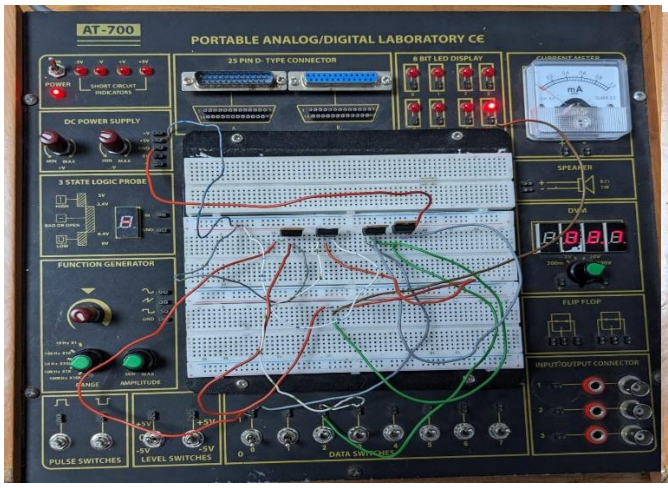


Fig.3: NAND gate using Cmos.

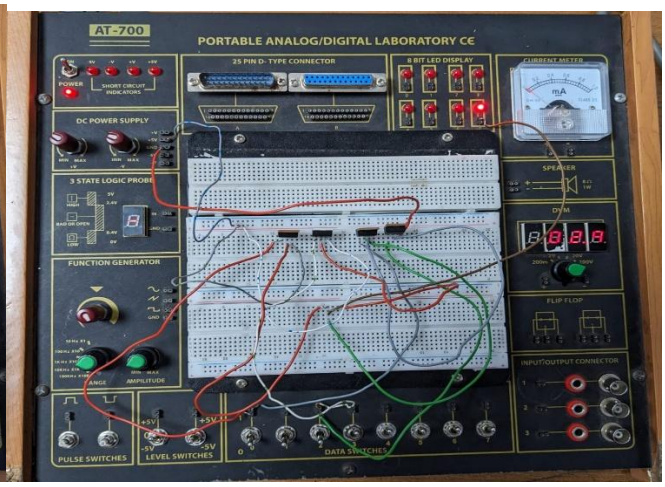


Fig.4: NAND gate using Cmos.

Simulation:

NMOS inverter with NMOS load:

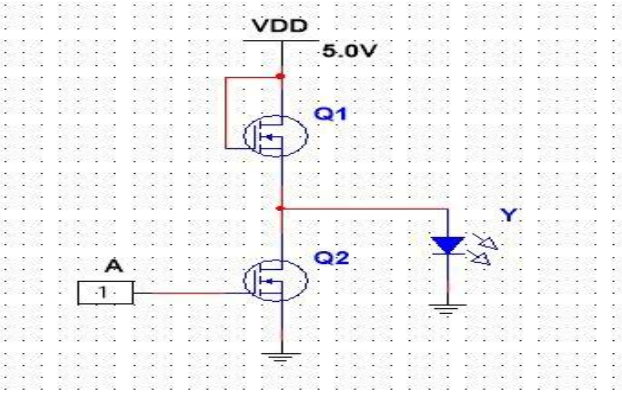


Fig.5: NMOS inverter

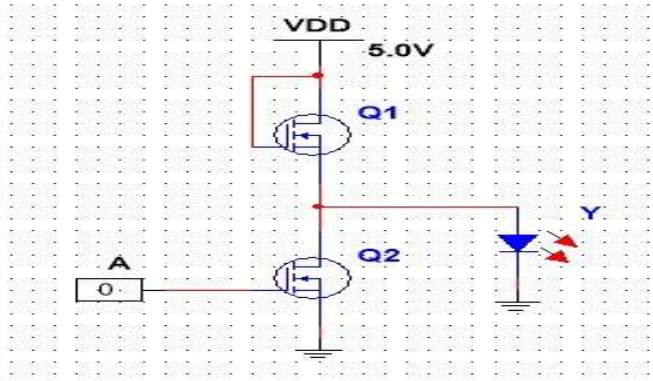


Fig.6: NMOS inverter

NMOS NOR gate:

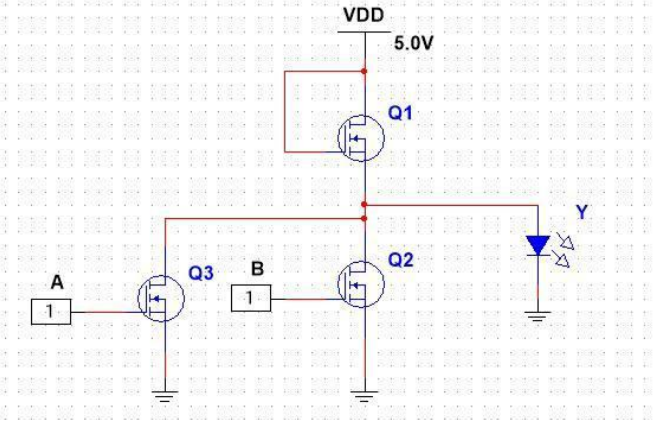


Fig.7: NMOS NOR gate

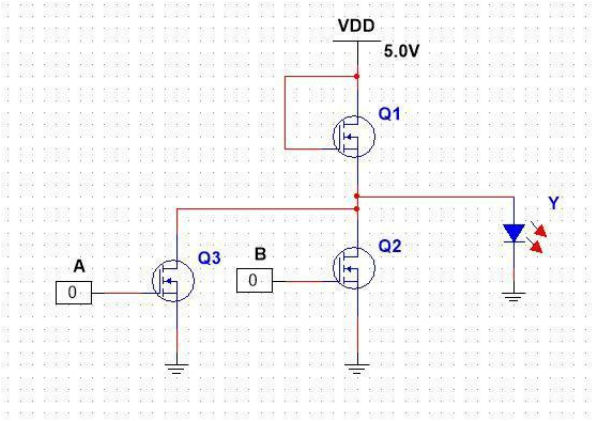


Fig.8: NMOS NOR gate

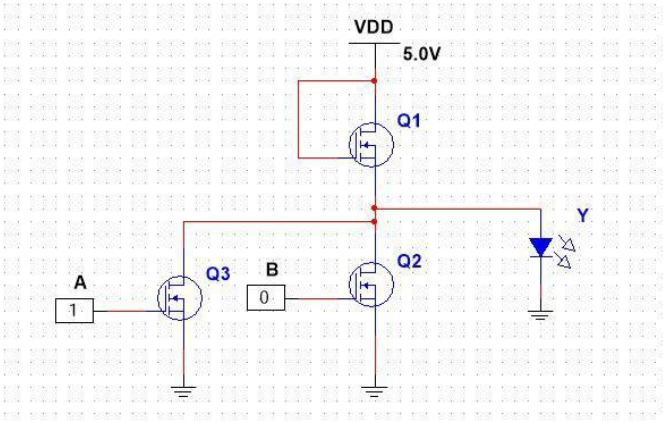


Fig.9: NMOS NOR gate

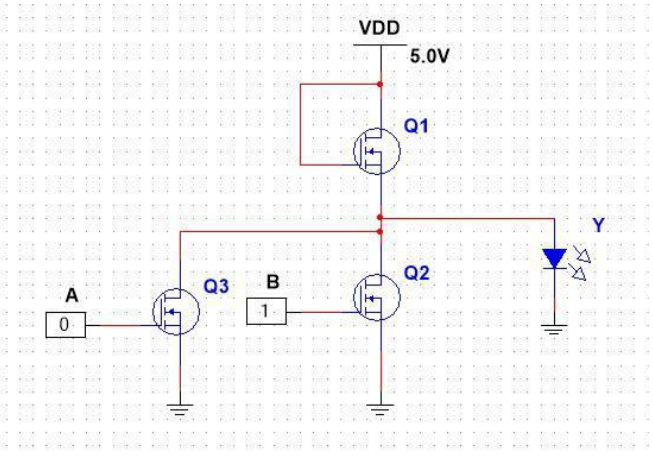


Fig.10: NMOS NOR gate

CMOS NAND gate:

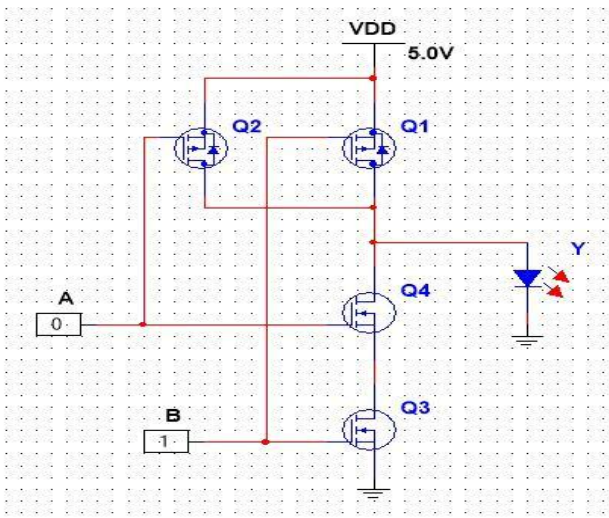


Fig.11: CMOS NAND gate

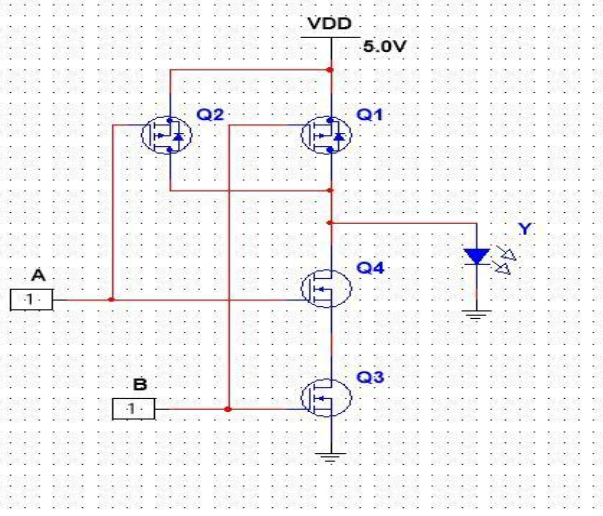


Fig.12: CMOS NAND gate

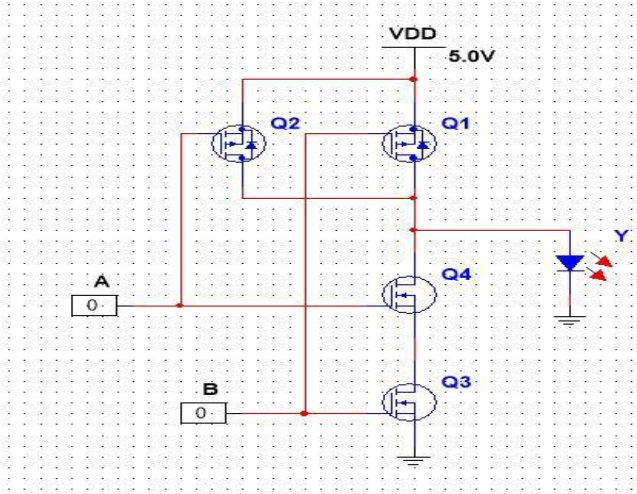


Fig.13: CMOS NAND gate

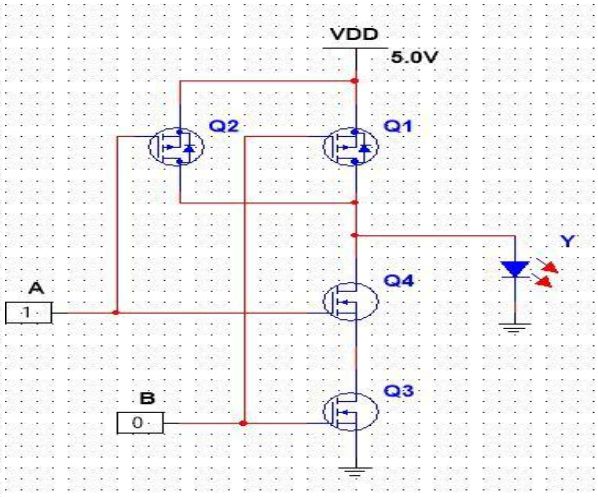


Fig.14: CMOS NAND gate

CMOS NOR gate:

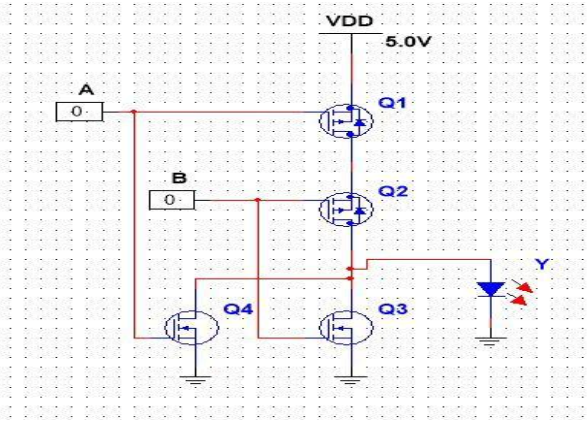


Fig.15: CMOS NOR gate

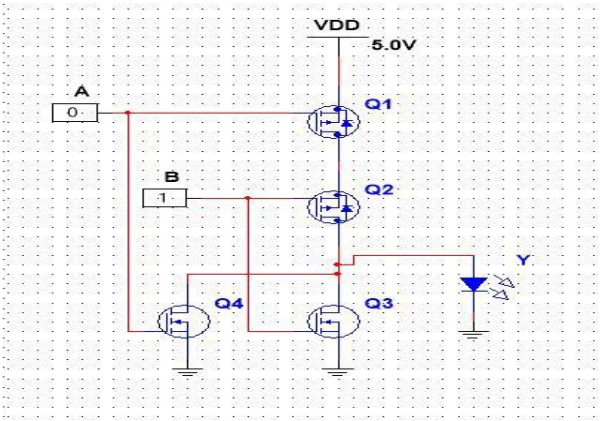


Fig.16: CMOS NOR gate

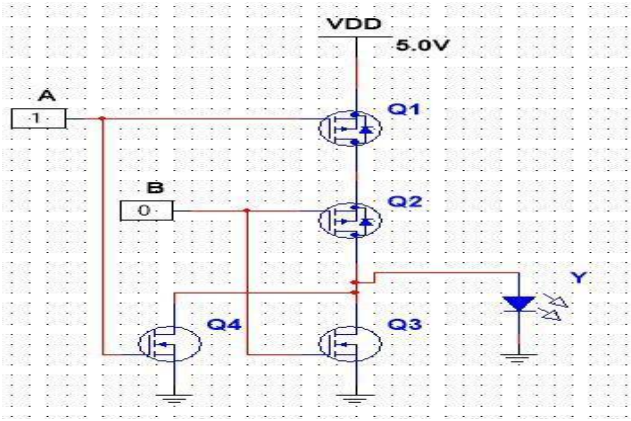


Fig.17: CMOS NOR gate

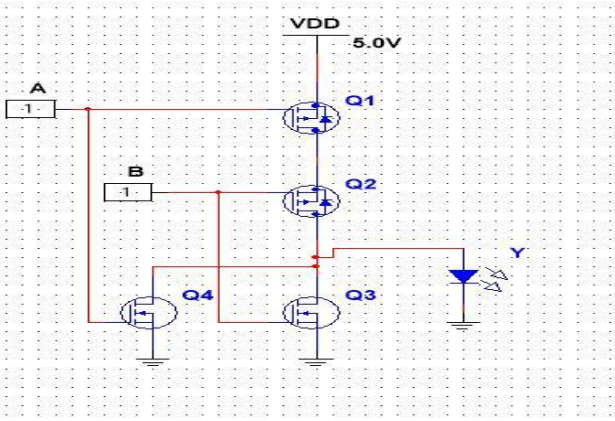


Fig.18: CMOS NOR gate

NMOS NAND gate:

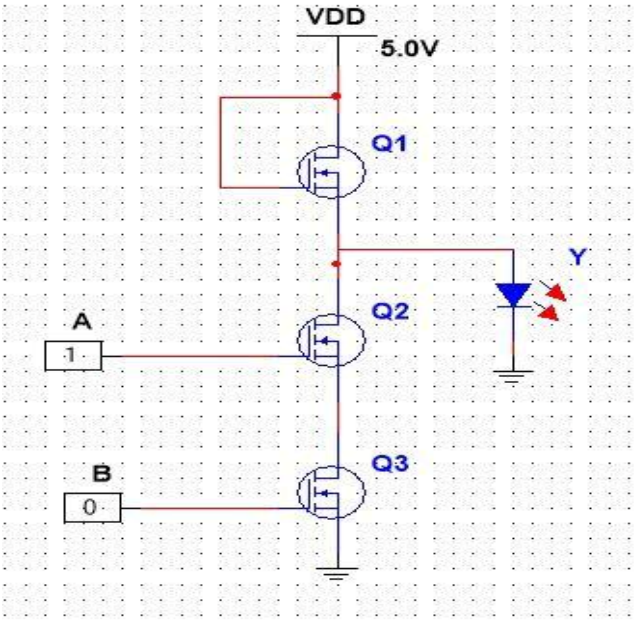


Fig.19: NMOS NAND gate

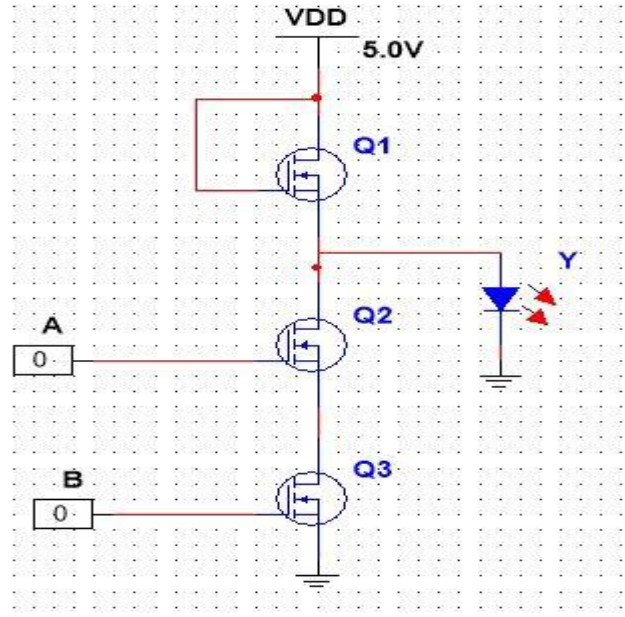


Fig.20: NMOS NAND gate

CMOS Inverter:

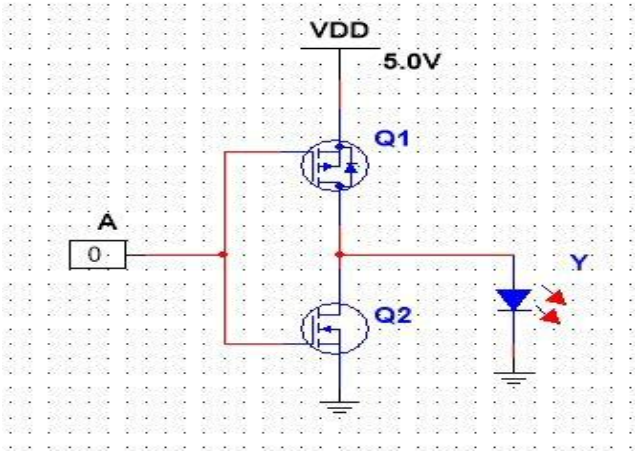


Fig.21: CMOS Inverter:

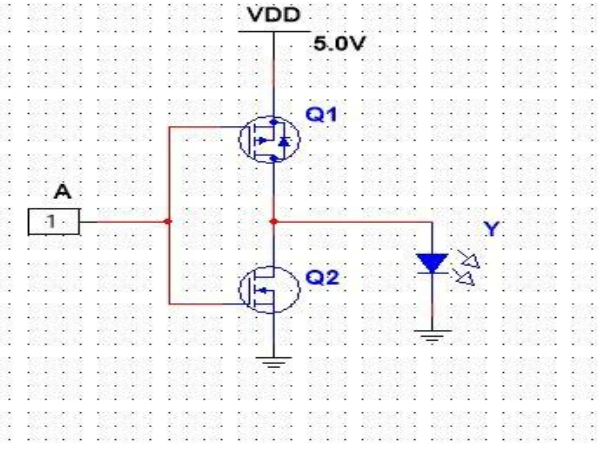


Fig.22: CMOS Inverter:

Report

Half Adder Sum:

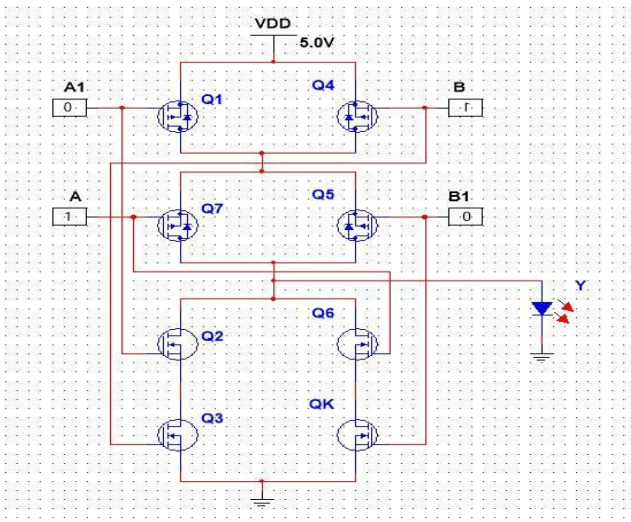


Fig.21: CMOS Inverter:

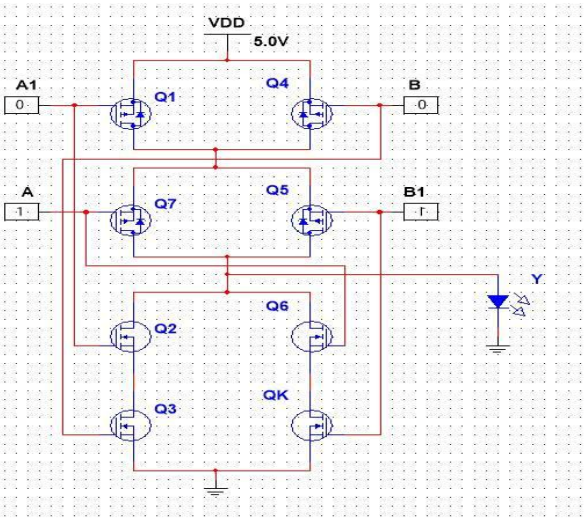


Fig.22: CMOS Inverter:

Half Adder Carry:

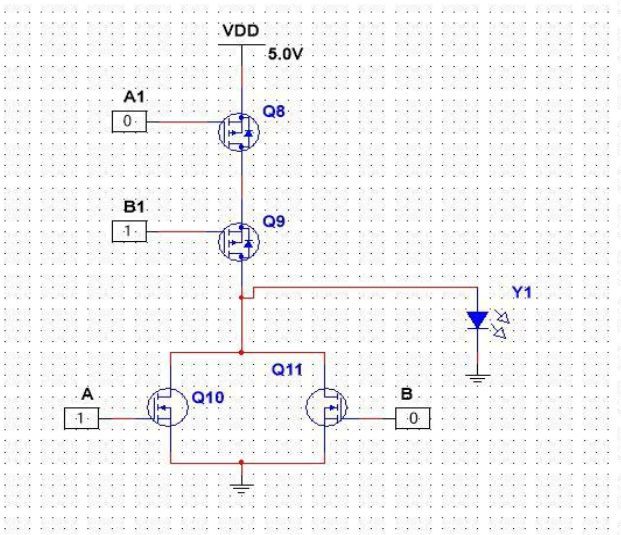


Fig.22: Full Adder Carry using

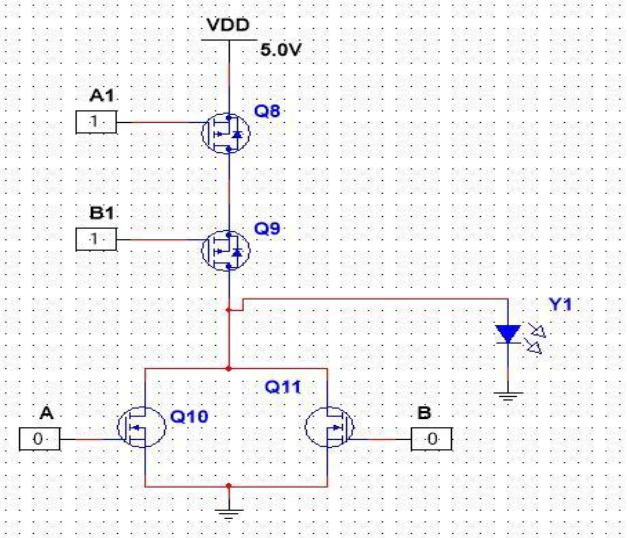


Fig.23: Full Adder Carry using CMOS

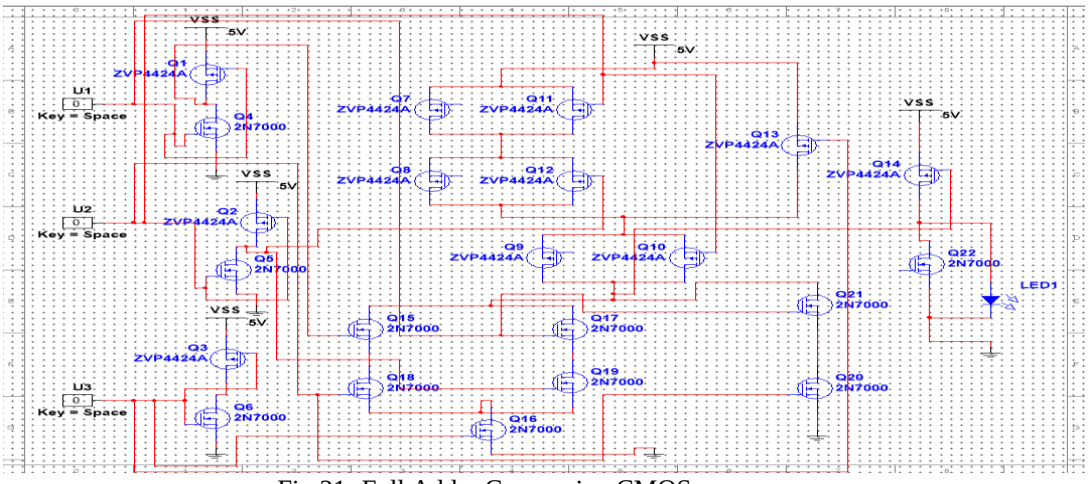


Fig.21: Full Adder Carry using CMOS

Discussion:

In the construction of logic gates using various MOS transistors, the process was swift and error-free. By meticulously designing circuits with NMOS and PMOS transistors, logic gates like NAND, NOR, and XOR were accurately assembled. Rigorous testing, including applying input signals and observing output signals, confirmed the correct operation of these gates. This practical exercise not only deepened understanding of MOS transistor behavior and digital logic design but also provided valuable insight into circuit construction. The simulations were conducted using Multisim NI Version 14.

Conclusion:

In summary, the experiment successfully demonstrated the construction of logic gates using MOS transistors. Through careful design and assembly, including NMOS and PMOS transistors, gates like NAND, NOR, and XOR were accurately implemented. Rigorous testing confirmed their functionality, enhancing understanding of MOS transistor behavior and digital logic design principles. Simulation in Multisim 14 further validated circuit operation, providing a comprehensive learning experience for students in electronics and computer engineering.

Reference:

1. www.electronics-tutorials.ws
2. faculty.kfupm.edu.sa
3. “Digital Fundamentals” by Thomas L. Floyd
4. American International University–Bangladesh (AIUB) Digital Logic And Circuits Lab Manual.