2.2 Functional overview

External memor CLK, NE [3:0], A[23:0], CCM data RAM 64 KB controller (FSMC) NJTRST, JTDI. D[31:0], OEN, WEN, JTCK/SWCLK JTDO/SWD, JTDO JTAG & SW MPU SRAM, PSRAM, NOR Flash, NBL[3:0], NL, NREG, NWAIT/IORDY, CD PC Card (ATA), NAND Flash ETM TRACEC NIORD, IOWR, INT[2:3] D-BUS INTN, NIIS16 as AF TRACED[3:0] Arm Cortex-M4 168 MHz FPU Flash S-BUS up to RNG MII or RMII as AF MDIO as AF Ethernet MAC DMA 1 MB . HSYNC, VSYNC 10/100 FIFC Camera SRAM 112 KB PUIXCLK, D[13:0] USB SRAM 16 KB ULPI:CK, D[7:0], DIR, STP, NXT ID, VBUS, SOF OTG HS FIFC USB PΗΥ OTG FS DMA2 8 Streams FIFC ID, VBUS, SOF AHB2 168 MHz 8 Streams FIFO DMA1 VDD = 1.8 to 3.6 V Supply GPIO PORT A supervision POR/PDR BOR VDDA, VSSA GPIO PORT B PVD GPIO PORT D XTAL OSC GPIO PORT E **IWDG** clock control GPIO PORT F PWR VBAT = 1.65 to 3.6 V FCLK ♣ PG[15:0] GPIO PORT G PHI15:01 Z GPIO PORT H \Leftrightarrow S RTC AWU ckup regi PI[11:0] GPIO PORT I 4 KB BKPSRAM 4 cras... 4 channels, ETR as AF TIM2 TIM3 EXT IT. WKUP 140 AF TIM4 DMA1 Ξ TIM5 SDIO / MMC 江 2 channels as AF
16b 1 channel as AF
1 channel as AF
1 channel as AF
RX, TX as AF
CTS, RTS as AF
RX, TX as AF
CTS RTS as AF AHR/APR2 AHB/APB1 TIM12 4 compl. channels (TIM1_CH1[1:4]N, 4 channels (TIM1_CH1[1:4]ETR, BKIN as AF TIM1 / PWM 16b 😽 (; TIM13 4 compl. channels (TIM1_CH1[1:4]N, 4 channels (TIM1_CH1[1:4]ETR, BKIN as AF TIM14 (TIM8 / PWM 16b USART2 \Leftrightarrow 2 channels as AF TIM9 16b 😂 RX, TX as AF
CTS, RTS as AF
RX, TX as AF USART3 ₩ TIM10 16b 1 channel as AF UART4 ₩ WWDG 1 channel as AF TIM11 16b ₹ UART5 RX, TX as AF

MOSI/SD, MISO/SD_ext, SCK/CK
NSS/WS, MCK as AF

MOSI/SD, MISO/SD_ext, SCK/CK
NSS/WS, MCK as AF

SCI_SDA_SMBA as AF RX, TX, CK, CTS, RTS as AF ard USART1 ₩ ₩ SP2/I2S2 RX, TX, CK, CTS, RTS as AF USART6 ₩ TIM6 \Leftrightarrow SP3/I2S3 MOSI, MISO, SCK, NSS as AF SPI1 \bowtie TIM7 16b k∺y I2C1/SMBUS SCL, SDA, SMBA as AF X VDDREF_ADC \mathfrak{F} I2C2/SMBUS SCL, SDA, SMBA as AF Temperature sensor @V_{DDA} II. 8 analog inputs common to the 3 ADCs DAC1 \mathfrak{F} I2C3/SMBUS SCL, SDA, SMBA as AF ADC1 ITF \square 8 analog inputs common to the ADC1 & 2 DAC2 ADC2 IF K₩ bxCAN1 TX, RX ADC3 bxCAN2 DAC1_OUT as AF MS19920V4

Figure 5. STM32F40xxx block diagram

1. The camera interface and ethernet are available only on STM32F407xx devices.

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

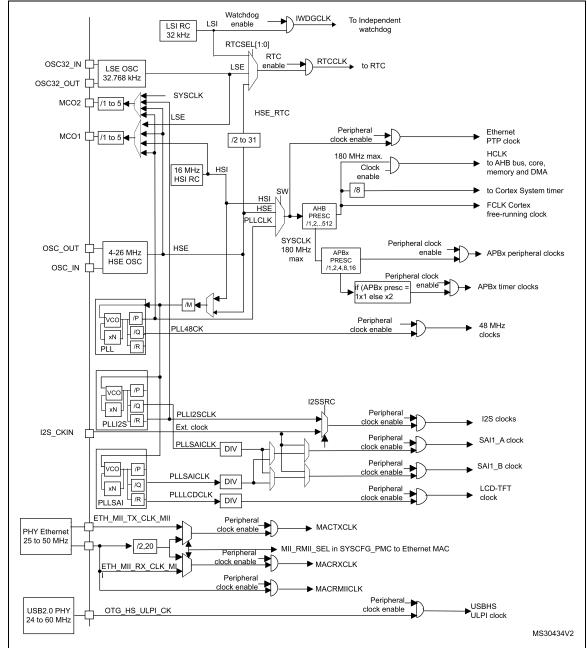


Figure 16. Clock tree

- For full details about the internal and external clock source characteristics, refer to the Electrical characteristics section in the device datasheet.
- When TIMPRE bit of the RCC_DCKCFGR register is reset, if APBx prescaler is 1, then TIMxCLK = PCLKx, otherwise TIMxCLK = 2x PCLKx.
- When TIMPRE bit in the RCC_DCKCFGR register is set, if APBx prescaler is 1,2 or 4, then TIMxCLK = HCLK, otherwise TIMxCLK = 4x PCLKx.

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5 Power controller (PWR)

This section applies to the whole STM32F4xx family, unless otherwise specified.

5.1 Power supplies

The device requires a 1.8 to 3.6 V operating voltage supply (V_{DD}). An embedded linear voltage regulator is used to supply the internal 1.2 V digital power.

The real-time clock (RTC), the RTC backup registers, and the backup SRAM (BKP SRAM) can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off.

Note:

Depending on the operating power supply range, some peripheral may be used with limited functionality and performance. For more details refer to section "General operating conditions" in STM32F4xx datasheets.

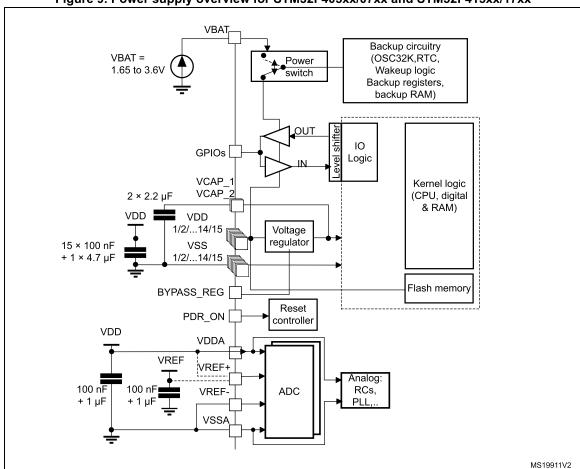


Figure 9. Power supply overview for STM32F405xx/07xx and STM32F415xx/17xx



^{1.} V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.