PCI Express M.2 Specification

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1

1. Introduction to M.2 Electro-Mechanical Specifications

The M.2M.2 form factor is used for Mobile Add-In cards. The M.2 is a natural transition from the Mini Card and Half-Mini Card to a smaller form factor in both size and volume. The M.2 is a family of form factors that will enable expansion, contraction, and higher integration of functions onto a single form factor module solution.

The key target for M.2 is to be significantly smaller in the XYZ and overall volume of the Half-Mini Card used today in mobile platforms in preparation for the very thin computing platforms (for example; Notebook, Tablet/Slate platforms) that require a much smaller solution.

The M.2 comes in two main formats:

- Connectorized
- Soldered-down

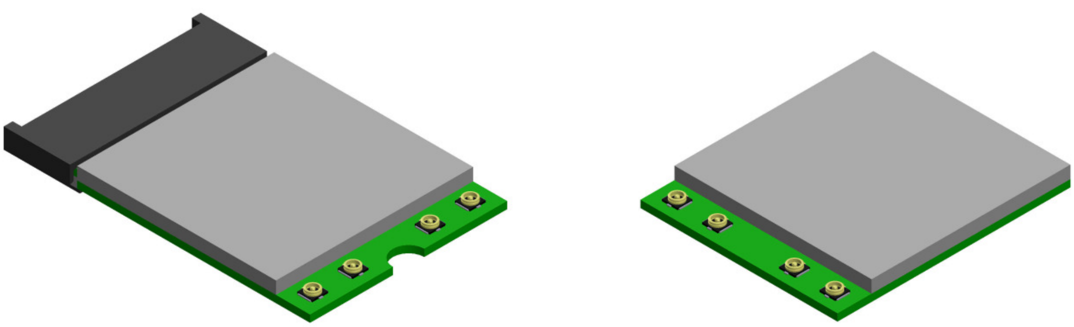


Figure 1. M.2 Concept Board/Modules

M.2 is targeted toward addressing system manufacturers' needs for build-to-order (BTO) and configure-to-order (CTO) rather than providing a general end-user-replaceable module. As such, the requirements provided in this document should be viewed in its entirety as an optional normative specification. It is expected that system manufacturers that build to and order modules to this specification are responsible for indicating to their module suppliers which aspects of the specification are normative, optional or explicitly not required for the products being ordered.

1.1. Targeted Application

The M.2 family of form factors is intended to support multiple function add-in cards/modules that include the following:

- WiFi
- Bluetooth
- Global Navigation Satellite Systems (GNSS)
- Near Field Communication (NFC)
- WiGig
- WWAN (2G, 3G and 4G)
- Solid-State Storage Devices
- Other & Future Solutions (e.g. Hybrid Digital Radio (HDR))

The M.2 Specification will cover multiple Host Interface solutions including:

- PCIe, PCIe LP
- HSIC
- SSIC
- USB
- SDIO
- UART
- PCM/ I2S
- I^2C
- SATA
- Display Port
- And future variants of the above

In light of the fact that the number of Host Interfaces has dramatically increased and in order to support the multitude of Comms and other solutions typically integrated into NB-based and very thin-based platforms, there is a need to clearly define several distinct sockets:

- A Connectivity Socket (typically WiFi, BT, NFC or WiGig) designated as Socket 1
- A WWAN/SSD/Other Socket that will support various WWAN+GNSS solutions, various SSD and SSD Cache configurations and potentially other yet undefined solutions designated as Socket 2
- SSD Drive Socket with SATA or up to 4 lanes of PCIe designated as Socket 3

Each of the three sockets is unique and incorporates a different collection of host interfaces to support the specific functionality of the modules. The modules are typically not interchangeable between sockets. Therefore, each Socket will have a unique mechanical key. However, there are cases where a dual mechanical key scheme will enable dual socket support. Details of the sockets will be described in the following sections of this document.

For the sake of coverage, the connectorized M.2 boards/modules will be defined as both single-sided for low profile solutions and dual-sided to enable more content to be integrated applicable in the platform. Several target Z-heights will be outlined as part of the specification. Actual configuration implementation will be determined between customer and vendor. A naming convention will enable an exact definition of all key parameters.

1.2. Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- PCI Express Mini Card Electromechanical Specification, Revision 2.0
- PCI Express Specification Revision 3.0
- SDIO3.0
- SSIC – SuperSpeed USB Inter-Chip Supplement to the USB 3.0 Specification
- HSIC
- DisplayPort Standard Specifications, version 1.2
- *Serial ATA* Revision 3.1
- *I^{2}C BUS Specifications*, Version 2.1, January 2000
- EIA-364 Electrical Connector/Socket Test Procedures including Environmental Classifications EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications

2

2. Mechanical Specification

2.1. Overview

This specification defines a family of M.2 modules and the corresponding system interconnects based on a 75 position edge card connection scheme or a derivation of the card edge and a soldered-down scheme for system interfaces.

The M.2 family comprised of several module sizes and designated by the following names (see Figure 2):

- Type 1216
- Type 2226
- Type 1630
- Type 2230
- Type 3026
- Type 3030
- Type 2242
- Type 3042
- Type 2260
- Type 2280
- Type 22110

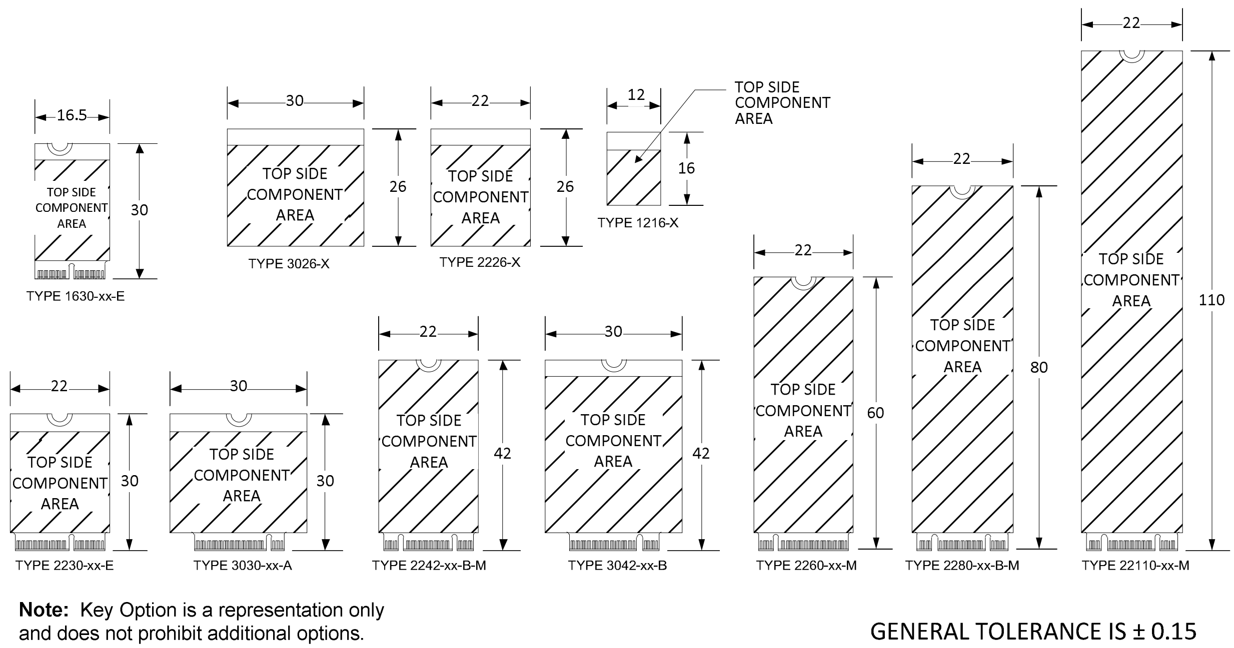


Figure 2. M.2 Family of Form Factors

The majority of M.2 types are connectorized using an edge connection scheme that can be either single-sided or dual-sided assembly. There will be several component Z-height options defined in this specification. The type of edge connector will cater to different platform Z-height requirements. In all cases, the board thickness is 0.8 mm ±10%. The type 1216, type 2226 and type 3026are unique as they are Soldered Down solutions that will have an LGA pattern on the back. Therefore, they can only be single sided and the board thickness does not need to adhere to the 0.8 mm ±10% requirement.

The edge connector requires a mechanical key for accurate alignment. The location of the mechanical key along the Gold Finger contacts will make each key unique per a given socket connector. This prevents wrongful insertion of an incompatible board which prevents a safety hazard.

The board type, the type of assembly, the component Z-heights on top and bottom, and the mechanical key will make up the M.2 board naming convention detailed in the next section.

2.2. Card Type Naming Convention

Because there are various types of M.2 solutions and configurations, a standard naming convention will be employed to define the main features of a specific solution.

The naming convention will identify: the following:

- The module size (width & length)
- The component assembly maximum Z-height for the top and bottom sides of the module
- The Mechanical Connector Key/Module key location/assignment or multiple locations/assignments

These naming conventions will clearly define the module functionality, what connector it coincides with, and what Z-heights are met. Figure 3 diagrams the naming convention.

The connectorized board width options are: 16.5 mm, the generic 22 mm, and the widest 30 mm board width.

The board length can scale to various lengths to support the content and expand as the content increases. The lengths supported are: 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

Together these two dimensions make up the first part of the module type definition portion of the module name.

The next part of the name describes whether the module is single-sided or dual-sided and a secondary definition of what are the maximum Z-heights of the components on the top and bottom side of the module. Here we have specific Z-height limits that are either 1.5 mm, 1.35 mm, or 1.2 mm on the top side and 1.5mm, 1.35 mm, 0.7 mm and 0 mm on the bottom side. The letter S will designate Single-sided and the letter D will designate Dual-sided. This will be complimented with a number that designates the specific Z-height combination option.

The last section of the name will designate the mechanical connector key/module key name and the coinciding pin location. These will be designated by a letter from A to M. In cases where the module will have a dual key scheme to enable insertion of the module into two different keyed sockets, a second letter will be added to designate the second mechanical connector key/module key.

Figure 4 on the following page shows an example of module Type 2242 – D2 – B – M.

Module Nomenclature
Sample type 2242-D2-B-M

Type XX XX - XX - X - X*

Width (mm)
12
16
22
30

Length (mm)
16
26
30
38
42
60
80
110

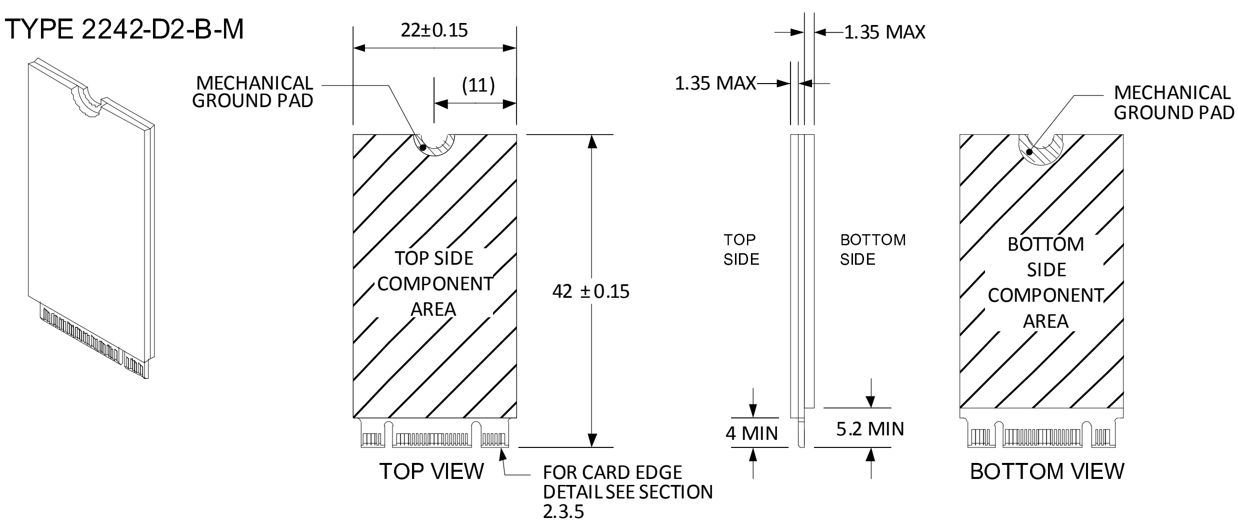
	Component Max Ht(mm)	
	T Max**	B Max**
S1	1.2	0^{τ}
S2	1.35	0^{τ}
S3	1.5	0^{τ}
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5

Key ID	Pin	Interface
A	8-15	PCIe x2 / USB / I2C / DP x4
B	12-19	PCIe x2 / SATA / USB / PCM / IUM / SSIC / UART-I2C
C	16-23	Reserved for Future Use
D	20-27	Reserved for Future Use
E	24-31	PCIe / USB / I2C-ME / SDIO / UART / PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)^
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	PCIe x4 / SATA

* Use ONLY when a double slot is being specified
** Label included in height dimension
^ Key G is designed for Non-M.2 compliant devices. Intended for custom use. Use at your own risk!
τ Insulating label allowed on connector-based designs

Figure 3. M.2 Naming Nomenclature

> **Note:** Key ID assignment must be approved by the PCI-SIG. Unauthorized use of Key IDs would render this use as non-compliant to M.2 specification.



The board is 22 x 42 mm, Double Sided with a maximum Z-height of 1.35 mm on both the Top and Bottom, and it has two mechanical Connector Keys/Module keys at locations B and M which will enable it to plug into two types of connectors (Key B or Key M).

Figure 4. Example of Type 2242-D2-B-M Nomenclature

Table 1 shows the various options for board configurations as a function of the Socket, Module Function and Module size.

Table 1. Preferred and Optional Module Configurations

	Soldered-down			Connectorized			
	Type	Preferred	Pinout Key	Connector Key	Type	Module Height Options	Module Key
Socket 1 Connectivity	1216	S1	E				
				A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S3	E	A, E	2230	S1, D1, S3, D3, D4	A, E, A+E
	3026	S3	A	A, E	3030	S1, D1, S3, D3, D4	A, E, A+E
Socket 2 WWAN/Other				B	3042	S1, D1, S3, D3, D4	B
Socket 2 SSD/Other				B	2230	S2, D2, S3, D3, D5	B+M
				B	2242	S2, D2, S3, D3, D5	B+M
				B	2260	S2, D2, S3, D3, D5	B+M
				B	2280	S2, D2, S3, D3, D5	B+M
				B	22110	S2, D2, S3, D3, D5	B+M
Socket 3 SSD Drive				M	2242	S2, D2, S3, D3, D5	M, B+M
				M	2260	S2, D2, S3, D3, D5	M, B+M
				M	2280	S2, D2, S3, D3, D5	M, B+M
				M	22110	S2, D2, S3, D3, D5	M, B+M

Type 1216, Type 2226 and Type 3026are unique as they are Soldered-Down solutions while all the others are connectorized with a PCB Gold Finger layout that coincides with an Edge Card connector. The Soldered-Down solutions do not have mechanical keys and their pin-out configuration needs to be specifically called out.

2.3. Card Specifications

There are multiple defined card outlines. Card thickness is fixed at 0.8 mm ±10% with optional increased/decreased XY dimensions so as to incorporate more or less functionality on the board.

For purposes of the drawings in this specification, the following notes apply:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ± 0.15 mm, unless otherwise specified.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- The board/module has a 4mm strip at the lower end of the board intended to support the Gold Finger pads used in conjunction with an Edge Card connector. The Gold Fingers appear on both top and bottom side of the board/module PCB
- In some configuration, the board/module has a 3.8 mm strip intended to support RF connectors.
- All connectorized versions have a mounting/retention screw (half-moon cutout) at the upper end of the board/module used to hold down the board onto the MB or chassis
- The remainder of the board area available is intended for Active Components but not limited to this. Encroachment into this area can be done if extra area is needed for additional RF antenna connectors
- The diagrams showing mechanical connector key/module key locations in this document are for example only. Actual Key location/definition is part of the actual module name per the naming convention
- General Tolerance Summary as given in Table 2

Table 2. General Tolerance

	+ Plus	– Minus
PCB Size Tolerance	0.15 mm	0.15 mm
PCB Thickness	10% mm	10% mm
Bevel Capabilities	0.25 mm	0.25 mm
Drill Capabilities for Module key	0.05 mm	0.05 mm

2.3.1. Card Form Factors Intended for Connectivity Socket 1

2.3.1.1. Type 2230 Specification

The Generic M.2 board/module size used for the majority of the Connectivity solutions such as WiFi+BT type solutions is Type 2230. However, this board size can also accommodate other Multi-Comm and Combo solutions as well.

The Type 2230 board/module is intended to support the multiple WiFi configurations such as 1x1, 2x2, and 3x3. An example of the Type 2230 board/module mechanical outline drawing is shown in Figure 3 and Figure 4.

The Type 2230 board/module uses a 75 position host interface connector and has room to support up to four (4) RF connectors in the upper section. The recommended location and assignment of the four RF connectors is described in section 2.3.7, *RF Connectors*. RF connectors can be placed in other locations on the Type 2230 board/module. In cases where additional RF connectors are needed, they can be added in the active component area and should maintain a minimal distance of 4.5 mm center-to-center to enable manufacturing test interface of the RF connection.

The diagrams in Figures 5 and 6 are an example of specific board type(s).

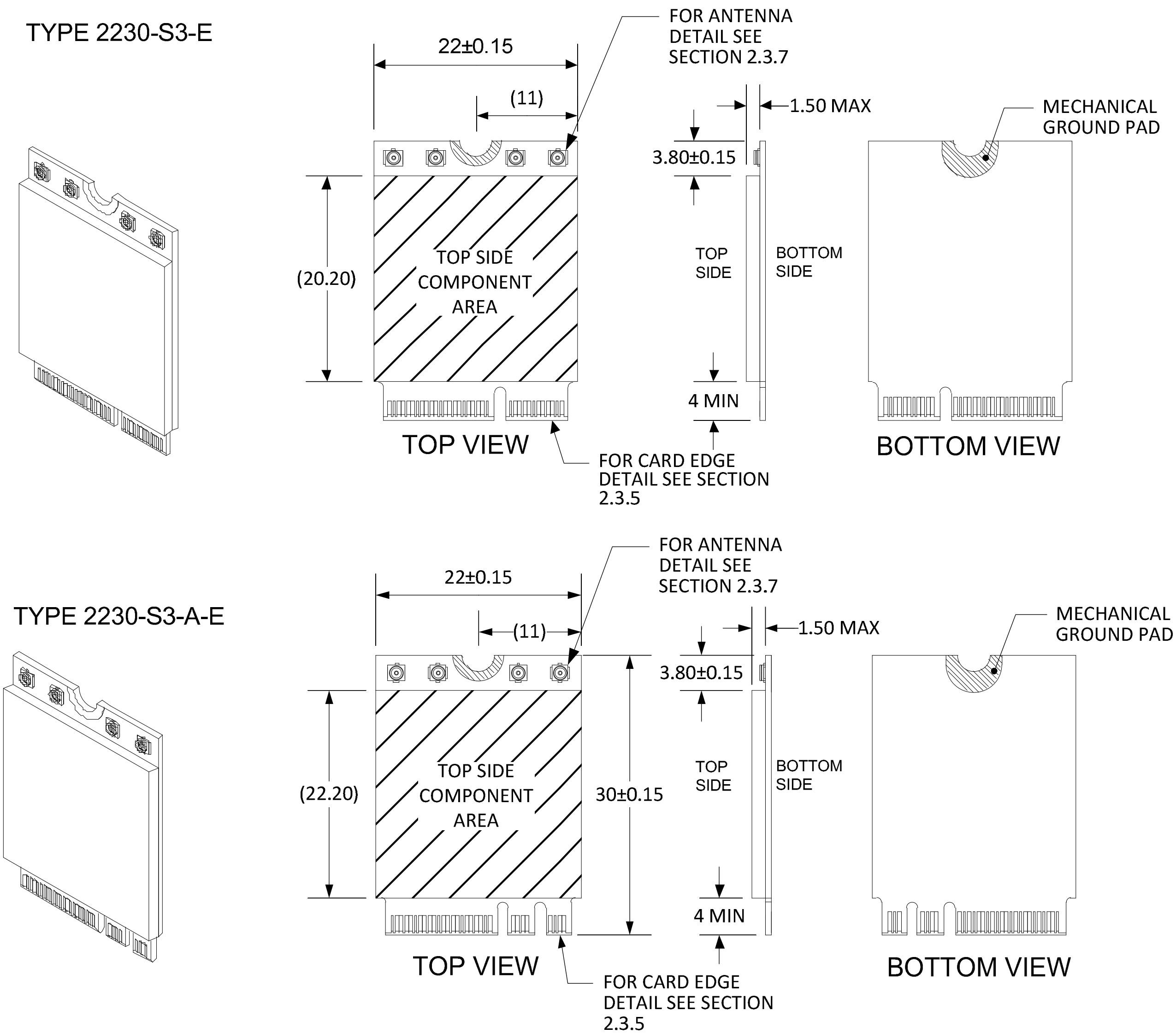


Figure 5. M.2 Type 2230-S3 Mechanical Outline Drawing Examples

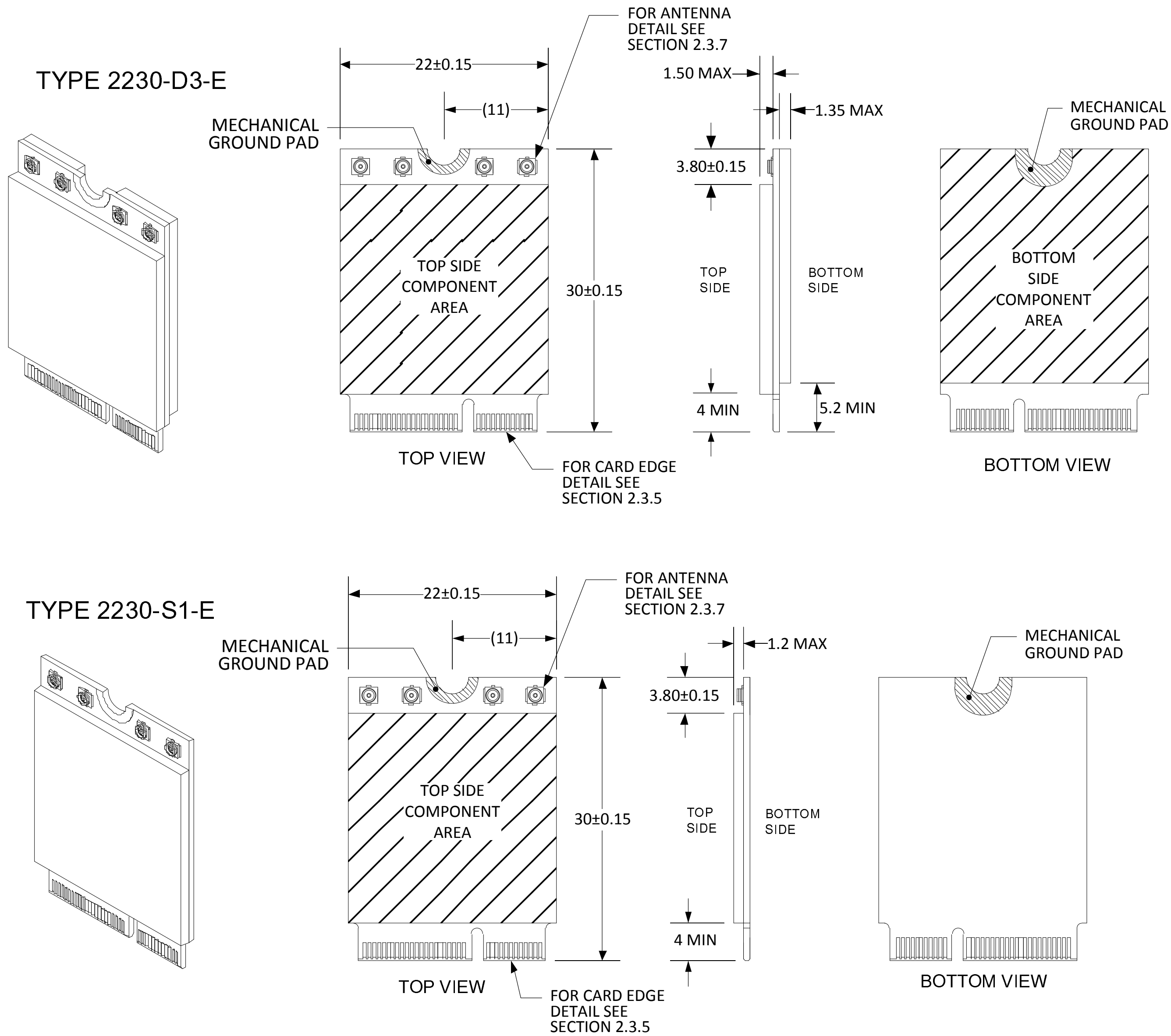


Figure 6. M2 Type 2230-D3/S1 Mechanical Outline Drawing Examples

2.3.1.2. Type 1630 Specification

Type 1630 is a smaller M.2 board/module size used for single Comm or more simplistic Comm combo solutions such as WiFi 1x1 or 2x2 + BT only or future multi-comm solutions that can fit in a smaller footprint.

The Type 1630 is a subset of the Type 2230 board with 5.5 mm sliced off along the entire length of the board. Therefore it is inherently limited in the number of RF connections and has a reduced number of pins used in the Host Interface connector.

Because the Type 1630 board/module utilizes only the first 57 pin locations (a mechanical key uses 8 pins and the connector uses 49 pins for the host interface), it is limited in its connection capability. Thus it is limited in the number of Comms that can be simultaneously supported on such a board/module.

The mounting hole and the mechanical key are exactly the same as those in the Type 2230 so that in principle the MB Socket can support both Type 2230 and Type 1630.

Note: Board/module Type 1630 is limited to Key ID A thru H only.

An example of the Type 1630 board/module mechanical outline drawing is shown in Figure 7.

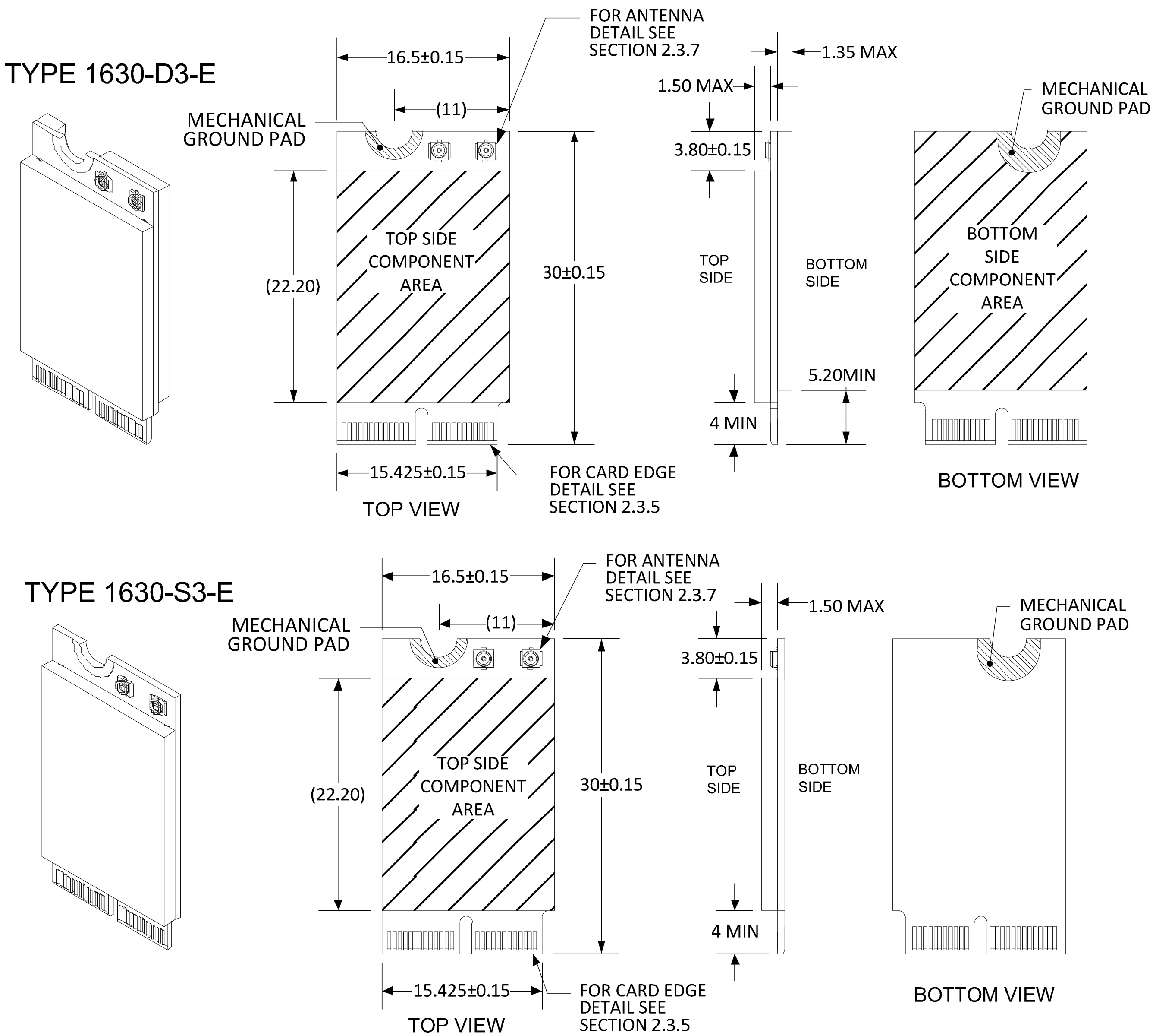


Figure 7. M.2 Type 1630-D3/S3 Mechanical Outline Diagram Examples

2.3.1.3. Type 3030 Specification

Type 3030 is an extended width M.2 board/module size used for more complex Comm combo solutions.

In principle the board is still comprised of three sections:

- Host I/F section
- RF connector and mounting hole section
- Active Component section

The active component section is 8 mm wider making an overall width of 30 mm (instead of the generic 22 mm width). The length remains the same at 30 mm so that it coincides with the other Type xx30 boards/modules.

An example of the Type 3030 board/module mechanical outline drawing is shown in Figure 8. The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors can be populated while maintaining the recommended 4.5 mm center-to-center distances. See section 2.3.7, *RF Connectors* in this document for recommended locations and assignments.

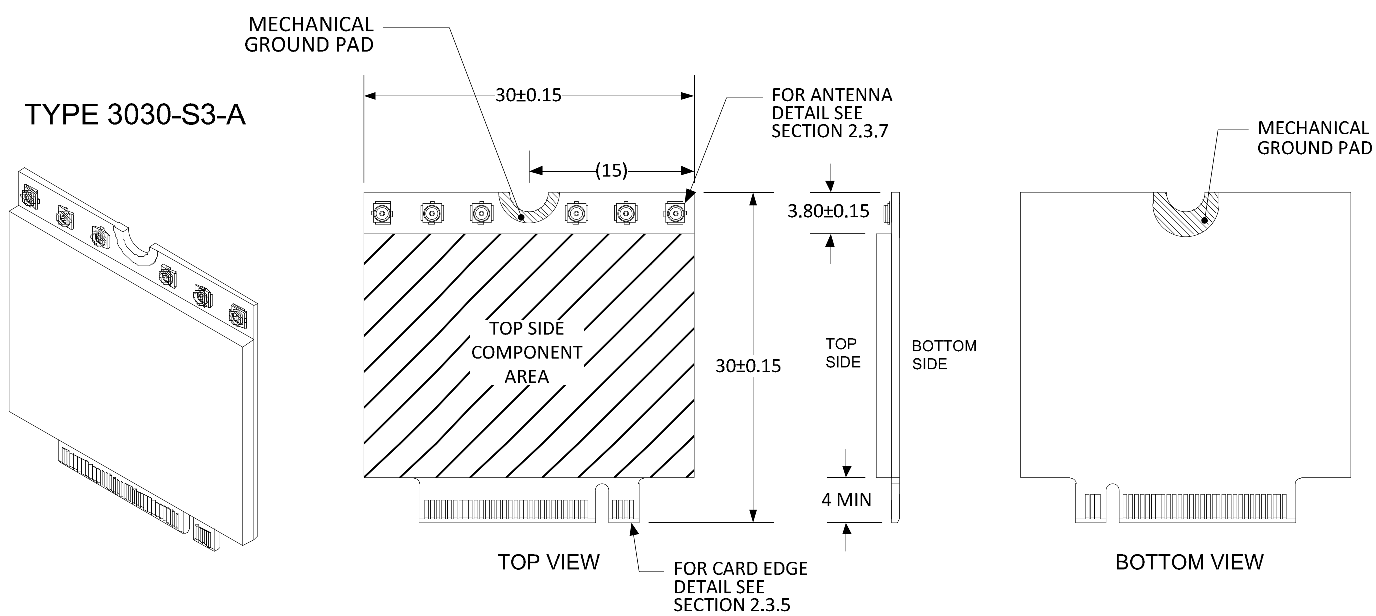


Figure 8. M.2 Type 3030 Mechanical Outline Diagram Example

2.3.2. Card Form Factor Intended for WWAN Socket 2

2.3.2.1. Type 3042 Specification

Type 3042 is an extended-width M.2 board/module size used for WWAN solutions.

In principle the board is still comprised of three sections:

- Host I/F section
- RF connector and mounting hole section
- Active Component section

The active component section is8 mm wider making it the same length as other board/module alternatives intended for Socket 2 with an overall length of 42 mm.

An example of the Type 3042 board/module mechanical outline drawing is shown in Figure 9.

The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors can be populated while maintaining the recommended 4.5 mm center-to-center distances. See 2.3.7, *RF Connectors* in this document for recommended locations and assignments.

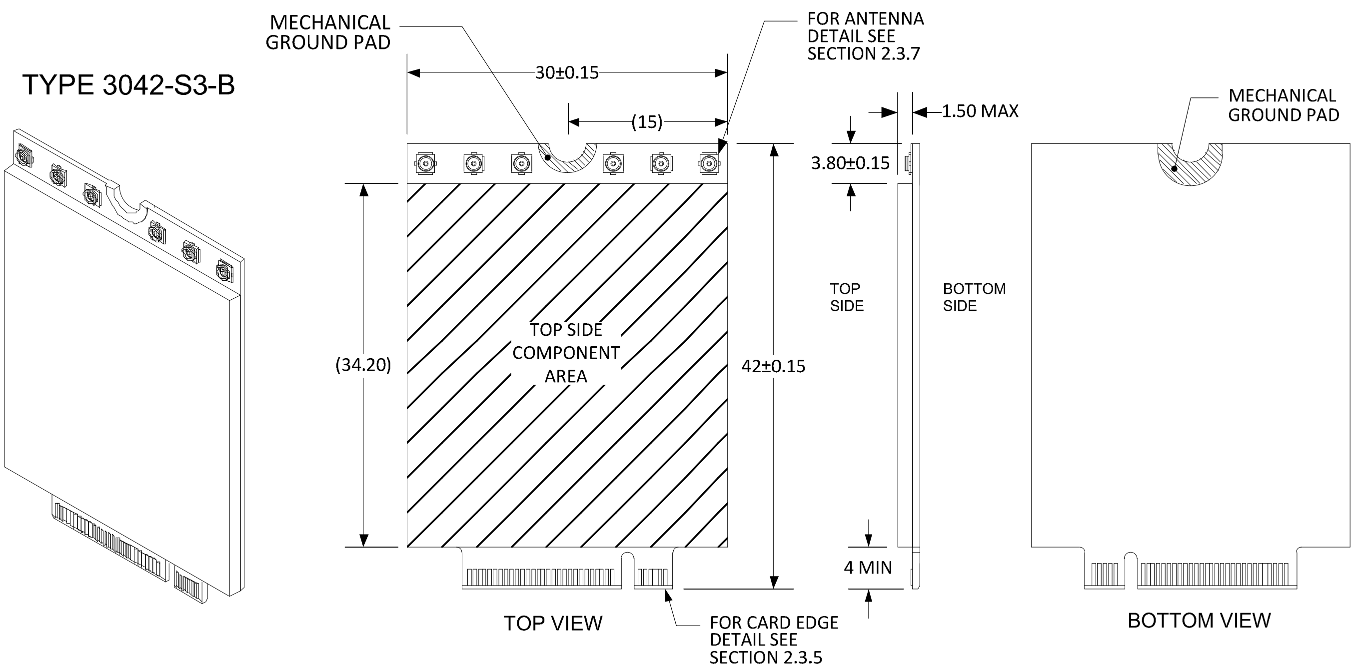


Figure 9. M.2 Type 3042 Single Sided Example Mechanical Outline Diagram Example

2.3.3. Card Form Factor for SSD Socket 2

2.3.3.1. Type 2230 Specification

Type 2230 is a M.2 board/module size used on Socket 2 and intended to support SSD Cache solutions and possibly other PCI Express based solutions. In principle the board is still comprised of two sections:

- Host I/F section
- Active Component section

The active component section with mounting hole has an overall length of 30 mm. Figure 10 shows Type 2230 board/module mechanical outline drawing.

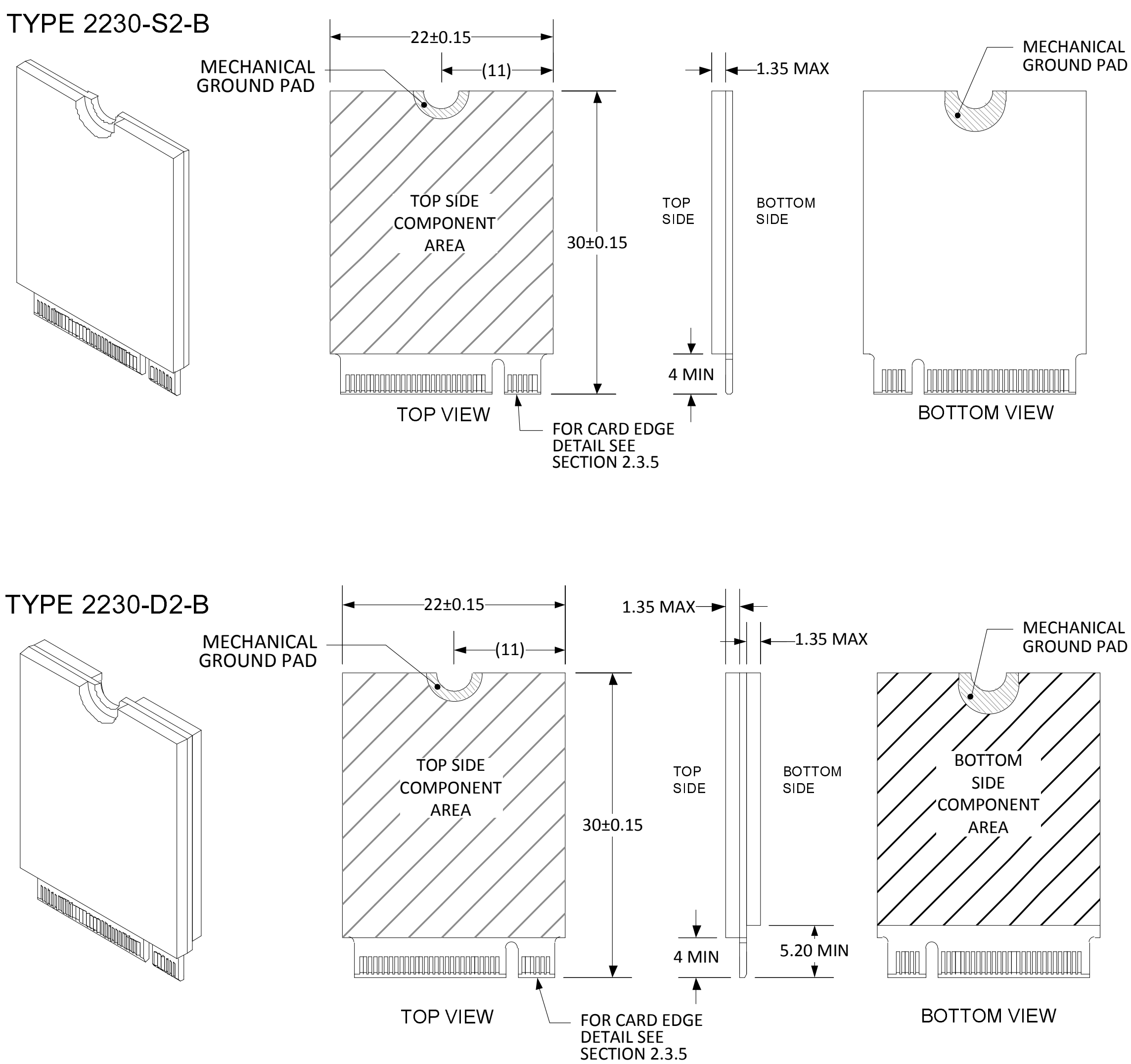


Figure 10. M.2 Type 2230 Mechanical Outline Diagram Examples

2.3.4. Card Form Factors for SSD Socket 2 and 3

2.3.4.1. Type 2242 Specification

Type 2242 is a M.2 board/module size used on Socket 2 and intended to support SSD solutions and possibly other PCI Express based solutions. In principle the board is still comprised of two sections:

- Host I/F section
- Active Component section

The active component section with mounting hole has an overall length of 42 mm (instead of the generic 30 mm length). Figure 11 shows Type 2242 board/module mechanical outline drawing. The SSD module can take advantage of the Dual Module key scheme to enable this module to plug into two different SSD-capable Sockets (for example; Socket 2 and Socket 3).

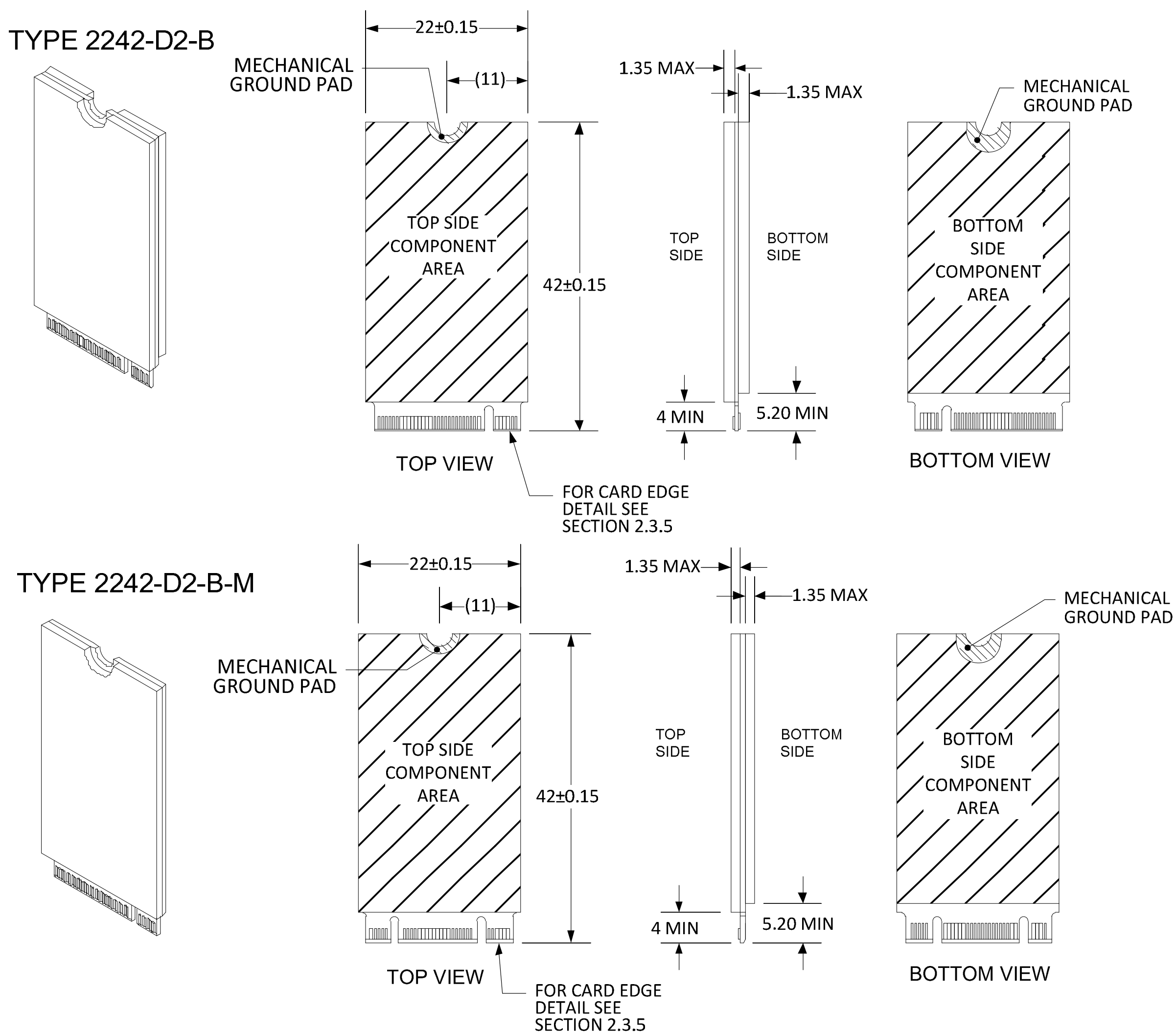


Figure 11. M.2 Type 2242 Mechanical Outline Diagram Examples

2.3.4.2. Type 2260 Specification

Type 2260 board/module is primarily intended to support high capacity SSD solutions. Figure 12 shows an example of Type 2260.

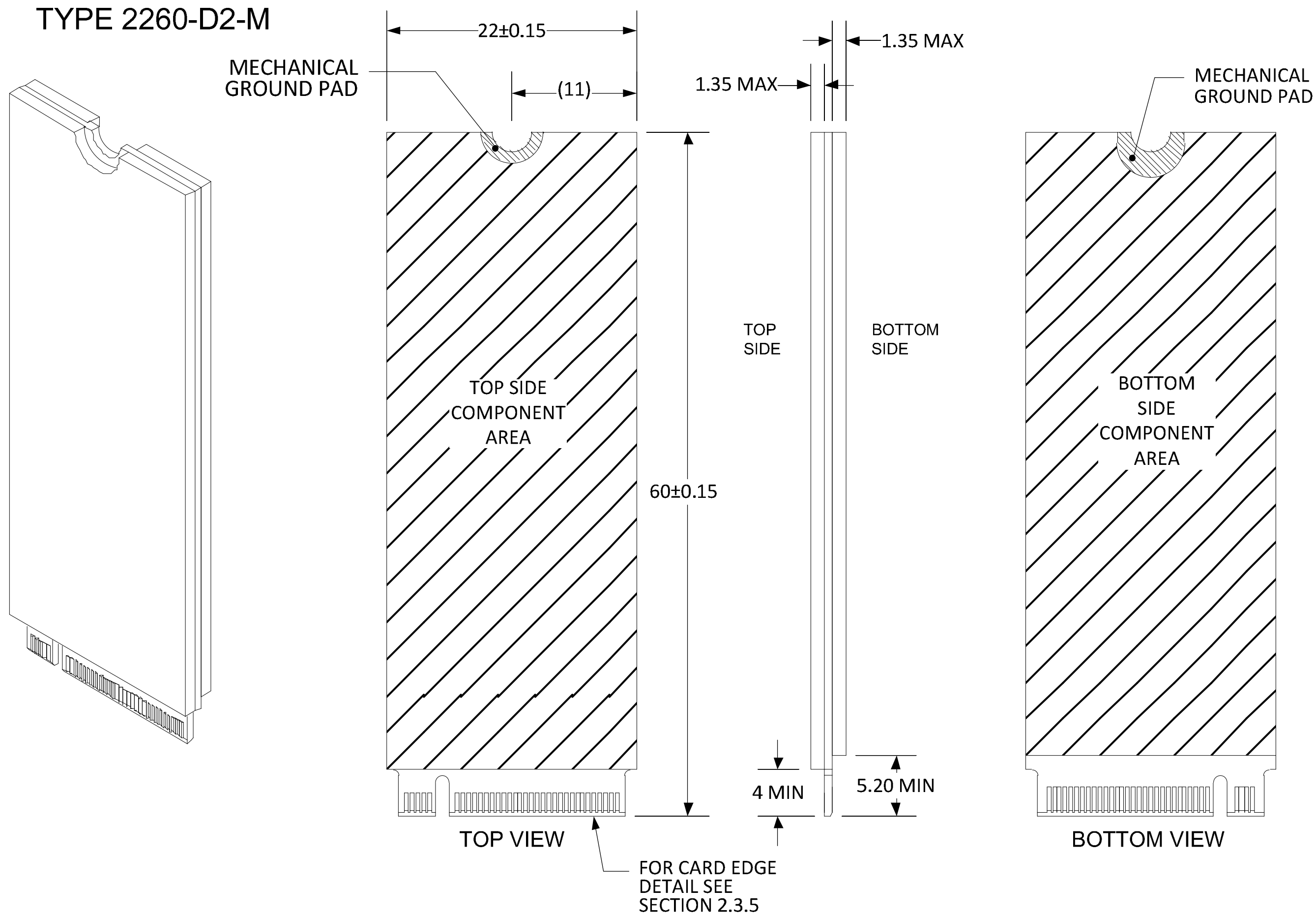


Figure 12. M.2 Type 2260 Mechanical Outline Drawing Example

2.3.4.3. Type 2280 Specification

This board/module type is primarily intended to support high-capacity SSD solutions. Figure 13 shows an example of board Type 2280.

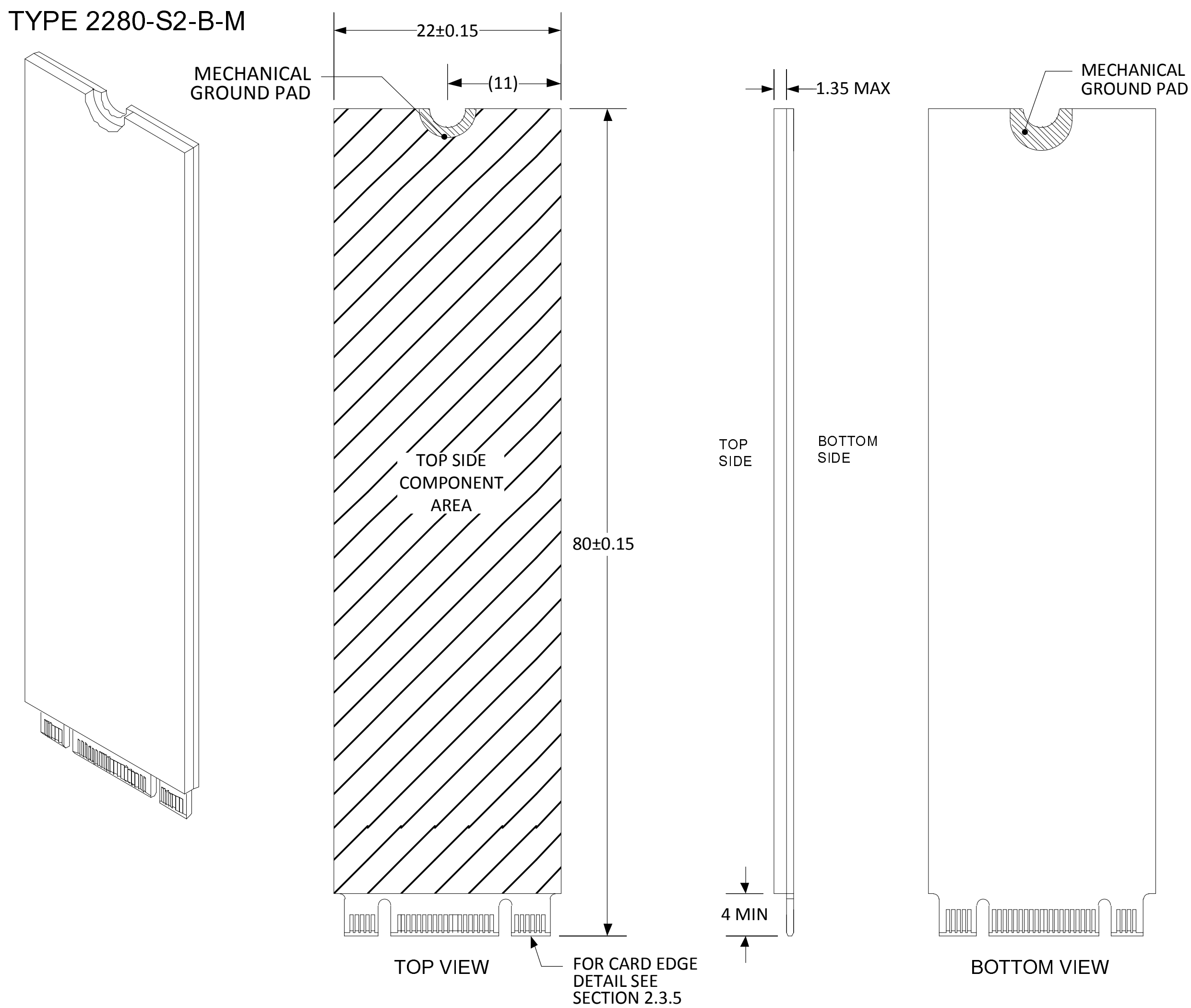


Figure 13. M.2 Type 2260 Mechanical Outline Drawing Example

2.3.4.4. Type 22110 Specification

This board/module type is primarily intended to support high-capacity SSD solutions. Figure 14 shows an example of specific board type(s).

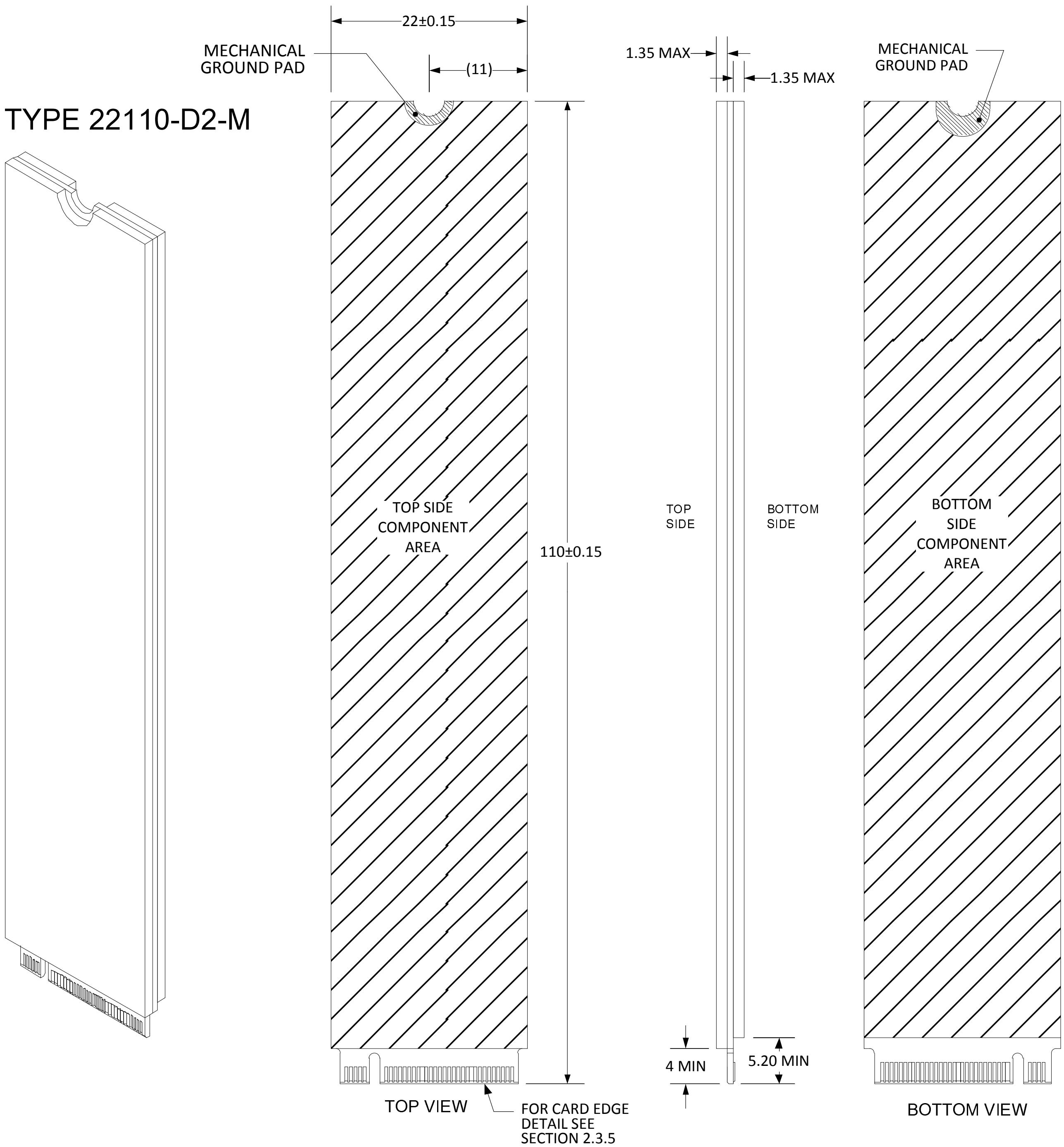


Figure 14. M.2 Type 22110 Mechanical Outline Drawing Example

2.3.5. Card PCB Details

2.3.5.1. Mechanical Outline of Card-Edge

Figure 15, Figure 16, and Figure 17 show typical card-edge mechanical outlines.

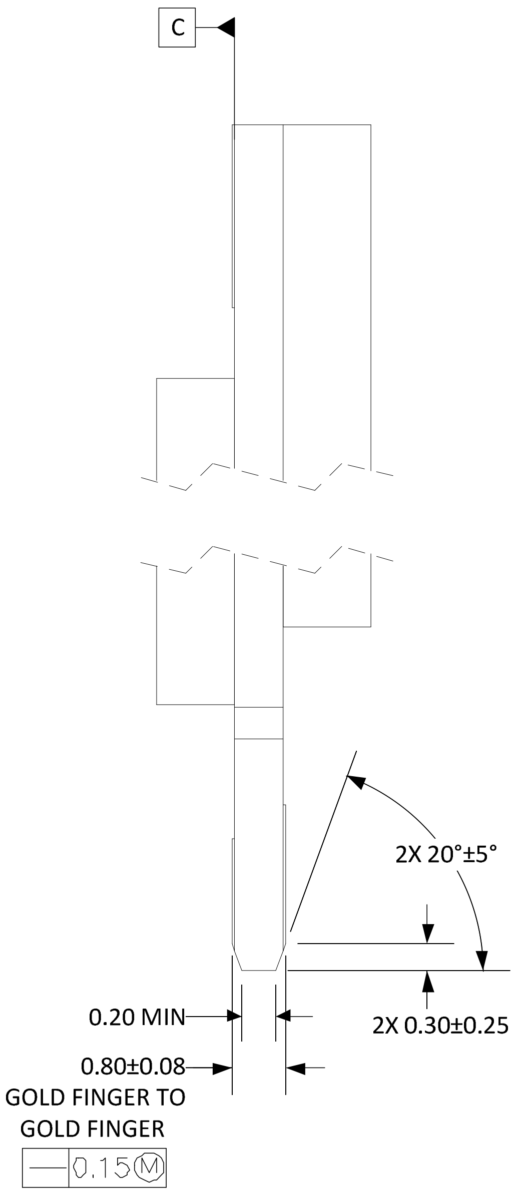


Figure 15. Card Edge Bevel

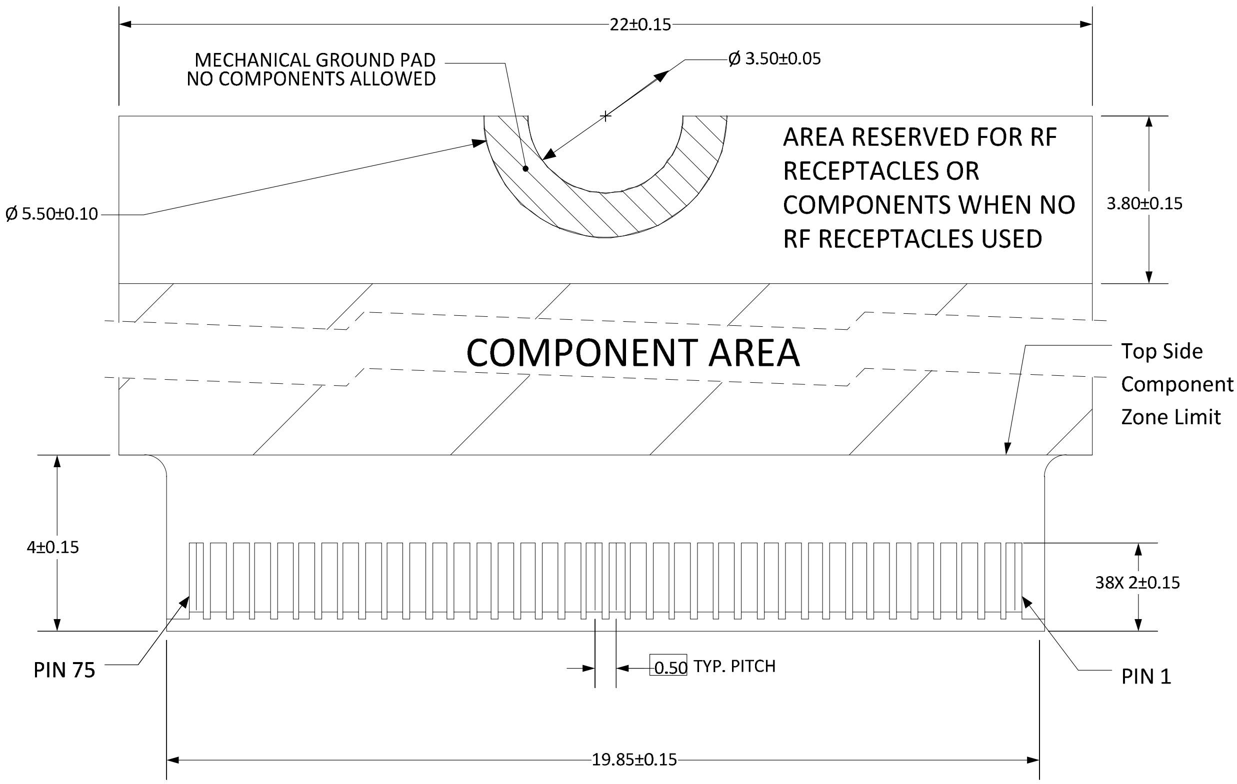


Figure 16. Card Edge Outline-Topside

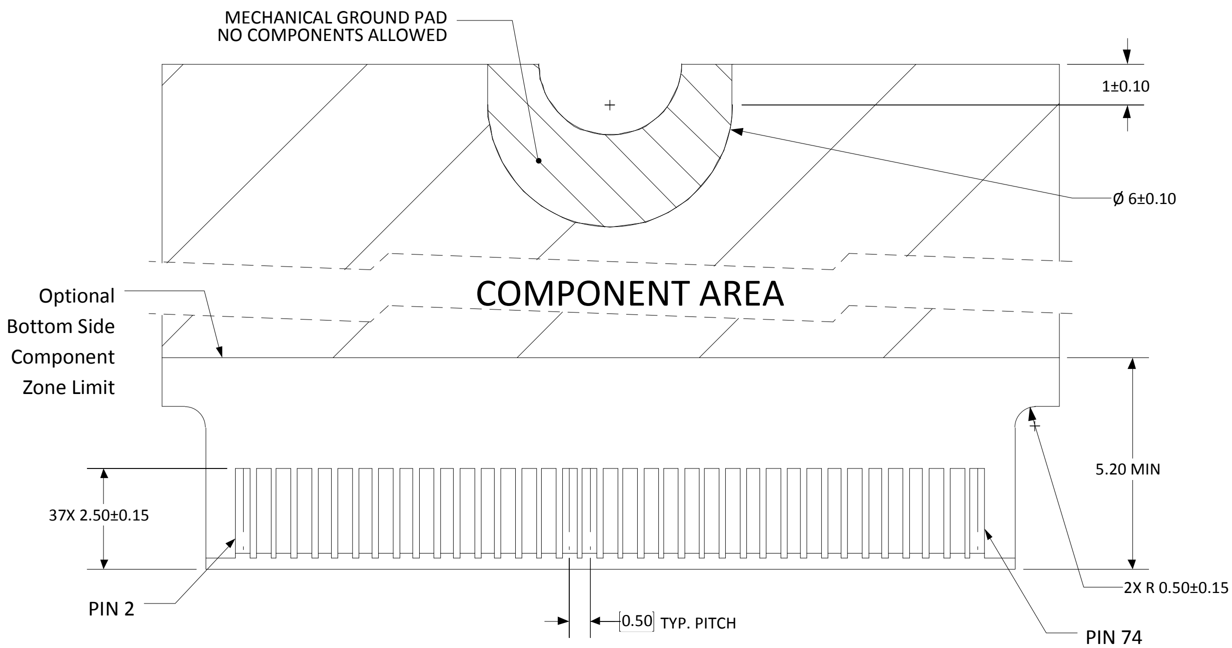


Figure 17. Card Edge Outline-Backside

2.3.5.2. Module Keying

Note: Key G is shown for reference only! This Key is allocated for custom use at one's own risk. It is not used for M.2 spec compliant devices

Keying is required to provide configurability as well as preventing incompatible module insertion. See the following figures and tables for dimensional values.

- Figure 18. Key Detail for Keys A Thru F
- Figure 19. Key Detail for Keys G Thru M
- Table 3. Key Location/Pin Block Dimensions for Keys A - F
- Table 4. Key Location/Pin Block Dimensions for Keys G - M
- Figure 20. Dual Key A-E Example
- Figure 21. Dual Key B-M Example

The key locations and pin block dimensions for Keys A thru F are listed in Table 3. Table 4 lists Keys G thru M .The key designation identifier should be marked with either Silk Screen, reverse copper etching, or solder mask removal on the Top-side of the module board to the right of the module key, as shown in Figure 18 and Figure 19. The letter size should be at least 1 mm tall.

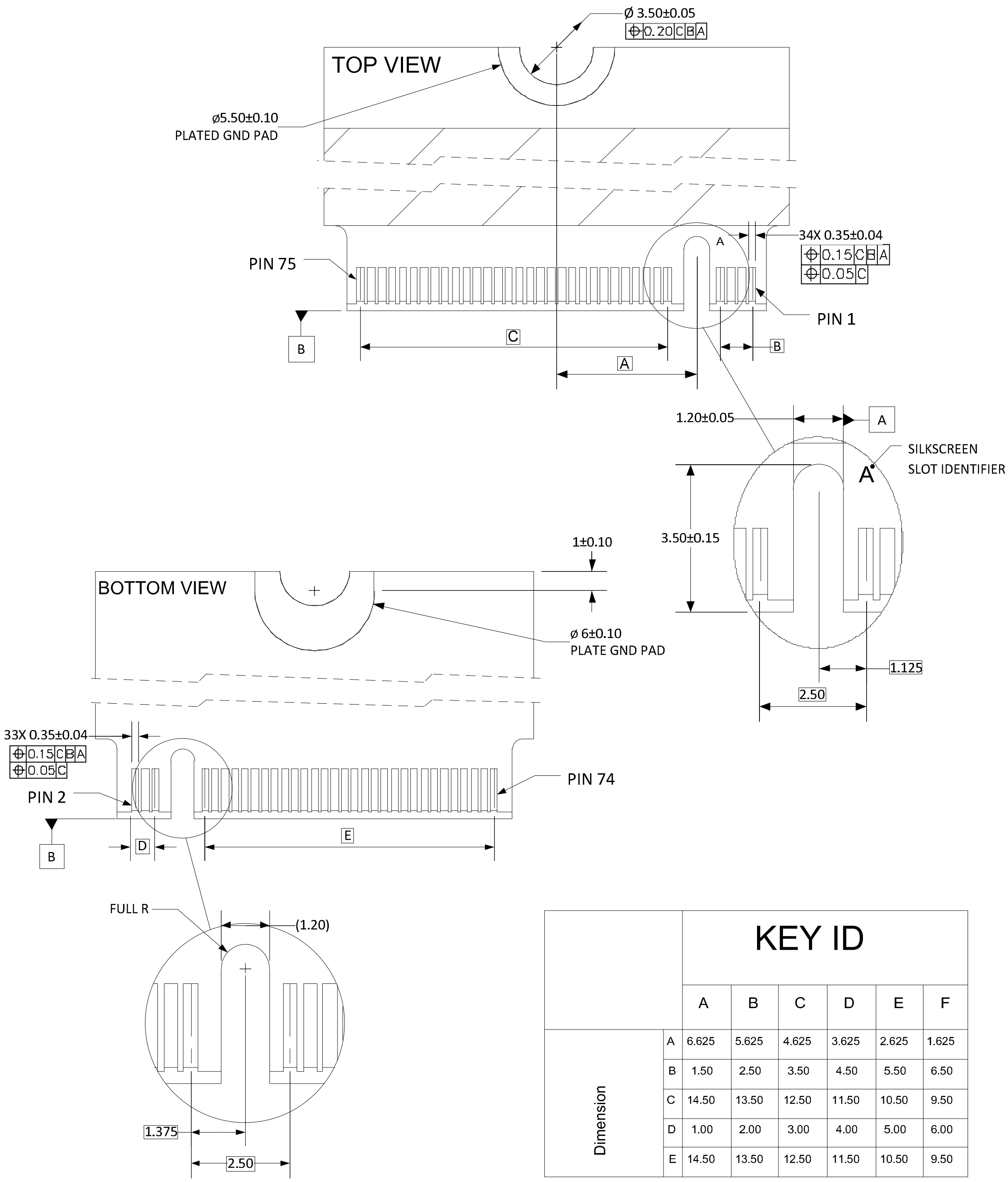
Table 3. Key Location/Pin Block Dimensions for Keys A - F

	Key ID					
Dimension	**A**	**B**	**C**	**D**	**E**	**F**
A	6.625	5.625	4.625	3.625	2.625	1.625
B	1.50	2.50	3.50	4.50	5.50	6.50
C	14.50	13.50	12.50	11.50	10.50	9.50
D	1.00	2.00	3.00	4.00	5.00	6.00
E	14.50	13.50	12.50	11.50	10.50	9.50

Table 4. Key Location/Pin Block Dimensions for Keys G - M

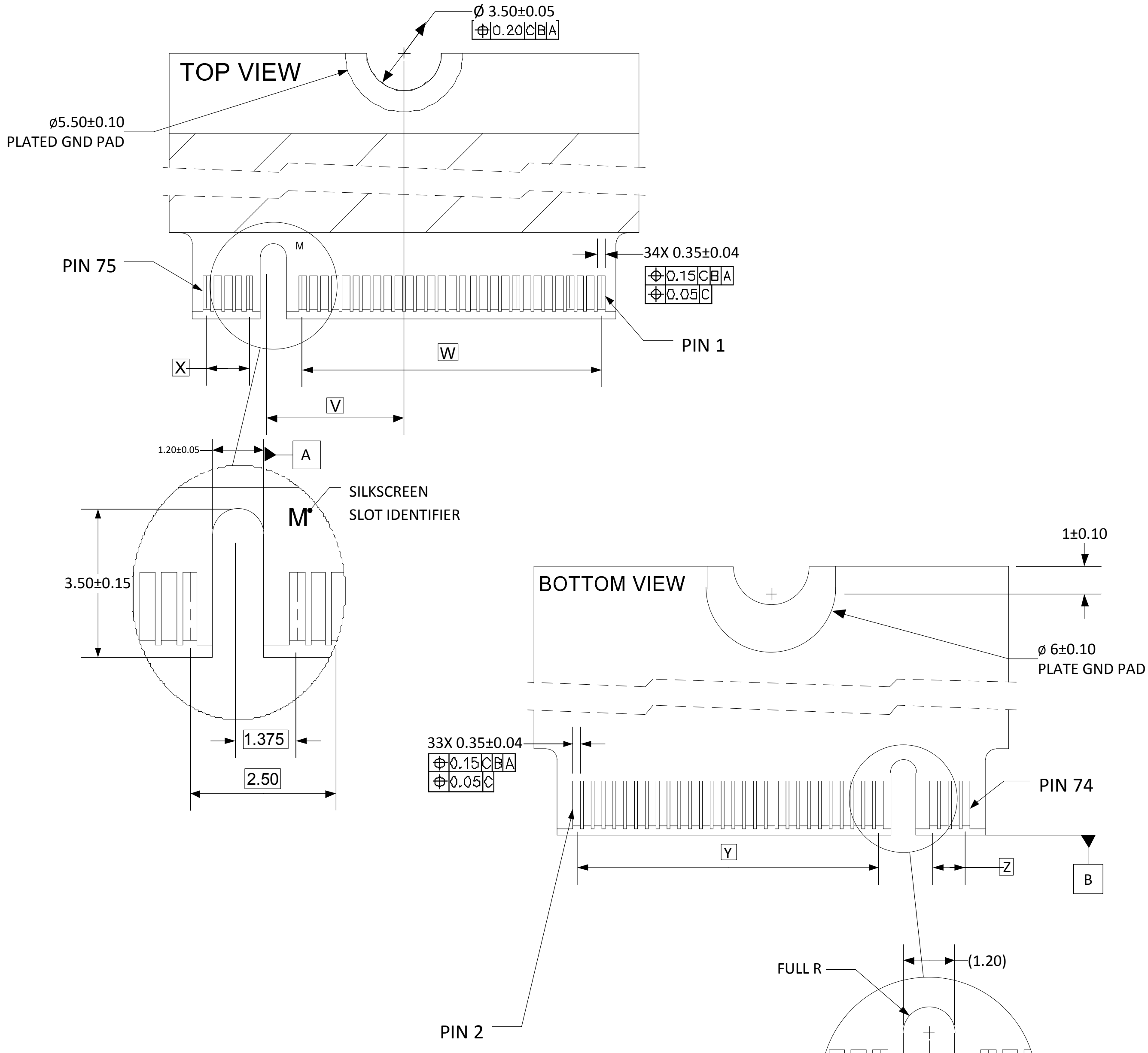
	Key ID					
Dimension	**G**	**H**	**J**	**K**	**L**	**M**
V	1.125	2.125	3.125	4.125	5.125	6.125
W	9.00	10.00	11.00	12.00	13.00	14.00
X	7.00	6.00	5.00	4.00	3.00	2.00
Y	9.00	10.00	11.00	12.00	13.00	14.00
Z	6.50	5.50	4.50	3.50	2.50	1.50

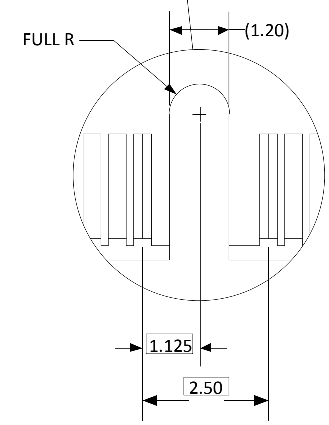
Two Key designation identifiers should be marked when the module employees a dual module key scheme as shown in Figure 20 and Figure 21.



		KEY ID					
		A	B	C	D	E	F
Dimension	A	6.625	5.625	4.625	3.625	2.625	1.625
	B	1.50	2.50	3.50	4.50	5.50	6.50
	C	14.50	13.50	12.50	11.50	10.50	9.50
	D	1.00	2.00	3.00	4.00	5.00	6.00
	E	14.50	13.50	12.50	11.50	10.50	9.50

Figure 18. Key Detail for Keys A Thru F





		KEY ID					
		G	H	J	K	L	M
Dimension	V	1.125	2.125	3.125	4.125	5.125	6.125
	W	9.00	10.00	11.00	12.00	13.00	14.00
	X	7.00	6.00	5.00	4.00	3.00	2.00
	Y	9.00	10.00	11.00	12.00	13.00	14.00
	Z	6.50	5.50	4.50	3.50	2.50	1.50

Figure 19. Key Detail for Keys G Thru M

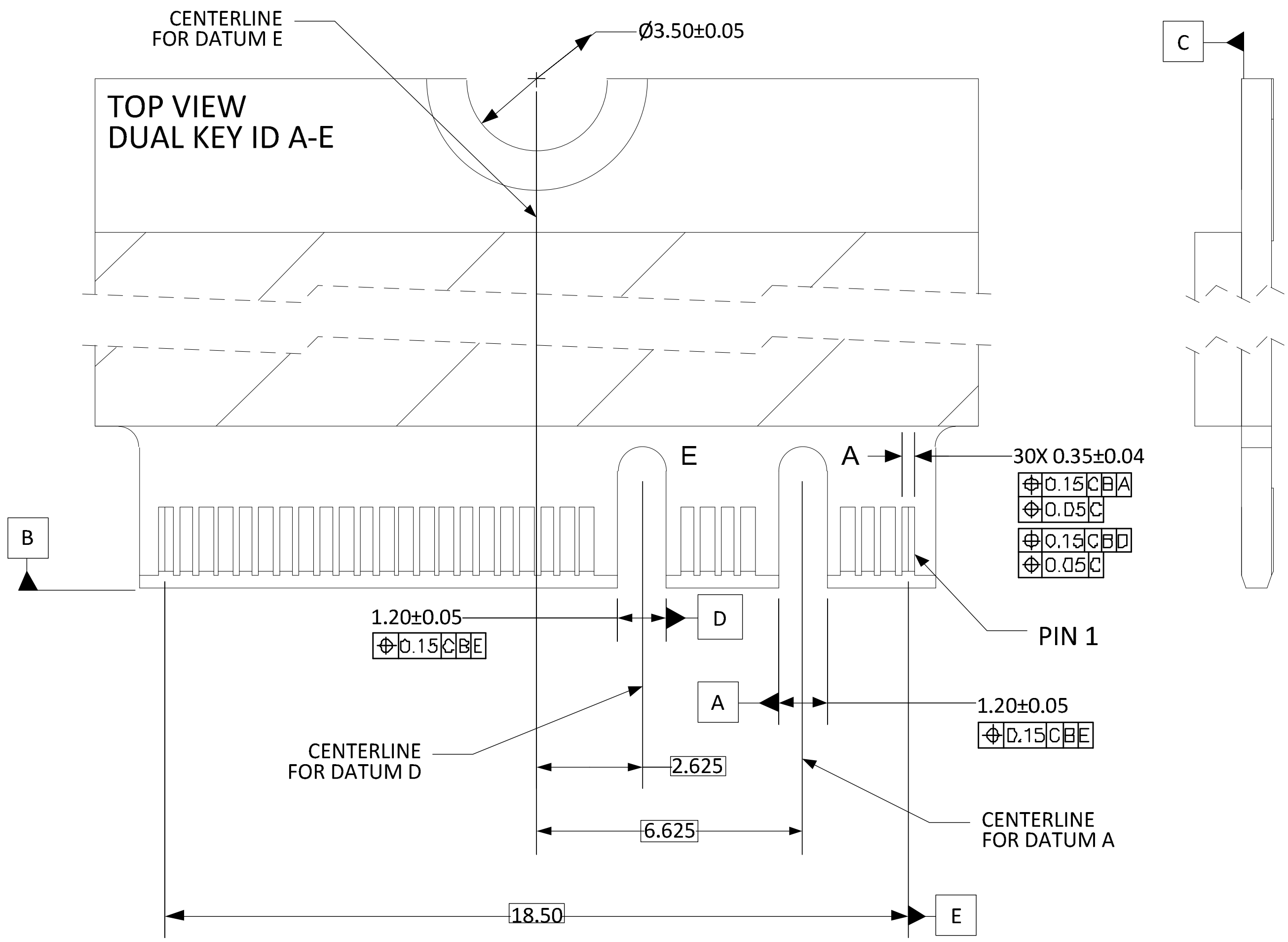


Figure 20. Dual Key A-E Example

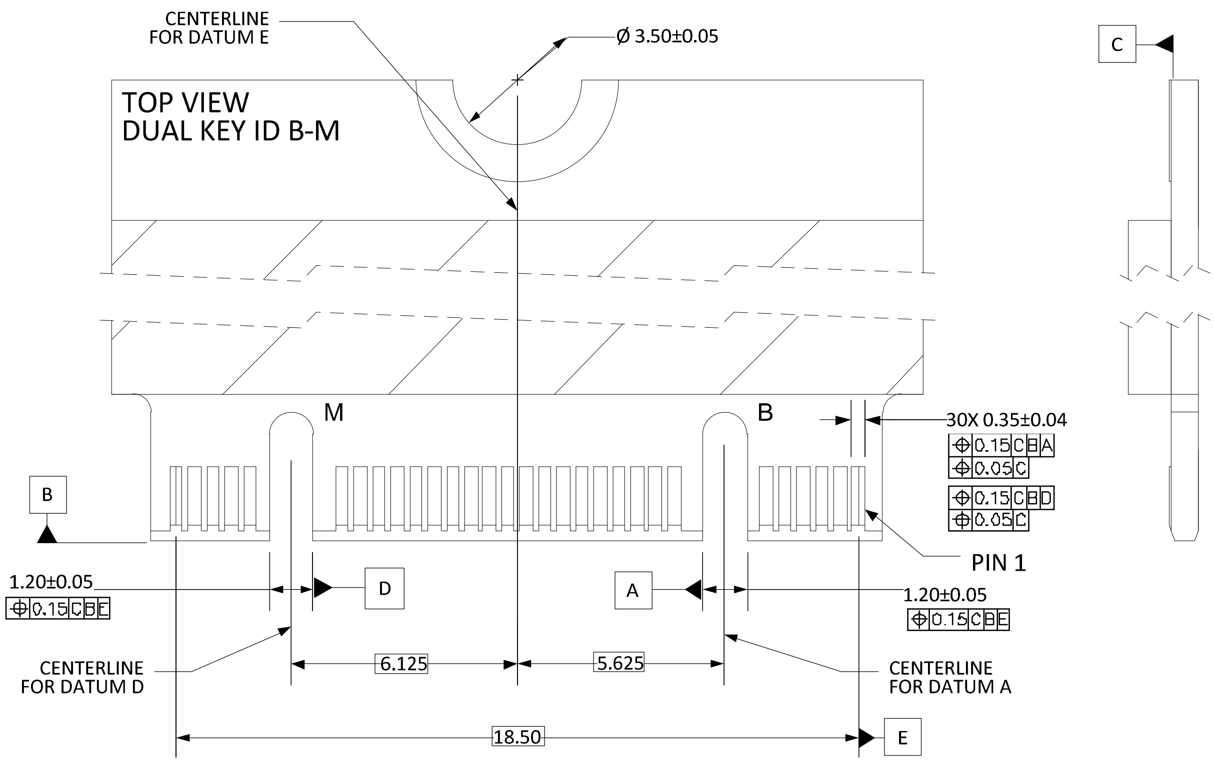


Figure 21. Dual Key B-M Example

2.3.6. Soldered-down Form Factors

2.3.6.1. Type 2226 Specification

Type 2226 board/module is a soldered-down, single sided version of Type 2230 board/module. It is therefore assuming the same board technology and silicon package technology. It has an LGA land pattern on the backside instead of the 75 position Host Interface Edge Card gold finger connector. As a result, type 2226 is 4 mm shorter.

To help prevent module-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers(i.e. outer to outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 22 shows the mechanical outline drawing for board/module Type 2226.

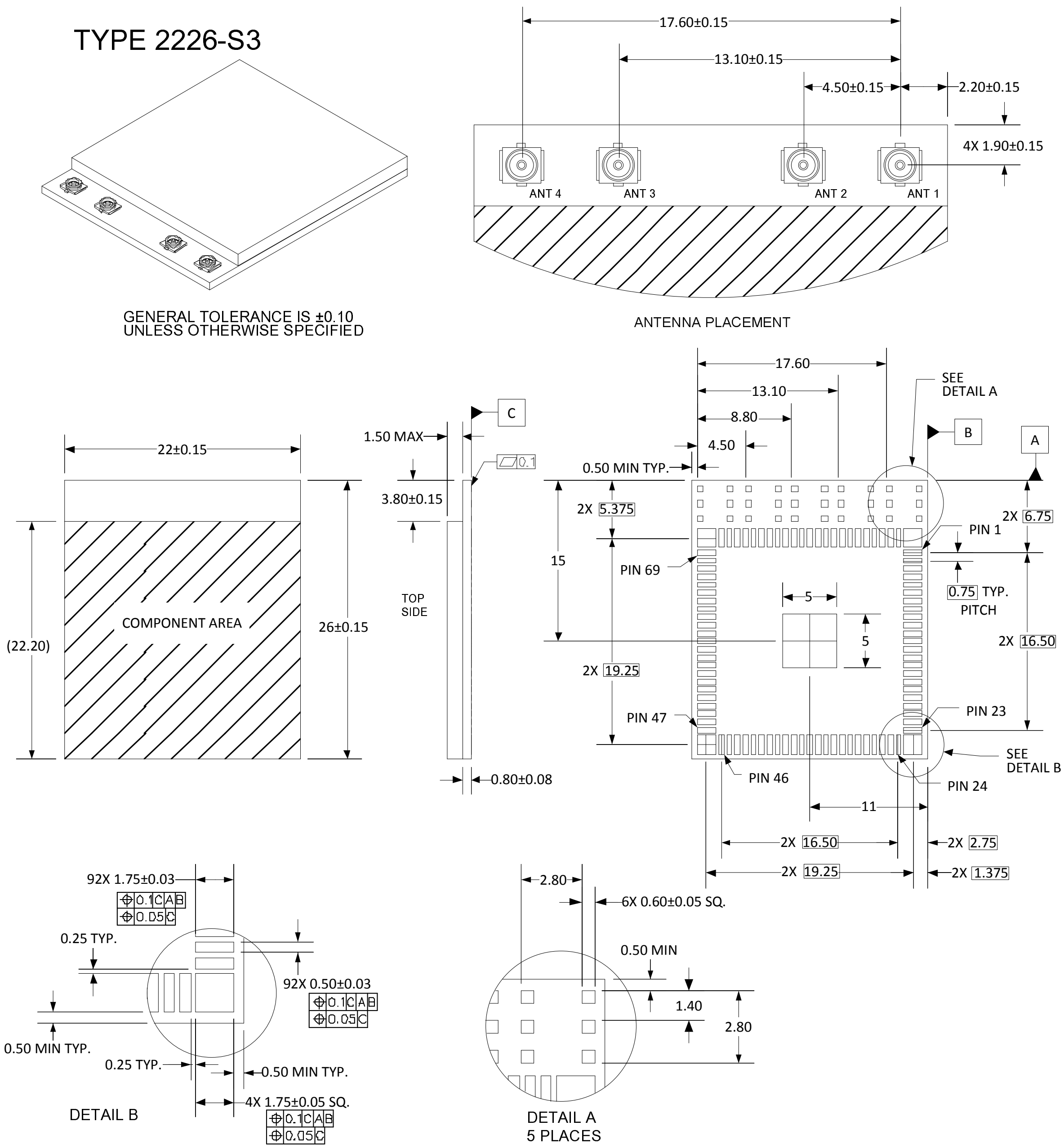


Figure 22. M.2 Type 2226-S3 Mechanical Outline Drawing

Footprint and copper area balance verbiage placeholder

2.3.6.2. Type 1216 Specification

This board/module type is another single-sided soldered-down solution based on a higher density interconnect technology and a smaller silicon package technology. It has an LGA land pattern on the backside and therefore the size is smaller.

To help prevent module-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (for example, outer to outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 23 shows the mechanical outline drawing for board/module Type 1216.

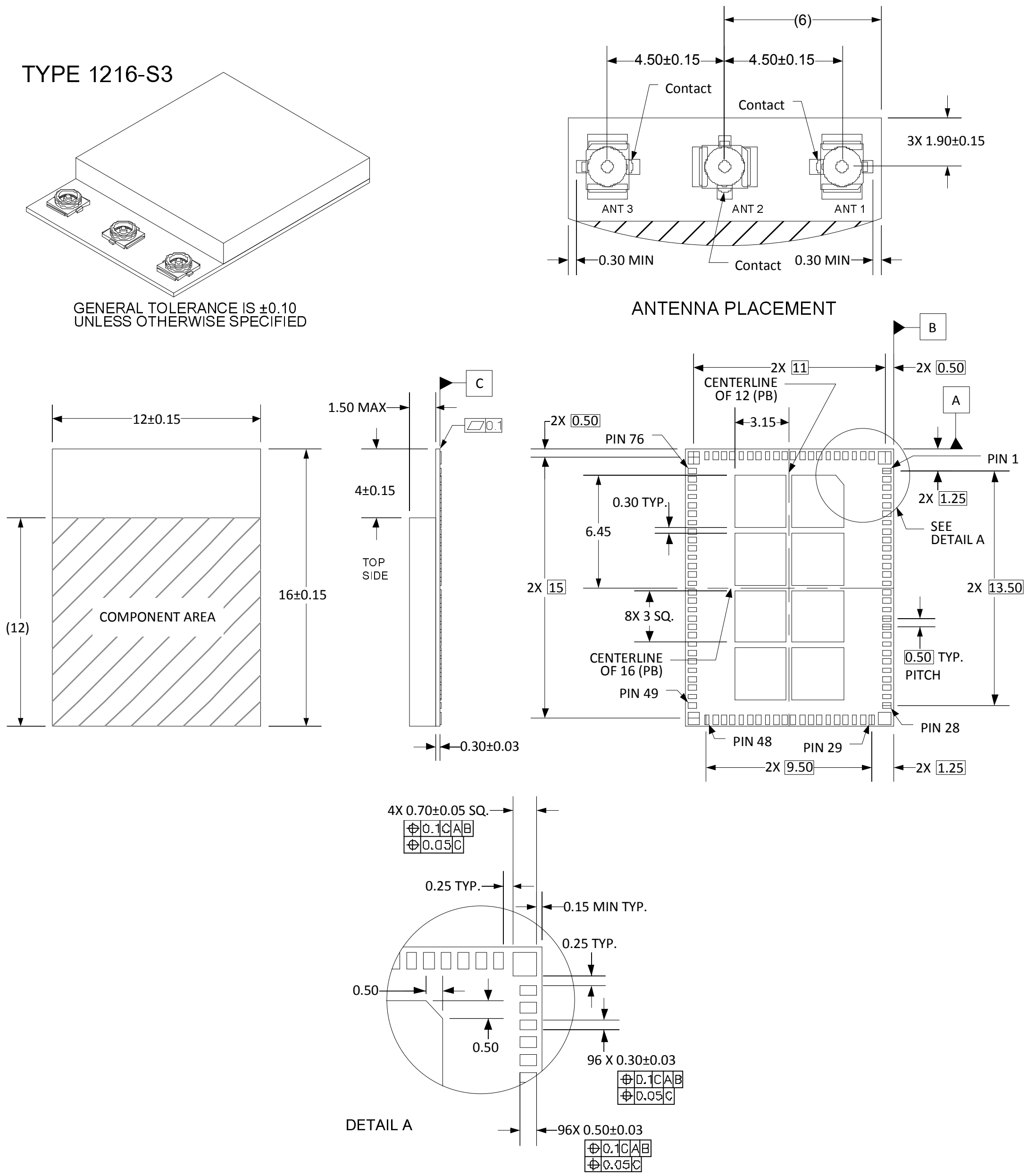


Figure 23. Type 1216 Soldered Down Solution Module Diagram

2.3.6.3. Type 3026 Specification

This board/module type is a single sided soldered-down version of the Type 3030 board/module and assumes the same board and silicon package technology. It has a unique LGA land pattern on the backside instead of the 75 position Host Interface Edge Card gold finger connector. This LGA pattern can accommodate a Type 2226 module as a drop-in replacement located at the center with two sets of LGA pads along the sides that cover the entire 3026 module size. Like the Type 2226 module, the module size is also 4 mm shorter than the Edge Card gold finger version.

To help prevent the module from warping, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (for example; outer-to-outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 24 shows the mechanical outline drawing for board/module Type 3026. See Figure 25 for more detailed information.

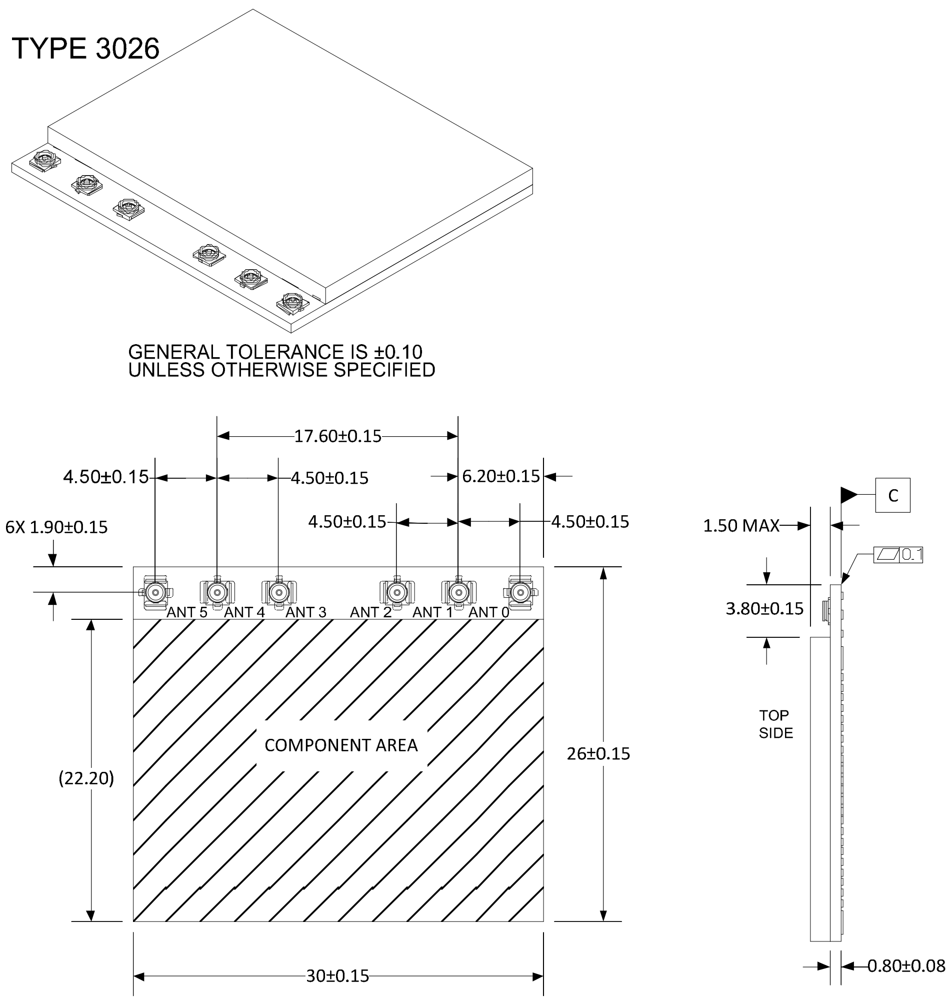


Figure 24. M.2 Type 3026-S3 Mechanical Outline Drawing

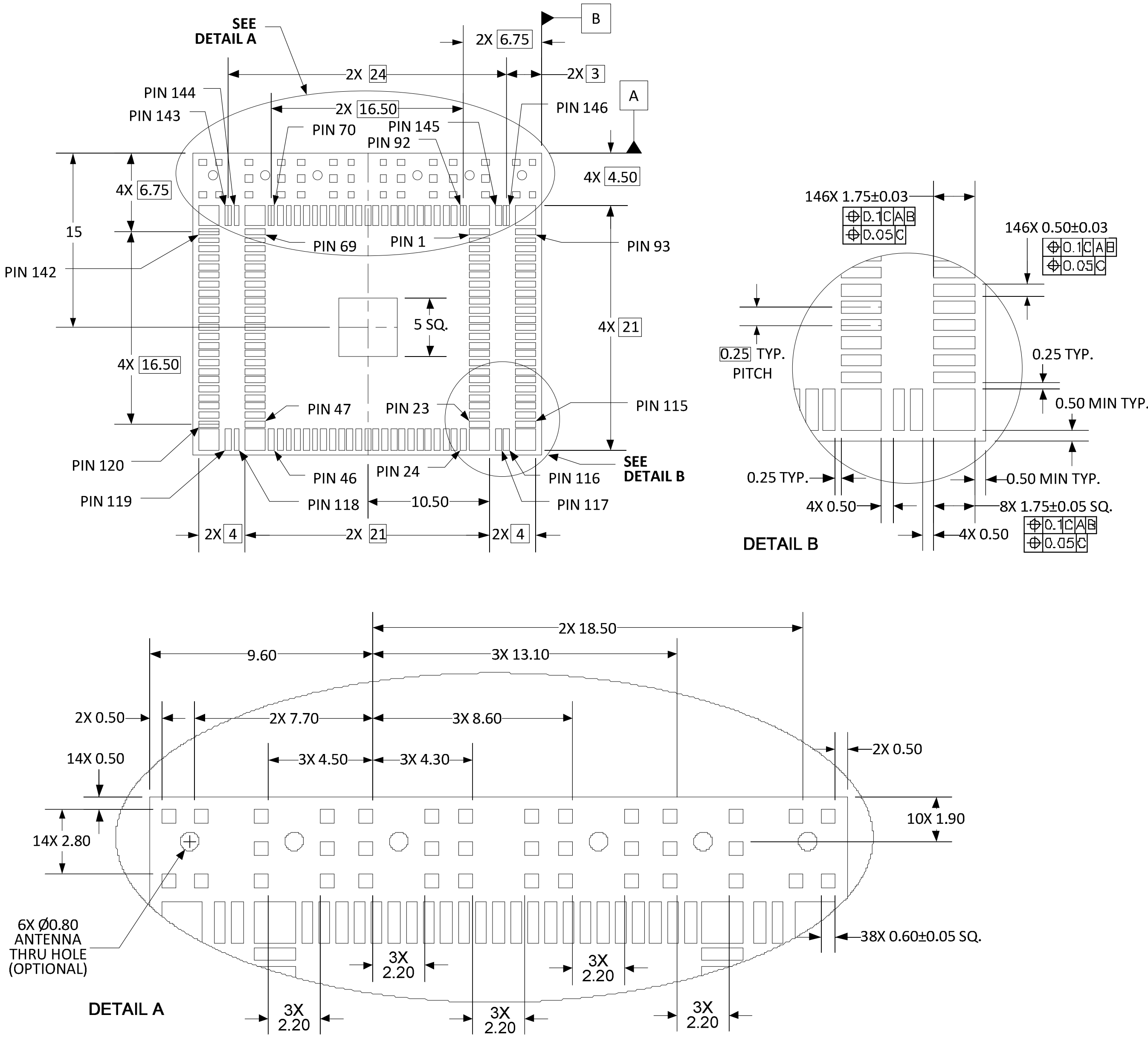


Figure 25. M.2 Type 3026-S3 Mechanical Outline Drawing Details

2.3.7. RF Connectors

The top end of the wireless module board area is the preferred location for the RF connectors. However, other areas can be used in cases that this area is not enough at the expense of the component area (Figure 26).

The standard 2x2 mm size RF receptacle connectors (Figure 27) to be used in conjunction with the M.2 boards/modules will accept two types of mating plugs that will meet a maximum Z-height of 1.45 mm (Figure 28) utilizing a Ø 1.13 mm coax cable or a maximum Z-height of 1.2 mm using a Ø 0.81 mm coax cable (Figure 29). Figure 30 shows the antenna connector.

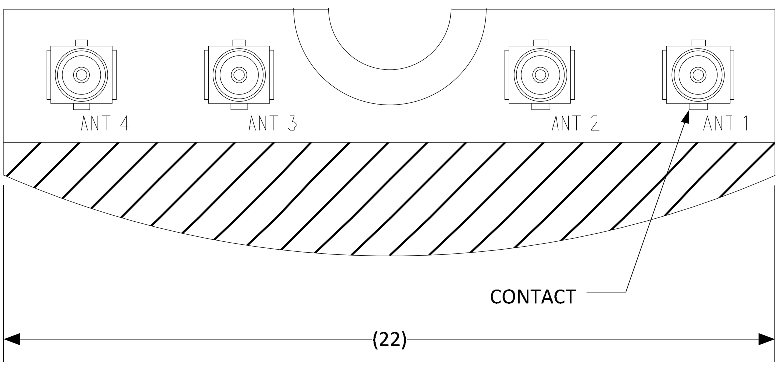


Figure 26. Board Type 2230 Antenna Connector Designation Scheme

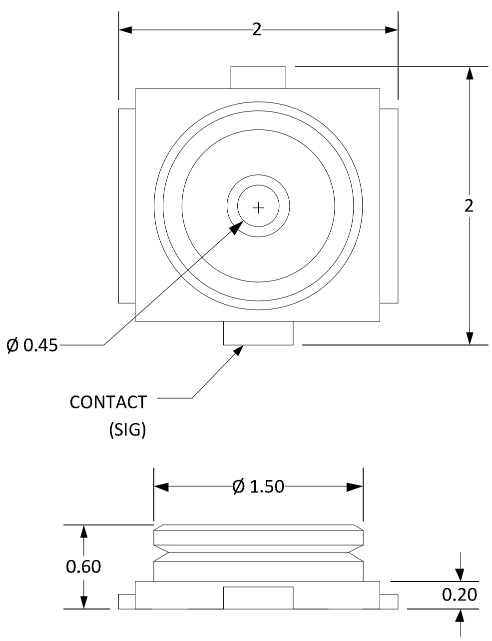


Figure 27. Generic 2x2 mm RF Receptacle Connector Diagram

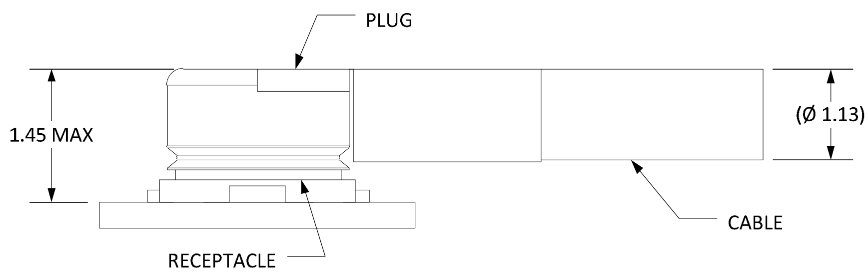


Figure 28. Mated Plug for Ø 1.13 mm Coax Cable

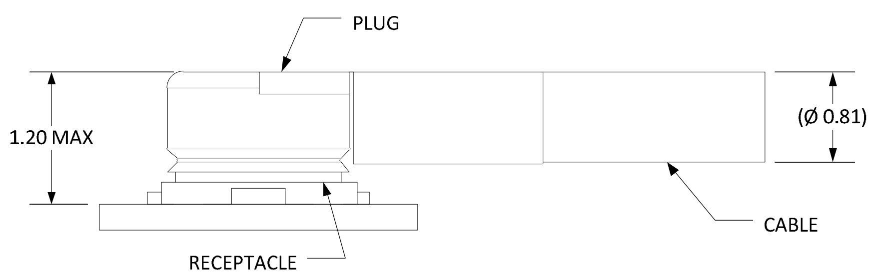


Figure 29. Mated Plug for Ø 0.81 mm Coax Cable

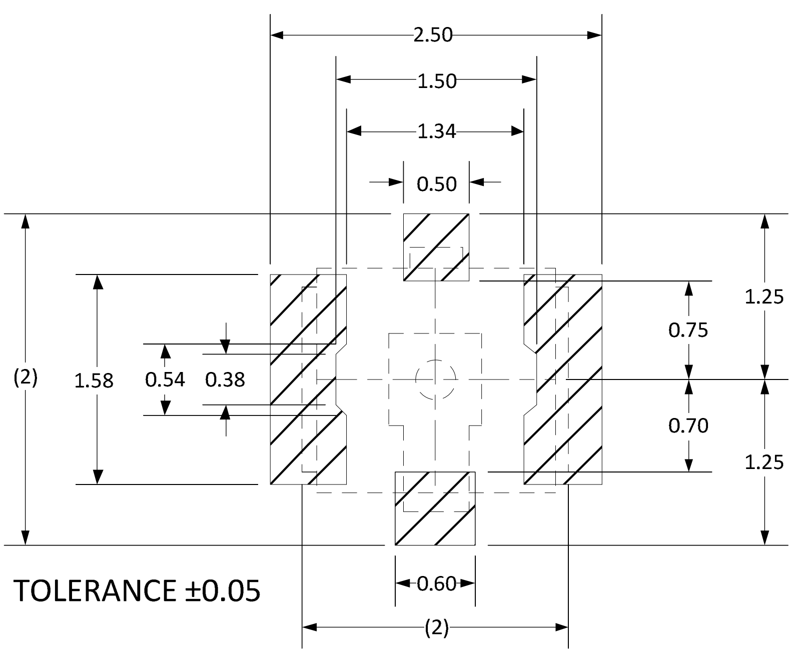


Figure 30. Antenna Connector PCB Recommended Land Pattern

The Module RF Connector will be able to accept/mate with both the Ø 0.81mm coax cable (Figure 29) and the Ø 1.13 mm coax cable (Figure 28) plugs.

Some *Reference Data Sheets* for the standard RF connectors can be seen at their respective web sites. The minimum requirements for the RF Connector are listed in Tables 5 through 9.

Table 5. RF Connector Physical Characteristics

Characteristic	Description
Receptacle Physical Outline	2 x 2 x 0.60 mm
Receptacle OD	1.5 mm
Housing Material	High Temperature Plastic
Flammability	UL 94-V0
Contact Material	Copper Alloy/Gold Plating
Ground Contact Material	Copper Alloy/Gold Plating

Table 6. RF Connector Mechanical Requirements

Description	Standard Requirement	Improved Requirement
Mating force	30 N maximum	
Un-mating force	5 N initial, 3 N minimum after 30 cycles, 20 N maximum	
Cable Retention at 0 Degree Pull (Parallel to PCB)	5 N min	20 N min
Cable Retention at 30 Degree Pull (PCB to Cable Angle)	Not Recommended	10 N min
Durability (# of mating cycles)	30 cycles (Contact Resistance-20 mΩ)	
Receptacle Shearing Strength	20 N min	
Vibration	No momentary disconnections of 1 micro-sec/min	

Table 7. RF Connector Electrical Requirements

Description	Requirements
Voltage Rating	60V AC
Current Rating	1.0 A Maximum
Impedance	50 Ω
Receptacle VSWR- 100MHz to about ~3 GHz[1]	1.3 Maximum
Receptacle VSWR- 3 GHz to ~6 GHz[1]	1.45 Maximum
Optional Enhanced Frequency Receptacle VSWR- 3 GHz to ~12GHz[1,2]	2.0 Maximum
Contact Resistance	Inner: 20 mΩ Maximum
	Outer: 20 mΩ Maximum
	Initial: 10 mΩ Maximum
Dielectric Withstanding Voltage	200V AC for one minute
Insulation Resistance	500 mΩ for one minute at 100 V DC

Note: [1] The VSWR of the receptacle is measured differently than the VSWR of the mating plug (see Section 6.4).

[2] The optional Enhanced frequency performance to 12 GHz to be provided upon specific request.

Table 8. RF Connector Environmental Requirements

Description	Requirement
Operating Temperature Range	-40˚C to +85˚C
Humidity	90%
Soldering Heat Resistance	Lead Free Reflow up to 260˚C peak for 10 sec
RoHs Compliant/Halogen Free	Must be compliant

2.3.7.1. Socket 1 & 2 RF Connector Pin-Out

The RF Connector area will allow two (2), four (4), or six (6) RF connectors to be placed as a function of the board Type.

- Type 22xx can support up to four RF Connectors
- Type 1630 can support up to two RF Connectors
- Type 30xx can support up to six RF Connectors

To remain consistent with the Host I/F pin order, the RF connectors are labeled ANT0, ANT1, ANT2, ANT3, ANT4, and ANT5 from right to left. The recommended antenna function allocation is given in Table 9.

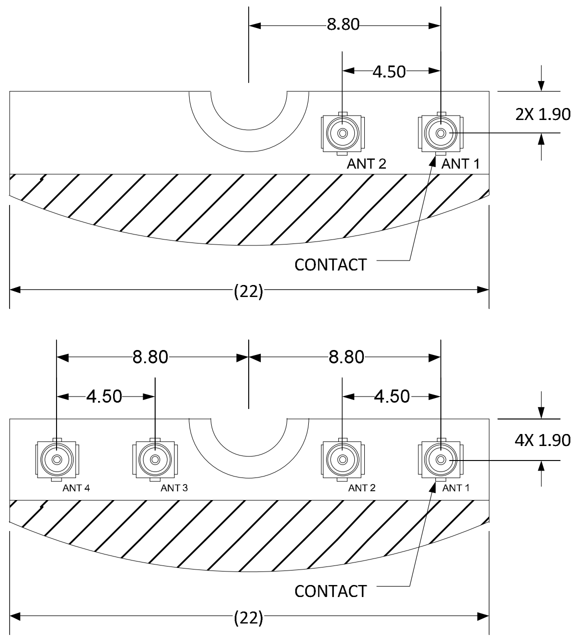
Table 9. Recommended Antenna Function Allocation Table

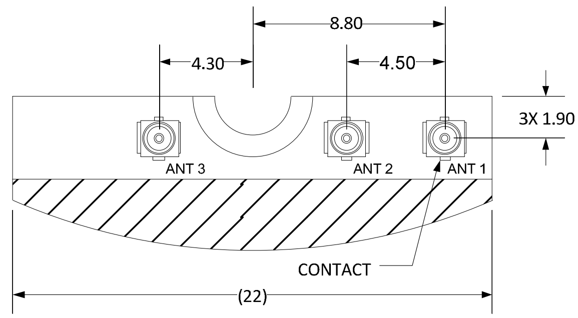
Type	ANT5	ANT4	ANT3	ANT2	ANT1	ANT0
Socket 1 WiFi+BT+Other (Type 1630, 2230, 3030, 2226)	N/A	Other Comm (when applicable)	WiFi3 (when applicable)	WiFi1	WiFi2+BT	N/A
Socket 2 WWAN+GNSS (Type 3042)	Vendor Specific	Vendor Specific	Vendor Specific	Vendor Specific	Vendor Specific	Vendor Specific
Type 1216	N/A	N/A	Vendor Specific	Vendor Specific	Vendor Specific	N/A

Note: Actual RF connector functions to be defined by vendor←→customer if not using the recommended allocations in this table.

The recommended WiFi antenna port assignment implies that the main WiFi antenna port (for example; WiFi 1x1) would use ANT2 and listed as WiFi1. When WiFi expands to a 2x2 configuration, it should share the antenna port with the BT using ANT1. This is listed as WiFi2+BT. In extended WiFi 3x3 solutions, the third antenna port used is ANT3 and this is listed as WiFi3. Other Comms should use ANT4 when more complex wireless Combo solutions are implemented

Figure 31 and Figure 32 show Socket 1 Type 2230 and 3030 RF connector assignment recommendations. Socket 2 Type 3042 RF connector assignment recommendations are vendor-specific.

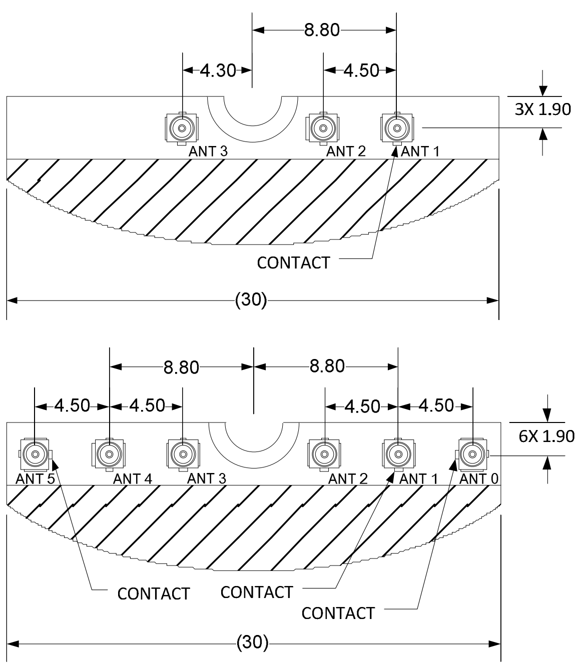


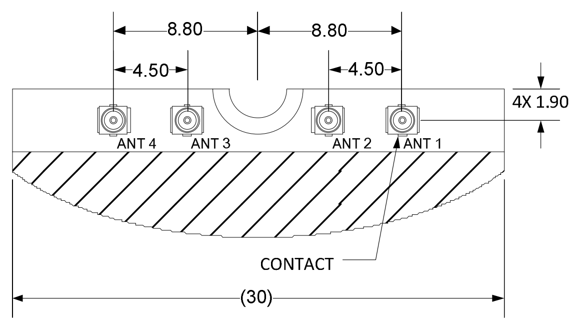


GENERAL TOLERANCE IS ±0.15

Antenna	Interface
1	WiFi/Blue Tooth
2	WiFi Main
3	WiFi Aux 1
4	Other Wireless

Figure 31. Socket 1 Type 2230 RF Connector Assignment Recommendation





GENERAL TOLERANCE IS ±0.15

Antenna	Interface
0	TBD
1	WiFi/Blue Tooth
2	WiFi Main
3	WiFi Aux 1
4	Other Wireless
5	TBD

Figure 32. Socket 1 Type 3030 RF Connector Assignment Recommendation

2.4. System Connector Specifications

The card interconnect is based on a 75 position Edge Card connector. The 75 position connector is intended to be keyed so as to distinguish between families of Host Interfaces and the various Sockets used in NB/very thin platforms and Tablet platforms. This specification document makes provision for the following three Socket families:

- Connectivity Socket 1
- WWAN/SSD/Other Socket 2
- SSD Drive Socket 3

In order to accommodate various product Z-Height limitations, there will be generic types of Edge Connectors in multiple Height variants designated below:

- M1.8 - Mid Line (1.80 Max Ht.) – For very low profile platforms
- H2.3 - Top Side – Single Sided (2.25mm Max Ht.) Connector
- H2.5 - Top Side – Single Sided (2.45mm Max Ht.) Connector
- H2.8 – Top Side – Dual Sided (2.75mm Max Ht.) Connector
- H3.2 – Top Side – Dual Sided (3.20mm Max Ht.) Connector
- H4.2 – Top Side – Dual Sided (4.20mm Max Ht.) Connector

Note: This list of connector options is not exclusive; other connector designs are allowable per market needs, however they must comply with mating interface mechanical and electrical requirements.

Table 10 lists the module types supported by the different connector types.

Table 10. Connector/Module Type Supported Matrix

		Component Height Descriptors							
	Description	**S1**	**S2**	**S3**	**D1**	**D2**	**D3**	**D4**	**D5**
M1.8	Mid-plane Connector	✓	✓	✓	✓*	✓*	✓*	✓	✓
H2.3	Single-Sided (2.25 Max Ht.) Connector	✓	✓	✓					
H2.5	Single-Sided (2.45 Max Ht.) Connector	✓	✓	✓					
H2.8	Double-Sided (2.75 Max Ht.) Connector	✓	✓	✓				✓	
H3.2	Double-Sided (3.2 Max Ht.) Connector	✓	✓	✓	✓	✓	✓	✓	
H4.2	Double-Sided (4.2 Max Ht.)	✓	✓	✓	✓	✓	✓	✓	✓

Note: *System clearance will have to be evaluated.

The Hx naming convention along with the mechanical Key letter enables easy recognition of the required connector through simple nomenclature; as shown in the following example:

M.2 Connector H2.3-E-Opt1

H2.3 designates Single-sided (2.25 Max Ht.),
-E designates Key E,
-Opt1 designates the minimum 25 insertion/extraction cycles (see the Durability line in Table 12).

This Hx descriptor also aligns with the coinciding Standoff descriptor described in the Section 2.5.

2.4.1. Connector Pin count

The connector has 75 positions. However, eight positions are used for each connector key so the pin count is 67 pins.

2.4.2. Contact Pitch

The contact pitch is 0.5 mm. The connector will have two rows of pins, top and bottom. The bottom row is staggered by 0.25 mm from the top row.

2.4.3. System Connector Parametric Specifications

Table 12, 13 and 14 specify the requirements for physical, environmental, and electrical performance for the M.2 connector.

Table 11. Connector Physical Requirements

Description	Requirement
Connector Housing	UL rated 94-V-0 Must be compatible with lead-free soldering process
Contact: Receptacle	Copper alloy with Gold Plating sufficient to meet all mechanical and environmental requirements
Contact Finish : Receptacle	Must be compatible with lead-free soldering process

Table 12. Connector Physical Requirements

Test Conditions	Specification
Durability	EIA-364-9; Option 1-25 cycles, Option 2-60 cycles. Upon completion of cycles the sample must meet all visual and electrical performance requirements.
Insertion Force	Insertion Force-20 N (2.04 KgF) maximum EIA-364-13, Method A
Shock	• 250 G (Ultra-book) and 285 G (Tablet) • At 2mSec half sine • On all six (6) axis
Vibration	EIA-364-1000 Test group 3, EIA-364-28
Operating Temperature	-40℃ to 80℃
Environmental Test Methodology	EIA-364-1000 Test Group 1, 2, 3, and 4
Useful Field Life	Three years

Table 13. Connector Physical Requirements

Description	Requirement
Low Level Contact Resistance	EIA-364-23 • 55 mΩ maximum (initial) per contact • 20 mΩ maximum change allowed
Insulation Resistance	EIA-364-21 • >5 x 108 Ω @ 500 V DC
Dielectric Withstanding Voltage	EIA-364-20 • >300 V AC (RMS) @ Sea Level
Current Rating	• 0.5 A/Power Contact (continuous) • The temperature rise above ambient shall not exceed 30°C. • The ambient condition is still air at 25°C. • EIA-364-70 Method 2
Voltage Rating	50 V AC per Contact

2.4.4. Additional Environmental Requirements

The connector must meet RoHS (no exceptions) and Low Halogen compliance.

2.4.5. Card Insertion

- Angles insertion is allowable and preferred; intent is to minimize the insertion/extraction force. The minimum of angle of insertion is 5°
- Minimum two step insertion is desirable; intent is to minimize the insertion/extraction force.

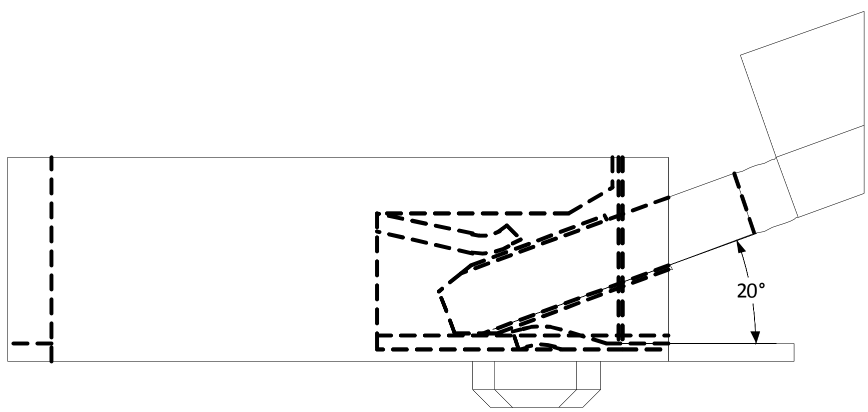
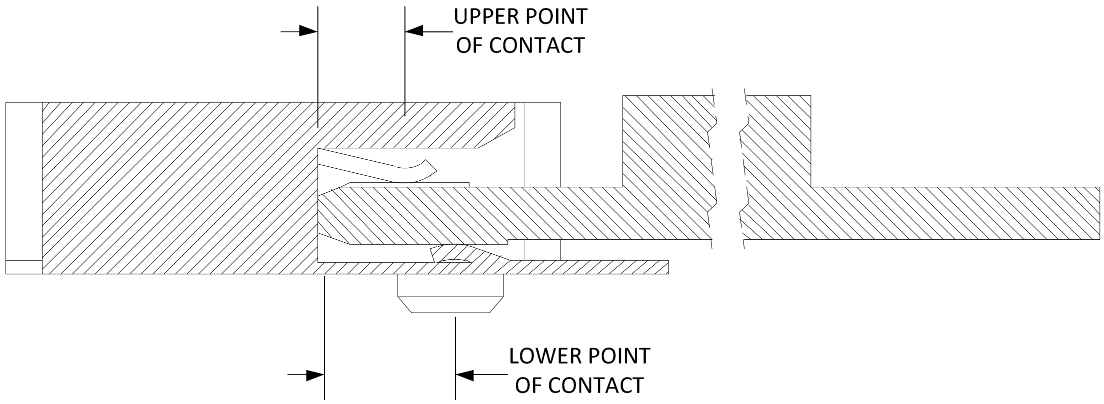


Figure 33. Angle of Insertion

2.4.6. Point of Contact Guideline

The signal integrity and mechanical requirements yield a starting point for the point of contact to module Gold Finger relationship. The range for the upper point of contact measured from the seating plane should be between 0.8 to 1.3 mm and the range for the lower point of contact should be between 0.9 to 2.2 mm. (see Figure 34, Point of Contact).

> **Note:** The angle of insertion is a key consideration for determining the point of contact; see Figure 33. Objective is to minimize insertion/removal forces while meeting signal integrity requirements.



Note: Connector design and contact shape are generic and infers no design intent beyond the dimensioned contact point.

Figure 34. Point of Contact

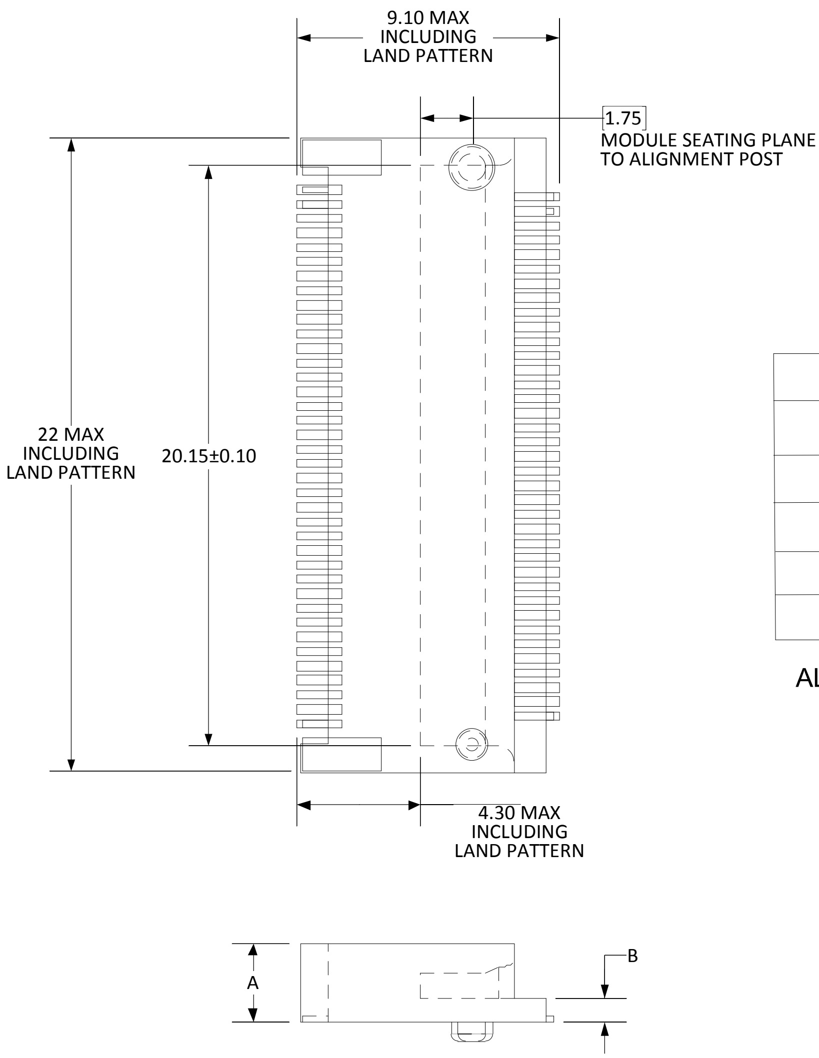
2.4.7. Top Side Connection

2.4.7.1. Top Side Connector Physical Dimensions

The top-side scheme has two connectors that share a common footprint but have a different stack-up requirement (see section 2.4.7.3 for more detail)

- Length—22 mm maximum including land pattern
- Width—9.1 mm maximum including land pattern

Figure 35 shows the top-side connector dimensions.



Height	A (MAX)	B (MAX)
H2.3	2.25	0.41
H2.5	2.45	0.61
H2.8	2.75	0.89
H3.2	3.20	1.54
H4.2	4.20	2.54

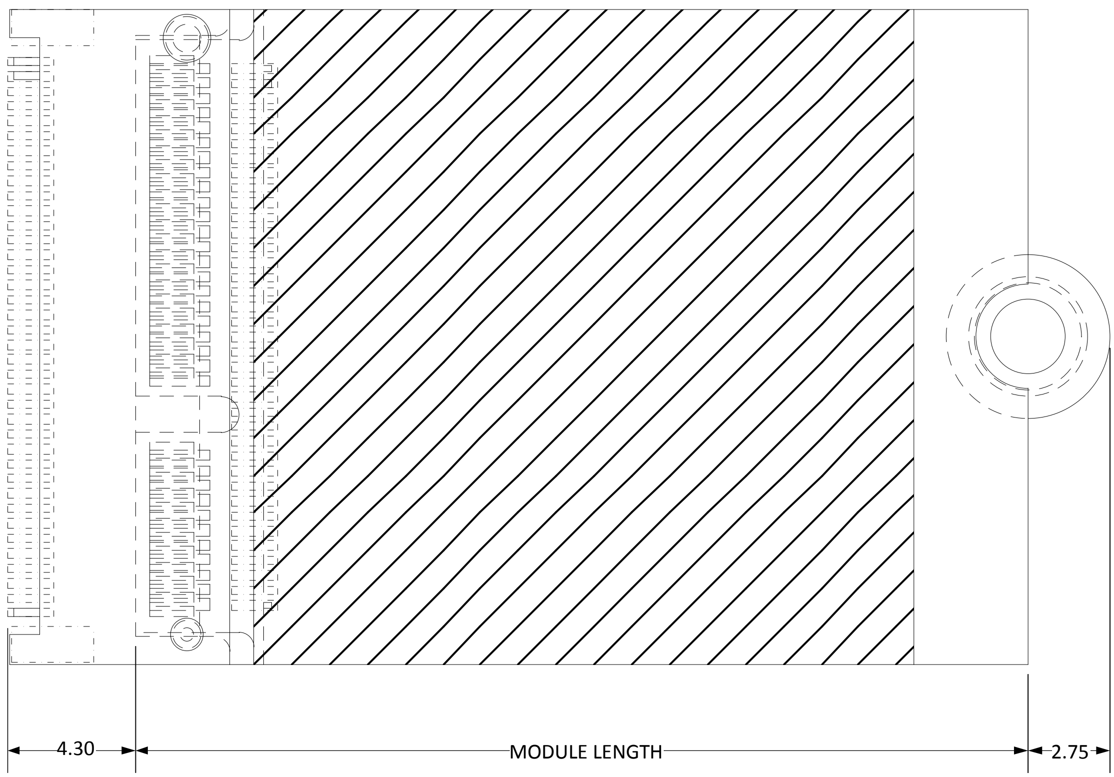
ALL DIMENSIONS mm

Figure 35. Top Side Connector Dimensions

2.4.7.2. Top Side Connection Total System Length

The maximum total solution is constrained to module length plus the following increases:

- The additional increase in length is 7.05 mm maximum for top-side connector to the module length (Figure 36).
  - The retention screw adds 2.75 mm maximum.
  - The maximum extension, including land pattern beyond the module leading edge is 4.3 mm.
- Module lengths are 30, 42, 60, 80, and 110 mm.



Note: The retention screw and stand-off are required for mechanical hold down and potential thermal path (see Section 2.5 for an example).

Figure 36. Top Mounting System Length

2.4.7.3. Top Side Connection Stack-up

2.4.7.3.1. Single Sided Module (Using H2.3 Connector)

Total solution above the main board varies based on the maximum component height on the module. Figure 37, Figure 38, and Figure 39 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The maximum RSS given is measured from the top of the main board to the top of the module.

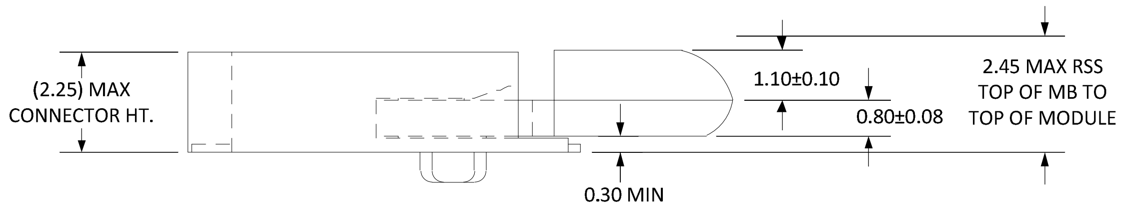


Figure 37. H2.3-S1 - Stack-up Top Mount Single-Sided Module for 1.2 Maximum Component Height

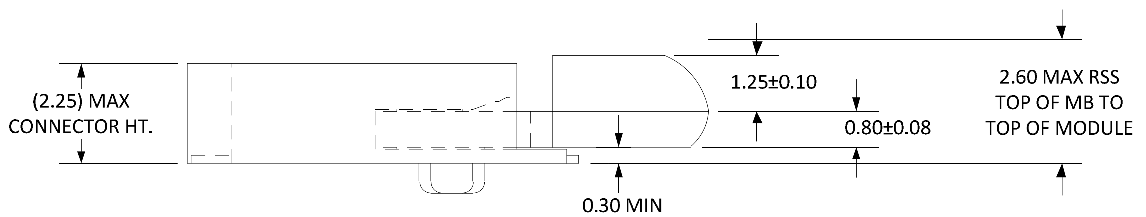


Figure 38. H2.3-S2 - Stack-up Top Mount Single Sided Module for 1.35 Maximum Component Height

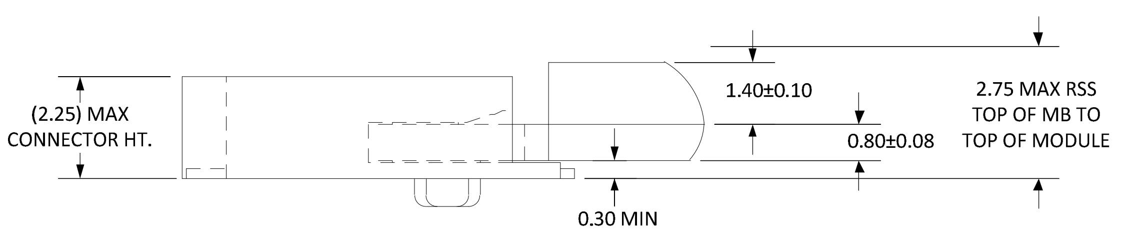


Figure 39. H2.3-S3 - Stack-up Top Mount Single Sided Module for 1.50 Maximum Component Height

2.4.7.3.2. Single Sided Module (Using H2.5 Connector)

Total solution above the main board varies based on the maximum component height on the module. Figure 40, Figure 41, and Figure 42 show the profiles based on three single-sided maximum component heights; 1.2, 1.35, and 1.5 mm. The maximum RSS given is measured from the top of the main board to the top of the module.

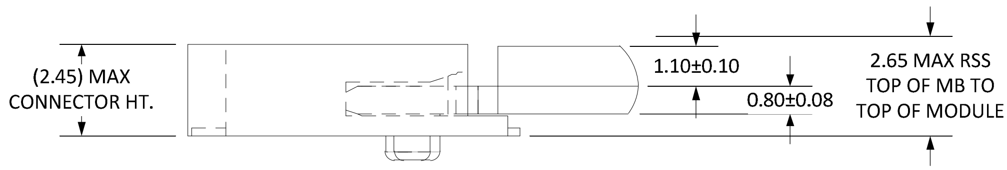


Figure 40. H2.5-S1 - Stack-up Top Mount Single-sided Module for 1.20 Maximum Top-side Component Height and with Higher Clearance above MB

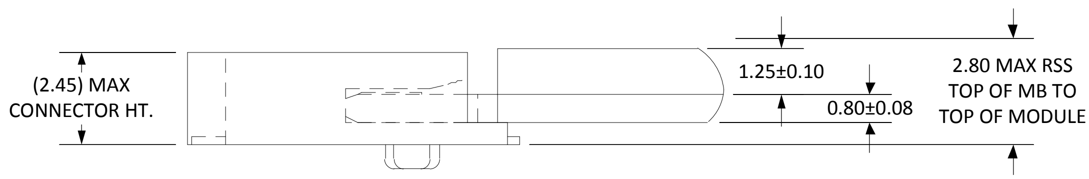


Figure 41. H2.5-S2 - Stack-up Top Mount Single-sided Module for 1.35 Maximum Top-side Component Height and with Higher Clearance above MB

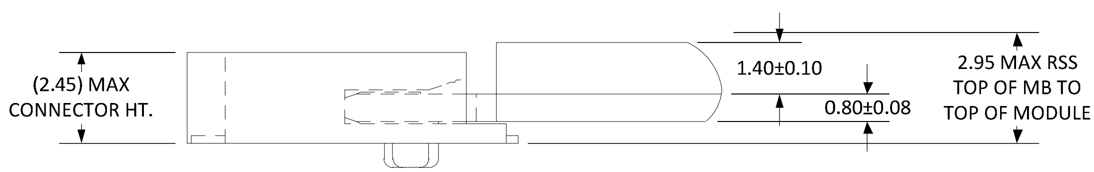


Figure 42. H2.5-S3 - Stack-up Top Mount Single-sided Module for 1.5 Maximum Top-side Component Height and with Higher Clearance above MB

2.4.7.3.3. Double Sided Module (Using H2.8, H3.2 and H4.2 Connector)

Total solution above the main board varies based on the maximum component height on the module. Figure 43, Figure 44, Figure 45, Figure 46, and Figure 47 show the profiles based on four top-side maximum component heights; 1.2, 1.35, and 1.5 mm. The bottom-side components maximum height is 1.50mm, 1.35 mm or 0.70 mm. The maximum RSS given is measured from the top of the main board to the top of the module.

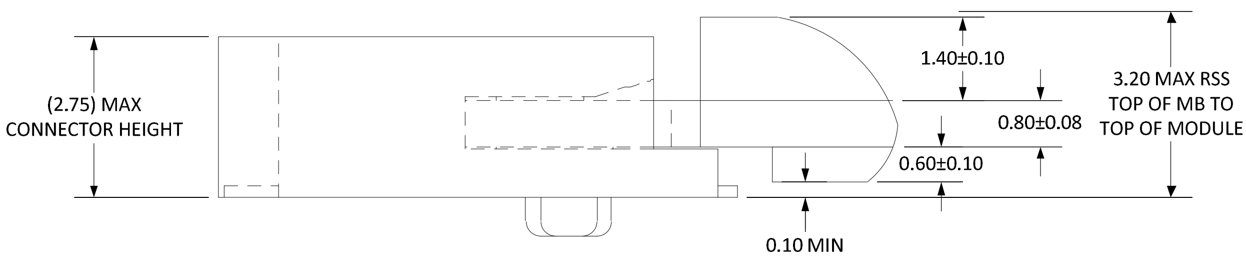


Figure 43. H2.8-D4 - Stack-up Top Mount Double-sided Module for 1.5 Maximum Top-side Component Height with 0.7 Maximum Bottom-side Component Height

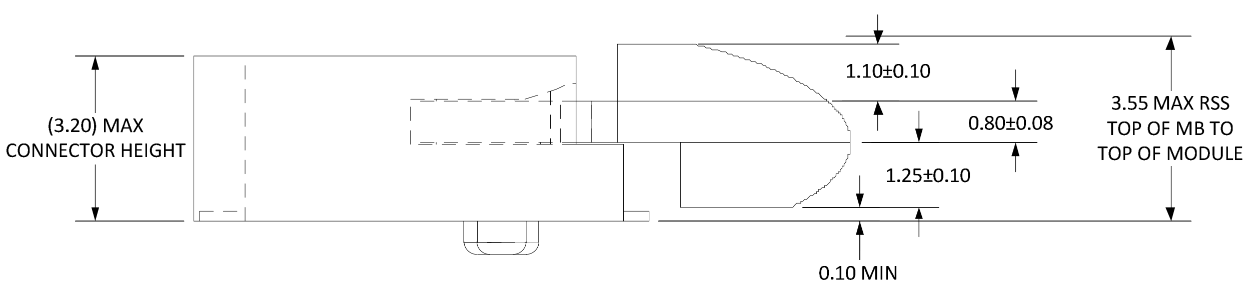


Figure 44. H3.2-D1 - Stack-up Top Mount Double-sided Module for 1.20 Maximum Top-side Component Height

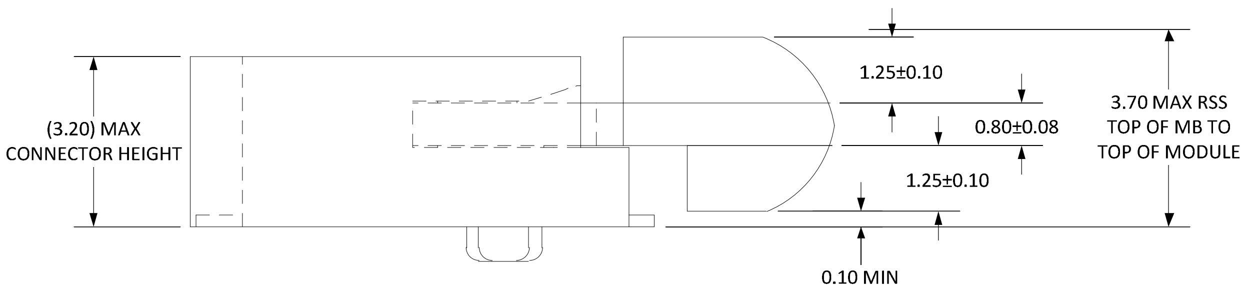


Figure 45. H3.2-D2 - Stack-up Top Mount Double-sided Module for 1.35 Maximum Top-side Component Height

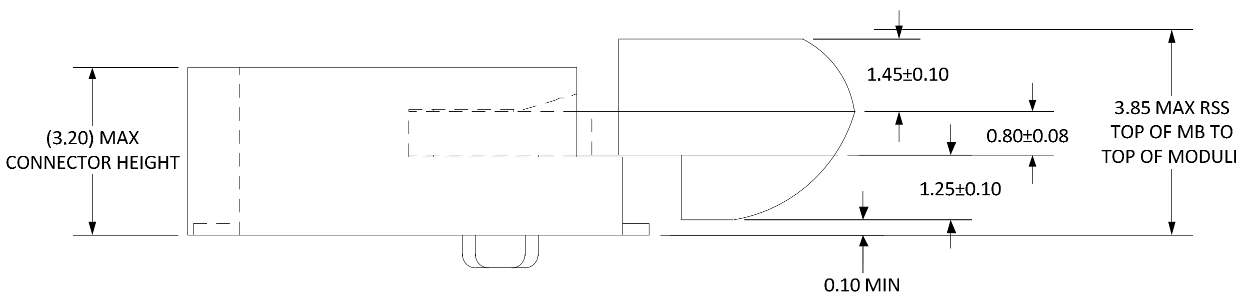


Figure 46. H3.2-D3 - Stack-up Top Mount Double-sided Module for 1.5 Maximum Top-side Component Height

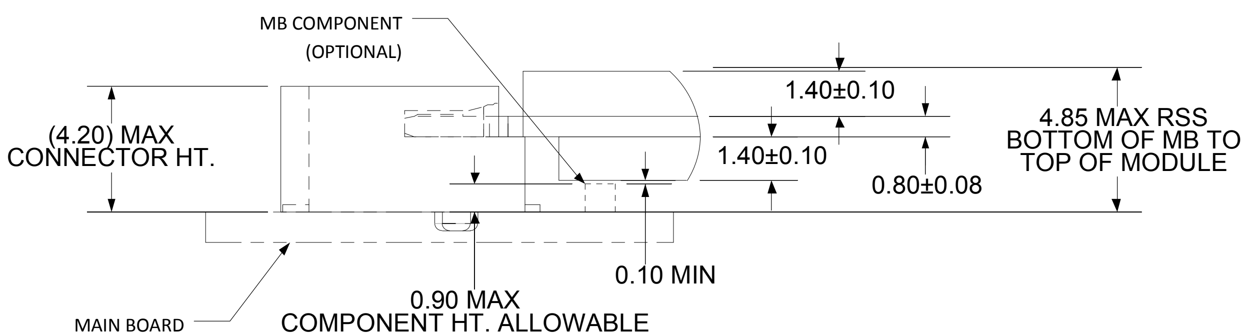
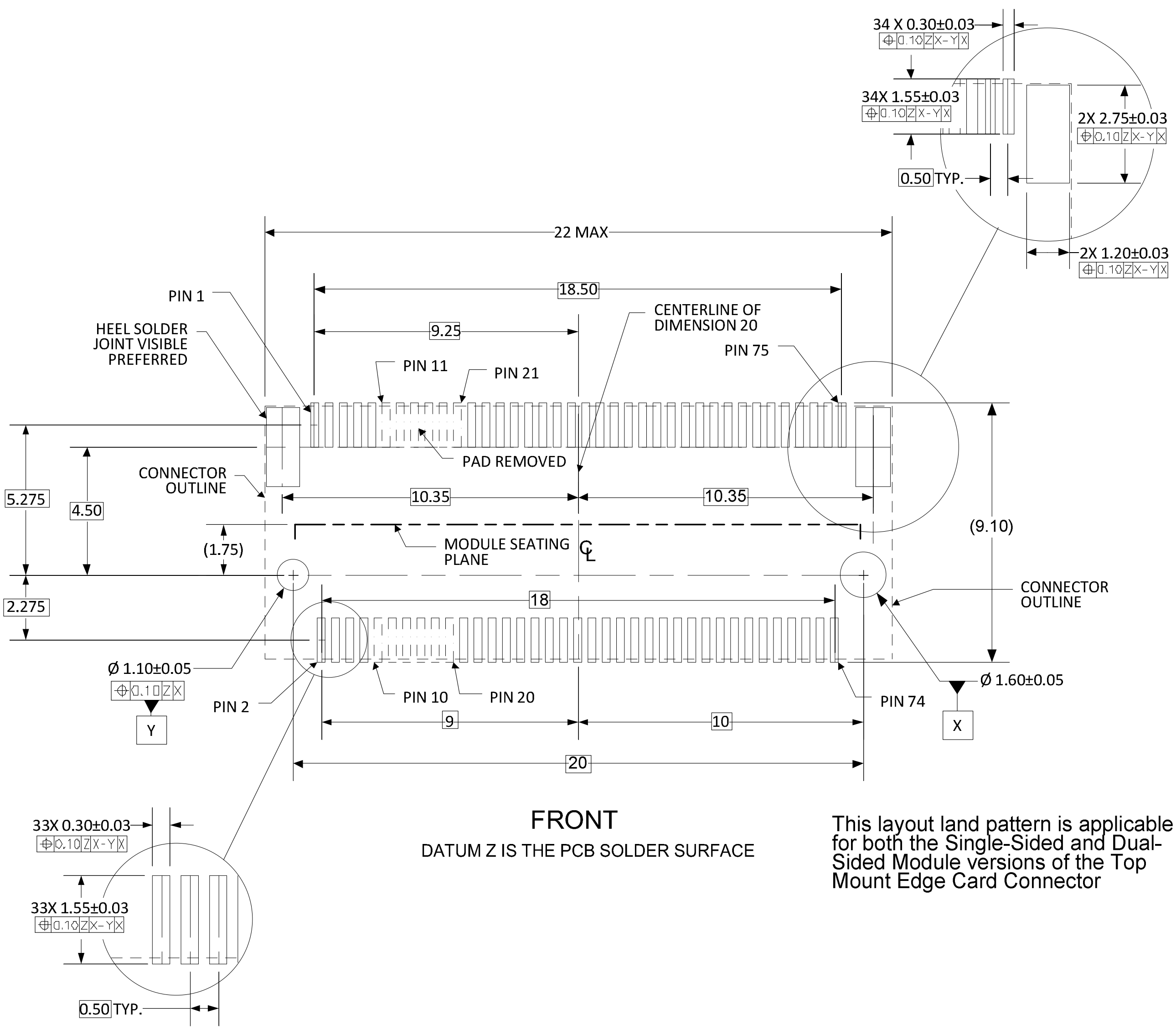


Figure 47. H4.2-D5 - Stack-up Top Mount Double-sided Module for 1.5 Maximum Top-side Component Height with 1.5 Maximum Bottom-side Component Height

2.4.7.4. Top Side Connector Layout Pattern

The layout footprint of the Top Mount Host I/F Edge Card Slot connector on the platform side Mother Board is shown in Figure 48. The land pattern includes all 75 pads although only up to 67 pads will be routed out while eight (8) pads will be redundant as they are located where the Mechanical Key is located. Figure 48 shows the eight redundant pads of Key B as faded.



This layout land pattern is applicable for both the Single-Sided and Dual-Sided Module versions of the Top Mount Edge Card Connector

Figure 48. Example of Top Mount MB Land Pattern Diagram Key B Shown

2.4.8. Mid Line Connection (Using M1.8 Connector)

2.4.8.1. Mid Line Connector Physical Dimensions

- Length-24 mm maximum including land pattern
- Width-9.5 mm maximum including land pattern

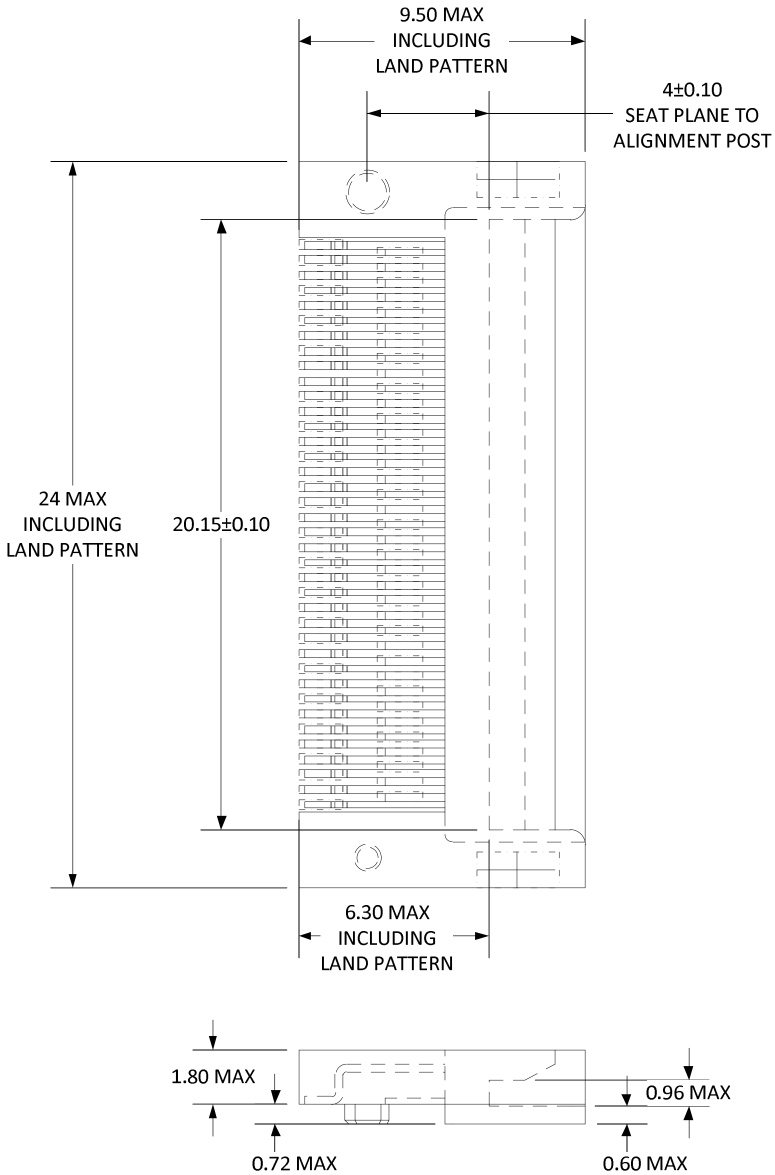


Figure 49. Mid-Line (In-line) Connector Dimensions

2.4.8.2. Mid Line Connection Total System Length

The maximum total solution is constrained to module length plus the following increases:

- The additional increase in length is 9.05 mm for top-side connector to the module length.
  - The retention screw adds 2.75 mm maximum.
  - The maximum extension, including land pattern beyond the module leading edge is 6.3 mm.
- Module lengths are 30, 42, 60, 80, and 110 mm.

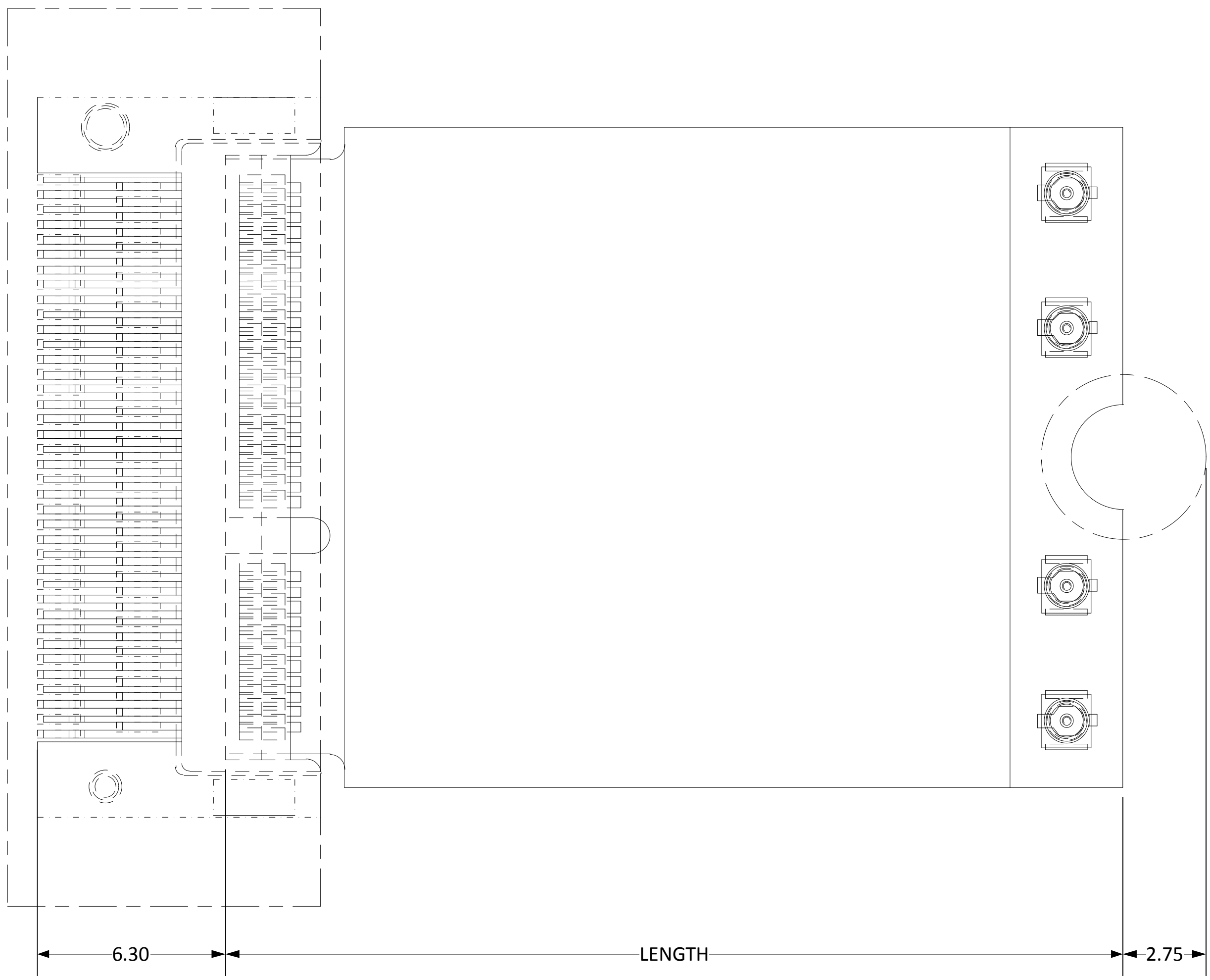


Figure 50. Mid-Line (In-Line) System Length

2.4.8.3. Mid Line Connection Stack-up

2.4.8.3.1. Single-sided Module

Total solution above the main board varies based on the maximum component height on the module. Figure 51, Figure 52, and Figure 53 show the profiles based on three single-sided maximum component heights; 1.2, 1.35 and 1.5 mm. The maximum RSS given is measured from the top of the main board to the top of the module. Also given is the maximum RSS as measured from the bottom of the main board to top of the module.

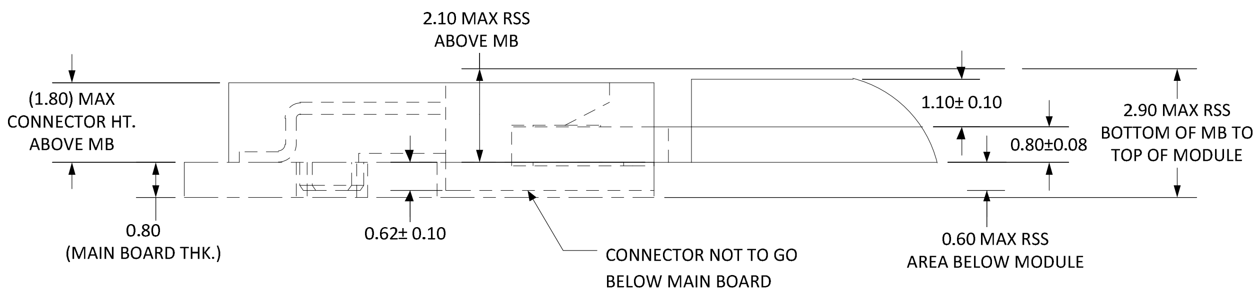


Figure 51. Stack-up Mid-Line (In-line) Single Sided Module for 1.2 Maximum Component Height

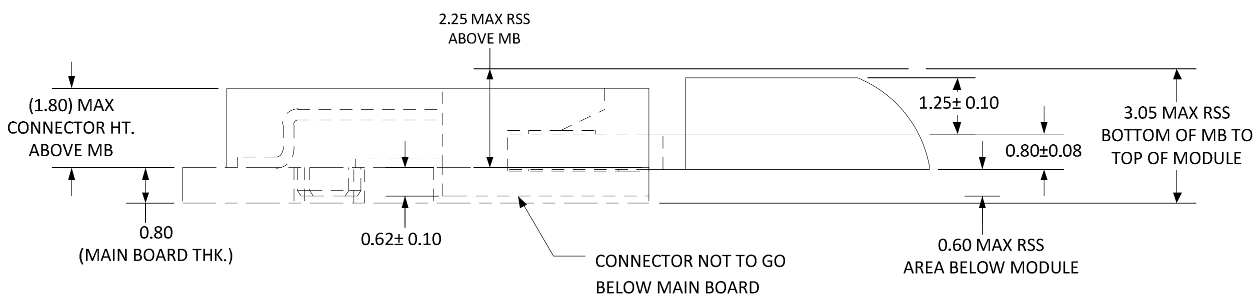


Figure 52. Stack-up Mid-Line (In-line) Single Sided Module for 1.35 Maximum Component Height

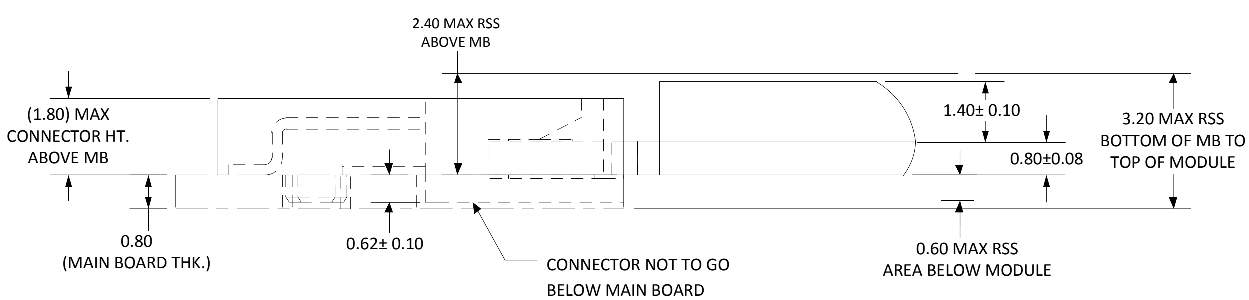


Figure 53. Stack-up Mid-Line (In-line) Single Sided Module for 1.5 Maximum Component Height

2.4.8.3.2. Double-sided Module

Total solution above the main board varies based on the maximum component height on the module. Figure 54 through Figure 57 show the profiles based on three top-side maximum component heights; 1.2, 1.35 and 1.5 mm. The bottom-side components maximum height is 1.5mm, 1.35 mm or 0.7mm. The maximum RSS given is measured from the top of the main board to the top of the module.

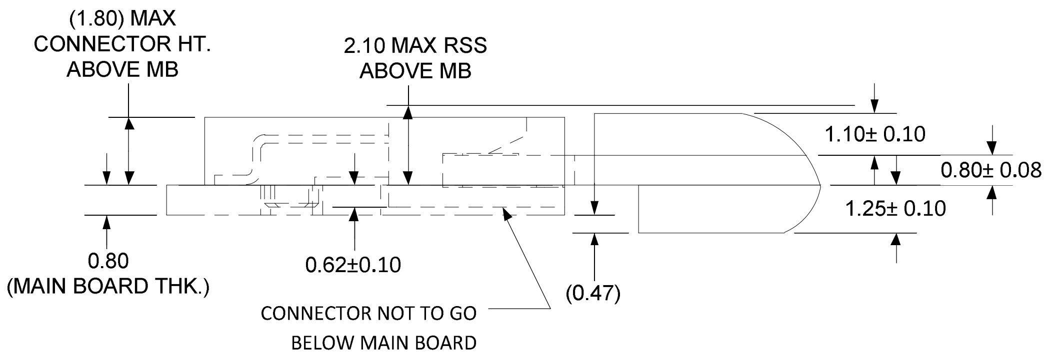


Figure 54. Stack-up Mid-Line (In-line) Double-sided (D1) Module for 1.2 Maximum Top-side Component Height

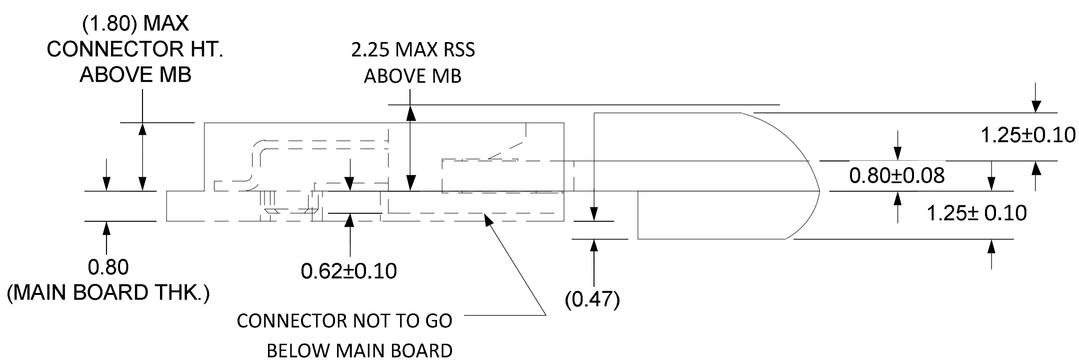


Figure 55. Stack-up Mid-Line (In-line) Double-sided (D2) Module for 1.35 Maximum Top-side Component Height

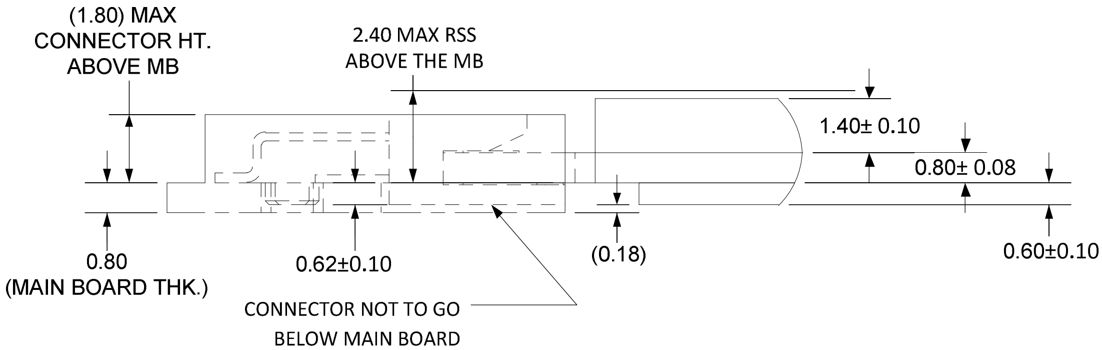


Figure 56. Stack-up Mid-Line (In-line) Double-sided (D4) Module for 1.5 Maximum Top-side Component Height

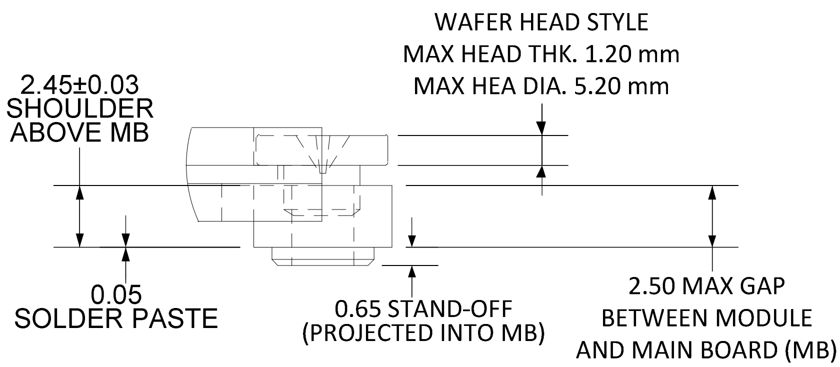


Figure 57. Stack-up Mid-Line (In-line) Double-sided (D5) Module for 1.5 Maximum Top-side and Bottom-side Component Height

2.4.8.4. Mid Line Connector Layout Pattern

The layout footprint of the Mid Mount Host I/F Edge Card Slot connector on the platform side Mother Board is shown in the following diagram. The land pattern includes all 75 pads although only up to 67 pads will be routed out while 8 pads will be redundant as they are located where the Mechanical Key is located. Figure 58 shows the eight redundant pads of Key B as faded.

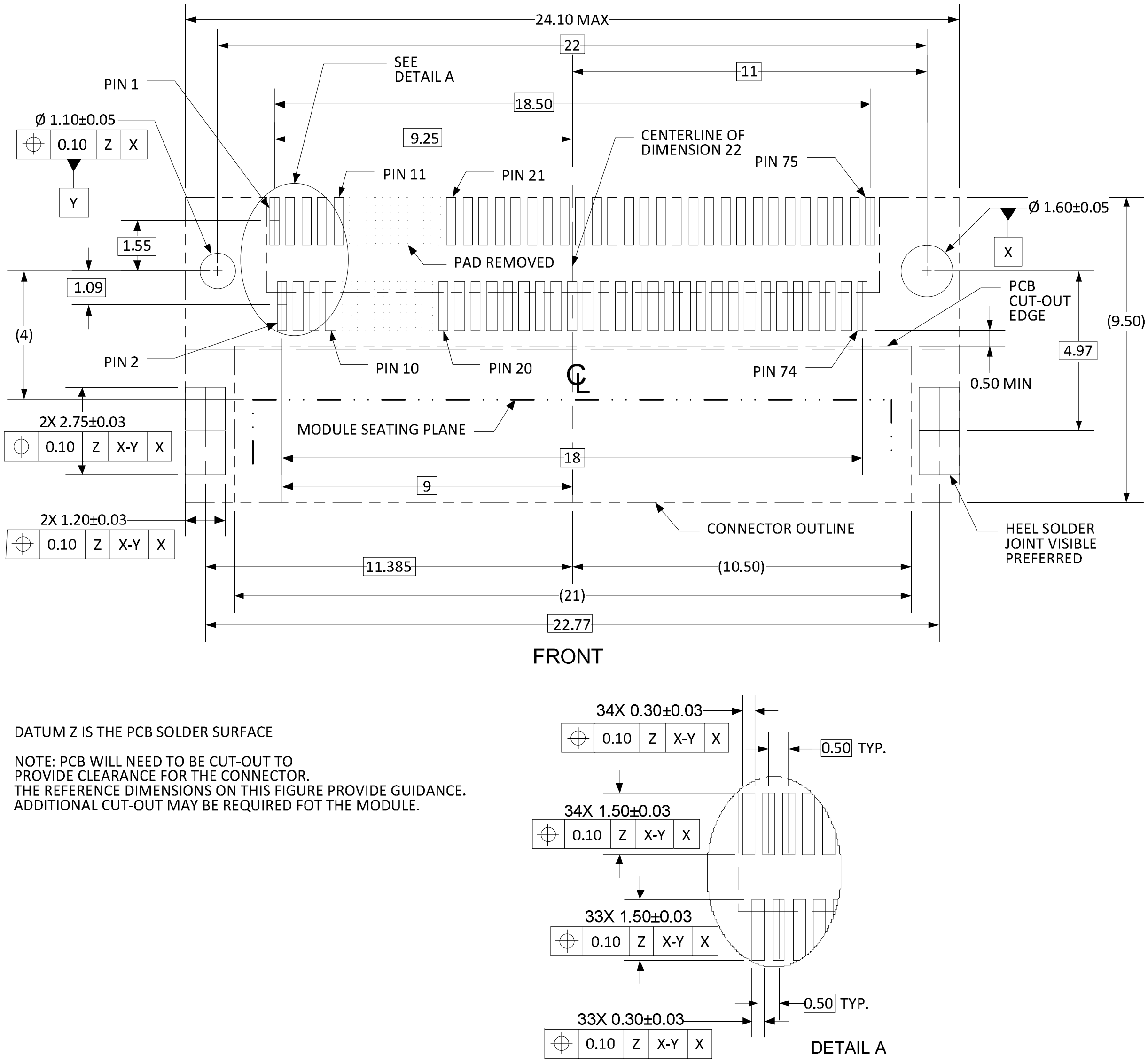


Figure 58. Example of Mid Line MB Land Pattern Diagram – Key B Shown

2.4.9. Connector Key Dimension

The width of the key is shown in Figure 59.

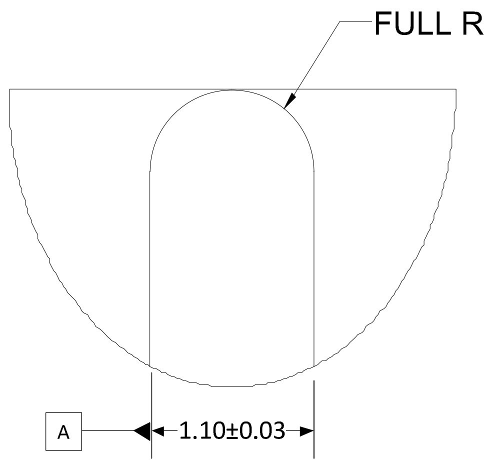


Figure 59. Connector Key

2.4.9.1. Host Connector Keying

The generic 75 position edge card connector on the mother board side will incorporate a mechanical keying scheme to enable mating with only a matching keyed module. This mechanical keying will also leave us four on the topside and four on the bottom side). The generic 75-pin connector is able to accommodate 12 different mechanical Keys that are designated by a *Letter*. Each such Keyed connector will have 67 usable pins available but at alternate pin locations within the generic 75 pin locations.

The Mechanical Key mechanism will enable the following:

- Each Socket on the MB with a different mechanical key location to signify a different pin-out and functionality of that particular socket
- To prevent wrongful insertion of an incompatible module into a wrong Socket connector on the MB. Including the potential module inversion. This is required for Safety reasons
- Multiple module key schemes that will enable insertion into more than one Socket

Mechanical keyed connectors that have their key locations within the first 49 pins (A, B, C, D, E, F, G, and H) can also accommodate the smaller 49 pin versions of the M.2 form factors like the Type 1630 board/module size. These smaller modules, which probably contain less content and require the reduced pin count, could still be plugged into the same MB keyed socket as their larger counterparts but enable module vendors a cost saving opportunity in the form of a smaller module for such simplistic solutions.

Figure 60 shows the relative location of the Mechanical Keys along the 75 positions. The Green and Blue marked areas are the locations of a reversed board showing that they do not coincide with the upright location of Keys. By assigning Key locations and making sure they are not interchangeable (upright or reversible), we end up with 12 distinct Keys.

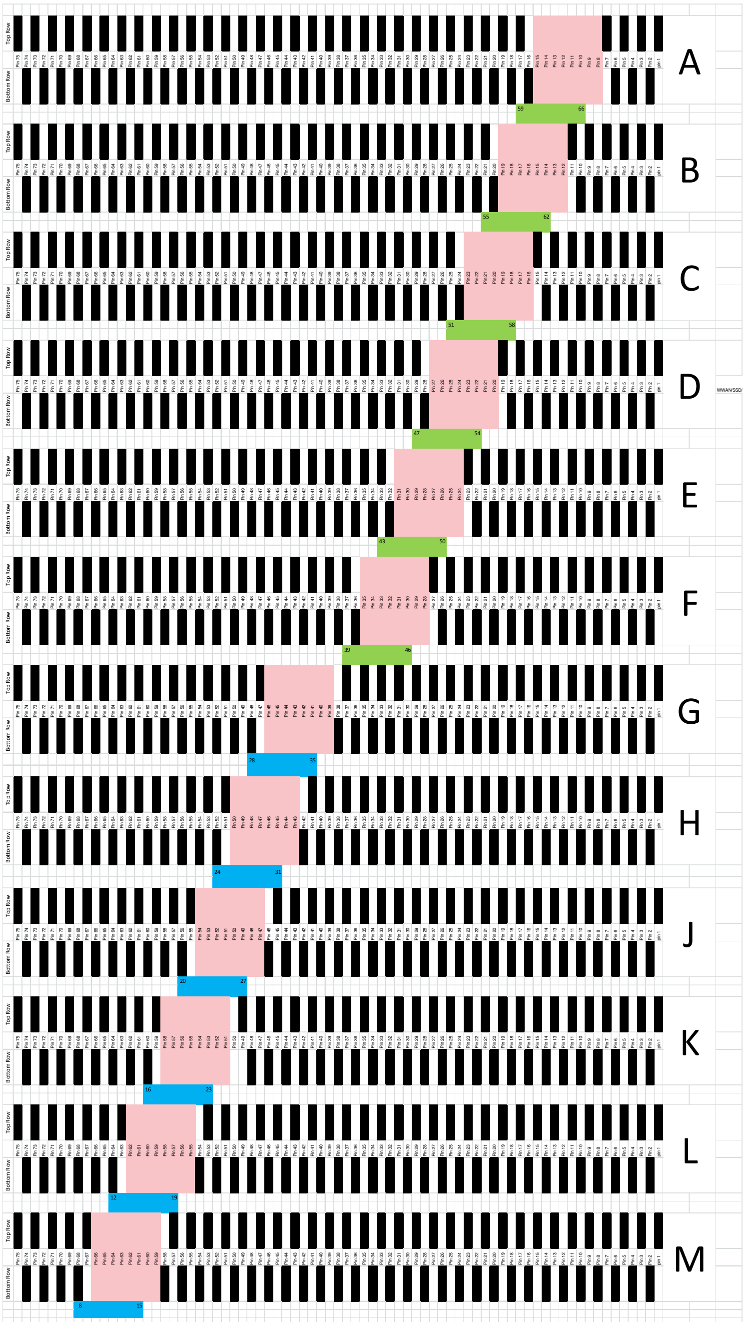


Figure 60. M.2 Connector Keying Diagram

This Connector Key/ Module Key system can enable some unique solutions in the form of a Dual Module key scheme. In such cases, a module with dual module keys would be able to plug into two different Keyed Connectors. But single module key modules intended for specific connector key would not be interchangeable. An example can be seen in Figure 61.

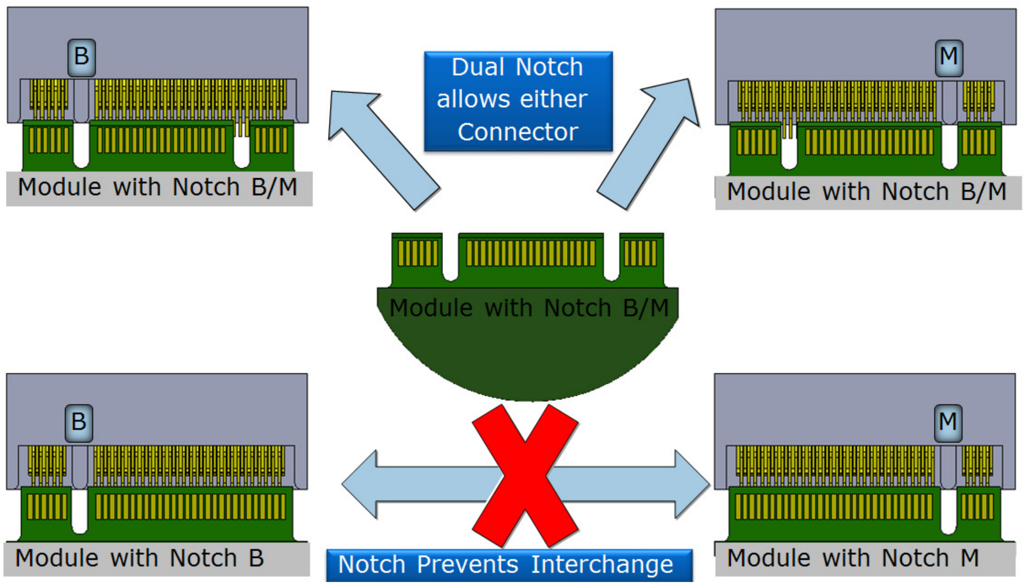


Figure 61. Dual Module key Scheme Example

Such a scheme could potentially be used to enable some modules to be plugged into two differently keyed connectors. For example, an SSD Cache module that incorporates a dual module key could be plugged into the WWAN/SSD/Other Socket 2 and also be plugged into a dedicated SSD Drive Socket 3. More details of such an example will be shown in the different Socket pin-out section. This scheme is not limited to this example and can be implemented in those cases where the pin outs supported are able to support this sort of scheme.

2.5. Module Stand-off

The modules will need a mechanical retention at the end of the board. The module specifies a 5.5 mm diameter. Keep-out zone at the end for attaching a screw. This section provides a guideline for using a M2 x 0.4 mm screw with a shoulder stand-off and a M3 x 0.5 mm screw. The guideline for the stand-off on the main board is recommending soldering down and assumed that the top-sided connectors are utilized. Alternatives are acceptable. The system will have to define the stand-off for utilizing the mid-plane connectors.

2.5.1. Recommended Main Board Hole

The recommended plated-hole sizes for the main board are:

- Drill size 4.3 mm
- Finish size 4.2 ±0.075 mm
- Pad size 6.5 mm

2.5.2. Electrical Ground Path

The module Stand-off and mounting screw also serve as part of the module Electrical Ground path. The Stand-off should be connected directly to the ground plane on the platform. So that when the module is mounted and the mounting screw is screwed on to hold the module in place, this will make the electrical ground connection from the module to the platform ground plane.

2.5.3. Thermal Ground Path

The stand-off must provide a Thermal Ground Path. The design requirements for thermal are a material with a minimum conductivity of 50 watts per meter Kelvin and surface area of 22 Sq mm.

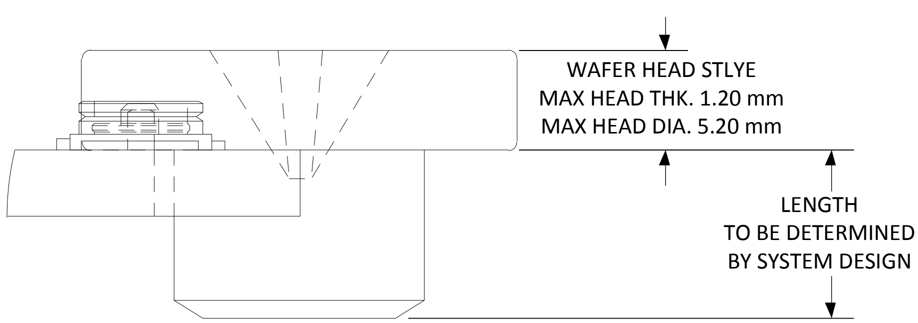


Figure 62. Mid-Line Module Mounting Interface

Top mount connectors will typically be complimented with a top mount stand-off. There are different types of stand-offs to coincide with the different height connectors as shown in Figure 63, through Figure 67.

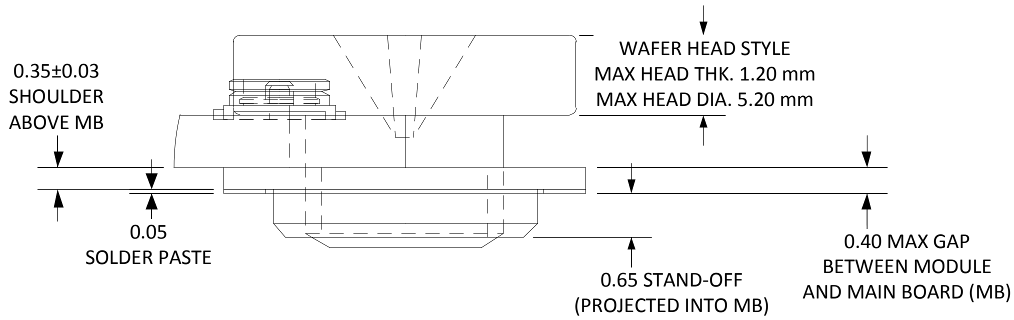


Figure 63. Single-sided Top Mount Solder Down Stand-off

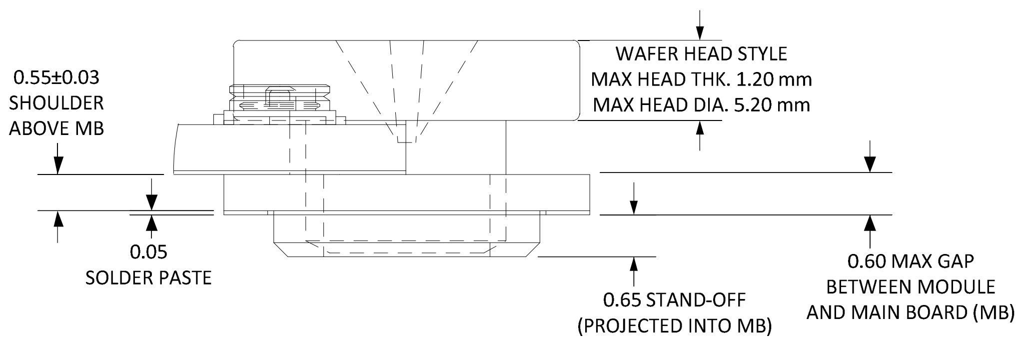


Figure 64. Elevated Single-sided Top Mount Solder Stand-Off

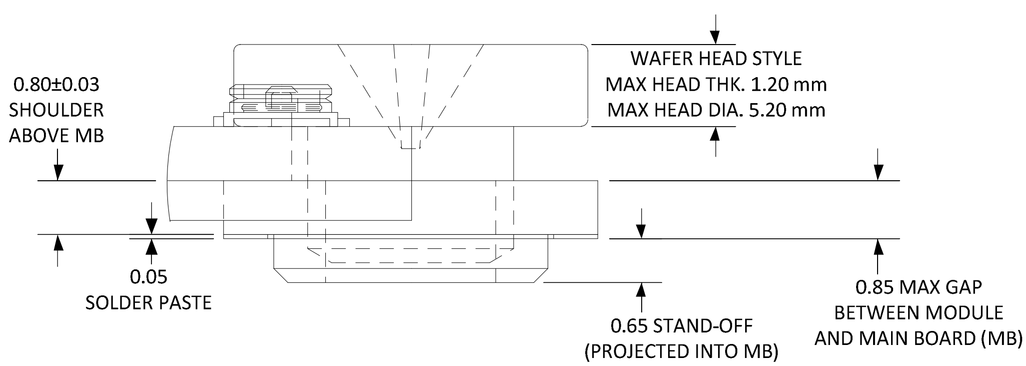


Figure 64

Figure 65. Low Profile Double-sided Top Mount Solder Down Stand-off

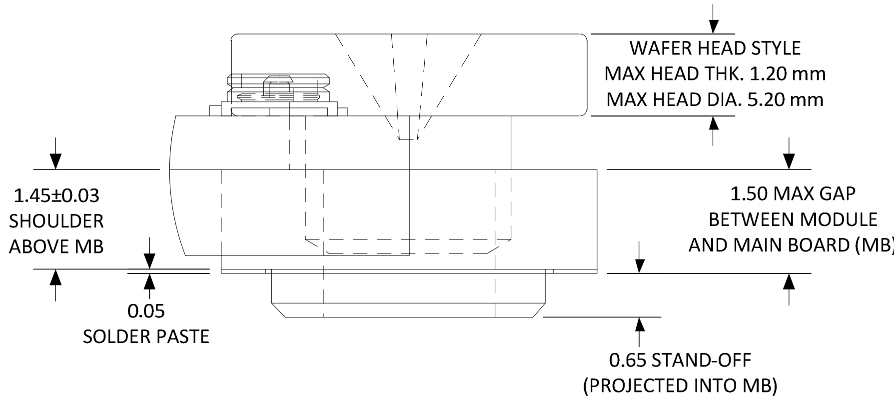


Figure 66. Double-sided Top Mount Solder Down Stand-off

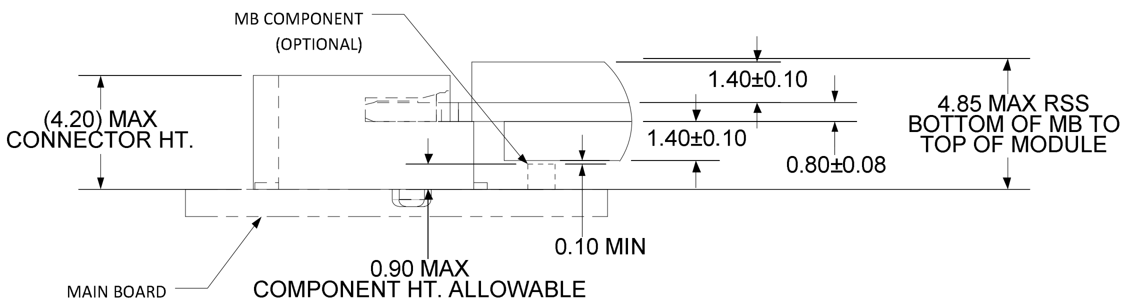


Figure 67. Elevated Double-sided Top Mount Solder Down Stand-off

2.5.4. Stand-Off Guidelines

Figure 68 and Figure 69 provide a guideline for stand-offs for top-sided connectors.

2.5.4.1. Stand-Off Guidelines Option 1

A flat stand-off is a board-level SMT component. This stand-off has a 3 x 0.5 thread. The height of the stand-off is determined by what connector is used (see Table 14).

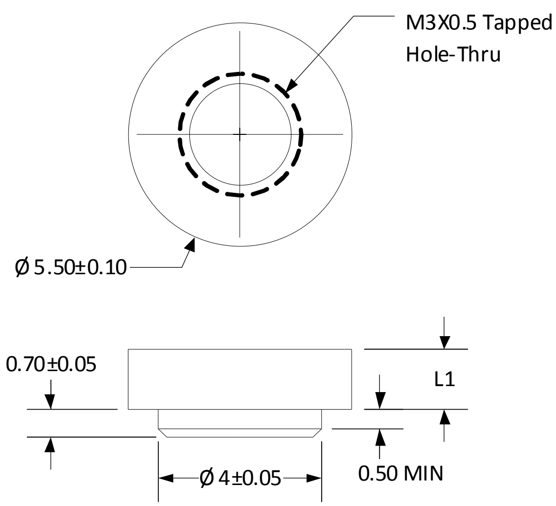


Figure 68. Flat Stand-Off

2.5.4.2. Stand-Off Guidelines Option 2

A shoulder stand-off is a board-level SMT component. This stand-off has a 2 x 0.4 thread. The height of the stand-off is determined by what connector is used (see Table 14).

> **Note:** For a single-side connector, the shoulder stand-off is not recommended due to the insertion being nearly horizontal. The shoulder could make insertion/removal of the module difficult due to clearing the cut-out.

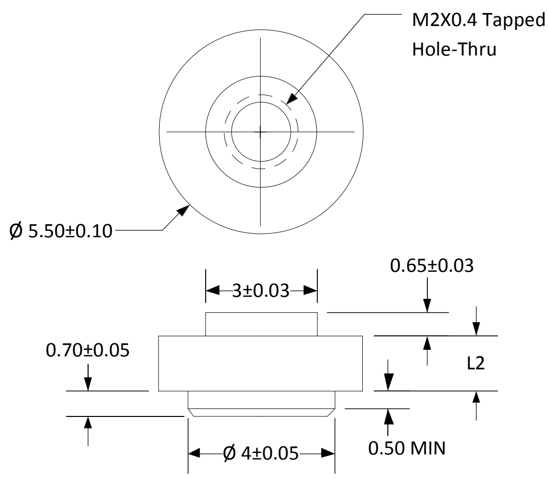


Figure 69. Shouldered Stand-Off

Table 14. Stand-Off Height Descriptor Table

Connector Height Descriptor	L1	L2
H2.3	0.35 ± 0.03	
H2.5	0.55 ± 0.03	
H2.8	0.80 ± 0.03	0.80 ± 0.03
H3.2	1.45 ± 0.03	1.45 ± 0.03
H4.2	2.45 ± 0.03	2.45 ± 0.03

Notes:

- Polymide patch required for vacuum pick-up
- Minimum thermal conductivity of 50 W/(mK) or greater
- Material = Steel
- Finish = Matte tin, 1.2 microns minimum average
- Tape and reel

2.5.5. Screw Selection Guideline

Screw selection consideration should be made to usage model. The tolerances of the connector, module and stand-off allow for a gap to exist between the seating plane and the contact, see Figure 70.

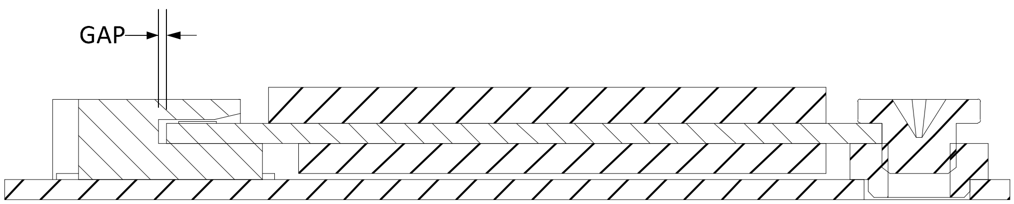


Figure 70. Screw Guidelines

2.5.5.1. Option 1, Wafer-Head Style M3 Screw

Option 1 provides the guidelines for a wafer-head style M3 screw (Figure 71). In using this screw type, the operator must be made aware that fully seating the module is required prior to securing the screw. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14

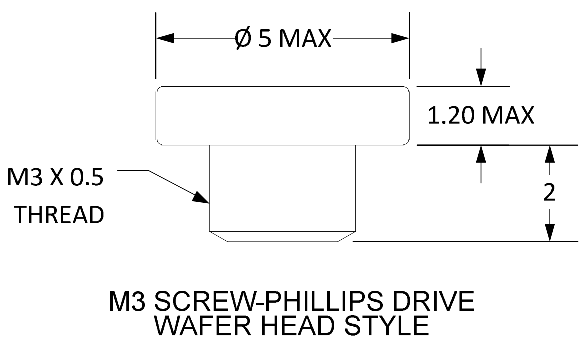


Figure 71. Wafer-Head Style M3 Screw

2.5.5.2. Option 2, M3 Screw with Tapered Shaft

Option 2 provides the guidelines for a wafer-head style M3 screw (shown in Figure 72) with a tapered shaft. In using this screw type, the taper shaft acts as a mechanical guide to minimize the gap. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14.

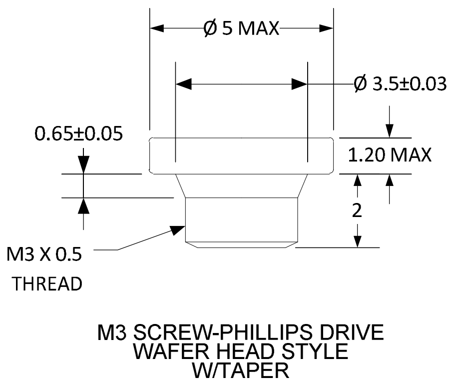


Figure 72. M3 Screw with Tapered Shaft

2.5.5.3. Option 3, Wafer-Head Style M2 Screw

Option 3 provides the guidelines for a wafer-head style M2 screw (shown in Figure 73). This screw is intended for use only with the stand-off. It is not recommended to be used alone as the cut-out size provides a strong potential of not seating properly. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14

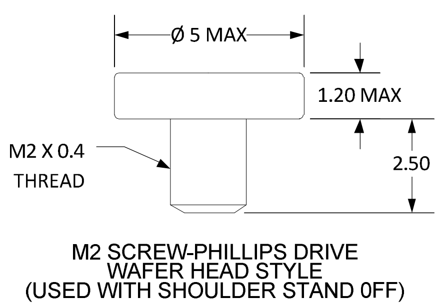


Figure 73. Wafer-Head Style M2 Screw

2.5.5.4. Option 4, Flat-Head Style M3 Screw

Option 4 provides the guidelines for a flat-head style M3 screw (shown in Figure 74). In using this screw type the taper shaft acts as a mechanical guide to minimize the gap. Caution should be taken not to over torque the screw as it could damage the barrel on the plated cut-out. This screw does offer a low cost standard option for providing a mention to mechanical control the gap. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14.

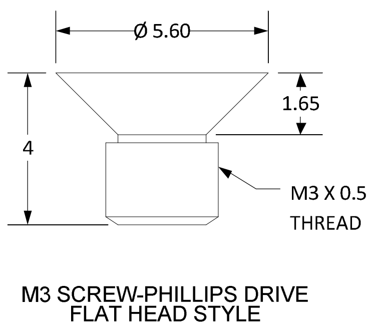


Figure 74. Flat-Head Style M3 Screw

2.6. Thermal Guidelines for the M.2

The following thermal guidelines are intended to provide guidance to system designers and module designers using M.2 modules. The thermal dissipation capability of any component or module is a function of the surrounding thermal environment. This guideline gives direction on assessing power dissipation capability for generic modules in certain classes of systems when no special thermal enhancement is applied to the module. It also gives module placement advice, although this advice should be considered informative rather than normative.

No specific maximum dissipation limits are given, as these limits are strongly system, use case, and system skin temperature dependent.

2.6.1. Objective

Establish dissipation response of modules; "Thermal Design Power"

- By *generic* system environment (various categories defined; many assumptions)
- By card component type (generic packages, power maps defined)
- In presence of steady state dissipation in the rest of the system (use cases)

Based on limiting factors

- *Skin* (exterior surface of casing) or display temperature limits,
  OR
- Die maximum temperature, if this limit is reached first

2.6.2. Introduction

This section addresses some of the key concepts for module thermal management. Because the connector forms a primary heat path to the main system board, thermal conditions on this board will provide a "background" temperature to an unpowered module. Powering the module increases its temperature as well as that of the surroundings: not only the board on which the connector is mounted but also nearby elements such as system casing, display if present, batteries, and keyboard.

2.6.2.1. Thermal Design Power Definition

The definition of Thermal Design Power (TDP) is worst case average dissipation over a time duration. The time scales for fan systems are in the one minute range. The time scales for fanless systems are in the three minute range. Die thermal time constants are on the order of milliseconds, while power transients occur over even shorter time durations. However, since the thermal mass of the surrounding system is significant, the longer response time is of interest.

Note that this longer time scale dissipation is quite different from the maximum power, or even "normal" power drawn by the module, as these tend to occur on a duty cycle with much shorter time scales than the Thermal Design Power. In addition, any power sent out through an antenna would subtract from the electrical power. The thermal design power is therefore always less than the maximum electrical power.

2.6.2.2. Skin Temperature Definition

For compact, portable systems, most of all the system's exterior surfaces ("casing" or "skin") may be touched by the user. There are safety limits that apply to such surfaces, but the user's perception of "hot" is far lower than these safety limits. The perception is highly subjective and a matter of individual preference. Therefore, it is important for the system criteria to include a target temperature for various areas of the outer surface, and the conditions under which these should be met (ambient temperature, system activity, system orientation, area of system, size of hot spot, and so on). Some examples are given in this document, but these are intended only as examples and are not intended to cover the complete range of all possibilities. Careful consideration of the intended user and environment is imperative.

Note that although the system's exterior housing is often called "skin," this refers only to the casing material and not to the human skin that may be touching it. In fact, the act of touching the casing may change its temperature. The ***perception*** of temperature is less a matter of actual temperature than a question of the heat rate into the sensors embedded in human skin. This phenomenon is common in real life; for example, the perception of "hot" by a young child is very different from the perception by calloused or older hands. The perception aspect of the surface temperature leads to a variety of limit definitions.

2.6.2.3. Unpowered M.2 Module Temperature

The "background" or unpowered module temperature is a function of motherboard "source" power, system environments, and other dissipation distributed around the system. This "adiabatic" or unpowered temperature is the **starting point for thermal ramp** as module switches from off or idle (~0 W) to powered. Skin temperatures in the vicinity of the module should be below the desired limits when the module is in this state.

Other characteristics of the unpowered module temperature are that it is nearly linear with **system power**; it is *specific to the individual system* (motherboard heat distribution, proximity of modules to other heat sources, cooling parameters, etc.); and the module's own dissipation also raises temperatures of neighboring modules, motherboard, and system skin. These surrounding temperature increases are also roughly linear with **module power**, and vary with module characteristics (size, heat distribution, heat paths to surroundings) and are also specific to individual system design parameters. Therefore, these characteristics should be quantified for each system design. By extension, the results given in this document are meant to provide only an example of the approach to determining the dissipation response of modules.

2.6.2.4. System Skin Temperature—Fan-based System

In a system that includes a fan, major heat sources are cooled by a thermal solution if needed and a fan. The air flow path is determined by vent placement, fan speed, obstructions, and so on. The cooling strategy should seek to maximize air flow for a given fan speed by reducing the pressure drop though the air path. As a general rule, sources of pressure drop that do not also accomplish a cooling task should be avoided as much as possible.

As skin temperature is a local heat density effect, it is important to flush air through the gap between skin and the module. This will not completely prevent the module heating the skin, but allows more of the module heat to be exhausted from the system without having to pass through the casing. The module dissipation limit depends on air speed, but the air speed depends on the gap size, vent placement, fan speed, and other parameters in the flow path both upstream and downstream.

Another approach to reducing skin temperature over modules is to include a long, narrow vent between high heat areas and the module. The vent can act as a thermal break for the module, but it will reduce the area of outer casing available for cooling the high heat components.

In some systems, the fan flow rate is severely restricted by the proximity of the system casing or other elements. The fan's inlet side is obstructed by the resulting narrow gap, and this may alter the fan's characteristic curve from published data. Therefore, care should be taken to evaluate the true fan flow rate as installed in the system. In such systems, the low fan flow will exhaust proportionately less heat, leaving the remainder to pass through the casing as for fanless systems, below.

2.6.3. System Skin Temperature—Fanless System

All heat dissipated inside the system, by any heat source, must pass *through* the casing (which has minimal temperature gradient through the material thickness, even if resin based) and dissipate off the exterior surface to the environment by radiation and natural convection. Thus, the surface temperature is *total system power* and *surface area dependent.* High emissivity of the outer surface in the long-infrared range, for example by paint, anodize, or resin coating, is helpful for decreasing surface temperature. A metal casing produces more uniform skin temperature than resins, but has more restrictive temperature limits. In most cases the heat spreading ability of the metal is beneficial to system cooling despite the lower temperature limits.

2.6.4. Examples

Examples of dissipation (TDP) response of modules in systems can be found in section 6.5, Thermal Guideline Annex. The general trend is that the skin temperature of a system is dominated by the system's use case and layout—changes in the module TDP locally perturbs the skin temperature. Higher levels of fan ventilation reduce the sensitivity of local skin temperature to module TDP.

3

3. Electrical Specifications

This chapter covers the electrical specifications for the PCI Express M.2 family of modules.

3.1. Connectivity Socket 1 System Interface Signals

Table 15 applies to both Socket 1-SD and Socket 1-DP pin-out versions.

Table 15. Socket 1 System Interface Signals and Voltage Table

Signal Group	Signal	Direction	Description	Voltage
Power	+3.3V (4 pins)	Input	3.3V source	3.3V
	GND		Return current path	0V
WiFi-SDIO	SDIO_CLK	Input	SDIO 3.0 Clock, 1.8V for SDR25 & DDR50 mode	1.8V
	SDIO_CMD	I/O	SDIO Command Interface, 1.8V for SDR25 and DDR50 mode	1.8V
	SDIO_DATA[0:3]	I/O	Four lines for SDIO data exchange, 1.8V for SDR25 & DDR50 mode	1.8V
	SDIO_ WAKE#	Output	SDIO sideband Wake. Note in band SDIO wake is not used for non-active modes, Active Low. Require pull up on the host side (recommended 15K to 100K)	1.8V
	SDIO_ RESET#	Input	SDIO sideband GPIO pin to enable/disable (reset) the WiFi function. Platform firmware is required to assert/de-assert this pin on every boot (warm and cold). The WiFi device may use 0.5 to 1 mW in reset, Active Low	1.8V

Signal Group	Signal	Direction	Description	Voltage
UART	UART_RXD	Output	UART Receive Data connected to TXD on the platform.	1.8V
	UART_TXD	Input	UART Transmit Data connected to RXD on the platform.	1.8V
	UART RTS	Input	UART Ready To Send connected to CTS on the platform.	1.8V
	UART CTS	Output	UART Clear To Send connected to RTD on the platform.	1.8V
	UART_WAKE#	Output	Bluetooth sideband Wake. Open Drain, Active Low. Require pull up on the host side (recommended 15K to 100K)	3.3V
PCM(I2S)	PCM_CLK / I^{2}S SCK	I/O	PCM Clock/ I^{2}S Continuous Serial Clock (SCK)	1.8V
	PCM_SYNC/ I^{2}S WS	I/O	PCM Synchronous data sync/ I^{2}S Word Select	1.8V
	PCM_IN/ I^{2}S SD_IN	Input	PCM Synchronous data input/ I^{2}S Serial Data IN	1.8V
	PCM_OUT/ I^{2}S SD_OUT	Output	PCM Synchronous data output/ I^{2}S Serial Data OUT	1.8V
PCIe (up to 2 instances)	PERp0, PERn0/ PETp0, PETn0	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLKP0/ REFCLKN0	Input	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST0#	Input	PE-Reset is a functional reset to the Add-In card as defined by the PCIe Mini Card CEM specification	3.3V
	CLKREQ0#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates.	3.3V
	PEWAKE#/ OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3V
USB	USB D+, USB D-	I/O	USB Data ± Differential serial data interface compliant to the *USB 2.0 Specification*	
I2C	ALERT#	Output	IRQ line to host processor; Active Low	3.3V
	I2C CLK	Input	I2C clock input from host	3.3V
	I2C DATA	I/O	I2C data	3.3V
Display Port	DP_HPD	Input or Output	Hot Plug Detect. Direction is determined by MLDIR	3.3V

Signal Group	Signal	Direction	Description	Voltage
	DP_MLDIR	I/O	Display Port data interface direction	0V/ 3.3V / NC
	DP_AUXp/DP_AUXn	I/O	Auxiliary Channel; Bidirectional half-duplex AUX channel, DisplayPort v1.2, AUX channel 1Mbit/s Signal direction dictated by MLDIR	
	DP_ML0p/DP_ML0n, DP_ML1p/DP_ML1n, DP_ML2p/DP_ML2n, DP_ML3p/DP_ML3n,	Input or Output	Up to 4 Lane; Effective data rate 1.296, 2.16 or 4.32 Gbit/s per lane; DisplayPort main link data interface: four unidirectional differential pairs, signal direction dictated by MLDIR	
Communication Specific Signals	SUSCLK	Input	Suspend Clock is a 32.768 kHz clock supply input that is provided by platform to enable the add-in card to enter reduce power consumption modes. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. Accuracy will be up to 200ppm.	3.3V
	W_DISABLE1# W_DISABLE2#	Input	Active low, debounced signal when applied by the system it will disable radio operation on the add-in cards that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3V
	LED_1# LED_2#	Output	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. These LED devices should be tied to +3.3V through a current limiting resistor. Current should be limited to 9mA when LED is On.	3.3V
	COEX[1..3]	I/O	Coexistence between WiFi+BT and WWAN on Socket 2	1.8V

3.1.1. Supplemental NFC Signals

The NFC solution can be complimented with the additional signals listed in Table 16 when a SIM device is used as the Secured Element.

Table 16. NFC Supplemental Signals and Voltage Table

Interface	Signal Name	I/O	Function	Voltage
NFC-UIM	UICC PWR IN/GPIO1	Input	UICC power out from BB PMU	Per ISO 7816 Specification
	UICC PWR OUT	Output	NFC PMU power to the UICC	
	SWP	I/O	UICC Secure element	

Note: Pins are not specifically allocated in the pinouts. They would need to be BTO between OEM and vendor and make use of available Reserved pins.

3.1.2. Power Sources and Grounds

PCI Express M.2 Socket 1 utilizes a single 3.3 V power sources. The voltage source, +3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ground (GND) pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

3.1.3. PCI Express Interface

The PCI Express interface supports a x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the *PCI Express Base Specification* for more details on the functional requirements for the PCI Express interface signals.

IMPLENTATION NOTE: Lane Polarity

By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) shall be connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the PCI Express M.2 Card add-in card. Similarly by default, the PERp0 and PERn0 pins (the receiver differential pair of the connector) shall be connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the PCI Express M.2 Card add-in card

However, the **p** and **n** connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI Express receivers incorporate automatic Lane polarity inversion as art of the Link initialization and training and will correct the polarity independently on each Lane. Refer to section 4.2.4 of the PCI Express Base Specification for more information on Link initialization and training.

IMPLENTATION NOTE: Link Power Management

PCI Express M.2 add-in cards that implement PCI Express-based applications are required by the PCI Express Base Specification to implement Link power management states, including support for the L0s and L1 (in addition to the primary L0 and L3 states). For PCI Express M.2 Card implementations, Active State PM for both L0s and L1 states shall also be enabled by default. Refer to Section 5.4 of the PCI Express Base Specification for more information regarding Active State PM.

Socket 1 pinout has provision for an additional PCI Express lane indicated by the suffix 1 to the signal names. These additional PETx1 and PERx1 signal sets can serve as the second Lane to the original PCI Express interface, or alternatively, they can be complimented with a second set of REFCLKx1 and a set of Auxiliary Signals on the adjacent Reserved pins to form a complete second PCI Express x1 interface.

3.1.4. PCI Express Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as PCI Express M.2 Card. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3V. The use of the +3.3V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express M.2 Card add-in card and system connectors support the auxiliary signals that are described in the following sections.

3.1.4.1. Reference Clock

The REFCLK+/REFCLK- signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Availability of the reference clock at the card interface may be gated by the CLKREQ# signal as described in section 3.1.4.2. When the reference clock is not available, it will be in the *parked* state. A parked state is when the clock is not being driven by a clock driver and both REFCLK+ and REFCLK- are pulled to ground by the ground termination resistors. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional and tolerance requirements for the reference clock signals.

3.1.4.2. CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express M.2 add-I Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control Register (offset 010h). When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the exception that it may be de-asserted during L1 PM Substates. When enabled, the CLKREQ# signal may be de-asserted during the L1 Link state.

The CLKREQ# signal is also used by the L1 PM Substates mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

The card must drive the CLKREQ# signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. The device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when it needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock.

Add-in cards that do not implement a PCI Express interface shall leave this output unconnected on the card.

CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases; including when the related function is in D3cold. This means that any component implementing CLKREQ# must be designed such that:

- Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of CLKREQ#.
- When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

3.1.4.2.1. Power-up Requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (TPVCRL) from the power rails achieving specified operating limits and PERST# assertion (see Figure 75). This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.

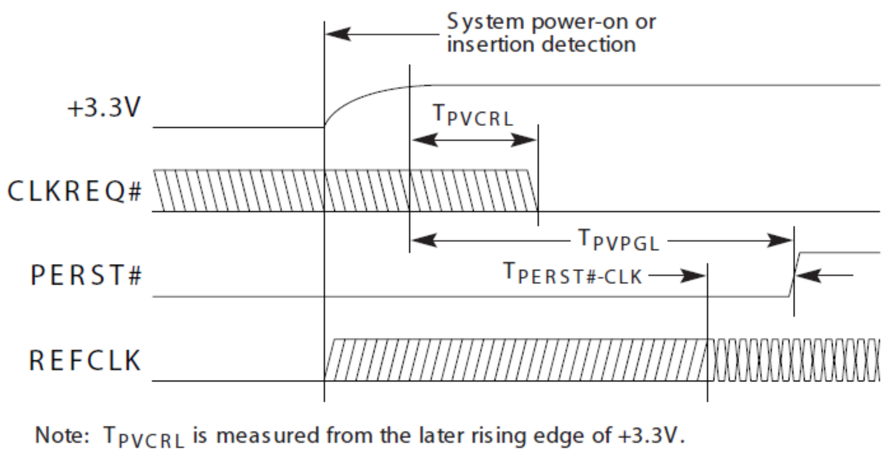


Figure 75. Power-Up CLKREQ# Timing

The system is required to have the reference clock for a PCI Express device in the parked clock state prior to device power-up. The state of the reference clock is undefined during device power-up, but it must be in the active clock state for a setup time $T_{PERST\#-CLK}$ prior to PERST# de-assertion. Table 17 lists the power-up CLKREQ# timing.

Table 17. Power-Up CLKREQ# Timings

Symbol	Parameter	Min	Max	Units
T_{PVCRL}	Power Valid to CLKREQ# Output active		100	µS
T_{PVPGL}	Power Valid to PERST# Input inactive	1		mS
$T_{PERST\#-CLK}$	REFCLK stable before PERST# inactive	100		µS

3.1.4.2.2. Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and must allow that the reference clock will transition to the parked clock state within a delay (T_{CRHoff}). Figure 76 shows the CLKREQ# clock control timing diagram.

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRLon}) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be taken into account when the device is reporting its L1 exit latency.

When the PCI Express device supports, and is enabled for, Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state may be additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.

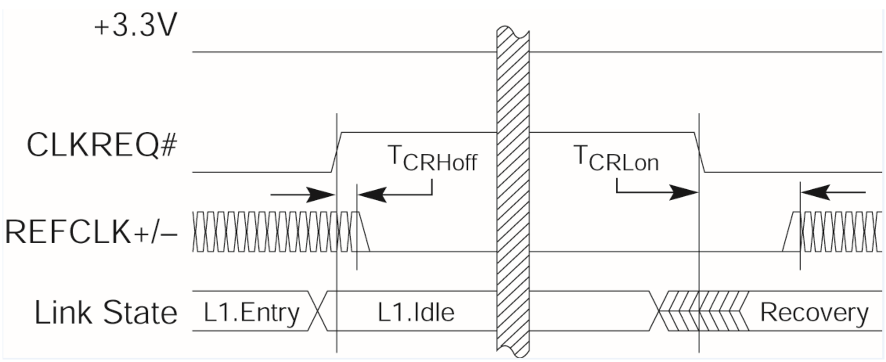


Figure 76. CLKREQ# Clock Control Timings

All links attached to a PCI Express device must complete a transition to the L1.Idle state before the device can de-assert CLKREQ#. The device must assert CLKREQ# when it detects an electrical idle break on any receiver port. The device must assert CLKREQ# at the same time it breaks electrical idle on any of its transmitter ports in order to minimize L1 exit latency. See Table 18 for CLKREQ# clock control timing.

Table 18. CLKREQ# Clock Control Timings

Symbol	Parameter	Min	Max	Units
T_{CRHOFF}	CLKREQ# de-asserted high to clock parked	0		nS
T_{CRL}	CLKREQ# asserted low to clock active		400*	nS
Note: *T_{CRLon} is allowed to exceed this value when LTR is supported and enabled for the device				

There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon}. This means that the system is not required to implement reference clock parking or that the implementation may not always act on a device de-asserting CLKREQ#. A device should also de-assert CLKREQ# when its link is in L2 or L3, much as it does during L1.

3.1.4.3. Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol should be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). To enable dynamic clock management, bit 8 of the Link Control register (offset 010h) is provided. By default, the card shall enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software may subsequently disable this feature as needed. Refer to the *PCI Express Base Specification*, Revision 1.1 (or later) for more information regarding these bits.

3.1.4.4. PERST# Signal

- The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable.
- PERST# should be used to initialize the card functions once power sources stabilize.
- PERST# is asserted when power is switched off and also can be used by the system to force a hardware reset on the card.
- System may use PERST# to cause a warm reset of the add-in card.

Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the PERST# signal.

3.1.4.5. WAKE# Signal

PCI Express M.2 Cards must implement WAKE# if the card supports either the wakeup function or the OBFF mechanism. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the WAKE# signal.

3.1.5. USB Interface

The USB interface supports USB 2.0 in all three modes (Low Speed, Full Speed, and High Speed). Because there is not a separate USB-controlled voltage bus, USB functions implemented on a PCI Express M.2 Card add-in card are expected to report as self-powered devices. All enumeration, bus protocol, and bus management features for this interface are defined by *Universal Serial Bus Specification*, Revision 2.0.

USB-based M.2 Cards that implement a wakeup process are required to use the in-band wakeup protocol (across the USB_D+/USB_D– pins) as defined in the *Universal Serial Bus Specification*.

3.1.6. Display Port Interface

The DisplayPort interface supports a full-featured implementation as defined in the referenced DisplayPort Specification. A full four lane implementation of the main link, the auxiliary channel, and hot plug detect (HPD) is supported. Additionally, a system level signal, MLDIR, is provided to assist in configuration of the platform when a Display-M.2 Card is installed.

3.1.6.1. HPD

The HPD signal connects to the standard Hot Plug Detect signal of the Display Port interface. The intent of this signal is to indicate to the DisplayPort source that a active display is connected. The logical direction of HPD is determined by the state of MLDIR.

For a wireless display application, HPD being asserted shall also be an indication that the wireless link between the system and the remote display is fully operational. When HPD is asserted, the host system software will know to locate and configure the remote display.

3.1.6.2. MLDIR

The MLDIR signal indicates the functional direction of the DisplayPort data and auxiliary interfaces on a M.2 Card; i.e. as a sink or source of the display-related interfaces. Based on the specific DisplayPort capabilities of the M.2 Card installed in the socket, the MLDIR signal termination on the card shall be as defined in Table 19.

For the M.2 Card that offers bi-directional DisplayPort capabilities, the mechanism for configuring the direction of the display interface is application and/or product-specific and not defined by this specification.

Table 19. MLDIR Pin Termination

Display-Capability on Display-M.2 Card	Example	MLDIR Pin Termination on Display-M.2 Card
DisplayPort Sink	Card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source	Card is a wireless display receiver	Terminated directly to +3.3V
DisplayPort Sink or Source	Card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

3.1.7. SDIO Interface

The M.2 SDIO interface comprise of the following Standard SDIO signals:

- Four bi-directional Data signals, each capable of data rates up to 100Mbits/Sec (for a total of 400Mbits/Sec)
- One bi-directional CMD signal.
- One Clock signal up to 50MHz

These signals are in accordance to standard SDIO specifications. Refer to the *SDIO Specification* for more details on the functional requirements for the SDIO interface signals.

The M.2 SDIO interface also includes two non-standard signals in support of new features related to the SDIO interface. This includes the following signals:

- **SDIO_Wake#**
  This signal is an output from the device (comms module) to the platform used to trigger the wake the host and to initiate SDIO interface communication between the device and the platform. This signal is an open drain output and needs to be pulled high by the platform to 1.8V always on.
- **SDIO_RESET#**
  This signal is an input to the device from the platform and it is used to reset the SDIO interface. The signal is 1.8V at the module input.

Since the SDIO_RESET# and SDIO_WAKE# are not part of the standard SDIO specification, the timing diagrams shown in Figure 77 and Figure 78 show their expected timing behavior. Table 20 lists the SDIO reset and power-up timing parameters.

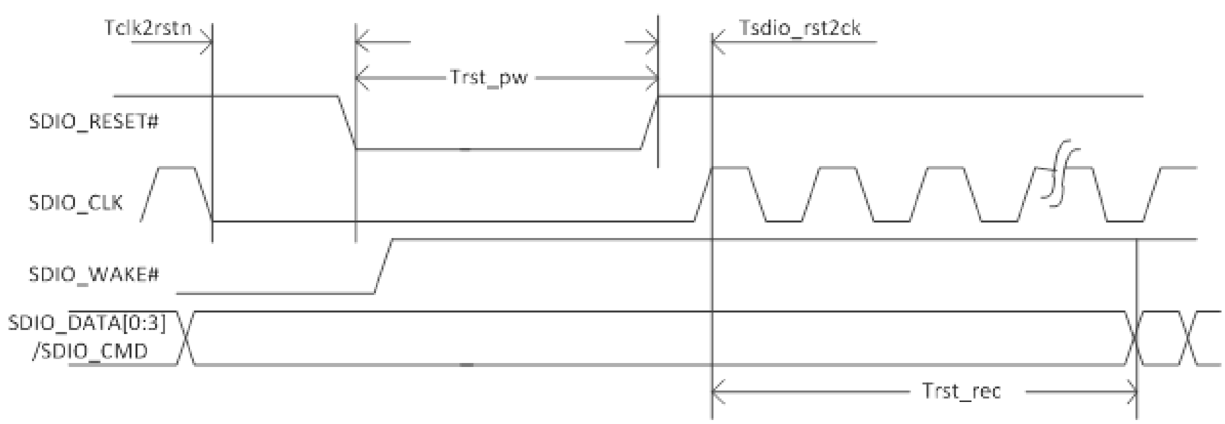


Figure 77. SDIO Reset Sequence

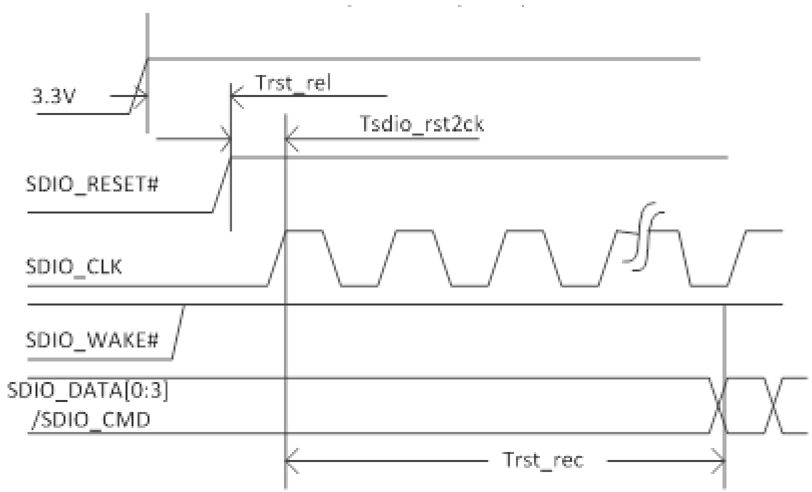


Figure 78. SDIO Power-Up Sequence

Table 20. SDIO Reset and Power-Up Timing

Symbol	Parameter	Min	Max	Unit
T_{RST_REL}	This time is measured from 3.3V ≥2.9 V	1		µS
$T_{SDIO\_RST2CLK}$	10x clock cycles of 400 KHz	25		µS
T_{RST_REC}	The time needed to allow power up the DC/DC and some basic configuration operations	100		µS
$T_{CLK2RSTN}$		0		
T_{RST_PW}	Reset pulse width	10		µS

SDIO_WAKE can be asserted by the device at any given time and it is NOT bound by timing constraint. Yet, from functionality point of view it is expected that:

- The SDIO_Wake# will be asserted (“0”) only when the host is in sleep and the device needs a service from the host.
- The SDIO_Wake# will be asserted and will not de-assert before the source for the assertion is served in the device.

3.1.8. UART Interface

The on-chip asynchronous interface (UART, Universal Asynchronous Receiver and Transmitter) can be used for communication with other host controllers or systems.

The UART can handle 8-bit data frames and inserts one start and one stop bit (with/without parity). The format of the UART frame is in Figure 79.

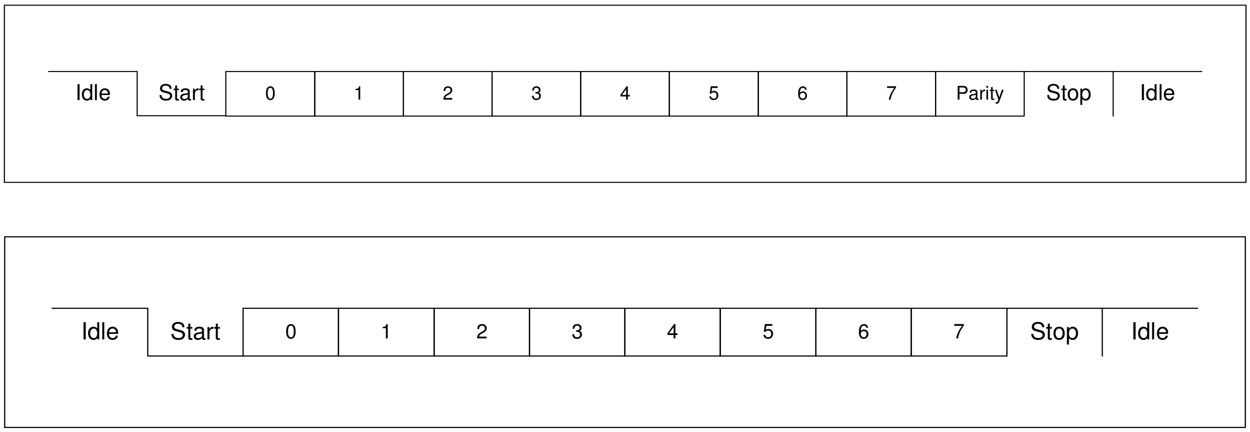


Figure 79. UART Frame Format

3.1.8.1. UART Wakeup

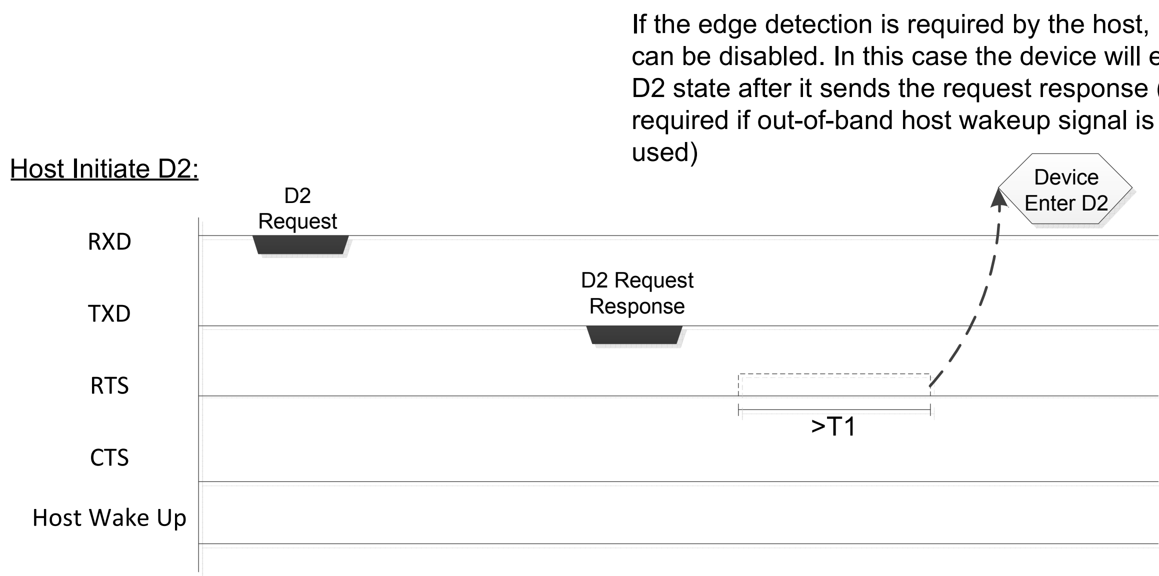
The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- RDX (Input): Receive Data
- RTX (Output): Transmit Data
- RTS (Input): Request to Send (Host Flow Control)
- CTS (Output): Clear to Send (Device Flow Control)
- Host Wake-Up (Output): Host wake-up line is optional in case the host support in band wake-up

The protocol is based on three message exchanges and a handshake between the device and host before changing the transport power state. Both sides can initiate low power modes or wake-up. The following messages are supported:

- Sleep Request
- Sleep Request Response
- Wake Up: in case the host doesn't support in band wake up using a message the device shall use the out of band Host Wake-Up signal.

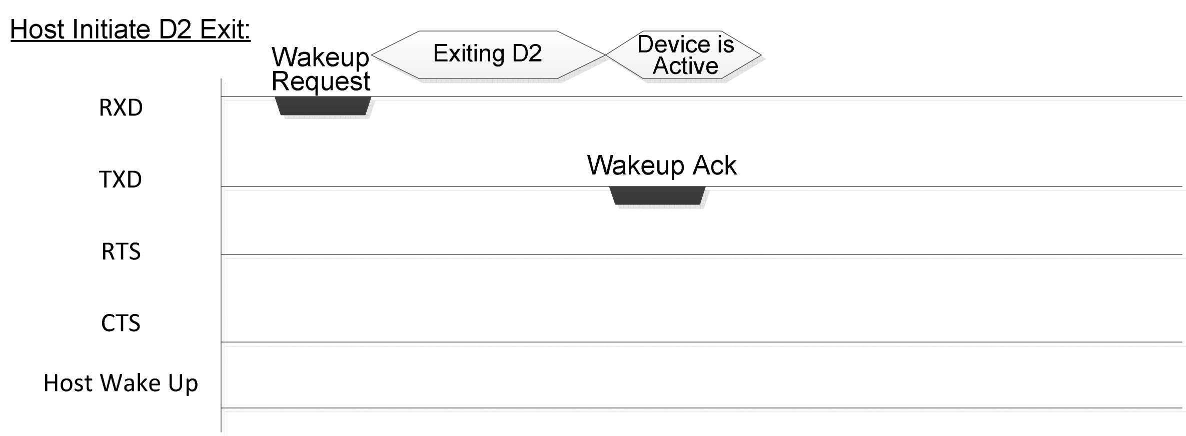
Figure 80 through Figure 83 describe the power state transitions.



1. Host sends sleep request to the device
2. Device sends Sleep Request Response Accepting the request
3. Wait for RTS falling edge if RTS Edge Detections is Enabled
4. Device enters D2

0.

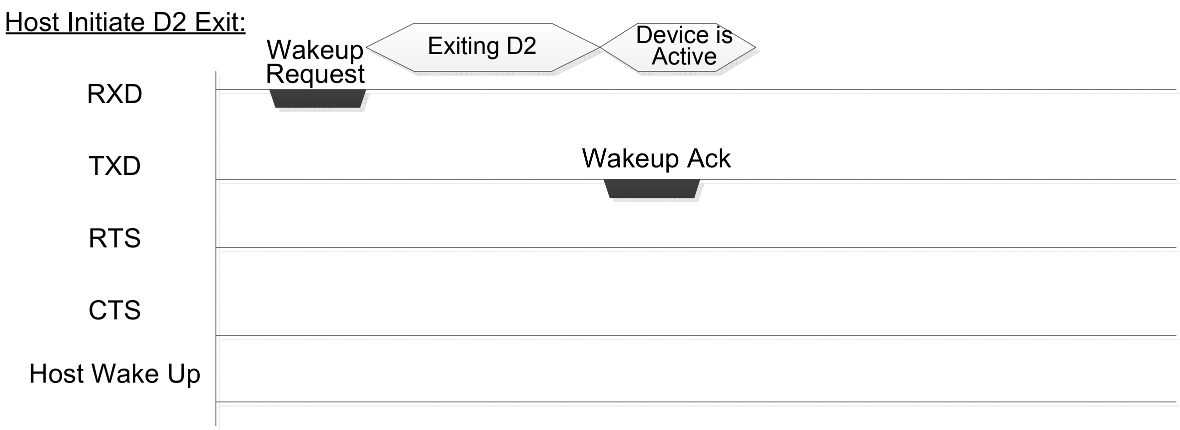
Figure 80. Sleep Request Initiated by the Host



1. Device sends a sleep request to the Host
2. Host send Seep Request Response Accepting the request
3. Device enters D2

0.

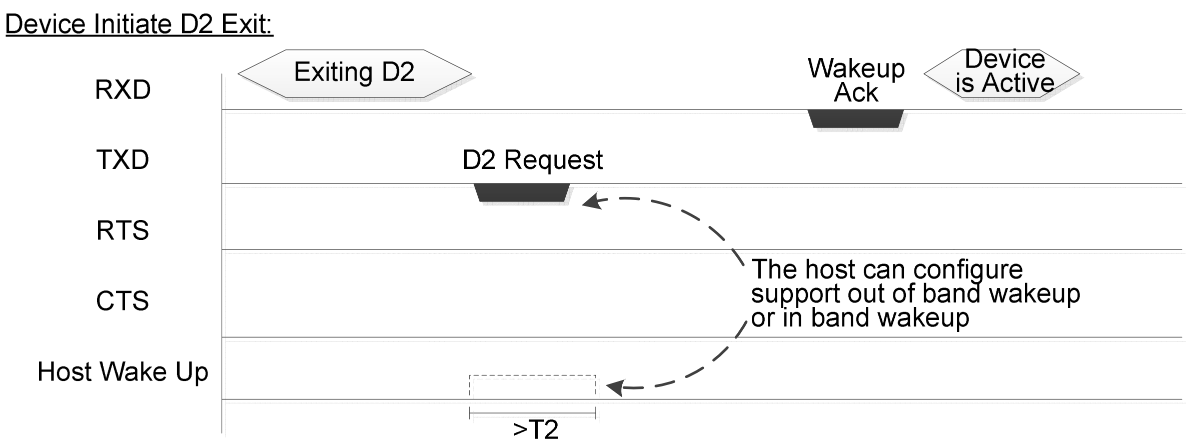
Figure 81. Sleep Request Initiated by the Device



1. Host sends wake-up request
2. Device exiting D2
3. Device send wake-up acknowledge

0.

Figure 82. Wakeup Sequence Initiated by the Host



1. Device exits D2
2. Device sends wake-up request; if in band wake-up is not supported the device shall wiggle the host wake-up signal
3. Host sends wake-up acknowledge

0.

Figure 83. Wakeup Initiated by the Device

3.1.9. PCM/I2S Interface

The following features are supported by the PCM interface:

- ❑ Four wire interface
  - Clock signal
    PCM_CLK/I2S SCK; Output if master, Input if slave
  - Two frame signals
    - PCM_SYNC/I2S WS: Output if master, Input if slave
    - PCM_CLK / I2S SCK: Output if master, Input if slave
  - Data in
    PCM_IN/I2S SD_IN: Input
  - Data out signal
    PCM_OUT/I2S SD_OUT: Output
- ❑ Single bidirectional PCM channels
- ❑ 16-bit and 24-bit data words
- ❑ Various PCM data sample rates including. 8 kHz and 16 kHz are supported

The PCM/I2S mode is used for Standard (Narrowband) Mono speech or Wideband Mono speech. I2S will also be used for offloading of stereo audio data from the host (A2DP offload).

The PCM interface consists of four signals as shown in Figure 84.

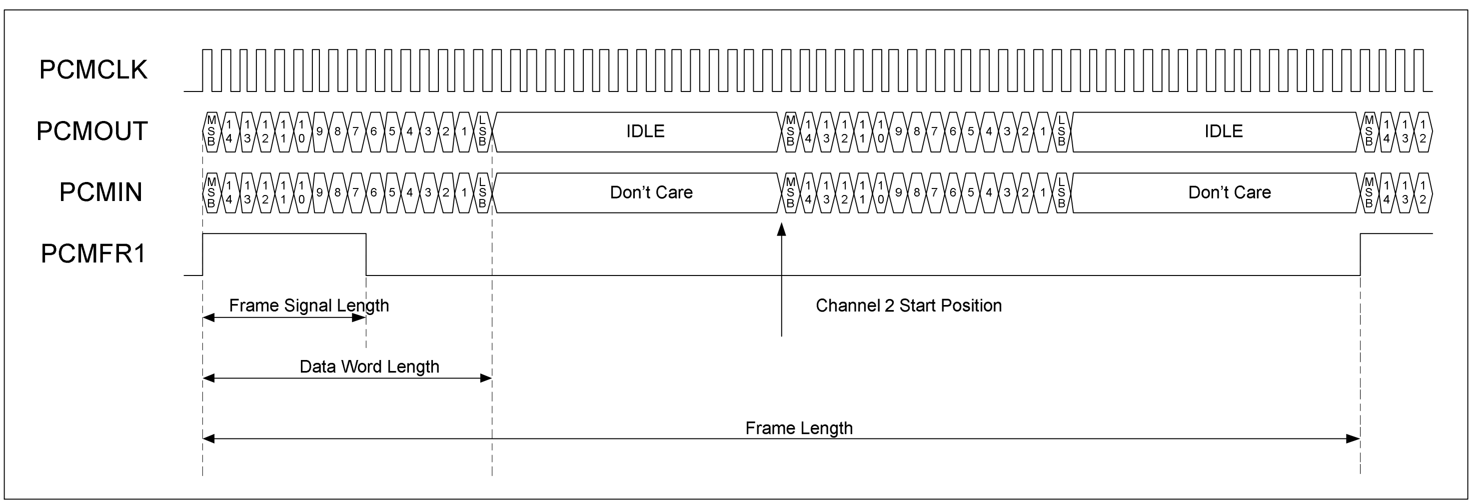


Figure 84. Typical PCM Transaction Timing Diagram

The clock signal PCMCLK is the timing base for the other signals in the PCM interface. In clock master mode, the Bluetooth device generates PCMCLK from the internal system clock using a fractional divider. In clock slave mode PCMCLK is an input to the Bluetooth device and has to be supplied by an external source.

The PCM interface supports one bidirectional channel. Data is transmitted on PCMOUT and received on PCMIN; always with the most significant bit first. The 16-bit linear audio samples and 8-bit A-law or μ-law compressed audio samples are supported.

3.1.10. I2C Interface

3.1.10.1. ALERT# Signal

This ALERT# signal is intended to indicate to the platform/system that the I2C device requires attention. This GPIO can be used to establish specific communication/signaling to the host from the device. This signal is Active Low.

3.1.10.2. I2C Data Signal

The I2C Data signal is used to send the data packets from the host to the device according to the I2C protocol. The speed supported on this line depends on the platform SMBus speeds and the device processing capability.

3.1.10.3. I2C Clock Signal

The I2C Clock signal provides the clock signaling from the host to the device to be able to decode the data on the I2C data lines.

3.1.11. NFC Supplemental UIM Interface

The UIM Power In, Power Out, and UIM SWP signals are supplemental NFC signals that can be used when a UIM device is implemented as the Secure Element. These signals are not defined in the pinouts but can be assigned to some Reserved pins in agreement between OEM←→Vendor.

3.1.11.1. UIM Power In

In systems where there is a WWAN device on one M.2 Card and an NFC solution on another M.2 Card, then the WWAN UIM Power Out should be routed to the UIP Power In pin of the M.2 Card on which the NFC device is located. This UIM power signals is basically passed through the NFC device and output through the UIP Power Out signal described in the following paragraph.

3.1.11.2. UIM Power Out

Refer to the ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements can be provided by using any GND pin. Only PCI Express M.2 Card add-in cards that support a UIM card shall connect to this pin. If the add-in card has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (for example, voltage) supported as defined in ISO/IEC 7816-3.

UIM_PWR maps to contact number C1 as defined in ISO/IEC 7816-2.UIM_PWR maps to contact number C1 as defined in ISO/IEC 7816-2.

3.1.11.3. UIM SWP

NFC includes a SWP master using ETSI TS102.613 protocol version v7.8.0, v8.1.0, v9.1.0. SWP is a full duplex, auto-clocking interface. NFC (S1) sends using V-Domain, UICC/ SE (S2) sends using I-Domain, as described in ETSI TS102.613 in chapter 8 (Physical transmission layer).

3.1.12. Communication Specific Signals

3.1.12.1. Suspend Clock

The Suspend Clock is a slow clock signal running at 32.768 kHz. It is a buffered signals derived from the platform RTC. The Suspend Clock is available during platform normal and suspend modes of operation during which time, the module can make use of this SUSCLK signal as the clock source for critical keep alive circuitry as needed. The SUSCLK is not available in platform hard shut down modes at which point, the 3.3 V power to the module is also shut down. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. Accuracy will be up to 200 ppm.

3.1.12.2. Status Indicators

Two LED signals are provided to enable wireless communication add-in cards to provide status indications to users via system provided indicators.

LED1# and LED2# output signals are active low and are intended to drive system-mounted LED indicators. These signals shall be capable of sinking to ground a minimum of 9.0 mA at up to a maximum VOL of 400 mV.

Figure 85 shows an example of how such LEDs are typically connected in a platform/system using 3.3V.

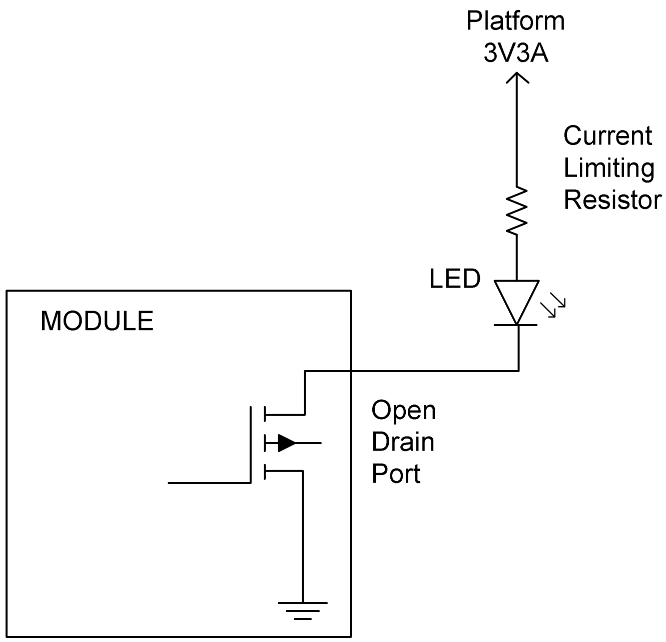


Figure 85. Typical LED Connection in Platform/System

In a typical LED connection case, the current limiting resistor value will be in the 100 Ω range to enable the 9 mA current needed to light up the LED. Other platform LED connections are possible including other alternate voltage sources. However, caution should be used to prevent back-biasing through the LED pin in various power states.

Table 21 presents a simple indicator protocol for each of two defined LED states as applicable for wireless radio operation. Although the actual definition of the indicator protocol is established by the OEM system developer, the interpretations may be useful in establishing a minimum common implementation across many platforms.

Table 21. Simple Indicator Protocol for LED States

State	Definition	Interpretation
OFF	The LED is emitting *no* light.	Radio is incapable of transmitting. This state is indicated when the card is not powered, a wireless disable signal is asserted to disable the radio, or when the radio is disabled by software.
ON	The LED is emitting light.	Radio is capable of transmitting. The LED should remain ON even if the radio is not actually transmitting. For example, the LED remains ON during temporary radio disablements performed by the M.2 Card of its own volition to do scanning, switching radios/bands, power management, etc. If the card is in a state wherein it is possible that radio can begin transmitting without the system user performing any action, this LED should remain ON.

More advanced indicator protocols are allowed as defined by the OEM system developer. Advanced features might include use of blinking or intermittent ON states which can be used to indicate radio operations such as scanning, associating, or data transfer activity. Also, use of blinking states might be useful in reducing LED power consumption.

3.1.12.3. W_DISABLE# Signal

W_DISABLE1# and W_DISABLE2# are wireless disable signals that are provided for wireless communications add-in cards. These signals allow users to disable, via a system-provided switch, the add-in card's radio operation in order to meet public safety regulations or when otherwise desired. Implementation of this signal is required for systems and all add-in cards that implement radio frequency capabilities. Multiple wireless disable signals are provided to ease managing multiple radios on a single add-in card. If only one wireless disable signal is implemented by the system, asserting that single signal should be used for collectively disabling all radios on the add-in card.

The wireless disable signals are active low signals that when asserted (driven low) by the system shall disable radio operation. When implemented, a pull-up resistor between each wireless disable signal and +3.3 V is required on the card and should be in the range of 100 kΩ to 200 kΩ. The assertion and de-assertion of each wireless disable signal is asynchronous to any system clock. All transients resulting from mechanical switches need to be de-bounced by system circuitry.

When a wireless disable signal is asserted, all of the radios associated with that signal shall be disabled. When a wireless disable signal is not asserted, the associated radios may transmit if not disabled by other means such as software. These signals may be shared between multiple M.2 Cards.

In normal operation, the card should disassociate with the wireless network and cease any further operations (transmit/receive) as soon as possible after the wireless disable signal is asserted. Given that a graceful disassociation with the wireless network fails to complete in a timely manner, the M.2 Card shall discontinue any communications with the network and assure that its radio operation has ceased no later than 30 seconds following the initial assertion of the wireless disable signal. Once the disabling process is complete, the LED specific to the radio shall indicate the disabled condition to the user.

The card should initiate and indicate to the user the process of resuming normal operation within ne second of de-assertion of the wireless disable signal. Due to the potential of a software disable state, the combination of both the software state and wireless disable signal assertion state must be determined before resuming normal operation. Table 22 defines this requirement as a function of wireless disable signal and the software control setting such that the radio's RF operation remains disabled unless both the hardware and software are set to enable the RF features of the card.

The system is required to assure that each wireless disable signal be in a deterministic state (asserted or de-asserted) whenever power is applied to the add-in; for example, +3.3 V is present.

Table 22. Radio Operational States

Wireless Disable	Signal SW Control Setting*	Radio Operation
De-asserted (HIGH)	Enable Radio	Enabled (RF operation allowed)
De-asserted (HIGH)	Disable Radio	Disabled (no RF operation allowed)
Asserted (LOW)	Enable Radio	Disabled (no RF operation allowed)
Asserted (LOW)	Disable Radio	Disabled (no RF operation allowed)
Note: *This control setting is implementation-specific and represents the collective intention of the host software to manage radio operation.		

3.1.12.4. Coexistence Signals

COEX1, COEX2 and COEX3 are provided to allow for the implementation of wireless coexistence solutions between the radio(s) on the M.2 Card and other off-card radio(s). These other radios can be located on another M.2 Card located in the same host platform or as alternate radio implementations (for example, using a PCI Express M.2 CEM or a proprietary form-factor add-in solution).

The functional definition of these pins is OEM-specific and should be coordinated between the host platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations, where practical, across multiple instances of cards in the host platform.

3.1.13. Reserved Pins

It is expected that the Reserved pins are not terminated on either the add-in card or system board-side of the connector. These pins are reserved for definition in future revisions of this specification. Non-standard use of these pins may result in incompatibilities in solutions aligned with the future revisions.

Add vendor specific section here

3.1.14. Socket 1 Connector Pin-out Definitions

The following tables illustrate signal pin-outs for the module edge card connector.

- Table 23 lists the pin-out for the SDIO based solution pinout.
- Table 24 lists the pin-out for the Display Port based solution pinout.
- Table 25 lists the pin-out for a basic module solution using the common host interfaces and utilizes a Dual Module key that will enable it to plug into two socket 1 types (Keys).

There are also module pinout definitions for Type 1216, Type 2226, and Type 3026 LGA soldered down modules in Section 3.1.15, *Socket 1 Based Soldered-down Module Pinouts*.

Table 23. SDIO Based Module Solution Pinout (Module Key E)

		GND	75
74	3.3V	RESERVED/REFCLKN1	73
72	3.3V	RESERVED/REFCLKP1	71
70	UIM_Power_In/GPIO1/PEWake1#	GND	69
68	UIM_Power_Out/CLKREQ1#	Reserved/PETn1	67
66	UIM_SWP/PERST1#	Reserved/PETp1	65
64	RESERVED	GND	63
62	ALERT# (O)(0/3.3)	Reserved/PERn1	61
60	I2C CLK (I)(0/3.3)	Reserved/PERp1	59
58	I2C DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (I)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (I)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (I)(0/3.3V)	REFCLKN0	49
48	COEX1 (I/O)(0/1.8V)	REFCLKP0	47
46	COEX2(I/O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	UART CTS (I)(0/1.8V)	PERp0	35
34	UART RTS (O)(0/1.8V)	GND	33
32	UART Rx (I)(0/1.8V)	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	SDIO Reset(I)(0/1.8V)	23
22	UART Tx (O)(0/1.8V)	SDIO Wake(O)(0/1.8V)	21
20	UART Wake (O)(0/3.3V)	SDIO DAT3(IO)(0/1.8V)	19
18	GND	SDIO DAT2(IO)(0/1.8V)	17
16	LED#2 (O)(OD)	SDIO DAT1(IO)(0/1.8V)	15
14	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
12	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
10	PCM_SYNC/I2S WS (IO)(0/1.8V)	SDIO CLK(I)(0/1.8V)	9
8	PCM_CLK/I2S SCK (IO)(0/1.8V)	GND	7
6	LED#1 (O)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

Table 24. Display Port-based Module Solution Pinout (Module key A)

		GND	75
74	3.3V	REFCLKN1	73
72	3.3V	REFCLKP1	71
70	PEWake1# (IO)(0/3.3V)	GND	69
68	CLKREQ1# (IO)(0/3.3V)	PETn1	67
66	PERST1# (I)(0/3.3V)	PETp1	65
64	RESERVED	GND	63
62	ALERT# (O)(0/3.3)	PERn1	61
60	I2C CLK (I)(0/3.3)	PERp1	59
58	I2C DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (I)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (I)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (I)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (I)(0/3.3V)	REFCLKN0	49
48	COEX1 (I/O)(0/1.8V)	REFCLKP0	47
46	COEX2(I/O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	GND	PERp0	35
34	DP_ML0p	GND	33
32	DP_ML0n	DP_HPD (IO)(0/3.3V)	31
30	GND	GND	29
28	DP_ML1p	DP_ML2p	27
26	DP_ML1n	DP_ML2n	25
24	GND	GND	23
22	DP_AUXp	DP_ML3p	21
20	DP_AUXn	DP_ML3n	19
18	GND	DP_MLDIR GND (In)/ 3.3V (Out)/NC (IO)	17
16	LED#2 (O)(OD)	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	GND	7
6	LED#1 (O)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

Table 25. Socket 1 Module Pinout with Dual Module Key (A-E)

		GND	75
74	3.3V	Reserved/REFCLKN1	73
72	3.3V	Reserved/REFCLKP1	71
70	UIM_Power_In/GPIO1/PEWake1#	GND	69
68	UIM_Power_Out/CLKREQ1#	Reserved/PERn1	67
66	UIM_SWP/PERST1#	Reserved/PERp1	65
64	RESERVED	GND	63
62	ALERT# (O)(0/3.3)	Reserved/PETn1	61
60	I2C CLK (I)(0/3.3)	Reserved/PETp1	59
58	I2C DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (I)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (I)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (I)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (I)(0/3.3V)	REFCLKN0	49
48	COEX1 (I/O)(0/1.8V)	REFCLKP0	47
46	COEX2(I/O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	N/C	PERp0	35
34	N/C	GND	33
32	N/C	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	N/C	23
22	N/C	N/C	21
20	N/C	N/C	19
18	GND	N/C	17
16	LED#2 (O)(OD)	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	GND	7
6	LED#1 (O)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

3.1.15. Socket 1 Based Soldered-down Module Pinouts

This section contains the module pinout maps for Type 2226, Type 1216, and Type 3026 LGA soldered-down modules.

- Figure 86 shows the Type 2226 A-SD Based module-side pin-out.
- Figure 87 shows the Type 1216 A-SD Based module-side pin-out
- Figure 88 shows the Type 3026 A-DP over A-SD Based module-side pin-out

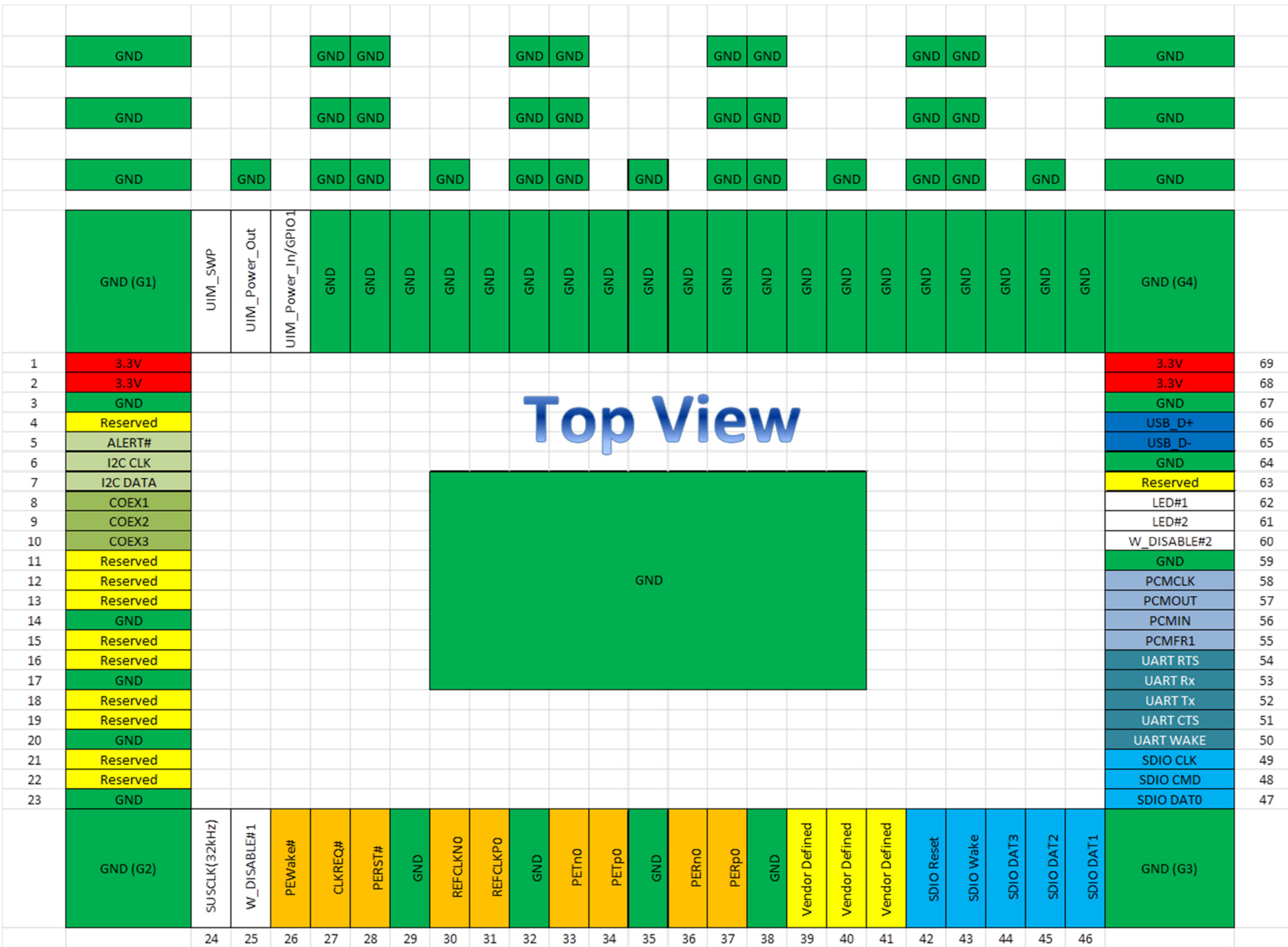


Figure 86. Type 2226 A-SD Based Module-Side Pin-Out

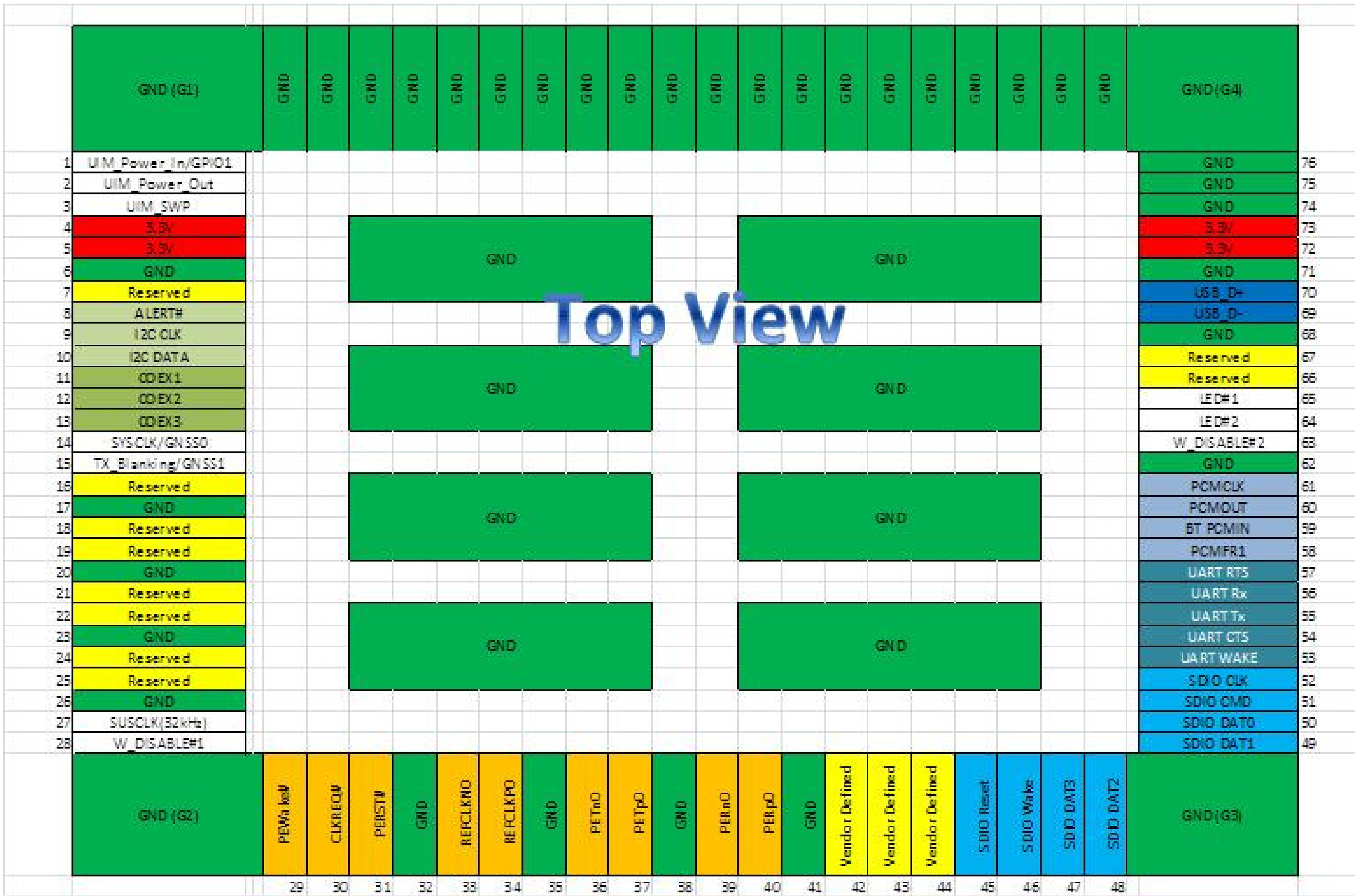
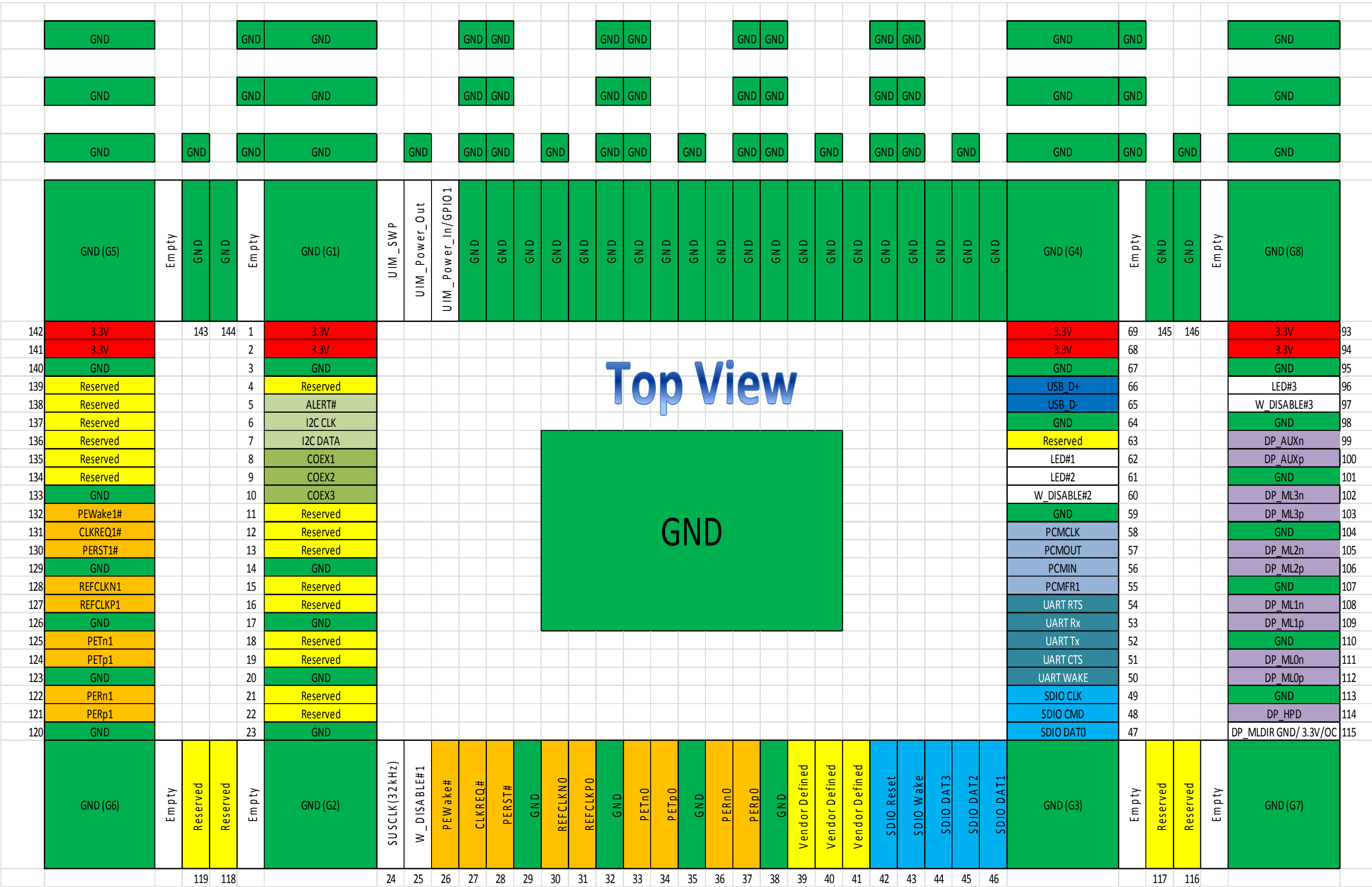


Figure 87. Type 1216 A-SD Based Module-Side Pin-Out



In this LGA pattern, the A-DP unique pins are located on the two outer columns of the pads while the center pinout pattern is the exact same pinout of Type 2226. This is done so that a land pattern footprint suitable for Type 3026 on the platform motherboard can also accommodate the regular Type 2226 as an alternate option (a drop in replacement).

Figure 88. Type 3026 A-DP over A-SD Based Module-Side Pin-Out

3.2. WWAN/SSD/Other Socket 2 System Interface Signals

The socket 2 system interface signals are listed in Table 26.

Table 26. Socket 2 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	+3.3V (5 pins)	I	3.3V source	3.3V
	GND (11 pins)		Return current path	0V
Communication Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by PCH to reduce power and cost for the module. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. 200ppm.	3.3V
	W_DISABLE1# W_DISABLE2#	I	Active low, debounced signal when applied by the system it will disable radio operation on the add-in cards that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3V
	WAKE#	O	Active low, signal is sent from module to system to provide a signal to wake up the host when required. Signal is Open Drain and requires a pull up resistor on the host	3.3V
	LED_1# (Same as SSD DAS/DSS#)	O	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. These LED devices should be tied to +3.3V through a current limiting resistor. Current should be limited to 9mA when LED is On.	3.3V
	COEX[1..3]	I/O	Coexistence between WWAN and WiFi+BT on Socket 1	1.8V
Supplemental Communication Specific Signals	Full_Card_Power_Off#	I	A single control to turn Off the WWAN solution. It is Active Low. This is only required on Tablet devices working directly off VBAT	1.8V
	Reset#	I	A single control to Reset the WWAN solution. Active Low. This is needed when working in systems/platforms running directly off VBAT	1.8V
	GPIO[0..12]	I/O	These signals form a block of programmable signals which can be used to perform various functions – See Table 33 for specific functions performed.	1.8V

Interface	Signal Name	I/O	Function	Voltage
Supplemental Communication Specific Signal **continued…**	ANTCTL[0..3]	O	These signals are used for Antenna Control and should be routed to the appropriate Antenna Control Circuitry on the platform	1.8V Nominal/ 2.8V Max
	IPC_{0..8]	I/O	Pins to facilitate IPC signals exchanged between the host and the card. Optional. Functions are BTO/CTO.	1.8V
	Audio[0..3]	I/O		1.8V
	Wake_On_WWAN	O	Used to wake the platform by the WWAN device	1.8V
	DPR	I	This signal is an input directly to the WWAN module from a suitable SAR sensor. The specific implementation will be determined by the module vendor and their customer	1.8V
PCI-e	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLK+/ REFCLK-	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the PCIe Mini Card CEM specification	3.3V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates	3.3V
	WAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3V
USB	USB D+, USB D-	I/O	USB Data ± Differential defined in the USB 2.0 Specification	
USB3.0	USB3.0-Rx+, USB3.0-Rx- USB3.0-Tx+, USB3.0-Tx-	I/O	USB3.0 TX/RX Differential signals defined by the USB 3.0 specification	
HSIC	HSIC-Data, HSIC-Strobe	I/O	HSIC Data and Strobe signals as functionally defined by the HSIC Electrical Specification.	1.2V
SSIC	SSIC-RxP, SSIC-RxN SSIC-TxP, SSIC-TxN	I/O	SSIC Tx/Rx Differential signals defined in the SSIC specification	
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	SATA A/B Differential signals defined in the SATA specification	
	DEVSLP	I	Active high signal used by the platform to put the SSD into Sleep mode	3.3V

Interface	Signal Name	I/O	Function	Voltage
SATA (continued)	DAS/DSS# (same as comm LED1#)	O	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. These LED devices should be tied to +3.3V through a current limiting resistor. Current should be limited to 9mA when LED is On.	3.3V
SSD Specific Signals	Reserved for MFG Data/Reserved for MFG Clock		Dedicated Data and Clock pins for SSD Manufacturing. Not to be connected to in the platform system	
User Identity Module (UIM) Signals	SIM Detect	I	This is an indication to the modem to detect the SIM insertion/removal. It is usually connected to the SIM reader SW pin and is card type dependent	1.8V
	UIM_RESET	O	UIM reset signal. Compliant to the ISO/IEC 7816-3 specification (RST).	
	UIM_PWR	O	Power source for the UIM. Compliant to the ISO/IEC 7816-3 specification (VCC).	
	UIM_CLK	O	UIM clock signal. Compliant to the ISO/IEC 7816-3 specification (CLK).	
	UIM_DATA	I/O	UIM data signal. Compliant to the ISO/IEC 7816-3 specification (I/O).	
Module Configuration Pins	CONFIG[0..3]	O	These signals provide the means to indicate the specific configuration of the module as well as indication of whether a module is present or not. The meaning of each of the 16 possible decodes is shown in Table 3-14 These signals should either be grounded or left No Connect to build the decode required for a given module type. The host must provide a pull up resistor for each of these signals.	0V (GND) /NC

3.2.1. Power Sources and Grounds

PCI Express M.2 Socket 2 utilizes a single power sources (3.3 V) similar to that of Socket 1. The voltage source (+3.3 V) is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In socket 2, there is provision for five 3.3 V pins to enable higher continuous current if required.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ground (GND) pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

3.2.2. PCI Express Interface

The PCI Express interface supported in Socket 2 is a two Lane interface intended for either WWAN, SSD, or other devices that need this sort of host interface. See sections 3.1.3, *PCI Express Interface* and 3.1.4, *PCI Express Auxiliary Signals* in this specification for more information.

3.2.3. USB Interface

See section 3.1.5, *USB Interface* for a detailed description of the USB signals.

3.2.4. HSIC Interface

High-Speed Inter-Chip USB (HSIC) is a low power, chip-to-chip interconnect which is 100% host driver compatible with traditional USB cable-connected topologies. HSIC is a 2-signal (strobe, data) serial interface which only supports the USB High-Speed 480 Mbps data rate. HSIC may be used through a connectorized interface taking into consideration the electrical limitations identified by the HSIC standard:

- Data/strobe trace length (TL) < 10 cm
- Data/strobe trace propagation skew (TS) < 15 ps

The current version of the HSIC specification is available at: http://www.usb.org/developers/docs/

3.2.5. SSIC Interface

SuperSpeed USB Inter-Chip (SSIC) is a chip-to-chip interconnect interface defined as a supplement to the USB 3.0 Specification. SSIC augments USB 3.0 in that the physical layer of the interconnect is based on the MIPI® Alliance M-PHYSM rather than the external cable-capable PHY of traditional SuperSpeed USB. This method better optimizes power, cost, and EMI robustness appropriate for being used for embedded inter-chip interfaces. All higher-layer aspects (software, transaction protocol, etc.) of SSIC follow the USB 3.0 specification.

SSIC – Inter-Chip Supplement to the *USB 3.0 Specification*, Revision 1.0 as of May 3, 2012; available from http://www.usb.org/developers/docs/ and located within the *USB 3.0 Specification* download package.

3.2.6. USB3.0 Interface

The *USB 3.0 Specification* defines all electrical characteristics, enumeration, protocol, and management features to support USB 3.0 (SuperSpeed).

The SuperSpeed differential transmit lines (SSTX+, SSTX-) are required to implement the transmit path of a USB 3.0 SuperSpeed interface. These pins shall be connected to the transmitter differential pair in the system and to the receiver differential pair on the module.

Likewise, SuperSpeed differential receive lines (SSRX+, SSRX-) are required to implement the receive path of a USB 3.0 SuperSpeed interface. These pins shall be connected to the receiver differential pair in the system and to the transmitter differential pair on the module.

The current version of the USB 3.0 SuperSpeed specification is available at: http://www.usb.org/developers/docs/. Also refer to the SSIC interface regarding USB3.0.

3.2.7. SATA Interface

SATA is a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers) for hard and solid state drives as defined by the *Serial ATA International Organization*.

3.2.8. User Identity Module (UIM) Interface

The UIM interface signals are defined on the system connector to provide the interface between the removable UIM, an extension of a Subscriber Identity Module (SIM), and a wireless wide area network (WWAN) radio device residing on the M.2 add-in card. The UIM contains parameters necessary for the WWAN device's operation in a wireless wide area network radio environment. The UIM signals are described in the following paragraphs for M.2 add-in cards that support the off-card UIM interface.

3.2.8.1. UIM_PWR

Refer to *ISO/IEC 7816-3* for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements can be provided by using any GND pin. Only M.2 add-in cards that support a UIM card shall connect to this pin. If the add-in card has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (for example voltage) supported as defined in *ISO/IEC 7816-3*.

UIM_PWR maps to contact number C1 as defined in *ISO/IEC 7816-2*.

3.2.8.2. UIM_RESET

The UIM_RESET signal provides the UIM card with the reset signal. Refer to *ISO/IEC 7816-3* for more details on the functional and tolerance requirements for the UIM_RESET signal. Only M.2 add-in cards that support a UIM card shall connect to this pin.

UIM_RESET maps to contact number C2 as defined in *ISO/IEC 7816-2*.

3.2.8.3. UIM_CLK

This signal provides the UIM card with the clock signal. Refer to *ISO/IEC 7816*-3 for more details on the functional and tolerance requirements for the UIM_CLK signal. Only M.2 add-in cards that support a UIM card shall connect to this pin.

UIM_CLK maps to contact number C3 as defined in *ISO/IEC 7816-2*.

3.2.8.4. UIM_DATA

This signal is used as output (UIM reception mode) or input (UIM transmission mode) for serial data. Refer to *ISO/IEC 7816-3* for more details on the functional and tolerance requirements for the UIM_DATA signal. Only M.2 add-in cards that support a UIM card shall connect to this pin.

UIM_DATA maps to contact number C7 as defined in *ISO/IEC 7816-2.Communication Specific Signals*.

3.2.8.5. SIM_DET

This signal is used to detect the insertion and removal of a SIM device in the SIM socket. With a Normal Short SIM Card connector, PUSH-PUSH type, the detect switch is normally shorted to ground when no SIM card is inserted. When the SIM is inserted, the SIM_DETECT will transition from a logic 0 to a logic 1 state. The rising edge will indicate insertion of the SIM card. When the SIM is pulled out, the SIM_DETECT will transition from the logic1 to a logic 0. This falling edge will indicates the pulling out of the SIM card. The M.2 module monitoring this signal will treat the rising/falling edge or the actual logic state as an interrupt, that when triggered, the module will act accordingly.

This will require a weak pull-up on the module tied to its 1.8 V power rail.

An example of a typical implementation can be seen in Figure 89.

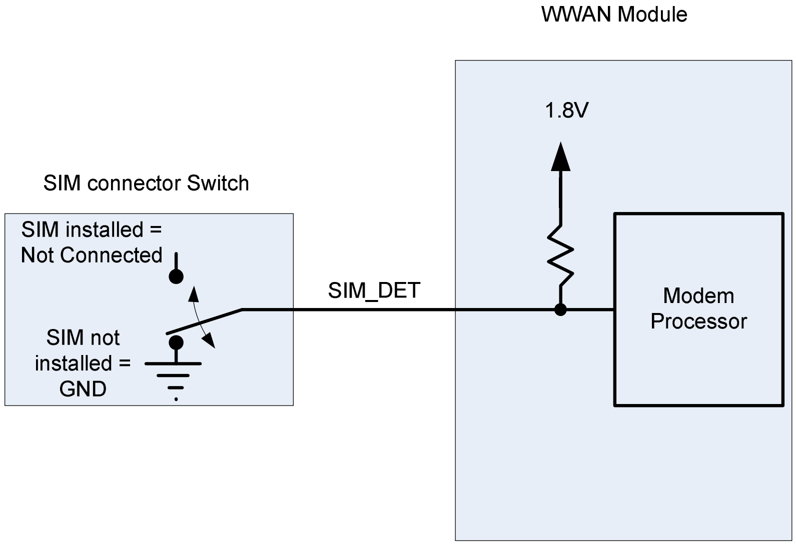


Figure 89. Typical SIM Detect Circuit Implementation

3.2.9. Communication-specific Signals

3.2.9.1. Suspend Clock

See section 3.1.12.1, *Suspend Clock* for a more detailed description of the SUSCLK signal.

3.2.9.2. Status Indicators

See section 3.1.12.2, Status Indicators for a more detailed description of the LED1# signal.

3.2.9.3. W_DISABLE# Signals

See section 3.1.12.3, *W_DISABLE# Signal* for a more detailed description of the W_Disable1# and W_Disable2# signals.

3.2.9.4. Coexistence Signals

See section 3.1.12.4, *Coexistence Signals* for a more detailed description of the COEX signals.

3.2.10. Supplemental Communication Specific Signals

3.2.10.1. Full Card Power Off

Full Card Power Off signal is an Active Low input that will turn the module On when asserted high (≥1.7 V) and will force the module to shut down when asserted low (≤0.2 V) or Tri-stated. The FULL_CARD_POWER_OFF# pin needs to be internally pulled low with a weak pull-down resistor of >20Kohms.

The module design must ensure that the operation of this pin is asynchronous to any other interface operation.

The input must be 3.3V tolerant but can be driven by either 1.8V or 3.3V GPIO. Host side implementation for this signal to be defined by Module vendor including timing diagrams, operation sequencing etc. that are implementation specific.

3.2.10.1.1. Example of Power On/Off Sequence

Following is an example of a full-card power On/Off sequences:

1. Modem power on:
   High level will trigger modem power on sequence.
2. Modem power off:
   The modem is powered off first via an AT command, subsequently there is a handshaking between host and modem.
3. FULL_CARD_POWER_OFF# pin will turn to LOW level or Tri-state to shutdown modem's PMU.

3.2.10.1.2. Example of Tablet Power On/Off Sequence

The following example sequences are for illustrative purposes only, as module vendors can offer alternate solutions and requirements.

1. Battery always connected to modem.
2. Host triggers GPIO to High on the FULL_CARD_POWER_OFF# pin
3. Modem turns On.
4. Host issue AT command to switch off modem.
5. Handshaking between modem and host
6. Host sets GPIO to LOW (or Tri-state) on FULL_CARD_POWER_OFF# pin which will switch off modem PMU Proper Shutdown Handshaking Process.
7. PC Host sends AT+CFUN=0 to Modem,

8. Modem responds OK.
   Modem will do the essential shutdown tasks before sending OK:
   a) Proper detaching from cellular network.
   b) SW clean up functions, saving necessary NVM parameters and etc.
   c) Activate SIM/EBU shutdown sequences.
   d) Above task may need few milliseconds to couple of seconds depending on the state of the modem.
9. Modem sends OK to AP upon completion of essential tasks.
10. If AP receives ERROR, it should try again for AT+CFUN=0.
11. Modem completes PMU power off sequences/register access after sending OK.
    The following process takes less than one second:
    a) Disable all regulators (except VPMU and VRTC LDOs).
    b) Assert reset signals.
    c) Release the 26 MHz system clock request signal.
12. AP cuts off power supply or pull-on/off pin LOW /Tri-state after fixed delay of one second.
    In a rare case, if AP did not receive any response within _*_ seconds of issuing AT+CFUN=0, AP will assume that it is OK. There may be times when USB may be over loaded and by the time it is ready to send OK, the driver shutdown will already have started and OK may not reach AP.

Note: *The response time _*_ is to be decided by the host.

3.2.10.1.3. Example of Very-thin Notebooks Power On/Off Sequence

Very-thin notebooks do not use the FULL_CARD_POWER_OFF# signal. Following is the power ON/Off sequence for very-thin notebooks:

1. Modem gets 3.3V when supply for the modem is switched on.
2. Modem turns On since the FULL_CARD_POWER_OFF# pin is pulled high by the host (pin 6 connected to 1.8V or 3.3V).
3. Host issues AT command to switch off modem.
4. Handshaking between modem and host.
   Once the handshake has been complete, the host will cut off supply to the modem.

3.2.10.2. RESET#

Asynchronous RESET# pin, active low. Whenever this pin is active, the modem will immediately be placed in a Power On reset condition. Care should be taken not to activate this pin unless there is a critical failure and all other methods of regaining control and/or communication with the WWAN sub-system have failed.

! CAUTION: Triggering the RESET# signal will lead to loss of all data in the modem and the removal of system drivers. It will also disconnect the modem from the network resulting in a call drop.

3.2.10.3. General Purpose Input Output Pins

The GPIO0–12 pins have configurable assignments. There are four possible functional pinout configurations. These four configurations are called Port Config 0–3. In each Port Configuration, each GPIO is defined as a specific functional pin. The GPIO pin assignments are listed in Table 27.

Table 27. GPIO pin Function Assignment per Port Configuration

	Pin	Port Config_0[1]	Port Config_1[2]	Port Config_2[3]	Port Config_3[4]
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	HSIC_Data
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2	HSIC_Strobe
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_0
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_1
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_2
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	Audio_0
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	Audio_1
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_3/Audio_2
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_4/Audio_3
GPIO_9	10	LED#1	LED#1	LED#1	IPC_5
GPIO_10	26	W_Disable2#	W_Disable2#	W_Disable2#	IPC_6
GPIO_11	23	Wake_On_WWAN	Wake_On_WWAN	Wake_On_WWAN	IPC_7
GPIO_12	25	DPR	DPR	DPR	IPC_8

[1] GNSS+Audio version 1
[2] GNSS+Audio version 2
[3] 2nd UIM/SIM Support
[4] HSIC Support

3.2.10.3.1. GNSS Signals

- **GNSS_SCL**
  Input clock for I2C interface for transfer of location data. External device is bus master. For use as a low power interface for location data when host CPU is in low power mode.
- **GNSS_SDA**
  Bi-directional data interface for I2C. For transfer of location data to/from external device (such as a sensor hub).
- **GNSS_IRQ**
  Interrupt signal – bi directional to provide on demand GNSS data to/from external device (such as a sensor hub). Goal is provide a low power interface for location data when host CPU is in low power mode.

- **SYSCLK**
  A clock generated by the module to provide a means to synchronize the internal WWAN sub system on the module to an external GNSS device. Used in conjunction with Tx_Blanking signal. Frequency of operation (and clock type) will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.
- **TX_BLANKING**
  This signal is active high and will be asserted to signal when the WWAN sub system is engaged in activity which would swamp the GNSS signal being received by an external device. This signal is used in conjunction with SY_CLK signal – specific operation will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.
- **GNSS0.1**
  These are pins reserved for proprietary GNSS functions which will be part of BTO on a vendor specific basis.

3.2.10.3.2. Audio Signals

- **AUDIO0–3**
  These pins are reserved for Audio use. However the specific implementations with be part of a BTO option determined specifically by the module vendor and their customers. Support for this function is optional.

3.2.10.3.3. Second UIM Signals

- **UIM**
  Interface to support Dual SIM operation – this interface consists of the following signals;
- **SIM_DET2#, UIM_DAT2, UIM_CLK2, UIM_RST2, UIM_PWR2**
  Support for Dual SIM operation is optional – however these pins cannot be used for an alternative function in this configuration matrix. For specific pin definitions please section 3.2.7
- **RFU – Reserved for Future Use**
  These pins are not yet assigned as part of this standard but will be allocated as the need arises. These pins cannot be used for any function in this configuration matrix and should be avoided and treated as No Connects at this time.

3.2.10.3.4. IPC[0..8] Signals

These pins may be used for inter-processor communications between the host and the card. The signals assigned to the pins are BTO/CTO.

3.2.10.3.5. DPR Signal

The optional DPR (Dynamic Power Reduction) signal is used by wireless devices to assist in meeting regulatory SAR (Specific Absorption Rate) requirements for RF exposure. The signal is provided by a host system proximity sensor to the wireless device to provide an input trigger causing a reduction in the radio transmit output power.

The required value of the power reduction will vary between different host systems and is left to the host platform OEM and card vendor to determine, along with the specific implementation details. The assertion and de-assertion of DPR is asynchronous to any system clock. All transients resulting from the proximity sensor need to be de-bounced by system circuitry.

3.2.10.3.6. WAKE_ON_WWAN Signal

The WAKE_ON_WWAN# signal is used to wake up the host. It is open drain and should be pulled up at the host side. When the WWAN needs to wake up the host, it will output a one second low pulse, shown in Figure 90.

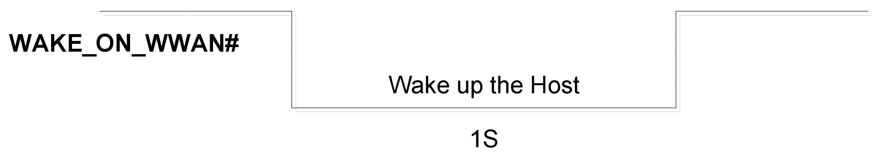


Figure 90. WAKE_ON_WWAN# Signal

3.2.10.4. Antenna Control

ANTCTRL (0-3) are provided to allow for the implementation of antenna tuning solutions. The number antenna control lines required will depend on the application and antenna/band requirements.

The functional definition of the antenna control pins are OEM-specific and should be coordinated between the host platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations—where practical—across multiple instances of cards in the host platform.

3.2.11. SSD Specific Signals

3.2.11.1. DEVSLP

The DEVSLP (Device Sleep) pin is used to inform an SSD that it should enter a lower-power state.

3.2.11.2. DAS/DSS#

The DAS (Drive activity Signal) is driven by the SSD to indicate that an access is occurring. See section 3.1.12.2, Status Indicators for information on the LED signal pin.

3.2.11.3. Reserved for MFG Clock and Data

There are two module pins that are dedicated as SSD Manufacturing pins. Their purpose is dependent on implementation of the vendor. These pins must be no-connect on the motherboard.

On the Platform/System side, these pins should be left no-connect.

3.2.12. Configuration Pins

Socket 2 incorporates four configuration pins which can assist the platform to identify the presence of an Add-In card in the socket and identify card Type, Host I/F it utilizes, and, in the case of WWAN, Port Configuration for the GPIO0–7 interface pins.

The operation of this configuration interface is as follows:

- Pins CONFIG_0..3
  These pins are grounded or left NC on the Module per the desired configuration attached to the Host device when plugged into the Socket 2. All configuration pins should be read and decoded by the host platform to recognize the indicated module configuration and host interface supported as listed in Table 28.
- On the platform side, each of the CONFIG_0..3 signals needs to be fitted with a pull-up resistor. Based on the state of the configuration pins on the module, being tied to GND or left No Connect (NC), the sensed pins will create a 4-bit logic state that require decoding.
- This configuration scheme will ensure that a module and it's configuration can always be detected

Table 28. Socket 2 Module Configuration

Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
GND	GND	GND	GND	SSD – SATA	N/A
GND	NC	GND	GND	SSD – PCIe	N/A
GND	GND	NC	GND	WWAN – PCIe	0
GND	NC	NC	GND	WWAN – PCIe	1
GND	GND	GND	NC	WWAN – USB 3.0	0
GND	NC	GND	NC	WWAN – USB 3.0	1
GND	GND	NC	NC	WWAN – USB 3.0	2
GND	NC	NC	NC	WWAN – USB 3.0	3
NC	GND	GND	GND	WWAN – SSIC	0
NC	NC	GND	GND	WWAN – SSIC	1
NC	GND	NC	GND	WWAN – SSIC	2
NC	NC	NC	GND	WWAN – SSIC	3
NC	GND	GND	NC	WWAN – PCIe	2
NC	NC	GND	NC	WWAN – PCIe	3
NC	GND	NC	NC	RFU	N/A
NC	NC	NC	NC	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
[2] Applicable to WWAN only

3.2.12.1. Socket 2 Connector Pin-out Definitions

The following tables list the signal pin-outs for the module edge card connector.

- Table 29, SSIC based WWAN solution pinout
- Table 30, USB3.0 based WWAN solution pinout
- Table 31, PCIe based WWAN solution pinout

All three of these WWAN pinouts also support legacy USB2.0-based WWAN solutions or optionally HSIC.

Table 29. Socket 2 SSIC-based WWAN Module Pinout

		CONFIG_2 (States 8, 9, 10, 11)	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	CONFIG_1 (States 8, 9, 10, 11)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	Reset# (I)(0/1.8V)	67
66	SIM Detect (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX1 (I/O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX2(I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3(I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	N/C	GND	57
56	N/C	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	N/C	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_2 (IO)(0/1.8V*)	N/C	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_1 (IO)(0/1.8V*)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_0 (IO)(0/1.8V*)	N/C	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DTA2/HSIC_Strobe (IO)(0/1.8V*)	N/C	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/HSIC_Data (IO)(0/1.8V*)	GND	39
38	N/C	SSIC-RxP	37
36	UIM-PWR (O)	SSIC-RxN	35
34	UIM-DATA (IO)	GND	33
32	UIM-CLK (O)	SSIC-TxP	31
30	UIM-RESET (O)	SSIC-TxN	29
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_4-AUDIO_3 (IO) (0/1.8V)	GND	27
26	GPIO_10 - W_Disable2#/W_Disable2#/W_Disable2#/IPC_6 (IO) (0/1.8V)	GPIO_12 - DPR/DPR/DPR/IPC_8 (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_3-AUDIO_2 (IO) (0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN#/IPC_7 (O)(0/1.8V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (IO)(0/1.8V)	CONFIG_0 = NC	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (IO)(0/1.8V)	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	GND	11
10	GPIO_9 - LED#1/LED#1/LED#1/IPC_5 (O)(OD)	USB_D-	9
8	W_DISABLE#1 (I)(0/3.3V)	USB_D+	7
6	Full_Card_Power_Off# (I)(0/1.8V)	GND	5
4	3.3V	GND	3
2	3.3V	CONFIG_3 = GND	1

Table 30. Socket 2 USB3.0-based WWAN Module Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 4, 5, 6, 7)	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	CONFIG_1 (States 4, 5, 6, 7)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	Reset# (I)(0/1.8V)	67
66	SIM Detect (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX1 (I/O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX2(I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3(I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	N/C	GND	57
56	N/C	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	N/C	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_2 (IO)(0/1.8V*)	N/C	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_1 (IO)(0/1.8V*)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_0 (IO)(0/1.8V*)	N/C	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DTA2/HSIC_Strobe (IO)(0/1.8V*)	N/C	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/HSIC_Data (IO)(0/1.8V*)	GND	39
38	N/C	USB3.0-Rx+	37
36	UIM-PWR (O)	USB3.0-Rx-	35
34	UIM-DATA (IO)	GND	33
32	UIM-CLK (O)	USB3.0-Tx+	31
30	UIM-RESET (O)	USB3.0-Tx-	29
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_4-AUDIO_3 (IO) (0/1.8V)	GND	27
26	GPIO_10 - W_Disable2#/W_Disable2#/W_Disable2#/IPC_6 (IO) (0/1.8V)	GPIO_12 - DPR/DPR/DPR/IPC_8 (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_3-AUDIO_2 (IO) (0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN#/IPC_7 (O)(0/1.8V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (IO)(0/1.8V)	CONFIG_0 = GND	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (IO)(0/1.8V)	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	GND	11
10	GPIO_9 - LED#1/LED#1/LED#1/IPC_5 (O)(OD)	USB_D-	9
8	W_DISABLE#1 (I)(0/3.3V)	USB_D+	7
6	Full_Card_Power_Off# (I)(0/1.8V)	GND	5
4	3.3V	GND	3
2	3.3V	CONFIG_3 = NC	1

Table 31. Socket 2 PCIe-based WWAN Module Pinout

74	3.3V	CONFIG_2 (States 2, 3, 12, 13)	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 2, 3, 12, 13)	69
66	SIM Detect (I)	Reset# (I)(0/1.8V)	67
64	COEX1 (I/O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX2(I/O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3(I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	N/C	ANTCTL0 (O)(0/1.8V)	59
56	N/C	GND	57
54	PEWake# (IO)(0/3.3V)	REFCLKP	55
52	CLKREQ# (IO)(0/3.3V)	REFCLKN	53
50	PERST# (I)(0/3.3V)	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_2 (IO)(0/1.8V*)	PERp0	49
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_1 (IO)(0/1.8V*)	PERn0	47
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_0 (IO)(0/1.8V*)	GND	45
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DTA2/HSIC_Strobe (IO)(0/1.8V*)	PETp0	43
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/HSIC_Data (IO)(0/1.8V*)	PETn0	41
38	N/C	GND	39
36	UIM-PWR (O)	N/C	37
34	UIM-DATA (IO)	N/C	35
32	UIM-CLK (O)	GND	33
30	UIM-RESET (O)	N/C	31
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_4-AUDIO_3 (IO) (0/1.8V)	N/C	29
26	GPIO_10 - W_Disable2#/W_Disable2#/W_Disable2#/IPC_6 (IO) (0/1.8V)	GND	27
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_3-AUDIO_2 (IO) (0/1.8V)	GPIO_12 - DPR/DPR/DPR/IPC_8 (I)(0/1.8V)	25
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (IO)(0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN#/IPC_7 (O)(0/1.8V)	23
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (IO)(0/1.8V)	CONFIG_0 (States 2, 3, 12, 13)	21
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
10	GPIO_9 - LED#1/LED#1/LED#1/IPC_5 (O)(OD)	GND	11
8	W_DISABLE#1 (I)(0/3.3V)	USB_D-	9
6	Full_Card_Power_Off# (I)(0/1.8V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	GND	3
		CONFIG_3 (States 2, 3, 12, 13)	1

See Table 28 for a list of Socket 2 configuration bits on the Module used to identify the desired pinout and Port Configuration.

This section also contains the following tables containing the signal pinout for:

- Table 32, SATA based SSD solution
- Table 33, PCIe Multi-Lane based SSD solution

The pinouts in these two tables utilize a dual module key scheme to enable these solutions to also plug into a Socket 3 connector if available in the platform. The CONFIG_1 pin in these pinouts is equivalent to the PEDET signal used in Socket 3.

Table 32. Socket 2 SATA-based SSD Module Pinout

		CONFIG_2 = GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	CONFIG_1 = GND	69
68	SUSCLK(32kHz) (I)(0/3.3V)	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved for MFG Clock	GND	57
56	Reserved for MFG Data	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	SATA-A+	49
48	N/C	SATA-A-	47
46	N/C	GND	45
44	N/C	SATA-B-	43
42	N/C	SATA-B+	41
40	N/C	GND	39
38	DEVSLP (I)(0/3.3V)	N/C	37
36	N/C	N/C	35
34	N/C	GND	33
32	N/C	N/C	31
30	N/C	N/C	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	CONFIG_0 = GND	21
20	N/C	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	N/C	11
10	DAS/DSS# (O)(OD)	N/C	9
8	N/C	N/C	7
6	N/C	N/C	5
4	3.3V	GND	3
2	3.3V	CONFIG_3 = GND	1

Table 33. Socket 2 PCIe-based SSD Module Pinout

Pin	Signal (even side)	Signal (odd side)	Pin
		CONFIG_2 = GND	75
74	3.3V		
		GND	73
72	3.3V		
		GND	71
70	3.3V		
		CONFIG_1 = NC	69
68	SUSCLK(32kHz) (I)(0/3.3V)		
		N/C	67
	Module Key		
		Module Key	
	Module Key		
		Module Key	
	Module Key		
		Module Key	
	Module Key		
		Module Key	
58	Reserved for MFG Clock		
		GND	57
56	Reserved for MFG Data		
		REFCLKP	55
54	PEWake# (IO)(0/3.3V)		
		REFCLKN	53
52	CLKREQ# (IO)(0/3.3V)		
		GND	51
50	PERST# (I)(0/3.3V)		
		PERp0	49
48	N/C		
		PERn0	47
46	N/C		
		GND	45
44	N/C		
		PETp0	43
42	N/C		
		PETn0	41
40	N/C		
		GND	39
38	DEVSLP (I)(0/3.3V)		
		PERp1	37
36	N/C		
		PERn1	35
34	N/C		
		GND	33
32	N/C		
		PETp1	31
30	N/C		
		PETn1	29
28	N/C		
		GND	27
26	N/C		
		N/C	25
24	N/C		
		N/C	23
22	N/C		
		CONFIG_0 = GND	21
20	N/C		
		Module Key	
	Module Key		
		Module Key	
	Module Key		
		Module Key	
	Module Key		
		Module Key	
	Module Key		
		N/C	11
10	DAS/DSS# (O)(OD)		
		N/C	9
8	N/C		
		N/C	7
6	N/C		
		N/C	5
4	3.3V		
		GND	3
2	3.3V		
		CONFIG_3 = GND	1

3.3. SSD Socket 3 System Interface Signals

Table 34 contains a list of the Socket 3 system interface signals.

Table 34. Socket 3 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	+3.3V (9 pins)	I	3.3V source	3.3V
	GND (14 pins)		Return current path	0V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLK+/ REFCLK-	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	O	PE-Reset is a functional reset to the card as defined by the PCIe Mini Card CEM specification	3.3V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates	3.3V
	WAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3V
SATA	SATA-A+, SATA-A-/SATA-B+, SATA-B-	I/O	SATA A/B Differential signals defined in the SATA specification	
	DEVSLP	I	Active high signal used by the platform to put the SSD in Sleep mode	3.3V
	DAS/DSS#	O	Status indicators via LED devices that will be provided by the system Active Low. A pulled-up LED with series current limiting resistor should allow for 9mA when On	3.3V
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by PCH to reduce power and cost for the module. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. 200ppm.	3.3V
	Reserved for MFG Data		Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket	
	Reserved for MFG Clock		Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket	

3.3.1. Power and Grounds

PCI Express M.2 Socket 3 utilizes a single 3.3 v power sources similar to that of Socket 1 and 2. The voltage source, +3.3V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In socket 3, there is provision for nine 3.3 V pins to enable high continuous current, the same as in Socket 2 if required. The higher number of pins will help to reduce further the IR drop on the connector.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ground (GND) pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

3.3.2. PCI Express Interface

The PCI Express interface supported in Socket 3 is a four lane PCI Express interface intended for premium SSD devices that need this sort of host interface. Socket 3 can also support SSD devices that make use of only two lanes PCI Express and are able to be plugged in Socket 2 with the aid of a Dual Module key.

See section 3.1.3 in this specification for a detailed description of the PCIe signals.

3.3.3. SATA Interface

SATA is a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers) for hard and solid state drives as defined by the Serial ATA International Organization.

3.3.4. SSD Specific Signals

3.3.4.1. SUSCLK

See section 3.1.12.1 in this specification for a detailed description of the SUSCLK (Suspend Clock) signal.

3.3.4.2. PEDET

The interface detect can be used by the host computer to determine the communication protocol that the M.2 card uses; SATA signaling (low) or PCIe signaling (high).

3.3.4.3. DEVSLP

The DEVSLP (Device Sleep) pin is used to inform an SSD that it should enter a lower-power state.

3.3.4.4. DAS/DSS#

The DAS (Drive Activity Signal) is driven by the SSD to indicate that an access is occurring. See section 3.1.12.2 for information on the LED signal pin.

3.3.4.5. MFG Clock & Data

There are two module pins that are dedicated as SSD Manufacturing pins. Their purpose is dependent on implementation of the vendor. These pins must be no-connect on the motherboard.

3.3.4.6. Socket 3 Connector Pin-out Definitions

Table 35 and Table 36 list the signal pin-outs for the module edge card connector. Table 35 lists the SATA based solution pinout. Table 36 lists the PCIe Multi-Lane based solution pinout.

Table 35. Socket 3 SATA-based Module Pinout

		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET (GND-SATA)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved/MFG Clock	GND	57
56	Reserved/MFG Data	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	SATA-A+	49
48	N/C	SATA-A-	47
46	N/C	GND	45
44	N/C	SATA-B-	43
42	N/C	SATA-B+	41
40	N/C	GND	39
38	DEVSLP (I)(0/3.3V)	N/C	37
36	N/C	N/C	35
34	N/C	GND	33
32	N/C	N/C	31
30	N/C	N/C	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	GND	21
20	N/C	N/C	19
18	3.3V	N/C	17
16	3.3V	GND	15
14	3.3V	N/C	13
12	3.3V	N/C	11
10	DAS/DSS# (O)(OD)	GND	9
8	N/C	N/C	7
6	N/C	N/C	5
4	3.3V	GND	3
2	3.3V	GND	1

Table 36. Socket 3 PCIe-based Module Pinout

		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET (NC-PCIe)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved/MFG Clock	GND	57
56	Reserved/MFG Data	REFCLKP	55
54	PEWake# (IO)(0/3.3V)	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	N/C	PERn0	47
46	N/C	GND	45
44	N/C	PETp0	43
42	N/C	PETn0	41
40	N/C	GND	39
38	DEVSLP (I)(0/3.3V)	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	N/C	PETn1	29
28	N/C	GND	27
26	N/C	PERp2	25
24	N/C	PERn2	23
22	N/C	GND	21
20	N/C	PETp2	19
18	3.3V	PETn2	17
16	3.3V	GND	15
14	3.3V	PERp3	13
12	3.3V	PERn3	11
10	DAS/DSS# (O)(OD)	GND	9
8	N/C	PETp3	7
6	N/C	PETn3	5
4	3.3V	GND	3
2	3.3V	GND	1

4

4. Electrical Requirements

4.1. 3.3 V Logic Signal Requirements

The 3.3 V card logic levels for single-ended digital signals (WAKE#, CLKREQ#, PERST#, SUSCLK, W_DISABLE#, UART_WAKE, I2C, MLDIR) are given in Table 37.

Table 37. DC Specification for 3.3V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
+3.3V	Supply Voltage		3.3 – 5%	3.3 + 5%	V	
V_{IH}	Input High Voltage		2.0	3.6	V	
V_{IL}	Input Low Voltage		-0.5	0.8	V	
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	1
I_{IN}	Input Leakage Current	0 V to 3.3 V	-10	+10	µA	
I_{LKG}	Output Leakage Current	0 V to 3.3 V	-50	+50	µA	
C_{IN}	Input Pin Capacitance			7	pF	
C_{OUT}	Output Pin Capacitance			30	pF	
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	2

Notes:

1. Not applicable to LED# and DAS/DSS# pins.
2. Applies to CLKREQ# pull-up on host system

4.1.1. 1.8 V Logic Signal Requirements

The 1.8 V card logic levels for single-ended digital signals (SDIO, UART, PCM/I2S, etc.) are given in Table 38.

Table 38. DC Specification for 1.8V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
+1.8V	Supply Voltage		1.7	1.9	V	
V_{IH}	Input High Voltage		0.65 * 1.8	1.8 + 1.0	V	
V_{IL}	Input Low Voltage		-0.3	0.35 * 1.8	V	
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	
I_{IN}	Input Leakage Current	0 V to 1.8 V	-10	+10	µA	
I_{LKG}	Output Leakage Current	0 V to 1.8 V	-50	+50	µA	
C_{IN}	Input Pin Capacitance			7	pF	
C_{OUT}	Output Pin Capacitance			10	pF	

4.1.2. Power

The M.2 module utilizes a single regulated power rail of 3.3V provided by the platform. There is no other VDDIO like pin and the module is responsible for generating its own I/O voltage source using the 3.3V power rail. This 3.3V voltage rail source on the platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs may require host (driver) intervention after a power-on.

The number of 3.3V pins for any given pin-out is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pin-out.

- Type 1630, intended for Socket 1, has two power pins allocated in the pinout that supports up to 1A continuous.
- Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and can support up to 2A continuous.
- The Socket 2 board types have five power pins in their pinout and can support up to 2.5A continuous.
- The Socket 3 board types, with a single Module Key, have nine power pins but can support up to 2.5A continuous.
- The four extra power pins enable reduced IR drop for these devices.

Table 39. Key Regulated Power Rail Parameters

Power Rail	Voltage Tolerance	Platform Rail Type
3.3 V	± 5%	Always On

The power rail voltage tolerance listed in Table 40 is ±5%. This is different from the ±9% tolerance allowed in the Mini Card specification.

Table 40. Power Rail Settling Time

Symbol	Parameter	Min	Max	Unit	Condition
T_{SETTLE}	Settling time of the 3.3V power rail		5	mS	1) Settle time from 0V to 3.135V. Should be achievable even with 330µF module load and 200mA Soft-Start current limit 2) In case 5mS settling cannot be met, PERST# de-assertion ('1'), must be at least 1mS AFTER the 3.3V supply is settled

Alternatively, and primarily for Tablet platforms, the 3.3 V regulated power rail can be replaced with a direct VBAT connection. In such a case, the module will need to produce any and all required voltages needed to support those modules and meet the Host I/F voltage levels defined in section 3.2. The current limit per pin of 500 mA/pin would still apply even if connected to VBAT. Note: the requirements in Table 41 only apply to Socket 2 WWAN-based module pinouts:

Table 41. Key VBAT Power Rail Parameters

Power Source	V_{MIN}	V_{MAX}	Cell Type
VBAT	3.135V	4.4V	One cell Li ion battery

The power rating of each M.2 module type is different based on the technology that is enabled and defined by the M.2 connector key. A list of connector keys and the power rating enabled for those keys is given in Table 42.

Table 42. Power Rating Table for the Various Modules and Connector Keys

Key	Power Rail	Voltage Tolerance	D0-D2, D3(Hot) Power		D3(Cold) Power	
			Peak mA Max Avg @ 100µS	**Normal mA** Max Avg @ 1S	**Peak mA** Max Avg @ 100µS	**Normal mA** Max Avg @1S
A	3.3V	±5%	2000		2000	
B	3.3V	±5%	2500		2500	
B	V_{BAT}	3.135V – 4.4V	2500		2500	
C	TBD	TBD	TBD	TBD	TBD	TBD
D	TBD	TBD	TBD	TBD	TBD	TBD
E	3.3V	±5%	2000		2000	
F	TBD	TBD	TBD	TBD	TBD	TBD
G	TBD	TBD	TBD	TBD	TBD	TBD
H	TBD	TBD	TBD	TBD	TBD	TBD
J	TBD	TBD	TBD	TBD	TBD	TBD
K	TBD	TBD	TBD	TBD	TBD	TBD
L	TBD	TBD	TBD	TBD	TBD	TBD
M	3.3V	±5%	2500		2500	
Peak – The maximum highest averaged current value over any 100-microsecond period Normal – The maximum highest averaged current value over any 1-second period						

The operation of the +3.3V power source shall conform to the PCI Bus Power Management Interface Specification and the Advanced Configuration and Power Interface (ACPI) Specification, except as otherwise specified by this document.

5

5. Platform Socket Pin-Out and Key Definitions

ALL PINOUT TABLES IN THIS SECTION ARE WRITTEN FROM THE PLATFORM/SYSTEM POINT OF VIEW WHEN REFERENCING SIGNAL DIRECTIONS.

In all pin outs, the Power Rail referred to in the M.2 connectors are the +3.3V rail unless otherwise indicated.

The M.2 pin outs are primarily intended to allocate specific pin functionalities that need to be routed on the Platform side to the respective Edge Card Slot Connector. Although many Host I/Fs are supported in the various pin-outs, it does not necessarily imply that all I/F need to be supported by the Add-In card/module at the same time. But the assigned allocations will enable each vendor and platform to design their circuits with the aligned pin assignment.

In some cases, multiple Host I/Fs and other signals are overlaid using the same pin assignment. In these cases, there are sense pins that clearly identify what assignment is supported by the Add-In card so that automatic multiplexing/routing would be possible on the platform.

A mechanical connector key/module key scheme is introduced to distinguish between different pinouts and functionalities because of the various connectorized pin-out assignments needed in support of the multiple add-in functions and to prevent wrongful insertions. However, all these connectors share the same basic connection scheme of a Gold Finger Edge Card that plugs into a slot connector mounted on the platform side. Connector mating can only occur when the Connector Key and Module key align to the same location.

The connector key/module key system used in conjunction with the M.2 75 position connector will enable up to 12 unique key locations and assignments. Different Keys are needed when the family of Host I/F differ significantly from each other in support of the different types of Sockets in a platform. Connector Keys are associated with the Socket Connector on Platform while Module Keys are associated with the Card Edge connection on the Module side.

The initial Key assignments are listed in Table 43.

Table 43. Mechanical Key Assignments

Key ID	Pin Location	Key Definition
A	8-15	Connectivity Version 1-DP
B	12-19	WWAN/SSD/Others Primary Key
C	16-23	Reserved for Future Use
D	20-27	Reserved for Future Use
E	24-31	Connectivity Version 1-SD
F	28-35	Future Memory Interface
G	39-46	Generic (Not used for M.2)
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	SSD 4 Lane PCIe

Note: Key ID assignment must be approved by the PCI-SIG. Unauthorized use of Key IDs would render this use as non-compliant to M.2 specifications.

5.1. Connectivity Socket; Socket 1

Connectivity Socket 1 will have two Key and Pinout variations in support of multiple Connectivity Add-In functions (such as WiFi+Bluetooth) along with some additional wireless solutions such as NGSS, NFC, or WiGig. The different Keys will support variations of the functional Host I/Fs as listed in Table 44.

Table 44. Socket 1 Versions

	Socket Version	
	Socket 2 – SD	**Socket 2 - DP**
Mechanical Key	E	A
WIFI	PCIe	
	SDIO	(1)
BT	USB	
	PCM/UART	(1)
WiGIG	PCIe	
	(1)	DP x4
NFC	I2C (or USB or UART(2))	
NFC Types	1630, 2230, 3030	2230, 3030

1 Not supported
2 Function to Host I/F allocation is a preferred example. Alternative function to Host I/F allocations are possible if using the Host I/Fs supported in the pin-out and in agreement between Customer ←→ Vendor

Because several of the interfaces listed in Table 44 have common signals located at the exact same pin locations with only the odd interfaces and mechanical keys trading places, we are able to create modules with a dual Module Key that can plug into two different Connector Keys

5.1.1. Socket 1-DP (Mechanical Key A) On Platform

- Socket 1-DP pinout Key A is intended to support Wireless Connectivity devices including combinations of WIFi, BT, NFC, and/or WiGig. Other Combos are possible provided they use the defined Host I/Fs in the pinout.
- PCIe Lane 0 is intended for use with the WiFi.
- PCIe Lane 1 is intended for use with the WiGig if the PCIe Lane 0 is not shared with the WiFi.
- Four Lane Display Port with assorted sideband signaling is also intended for use with the WiGig.
- LED#1 and W_DISABLE1# are intended for use with the WiFi and WiGig.
- USB and LED#2 are intended for use with the BT. There is only one W_DISABLE# supported by default. However, an adjacent Reserved pin (Pin 54) can be used alternatively as W_DISABLE2# for the BT.
- I2C and ALERT are intended for use with NFC.
- COEX can be used as needed by the different Wireless Comms. These COEX signals should be connected to the Socket 2 COEX signals for coexistence with the WWAN solution.
- Other Comm/Host I/F combinations are possible. Actual implementation needs to be defined agreed upon by Vendor←→Customer.

Table 45 provides a list of pin assignments on Socket 1 with mechanical key A.

Table 45. Socket 1-DP Pin-Out Diagram (Mechanical Key A) On Platform

74	3.3V	GND	75
72	3.3V	REFCLKN1	73
70	PEWake1# (IO)(0/3.3V)	REFCLKP1	71
68	CLKREQ1# (IO)(0/3.3V)	GND	69
66	PERST1# (O)(0/3.3V)	PERn1	67
64	RESERVED	PERp1	65
62	ALERT# (I)(0/3.3)	GND	63
60	I2C CLK (O)(0/3.3)	PETn1	61
58	I2C DATA (IO)(0/3.3)	PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKN0	49
46	COEX2(I/O)(0/1.8V)	REFCLKP0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	GND	PETn0	37
34	DP_ML0p	PETp0	35
32	DP_ML0n	GND	33
30	GND	DP_HPD (IO)(0/3.3V)	31
28	DP_ML1p	GND	29
26	DP_ML1n	DP_ML2p	27
24	GND	DP_ML2n	25
22	DP_AUXp	GND	23
20	DP_AUXn	DP_ML3p	21
18	GND	DP_ML3n	19
16	LED#2 (I)(OD)	MLDIR Sense (I)	17
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
6	LED#1 (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

5.1.2. Socket 1-SD (Mechanical Key E) On Platform

- Socket 1-SD pinout Key E is intended to support Wireless Connectivity devices including combinations of WIFi, BT, NFC, and/or GNSS. Other Combos are possible provided they use the defined Host I/Fs.
- PCIe Lane 0 or SDIO, LED#1, and W_DISABLE1# are intended for use with WiFi.
- USB or UART+PCM, LED#2 are intended for use with BT. There is only one W_DISABLE# supported by default. However, an adjacent Reserved pin (Pin 54) can be used alternatively as W_DISABLE2# for the BT.
- PCIe Lane 1 PET and PER are intended for future expansion in case a two Lane PCIe is needed (for example,. with WiGig Combo).
- I2C and ALERT# are intended for use with NFC.
- COEX can be used as needed by the different Wireless Comms. These COEX signals should be connected to Socket 2 COEX signals for coexistence with the WWAN solution.
- Other Comm/Host I/F combinations are possible. Actual implementation needs to be defined and agreed upon by Vendor←→Customer.

The pin assignments on socket 1 SD with mechanical key E are given in Table 46.

Table 46. Socket 1-SD Pin-Out Diagram (Mechanical Key E) On Platform

		GND	75
74	3.3V	RESERVED/REFCLKN1	73
72	3.3V	RESERVED/REFCLKP1	71
70	UIM_Power_In/GPIO1/PEWake1#	GND	69
68	UIM_Power_Out/CLKREQ1#	Reserved/PERn1	67
66	UIM_SWP/PERST1#	Reserved/PERp1	65
64	RESERVED	GND	63
62	ALERT# (I)(0/3.3)	Reserved/PETn1	61
60	I2C CLK (O)(0/3.3)	Reserved/PETp1	59
58	I2C DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(0/3.3V)	REFCLKN0	49
48	COEX1 (I/O)(0/1.8V)	REFCLKP0	47
46	COEX2(I/O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART RTS (O)(0/1.8V)	PETp0	35
34	UART CTS (I)(0/1.8V)	GND	33
32	UART Tx (O)(0/1.8V)	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	SDIO Reset(O)(0/1.8V)	23
22	UART Rx (I)(0/1.8V)	SDIO Wake(I)(0/1.8V)	21
20	UART Wake (I)(0/3.3V)	SDIO DAT3(IO)(0/1.8V)	19
18	GND	SDIO DAT2(IO)(0/1.8V)	17
16	LED#2 (I)(OD)	SDIO DAT1(IO)(0/1.8V)	15
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
10	PCM_SYNC/I2S WS (OI)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
8	PCM_CLK/I2S SCK (OI)(0/1.8V)	GND	7
6	LED#1 (I)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

5.1.3. Dual Module key Module: Supports Socket 1-SD and Socket 1-DP

In cases where the Connectivity type solutions adopt the Dual Module key scheme, where the solution use only PCIe, USB, and I2C host interfaces, they can be inserted into the both Socket 1-DP and Socket 1-SD.

See Table 25, *Socket 1 Module Pinout with Dual Module Key (A-E)* for an example of a Module-side pinout that makes use of the Double Module key option.

5.2. WWAN+GNSS/SSD/Other Socket; Socket 2

Socket 2 has a single Key (Mechanical Key B) to support various WWAN+GNSS (Global Navigation Satellite System that may include GPS, GLONASS and/or Galileo), various SSD, and other Add-In functions. This is done by Overlaying functional pins that can be identified with the aid of Configuration pins and/or having functional pins at different pin allocations in the pin-out.

Socket 2 is primarily targeted for board types 2230, 2242, 3042, 2260, 2280, and 22110 board sizes.

5.2.1. Socket 2 – Configuration Pin Definitions

The Socket 2 Key (Mechanical Key B) is unique in that it enables five major pinout configurations and four variants for each of the three WWAN configurations. The five major configurations supported are:

- ❑ WWAN that is PCIe Based
- ❑ WWAN that is SSIC Based
- ❑ WWAN that is USB3.0 Based
- ❑ SSD that is PCIe (2 lane) Based
- ❑ SSD that is SATA Based

All Socket 2 WWAN pinout configurations (1, 2, and 3) support USB2.0 and USB HS with the generic USB_D± pins as a baseline. All three have four alternate functional pins, with the aid of eight GPIO pin allocations, in support of various secondary functions such as GNSS interface and coexistence pins, second UIM support, Audio support, and Reserved for Future Use pins.

The Platform must read all four Configuration pins so it can clearly identify which unique configurations needed to be supported. The platform can also identify when no module is plugged into the slot.

It is mandatory that the Module side maintain the Configuration Pin states correctly to enable interoperability between the systems that make use and do not make use of these Indication Pins.

The Configuration Pins are:

- Pin 21 – CONFIG_0
- Pin 69 – CONFIG_1
- Pin 75 – CONFIG_2
- Pin 1 – CONFIG_3

In order for the platform to read these Configuration bits, it must pull-up these four pins to an appropriate power rail. If designed properly, these configuration bits can be read even if the Module is not powered up.

Table 47 shows all the variant configurations as a function of the configuration bits. The platform can then adjust its' host interface connection and support signal connections to the proper setting to work with the Module.

Table 47. Socket 2 Module Configuration Table

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - USB 3.0	0
0	1	0	1	WWAN - USB 3.0	1
0	0	1	1	WWAN - USB 3.0	2
0	1	1	1	WWAN - USB 3.0	3
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
1	0	1	1	RFU	N/A
1	1	1	1	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations
[2] Applicable to WWAN only

The four configuration pins listed in Table 52 need to be set to Not Connected (NC) or Ground (GND) on the Add-In Module side according to Table 34. By sensing and decoding these pins the platform can configure the pin-out configuration and functionality.

5.2.2. Socket 2 Pin-Out (Mechanical Key B) On Platform

- Socket 2 pinout is intended to support WWAN+GNSS, SSD, and Other types of Add-In solutions with the defined and configurable Host I/Fs.
- WWAN can make use of USB2.0, USB3.0, PCIe (up to two Lanes), or SSIC host I/Fs. The actual implemented I/F is identified through the Configuration pins state (1 of 16 states) on the Module side. LED#1 and W_DISABLE1# are intended for use with the WWAN solution. There are additional Optional WWAN and GNSS related pins including W_DISABLE2#, DPR, and WAKE_ON_WWAN#
- The UIM and SIM Detect pin are used in conjunction with a SIM device in support of the WWAN solution.
- The COEX and ANTCTL pins are placeholders for future expansion and definition of these functions.
- The GPIO0..7 pins are configurable with four different variants. These variants can be in support of the GNSS interface and coexistence, second UIM/SIM, and Audio interfaces. The exact definition is determined by which configuration was identified by decoding the four Configuration pins.
- The FULL_CARD_POWER_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into platforms that provide a direct connection to $V_{\mathbf{BATT}}$ (and not a regulated 3.3 V) such as Tablet platforms. They are not used in NB and Very thin notebooks type platforms that provide a regulated 3.3 V power rail. But the Full_Card_Power_Off# signals should be tied to the 3.3V power rail on the NB/very thin platform.
- The SSD can make use of the PCIe two Lanes or overlaid SATA host I/F. The actual implemented I/F is identified through the CONFIG_1 pin state (1 or 0) in conjunction with the other three Configuration pin states that are all 0. DAS/DSS#1 (overlaid on the LED#1) and DEVSLP are intended for use with the SSD solution.
- The SUSCLK pin provides a Slow Clock signal of 32 kHz to enable Low Power States.
- Pins labeled NC should Not Be Connected.

Table 48 lists the pinout for Socket 2 (mechanical key B).

Table 48. Socket 2 Pinout Diagram (Mechanical Key B)

74	3.3V	CONFIG_2	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	CONFIG_1	69
66	SIM Detect (O)	Reset# (O)(0/1.8V)	67
64	COEX1 (I/O)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
62	COEX2(I/O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
60	COEX3(I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
58	N/C	ANTCTL0 (I)(0/1.8V)	59
56	N/C	GND	57
54	PEWake# (IO)(0/3.3V)	REFCLKP	55
52	CLKREQ# (IO)(0/3.3V)	REFCLKN	53
50	PERST# (O)(0/3.3V)	GND	51
48	GPIO_4 (IO)(0/1.8V*)	PETp0/SATA-A+	49
46	GPIO_3 (IO)(0/1.8V*)	PETn0/SATA-A-	47
44	GPIO_2 (IO)(0/1.8V*)	GND	45
42	GPIO_1 (IO)(0/1.8V*)	PERp0/SATA-B-	43
40	GPIO_0 (IO)(0/1.8V*)	PERn0/SATA-B+	41
38	DEVSLP (O)(0/3.3V)	GND	39
36	UIM-PWR (I)	PETp1/USB3.0-Tx+/SSIC-TxP	37
34	UIM-DATA (IO)	PETn1/USB3.0-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3.0-Rx+/SSIC-RxP	31
28	GPIO_8 (IO) (0/1.8V)	PERn1/USB3.0-Rx-/SSIC-RxN	29
26	GPIO_10 (IO) (0/1.8V)	GND	27
24	GPIO_7 (IO) (0/1.8V)	GPIO_12 (IO) (0/1.8V)	25
22	GPIO_6 (IO)(0/1.8V)	GPIO_11 (IO) (0/1.8V)	23
20	GPIO_5 (IO)(0/1.8V)	CONFIG_0	21
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
10	GPIO_9/DAS/DSS# (I)(OD)	GND	11
8	W_DISABLE#1 (O)(0/3.3V)	USB_D-	9
6	Full_Card_Power_Off# (O)(0/1.8V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	GND	3
		CONFIG_3	1

5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinout and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (67) will indicate to the platform which I/F of these two is actually connected.

Table 49. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET (NC-PCIe/GND-SATA)	69
68	SUSCLK(32kHz) (O)(0/3.3V)	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWake# (IO)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)(0/3.3V)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I)(OD)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

Although the pinout in Table 49 allocates four additional 3.3 V power pins, it is not intended to increase the current sinking capability of the Module. The intention is to further reduce the IR drop of the power under extreme high current cases and increase the robustness of the SSD devices. The maximum power consumption of this socket remains as identified in section 3.3, *SSD Socket 3 System Interface Signals*. This Socket will also accept SSD devices that employ a Dual Module key on Module scheme.

5.4. Soldered Down Pinout Definitions

The soldered-down pinout definitions are shown in the following figures:

- Figure 91, Type 2226 LGA Pin-Out Using Socket 1-SD Based Pin-Out on Platform
- Figure 92, Type 1216 LGA Pin-Out Using Socket 1-SD Based Pin-Out on Platform
- Figure 93, Type 3026 LGA Pin-Out Using Socket 1-SD & 1-DP Based Pin-Out on Platform

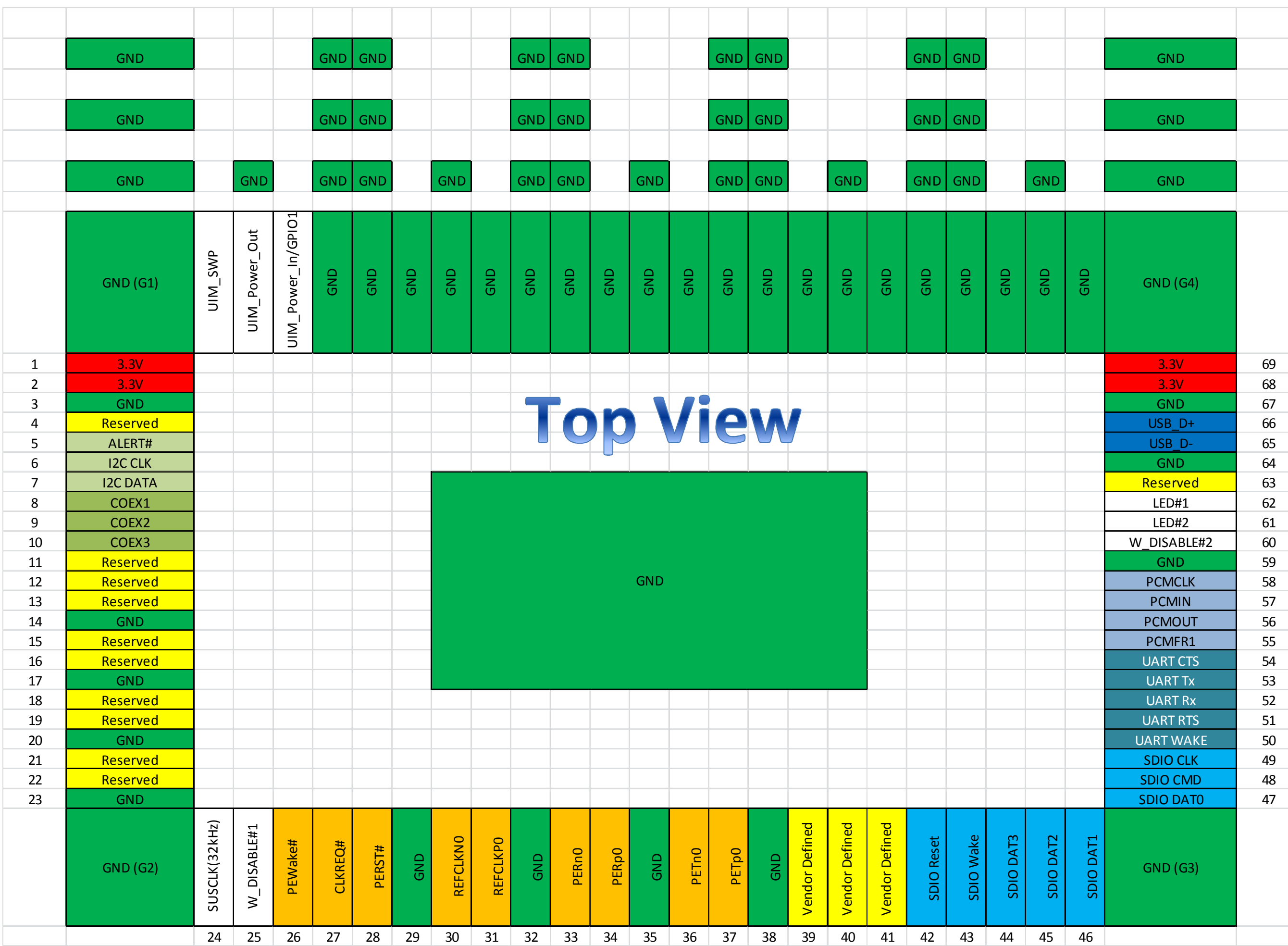


Figure 91. Type 2226 LGA Pin-Out Using Socket 1-SD Based Pin-Out on Platform

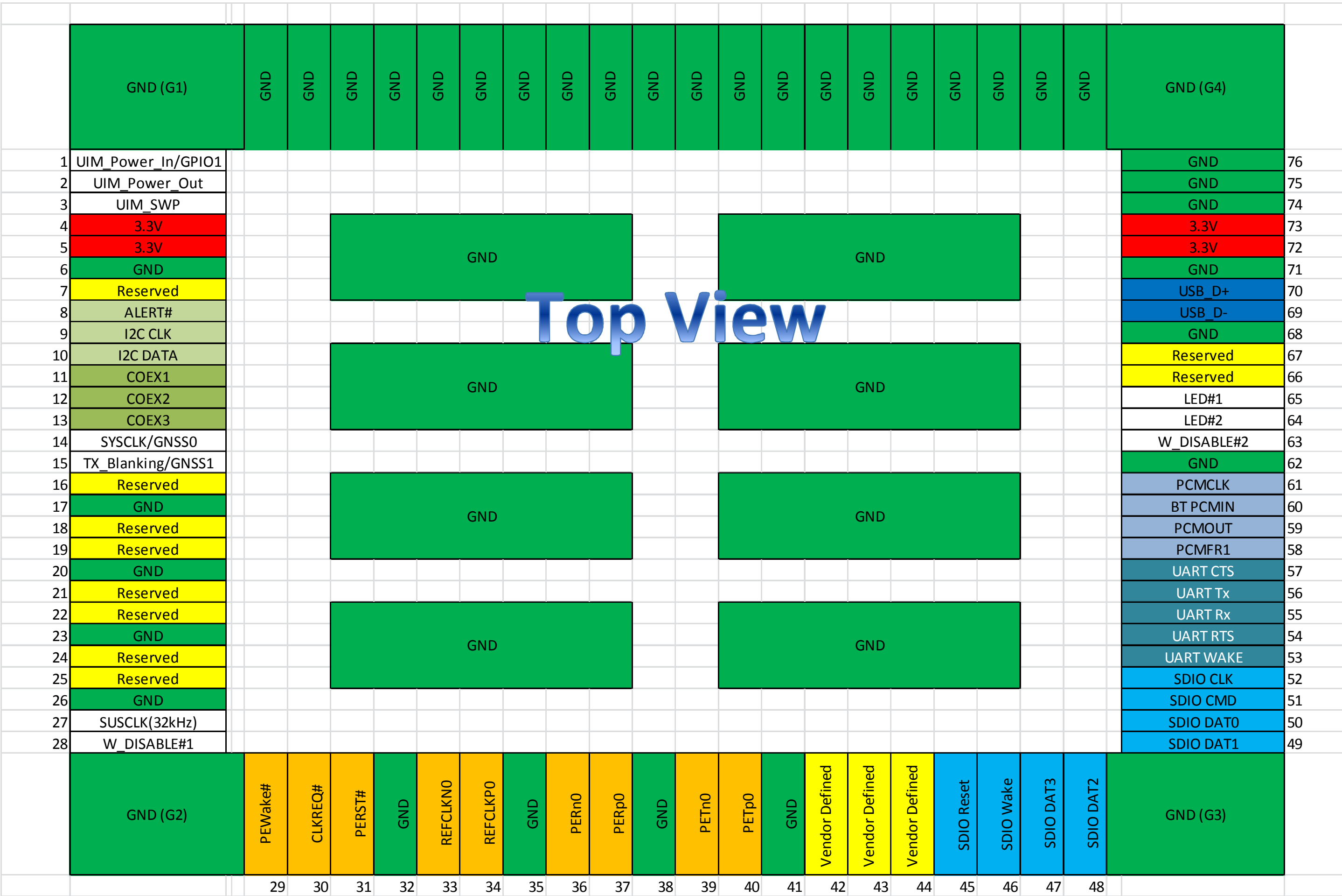


Figure 92. Type 1216 LGA Pin-Out Using Socket 1-SD Based Pin-Out on Platform

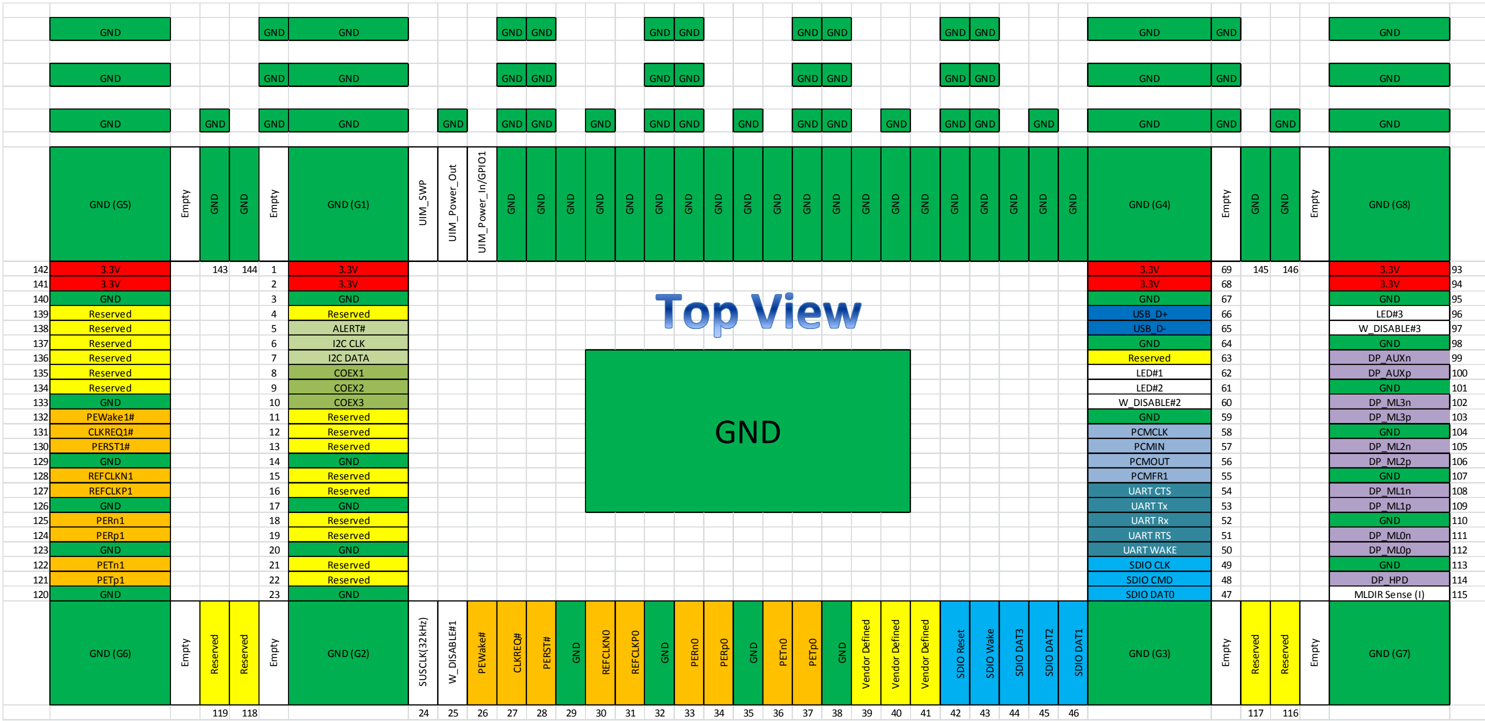


Figure 93. Type 3026 LGA Pin-Out Using Socket 1-SD & 1-DP Based Pin-Out on Platform

6

6. Annex

6.1. Glossary

A	Amperage or Amp	**SATA**	Serial Advanced Technology Attachment or Serial ATA
DC	Direct Current	**PCIe**	Peripheral Component Interconnect Express
GND	Ground	**PCM**	Pulse Code Modulation
GNSS	Global Navigation Satellite System (GPS+GLONASS)	**SDIO**	Secure Digital Input Output
HDR	Hybrid Digital Radio	**SIM**	Subscriber Identity Module
HSIC	High Speed Inter-Chip	**SSD**	Sold-State Storage Device
I/F	Interface	**SSIC**	Super Speed USB Inter-Chip
I/O	Input/Output	**RF**	Radio Frequency
IR	Current x Resistance = Voltage	**RM**	Root Mean Square
I^2C	Inter-Integrated Circuit	**RoHS**	Restriction of Hazardous Substances Directive
I2S	Integrated Interchip Sound	**RTC**	Real Time Clock
LED	Light Emitting Diode	**RFU**	Reserved for Future Use
LGA	Land Grid Array	**UIM**	User Identity Module
mΩ	milli Ohm	**USB**	Universal Serial Bus
mA	milli Amp	**UART**	Universal Asynchronous Receive Transmit
mV	milli Volt	**W**	Wattage or Watts
NFC	Near Field Communications	**WiGig**	Wireless Giga communication
M.2	Formally called Next Generation Form Factor (NGFF)	**WLAN**	Wireless Local Area Network
NB	Notebook	**WPAN**	Wireless Personal Area Network
NIC	Network Interface Card	**WWAN**	Wireless Wide Area Network
NC	Not Connected	**V**	Voltage

6.2. M.2 Signal Directions

This section describes the directionality of some of the interface signals incorporated in the various pinouts. Because some signals have directionality associated with them, their names and locations may be different between the Platform side and the Module side.

The Module pinouts are described in Chapter 3 and Platform pinouts are described in Chapter 5.

The main differences between Platform-side pinouts and Module-side pinouts are shown in Figure 95 and Figure 96.

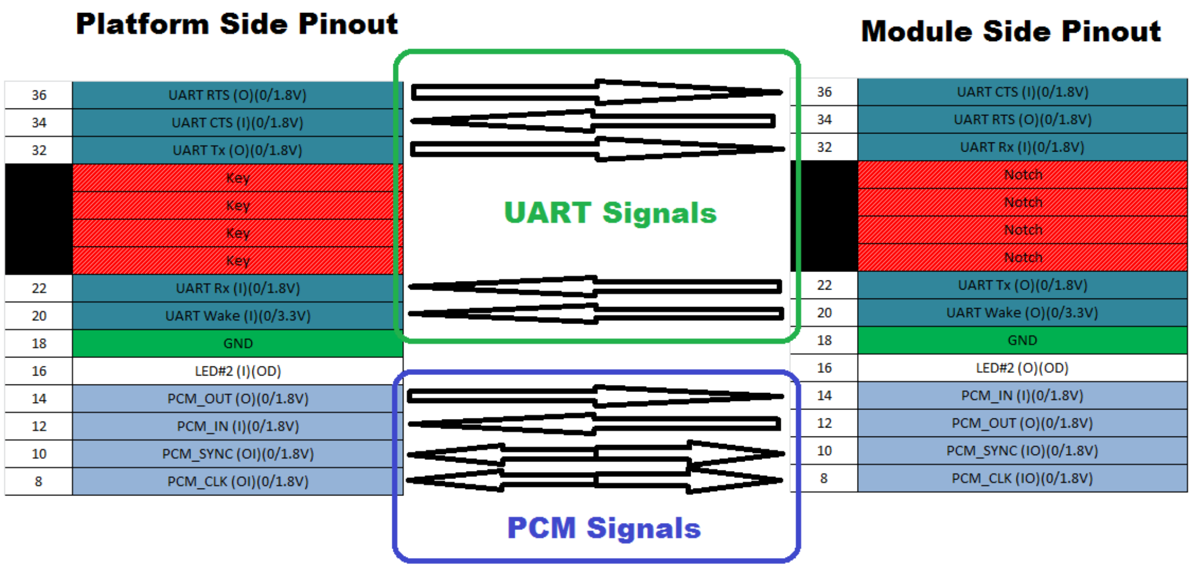


Figure 94. UART and PCM Signal Direction and Signal Name Changes

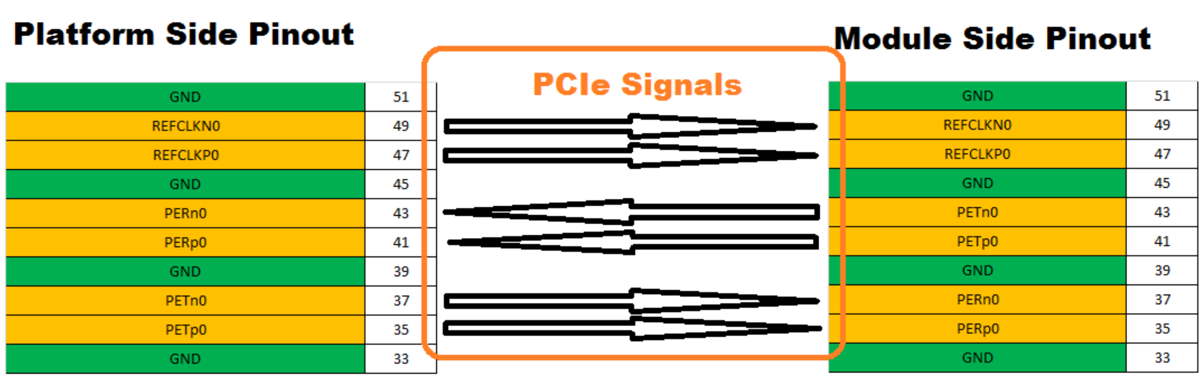


Figure 95. PCIe Signal Direction and Signal Name Changes

Figure 94 and Figure 95 are examples of signaling directions and name changes from platform to module. Other cases exist for other signals in various Sockets, such as the USB3.0 Tx and Rx, SSIC_Tx and SSIC_Rx.

6.3. Signal Integrity Guideline

Table 50 provides the signal integrity requirements for the M.2 module.

Table 50. Signal Integrity Parameters

Parameter	Requirement	Notes
Differential Impedance	75 - 95 Ω measured @ 50 ps rise time (20-80%)	1
Differential Insertion Loss (DDIL)	≥ -0.5 dB up to 4 GHz and then ≥ -1 dB up to 8 GHz	1, 2
Differential Near End Crosstalk (DDNEXT)	≤ -36 dB up to 4 GHz and then ≤ -32 dB up to 8 GHz	1, 2, 3
Differential Far End Crosstalk (DDFEXT)	≤ -40 dB up to 4 GHz and then ≤ -32 dB up to 8 GHz	1, 2, 3
1 Mated connector and module including solder pad and gold finger 2 The result shall be referenced to 85 Ω differential impedance 3 The crosstalk shall be pair-to-pair between any two differential pairs		

Figure 96, Figure 97, and Figure 98 show the recommended pad and anti-pad guideline for Signal Integrity modeling.

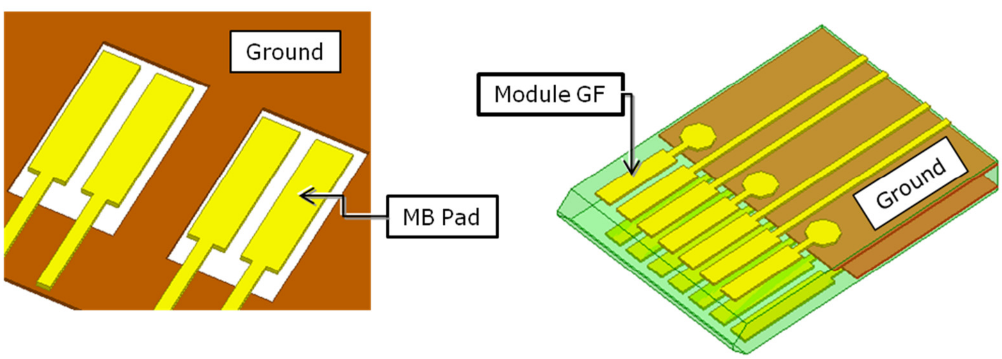


Figure 96. Suggested Motherboard and Module Board Signals and Ground Pad Layout Guideline

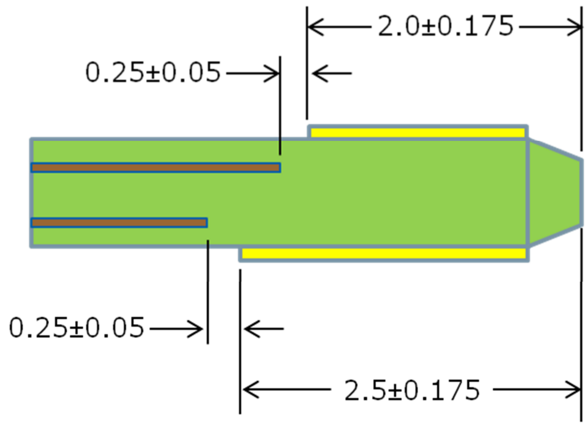


Figure 97. Suggested Ground Void for Module Simulation

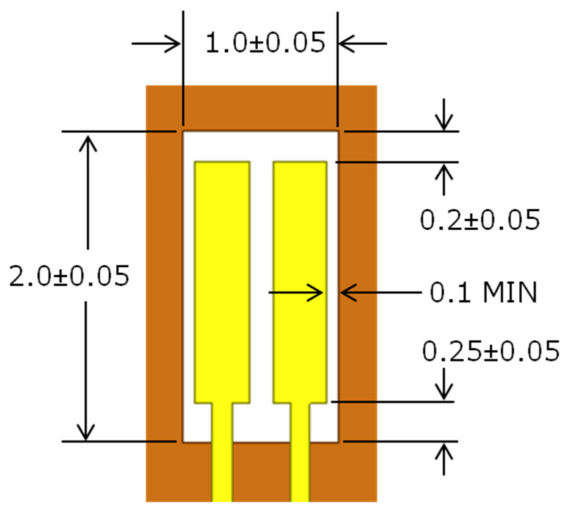


Figure 98. Suggest Ground Void for Main Board

6.3.1. Suggested Signal Integrity PCB Layout

Placeholder for a board layout drawing

6.4. VSWR Test Set-up Method for RF Connector Receptacles

Measure the VSWR of the receptacle as shown in Figure 99 with the aid of a Network Analyzer. Measure between 100 MHz and 6 GHz or alternatively for the optional enhanced connector from 100 MHz and 12 GHz.

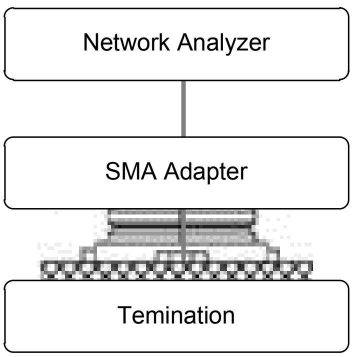


Figure 99. VSWR Test Setup for Receptacle RF Connector

6.5. Thermal Guideline Annex

This section details examples of module and system skin (casing) thermal response to thermal and dissipation boundary conditions in systems. The boundary conditions vary by system, as do the skin temperature limits.

6.5.1. Assumptions

6.5.1.1. Die Thermal Dissipation Overview

Assumptions for typical components and dissipation for several module types are given in Table 51. Keep in mind the definition of thermal design power (TDP) given above. Note that the maxima given here do not necessarily correspond to their actual use in a system; these values are, from the die perspective, what they would dissipate when running all the time at their maximum capacity. The system use case scenarios make assumptions about how much of the time the devices would run and scale the dissipation accordingly. The thermal design power therefore is different from the thermal dissipation given in Table 52.

Table 51. Assumptions for Typical Components and Dissipation

Module Type	Die #	Function	Thermal Dissipation Estimates	Module Total Dissipation (Not Necessarily TDP)	Power Allocation	Power Map
WiFi/BT	1	WiFi/BT	2	2	100%	WiFi/BT
WWAN	1	Baseband	1.2	1.9 Typical 3.25 Worst	32%	Uniform
	2	Power Mgmt			14%	
	3	RF Transceiver	0.4		11%	
	4	PA	0.3 Typ / 1.65 Worst		43%	
SSD	1	ASIC	1.5	1.74	86%	Uniform
	2	DRAM	0.05		3%	
	3	NAND1	0.03 Typ / 0.25 Worst		2%	
	4	NAND2	0.03 Typ / 0.25 Worst		2%	
	5	NAND3	0.03 Typ / 0.25 Worst		2%	
	6	NAND4	0.03 Typ / 0.25 Worst		2%	
	7	POWER	0.07		4%	
WiGig	1	WiFi/BT	2	3	67%	WiFi/BT
	2	WiGig	1		33%	WiFi no BT

Note: For comparison, maximum dissipations for WWAN components can vary by technology, and are shown below. Most of these are in the 3 W range

For comparison, maximum dissipations for WWAN components can vary by technology, and are shown in Table 52. Most of these are in the 3 W range.

Table 52. Maximum Dissipation for WWAN Modules

WWAN Technology	Maximum Dissipation, W (not necessarily Thermal Design Power)
W-CDMA HSDPA 1900 @ 22 dBm	3.0 ± 0.1
W-CDMA HSDPA 850 @ 22 dBm	2.9 ± 0.1
W-CDMA HSDPA 2100 @ 22 dBm	2.7
CDMA 1xEVDO @ 24 dBm	2.8 ± 0.1
GPRS Class 10 @ 32 dBm	1.8
LTE @ 22 dBm	3.1 ± 0.1

6.5.1.2. Component Overview

Generic assumptions for package designations and types expected to populate modules are listed in Table 53.

Table 53. Generic Assumptions for Package Designations and Types Expected to Populate Modules

Type	Layers	Function	Die #	Type	Package	Package Size	Die Size	Via Array	Via Pitch
2230	4 1 oz	WiFi/BT	1	WiFi/BT	QFN	9x9	6x6	6x6	1
3042	8 1 oz	WWAN	1	Baseband	PBGA	10x10	5.5x5.5	4x4	1.27
			2	Power Mgmt	PBGA	4x4	2x2	2x2	1.27
			3	RF Transceiver	PBGA	5x5	3x3	2x2	1.27
			4	PA	LGA	5x7	1.3x2	2x6	1
2280 Double Sided	6 1 oz	SSD	1	ASIC	BGA	20x20	12x12	9x9	1.27
			2	DRAM	BGA	11x10	7x7		
			3	NAND1	BGA	15x18	10x12		
			4	NAND2	BGA	15x18	10x12		
			5	NAND3	BGA	15x18	10x12		
			6	NAND4	BGA	15x18	10x12		
			7	POWER	DFN	6x5	4.125x3.75		
3030	6 1 oz	WiFi/BT + WiGig	1	WiFi/BT	QFN	9x9	6x6	6x6	1
			2	WiGig	PBGA	9x9	6x6	4x4	1.27

6.5.2. Generic System Environment Categories (Assumptions)

Table 54 gives assumptions for each generic system environment. These are meant to be slightly aggressive targets at the time of writing.

Table 54. Assumptions for Generic System Environments

Type	Notebook		Thin Platform Notebook With Fan		Tablet Fanless	Units
Case Size	325x225		325x225 (14”?)		250x170	
Total /Base Thickness	28/18		15/10		8	mm
Case Material	Resin		Mg		Mg	
Case Thickness	1.1		0.8		0.8	mm
Case Exterior Emissivity	High		High		High	
Case Interior Emissivity	High		Low		Low	
External Ambient	25	35*	25	35*	25	°C
Skin T Limit Top (“Forehead”)	37	55	37	46	40 (display)	°C
Skin T Limit Bottom	48	58	42	46	38	°C
Gap Module to Case	> 2		> 1		< 0.5	mm
Motherboard Size	180x83x1.2		180x83x1		140x45x0.9	mm
Module Orientation	Table		Table		Back	
Inlet Vent Area	30x30 + 83x16 + 2 edge vents 20x2.5		60x30 + 2 edge vents 20x5		N/A	
Outlet Vent Area	60x10 grille		60x10 grille		N/A	mm
Fan Flow Rate	2.4 cfm 68 l/min		0.6 cfm 17 l/min		N/A	

* Shown for example purposes only

6.5.2.1. Module Slot Definitions by System

The following assumptions apply to the results and discussions of the examples in this document.

- 25 °C ambient is assumed for skin temperature compliance
- Socket 1 = WiFi/BT OR WiFi/WiGig
- Socket 2 = WWAN
- Socket 3 if present = SSD
- WiFi/BT and WWAN operation are **mutually exclusive**, i.e. the system is connected to one or the other, but not both
- If socket 3 is present, socket 2 is WWAN
- Skin temperature limits are OEM dependent and sometimes market sector dependent
- Global skin temperature levels are system dependent (heat exchanger design, fan flow rate, board layout, system TDP distribution)
- Local skin temperatures and module TDP values are given assuming no special thermal management techniques have been applied to either the module or the nearby casing
- Thermally advantageous placement of modules is assumed

6.5.2.1.1. Systems with Fans

Table 55. Slot Definitions, Systems with Fans

	Notebook		Thin Platform Notebook With Fan		
Socket #	1	2	1	2	3
Module Size	2230	3042	3030	3042	2280
Function	WiFi/BT	WWAN	WiFi/BT + WiGig	WWAN	SSD

6.5.2.1.2. Systems without Fans

Table 56. Slot Definitions, Systems without Fans

	Tablet	
Scenario		
Socket #	1	2
Module Size	2230	3042
Function	WiFi/BT	WWAN LTE

6.5.3. Assessing Thermal Design Power Capability

6.5.3.1. Use Cases

Assumptions for the distribution of thermal dissipation throughout the system are needed for each system type. These are known as "use cases" and are established by defining a scenario for what the user is asking the system to do. In many cases, there are simultaneous active applications taxing different areas of the system. The use cases in this document are intended for illustration only; an analogous process should be carried out by system designers for each system.

6.5.3.2. Extended Use Cases

To evaluate system and module response to TDP variations, a use case baseline is established, and the module dissipation varied around the nominal value for the use case. In this document, the "extended use case" (the use case plus a higher dissipation for the module in question) is analyzed for skin temperature response. Hypothetical example systems are modeled with use cases relevant to dissipation in the modules. The module dissipation is varied over the range 0 – use case TDP – 3 W to obtain the sensitivity of skin temperature to module dissipation.

6.5.3.3. Unpowered Module

For module designers, the use cases are valuable background to establishing potential module environments. Particularly helpful for them should be the system skin and module temperatures when there is an **unpowered** module, which is meant to give an idea of the starting point for any thermal excursion due to the module's own power.

6.5.3.4. Use Case Flexibility

It is worthwhile to note that in some instances, the stated assumptions about use case do not result in a system that meets its specifications. Including power management features in the module components will give system designers maximum flexibility to manage power dissipation. This flexibility can be applied to many of the system's components to meet specifications. It should be noted again that for skin temperature limits, the time scale of interest is of the order of several minutes, while the time scale for many system tasks is much shorter.

Most business applications enable the wireless communications modules to go dormant, thereby lowering the average thermal dissipation. Applications that perform data streaming such as VOIP, video streaming from an attached camera or streaming audio prevent the communications modules from going dormant. The host should support the USB Selective Suspend feature to reduce electrical power consumption and thermal dissipation by the wireless modules.

6.5.4. Module Placement Advice

Lowest skin temperatures will be achieved when the heat sources are distributed over the largest possible area. This implies that, within reason, the modules should be located away from areas of concentrated heat on the motherboard, and also as far as possible from any heat exchanger.

For systems with fans, place inlet vents near modules to flush the inside surface of the casing, and use the bottom vent to act as a thermal break if needed.

Address global hot spots via general system layout and use case assumptions.

6.5.5. Skin Temperature Sensitivity to Module Power

Skin temperatures in the vicinity of modules will depend on the module power and the total system power and its arrangement. Systems with low flow rates will have higher sensitivity than systems with higher flow rates. Systems without ventilation are most sensitive, up to 3 °C skin temperature increase per Watt of module power in the example systems shown in the Appendix. This value may not be generally applicable – thermal studies should be carried out at the system level.

6.5.6. General Applicability

The examples shown in section 6.5.8, Examples, are not intended to be generally applicable. They are only meant to show the potential range of responses, and to determine sensible advice for module placement and other approaches to thermal management. The TDP response has to be established by the design team for each system design. Thermal analysis by computational and physical (experimental) modeling is strongly encouraged at the system level.

6.5.7. Generic assumptions for module arrangement

Modules may represent a significant portion of the total system dissipation and may be a major contributor to system skin temperature. It is a good idea to place them in thermally advantageous locations. Examples shown throughout this document indicate such thermally advantageous placements, but of course are only meant to show the possibilities, and do not represent actual final designs. Nor have all the model assumptions been completely tested, so the accuracy of any predictions is within several degrees at best.

For systems with fans, vents upstream help to cool both the module and the nearby casing to minimize skin temperature. They may also have a "thermal break" effect, protecting the local surface near the modules from the larger global maximum surface temperature.

For systems without fans, concentrations of high heat density should be avoided as a matter of course, since the thin metal skin can achieve only a limited level of heat spreading. In addition, it is well known that placing heat sources near edges or corners of a heat spreader cause higher temperatures than placing them in a central location on the spreader.

6.5.8. Examples

6.5.8.1. Notebook Category

Many assumptions are used in this document. Table 57 lists examples of cases applicable to modules for notebooks.

Table 57. Example Use Case Applicable to Modules for Notebooks

Component	Thermal Design Power (W)
Scenario	Comms Excursion
Application Mix	Local Network (WiFi) File Transfer+ Device (BT) File Copy+ Netflix (Chrome) 1080p [+WiDi]
Motherboard CPU	26
MB VR, chipset, etc	8.2
Memory	1.5
HDD+SSD Cache	1.1
HDD	0.1
SSD Cache	1.0
Comms: WLAN/BT	2.2
Comms: WWAN	0
ODD	.1
Fan	0.9
Platform Total	40

6.5.8.1.1. Generic Motherboard Assumptions

The bottom view of a single-sided motherboard (all components facing the table within the system) with a thermal solution applied to CPU is shown in Figure 100. The modules are installed in top mount connectors at one edge of the board, as far from the CPU as possible. There are several memory modules and two areas of clustered small heat sources, each shown as a rectangular heated area. The motherboard heat sources form a thermal boundary condition for the modules.

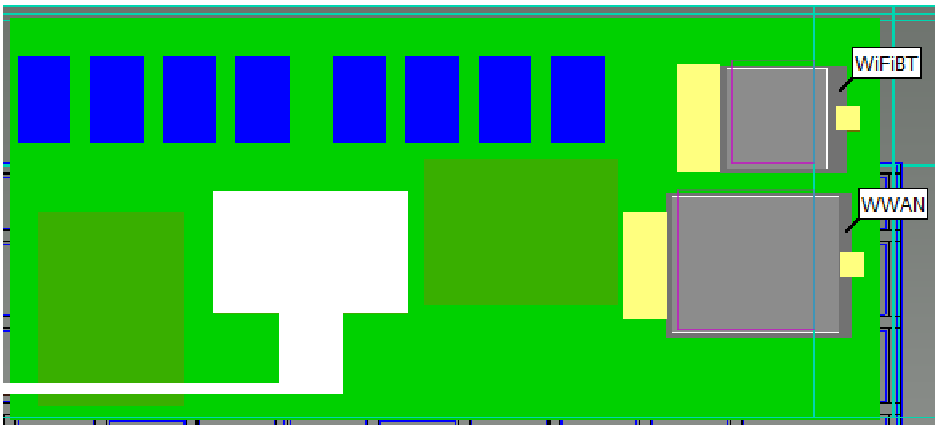


Figure 100. Example View of Notebook Motherboard

6.5.8.1.2. System Layout Assumptions

Flow related assumptions include a fan at 2.4 cfm/68 l/min, a vent opening near the cards, and small slot vents in the system's side (Figure 101 shows edge vents and Figure 102 shows bottom vents).

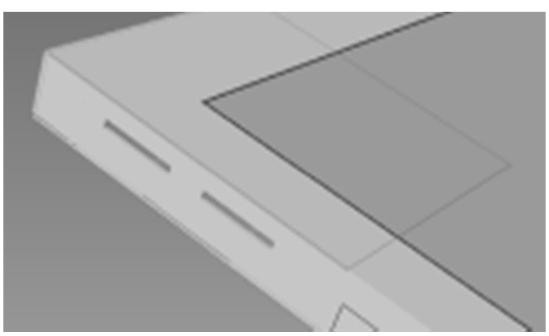


Figure 101. Example View of Edge Vents

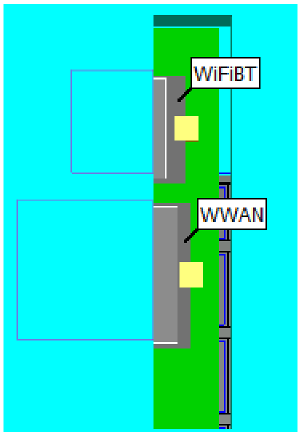


Figure 102. Example View of Bottom Vents

6.5.8.1.3. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. For a notebook system, the global maximum is likely to be near the heat exchanger and fan exhaust. The temperature in this region is only very slightly dependent on the module dissipation, as in this system category the module makes up a relatively small fraction of the total system TDP.

Local maxima are trickier to identify if they are lower than the global maximum. For the purposes of the examples shown in Figure 103 and Figure 104, a region of interest is defined in the vicinity of the modules, and the region maximum obtained. Another method might be to track a single consistent point over each module.

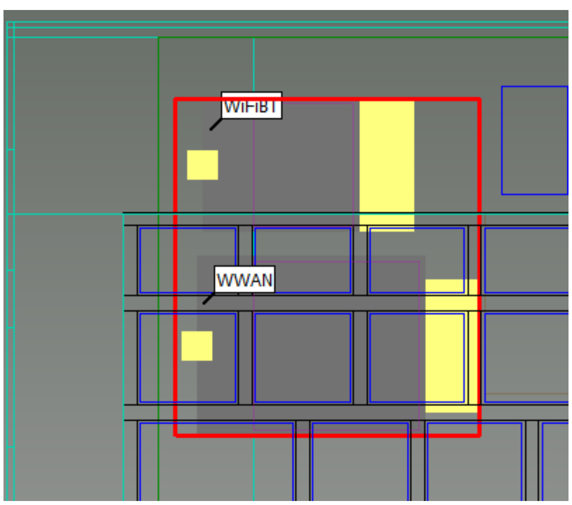


Figure 103. Example View of Region Over Modules

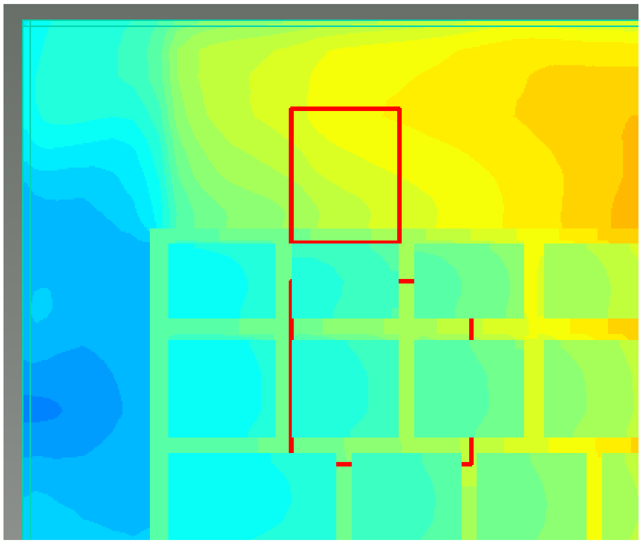


Figure 104. Example View of Hot Spot Over Modules

6.5.8.1.4. Thermal Design Power Response – Notebook Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to 3 W in the use case. Results are shown in Table 58, Table 59, and Table 60. Temperatures are rounded to the nearest whole degree.

Note that the table distinguishes between local skin temperature (directly over or under the module) and a global skin hot spot, caused by the remainder of the system and use case, sometimes even in the absence of any module dissipation. Although the modules do not heat the skin excessively, the system designer will have to consider changes in the use case and/or the design to meet skin temperature requirements.

Also note that with so many assumptions in each analysis, the results shown in the table are not intended as accurate predictions, but only to provide guidance about sensible system design for module effects on skin temperature. The particulars of the keyboard model especially determine the skin temperature of modules below the keyboard area.

Table 58. Thermal Design Power Response – Notebook Category

	Notebook	
Socket #	1	2
Module Size	2230	3042
Function	WiFi/BT	WWAN
Use case	Comms Exc	Comms Exc WWAN
System Dissipation W/O Module	37.8	37.8
Module Off	0 W	0 W
Mean Card T	32	34
Local Skin T Top	30	28
Local Skin T Bottom	28	30
Global Skin Hot Spot (HX)	47	47
Use Case TDP	2.2 W	2.2 W
Local Skin T Top	31	28
Local Skin T Bottom	30	31
Global Skin Hot Spot (HX)	47	47
Extended Case TDP	3 W	3 W
Local Skin T Top	31	29
Local Skin T Bottom	31	31
Fan Flow Rate, CFM	2.4	2.4

Table 59. Skin Temperature Limit Assumptions, Notebook

Ext Ambient	25
Skin T Limit Top	37
Skin T Limit Bottom	48

Table 60. Skin Temperature Effect of Module Position

Modules Switched Places	Notebook	
Socket #	1	2
Module Size	3042	2230
Function	WWAN	WiFi/BT
Use Case	Comms exc WWAN	Comms exc
Use Case TDP	2.2 W	2.2 W
Local Skin T Top	28	31
Local Skin T Bottom	31	30

6.5.8.2. Thin Platform Notebook with Fan Category

Many assumptions are used in this document.

Table 61. Use Cases Applicable to Modules for Thin Platform Notebook with Fan

Component	Thermal Design Power (W) by Scenario	
Scenario	PCH Excursion	Comms Excursion
Application Mix	Skype+ Windows Media Player+ OS File Transfers+ SS Storage File Copy	Local Network (WiFi) File Transfer+ Device (BT) File Copy+ Netflix(Chrome) 1080p [+WiDi]
Motherboard CPU + Chipset	13.5	12.8
Motherboard Distributed	4.2	3.7
Memory	1.5	1.5
SSD	2.4	0.5
Comms :WLAN/BT or WWAN	0.9	1.4
Platform Total	23.4	20.8

6.5.8.2.1. Generic motherboard assumptions

The bottom view of a single-sided motherboard (all components facing the table within the system) with thermal solution applied to CPU is shown in Figure 105. The cards are installed in mid plane connectors at one edge of the board, as far from the CPU as possible. There are several memory modules and two areas of clustered small heat sources, each shown as a rectangular heated area. The motherboard heat sources form a thermal boundary condition for the modules.

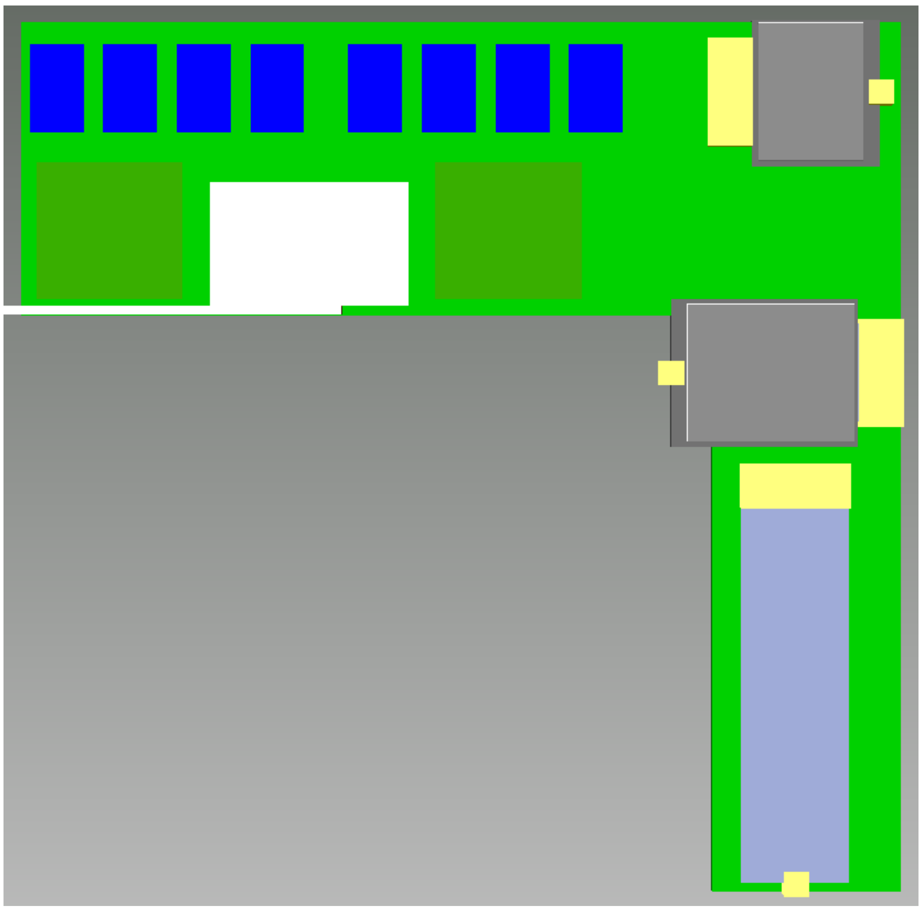


Figure 105. Example View of Motherboard for Thin Platform Notebook with fan

6.5.8.2.2. System Layout Assumptions

Flow related assumptions include a fan at 0.6 cfm/17 l/min, a vent opening below the modules, and small slot vents in the system's side (Figure 106). The vent opening below the cards can reduce the local surface temperature.

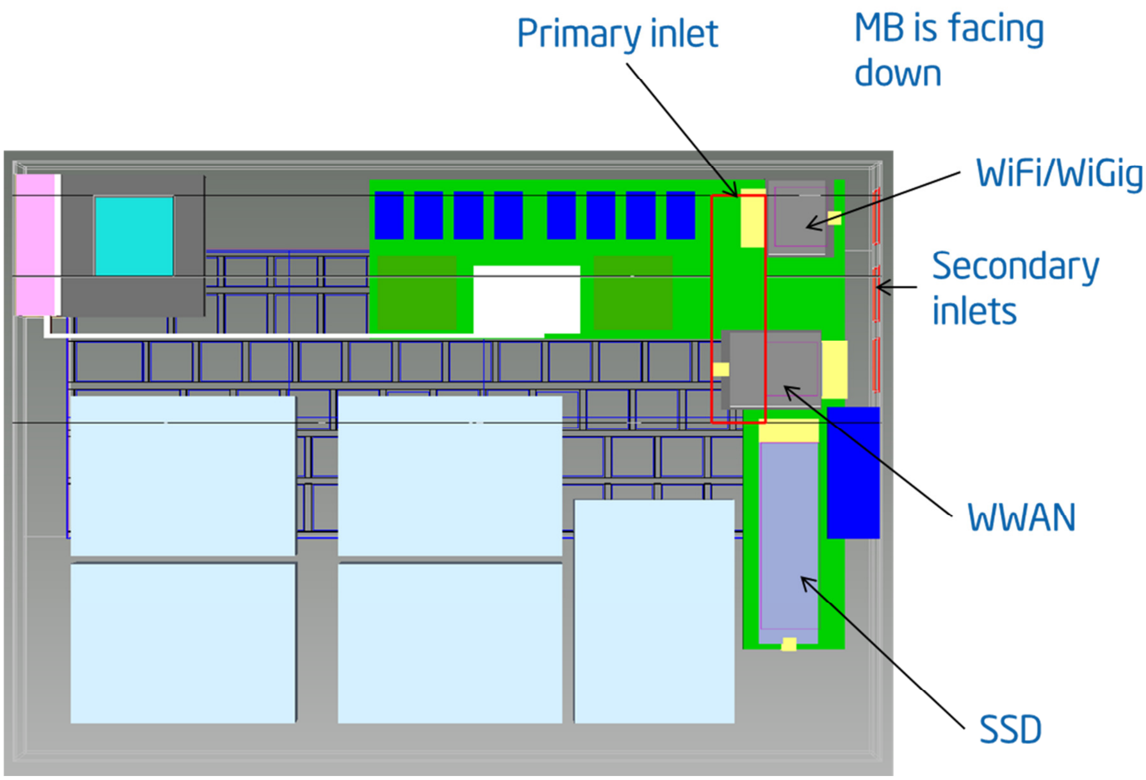


Figure 106. Thin Platform Notebook Layout with Vents and Key Components

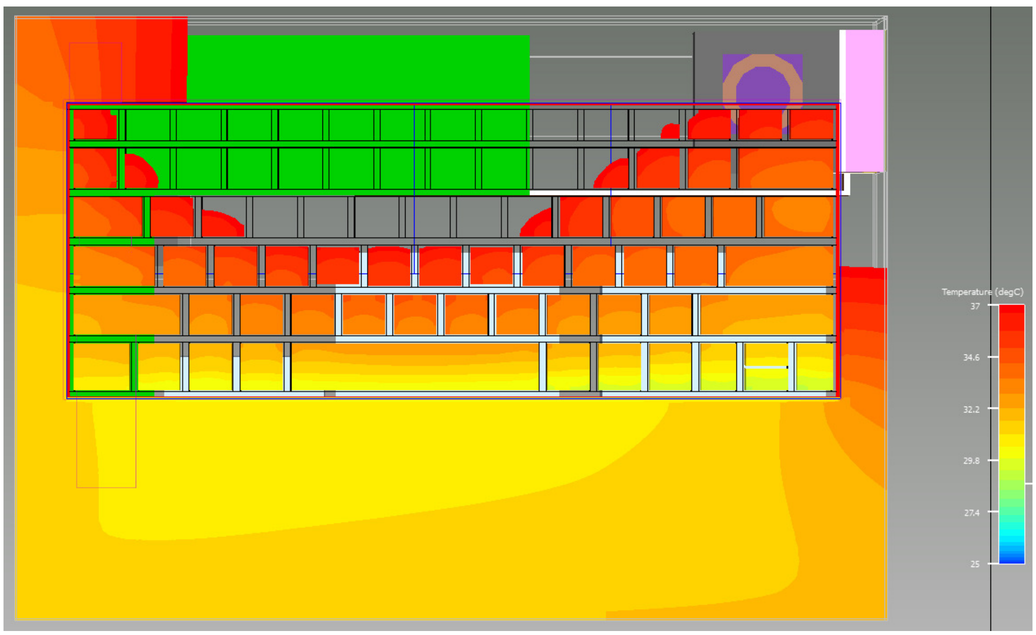
6.5.8.2.3. Module Placement Advice – Thin Platform Notebook

Lowest skin temperatures will be achieved when the heat sources are distributed over the largest possible area. This implies that, within reason, the modules should be located away from areas of concentrated heat on the motherboard, and especially as far as possible from the heat exchanger. Place inlet vents near modules to flush the inside surface of the casing, and use the bottom vent to act as a thermal break if needed. Address global hot spots via general system layout and use case assumptions.

6.5.8.2.4. Local Skin Temperature

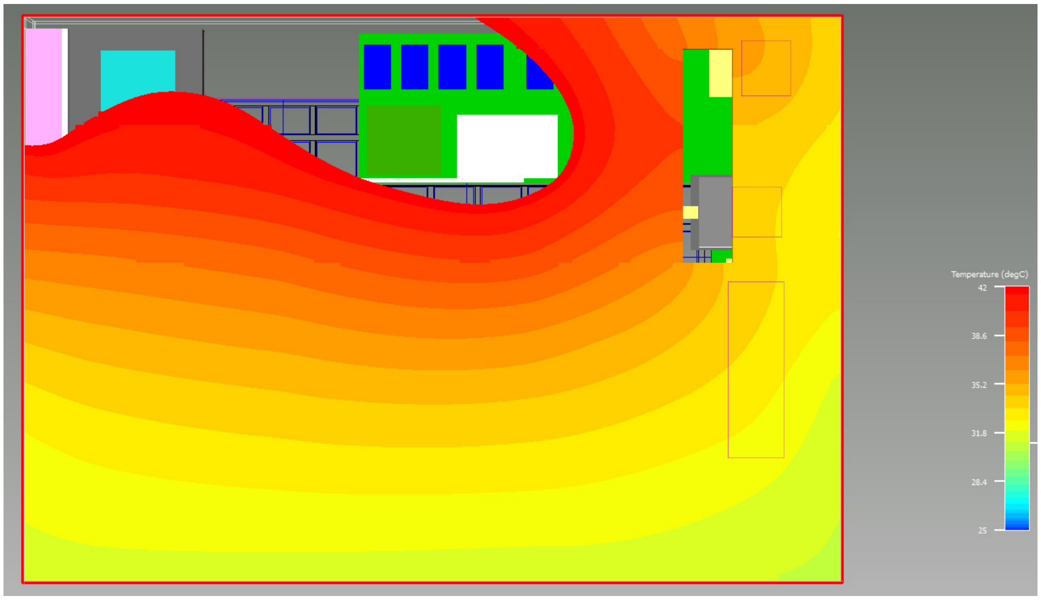
Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. For a notebook system, the global maximum is likely to be near the heat exchanger and fan exhaust. The temperature in this region is somewhat dependent on the module dissipation, as in this system category is makes up a meaningful fraction of the total system TDP. In addition, the fan flow rate is quite low, so that the casing needs to transfer a larger fraction of the total heat.

Local maxima are trickier to identify if they are lower than the global maximum. For the purposes of the examples shown in Figure 107 and Figure 108, a region of interest is defined in the vicinity of the modules, and the region maximum obtained. Another method might be to track a single consistent point over each module.



- Rectangles indicate local card areas;
- Irregularly unshaded areas indicate surface above the maximum scale temperature;
- Note scale corresponds to maximum skin temperature assumptions

Figure 107. Example View of Region and Hot Spots Over Modules



- Rectangles indicate local card areas;
- Irregularly unshaded areas indicate surface above the maximum scale temperature
- Note scale corresponds to max skin temperature assumptions

Figure 108. Example View of Region and Hot Spots Under Modules

6.5.8.2.5. Thermal design Power Response – Thin Platform Notebook with Fan Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to ~3+ W in the use case. Results in Table 62 and Table 63are model predictions at zero and at the extended use case, to bracket expectations. Temperatures are rounded to the nearest whole degree.

Note that the table distinguishes between local skin temperature (directly over or under the module) and a global skin hot spot, caused by the remainder of the system and use case, sometimes even in the absence of any module dissipation. Although the modules do not heat the skin excessively, the system designer will have to consider changes in the use case and/or the design to meet skin temperature requirements.

Also note that with so many assumptions in each analysis, the results shown in the table are not intended as accurate predictions, but only to provide an example of module effects on skin temperature. The flow rate of the fan and particulars of the keyboard model especially determine the skin temperature of modules below the keyboard area.

Table 62. Thermal Design Power Response – Thin Platform Notebook with Fan Category

	Thin Platform Notebook with Fan			
Socket #	1	1	2	3
Module Size	3030	3030	3042	2280
Function	WiFi/BT + WiGig	WiFi/BT + WiGig	WWAN	SSD
Use Case	Comms exc	Comms exc 50% power	Comms exc WWAN	PCH exc
Sys Dissipation W/O Module	19.4	9.7	19.4	21
Module Off	0 W	0 W	0 W	0 W
Mean Card T	42	31	38	33
Local Skin T Top	33	29	34	32
Local Skin T Bottom	32	29	32	33
Global Skin Hot Spot (HX)	46	36	47	47
Use Case TDP	1.4 W	0.7 W	1.4 W	2.4 W
Local Skin T Top	35	30	39	37
Local Skin T Bottom	36	30	36	38
Global Skin Hot Spot	47	37	48	49
Extended Case TDP	3 W	3 W	3 W	3 W
Local Skin T Top	38	35	41	39
Local Skin T Bottom	38	36	37	39
Fan Flow Rate, Cfm	0.6	0.6	0.6	0.6

Table 63. Skin temperature limit assumptions, Thin platform notebook with Fan

Ext Ambient	25
Skin T Limit Top	37
Skin T Limit Bottom	42

6.5.8.3. Tablet without Fan Category

Many assumptions are used in this document.

Table 64. Use Cases Applicable to Modules for Tablet without Fan

Component Dissipation (W)	Estimate I Skype—Over 3G Steady State	Estimate II Skype + 19x10 Display + 3G
SOC Package	1.16	1.5
POP Memory (2 GB)	0.29	.4
3G Comms	0.80	1.4
Camera	--	.25
Storage (eMMC)	0.05	--
PMIC	0.86	.7
Audio LPE	0.05	.1
MIPI to LVDS	0.13	--
Display (10”, 200 nits)	2.46	1.935
Battery Discharge	0.14	.1
Others (system VR, LEDs, etc.)	0.43	.1
Platform Total	6.37	6.485

6.5.8.3.1. Generic Motherboard Assumptions

The bottom view of a single-sided motherboard (all components facing the back within the system) are shown in Figure 109. The cards are installed in mid-plane connectors at one edge of the U-shaped board. There are several memory modules, a power management IC (PMIC), and two areas of clustered individual small heat sources (each shown as a rectangular heated area). The motherboard heat sources form a thermal boundary condition for the modules.

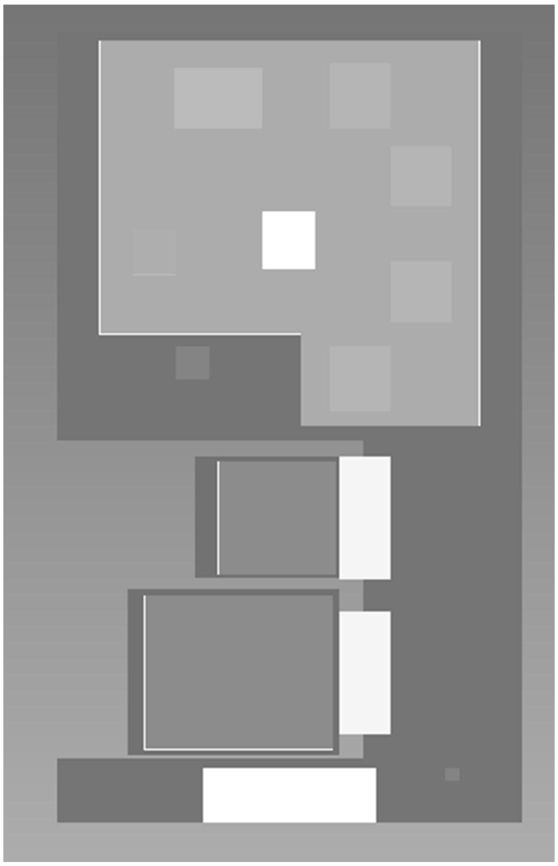


Figure 109. Example View of Tablet Motherboard

6.5.8.3.2. System Layout Assumptions

It is assumed that there is neither a fan nor venting in a tablet—a high emissivity surface has been assumed on the outside surface of the magnesium enclosure. In addition, the heat spreader under the backlight assembly is 0.2 mm thick copper since copper will reduce the hot spot compared to an aluminum spreader.

The motherboard is centrally located, between banks of batteries. This arrangement allows the heat to spread in all directions; concentrating heat sources in a corner restricts their heat spreading ability (Figure 110).

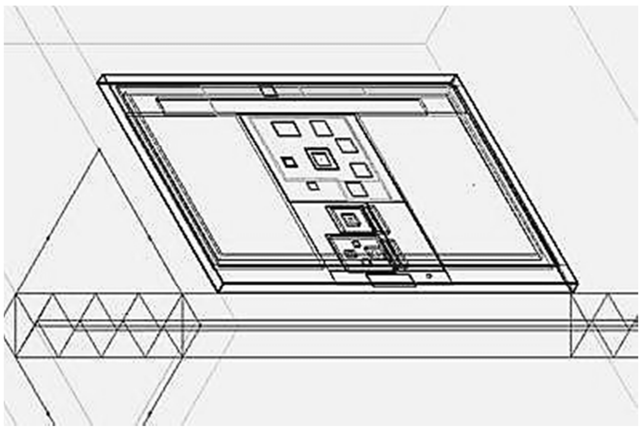


Figure 110. Example View of System Layout, Including Table

6.5.8.3.3. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. The global maximum is likely to be over the main dies (SoC and PMIC). The temperature in this region is somewhat dependent on the module dissipation, as in this system category it makes up a significant fraction of the total system TDP. As there is no flow at all, the casing needs to transfer all the heat dissipated inside (Figure 111 and Table 65).

Local maxima are trickier to identify if they are lower than the global maximum. The global maximum point was chosen because with no ventilation possible, any hot spots interact; all heat must spread and dissipate off the surface.

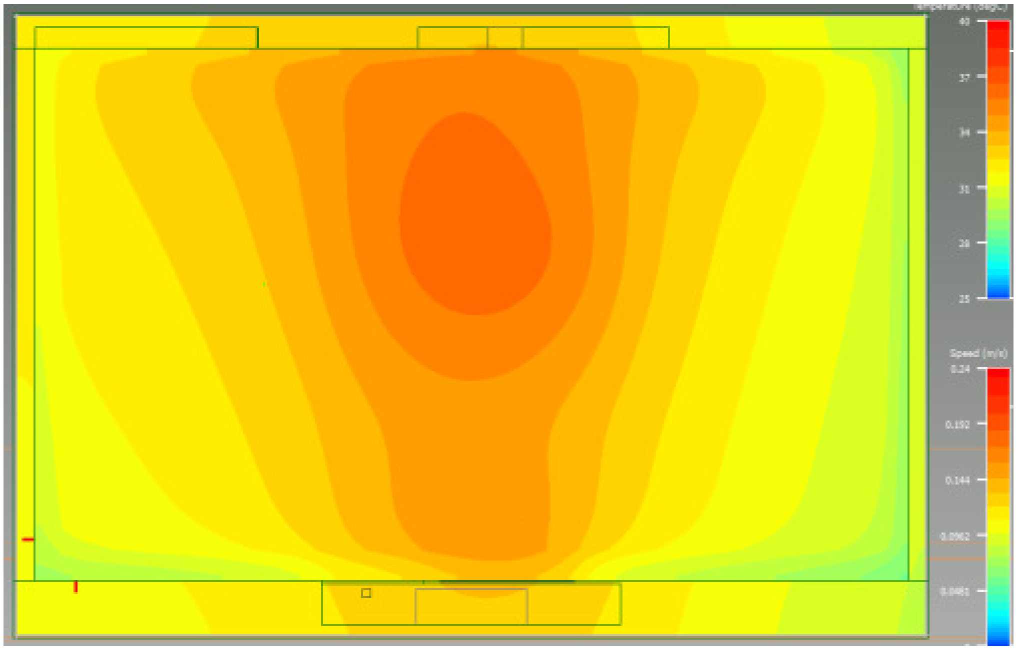


Figure 111. Example View of Display Surface Temperature with WWAN Use Case Estimate II

Table 65. Thermal Design Power Response—Tablet Category

	Tablet	
Socket #	1	2
Module Size	2230	3042
Function	WiFi/BT	WWAN LTE
Use Case	Estimate II	
Sys Dissipation W/O Module	5.1	5.1
Module Off	0 W	0 W
Mean Card T	31	31
Local Display T	35	35
Max Back T	32	32
Use Case TDP	1.4 W	1.4 W
Local Display T	37	37
Max Back T	34	34
Extended Case TDP	3 W	3 W
Local Display T	39	38
Max Back T	39	37

6.5.8.3.4. Thermal Design Power Response—Tablet Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to ~3+ W in the use case. Results in the table are model predictions at zero and at the extended use case, to bracket expectations. Temperatures are rounded to the nearest whole degree.

Also note that with so many assumptions in each analysis, the results shown in Table 66are not intended as accurate predictions, but only to provide an example of module dissipation effects on skin temperature.

Table 66. Skin Temperature Limit Assumptions, Tablet without Fan

Ext Ambient	Skin T Limit Display	Skin T Limit Back
25	40	38