# MP2651

## I²C-Controlled 1 to 4S Buck-Boost Charger with Reverse Source Mode

***PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE***

## DESCRIPTION

The MP2651 is a Buck-Boost Charger IC designed for battery pack with 1 to 4 cells in series. It can accept a wide range (4V to 22V) of input operation voltage for charging the battery. The battery voltage can be either lower or higher than input voltage due to the buck-boost topology.

When the input is present, the MP2651 operates in charge mode. It measures the battery voltage and charges the battery with four phases: constant current trickle charge, constant current pre-charge, constant current fast charge and constant voltage charge. Other features include charge termination and auto-recharge.

The MP2651 also integrates the input current limit and input voltage limit to avoid overloading the input power source. This is compliant to the USB and PD specification.

The MP2651 can also supply a wide range (3V to 21V) of voltage at input when Source mode is enabled. It also has output current limit with high resolution in source mode.

With I²C/SMBus interface, the MP2651 can be flexibly programmed the charging and discharge parameters, such as input current limit, input voltage limit, charging current, battery full regulation voltage, output voltage and current in source mode and so on. It can also provide the status and faults in operation through registers.

To guarantee safe operation, the IC limits the die temperature to a programmable threshold. Other safety features include input over-voltage protection, battery over-voltage protection, CFLR over-voltage protection, thermal shutdown, and a programmable timer to prevent prolonged charging of a dead battery.

MP2651 is available in TQFN-30 (4mm x 5mm) package.

## FEATURES

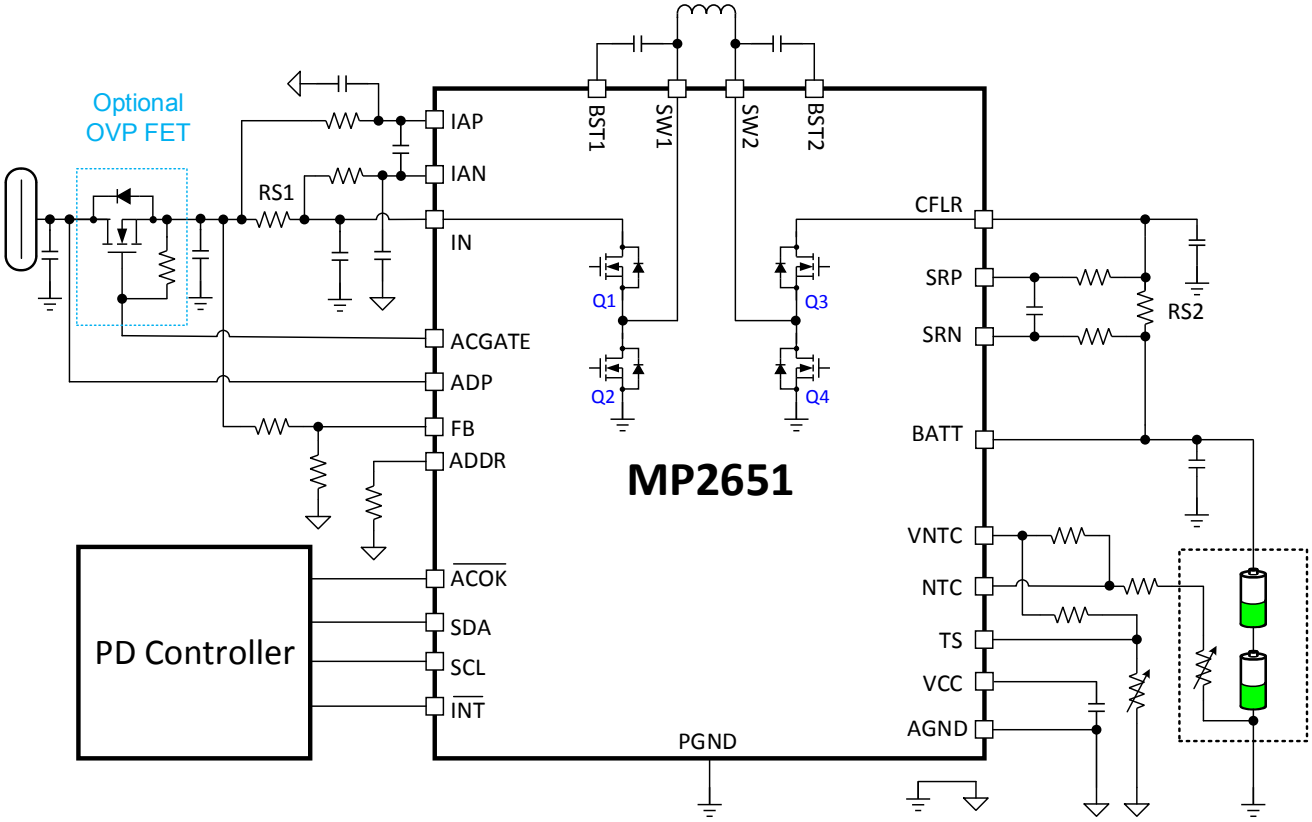
- Buck-boost Charger for 1 to 4 Cells in Series Battery Pack
- 4V to 22V Input Operation Voltage
- Up to 26V Sustainable Voltage
- Up to 28V Sustainable Voltage by Using External MOSFET
- Seamless and Smoothly Transition Between Buck and Boost Operation
- Configurable Input Maximum Current Limit and Input Minimum Voltage Limit
- Up to 6A Configurable Charge Current
- Configurable Battery-Full Voltage Up to 4.67V/Cell with 0.5% Accuracy
- Output Compatible with USB PD 3.0 source mode
- Configurable 3V to 21V Output Voltage with 20mV/Step
- Up to 6A Output Current with 50mA/Step
- 500kHz to 1.2MHz Configurable Switching Frequency
- I²C or SMBus Host Control Interface to Support Flexible Parameter Setting
- Input Power Source Status Indicator
- Integrated 10-bit ADC for voltage, current and temperature monitor in both charge mode and source mode
- Analog Output Pin to Monitor Charge Current.
- Input Over Voltage-Protection (OVP)
- Battery Over-Voltage-Protection (OVP)
- Output Short-Circuit-Protection (SCP) in Source Mode
- Battery Missing Detection
- NTC Pin Floating Detection
- Integrated N-channel MOSFET Driver for Input Power Pass Through or OVP
- Configurable JEITA for Battery Temperature Protection
- Thermal Regulation and Thermal Shutdown
- TQFN-30 (4mm x 5mm) Package

## APPLICATIONS

- Power Banks
- Wireless Speakers
- Drones
- Mobile Printers
- USB PD Multi-Cell Applications



## TYPICAL APPLICATION




**Typical Application Circuit**

## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP2651GVT-xxxx** | TQFN-30 (4mm×5mm) | *See Below* | 1 |
| EVKT-MP2651 | Evaluation Kit | *See Below* | |

* For Tape & Reel, add suffix –Z (e.g.: MP2651GVT-xxxx-Z).

**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain an "xxxx" value.

## TOP MARKING

MPSYWW
MP2651
LLLLLL

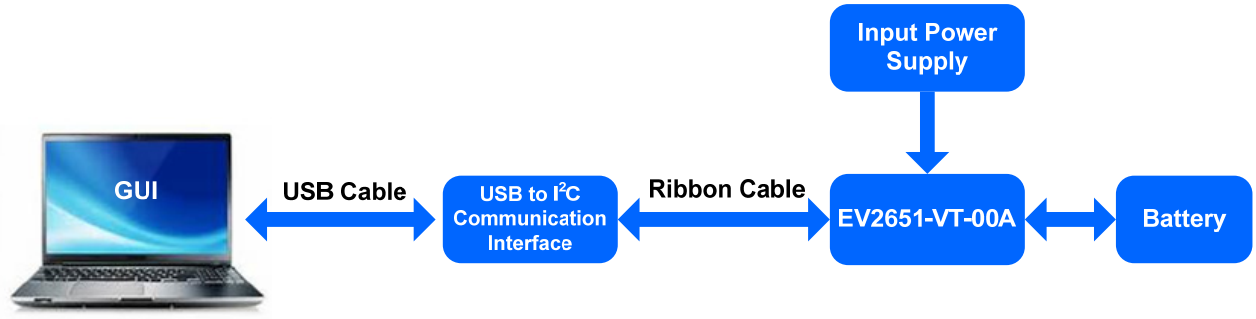
MPS: MPS prefix
Y: Year code
WW: Week code
MP2651: Part number
LLLLLL: Lot number

## EVALUATION KIT EVKT-MP2651

EVKT-MP2651 Kit contents: (Items below can be ordered separately).

| # | Part Number | Item | Quantity |
|---|---|---|---|
| 1 | EV2651-VT-00A | MP2651 Evaluation Board | 1 |
| 2 | EVKT-USBI2C-02-BAG | Includes one USB to I²C communication interface, one USB cable, and one ribbon cable | 1 |
| 3 | Online resources | Include datasheet, user guide, product brief, and GUI | 1 |

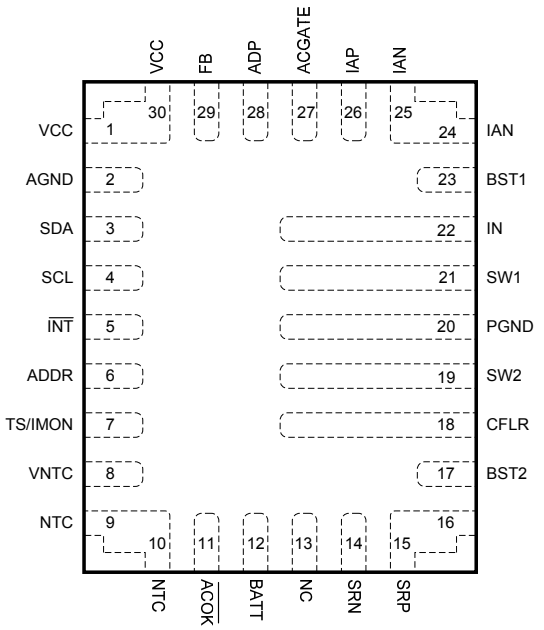
**Order direct from MonolithicPower.com or our distributors.**




**EVKT-MP2651 Evaluation Kit Set-Up**

## PACKAGE REFERENCE

**TOP VIEW**




**TQFN-30 (4mm×5mm)**

## PIN FUNCTIONS

| Package Pin # | Name | Description |
|---|---|---|
| 1/30 | VCC | **VCC LDO Output.** Connect 4.7μF ceramic capacitor from this pin to AGND. It can provide 3.6V output for internal circuit and open-drain pin pull-up. |
| 2 | AGND | **Analog ground.** All parameter settings refers to this ground. |
| 3 | SDA | **I²C/SMBus Data.** Connect SDA to the logic rail through a 10kΩ resistor. |
| 4 | SCL | **I²C/SMBus Clock.** Connect SCL to the logic rail through a 10kΩ resistor. |
| 5 | $\overline{\text{INT}}$ | **Interrupt Request Output.** This is open-drain structure and is required to pull up to VCC by 10kΩ resistor externally. |
| 6 | ADDR | **Address Setting.** Connect a resistor to AGND to set the IC address. |
| 7 | TS/IMON | **Temperature Sense/ Current Monitor.** This pin can be set as either temperature sense pin or current monitor pin. If it's configured as IMON pin function, which can monitor charge current. |
| 8 | VNTC | **Battery Temperature Sense Bias.** This pin is used for voltage bias of NTC comparator resistive divider. |
| 9/10 | NTC | **Negative Temperature Coefficient Thermistor Pin.** Battery temperature sense input. |
| 11 | $\overline{\text{ACOK}}$ | **Input Power Good Indication.** Open-drain output to indicate the adapter is present or not. Need external pull-up voltage source. |
| 12 | BATT | **Battery Pin.** Battery positive terminal. Connect 22μF ceramic capacitor from BATT to PGND as close as possible to the IC. Connect battery as close as possible to this pin to reduce IR drop. |
| 13 | NC | **No Connection.** Leave this pin floating. |
| 14 | SRN | **Battery Current Sense Resistor Negative Terminal.** |
| 15/16 | SRP | **Battery Current Sense Resistor Positive Terminal.** |
| 17 | BST2 | **Bootstrap.** Connect a 100nF bootstrap capacitor between BST2 and SW2 pin to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage. |
| 18 | CFLR | **DC/DC Power Stage Output.** Connect 2x22μF ceramic filter capacitor from CFLR to PGND as close as possible to the IC. |
| 19 | SW2 | **Switching Node.** The middle point of the boost phase half bridge. |
| 20 | PGND | **Power Ground.** |
| 21 | SW1 | **Switching Node.** The middle point of the buck phase half bridge. |
| 22 | IN | **Input Pin.** Power input of the IC. |
| 23 | BST1 | **Bootstrap.** Connect a 100nF bootstrap capacitor between BST1 and SW1 pin to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage. |
| 24/25 | IAN | **Input Current Sense Negative Terminal.** |
| 26 | IAP | **Input Current Sense Positive Terminal.** |
| 27 | ACGATE | **Input N-Channel MOSFET Gate Driver.** Used to drive the external pass through N-Channel MOSFET. Recommend connect a 1MΩ resistor between GATE and Source port of the N-Channel MOSFET. |
| 28 | ADP | **Adapter Voltage Sense.** If ADP OVLO is reached, external OVP MOSFET (if used) and power stage are turned off, IC internal bias voltage is also provided through this pin. |
| 29 | FB | **Feedback Pin.** Output voltage feedback pin in Source mode. If the output voltage at IN pin is programmed via register in Source mode, this pin will not be functional. Leave this pin floating or connect it to AGND via 10kΩ resistor. |

## ABSOLUTE MAXIMUM RATINGS (1)

ADP, ACGATE to PGND (DC) ..... -0.3V to 28V
IAP, IAN, IN to PGND (DC) ..... -0.3V to 26V
IAP, IAN, IN to PGND (20ns) ..... -0.3V to 28V
IAP to IAN ..... -3.6V to 3.6V
SW1, SW2 to PGND (DC) ..... -0.3V to 24V
SW1, SW2 to PGND (20ns) ..... -2V to 28V
CFLR, BATT to PGND ..... -0.3V to 24V
SRP, SRN to PGND ..... -0.3V to 24V
SRP to SRN ..... -3.6V to 3.6V
BST1 to SW1 ..... 0 to 5V
BST2 to SW2 ..... 0 to 5V
All Others Pins to AGND ..... -0.3V to 5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation ($T_A$ = +25°C) (2) ..... 3.29W
Storage Temperature…. .....-65°C to +150°C

### *ESD Ratings*

Human Body Model (HBM) ..... 2kV
Charge Device Model (CDM) ..... 250V

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 4V to 22V
Input Current ($I_{IN}$) ..... Up to 6A
Charge Current ($I_{CC}$) ..... Up to 6A
Battery Voltage ($V_{BATT}$) ..... Up to 18.68V
Operating junction temp. ($T_J$) ....-40°C to +125°C

### *Thermal Resistance* (4)

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| TQFN-30 (4mmx5mm) | 38 | 8 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Power Characteristic** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 4 | | 22 | V |
| ADP Under Voltage Lockout Threshold | $V_{ADP\_UVLO}$ | $V_{ADP}$ falling | 2.4 | 2.6 | 2.8 | V |
| ADP Under Voltage Lockout Hysteresis | | $V_{ADP}$ rising | | 1 | | V |
| ADP Over Voltage Lockout Threshold | $V_{ADP\_OVP}$ | $V_{ADP}$ rising | 23 | 23.9 | 24.7 | V |
| ADP Over Voltage Lockout Hysteresis | | $V_{ADP}$ falling | | 500 | | mV |
| ADP Over Voltage Protection Recover Deglitch Time | | $V_{ADP}$ falling | | 100 | | ms |
| Input Under Voltage Lockout Recovery Degltich Time | $t_{INUVLO\_DGL}$ | $V_{IN}$ rising | | 30 | | ms |
| Input Under Voltage Protection | $V_{IN\_UVP}$ | $V_{IN}$ falling, REG11h, bits [9:8] = 00 | 2.9 | 3.2 | 3.5 | V |
| | | $V_{IN}$ falling, REG11h, bits [9:8] = 01 | 6 | 6.4 | 6.8 | V |
| | | $V_{IN}$ falling, REG11h, bits [9:8] = 10 | 11.5 | 12 | 12.5 | V |
| | | $V_{IN}$ falling, REG11h, bits [9:8] = 11 | 16.2 | 16.8 | 17.4 | V |
| Input Under Voltage Protection Threshold Hysteresis | | $V_{IN}$ rising, REG11h, bits [9:8] = 01/10/11 | | 328 | | mV |
| | | $V_{IN}$ rising, REG11h, bits [9:8] = 00 | | 490 | | mV |
| Input Under Voltage Protection Recovery Deglitch Time | $t_{INUVP\_DGL}$ | $V_{IN}$ rising | | 30 | | ms |
| Input Over Voltage Protection Threshold | $V_{IN\_OVP}$ | $V_{IN}$ rising, REG11h, bits [7:6] = 00 | 6.9 | 7.25 | 7.6 | V |
| | | $V_{IN}$ rising, REG11h, bits [7:6] = 01 | 10.8 | 11.25 | 11.7 | V |
| | | $V_{IN}$ rising, REG11h, bits [7:6] = 10 | 17 | 17.65 | 18.25 | V |
| | | $V_{IN}$ rising, REG11h, bits [7:6] = 11 | 22 | 22.45 | 23.15 | V |
| Input Over Voltage Protection Deglitch Time | $t_{INOVP\_DGL}$ | $V_{IN}$ rising, REG11h, bit[10] = 0 | | 1 | | µs |
| | | $V_{IN}$ rising, REG11h, bit[10] = 1 | | 15 | | ms |
| Input Over Voltage Protection Hysteresis | | $V_{IN}$ falling | | 320 | | mV |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Over Voltage Protection Recover Deglitch Time | | $V_{IN}$ falling | | 30 | | ms |
| **DC/DC Converter** | | | | | | |
| Input Quiescent Current | $I_{IN\_Q}$ | $V_{IN}$=5V, Buck-boost and ACGATE driver are disabled. | | 550 | 620 | μA |
| | | $V_{IN\_UVLO}$ <$V_{IN}$ <$V_{IN\_OVLO}$, Buck-boost is disabled, ACGATE is enabled. | | 1 | 1.2 | mA |
| VCC LDO Output Voltage | $V_{VCC}$ | $V_{IN}$ = 5V, $I_{VCC}$= 15mA | | 3.6 | | V |
| VCC LDO Current Limit | $I_{VCC}$ | $V_{IN}$ = 5V, $V_{VCC}$=3.3V | | 23 | | mA |
| IN to SW1 N-Channel MOSFET (Q1) On Resistance | $R_{ON\_Q1}$ | | | 10 | | mΩ |
| SW1 to PGND N-Channel MOSFET (Q2) On Resistance | $R_{ON\_Q2}$ | | | 8 | | mΩ |
| CFLR to SW2 N-Channel MOSFET (Q3) On Resistance | $R_{ON\_Q3}$ | | | 8 | | mΩ |
| SW2 to PGND N-Channel MOSFET (Q4) On Resistance | $R_{ON\_Q4}$ | | | 20 | | mΩ |
| Operation Frequency | $f_{SW}$ | REG0Eh, bits [6:4] = 000 | 450 | 500 | 550 | kHz |
| | | REG0Eh, bits [6:4] = 001 | 540 | 600 | 660 | kHz |
| | | REG0Eh, bits [6:4] = 010 | 630 | 700 | 770 | kHz |
| | | REG0Eh, bits [6:4] = 100 | 675 | 750 | 825 | kHz |
| | | REG0Eh, bits [6:4] = 011 | 720 | 800 | 880 | kHz |
| | | REG0Eh, bits [6:4] = 101 | 810 | 900 | 990 | kHz |
| | | REG0Eh, bits [6:4] = 110 | 900 | 1000 | 1100 | kHz |
| | | REG0Eh, bits [6:4] = 111 | 1070 | 1200 | 1280 | kHz |
| **Battery Charger** | | | | | | |
| Battery Charge Voltage Regulation Range | $V_{BATT\_REG}$ | 1Cell OTP code setting | 3.4 | | 4.67 | V |
| | | 2Cell OTP code setting | 6.8 | | 9.34 | V |
| | | 3Cell OTP code setting | 10.2 | | 14.01 | V |
| | | 4Cell OTP code setting | 13.6 | | 18.68 | V |
| Battery Charge Voltage Regulation Accuracy (Continued) | | $T_A$= 25°C, $V_{BATT\_REG}$ = 4.35V, 1 Cell OTP setting | -0.5 | | +0.5 | % |
| | | $T_A$= 0 to 70°C, $V_{BATT\_REG}$ = 4.35V, 1 Cell OTP setting | -0.7 | | +0.7 | % |
| | | $T_A$= 25°C, $V_{BATT\_REG}$ = 8.4V, 2 Cells OTP setting | -0.5 | | +0.5 | % |
| | | $T_A$= 0 to 70°C, $V_{BATT\_REG}$ = 8.4V, 2 Cells OTP setting | -0.7 | | +0.7 | % |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Battery Charge Voltage Regulation Accuracy | | $T_A$= 25°C, $V_{BATT\_REG}$ = 12.6V, 3 Cells OTP setting | -0.5 | | +0.5 | % |
| | | $T_A$= 0 to 70°C, $V_{BATT\_REG}$ = 12.6V, 3 Cells OTP setting | -0.7 | | +0.7 | % |
| | | $T_A$= 25°C, $V_{BATT\_REG}$ = 16.8V, 4 Cells OTP setting | -0.5 | | +0.5 | % |
| | | $T_A$= 0 to 70°C, $V_{BATT\_REG}$ = 16.8V, 4 Cells OTP setting | -0.7 | | +0.7 | % |
| Fast Charge Current Range | $I_{CC}$ | RS2=10mΩ, REG10h, bit 7 = 0. | 0 | | 6.35 | A |
| Fast Charge Current Accuracy | $I_{CC\_ACC}$ | $I_{CC}$ = 6A, REG14h, bits [13:6] = 0111 1000 | 5.79 | 6 | 6.2 | A |
| | | $I_{CC}$ = 3A, REG14h, bits [13:6] = 0011 1100 | 2.84 | 3.0 | 3.14 | A |
| | | $I_{CC}$ = 2A, REG14h, bits [13:6] = 0010 1000 | 1.88 | 2.0 | 2.13 | A |
| | | $I_{CC}$ = 500mA, REG14h, bits [13:6] = 0000 1010 | 0.4 | 0.5 | 0.6 | A |
| Pre-charge to Fast Charge Threshold | $V_{BATT\_PRE}$ | REG0Bh, bit [12] = 1 | 2.9 | 3 | 3.1 | V/Cell |
| | | REG0Bh, bit [12] = 0 | 2.45 | 2.55 | 2.6 | V/Cell |
| Pre-charge to Fast Charge Deglitch Time | | | | 30 | | ms |
| Pre-charge to Fast Charge Hysteresis | | 1 Cell | | 85 | | mV |
| | | 2 Cells | | 160 | | mV |
| | | 3 Cells | | 240 | | mV |
| | | 4 Cells | | 315 | | mV |
| Pre-Charge Current Range | $I_{PRE}$ | RS2=10mOhm, REG10h, bit [7] = 0. | 0 | | 1.5 | A |
| Pre-Charge Current Accuracy | | $V_{BATT}$ = 5V, $I_{PRE}$ = 300mA, REG0Fh, bits [7:4] = 0011 | -20 | | 20 | % |
| | | $V_{BATT}$ = 5V, $I_{PRE}$= 500mA, REG0Fh, bits [7:4] = 0101 | -15 | | 15 | % |
| Trickle Charge to Pre-charge Threshold | $V_{BATT\_TC}$ | $V_{BATT}$ Rising | | 2 | | V/Cell |
| Trickle Charge to Pre-charge Hysteresis | | $V_{BATT}$ Falling | | 200 | | mV/Cell |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Trickle Charge Current Range | $I_{TC}$ | RS2=10mOhm, REG10h, bit [7] = 0. | 0 | | 750 | mA |
| Trickle Charge Current Accuracy | | 2 Cell, $V_{BATT}$=5V, REG0Fh, bits [11:8] = 0010, $I_{TC}$ = 100mA | 55 | 100 | 155 | mA |
| Auto-recharge Battery Voltage Threshold | | Lower than battery charge voltage, REG10h, bit [11] =0 | | -120 | | mV/Cell |
| Battery Over-voltage Protection Threshold | $V_{BATT\_OVP}$ | $V_{BATT}$ rising | 170 | 230 | 285 | mV/Cell |
| Battery Over-voltage Protection Hysteresis | | $V_{BATT}$ falling | | 113 | | mV/Cell |
| Battery Over-voltage Protection Deglitch Time | | | | 30 | | ms |
| TC and Pre Charge Timer | | | 1.8 | 2 | 2.2 | hours |
| CC and CV Charge Timer | | REG12h, bits [12:11] = 11 | 18 | 20 | 22 | hours |
| Termination Current Accuracy | $I_{TERM}$ | $I_{TERM}$ = 100mA, REG0Fh, bits [3:0] = 0010 | 60 | 120 | 180 | mA |
| | | $I_{TERM}$ = 200mA, REG0Fh, bits [3:0] = 0100 | 160 | 220 | 290 | mA |
| | | $I_{TERM}$ = 400mA, REG0Fh, bits [3:0] = 1000 | 360 | 420 | 490 | mA |
| Charge Termination Deglitch Time | $t_{TERM\_DGL}$ | | | 1 | | s |
| **Pin Leakage Current** | | | | | | |
| SRP, SRN leakage Current | $I_{LKG\_SRP\_SRN}$ | | -0.5 | | 0.5 | µA |
| IAP, IAN leakage Current | $I_{LKG\_IAP\_IAN}$ | | -0.5 | | 0.5 | µA |
| **Input Current Limit and Input Voltage Limit** | | | | | | |
| Input Current Limit Range | $I_{IN\_LIM}$ | RS1 = 10mΩ, REG10, bit [8] = 0 | 0 | | 5.8 | A |
| Input Current Limit Accuracy | $I_{IN\_LIM\_ACC}$ | REG08h, bits [6:0] = 000 1010, $I_{IN\_LIM}$ = 0.5A | 0.368 | 0.43 | 0.5 | A |
| | | REG08h, bits [6:0] = 001 0010, $I_{IN\_LIM}$ = 0.9A | 0.768 | 0.82 | 0.9 | A |
| | | REG08h, bits [6:0] = 001 1110, $I_{IN\_LIM}$ = 1.5A | 1.32 | 1.41 | 1.5 | A |
| | | REG08h, bits [6:0] = 011 1100, $I_{IN\_LIM}$ = 3.0A | 2.76 | 2.87 | 2.98 | A |
| | | REG08h, bits [6:0] = 110 0100, $I_{IN\_LIM}$ = 5.0A | 4.688 | 4.836 | 4.98 | A |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Minimum Voltage Regulation | $V_{IN\_MIN}$ | REG06h, bits [7:0]= 0011 1001, $V_{IN\_MIN}$ = 4.56V | 4.44 | 4.58 | 4.72 | V |
| | | REG06h, bits [7:0]=1000 0010, $V_{IN\_MIN}$ = 10.4V | 10.19 | 10.4 | 10.61 | V |
| | | REG06h, bits [7:0]=1010 1010, $V_{IN\_MIN}$ = 13.6V | 13.33 | 13.6 | 13.87 | V |
| | | REG06h, bits [7:0]=1110 0111, $V_{IN\_MIN}$ = 18.48V | 18.11 | 18.48 | 18.85 | V |
| **Thermal Regulation and Protection** | | | | | | |
| Thermal Shutdown Rising Threshold(5) | $T_{J\_SHDN}$ | $T_J$ rising | | 150 | | ºC |
| Thermal Shutdown Hysteresis(5) | | | | 20 | | ºC |
| Thermal Regulation Threshold | $T_{J\_REG}$ | REG0Fh, bits [14:12] = 111 | | 120 | | ºC |
| **Battery Temperature Monitoring** | | | | | | |
| NTC Floating Threshold | $V_{NTC\_FLT}$ | $V_{NTC}$ rising as percentage of $V_{VNTC}$ | | 95 | | % |
| NTC Floating Threshold Hysteresis | | $V_{NTC}$ falling as percentage of $V_{VNTC}$ | | 3 | | % |
| NTC Cold Temp Threshold | $V_{COLD}$ | $V_{NTC}$ rising as percentage of $V_{VNTC}$ , REG0Dh, bits [1:0] = 01 | 73.5 | 74.5 | 75.5 | % |
| NTC Cold Temp Threshold Hysteresis | | $V_{NTC}$ falling as percentage of $V_{VNTC}$ , | | 1.2 | | % |
| NTC Cool Temp Threshold | $V_{COOL}$ | $V_{NTC}$ rising as percentage of $V_{VNTC}$ ,REG0Dh, bits [3:2] = 10 | 64.2 | 65.2 | 66.2 | % |
| NTC Cool Temp Threshold Hysteresis | | $V_{NTC}$ falling as percentage of $V_{VNTC}$ | | 1.2 | | % |
| NTC Warm Temp Threshold | $V_{WARM}$ | $V_{NTC}$ falling as percentage of $V_{VNTC}$ , REG0Dh, bits [5:4] = 01 | 32.2 | 33.2 | 34.2 | % |
| NTC Warm Temp Threshold Hysteresis | | $V_{NTC}$ rising as percentage of $V_{VNTC}$ | | 1.2 | | % |
| NTC Hot Temp Threshold | $V_{HOT}$ | $V_{NTC}$ falling as percentage of $V_{NTC}$ , REG0Dh, bits [7:6] = 10 | 22.6 | 23.6 | 24.6 | % |
| NTC Hot Temp Threshold Hysteresis | | $V_{NTC}$ rising as percentage of $V_{NTC}$ | | 1.2 | | % |
| TS Hot | $V_{TS}$ | REG0Dh, bits [12:10] = 011, $T_A$ = 100°C | 12.5 | 13.5 | 14.5 | % |
| VNTC | $V_{VNTC}$ | | 1.26 | 1.28 | 1.30 | V |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Source Mode** | | | | | | |
| Output Voltage in Source Mode | $V_{IN\_SRC}$ | $I_{IN\_SRC}$ = 0A, $V_{BATT}$=7.6V REG09h, bits [9:0] = 00 1111 1010 | 4.85 | 5.0 | 5.15 | V |
| | | $I_{DSCHG}$ = 0A, $V_{BATT}$=7.6V REG09h, bits [9:0] = 01 1100 0010 | 8.82 | 9.0 | 9.18 | V |
| | | $I_{DSCHG}$ = 0A, $V_{BATT}$=7.6V REG09h, bits [9:0] = 10 0101 1000 | 11.76 | 12.0 | 12.24 | V |
| | | $I_{DSCHG}$ = 0A, $V_{BATT}$=7.6V REG09h, bits [9:0] = 10 1110 1110 | 14.7 | 15.0 | 15.3 | V |
| | | $I_{DSCHG}$ = 0A, $V_{BATT}$=7.6V REG09h, bits [9:0] = 11 1110 1000 | 19.7 | 20.0 | 20.3 | V |
| FB Reference Voltage for External Setting | $V_{FB}$ | REG09h, bits [9:0] = 11 1110 1000 | 1.194 | 1.206 | 1.218 | V |
| | | REG09h, bits [9:0] = 00 1111 1010 | 0.306 | 0.313 | 0.32 | V |
| Output Over Voltage Protection in Source Mode | $V_{IN\_SRC\_OV}$ | $V_{BATT}$ = 7.4V, $V_{IN}$ rising, percentage of discharge voltage setting. REG11h, bits [14:13] = 11 | | 110 | | % |
| Output Over Voltage Protection Hysteresis in Source Mode | | $V_{IN}$ falling | | 5 | | % |
| Output Under Voltage Protection in Source Mode | $V_{IN\_SRC\_UV}$ | REG11h, bits [12:11] = 00 | | 75 | | % |
| Output Under Voltage Protection Hysteresis in Source Mode | | | | 5 | | % |
| Discharge Output Under Voltage Deglitch Time | | $V_{IN}$ falling | | 10 | | ms |
| Discharge Output Under Voltage Recover Deglitch Time | | $V_{IN}$ rising | | 30 | | ms |
| Output Current Regulation In Discharge Mode | $I_{IN\_SRC}$ | REG0Ah, bits [6:0] = 001 1110, $V_{BATT}$ = 7.4V | 0.9 | | | A |
| | | REG0Ah, bits [6:0] = 010 1100, $V_{BATT}$ = 7.4V | 1.5 | | | A |
| | | REG0Ah, bits [6:0] =100 1100, $V_{BATT}$=7.4V | 3.0 | | | A |
| Battery Under Voltage Lockout Threshold | $V_{BATT\_UVLO}$ | $V_{BATT}$ falling | 2.5 | 2.6 | 2.7 | V/Cell |
| Battery Under Voltage Lockout Hysteresis | | $V_{BATT}$ rising | | 280 | | mV |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Battery Low Voltage Threshold | $V_{BATT\_LOW}$ | $V_{BATT}$ falling, REG0Bh, bits [10:9] = 10 | 3.1 | 3.2 | 3.3 | V/Cell |
| Battery Low Voltage Hysteresis | | $V_{BATT}$ rising | | 200 | | mV/Cell |
| Battery Low Voltage Deglitch Time | | $V_{BATT}$ falling | | 30 | | ms |
| Battery Quiescent Current | $I_{BATT\_Q}$ | $V_{IN}$ = 0V, $V_{BATT}$=8.4V, source mode is disabled, ADC,watchdog timer and ACGATE driver are disabled. | | 33 | 39.5 | µA |
| | | $V_{IN}$ = 0V, $V_{BATT}$=8.4V, source mode is disabled, ADC and ACGATE driver are disabled, Watchdog timer is enabled. | | | 0.655 | mA |
| | | $V_{IN}$= 0V, $V_{BATT}$=8.4V, source mode is disabled. Both ADC and watchdog timer are enabled. ACGATE driver is disabled. | | | 3.2 | mA |
| **ACGATE Driver** | | | | | | |
| ACGATE | $V_{ACGATE}$ | Higher than $V_{ADP}$ when enabled | | 6 | | V |
| | | Higher than $V_{ADP}$ when disabled | | 0 | | V |
| **Open-Drain Pin Characteristics (INT, ACOK)** | | | | | | |
| Low Logic Voltage Threshold | $V_L$ | Sink 10mA current | | | 0.4 | V |
| **ADC** | | | | | | |
| Sample Rate | | | | 50 | | kHz |
| ADC Reference | | | | 1.28 | | V |
| ADC Resolution | | | | 10 | | Bits |
| **SMBus Interface (Note: SMBus should cover I²C spec) And I²C/SMBus lines are compatible with 1.8V/3.3V/5V logic** | | | | | | |
| Input High Threshold Level | $V_{IH}$ | $V_{PULL\ UP}$ = 1.8V, SDA and SCL | 1.3 | | | V |
| Input Low Threshold Level | $V_{IL}$ | $V_{PULL\_UP}$ = 1.8V, SDA and SCL | | | 0.4 | V |
| Output Low Threshold Level | $V_{OL}$ | $I_{SINK}$ = 1mA | | | 0.4 | V |
| Input leakage current | $I_{LEAK}$ | | -0.2 | | 0.2 | µA |
| **SMBus Timing Characteristics**(5) | | | | | | |
| SMBus Clock Frequency | $F_{SCL}$ | | 10 | | 400 | kHz |
| BUS free time | | Between stop and start condition | 4.7 | | | µs |
| Start condition hold time after which first clock is generated | | | 4.0 | | | µs |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $V_{BATT}$ = 3.7V/Cell, 2 Cell Setting, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Start condition setup time | | | 4.7 | | | µs |
| Stop condition setup time | | | 4.0 | | | µs |
| Data hold time | | | 300 | | | ns |
| Data setup time | | | 250 | | | ns |
| Clock low time out | | | 25 | | 35 | ms |
| Clock low period | | | 4.7 | | | µs |
| Clock high period | | | 4.0 | | 50 | µs |
| Clock/data fall time | | | | | 300 | ns |
| Clock/data rise time | | | | | 1000 | ns |

**Notes:**

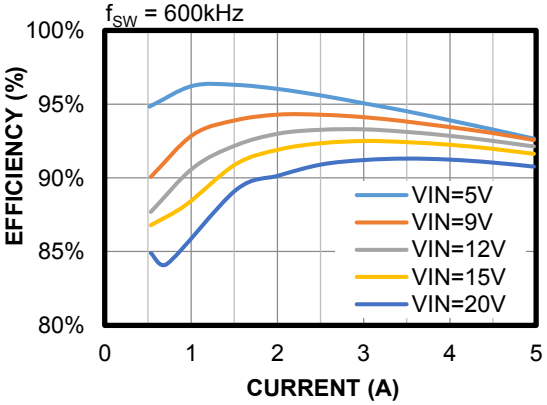
5) Guaranteed by design.

## TYPICAL CHARACTERISTICS

**Inductor DCR = 10mΩ**

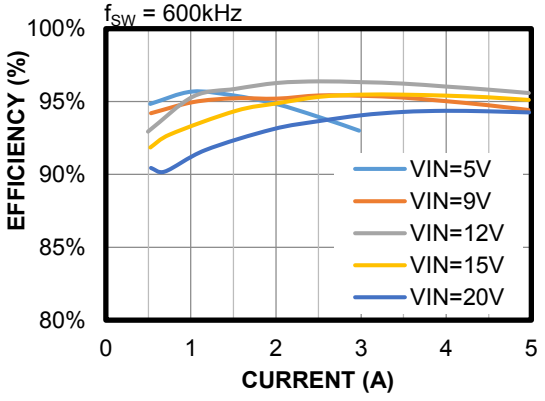
**Efficiency vs. Charge current in Charge Mode with 1s Battery**

$V_{BATT}$ = 4V, $V_{IN}$ = 5V / 9V / 12V / 15V / 20V, $f_{SW}$ = 600kHz



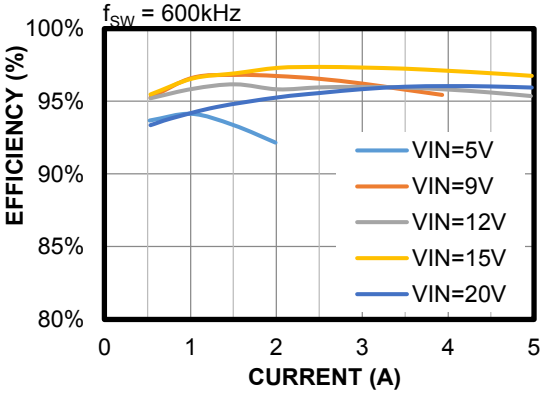

**Efficiency vs. Charge current in Charge Mode with 2s Battery**

$V_{BATT}$ = 8V, $V_{IN}$ = 5V / 9V / 12V /15V / 20V, $f_{SW}$ = 600kHz



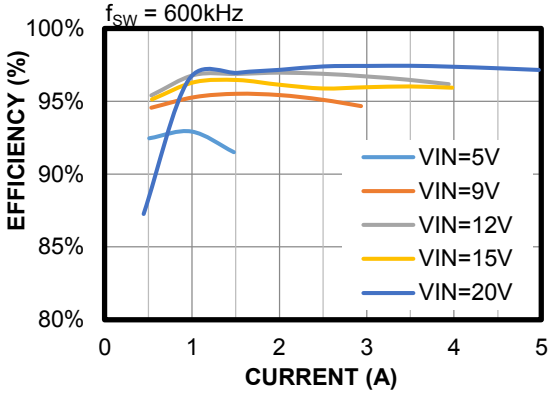

**Efficiency vs. Charge current in Charge Mode with 3s Battery**

$V_{BATT}$ = 12V, $V_{IN}$ = 5V / 9V / 12V /15V / 20V, $f_{SW}$ = 600kHz



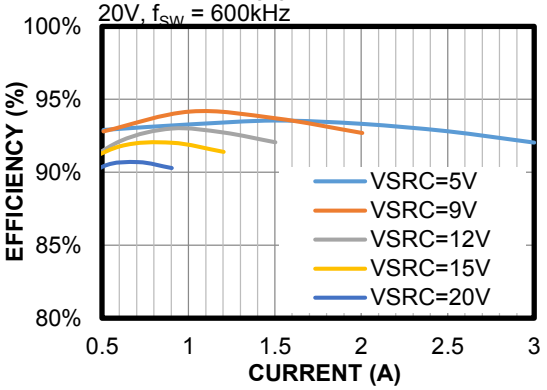

**Efficiency vs. Charge current in Charge Mode with 4s Battery**

$V_{BATT}$ = 16V, $V_{IN}$ = 5V / 9V / 12V / 20V, $f_{SW}$ = 600kHz



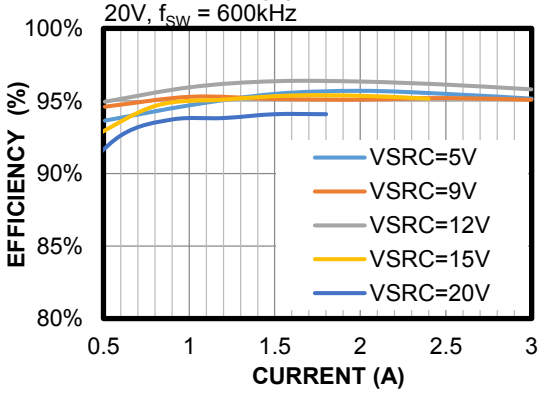

**Efficiency vs. Source Current in Source Mode with 1s Battery**

$V_{BATT}$ = 4.2V, $V_{SRC}$ = 5V / 9V / 12V / 15V / 20V, $f_{SW}$ = 600kHz




**Efficiency vs. Source Current in Source Mode with 2s Battery**

$V_{BATT}$ = 8.4V, $V_{SRC}$ = 5V / 9V / 12V / 15V / 20V, $f_{SW}$ = 600kHz

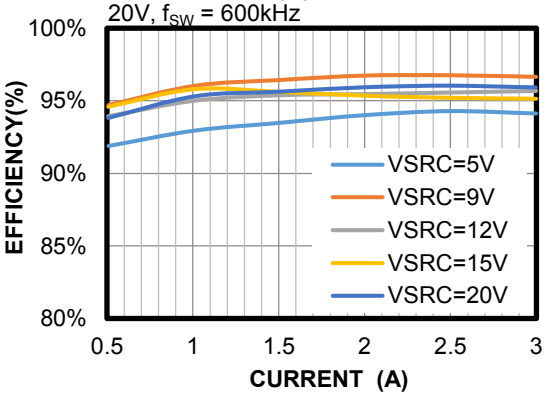


## TYPICAL CHARACTERISTICS *(continued)*

**Inductor DCR = 10mΩ**

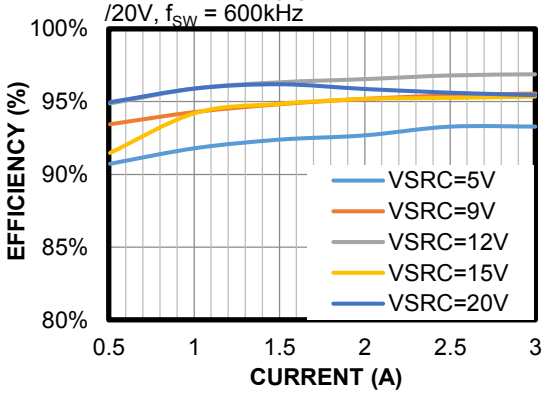
**Efficiency vs. Source Current in Source Mode with 3s Battery**

$V_{BATT}$ = 12.6V, $V_{SRC}$ = 5V / 9V / 12V / 15V/ 20V, $f_{SW}$ = 600kHz




**Efficiency vs. Source Current in Source Mode with 4s Battery**

$V_{BATT}$ = 16.8V, $V_{SRC}$ = 5V / 9V / 12V /15V /20V, $f_{SW}$ = 600kHz

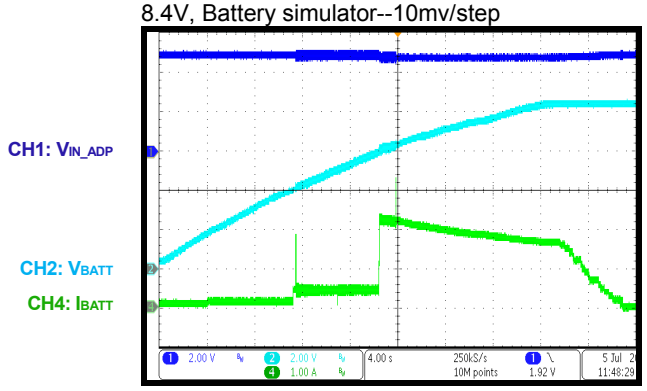


## TYPICAL PERFORMANCE CHARACTERISTICS

**Performance waveforms are tested on the evaluation board in the Design Example section. $C_{IN}$ = 10µFx5pcs+1µF,$C_{CFLR}$ = 22µFx2pcs+1µF, $C_{BATT}$ = 22µFx2pcs, L1 = 1.5µH,$f_{SW}$ = 600kHz. $I_{IN\_LIM}$ = 3000mA, $I_{CC}$ = 3000mA, 2Cell Application, $V_{BATT\_REG}$ = 8.4V.**

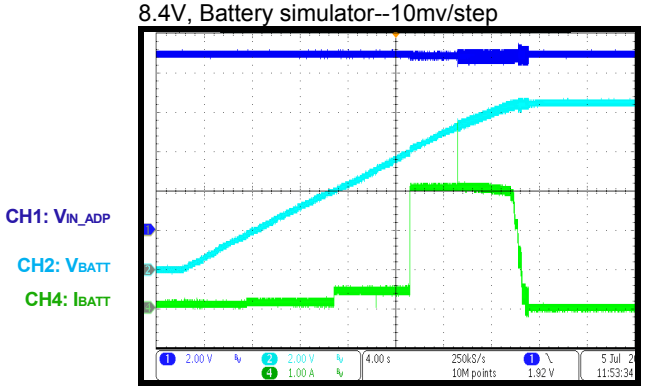
### Charge profile

$V_{IN\_ADP}$ = 5V, $I_{IN\_LIM}$ = 3A, $I_{CC}$ = 3A,$V_{BATT\ REG}$ = 8.4V, Battery simulator--10mv/step



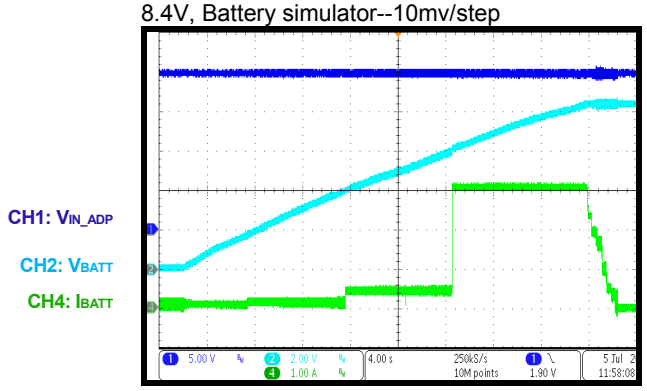

### Charge profile

$V_{IN\_ADP}$ = 9V, $I_{IN\_LIM}$ = 3A, $I_{CC}$ = 3A,$V_{BATT\ REG}$ = 8.4V, Battery simulator--10mv/step



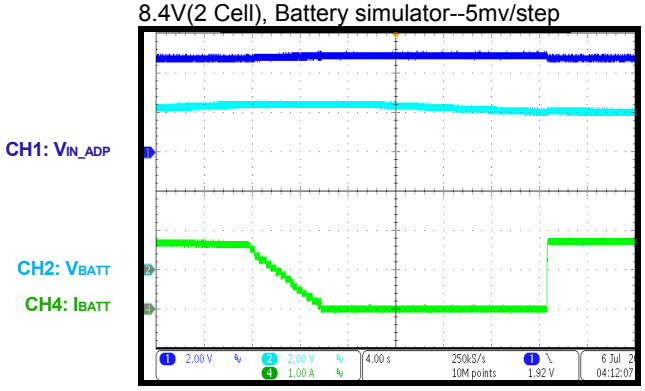

### Charge profile

$V_{IN\_ADP}$ = 20V, $I_{IN\_LIM}$ = 3A, $I_{CC}$ = 3A,$V_{BATT\ REG}$ = 8.4V, Battery simulator--10mv/step



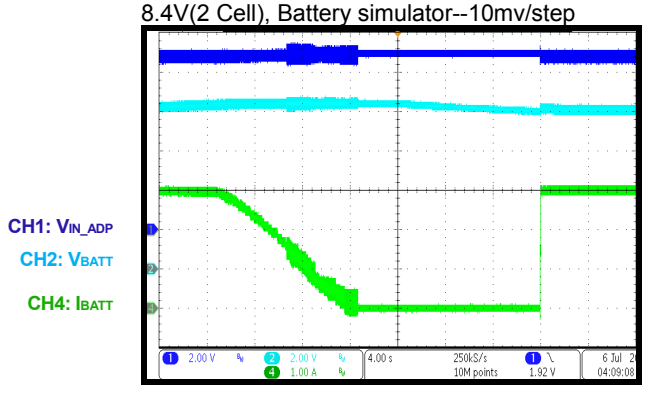

### Auto recharge profile

$V_{IN\_ADP}$ = 5V, $I_{IN\_LIM}$ = 3A, $I_{CC}$ = 3A,$V_{BATT\ REG}$ = 8.4V(2 Cell), Battery simulator--5mv/step



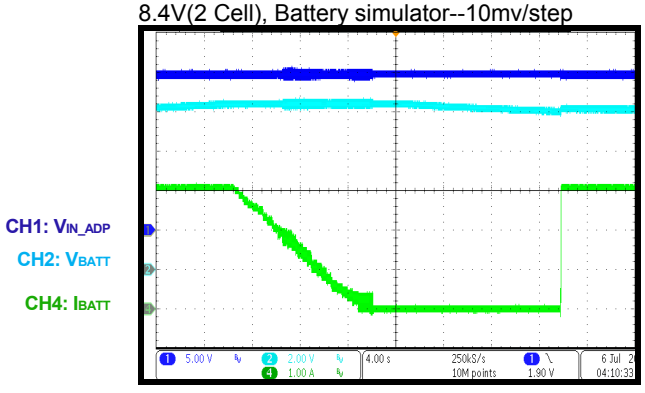

### Auto recharge profile

$V_{IN\_ADP}$ = 9V, $I_{IN\_LIM}$ = 3A, $I_{CC}$ = 3A,$V_{BATT\ REG}$ = 8.4V(2 Cell), Battery simulator--10mv/step




### Auto recharge profile

$V_{IN\_ADP}$ = 20V, $I_{IN\_LIM}$ = 3A, $I_{CC}$ = 3A,$V_{BATT\ REG}$ = 8.4V(2 Cell), Battery simulator--10mv/step

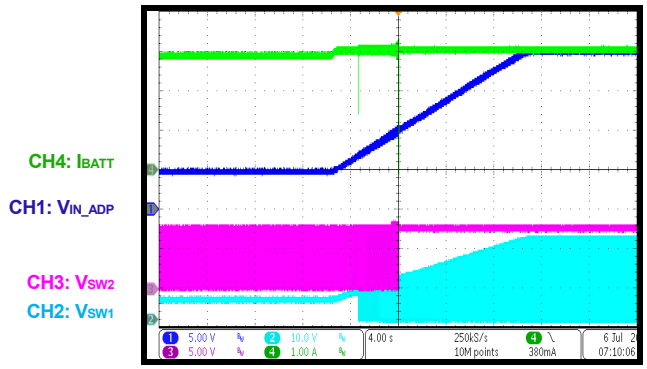


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board in the Design Example section. $C_{IN}$ = 10µFx5pcs+1µF,$C_{CFLR}$ = 22µFx2pcs+1µF, $C_{BATT}$ = 22µFx2pcs, L1 = 1.5µH,$f_{SW}$ = 600kHz. $I_{IN\_LIM}$ = 3000mA, $I_{CC}$ = 3000mA, 2Cell Application, $V_{BATT\_REG}$ = 8.4V.**

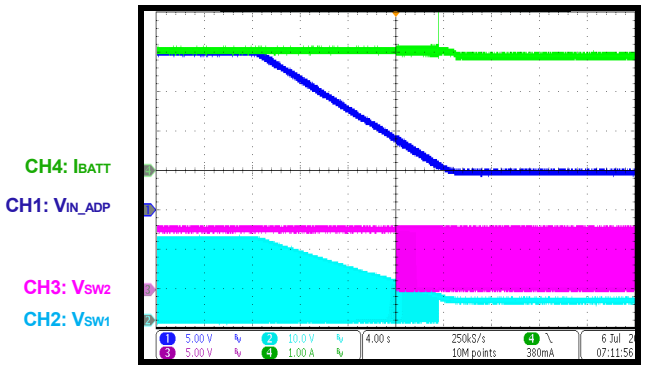
### $V_{IN\_ADP}$ step from 5V to 20V

$V_{BATT}$ = 7.4V(2Cell), $I_{CC}$ = 3A, enable charge



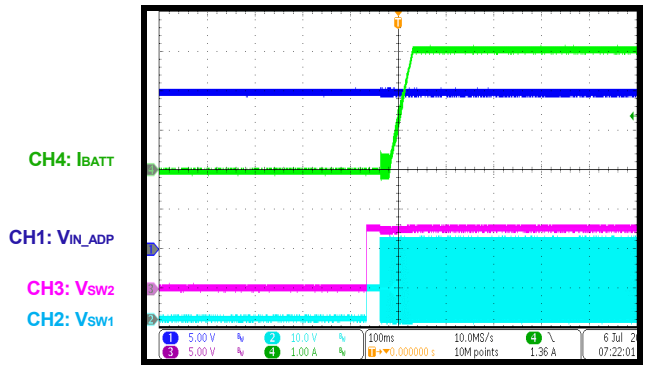

### $V_{IN\_ADP}$ step from 20V to 5V

$V_{BATT}$ = 7.4V(2Cell), $I_{CC}$ = 3A, enable charge



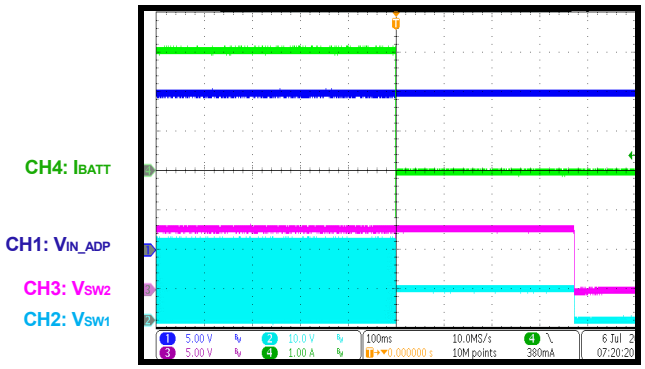

### Charge enable

$V_{IN\_ADP}$ = 20V,$V_{BATT}$ = 7.4V(2Cell), $I_{CC}$ = 3A



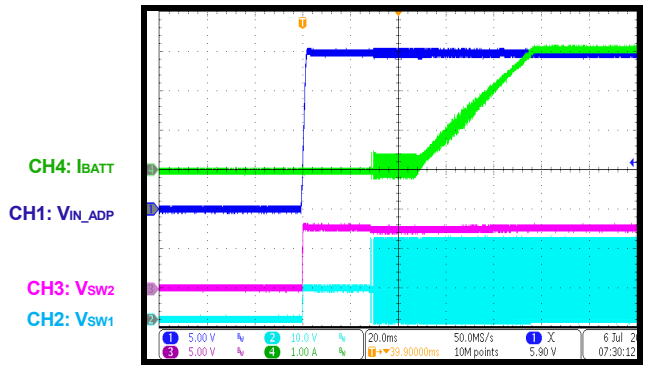

### Charge Disable

$V_{IN\_ADP}$ = 20V,$V_{BATT}$ = 7.4V(2Cell), $I_{CC}$ = 3A



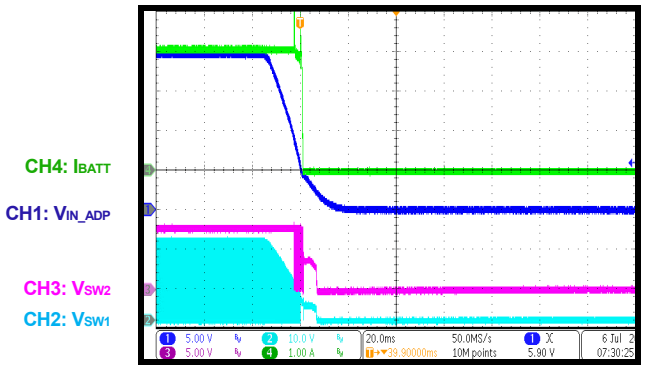

### Input power on

$V_{IN\_ADP}$ = 20V,$V_{BATT}$ = 7.4V(2Cell), $I_{CC}$ = 3A




### Input power off

$V_{IN\_ADP}$ = 20V,$V_{BATT}$ = 7.4V(2Cell), $I_{CC}$ = 3A

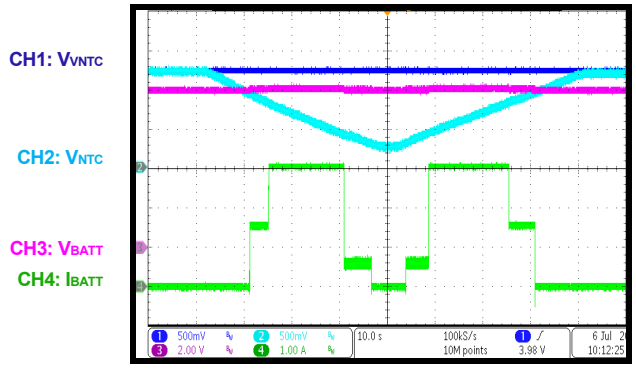


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board in the Design Example section. $C_{IN}$ = 10µFx5pcs+1µF,$C_{CFLR}$ = 22µFx2pcs+1µF, $C_{BATT}$ = 22µFx2pcs, L1 = 1.5µH,$f_{SW}$ = 600kHz. $I_{IN\_LIM}$ = 3000mA, $I_{CC}$ = 3000mA, 2Cell Application, $V_{BATT\_REG}$ = 8.4V.**

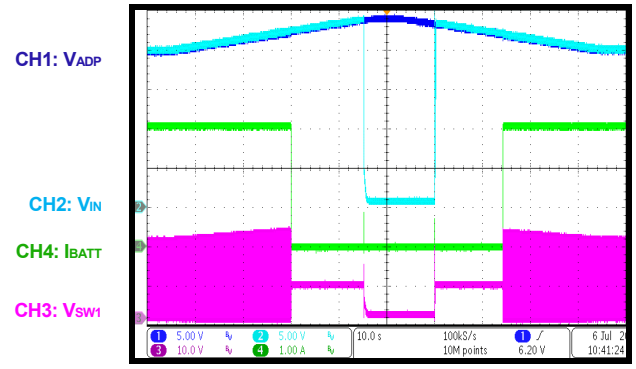
### JEITA compatible NTC protection

$V_{IN\_ADP}$ = 12V,$V_{BATT}$ = 8V, $V_{BATT\_REG}$ decreases 400mV in warm window, $I_{CC}$ decreases by half in cool window.



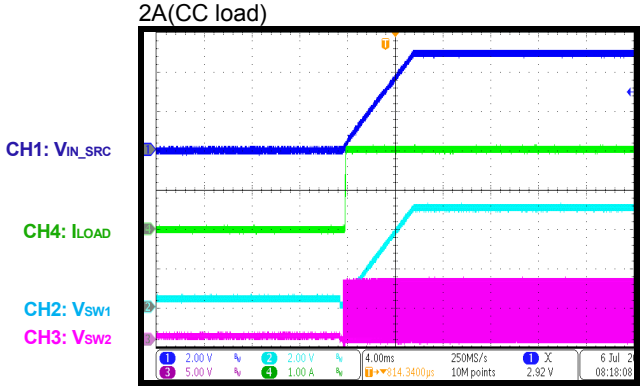

### ADP and IN OV protection

$V_{BATT}$ = 8V, enable ACGATE dirver with external N-channel pass through FET.Ramp up and down $V_{ADP}$.



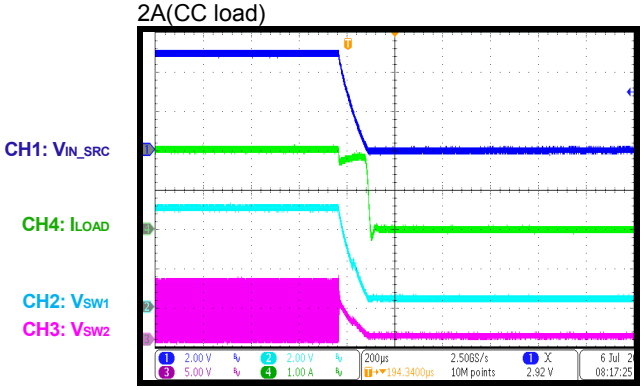

### Source Mode Enable

$V_{BATT}$ = 7.4V(2Cell),$V_{IN\text{-}SRC}$ = 5V, $I_{IN\_SRC}$ = 2A(CC load)



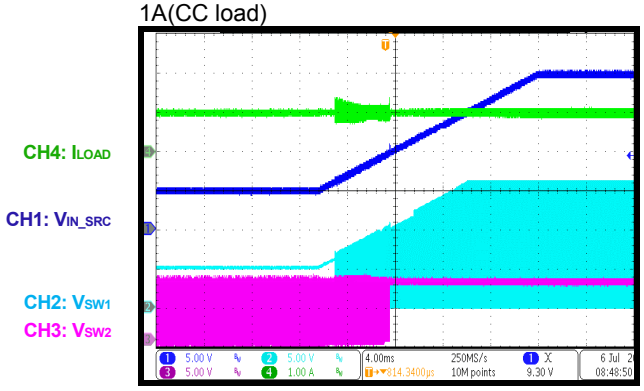

### Shutdown through VIN

$V_{BATT}$ = 7.4V(2Cell),$V_{IN\text{-}SRC}$ = 5V, $I_{IN\_SRC}$ = 2A(CC load)



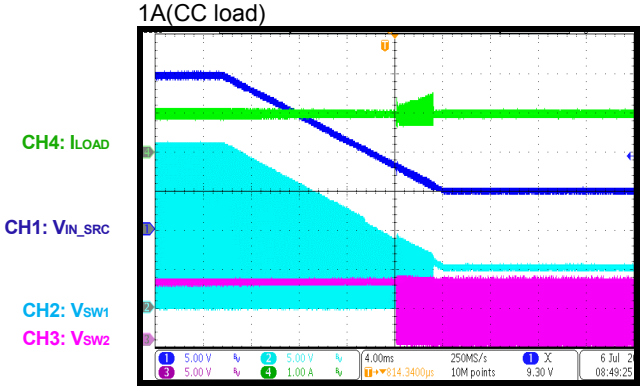

### $V_{IN\_SRC}$ step from 5V to 20V

$V_{BATT}$ = 7.4V(2Cell),$V_{IN\text{-}SRC}$ = 5V-20V, $I_{IN\_SRC}$ = 1A(CC load)




### $V_{IN\_SRC}$ step from 20V to 5V

$V_{BATT}$ = 7.4V(2Cell),$V_{IN\text{-}SRC}$ = 20V-5V, $I_{IN\_SRC}$ = 1A(CC load)

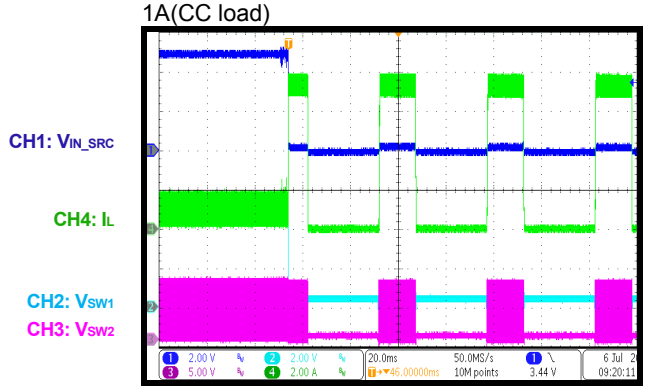


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board in the Design Example section. $C_{IN}$ = 10µFx5pcs+1µF,$C_{CFLR}$ = 22µFx2pcs+1µF, $C_{BATT}$ = 22µFx2pcs, L1 = 1.5µH,$f_{SW}$ = 600kHz. $I_{IN\_LIM}$ = 3000mA, $I_{CC}$ = 3000mA, 2Cell Application, $V_{BATT\_REG}$ = 8.4V.**

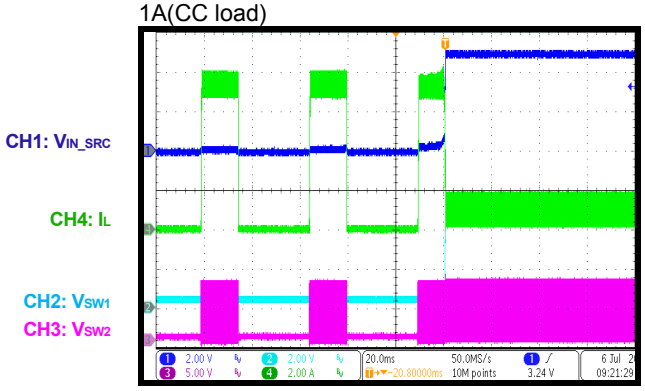
**$V_{IN\_SRC}$ short protection**

$V_{BATT}$ = 7.4V(2Cell),$V_{IN-SRC}$ = 5V, $I_{IN\_SRC}$ = 1A(CC load)




**$V_{IN\_SRC}$ short recovery**

$V_{BATT}$ = 7.4V(2Cell),$V_{IN-SRC}$ = 5V, $I_{IN\_SRC}$ = 1A(CC load)



## BLOCK DIAGRAM

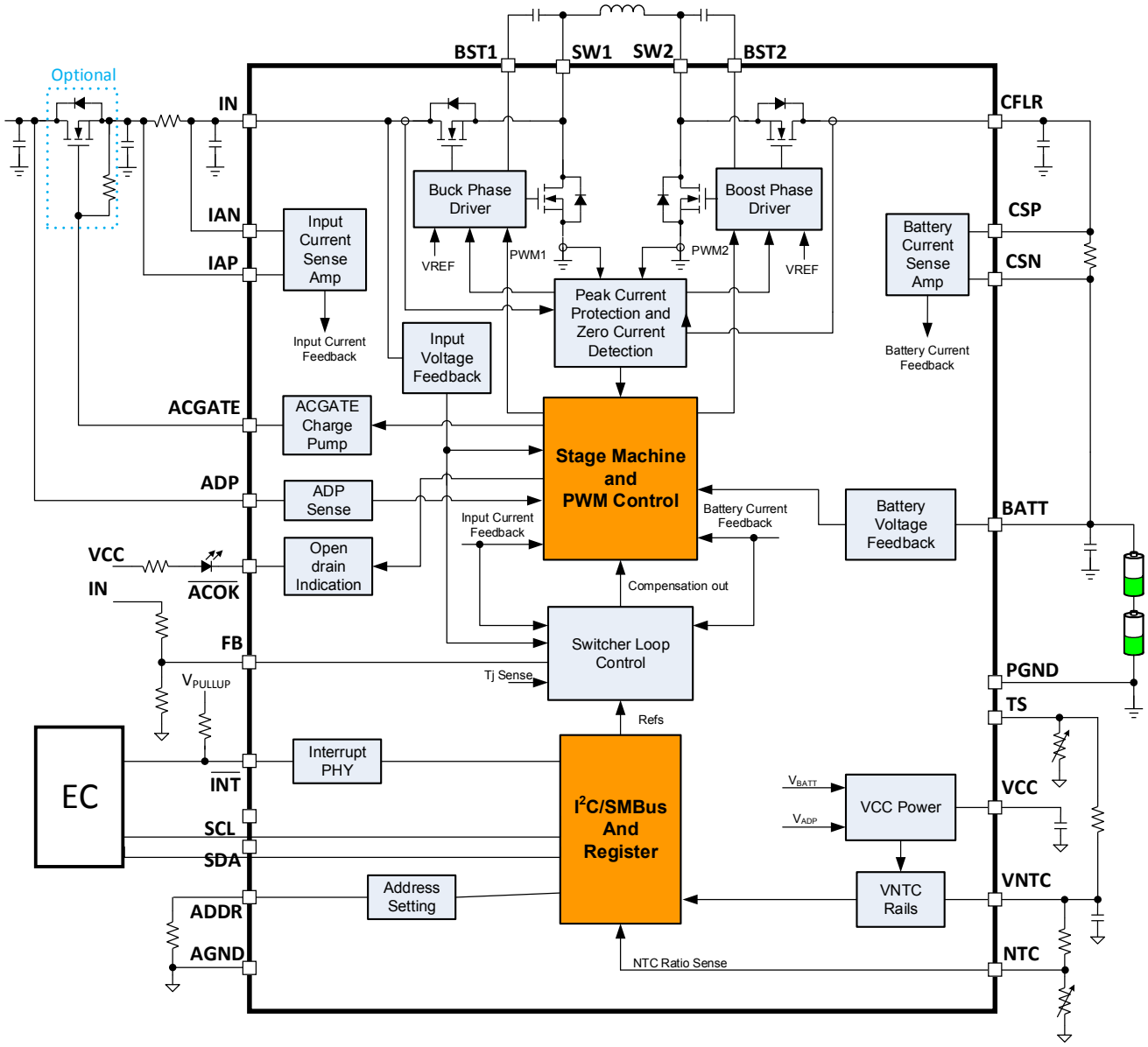



**Figure 1: Functional Block Diagram**

# OPERATION

## Introduction

The MP2651 is a highly integrated Buck-Boost charger IC with 4 switching FETs for battery pack with 1 to 4 cells in series. It also integrates one N-Channel MOSFET driver for higher input over-voltage protection.

The MP2651 also can operate by reverse direction to power the input from battery. Which is compliant to the USB PD Source Mode.

When input power is present, the MP2651 operates at charge mode. The buck-boost converter has three operating modes: boost mode when input voltage is lower than battery voltage; buck mode while input voltage is higher than battery voltage; and buck-boost mode when input voltage is close to battery voltage. The power structure is shown as Figure 2. And the Q1 to Q4 MOSFET state in different operation modes is shown as Table 1.

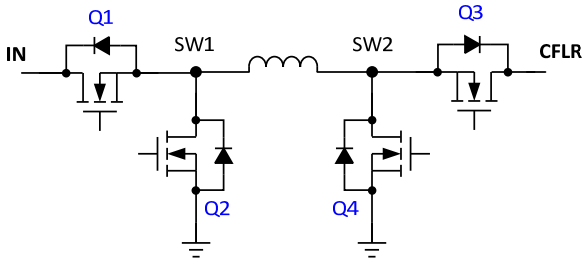



**Figure 2: Power Stage of MP2651**

**Table 1-a: Q1-Q4 Operation State in Charging Mode**

| MOSFET | Boost | Buck-Boost | Buck |
|---|---|---|---|
| **Q1** | On | Switching | Switching |
| **Q2** | Off | Switching | Switching |
| **Q3** | Switching | Switching | On |
| **Q4** | Switching | Switching | Off |

**Table 1-b: Q1-Q4 Operation State in Source Mode**

| MOSFET | Boost | Buck-Boost | Buck |
|---|---|---|---|
| **Q1** | Switching | Switching | On |
| **Q2** | Switching | Switching | Off |
| **Q3** | On | Switching | Switching |
| **Q4** | Off | Switching | Switching |

When the input is absent, IC is able to operate reversely to power the input from the battery by I²C/SMBus control. It can provide 3-21V output voltage with 20mV/step at input. It also has output current limit with 50mA/step in this mode. It's usually called source mode in USB PD.

## VCC LDO Output

The MP2651 integrates an LDO to power internal circuit including I²C block, FET driver, bias current and so on.

The VCC is powered by $V_{ADP}$ or $V_{BATT}$. When the voltage of ADP pin ($V_{ADP}$) is higher than $V_{ADP\_UVLO}$ threshold, the VCC is always powered by the $V_{ADP}$ whether in charge mode or source mode. When the input is absent or $V_{ADP}$ is lower than $V_{ADP\_UVLO}$ the VCC power will be switched from $V_{ADP}$ to $V_{BATT}$ as long as $V_{BATT}$>$V_{BATT\_UVLO}$.

The VCC can provide 3.6V output to supply the power to internal circuit and open-drain pin pull-up. It's not recommended to power other circuits any more.

## Input Power Status Indication

The MP2651 has both $\overline{ACOK}$ pin and register to indicate the input power supply status in charge mode. $\overline{ACOK}$ pin is open-drain structure and it will be pulled to AGND once $V_{IN\_UVP}$<$V_{IN}$<$V_{IN\_OVP}$.

At the same time, the status register PG_STAT shows power good.

## Input Over-Voltage Protection

The MP2651 has two-tier input OVP protection, $V_{ADP\_OVP}$ and $V_{IN\_OVP}$. The MP2651 has a dedicated ADP pin to sense the input voltage. If $V_{ADP}$ > $V_{ADP\_OVP}$, the ACGATE will be pulled down to turn off M1 immediately and at the same time the buck-boost of MP2651 is also turned off. The MP2651 will report ADP OVP fault in fault register. It has 100ms deglitch time when recovery from ADP OVP fault.

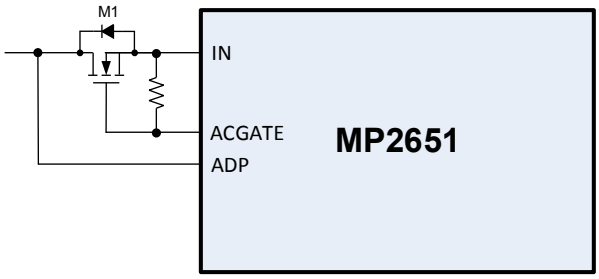



**Figure 3: ACGATE Driver**

When $V_{IN\_OVP}<V_{IN}<V_{ADP\_OVP}$, the M1 will still be turned on and switcher of MP2651 is disabled. A fault will be reported in REG17h bit [13].

### Input Current Limit and Input Voltage Limit Regulation

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the MP2651 has both input current limit and input voltage limit regulation. When either input current limit or input voltage limit is reached, the MP2651 will regulate the duty cycle of Q1 and Q4 to limit the input power according to the setting.

### Battery Charge Profile

In charge mode, the IC has 5 control loops to regulate input voltage, input current, charge current, battery-full regulation voltage, and device junction temperature.

The IC provides four main charging phases: constant current trickle charge, constant pre-charge, constant current fast charge and constant voltage charge.

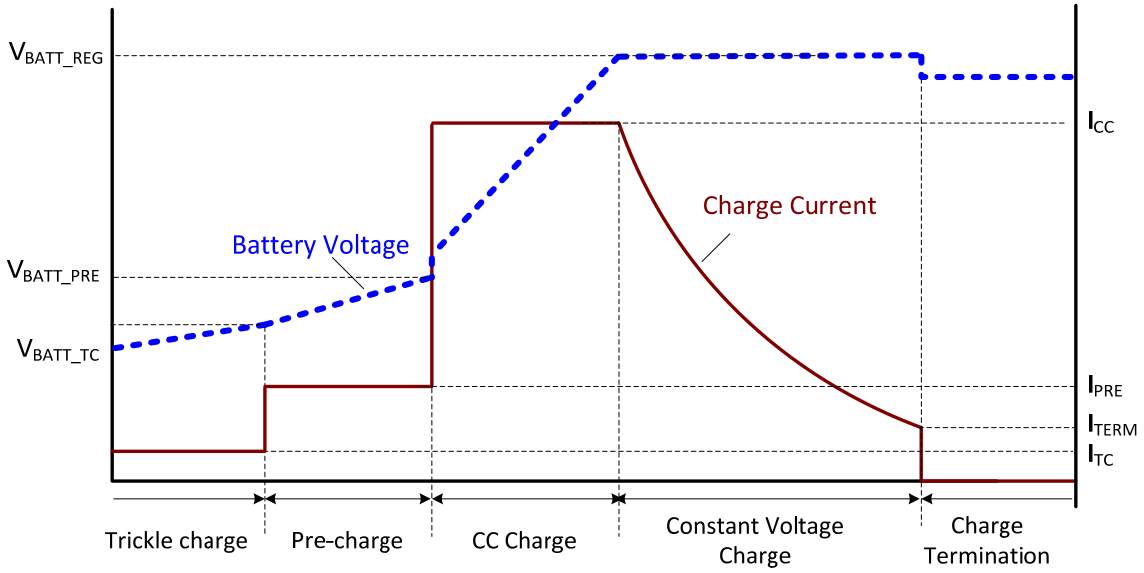



**Figure 4: Charge Profile**

### Phase 1 (Constant Current Trickle Charge):

When the input power is qualified as a good power supply, the IC checks the battery voltage to decide if trickle-charging is required. If the battery voltage is lower than $V_{BATT\_TC}$, a programmable trickle charging current is applied on the battery.

### Phase 2 (Constant Current Pre-charge)

When the battery voltage exceeds the $V_{BATT\_TC}$, the IC starts to safely pre-charge the deeply depleted battery until the battery voltage reaches “pre-charge to fast charge threshold” $V_{BATT\_PRE}$. If $V_{BATT\_PRE}$ is not reached before pre-charge timer (2hours) expires, the charge cycle is ceased and a corresponding timeout fault signal is asserted. The Pre-charge current can be programmable via the I²C register REG0Fh, bits [7:4] and $V_{BATT\_PRE}$ can be configurable by REG0Bh, bit [12]. There are two options: 2.5V/Cell for LiFePO4 battery and 3.0V/Cell for other chemistry Li-ion battery.

### Phase 3 (Constant Current Fast Charge)

When the battery voltage exceeds $V_{BATT\_PRE}$ set via REG0Bh, bit [12], the IC enters into constant-current charge (fast charge) phase.

The fast charge current can be configured via REG14h, bits [13:6].

### Phase 4 (Constant Voltage Charge)

When the battery voltage rises to the pre-programmable battery-full voltage $V_{BATT\_REG}$ set via REG15h, bits [14:4], the charge current begins to taper off.

The charge cycle is considered as completed when the charge current reaches the termination threshold $I_{TERM}$ set via REG0Fh, bits [3:0], assuming the termination function is enabled. If $I_{TERM}$ is not reached before the safety charge timer expires (***see Safety Timer section***), the charge cycle is ceased and corresponding timeout fault signal is asserted.

### Automatic Recharge

When the battery is charged full and the charging is terminated, the battery may be discharged because of the system consumption or self-discharge. When the battery voltage is discharged below recharge threshold (programmable), the IC automatically starts another new charging cycle without the requirement of manually re-starting a charging cycle if the input power is valid. The timer resets when the auto-recharge cycle begins.

A new charge cycle starts when the following conditions are valid:

- The input power is re-plugged.
- Battery charging is enabled by I²C/SMBus.
- No thermistor fault
- No safety timer fault
- No battery over-voltage

It means re-plugging of the input power or toggling of battery charging control bit (REG12h, bit [0]) can restart a charge cycle without any

fault happening. The new charge cycle can start with any phase as previous description depending on $V_{BATT}$.

### Battery Over-Voltage Protection

The IC has battery over-voltage protection. If the battery voltage exceeds the battery over voltage threshold (230mV higher than the battery regulation voltage per cell), charging is disabled. The battery OVP has 30ms deglitch time. Under this condition, the switcher will be off.

### Junction Thermal Regulation

Thermal regulation loop always monitors the internal junction temperature of the IC. When internal junction temperature exceeds the temperature limit the charge current is reduced to keep the junctional temperature at the regulation point. The multiple thermal regulation thresholds from 80ºC to 120ºC help system design to meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via REG0Fh, bits [14:12].

### Modes Transition Between Buck-Boost and Buck or Boost

The MP2651 always monitors the input voltage and CFLR voltage. It automatically switches between different modes as below figure 5.
When $V_{IN}$ rises higher than 90% x $V_{BATT}$, the MP2651 transits from Boost mode to Buck-boost mode.

When $V_{IN}$ decreases lower than 75% x $V_{BATT}$, the MP2651 transits from Buck-boost mode to Boost mode.

When $V_{IN}$ decreases lower than 120% x $V_{BATT}$, the MP2651 transits from Buck mode to Buck-boost mode.

When $V_{IN}$ rises higher than 135% x $V_{BATT}$, the MP2651 transits from Buck-boost mode to Buck mode.

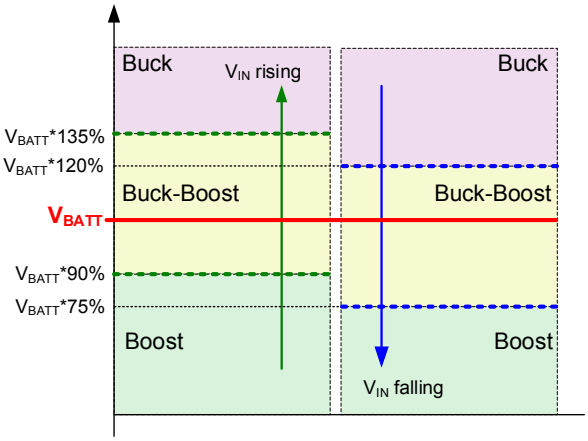



**Figure 5: Mode Transition Threshold**

### Pulse Skipping Mode (PSM) Operation

The MP2651 has PSM control to improve the efficiency when the load is light enough. In PSM, the lighter the load is, more pulse width will be skipped.

### Cycle-by-Cycle MOSFET Current Limit

MP2651 senses both High-side and Low-side MOSFET current in the loop control, it provides valley current limit in buck mode and peak current limit in boost mode in each cycle-by-cycle switching. In buck mode, the next period won't start before IL drops to the valley current limit and IL rises with minimum on time, so it may fold back the frequency when trigger valley current limit.

### ADC Conversion and Multiplexer

The MP2651 integrates a 10bit SAR ADC with 50kSPS. A 10-channel multiplexer is used to measure below parameters in Table 2.

**Table 2: ADC Channels**

| Sink Mode | Source Mode |
|---|---|
| • Input voltage<br>• Input current<br>• Battery voltage<br>• Charge current<br>• Battery temperature (NTC pin voltage ratio)<br>• TS pin voltage ratio<br>• Chip junction temperature | • Source voltage at input<br>• Source current at input<br>• Battery voltage<br>• Battery temperature.<br>• TS pin voltage ratio<br>• Chip junction temperature |

### Safety Timer

The IC provides both the pre-charge and CC/CV charge safety timer to prevent extended charging cycle due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is 2 hours when battery voltage is lower than $V_{BATT\_PRE}$.

The CC/CV charge safety timer starts when the battery enters fast charge phase. The user can configure this time via REG12h, bits [12:11]. Above two safety timers can be disabled via REG12h, bit [13]. The safety timer does not operate in the discharge mode.

The safety timer is reset at the beginning of a new charging cycle. The following actions restart the safety timer,

- Auto-recharge
- Charge enable toggling
- Input power toggling
- Safety timer enable toggling
- Thermal shutdown Recovery

The IC will automatically suspend the timer when NTC hot or cold fault.

The IC will automatically extend remain time by 2 times when any of below action happens.

- Input current limit loop kicks in.
- Input voltage limit loop kicks in.
- Thermal regulation loop kicks in.

Once the IC exits from previous events, the rest of time becomes half again. This function can be disabled via REG12h, bit [10].

### Watchdog Timer

The MP2651 has a watchdog timer to monitor action of the I²C interface. If the watchdog timer is enabled, the host needs to periodically reset the watchdog timer reset bit before watchdog timer expires. If the watchdog timer expires, some of the registers will reset its value to default. Please refer to the register map to check which registers will be reset after watchdog timer expires.

The following actions will reset the watchdog timer and make the IC recover from watchdog timer fault.

- Write to watchdog timer reset bit
- Write to the charge current register (REG14h)
- Write to the battery regulation voltage register. (REG15h)

The watchdog timer can be disabled via REG12h, bits [9:8].

### Battery Temperature Monitor by NTC (Negative Temperature Coefficient) Thermistor

“Thermistor” is the generic name given to thermally sensitive resistors. Negative temperature coefficient thermistor is generally called as thermistor. Depending on the manufacturing method and the structure, there

are many shapes and characteristic for various purposes. The thermistor resistance values, unless otherwise specified, are classified at a standard temperature of 25ºC. The resistance of a temperature is solely a function of its absolute temperature.

Refer to datasheet of the thermistor, the mathematic expression which relates the resistance and the absolute temperature of a thermistor is as follows,

$$R_1 = R_2 \cdot e^{\beta \cdot \left(\frac{1}{T1} - \frac{1}{T2}\right)}$$

Where: R1 is the resistance at absolute temperature T1, R2 is the resistance at absolute temperature T2 and β is a constant which depends on the material of the thermistor.

The MP2651 continuously monitors battery's temperature by measuring the voltage at the NTC pin. This voltage is determined by the resistive divider whose ratio produced by different resistance of the NTC thermistor under different ambient temperature of the battery.

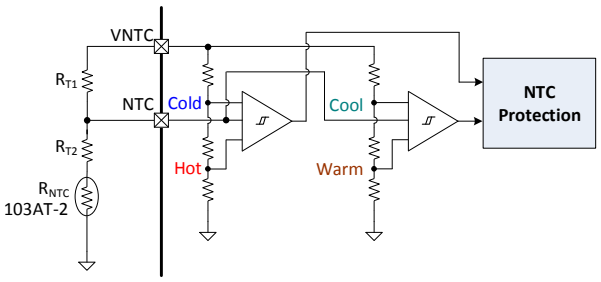



**Figure 6: NTC Protection Circuit**

MP2651 internally sets a pre-determined upper and lower bound of the range. If the voltage at the NTC pin goes out of this range which means the temperature is outside safe operating limit, the charging is ceased unless the operating temperature returns into the safe range.

To satisfy the JEITA requirement, the MP2651 has four temperature thresholds, the cold battery threshold (0ºC by default), the cool battery threshold (10ºC by default), the warm battery threshold (45ºC by default), and the hot battery threshold (60ºC by default). For given NTC thermistor, these temperatures correspond to the $V_{COLD}$, $V_{COOL}$, $V_{WARM}$, and $V_{HOT}$, which can be programmable by REG0Dh, bits [7:0]. When $V_{NTC}$ < $V_{HOT}$ or $V_{NTC}$ > $V_{COLD}$, the charging is suspended and timers are suspended. When $V_{HOT}$ < $V_{NTC}$ < $V_{WARM}$ or when $V_{COOL}$ < $V_{NTC}$ < $V_{COLD}$, the charging behavior is programmable via REG0Ch, bits [14:4]. Figure 7 shows the JEITA control profile.

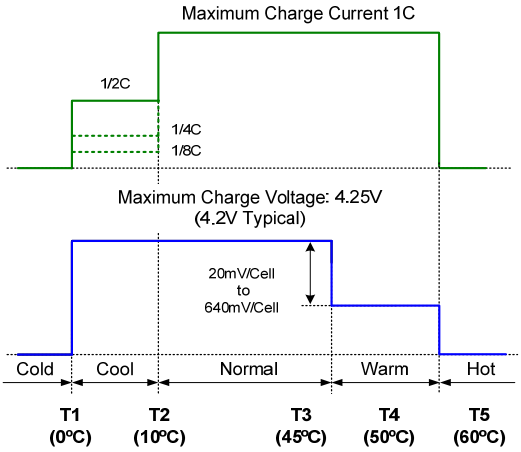



**Figure 7: NTC Window**

MP2651 also monitors the battery temperature in discharge mode. It only sends out NTC fault indication when battery temperature is out of range between $V_{COLD}$ and $V_{HOT}$.

### NTC Floating Detection

If NTC voltage is higher than 95%, NTC float is detected, an INT is asserted the corresponding status register is changed. When the NTC is floating the switcher will be off.

### Battery Missing Detection

The MP2651 will count the times of charge termination every 10s, if charge termination repeats more than three times in 10s, the MP2651 will report that the battery is missing in status register and initiate an INT signal.

### TS/IMON Pin Function

The MP2651 has a pin either used for temperature monitoring or current monitoring. When REG10h, bit [12] = 0, this pin is configured for temperature monitoring. When REG10h, bit[12] = 1, this pin will be used for charge current monitoring.

### TS Function

When TS function is enabled. TS pin can be used for sensing input connector temperature by setting REG0Dh, bits [12:10].

When TS pin is configured to sense input connector temperature, when $V_{TS\_HOT}$ is reached, an INT is asserted to indicate TS fault happens. In charging mode, the input current limit is reduced to 500mA with 50mA/Step every 62.5ms. When IC recovers from TS fault, the input current limit will rise to setting value with 50mA/Step every 62.5ms.

The triggered INT is masked by REG18h as default.

### IMON Function

When IMON function is used, the IMON pin can represent battery charge current with gain of 0.1V/A.

### Thermal Shutdown

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the junction temperature reaches 150ºC, the PWM converter is shutdown. It will not resume normal operation until the junction temperature drops below 120ºC.

### Host Mode and Default Mode

The IC is host-controlled device. After power on reset, the IC starts in the watchdog timer expiration state, or default mode. All the registers are in the default settings.

Any write to the IC transits it to host mode. All the device parameters are programmable by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG01h Bit [6] before the Watchdog Timer expires. Once the watchdog timer expires, the IC goes back into default mode.

### Impedance Compensation to Accelerate Charging

In the whole charging cycle, the constant-voltage charging stage occupies larger ratios. To accelerate the charging cycle, it's better to have the charging stay at constant-current charge stage as long as possible.

The IC allows the user to compensate the intrinsic resistance of the battery by adjusting the battery regulation voltage according to the charge current and internal resistance. In addition, a maximum allowed regulated voltage is also set for the sake of the safety condition.

$$V_{BATT\_REG\_ACT} = V_{BATT\_REG} + Min\ (V_{CLAMP},\ I_{CHG\_ACT}\ x\ R_{BATT})$$

Where, $V_{BATT\_REG\_ACT}$ is the real battery regulation voltage, $V_{BATT\_REG}$ is the battery regulation voltage set via the I²C REG15h, bits [14:4]. $I_{CHG\_ACT}$ is the real-time charge current during the operation.

### Source Mode Operation

MP2651 can work in source Mode to supply IN pin from battery. The IC will not enter this mode if the battery is below the configurable battery low threshold to ensure that battery is not drained. The source mode operation can be enabled when REG12h, bit [3] = 1. When both charging and discharge are enabled, the discharge operation takes higher priority.

In source mode, the IC employs a fixed frequency (500k to 1.2MHz configurable) switching regulator. And it switches from PWM operation to pulse-skipping operation at light load.

The output voltage is compliant with USB PD specification, including 5V, 9V, 12V, 15V and 20V, with 20mV step by either register programmable DAC or external FB pin.The output current limit is configurable via I²C/SMBus up to 5A with 50mA/step to be compliant.

As a conclusion only when the following conditions are valid the discharge operation will be enabled

- $V_{BATT} > V_{BATT\_LOW}$
- REG12h, bit [3] =1

To meet PD timing spec, output voltage should be settled within 275ms.

In source mode, the switcher can work in buck mode, boost mode or buck-boost mode according to the battery voltage and the discharge voltage.

### Over-Voltage Protection in Source Mode

The MP2651 also features output over voltage protection in Source mode. The IC continuously monitor the voltage at $V_{IN}$ pin in Source mode, when $V_{IN} > V_{IN\_SRC\_OV}$, the PWM will be disabled and OV fault will be asserted in status and fault register. And the PWM will recover

until the $V_{IN}$ is lower than $V_{IN\_SRC\_OV}$ by a hysteresis which is shown in EC table.

### Short-Circuit Protection in Source Mode

And the IC also features the output short circuit protection and output over voltage protection. When the load current reaches to the output current limit, $V_{IN}$ will start falling. When it falls below $V_{IN\_SRC\_UV}$ for more than 10ms, the discharge fault will be asserted and the discharge is disabled and restart after 30ms.

### Battery Standby Mode

If only the battery is connected and the input source is absent (and the discharge function is disabled), VCC LDO stays on. The maximum quiescent current of the IC is 35μA. The low quiescent current help to extend the running time of the battery.

### Battery Under Voltage Protection

The MP2651 has two-level battery under voltage protection. In source mode, when $V_{BATT}$<$V_{BATT\_LOW}$ for 30ms the MP2651 will generate an INT to report the battery voltage is low, then source mode is stopped. The user can configure the source mode behavior via REG0Bh bit [11]. When REG0Bh bit [11] = 0, source mode will restart automatically when VBATT recovery to higher than 6.4V; when REG0Bh bit [11] = 1, source mode is latched and only re-toggling the SRC-EN bit can restart source mode.

### SMBus and I²C Compatibility

The MP2651 has SCL/SDA interface which is compatible with SMBus and I²C.

The MP2651 registers are 16bits, so it's compatible with both SMBus and 16 bits I²C.

The System Management Bus (SMBus) is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. It is based on the principles of operation of I²C. MP2651 interface is a SMBus slave which will support both the standard mode (100kHz) and Fast mode (400kHz). The SMBus address is 0001 001x, where x is the read/write bit, receiving control inputs from the master device, like a micro controller or a digital signal processor.

### START and STOP Conditions

All the transactions begin with a START (S) and can be terminated by a STOP (P). A high to low transition on the SDA line while the SCL line is high defines a START condition. A low to high transition on the SDA line when the SCL line is high defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition; it is considered free after the STOP condition.

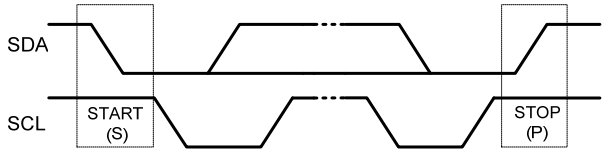



**Figure 8: START and STOP Conditions**

### Data Validity

The Data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

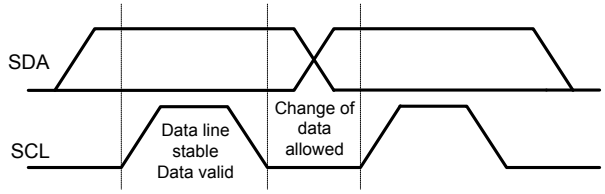



**Figure 9: Data Validity**

### Interrupt to Host (INT)

The IC also has an alert mechanism which can output an interrupt signal via INT pin to notice the system on the operation by outputting a 256μs low state INT pulse. The INT output is designed as open-drain structure, need an external pull-up voltage source in real operation. Please refer to the interrupt table to note which event will generate INT pulse. The INT can be shielded by via mask setting register REG18h-19h.

### Address Pin

To avoid being same address as other device on the I²C Bus. the address of MP2651 can be configured via one-time program memory after they are assembled.

To support multiple ICs of MP2760 connected on the same I²C/SMBUS lines, the device address can also be adjusted by register together with ADDR pin as the other option.

The address is 7 bits long, followed by the 8th bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE), and a one indicates a request for data (READ). The address bit arrangement is shown below.

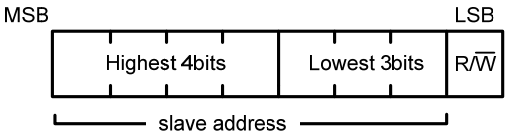



**Figure 10: 7-Bit Addressing**

The highest 4 bits of the address REG05h, bits [6:3] are configured via OTP.
The lowest 3 bits of the address REG05h, bits [2:0] are configured via two ways. It is controlled by the ADDR_CFG bit REG05h, bit [7].
If REG05h, bit [7] =1, the lowest 3 bits of address REG05h, bits [2:0] are fixed as 001.
If REG05h, bit [7] = 0, the ADDR pin programs the lowest 3 bits of IC address. There is a 10μA current flowing out of the ADDR pin. Connecting a resistor between ADDR pin and AGND to set different device address.

Table 3 shows the I²C/SMBus address for different resistor values from ADDR pin to AGND. This address is 7 bits long, followed by x, the 8th bit as a data direction bit (bit R/W).

**Table 3: Address Setting**

| $R_{ADDR}$ (kΩ) | Slave Address |
|---|---|
| 0 to 1k | 0001 000b |
| 4.34k to 5.87k | 0001 001b |
| 9.35k to 12.65k | 0001 010b |
| 16.92k to 22.89k | 0001 011b |
| Not recommend | 0001 100b (Reserved) |
| 41.4k to 56.01k | 0001 101b |
| 59.33k to 80.27k | 0001 110b |
| 85k to 115k | 0001 111b |

### SMBus Alert Response Address (ARA)

The SMBus alert response address (ARA) is a special address that can be used by the bus host.

In case more than one slave-only devices are connected on the bus and all INT lines are connected together. A slave-only device can signal the host through INT that it wants to talk. The host processes the interrupt and simultaneously accesses all INT devices through the Alert Response Address (ARA). Only the device(s) which pulled INT low will acknowledge the Alert Response Address.

The host performs a modified Receive Byte operation. The 7bit device address provided by the slave transmit device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

The SMBus Alert Response Address is 0001 100b.

### Byte Format

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received, so another byte may be sent. All clock pulses, including the acknowledge pulse (9th clock pulse), are generated by the master.

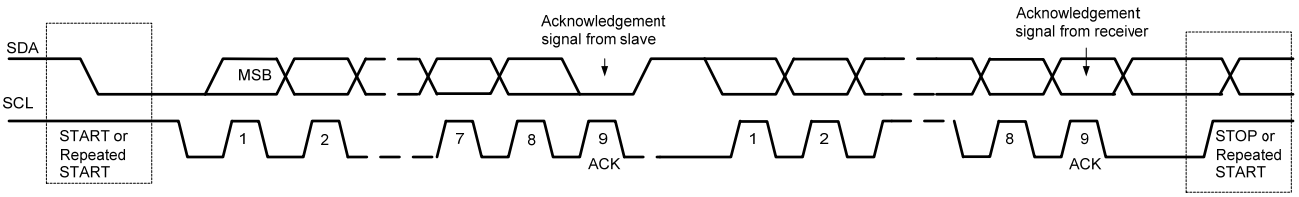



**Figure 11: Acknowledge Bit**

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. It remains high during the 9th clock pulse; this is the "not acknowledge" signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a transfer.

After the START, a slave address is sent. This address is 7 bits long followed by an 8th bit, a data direction bit (bit R/W). A zero indicates a transmission (WRITE), and a one indicates a request for data (READ). The complete data transfer is shown in

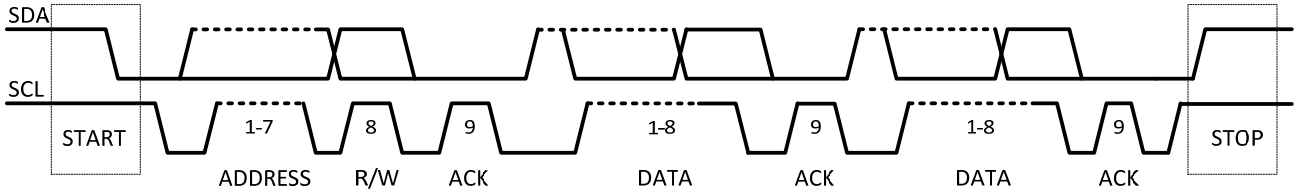



**Figure 12: Byte Format**

If the register address is not defined, the charger IC sends back NACK and returns to an idle state.

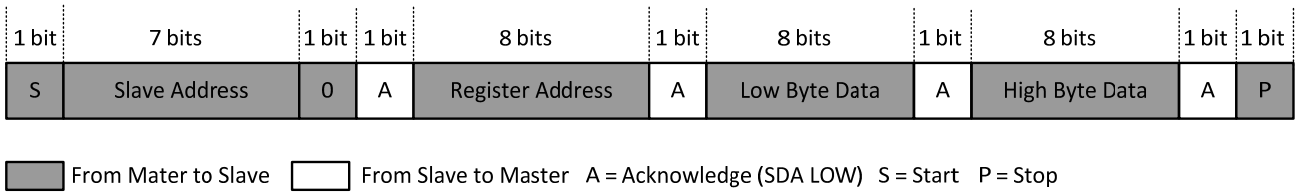



**Figure 13: Singe Word Write**

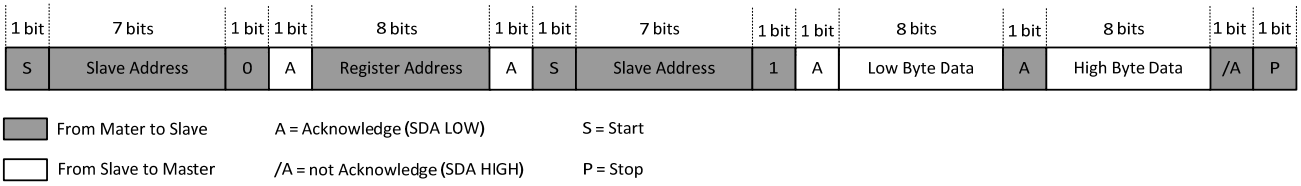



**Figure 14: Single Word Read**

## APPLICATION INFORMATION

### Selecting the Input Capacitor

The input capacitor absorbs the maximum ripple current from the PWM converter. In the buck mode operation, the input current is discontinuous. The RMS ripple current of input cap is calculated by the equation (1):

$$I_{CIN\_RMS} = I_{CHG} x \frac{\sqrt{V_{BATT} x (V_{IN} - V_{BATT})}}{V_{IN}}$$

The worst-case RMS ripple current occurs at 50% duty cycle condition. The battery voltage is approximately 6V to 9V for the 2s battery configuration, so the worst case is when input is 12V to 20V

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor, and should be placed as close as possible to IN and PGND pins of the IC. Their voltage rating must exceed the normal input voltage level. A capacitor with 25V or higher voltage rating is preferred for up to 20V input voltage. 1*1μF + 5*10μF capacitors are suggested for up to 3A input current limit.

Ceramic capacitors show a DC-bias effect. This effect reduces the effective capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. It's necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operation point.

### VCC Decoupling Capacitor

VCC is an internal LDO output. An external 4.7μF decoupling capacitor must be placed between VCC and AGND as close as possible.

### Selecting the Inductor

The MP2651 might be either operated in the buck mode or the boost mode, so the inductor current is equal to either the charging current or the input current. The inductor saturation current should be higher than the larger value of the input current (IIN) or the charging current (ICHG) plus half the ripple current. The inductor current ripples for buck mode and boost mode are calculated with equations (2) and (3), respectively.

$$I_{RIPPLE\_BUCK} = \frac{V_{BATT} x (V_{IN} - V_{BATT})}{V_{IN} x f_{SW} x L}$$

$$I_{RIPPLE\_BOOST} = \frac{V_{IN} x (V_{BATT} - V_{IN})}{V_{BATT} x f_{SW} x L}$$

The inductor ripple current ($I_{RIPPLE}$) depends on the input voltage ($V_{IN}$), the output voltage ($V_{CFLR}$), the switching frequency ($f_{SW}$) and the inductance (L).

The inductance in buck operation can be estimated with Equation (4):

$$L = \frac{V_{BATT} x (V_{IN} - V_{BATT})}{I_{RIPPLE\_BUCK} x V_{IN} x f_{SW}}$$

The required inductance in Boost operation can be estimated with Equation (5):

$$L = \frac{V_{IN} x (V_{BATT} - V_{IN})}{V_{BATT} x f_{SW} x I_{RIPPLE\_BOOST}}$$

The MP2651 has configurable switching frequency from 500kHz to 1.2MHz. Higher switching frequency allows the use of smaller inductor values. Inductor saturation current should be higher than the charging current plus half ripple current.

The maximum input ripple current happens with D = 0.5. For example, the battery charging voltage ranges from 6V to 9V for 2-cell battery pack. For 15V adapter voltage, 7.5V battery voltage gives the maximum inductor ripple current. Another example is 3-cell battery the battery voltage range is from 9V to 13.2V, for 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of 20% to 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

### Selecting the Output Capacitor

The output capacitor ($C_{BATT}$) should have enough ripple current rating to absorb the output AC current.

In the boost mode operation, the output current is discontinuous and dominates the output RMS

ripple current, which can be calculated by the equation (6)

$$I_{CBATT\_BOOST} = I_{CHG} x \frac{\sqrt{V_{IN} \times (V_{BATT} - V_{IN})}}{V_{IN}}$$

The worst case output RMS ripple current occurs at the lowest VBUS input voltage. The CFLR voltage is approximately 8V for the 2s battery configuration, so the worst case is 5V source mode condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the output decoupling capacitor and should be placed close to the CFLR and PGND pins of the IC.

The voltage rating of the capacitor must be higher than the normal battery voltage level. The capacitor with 16V or higher voltage rating is preferred for the 2-cell battery configuration.

### Current Sense

The MP2651 has current loops to limit the current and improve the current accuracy and loop stability. An external current-sense resistor is required to sense the average current. Figure 15 shows a recommended connection.

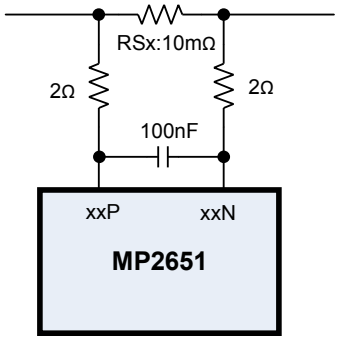



**Figure 15: Input or output current sense circuit**

1. The input current loop to limit the current drawn from the USB port or adapter. The input current is sensed through IAP and IAN pins.
2. The battery current loop to limit the charge current or discharge current. The battery current is sensed through SRP and SRN pins.

### Selecting the Resistive Divider for NTC Thermistor Temperature

In real applications, an external thermistor (negative temperature coefficient) is placed close to the battery to sense the battery's temperature. The MP2651 measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 6). Every temperature corresponds to a voltage ratio. The MP2651 has four temperature thresholds to satisfy JEITA requirements.

For a given NTC thermistor, the NTC hot and cold temperature points can be calculated with Equation (7) and Equation (8), respectively:

$$\frac{R_{T2} + R_{NTC\_HOT}}{R_{T1} + R_{T2} + R_{NTC\_HOT}} = \frac{V_{HOT}}{V_{VNTC}} \quad (7)$$

$$\frac{R_{T2} + R_{NTC\_COLD}}{R_{T1} + R_{T2} + R_{NTC\_COLD}} = \frac{V_{COLD}}{V_{VNTC}} \quad (8)$$

Where $R_{NTC\_HOT}$ is the thermistor value at the expected hot temperature protection point, and $R_{NTC\_COLD}$ is the thermistor value at the expected cold temperature protection point. $V_{HOT}$ / $V_{VNTC}$ and $V_{COLD}$ / $V_{VNTC}$ are 23.6% and 74.5%, respectively.

Assume the expected hot and cold temperature thresholds are 60°C and 0°C. Using a 103AT thermistor as an example, the thermistor values are:

- $R_{NTC\_HOT}$ = 2.981kΩ
- $R_{NTC\_COLD}$ = 28.704kΩ

$R_{T1}$ and $R_{T2}$ can be calculated with Equation (7) or Equation (8). $R_{T1}$ = 9.845kΩ, $R_{T2}$ = 60Ω.

To be simplified a 10kΩ $R_{T1}$ can be used and $R_{T2}$ can be replaced with a wire.

### PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 4-layer PCB is recommended. For the best performance, refer to Figure 16 and follow the guidelines below:

1. Place the output capacitors as close to CFLR and PGND as possible. Place a 1µF small size (such as 0603) capacitor closer than the other 22µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or PGND plane.
2. Place the input capacitors as close to IN and PGND as possible. Place a 1µF small size (such as 0603) capacitor closer than the other 10µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or PGND plane.
3. The connection from CFLR/IN to the 1µF has to be routed on the same layer with the IC, the returning back to PGND also has to be on the same layer with the IC. Keep the whole routing loop as small as possible.
4. Connect AGND to PGND to each decoupling capacitor via a single-point connection.
5. Place the VCC decoupling capacitor and the bootstrap capacitors next to the IC and make trace connections as short as possible.
6. A Kelvin connection is required for the current-sense resistor.
7. Route current sense wires (IAP and IAN, SRP and SRN) away from switching nodes such as SW1 and SW2.

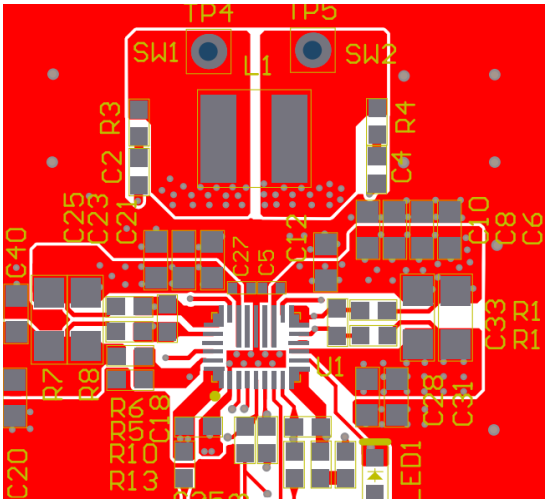



**Figure 16: Recommended PCB Layout**

## Typical Application Circuits

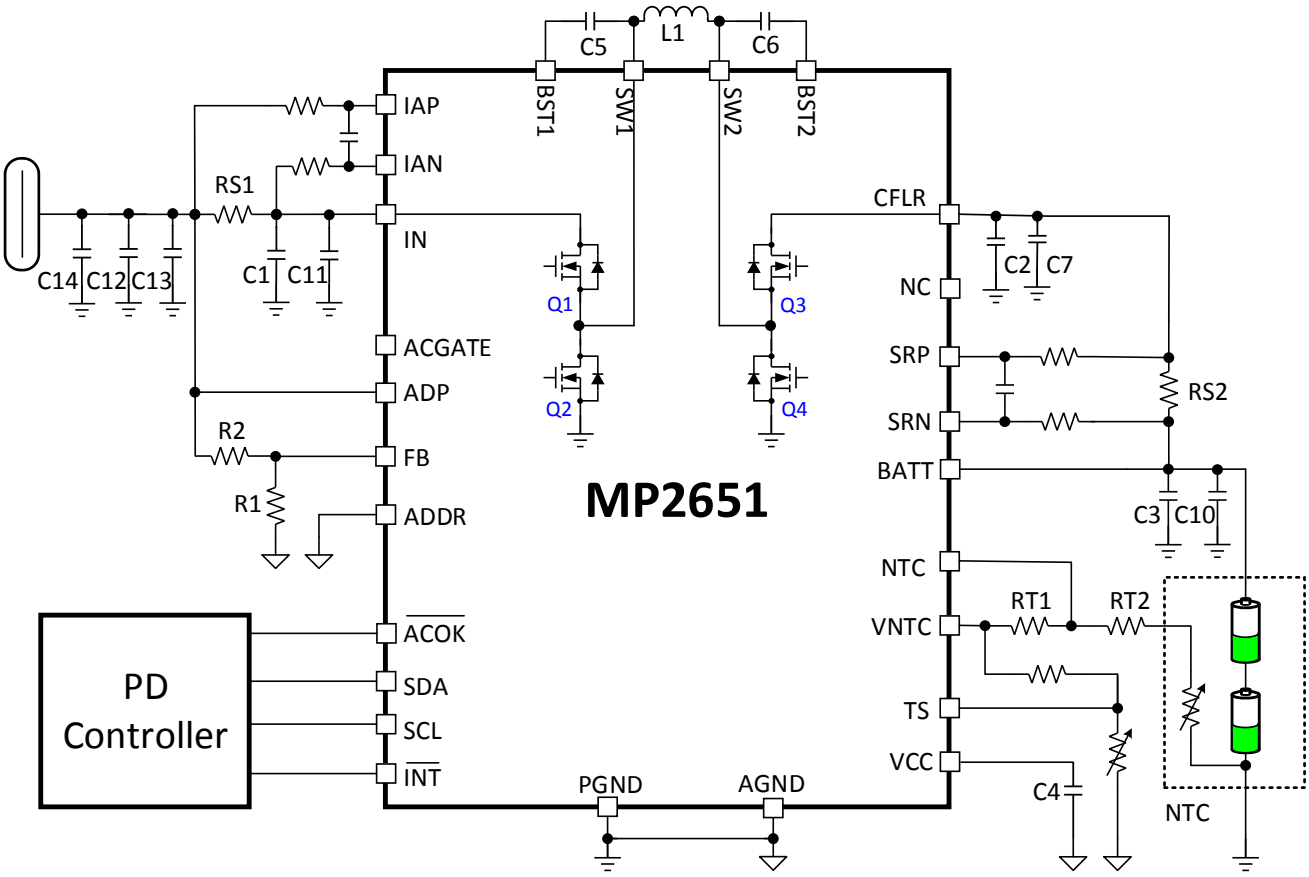



**Figure 17: Typical Application Circuit**

**Table 4: Key BOM for Figure 17**

| Qty | Ref | Value | Description | Package | Manufacturer |
|---|---|---|---|---|---|
| 5 | C1, C11, C12, C13, C14 | 10µF | Ceramic capacitor, 25V, X7S | 0805 | Any |
| 4 | C2, C3,C7, C10 | 22µF | Ceramic capacitor, 25V, X5R or X7R | 0805 | Any |
| 1 | C4 | 4.7µF | Ceramic capacitor, 10V, X5R or X7R | 0603 | Any |
| 2 | C5, C6 | 100nF | Ceramic capacitor, 25V, X5R or X7R | 0603 | Any |
| 1 | L1 | 1.5µH | Inductor, 1.5µH, low DCR, $I_{SAT}$ >14A | SMD | Any |
| 2 | RS1, RS2 | 10mΩ | Film resistor, 1% | 2512 | Any |

## TYPICAL APPLICATION CIRCUITS *(continued)*

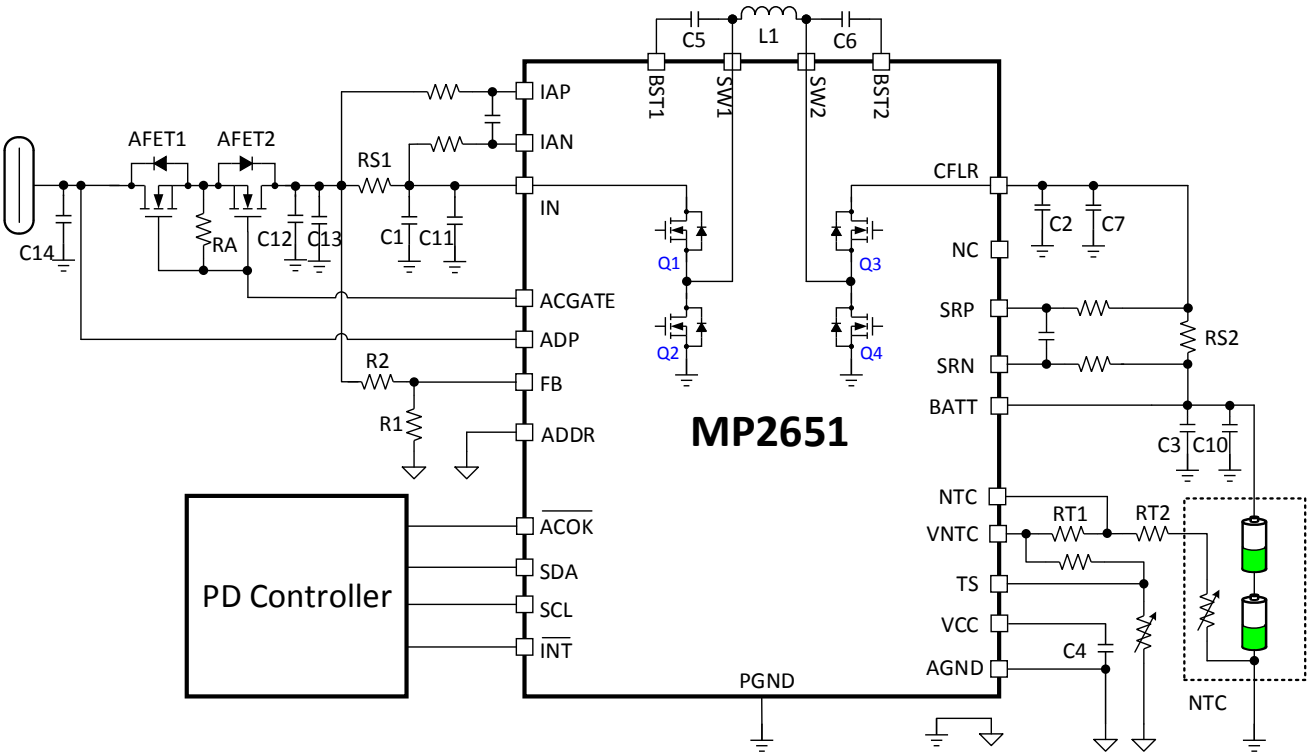



**Figure 18: Typical Application Circuit**

**Table 5: Key BOM for Figure 18**

| Qty | Ref | Value | Description | Package | Manufacturer |
|---|---|---|---|---|---|
| 5 | C1, C11, C12, C13, C14 | 10µF | Ceramic capacitor, 25V, X7S | 0805 | Any |
| 4 | C2, C3, C7, C10 | 22µF | Ceramic capacitor, 25V, X5R or X7R | 0805 | Any |
| 1 | C4 | 4.7µF | Ceramic capacitor, 10V, X5R or X7R | 0603 | Any |
| 2 | C5, C6 | 100nF | Ceramic capacitor, 25V, X5R or X7R | 0603 | Any |
| 1 | L1 | 1.5µH | Inductor, 1.5µH, low DCR, $I_{SAT}$ >14A | SMD | Any |
| 2 | RS1, RS2 | 10mΩ | Film resistor, 1% | 2512 | Any |
| 2 | RA | 5MΩ | Film resistor, 5% | 0603 | Any |
| 2 | AFET1, AFET2, | SISA14DN-T1-GE3 | N-Channel MOSFET; 30V; 5.1mΩ; 20A | Power PAK 1212-8 | Vishay |

## REGISTER MAP

| Register Name | Register Address | OTP | r/w | Description |
|---|---|---|---|---|
| REG05h | 0x05 | Yes | r/w | Device Address Setting |
| REG06h | 0x06 | Yes | r/w | Input Minimum Voltage Limit Setting |
| REG08h | 0x08 | Yes | r/w | Input Current Limit Setting |
| REG09h | 0x09 | No | r/w | Output Voltage Setting in Source Mode |
| REG0Ah | 0x0A | No | r/w | Battery Impedance Compensation and Output Current Limit Setting in Source Mode |
| REG0Bh | 0x0B | Yes | r/w | Battery Low Voltage Threshold and Battery Discharge Current Regulation in Source Mode |
| REG0Ch | 0x0C | No | r/w | JEITA Action Setting |
| REG0Dh | 0x0D | Yes | r/w | Temperature Protection Setting |
| REG0Eh | 0x0E | Yes | r/w | Configuration Register0 |
| REG0Fh | 0x0F | Yes | r/w | Configuration Register1 |
| REG10h | 0x10 | Yes | r/w | Configuration Register2 |
| REG11h | 0x11 | Yes | r/w | Configuration Register3 |
| REG12h | 0x12 | Yes | r/w | Configuration Register4 |
| REG14h | 0x14 | Yes | r/w | Charge Current Setting |
| REG15h | 0x15 | Yes | r/w | Battery-Regulation Voltage Setting |
| REG16h | 0x16 | No | r | Status and Fault Register 0 |
| REG17h | 0x17 | No | r | Status and Fault Register 1 |
| REG18h | 0x18 | No | r/w | INT Mask Setting Register 0 |
| REG19h | 0x19 | No | r/w | INT Mask Setting Register 1 |
| REG22h | 0x22 | No | r | Internal DAC Output of Input Current Limit Setting |
| REG23h | 0x23 | No | r | ADC Result of Input Voltage |
| REG24h | 0x24 | No | r | ADC Result of Input Current |
| REG25h | 0x25 | No | r | ADC Result of Battery Voltage |
| REG27h | 0x27 | No | r | ADC Result of Battery Current |
| REG28h | 0x28 | No | r | ADC Result of NTC Voltage Ratio |
| REG29h | 0x29 | No | r | ADC Result of TS Voltage Ratio |
| REG2Ah | 0x2A | No | r | ADC Result of Junction Temperature |
| REG2Bh | 0x2B | No | r | ADC Result of Battery Discharge Current |
| REG2Ch | 0x2C | No | r | ADC Result of Input Voltage In Discharge Mode |
| REG2 Dh | 0x2D | No | r | ADC Result of Output Current In Discharge Mode |

**NOTES:**

6) The default Device Address is 08h by Address pin connected to AGND. Refer to the section “Address Pin” to get the new device address if REG05h or Address pin connection is modified.

7) OTP in this section means one-time programmable memory.

# REGISTER MAP

## REG05h: Device Address Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 9 | WD_SET | 1 | N | r/w | 0: Disable<br>1: Enable | When this bit is 0, the watchdog timer will be disabled automatically when VIN is absent. |
| 8 | TLOW_EN | 0 | N | r | 0: Disable(I2C)<br>1: Enable(SMBus) | To be compliant to **SMBus,** a 25ms timer is required to release SCL and SDA (reset the communication) if the timer expired. This bit is set to 0 as default. It can be configurable via OTP. |
| 7 | ADDR_CFG | 0 | N | r | 0: ADDR [2:0] is decided by ADDR Pin<br>1: ADDR [2:0] is decided by OTP | This bit is used to decide the way of configuring the device address. It has 0 as default.<br>It can be configurable via OTP. |
| 6 | ADDR[6] | 0 | N | r | | These bits are highest 4 bits of device address. It has 0b0001 as default.<br>It can be configurable via OTP. |
| 5 | ADDR[5] | 0 | N | r | | |
| 4 | ADDR[4] | 0 | N | r | | |
| 3 | ADDR[3] | 1 | N | r | | |
| 2 | ADDR[2] | 0 | N | r | | If ADDR_CFG = 0, ADDR [2:0] are programmed by ADDR pin resistor.<br>If ADDR_CFG=1, ADDR [2:0] are fixed as 0b001. |
| 1 | ADDR[1] | 0 | N | r | | |
| 0 | ADDR[0] | 1 | N | r | | |

### REG06h: Input Minimum Voltage Limit Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-8 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 7 | $V_{IN\_MIN}$[6] | 0 | Y | r/w | 10240mV | These bits are used to set the input minimum voltage limit. It has a 4.56V default and up to 20.4V range.<br>It can be configurable via OTP. |
| 6 | $V_{IN\_MIN}$[6] | 0 | Y | r/w | 5120mV | |
| 5 | $V_{IN\_MIN}$[5] | 1 | Y | r/w | 2560mV | |
| 4 | $V_{IN\_MIN}$[4] | 1 | Y | r/w | 1280mV | |
| 3 | $V_{IN\_MIN}$[3] | 1 | Y | r/w | 640mV | |
| 2 | $V_{IN\_MIN}$[2] | 0 | Y | r/w | 320mV | |
| 1 | $V_{IN\_MIN}$[1] | 0 | Y | r/w | 160mV | |
| 0 | $V_{IN\_MIN}$[0] | 1 | Y | r/w | 80mV | |

### REG08h: Input Current Limit Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-7 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 6 | $I_{IN\_LIM}$[6] | 0 | Y | r/w | 3200mA | These bits are used to set the input current limit. It has a 500mA default and up to 5A range.<br>It can be configurable via OTP.<br><br>Notes: When RS1 changes to 5mΩ, internal gain should also be changed via REG10h, bit [8] and then LSB will keep unchanged. |
| 5 | $I_{IN\_LIM}$[5] | 0 | Y | r/w | 1600mA | |
| 4 | $I_{IN\_LIM}$[4] | 0 | Y | r/w | 800mA | |
| 3 | $I_{IN\_LIM}$[3] | 1 | Y | r/w | 400mA | |
| 2 | $I_{IN\_LIM}$[2] | 0 | Y | r/w | 200mA | |
| 1 | $I_{IN\_LIM}$[1] | 1 | Y | r/w | 100mA | |
| 0 | $I_{IN\_LIM}$[0] | 0 | Y | r/w | 50mA | |

### REG09h: Output Voltage Setting in Source Mode

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-12 | RESERVED | 0 | NA | r/w | Reserved | Reserved |
| 11 | $V_{IN\_SRC\_OS}$ | 0 | N | r/w | 0: 0V<br>1: 0.64V | When this bit is enabled, the $V_{IN\_SRC}$ is DEC (Bit [9:0])+0.64V<br>Default: 0 |
| 10 | $V_{IN\_SRC\_CFG}$ | 0 | N | r/w | 0: Configured by register bit.<br>1: Configured by FB pin. | This bit is used to decide the way of configuring the output voltage in source mode.<br>Default: 0 |
| 9 | $V_{IN\_SRC}$[9] | 0 | N | r/w | 10240mV | These bits are used to set the output voltage in source mode. It has a 4.98V default and up to 20.46V range. |
| 8 | $V_{IN\_SRC}$[8] | 0 | N | r/w | 5120mV | |
| 7 | $V_{IN\_SRC}$[7] | 1 | N | r/w | 2560mV | |
| 6 | $V_{IN\_SRC}$[6] | 1 | N | r/w | 1280mV | |
| 5 | $V_{IN\_SRC}$[5] | 1 | N | r/w | 640mV | |
| 4 | $V_{IN\_SRC}$[4] | 1 | N | r/w | 320mV | |
| 3 | $V_{IN\_SRC}$[3] | 1 | N | r/w | 160mV | |
| 2 | $V_{IN\_SRC}$[2] | 0 | N | r/w | 80mV | |
| 1 | $V_{IN\_SRC}$[1] | 0 | N | r/w | 40mV | |
| 0 | $V_{IN\_SRC}$[0] | 1 | N | r/w | 20mV | |

### REG0Ah: Battery Impedance Compensation and Output Current Limit Setting in Source Mode

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 14 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 13 | BATTR [2] | 0 | Y | r/w | 200mΩ/ Cell | These bits are used to input predicted battery internal impedance and cable impedance. It has a 0 default and 0 to 350mΩ/Cell range. |
| 12 | BATTR [1] | 0 | Y | r/w | 100mΩ/ Cell | |
| 11 | BATTR [0] | 0 | Y | r/w | 50mΩ/ Cell | |
| 10 | $V_{CLAMP}$[2] | 0 | Y | r/w | 240mV/ Cell | These bits are used to set the maximum compensation voltage which should be added to original battery-full regulation voltage if IR compensation function is used. It has a 0mV default and a 0 to 420mV/Cell range. |
| 9 | $V_{CLAMP}$[1] | 0 | Y | r/w | 120mV/ Cell | |
| 8 | $V_{CLAMP}$[0] | 0 | Y | r/w | 60mV/ Cell | |
| 7 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 6 | $I_{IN\_SRC}$ [6] | 0 | Y | r/w | 3200mA | These bits are used to set the output current limit of source mode. It has a 2A default and a 0 to 5.5A range.<br><br>Notes: When RS1 changes to 5mΩ, internal gain should be also changed via REG10h, bit [8] and then LSB will keep unchanged. |
| 5 | $I_{IN\_SRC}$ [5] | 1 | Y | r/w | 1600mA | |
| 4 | $I_{IN\_SRC}$ [4] | 0 | Y | r/w | 800mA | |
| 3 | $I_{IN\_SRC}$ [3] | 1 | Y | r/w | 400mA | |
| 2 | $I_{IN\_SRC}$ [2] | 0 | Y | r/w | 200mA | |
| 1 | $I_{IN\_SRC}$ [1] | 0 | Y | r/w | 100mA | |
| 0 | $I_{IN\_SRC}$ [0] | 0 | Y | r/w | 50mA | |

### REG0Bh: Battery Low Voltage Setting and Battery Discharge Current Regulation in Source Mode

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-14 | RESERVED | NA | NA | NA | Reserved | Reserved |
| 13 | $V_{BATT_LOW}$_EN | 1 | Y | r/w | 0: Disable<br>1: Enable | This bit is used to enable the battery low-voltage protection. It is enabled as default.<br>It can be configurable via OTP. |
| 12 | $V_{BATT\_PRE}$ | 1 | N | r/w | 0: 2.5V/Cell<br>1: 3.0V/Cell | This bit is used to set Pre-charge to CC charge threshold. It has a 3.0V/Cell default. |
| 11 | BATTLOW_ACT | 0 | Y | r/w | 0: Only generate INT<br>1: Generate INT and Latch off DC/DC | This bit is used to decide the behavior of battery low voltage protection when REG0Bh, bit [13] is set to 1. When $V_{BATT}$ < $V_{BATT\_LOW}$ which is set via REG0Bh, bits [10:9], and INT will be asserted to inform the host and DC/DC can also be latched off optionally.<br><br>It has a 0 default.<br>It can be configurable via OTP.<br><br>Notes: Either charging the battery or toggling SRC_EN bit will clear DSCHG_FLT bit. Then the source can be enabled again. When Source Mode is disabled, BATTLOW comparator doesn't operate. |
| 10 | $V_{BATT\_LOW}$ [1] | 0 | N | r/w | 00: 3.0V/Cell<br>01: 3.1V/Cell<br>10: 3.2V/Cell<br>11: 3.3V/Cell | These bits are used to set the low battery voltage threshold for battery low-voltage protection. It has a 3.0V/Cell default. |
| 9 | $V_{BATT\_LOW}$ [0] | 0 | N | r/w | | |
| 8 | $I_{BATT\_DSCHG}$ EN | 0 | N | r/w | 0: disable<br>1: enable | This bit is used to enable the battery discharge current regulation in source mode. It's disabled as default. |
| 7 | $I_{BATT\_DSCHG}$[7] | 1 | N | r/w | 6400mA | These bits are used to set the battery discharge current in source mode. It has 6.4A default and up to 12.75A range. |
| 6 | $I_{BATT\_DSCHG}$[6] | 0 | N | r/w | 3200mA | |
| 5 | $I_{BATT\_DSCHG}$[5] | 0 | N | r/w | 1600mA | |
| 4 | $I_{BATT\_DSCHG}$[4] | 0 | N | r/w | 800mA | |
| 3 | $I_{BATT\_DSCHG}$[3] | 0 | N | r/w | 400mA | |
| 2 | $I_{BATT\_DSCHG}$[2] | 0 | N | r/w | 200mA | |
| 1 | $I_{BATT\_DSCHG}$[1] | 0 | N | r/w | 100mA | |
| 0 | $I_{BATT\_DSCHG}$[0] | 0 | N | r/w | 50mA | |

### REG0Ch: JEITA Action Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | RESERVED | 0 | NA | NA | Reserved | |
| 14 | WARM_ACT [1] | 0 | Y | r/w | 00: No Action;<br>01: Only reduce $V_{BATT\_REG}$<br>10: Only reduce $I_{CC}$<br>11: Reduce both $V_{BATT\_REG}$ and $I_{CC}$ | These bits are used to decide the behavior when NTC warm protection. |
| 13 | WARM_ACT [0] | 1 | Y | r/w | | |
| 12 | COOL_ACT [1] | 1 | Y | r/w | 00: No Action<br>01: Only reduce $V_{BATT\_REG}$<br>10: Only reduce $I_{CC}$<br>11: Reduce both $V_{BATT\_REG}$ and $I_{CC}$ when NTC cool | These bits are used to decide the behavior when NTC cool protection. |
| 11 | COOL_ACT [0] | 0 | Y | r/w | | |
| 10 | JEITA_VSET[4] | 1 | Y | r/w | 320mV/Cell | These bits are used to set the decrease value of the battery-full voltage when NTC cool and warm protection. It has a 320mV/Cell default and up to 620mV/Cell range.<br><br>The battery-full voltage can be set via REG15h. |
| 9 | JEITA_VSET[3] | 0 | Y | r/w | 160mV/Cell | |
| 8 | JEITA_VSET[2] | 0 | Y | r/w | 80mV/Cell | |
| 7 | JEITA_VSET[1] | 0 | Y | r/w | 40mV/Cell | |
| 6 | JEITA_VSET[0] | 0 | Y | r/w | 20mV/Cell | |
| 5 | JEITA_ISET[1] | 0 | Y | r/w | 00: 1/2 times<br>01: 1/4 times<br>10: 1/8 times<br>11: 1/16 times | These bits are used to set the scaling value of the constant current charge current. It has 01 default.<br><br>The constant current charge current can be set via REG14h. |
| 4 | JEITA_ISET[0] | 1 | Y | r/w | | |
| 3-0 | RESERVED | 0 | NA | NA | Reserved | |

### REG0Dh: Temperature Protection Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | TS_EN | 1 | N | r/w | 0: Disable<br>1: Enable | This bit is used to enable the external temperature sense function. It's enabled as default. |
| 14 | RESERVED | 0 | NA | NA | Reserved | Don't change this bit value. |
| 13 | TS_ACT | 1 | Y | r/w | 0: Only deliver INT when reach TS threshold<br>1: Deliver INT and take TS action | This bit is used to decide the behavior when TS over-temperature protection happens. An INT will be asserted after TS over-temperature protection and an additional input current regulation can be taken optionally.<br>It has a 1 default.<br>It can be configurable via OTP. |
| 12 | $V_{TS\_HOT}$[2] | 1 | N | r/w | 000: 9%; (100°C)<br>001: 10%; (95°C)<br>010: 11.3%; (90°C)<br>011: 12.7%; (85°C)<br>100: 14.3%; (80°C)<br>101: 16.1%; (75°C)<br>110: 18.2%; (70°C)<br>111: 20.6%; (65°C) | These bits are used to set TS over-temperature threshold. It has a 14.3% (As a percentage of VNTC) defaut.<br>Notes: Assuming the thermistor is 103AT, pull up resistor is 10kΩ. |
| 11 | $V_{TS\_HOT}$[1] | 0 | N | r/w | | |
| 10 | $V_{TS\_HOT}$[0] | 0 | N | r/w | | |
| 9 | NTC_EN | 1 | N | r/w | 0: Disable<br>1: Enable | This bit is used to enable NTC protection. It is enabled as default. |
| 8 | NTC_ACT | 1 | N | r/w | 0: Only deliver INT when reach NTC threshold<br>1: Deliver INT and take JEITA action | This bit is used to decide the behavior when NTC protection. An INT will be asserted when NTC protection and addition actions can be taken optionally.<br>It has a 1 default value.<br>It can be configurable via OTP. |
| 7 | $V_{HOT}$[1] | 1 | N | r/w | 00: 29.1%; (50°C)<br>01: 25.9%; (55°C)<br>10: 23.0%; (60°C)<br>11: 20.4%; (65°C) | These bits are used to set the "Hot" temperature threshold which is marked as percentage of $V_{NTC}$. It has a 23% default.<br>Notes: Assuming the thermistor is 103AT |
| 6 | $V_{HOT}$[0] | 0 | N | r/w | | |
| 5 | $V_{WARM}$[1] | 0 | N | r/w | 00: 36.5%; (40°C)<br>01: 32.6%; (45°C)<br>10: 29.1%; (50°C)<br>11: 25.9%; (55°C) | These bits are used to set the "Warm" temperature threshold. It has a 32.6% default.<br>Notes: Assuming the thermistor is 103AT |
| 4 | $V_{WARM}$[0] | 1 | N | r/w | | |
| 3 | $V_{COOL}$[1] | 1 | N | r/w | 00: 74.2%; (0°C)<br>01: 69.6%; (5°C)<br>10: 64.8%; (10°C)<br>11: 59.9%; (15°C) | These bits are used to set the "Cool" temperature threshold. It has a 64.8% default.<br>Notes: Assuming the thermistor is 103AT |
| 2 | $V_{COOL}$[0] | 0 | N | r/w | | |
| 1 | $V_{COLD}$[1] | 0 | N | r/w | 00: 78.4%; (-5°C)<br>01: 74.2%; (0°C)<br>10: 69.6%; (5°C)<br>11: 64.8%; (10°C) | These bits are used to set the "Cold" temperature threshold. It has a 74.2% default.<br>Notes: Assuming the thermistor is 103AT |
| 0 | $V_{COLD}$[0] | 1 | N | r/w | | |

### REG0Eh: Configuration Register 0

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15:9 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 8 | ADC_START | 0 | N | r/w | 0: Disable ADC<br>1: Enable ADC | This bit is the enable bit for ADC when it is set to one-shot conversion mode via REG0Eh, bit [7]. At this mode this bit will be back to 0 after conversion done.<br>When DC/DC is enabled, this bit will be always 1 to enable ADC. This bit is read-only when ADC_CONV=1. The bit stays high during ADC conversion. |
| 7 | ADC_CONV | 0 | N | r/w | 0: one shot conversion<br>1: continuous conversion | This bit is used to decide the behavior of ADC conversion. |
| 6 | SW_FREQ[2] | 0 | Y | r/w | 000: 500k<br>001: 600k<br>010: 700k<br>011: 800k<br>100: 750k<br>101: 900k<br>110: 1000k<br>111: 1200k | These bits are used to set the switching frequency of buck-boost converter. It has a 600k default.<br>It can be configurable via OTP. |
| 5 | SW_FREQ[1] | 0 | Y | r/w | | |
| 4 | SW_FREQ[0] | 1 | Y | r/w | | |
| 3-0 | RESERVED | 0 | NA | NA | Reserved | Don’t change this bit value. |

### REG0Fh: Configuration Register 1

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | TJ_REG EN | 1 | Y | r/w | 0: Disable<br>1: Enable | This bit is used to enable the junctional over-temperature regulation. It's enabled as default<br>It can be configurable via OTP. |
| 14 | $T_{J\_REG}$[2] | 1 | Y | r/w | 000: 80ºC<br>001: 90ºC<br>010: 95ºC<br>011: 100ºC<br>100: 105ºC<br>101: 110ºC<br>110: 115ºC<br>111: 120ºC | These bits are used to set the junction temperature regulation point. It has a 120ºC default. |
| 13 | $T_{J\_REG}$[1] | 1 | Y | r/w | | |
| 12 | $T_{J\_REG}$[0] | 1 | Y | r/w | | |
| 11 | $I_{TC}$[3] | 0 | Y | r/w | 400mA | These bits are set the trickle-charge current. It has a 100mA default and a 0 to 750mA range. It can be configurable via OTP. |
| 10 | $I_{TC}$[2] | 0 | Y | r/w | 200mA | |
| 9 | $I_{TC}$[1] | 1 | Y | r/w | 100mA | |
| 8 | $I_{TC}$[0] | 0 | Y | r/w | 50mA | |
| 7 | $I_{PRE}$[7] | 0 | Y | r/w | 800mA | These bits are set the pre-charge current. It has a 400mA default and up to 1.5A range.<br>It can be configurable via OTP. |
| 6 | $I_{PRE}$[6] | 1 | Y | r/w | 400mA | |
| 5 | $I_{PRE}$[5] | 0 | Y | r/w | 200mA | |
| 4 | $I_{PRE}$[4] | 0 | Y | r/w | 100mA | |
| 3 | $I_{TERM}$[3] | 0 | Y | r/w | 400mA | These bits are set the termination current. It has a 200mA default and up to 750mA range.<br>It can be configurable via OTP. |
| 2 | $I_{TERM}$[2] | 1 | Y | r/w | 200mA | |
| 1 | $I_{TERM}$[1] | 0 | Y | r/w | 100mA | |
| 0 | $I_{TERM}$[0] | 0 | Y | r/w | 50mA | |

### REG10h: Configuration Register 2

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 14 | ACGATE_CTRL | 0 | N | r/w | 0: Not force ACGATE on<br>1: Force ACGATE on | This bit is used to control the ACGATE. It can force ACGATE to turn on external MOSFET when it's set to 1. It has a 0 default and ACGATE state depends ADP voltage. |
| 13 | RESERVED | 0 | NA | NA | Reserved | Don't change this bit |
| 12 | TS/IMON | 0 | Y | r/w | 0: TS/IMON pin act as TS<br>1: TS/IMON pin act as IMON | This bit is used to configure the function of the TS/IMON. It's configured to TS function as default.<br>It can be configurable via OTP. |
| 11 | VRECH | 1 | N | r/w | 0: -100mV/cell<br>1: -200mV/cell | This bit is used to set automatic recharge threshold which is comparing to battery-full voltage. It has a -200mV/Cell default.<br>It can be configurable via OTP |
| 10 | BAT_NUM[1] | 0 | N | r/w | 00: 1 cell;<br>01: 2 cell;<br>10: 3 cell;<br>11: 4 cell; | This bit is used to set the battery cells in series. It has a 2cell default.<br>It can be configurable via OTP. |
| 9 | BAT_NUM[0] | 1 | N | r/w | | |
| 8 | IN_RSNS | 0 | N | r/w | 0: 10mΩ<br>1: 5mΩ | This bit is used to set the input current sense gain. It should be set according to external sense resistor RS1. It assumes 10mΩ sense FET is used as default.<br>It can be configurable via OTP. |
| 7 | IBATT_RSNS | 0 | N | r/w | 0: 10mΩ<br>1: 5mΩ | This bit is used to set the battery current sense gain. It should be set according to external sense resistor RS2. It assumes 10mΩ sense FET is used as default.<br>It can be configurable via OTP. |
| 6 | ACGATE_EN | 1 | N | r/w | 0: Disable the ACGAET driver (External ACFET will be off mandatorily)<br>1: Enable ACGATE driver | This bit is used to enable ACGATE driver. It's enabled by default. |
| 5 | RESERVED | 0 | NA | NA | Reserved | Don't change these bits value. |
| 4 | RESERVED | 0 | NA | NA | Reserved | |
| 3 | RESERVED | 0 | NA | NA | Reserved | |
| 2 | RESERVED | 0 | NA | NA | Reserved | |
| 1 | RESERVED | 0 | NA | NA | Reserved | |
| 0 | RESERVED | 0 | NA | NA | Reserved | |

### REG11h: Configuration Register 3

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | Reserved | 0 | NA | NA | Reserved | Reserved |
| 14 | $V_{IN\_SRC\_OV}$ [1] | 1 | N | r/w | 00: 106%;<br>01: 120%;<br>10: 115%;<br>11: 110% | These bits are used to set the over-voltage threshold of source output voltage. It has a 110% default. |
| 13 | $V_{IN\_SRC\_OV}$ [0] | 1 | N | r/w | | |
| 12 | $V_{IN\_SRC\_UV}$ [1] | 0 | N | r/w | 00: 75%;<br>01: 80%;<br>10: 85%;<br>11: 30%; | These bits are used to set the under-voltage threshold of source output voltage. It has a 75% default. |
| 11 | $V_{IN\_SRC\_UV}$ [0] | 0 | N | r/w | | |
| 10 | VIN_OVP_DGL | 0 | N | r/w | 0: 1µs<br>1: 15ms | This bit is used to set deglitch time of input OVP in charging mode. It has a 1µs default |
| 9 | $V_{IN\_UVP}$ [1] | 0 | N | r/w | 00: 3.2V<br>01: 6.4V<br>10: 12V<br>11: 16.8V | These bits are used to set the input under-voltage protection threshold.<br><br>It has a 3.2V default.<br>It can be configurable via OTP. |
| 8 | $V_{IN\_UVP}$ [0] | 0 | N | r/w | | |
| 7 | $V_{IN\_OVP}$ [1] | 1 | N | r/w | 00: 7.2V<br>01: 11.2V<br>10: 17.6V<br>11: 22.4V | These bits are used to set the Input over-voltage protection threshold.<br><br>It has a 22.4V default.<br>It can be configurable via OTP. |
| 6 | $V_{IN\_OVP}$ [0] | 1 | N | r/w | | |
| 5 | RESERVED | 1 | NA | NA | Reserved | Don't change this bit value. |
| 4 | RESERVED | 0 | NA | NA | Reserved | Don't change this bit value. |
| 3 | BATTOVP_EN | 1 | N | r/w | 0: Disable BATT OVP<br>1: Enable BATT OVP | This bit is used to enable BATT OVP. Default. It's enabled by default. |
| 2 | RESERVED | 0 | NA | r/w | Reserved | Don't change this bit value. |
| 1 | RESERVED | 0 | NA | r/w | Reserved | Don't change this bit value. |
| 0 | RESERVED | 0 | NA | r/w | Reserved | Don't change this bit value. |

### REG12h: Configuration Register 4

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | RESERVED | 0 | NA | NA | Reserved | Don't change this bit value. |
| 14 | RESERVED | 0 | NA | NA | Reserved | Don't change this bit value. |
| 13 | TMR_EN | 1 | Y | r/w | 0: Disable<br>1: Enable | This bit enables the charging safety timer (both TC/Pre-charge timer and CC/CV charge timer). It is set to 1 by default.<br>It can be configurable via the OTP. |
| 12 | CHG_TMR[1] | 1 | Y | r/w | 00: 5hours<br>01: 8hours<br>10: 12hours<br>11: 20hours | This bit sets the CC/CV timer. They are set to 11 by default. |
| 11 | CHG_TMR[0] | 1 | Y | r/w | | |
| 10 | TMR2X_EN | 1 | Y | r/w | 0: The safety timer is not doubled during input DPM or thermal regulation.<br>1: The safety timer is doubled during input DMP and thermal regulation. | This bit sets the safety timer during DPM and thermal regulation. It is set to 1 by default. |
| 9 | WTD_RST | 0 | Y | r/w | 0: Normal<br>1: Reset | This $I^2C$ Watchdog Timer Reset<br>Default: (0)<br>Back to 0 after timer is reset. |
| 8 | WTD[1] | 0 | Y | r/w | 00: Disable Timer<br>01: 40s<br>10: 80s<br>11: 175s | This bit sets the $I^2C$ watchdog timer. They are set to 00 by default.<br>It can be configurable via the OTP. |
| 7 | WTD[0] | 0 | Y | r/w | | |
| 6 | DC/DC_EN | 1 | Y | r/w | 0: Disable<br>1: Enable | This bit is used to enable DC/DC. It is set to 1 by default.<br>It can be configurable via OTP. |
| 5 | RESERVED | 0 | NA | NA | Reserved | Don't change this bit value. |
| 4 | TERM_EN | 1 | Y | r/w | 0: Disable<br>1: Enable | This bit is used to enable charge termination. It is set to 1 by default via OTP. |
| 3 | SRC_EN | 0 | Y | r/w | 0: Disable source mode<br>1: Enable source mode | This bit is used to enable source mode configuration. It is set to 0 by default. SRC_EN will over-ride charge enable function. |
| 2 | REG_RST | 0 | Y | r/w | 0: Keep current register setting<br>1: Reset to default register value and reset safety timer | This bit sets the register reset setting. It is set to 0 by default. It resets to 0 after the register is reset. |
| 1 | IINLIM_EN | 1 | Y | r/w | 0: IIN_LIM Disable<br>1: IIN_LIM Enable | This bit is used to enable the input current limit loop. It is set to 1 by default. |
| 0 | CHG_EN | 1 | Y | r/w | 0: Charge Disable<br>1: Charge Enable | This bit configures the charge mode. It is set to 1 by default. SRC_EN overrides the CHG_EN enable function.<br>It can be configurable via the OTP. |

### REG14h: Charge Current Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-14 | Reserved | 0 | NA | NA | Reserved | |
| 13 | $I_{CC}$[7] | 0 | Y | r/w | 6400mA | These bits set the charge current. It has a 0A offset, 0A to 6A range, and is set to 2A by default.<br>It can be configurable via the OTP. |
| 12 | $I_{CC}$[6] | 0 | Y | r/w | 3200mA | |
| 11 | $I_{CC}$[5] | 1 | Y | r/w | 1600mA | |
| 10 | $I_{CC}$[4] | 0 | Y | r/w | 800mA | |
| 9 | $I_{CC}$[3] | 1 | Y | r/w | 400mA | |
| 8 | $I_{CC}$[2] | 0 | Y | r/w | 200mA | |
| 7 | $I_{CC}$[1] | 0 | Y | r/w | 100mA | |
| 6 | $I_{CC}$[0] | 0 | Y | r/w | 50mA | |
| 5-0 | Reserved | 0 | NA | NA | Reserved | Reserved |

### REG15h: Battery Regulation Voltage Setting

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 14 | $V_{BATT\_REG}$[10] | 0 | Y | r/w | 10240mV | These bits set the charge-full voltage. It has a 3.4V/Cell to 4.67V/Cell range for different cell count setting. It is set to 8.4V absolute voltage by default.<br>It can be configurable via the OTP. |
| 13 | $V_{BATT\_REG}$[9] | 1 | Y | r/w | 5120mV | |
| 12 | $V_{BATT\_REG}$[8] | 1 | Y | r/w | 2560mV | |
| 11 | $V_{BATT\_REG}$[7] | 0 | Y | r/w | 1280mV | |
| 10 | $V_{BATT\_REG}$[6] | 1 | Y | r/w | 640mV | |
| 9 | $V_{BATT\_REG}$[5] | 0 | Y | r/w | 320mV | |
| 8 | $V_{BATT\_REG}$[4] | 0 | Y | r/w | 160mV | |
| 7 | $V_{BATT\_REG}$[3] | 1 | Y | r/w | 80mV | |
| 6 | $V_{BATT\_REG}$[2] | 0 | Y | r/w | 40mV | |
| 5 | $V_{BATT\_REG}$[1] | 0 | Y | r/w | 20mV | |
| 4 | $V_{BATT\_REG}$[0] | 0 | Y | r/w | 10mV | |
| 3-0 | RESERVED | 0 | NA | r/w | Reserved | Reserved |

### REG16h: Status and Fault Register 0

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | MD_STAT[1] | 0 | N | r | 00: Shipping<br>01/11: Operation<br>10: Standby | These bits indicate the DC/DC operation status. It asserts INT when state changes. |
| 14 | MD_STAT[0] | 0 | N | r | | |
| 13 | PG_STAT | 0 | N | r | 0: $V_{IN}$ not power good<br>1: $V_{IN}$ power good | This bit indicates the power good status. It is set to 0 by default. It asserts INT when state changes. |
| 12 | SWITCH_STAT[1] | 0 | N | r | 00: IDLE<br>01: BUCK<br>10: BUCK-BOOST<br>11: BOOST | These bits indicate the DC/DC operation mode. It is set to 00 by default. |
| 11 | SWITCH_STAT[0] | 0 | N | r | | |
| 10 | BATT MISS_STAT | 0 | N | r | 0: Normal<br>1: Battery Missing | This bit indicates the battery is missing or not. It is set to 0 by default. |
| 9 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 8 | CHG_STAT [2] | 0 | N | r | 000: No Charging<br>001: Trickle charge<br>010: Pre-charge<br>011: CC charge<br>100: CV charge<br>101: Charge termination | These bits indicate the charging status. They are set to 000 by default.<br>It asserts INT when state changes. |
| 7 | CHG_STAT [1] | 0 | N | r | | |
| 6 | CHG_STAT [0] | 0 | N | r | | |
| 5 | VIN_MIN_STAT | 0 | N | r | 0: Not in input voltage limit<br>1: In input voltage limit | This bit indicates whether the IC stays in the input voltage loop. It is set to 0 by default.<br>It asserts INT when state changes. |
| 4 | IIN_LIM_STAT | 0 | N | r | 0: Not in input current limit<br>1: In input current limit | This bit indicates whether the IC stays in the input current loop. It is set to 0 by default.<br>It asserts INT when state changes. |
| 3 | TJREG_STAT | 0 | N | r | 0: Not in thermal regulation loop<br>1: In thermal regulation loop | This bit indicates whether the IC stays in the thermal regulation loop. It is set to 0 by default.<br>It asserts INT when state changes. |
| 2 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 1 | TS Fault | 0 | N | r | 0: Normal<br>1: TS Hot | This bit indicates a TS related fault happens.<br>It asserts INT when fault happens. |
| 0 | RESERVED | 0 | NA | NA | Reserved | Reserved |

### REG17h: Status and Fault Register 1

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | VIN_SRC _OV | 0 | N | r | 0: Normal<br>1: OVP at VIN in source mode. | This bit indicates output OVP happens in source mode.<br><br>It asserts INT when fault happens. |
| 14 | VIN_SRC _UV | 0 | N | r | 0: Normal<br>1: UVP at VIN in source mode | This bit indicates output UVP happens in source mode.<br><br>It asserts INT when fault happens. |
| 13 | VIN_ OV | 0 | N | r | 0: Normal;<br>1: Input OVP in charge mode | This bit indicates input OVP happens in charging mode.<br><br>It asserts INT when fault happens. |
| 12 | VADP_OV | 0 | N | r | 0: Normal<br>1: VADP OVP | This bit indicates ADP OVP happens in charging mode.<br><br>It asserts INT when fault happens. |
| 11 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 10 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 9 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 8 | VBATT_OV | 0 | N | r | 0: Normal<br>1: Battery OVP | This bit indicates battery OVP happens in charging mode.<br><br>It asserts INT when fault happens. |
| 7 | VBATT LOW | 0 | N | r | 0: Normal<br>1: Discharge stop due to BATT_LOW | This bit indicates low battery voltage in source mode.<br><br>It asserts INT when fault happens. |
| 6 | WTD_EXP | 0 | N | r | 0: Normal;<br>1: Watchdog timer expiration | This bit indicates the watchdog timer expires.<br><br>It asserts INT when fault happens. |
| 5 | CHG TMR_EXP | 0 | N | r | 0: Normal;<br>1: Charge Safety timer expiration | This bit indicates the charge safety timer expires. |
| 4 | THERM_SH DN | 0 | N | r | 0: Normal<br>1: Thermal Shutdown | This bit indicates the thermal shutdown happens.<br><br>It asserts INT when fault happens. |
| 3 | RESERVED | 0 | NA | r/w | Reserved | Reserved |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 2 | NTC_FAULT[2] | 0 | N | r | Charge Mode:<br>000: Normal<br>001: NTC Cold<br>010: NTC Cool<br>011: NTC Warm<br>100: NTC Hot<br>111: NTC Float | Source Mode:<br>000: Normal<br>001: NTC Cold<br>100: NTC Hot<br>111: NTC Float | These bits indicate the NTC faults happens in charging mode.<br><br>It asserts INT when fault happens. |
| 1 | NTC_FAULT[1] | 0 | N | R | | | |
| 0 | NTC_FAULT[0] | 0 | N | R | | | |

### REG18h: INT Mask Setting Register 0

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 14 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 13 | VIN_SRC_FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | For any fault which is masked, the INT will not be asserted when fault happens. But the fault bit will still shows. |
| 12 | VIN_OV_FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 11 | PG_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 10 | BATT_OV_FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 9 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 8 | WTD_FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | For any fault which is masked, the INT will not be asserted when fault happens. But the fault bit will still shows. |
| 7 | BATT LOW_FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 6 | BATT MISS_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 5 | THERM_SHDN | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 4 | TS Fault | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 3 | NTC FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 2 | CHG TMR_FAULT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 1 | MD_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 0 | CHG_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |

### REG19h: INT Mask Setting Register 1

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-3 | RESERVED | 0 | NA | NA | Reserved | Reserved |
| 2 | TJREG_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | For any fault which is masked, the INT will not be asserted when fault happens. But the fault bit will still shows. |
| 1 | VIN_MIN_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |
| 0 | IIN_LIM_STAT | 0 | Y | r/w | 0: Masked<br>1: Not masked | |

### REG22h: Internal DAC Output of Input Current Limit

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-7 | Reserved | 0 | NA | NA | Reserved | Reserved |
| 6 | $I_{IN\_DPM}$[6] | 0 | N | r | 3200mA | These bits only indicate the real input current limit value, which is read-only. |
| 5 | $I_{IN\_DPM}$[5] | 0 | N | r | 1600mA | |
| 4 | $I_{IN\_DPM}$[4] | 0 | N | r | 800mA | |
| 3 | $I_{IN\_DPM}$[3] | 0 | N | r | 400mA | |
| 2 | $I_{IN\_DPM}$[2] | 0 | N | r | 200mA | |
| 1 | $I_{IN\_DPM}$[1] | 0 | N | r | 100mA | |
| 0 | $I_{IN\_DPM}$[0] | 0 | N | r | 50mA | |

### REG23h: ADC Result of Input Voltage

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $V_{IN}$[9] | NA | NA | r | 10240mV | These bits indicate the ADC conversion of the input voltage |
| 8 | $V_{IN}$[8] | NA | NA | r | 5120mV | |
| 7 | $V_{IN}$[7] | NA | NA | r | 2560mV | |
| 6 | $V_{IN}$[6] | NA | NA | r | 1280mV | |
| 5 | $V_{IN}$[5] | NA | NA | r | 640mV | |
| 4 | $V_{IN}$[4] | NA | NA | r | 320mV | |
| 3 | $V_{IN}$[3] | NA | NA | r | 160mV | |
| 2 | $V_{IN}$[2] | NA | NA | r | 80mV | |
| 1 | $V_{IN}$[1] | NA | NA | r | 40mV | |
| 0 | $V_{IN}$[0] | NA | NA | r | 20mV | |

### REG24h: ADC Result of Input Current

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $I_{IN}$[9] | NA | NA | r | 3200mA | These bits indicate the ADC conversion of the input current. |
| 8 | $I_{IN}$[8] | NA | NA | r | 1600mA | |
| 7 | $I_{IN}$[7] | NA | NA | r | 800mA | |
| 6 | $I_{IN}$[6] | NA | NA | r | 400mA | |
| 5 | $I_{IN}$[5] | NA | NA | r | 200mA | |
| 4 | $I_{IN}$[4] | NA | NA | r | 100mA | |
| 3 | $I_{IN}$[3] | NA | NA | r | 50mA | |
| 2 | $I_{IN}$[2] | NA | NA | r | 25mA | |
| 1 | $I_{IN}$[1] | NA | NA | r | 12.5mA | |
| 0 | $I_{IN}$[0] | NA | NA | r | 6.25mA | |

### REG25h: ADC Result of Battery Voltage Per Cell

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $V_{BATT}$[9] | NA | NA | r | 2560 mV/Cell | These bits indicate the ADC conversion of the battery voltage per Cell.<br>The real battery voltage should be the value read times cell numbers. |
| 8 | $V_{BATT}$[8] | NA | NA | r | 1280 mV/Cell | |
| 7 | $V_{BATT}$[7] | NA | NA | r | 640 mV/Cell | |
| 6 | $V_{BATT}$[6] | NA | NA | r | 320 mV/Cell | |
| 5 | $V_{BATT}$[5] | NA | NA | r | 160 mV/Cell | |
| 4 | $V_{BATT}$[4] | NA | NA | r | 80 mV/Cell | |
| 3 | $V_{BATT}$[3] | NA | NA | r | 40 mV/Cell | |
| 2 | $V_{BATT}$[2] | NA | NA | r | 20 mV/Cell | |
| 1 | $V_{BATT}$[1] | NA | NA | r | 10 mV/Cell | |
| 0 | $V_{BATT}$[0] | NA | NA | r | 5 mV/Cell | |

### REG27h: ADC Result of Battery Charge Current

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $I_{BATT}$[9] | NA | NA | r | 6400mA | ADC conversion of Charge Current by external 10mΩ sense resistor. |
| 8 | $I_{BATT}$[8] | NA | NA | r | 3200mA | |
| 7 | $I_{BATT}$[7] | NA | NA | r | 1600mA | |
| 6 | $I_{BATT}$[6] | NA | NA | r | 800mA | |
| 5 | $I_{BATT}$[5] | NA | NA | r | 400mA | |
| 4 | $I_{BATT}$[4] | NA | NA | r | 200mA | |
| 3 | $I_{BATT}$[3] | NA | NA | r | 100mA | |
| 2 | $I_{BATT}$[2] | NA | NA | r | 50mA | |
| 1 | $I_{BATT}$[1] | NA | NA | r | 25mA | |
| 0 | $I_{BATT}$[0] | NA | NA | r | 12.5mA | |

### REG28h: ADC Result of NTC Sense Ratio

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | NTC[9] | NA | NA | r | 512/1024 | These bits indicate the ADC conversion of NTC voltage percentage of VNTC. The real battery temperature can be recalculated according to external divider and thermistor datasheet. |
| 8 | NTC[8] | NA | NA | r | 256/1024 | |
| 7 | NTC[7] | NA | NA | r | 128/1024 | |
| 6 | NTC[6] | NA | NA | r | 64/1024 | |
| 5 | NTC[5] | NA | NA | r | 32/1024 | |
| 4 | NTC[4] | NA | NA | r | 16/1024 | |
| 3 | NTC[3] | NA | NA | r | 8/1024 | |
| 2 | NTC[2] | NA | NA | r | 4/1024 | |
| 1 | NTC[1] | NA | NA | r | 2/1024 | |
| 0 | NTC[0] | NA | NA | r | 1/1024 | |

### REG29h: ADC Result of TS Sense Ratio

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-8 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | TS[9] | NA | NA | r | 512/1024 | These bits indicate the ADC conversion of TS voltage percentage of VNTC. |
| 8 | TS[8] | NA | NA | r | 256/1024 | |
| 7 | TS[7] | NA | NA | r | 128/1024 | |
| 6 | TS[6] | NA | NA | r | 64/1024 | |
| 5 | TS[5] | NA | NA | r | 32/1024 | |
| 4 | TS[4] | NA | NA | r | 16/1024 | |
| 3 | TS[3] | NA | NA | r | 8/1024 | |
| 2 | TS[2] | NA | NA | r | 4/1024 | |
| 1 | TS[1] | NA | NA | r | 2/1024 | |
| 0 | TS[0] | NA | NA | r | 1/1024 | |

### REG2Ah: ADC Result of Junction Temperature

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | TJ[9] | NA | NA | r | 512 | These bits indicate the ADC conversion of Junction Temperature<br>$T_J$=314 – 0.5703 x REG2A[9:0] |
| 8 | TJ[8] | NA | NA | r | 256 | |
| 7 | TJ[7] | NA | NA | r | 128 | |
| 6 | TJ[6] | NA | NA | r | 64 | |
| 5 | TJ[5] | NA | NA | r | 32 | |
| 4 | TJ[4] | NA | NA | r | 16 | |
| 3 | TJ[3] | NA | NA | r | 8 | |
| 2 | TJ[2] | NA | NA | r | 4 | |
| 1 | TJ[1] | NA | NA | r | 2 | |
| 0 | TJ[0] | NA | NA | r | 1 | |

### REG2Bh: ADC Result of Battery Discharge Current

| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-8 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $I_{BATT\_DIS}$[9] | NA | NA | r | 6400mA | These bits indicate the ADC conversion of battery discharge charge current. |
| 8 | $I_{BATT\_DIS}$[8] | NA | NA | r | 3200mA | |
| 7 | $I_{BATT\_DIS}$[7] | NA | NA | r | 1600mA | |
| 6 | $I_{BATT\_DIS}$[6] | NA | NA | r | 800mA | |
| 5 | $I_{BATT\_DIS}$[5] | NA | NA | r | 400mA | |
| 4 | $I_{BATT\_DIS}$[4] | NA | NA | r | 200mA | |
| 3 | $I_{BATT\_DIS}$[3] | NA | NA | r | 100mA | |
| 2 | $I_{BATT\_DIS}$[2] | NA | NA | r | 50mA | |
| 1 | $I_{BATT\_DIS}$[1] | NA | NA | r | 25mA | |
| 0 | $I_{BATT\_DIS}$[0] | NA | NA | r | 12.5mA | |

### REG2Ch: ADC Result of Input Voltage in Source Mode

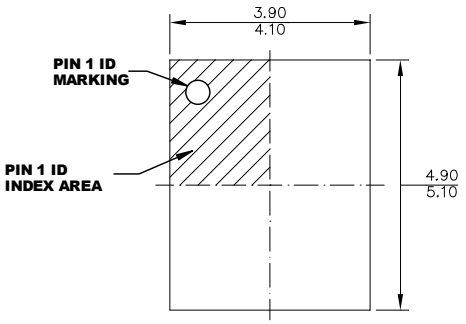
| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-10 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $V_{IN\_SRC}$[9] | NA | NA | r | 10240mV | These bits indicate the ADC conversion of the output voltage at IN pin in source mode |
| 8 | $V_{IN\_SRC}$[8] | NA | NA | r | 5120mV | |
| 7 | $V_{IN\_SRC}$[7] | NA | NA | r | 2560mV | |
| 6 | $V_{IN\_SRC}$[6] | NA | NA | r | 1280mV | |
| 5 | $V_{IN\_SRC}$[5] | NA | NA | r | 640mV | |
| 4 | $V_{IN\_SRC}$[4] | NA | NA | r | 320mV | |
| 3 | $V_{IN\_SRC}$[3] | NA | NA | r | 160mV | |
| 2 | $V_{IN\_SRC}$[2] | NA | NA | r | 80mV | |
| 1 | $V_{IN\_SRC}$[1] | NA | NA | r | 40mV | |
| 0 | $V_{IN\_SRC}$[0] | NA | NA | r | 20mV | |

### REG2Dh: ADC Result of Output Current in Source Mode

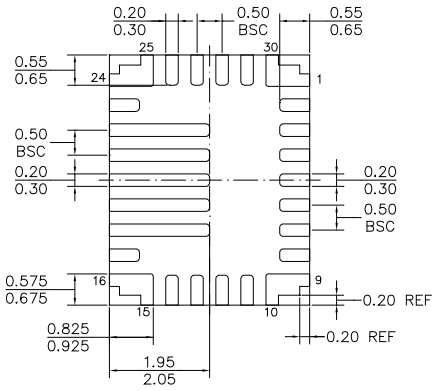
| Bit | Name | Default | Reset by WTD | r/w | Description | Comment |
|---|---|---|---|---|---|---|
| 15-8 | Reserved | NA | NA | NA | Reserved | Reserved |
| 9 | $I_{IN\_SRC}$[9] | NA | NA | r | 3200mA | These bits indicate the ADC conversion of the output current in source mode. |
| 8 | $I_{IN\_SRC}$[8] | NA | NA | r | 1600mA | |
| 7 | $I_{IN\_SRC}$[7] | NA | NA | r | 800mA | |
| 6 | $I_{IN\_SRC}$[6] | NA | NA | r | 400mA | |
| 5 | $I_{IN\_SRC}$[5] | NA | NA | r | 200mA | |
| 4 | $I_{IN\_SRC}$[4] | NA | NA | r | 100mA | |
| 3 | $I_{IN\_SRC}$[3] | NA | NA | r | 50mA | |
| 2 | $I_{IN\_SRC}$[2] | NA | NA | r | 25mA | |
| 1 | $I_{IN\_SRC}$[1] | NA | NA | r | 12.5mA | |
| 0 | $I_{IN\_SRC}$[0] | NA | NA | r | 6.25mA | |

# PACKAGE INFORMATION

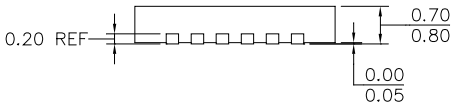
**TQFN-30 (4mm×5mm)**



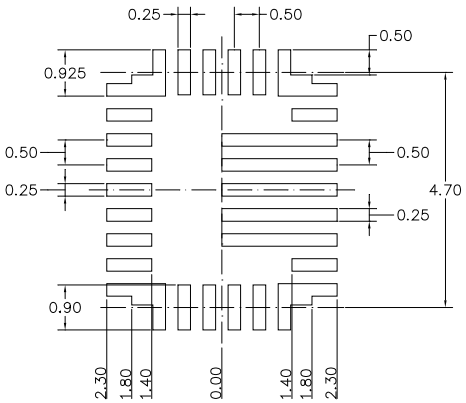

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**

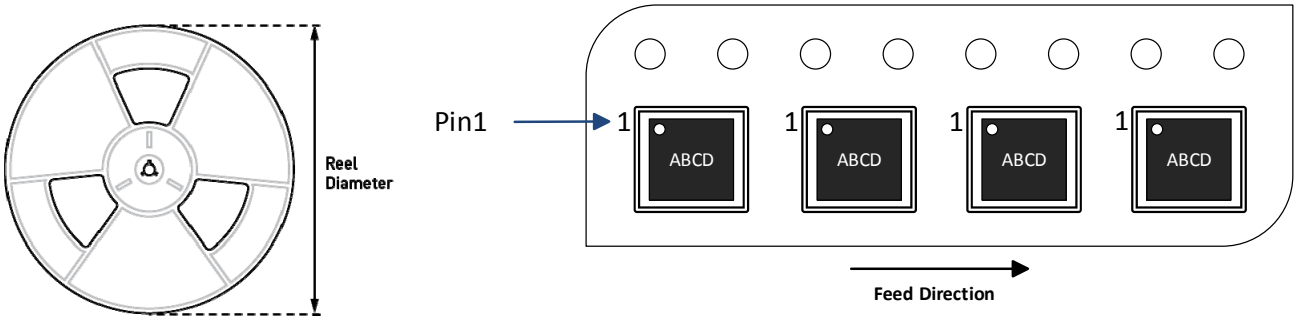



**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantiy/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP2651GVT-xxxx-Z | TQFN-30 (4mm×5mm) | 5000 | N/A | N/A | 13 in. | 12 mm | 8 mm |