# 8.5V High Efficiency High PSRR Low Noise Large Volume 2-in-1 TLTR-AGC 3rd Generation Smart K Audio Amplifier

## FEATURES

- Triple-Level Triple-Rate AGC algorithm to effectively eliminate noise, pure sound quality
- High efficiency large drive ability BOOST
- Highest voltage：8.5V
- Overall efficiency up to 80%
- Output Power：4.3W@8Ω，5.3W@6Ω
- High PSRR：-82dB（217Hz）
- Low noise：
  - 18 μV (Class D Receiver THD+N=0.03%)
  - 43 μV (Class K Speaker THD+N=0.04%)
- Selectable speaker-guard power level：0.5W~2W@8ohm, 100mW/step
- Speaker & receiver 2-in-1 mode application
- Battery tracking AGC selectable, for low voltage protection
- Shutdown current：0.1μA
- Super TDD-Noise suppression
- Excellent pop-click suppression
- Support 1.8V logic I²C control
- FCQFN 2.0mmX3.0mmX0.55mm-20L package

## APPLICATIONS

- Smart phone、Tablet PC

## DESCRIPTION

AW87519 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality. It is a new high efficiency, high PSRR，low noise, constant large volume, 3rd generation Smart K audio amplifier. AW87519 integrates AWINIC's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87519 integrates high voltage synchronous Boost with efficiency up to 88% as the class D power stage supply, significantly improving the dynamic range of music. AW87519 noise floor is as low as to 43μV at speaker mode, with 103dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.04% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87519 supports speaker and receiver 2-in-1 application. In the receiver mode, its ultra-low noise is 18μV. Class D receiver also has high PSRR performance to completely suppress TDD-noise.

AW87519 controls internal registers through the I²C interface. Register parameters include boost output voltage, boost maximum input peak current, PA gain, Triple-Level Triple-Rate AGC parameters, etc.

AW87519 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87519 features small FCQFN 2.0mmX3.0mmX0.55mm-20L package.

## TYPICAL APPLICATION CIRCUIT

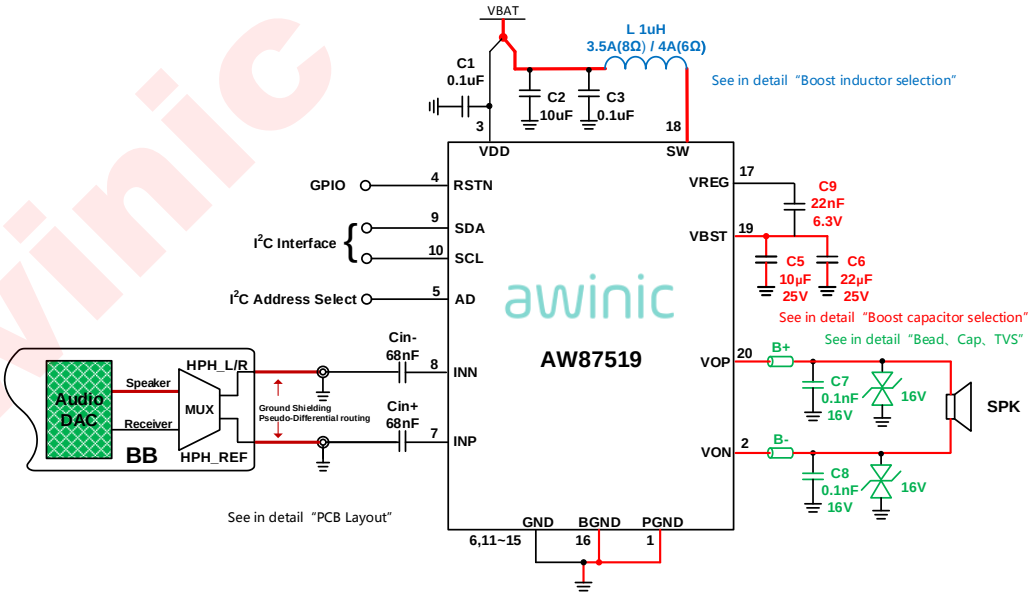


**Figure 1 AW87519 Single-ended Input Mode Application Diagram**

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## PIN CONFIGURATION AND TOP MARK

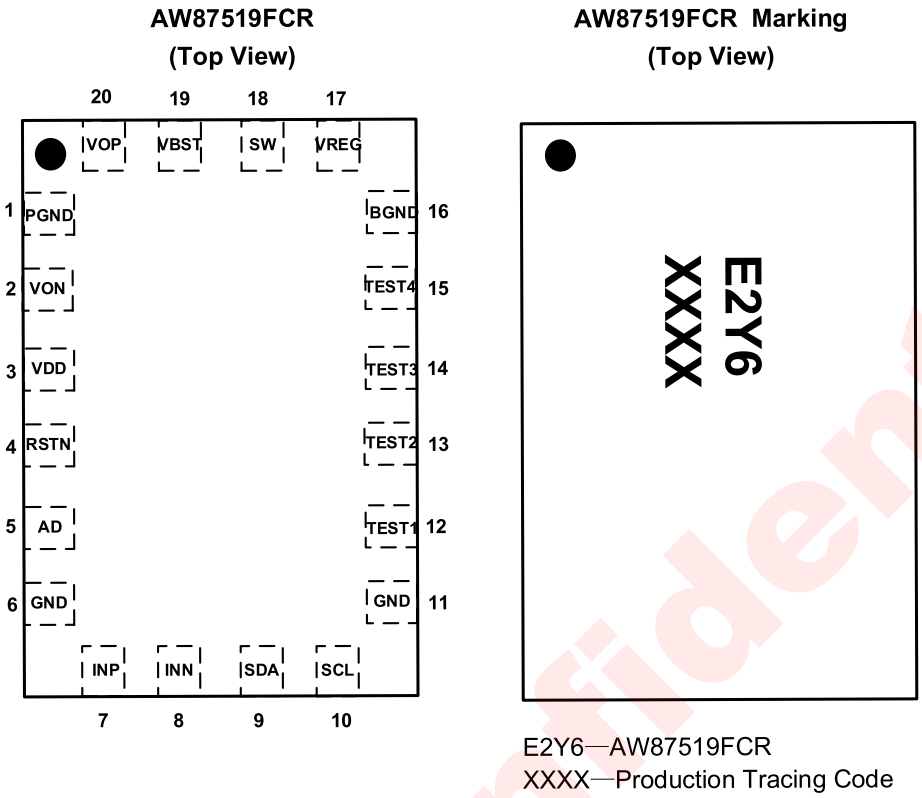


**Figure 2 AW87519FCR Pin configuration and Top Mark**

## PIN DESCRIPTION

| Number | Symbol | Description |
|---|---|---|
| 1 | PGND | Class D power ground |
| 2 | VON | Negative audio output terminal |
| 3 | VDD | Power supply |
| 4 | RSTN | Reset pin, active low reset, the internal 2MΩ pull-down resistor in chip |
| 5 | AD | I²C address pin |
| 6 | GND | Ground |
| 7 | INP | Positive audio input terminal |
| 8 | INN | Negative audio input terminal |
| 9 | SDA | I²C-bus data input/output |
| 10 | SCL | I²C-bus clock input |
| 11 | GND | Ground |
| 12~15 | TEST1~TEST4 | TEST pins，connect to GND in application |

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| | | |
|---|---|---|
| 16 | BGND | Boost power ground |
| 17 | VREG | Charge pump output pin |
| 18 | SW | Boost switch pin |
| 19 | VBST | Boost output pin |
| 20 | VOP | Positive audio output terminal |

## FUNCTIONAL DIAGRAM

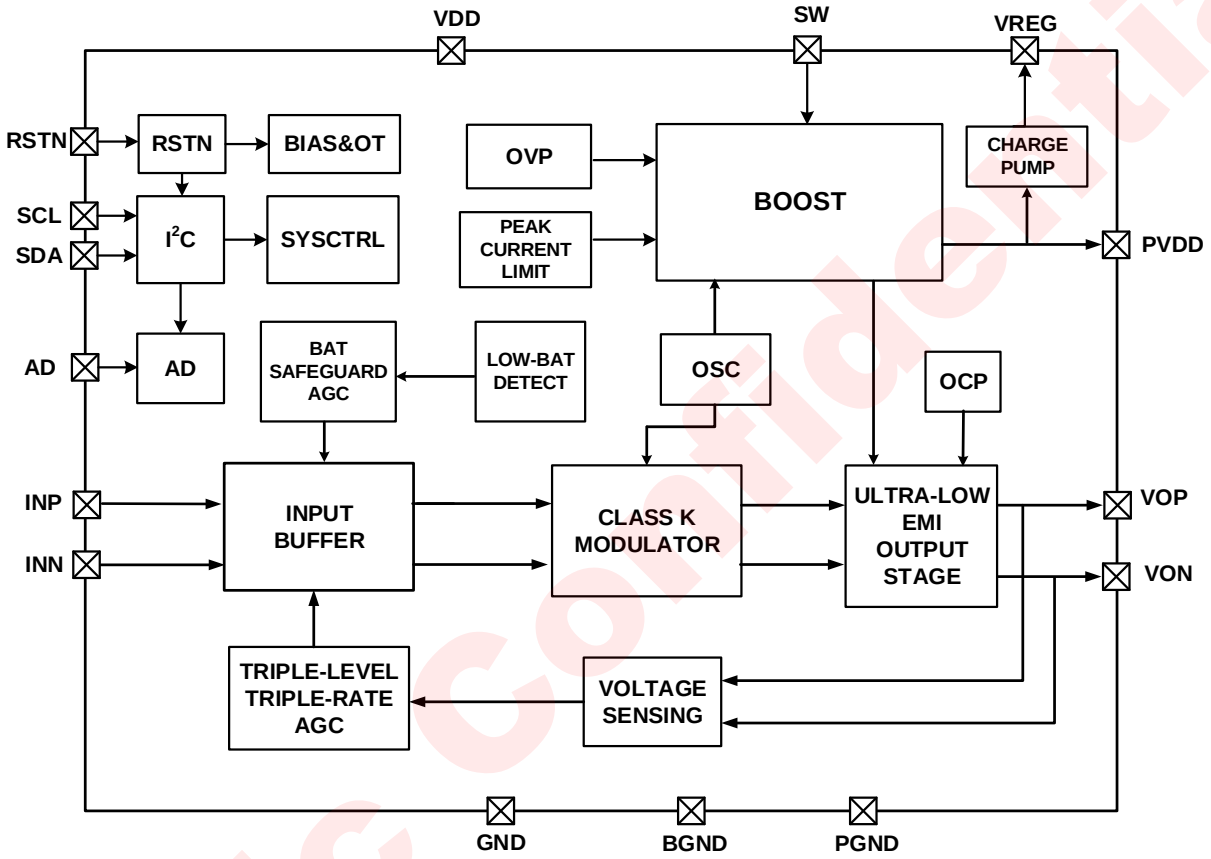


**Figure 3 AW87519 Functional Diagram**

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# TYPICAL APPLICATION CIRCUIT

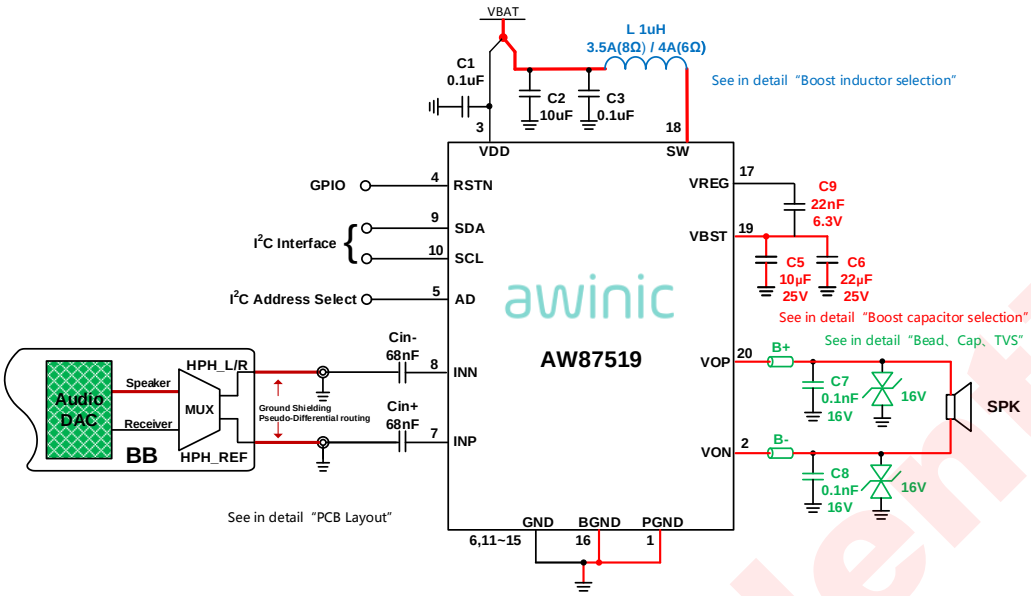


**Figure 4 AW87519 Single-ended Input Mode Application Diagram**(Note 1)

***Note1：****When single-ended input, audio signal line from audio DAC (HPH_L or HPH_R) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPH_REF) through input capacitor and resistor.*

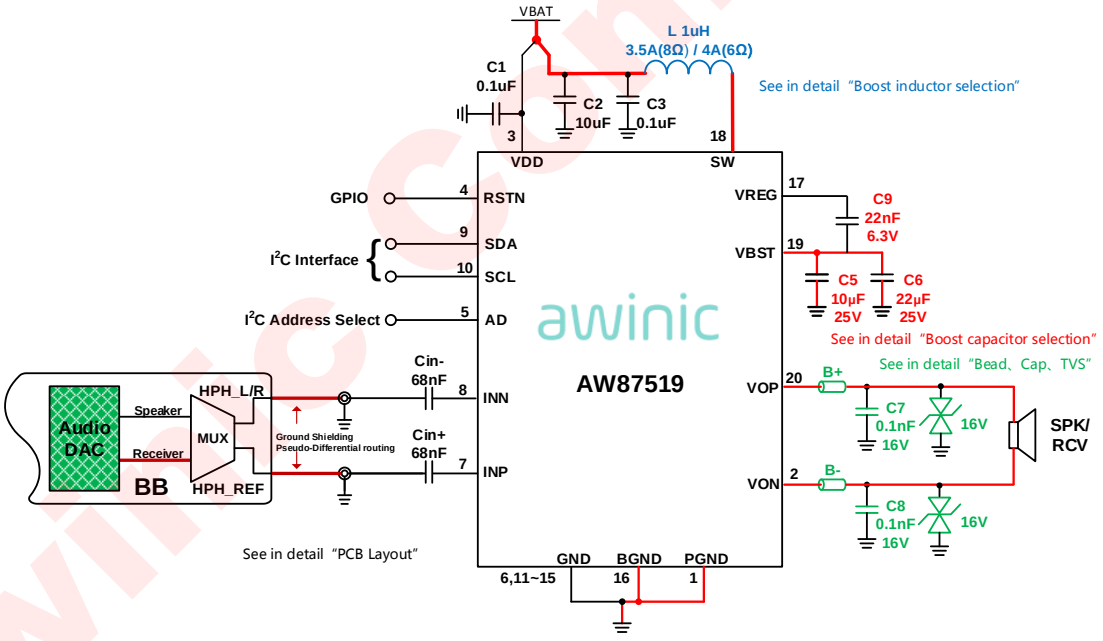


**Figure 5 AW87519 Speaker & Receiver 2-in-1 Mode Application Diagram**

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## ORDERING INFORMATION

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AW87519FCR | -40°C～85°C | FCQFN 2.0mmX3.0mm-20L | E2Y6 | MSL1 | ROHS+HF | 6000 units/ Tape and Reel |

## ABSOLUTE MAXIMUM RATING (Note2)

| Parameter | Range |
|---|---|
| Supply Voltage $V_{DD}$ | -0.3V to 6V |
| INN,INP | -0.3V to VDD+0.3V |
| Boost output voltage PVDD | -0.3V to 12V |
| SW | -0.3V to PVDD+2V |
| VOP,VON | -0.3V to PVDD+0.3V |
| Minimum load resistance $R_L$ | 5Ω |
| Package Thermal Resistance $\theta_{JA}$ | 57.9°C/W |
| Ambient Temperature Range | -40°C to 85°C |
| Maximum Junction Temperature $T_{JMAX}$ | 165°C |
| Storage Temperature Range $T_{STG}$ | -65°C to 150°C |
| Lead Temperature（Soldering 10 Seconds） | 260°C |
| ESD Rating (Note 3) | |
| HBM（human body model） | ±2kV |
| CDM（charged-device model） | ±1.5kV |
| Latch-up | |
| Test Condition：JEDEC STANDARD NO.78E | +IT：450mA<br>-IT：-450mA |

**NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.**

**NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017**

**Test method of the charge device model: ESDA/JEDEC JS-002-2014**

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## ELECTRICAL CHARACTERISTICS

Test condition：$T_A$=25°C, VDD=4.2V, PVDD=8.5V, $R_L$=8Ω+33μH, f=1kHz（unless otherwise noted）

| Parameter | | Test conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 2.8 | | 5.5 | V |
| UVLO | Under-voltage protection voltage | | | 2.5 | | V |
| | Under-voltage protection hysteresis voltage | | | 100 | | mV |
| $V_{IH}$ | RSTN, SCL, SDA, AD high-level input voltage | | 1.3 | | $V_{DD}$ | V |
| $V_{IL}$ | RSTN, SCL, SDA, AD low-level input voltage | | 0 | | 0.45 | V |
| $I_{SD}$ | Shutdown current | $V_{DD}$=3.6V, RSTN=0V | | 0.1 | 1 | μA |
| $T_{TG}$ | Thermal AGC start temperature threshold | | | 150 | | ℃ |
| $T_{TGR}$ | Thermal AGC exit temperature threshold | | | 130 | | ℃ |
| $T_{SD}$ | Over temperature protection threshold | | | 160 | | °C |
| $T_{SDR}$ | Over temperature protection recovery threshold | | | 130 | | °C |
| $T_{ON}$ | Turn-On time | | | 45 | | ms |
| **BOOST** | | | | | | |
| VBST | BOOST Output voltage | $V_{DD}$=2.8V to 5.5V | | 8.5 (Note4) | | V |
| OVP | OVP voltage | $V_{DD}$=2.8V to 5.5V | | VBST+0.5 | | V |
| | OVP hysteresis voltage | $V_{DD}$=2.8V to 5.5V | | 500 | | mV |
| $I_{L_PEAK}$ | Inductor peak current limit | | | 3.5 (Note4) | | A |
| $F_{BST}$ | Boost operating frequency | $V_{DD}$=2.8V to 5.5V | | 1.6 | | MHz |
| | Soft-start Switching frequency | | | 0.4 | | MHz |
| $D_{MAX}$ | The maximum duty cycle | | | 90 | | % |
| $T_{ST}$ | Soft-start time | No load，$C_{OUT}$=22μF | | 2 | | ms |
| $\eta_{CP}$ | Boost efficiency | $V_{DD}$=4.2V, $I_{load}$=200mA | | 88 | | % |
| **CLASS K MODE** | | | | | | |
| $V_{OS}$ | Output offset voltage | No input | -30 | 0 | 30 | mV |
| $\eta_T$ | total efficiency (BOOST+CLASS D) | $V_{DD}$=4.2V, Po=2.5W, $R_L$=8Ω+33μH | | 80 | | % |
| $I_{QK}$ | Speaker Quiescent current | $V_{DD}$=4.2V, input ac grounded, $R_L$=8Ω+33μH | | 16.5 | | mA |

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| Parameter | | Test conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $R_{dson}$ | Drain-Source on-state resistance | High side MOS + Low side MOS | | | 250 | | mΩ |
| Vinp | Recommended input signal amplitude | $V_{DD}$=2.8V to 5.5V | | | | 1 | Vp |
| Fosc | Modulation frequency | $V_{DD}$=2.8V to 5.5V | | 600 | | 1000 | kHz |
| Pagc | TLTR AGC power | $R_L$=8Ω+33μH | | 0.72 | 0.8 (Note4) | 0.88 | W |
| | | $R_L$=6Ω+33μH | | 0.96 | 1.067 (Note4) | 1.17 | W |
| PSRR | Power supply rejection ratio | $V_{DD}$=4.2V, Vpp_sin=200 mV | 217Hz | | -78 | | dB |
| | | | 1kHz | | -80 | | dB |
| SNR | Signal-to-noise ratio | $V_{DD}$=4.2V, Po=4.3W, Av=18dB ,$R_L$=8Ω+33μH, | | | 103 | | dB |
| | | $V_{DD}$=4.2V, Po=0.8W, Av=18dB,$R_L$=8Ω+33μH, | | | 94 | | dB |
| $E_N$ | Speaker Output noise | Av=24dB | 20Hz to 20kHz, input ac grounded, A-weighting | | 53 | | μV |
| | | Av=18dB | | | 43 | | |
| Av | Speaker gain | $V_{DD}$=2.8V to 5.5V | | | 24 (Note4) | | dB |
| Rini | Speaker Inner input resistance | Av=24dB | | | 9 | | kΩ |
| | Speaker Inner input resistance | Av=18dB | | | 18 | | |
| Fin | Speaker input Cut-off frequency | Cin=68nF, Av=24dB | | | 260 | | Hz |
| | Speaker input Cut-off frequency | Cin=68nF, Av=18dB | | | 130 | | |
| THD+N | Total harmonic distortion + noise | VDD=4.2V, Po=0.6W, RL=8Ω+33μH, f=1kHz | | | 0.04 | | % |
| Po | Speaker Output Power | THD+N=1%, $R_L$=8Ω+33μH, $V_{DD}$=4.2V, PVDD=8.5V, $I_{L_PEAK}$=4A | | | 4.3 | | W |
| | | THD+N=10%, $R_L$=8Ω+33μH, $V_{DD}$=4.2V, PVDD=8.5V, $I_{L_PEAK}$=4A | | | 5.2 | | W |
| | | THD+N=1%, $R_L$=6Ω+33μH, $V_{DD}$=4.2V, PVDD=8.5V, $I_{L_PEAK}$=4A | | | 5.3 | | W |
| | | THD+N=10% , $R_L$=6Ω+33μH, $V_{DD}$=4.2V, PVDD=8.5V, $I_{L_PEAK}$=4A | | | 6.3 | | W |
| **2-in-1 Receiver MODE** | | | | | | | |
| $I_{QD}$ | D Receiver quiescent current（overall） | $V_{DD}$=4.2V, input ac grounded, $R_L$=8Ω+33μH | | | 6.8 | | mA |

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| Parameter | | Test conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $\eta_D$ | CLASS D Receiver efficiency | $V_{DD}$=4.2V,Po=0.8W, $R_L$=8Ω+33μH | | | 90 | | % |
| Av | gain | $V_{DD}$=2.8V to 5.5V | | | 7.5 (Note4) | | dB |
| Rini | CLASS D Receiver Inner input resistance | Av=9dB | | | 24 | | kΩ |
| Fin | CLASS D Receiver input cut-off frequency | Cin=68nF, Av=9dB | | | 98 | | Hz |
| $E_N$ | CLASS D Receiver output noise | Av=7.5dB | 20Hz to 20kHz, input ac grounded, A-weighting | | 18 | | μV |
| | | Av=9dB | | | 21 | | μV |
| THD+N | Total harmonic distortion + noise | VDD=4.2V, Po=0.1W,RL=8Ω+33μH, f=1kHz, CLASS D Receiver | | | 0.03 | | % |
| PSRR | CLASS D Receiver Power supply rejection ratio | $V_{DD}$=4.2V, Vp-p_sin=200 mV | 217Hz | | -82 | | dB |
| | | | 1kHz | | -80 | | dB |
| Po | CLASS D Receiver Output Power | THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=7.5~9dB | | | 0.5 | | W |
| | | THD+N=1%, RL=8Ω+33μH, VDD=4.2V, GAIN=10.5dB | | | 0.85 | | W |
| **Battery Tracking AGC** | | | | | | | |
| $V_{BSGD}$ | Battery protection threshold voltage | | | | 3.4 (Note4) | | V |
| $V_{HYS}$ | Battery protection Hysteresis voltage | | | | 100 | | mV |
| **Triple-Level Triple-Rate AGC** | | | | | | | |
| $T_{AT1}$ | AGC1 Attack Time | | | | 0.08 (Note4) | | ms/dB |
| $T_{AT2}$ | AGC2 Attack Time | | | | 0.64 (Note4) | | ms/dB |
| $T_{AT3}$ | AGC3 Attack Time | | | | 41 (Note4) | | ms/dB |
| $T_{RLT}$ | Release time | | | | 21 (Note4) | | ms/dB |
| $A_{MAX}$ | The maximum attenuation gain | $V_{DD}$=2.8V to 5.5V | | | -13.5 | | dB |

***Note 4***：*Registers are adjustable; Refer to the list of registers.*

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# MEASUREMENT SETUP

AW87519 features switching digital output, as shown in Figure 6. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

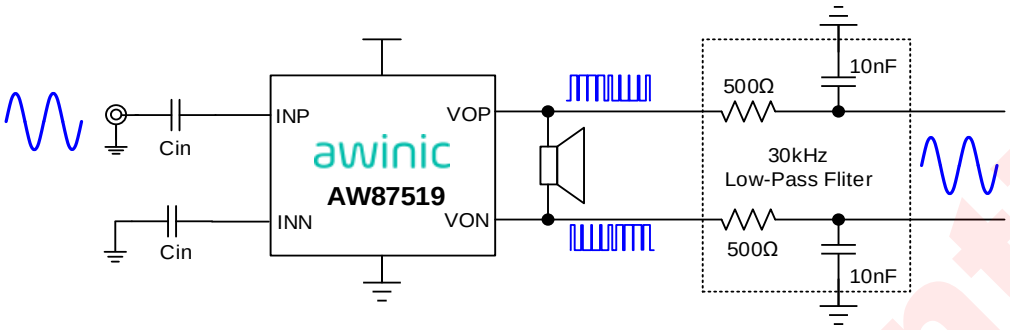


**Figure 6 AW87519 Test Setup**

Low pass filter uses resistance and capacitor values listed in Table 1.

| $R_{filter}$ | $C_{filter}$ | Low-pass cutoff frequency |
|---|---|---|
| 500Ω | 10nF | 32kHz |
| 1kΩ | 4.7nF | 34kHz |

**Table 1 AW87519 Recommended Values for Low Pass Filter**

### Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal , as shown in Figure 7：

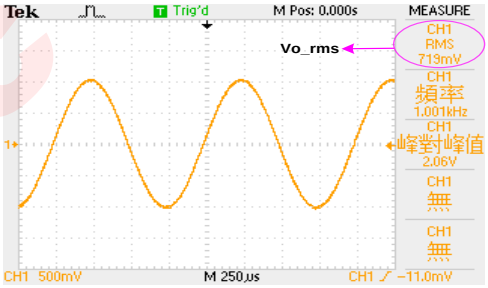


**Figure 7 Output RMS Value**

The power calculation of Speaker is as follows：

$$P_L = \frac{(V_{O_rms})^2}{R_L}$$ $R_L$: load impedance of the speaker

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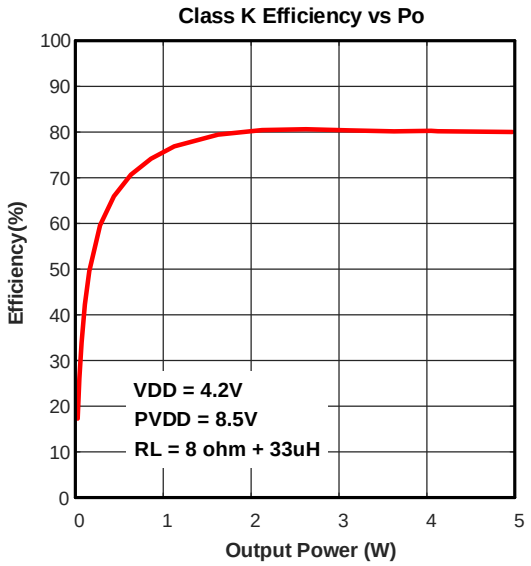
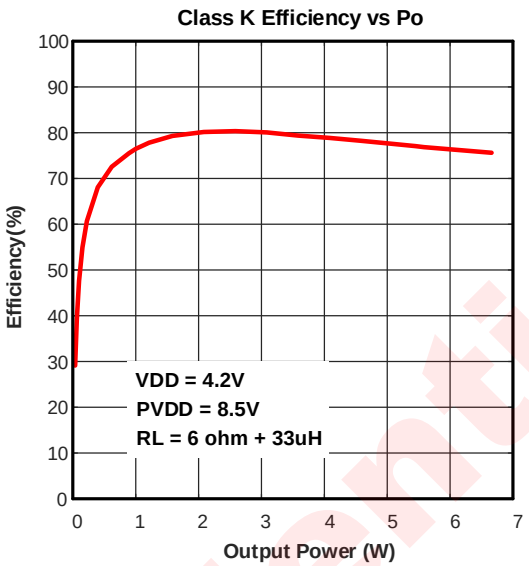
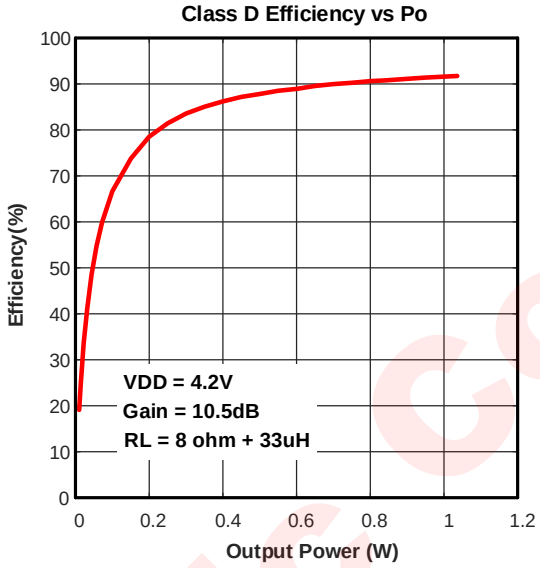
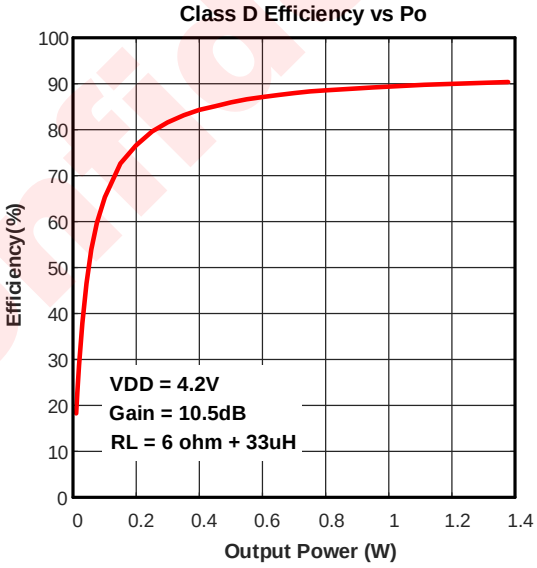
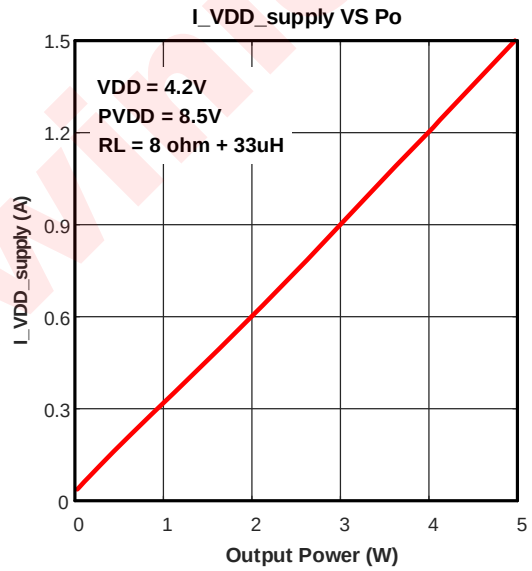
# TYPICAL CHARACTERISTICS

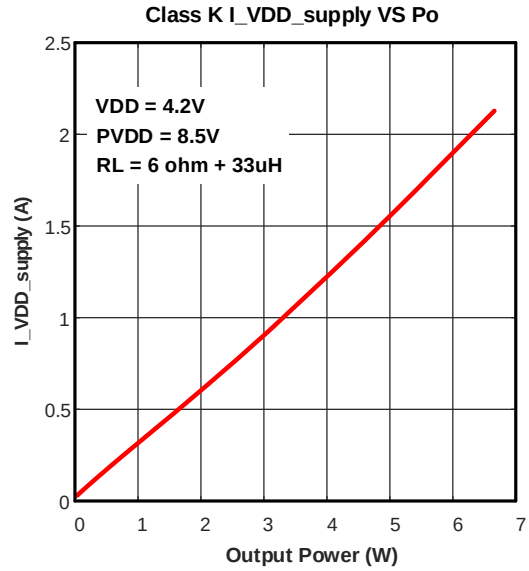
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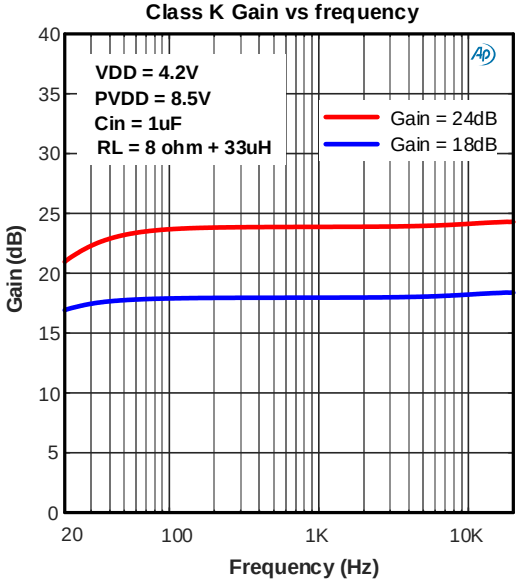
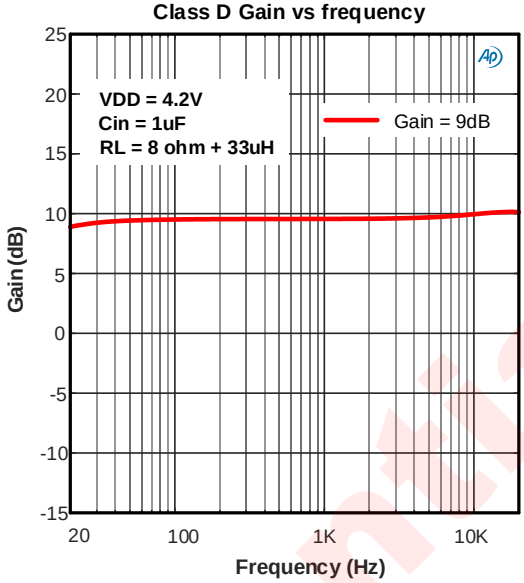
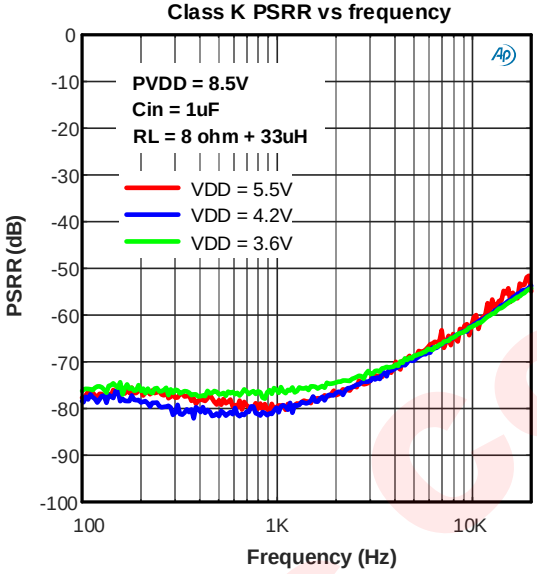
Class K Gain vs frequency



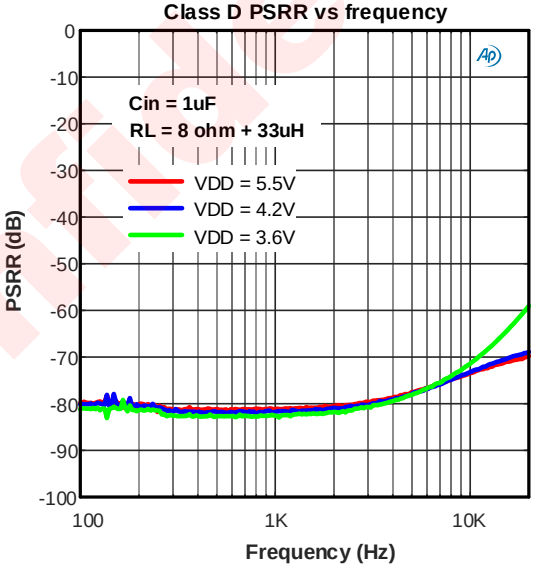

Class D Gain vs frequency



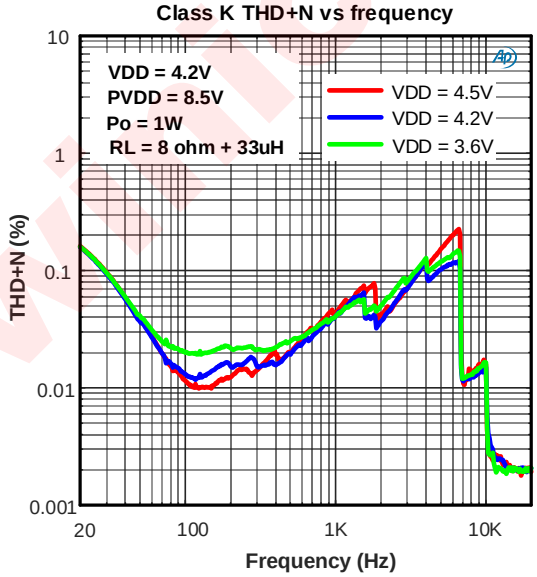

Class K PSRR vs frequency



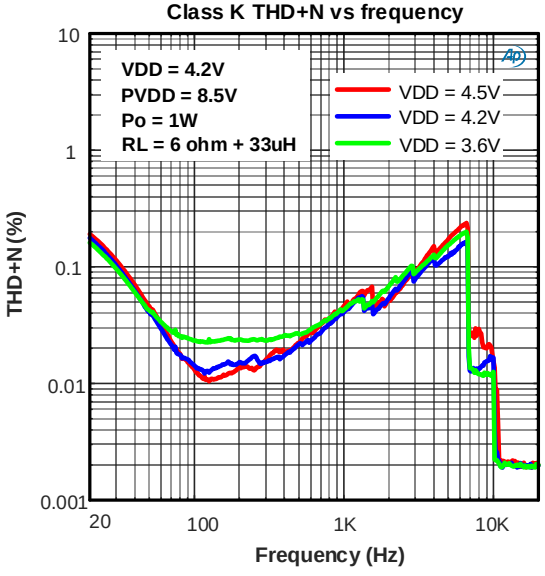

Class D PSRR vs frequency




Class K THD+N vs frequency




Class K THD+N vs frequency

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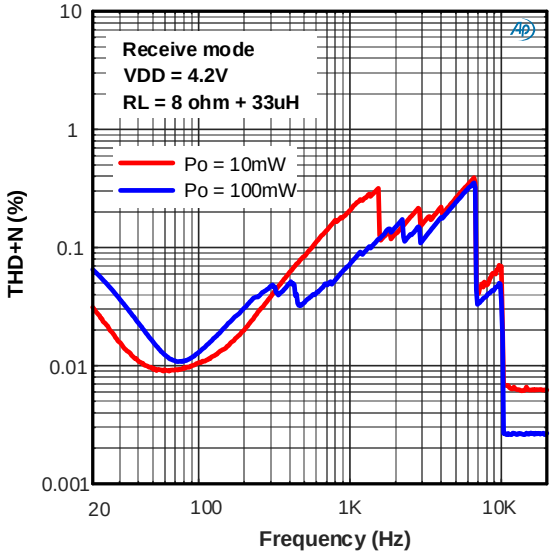
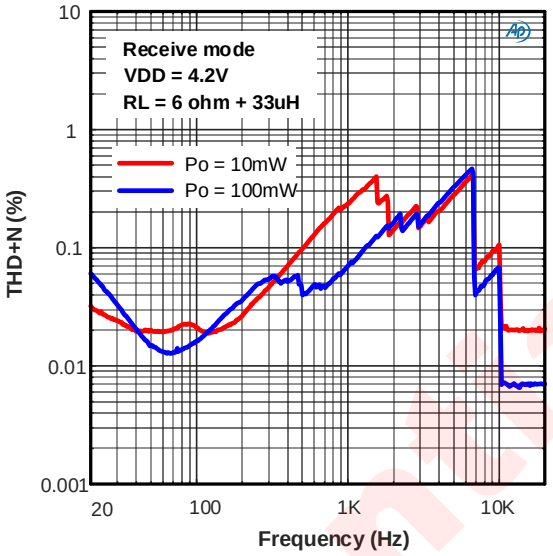
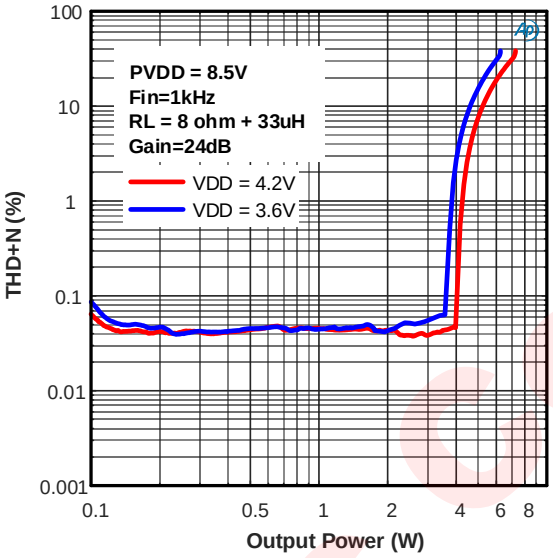
Class D THD+N vs frequency



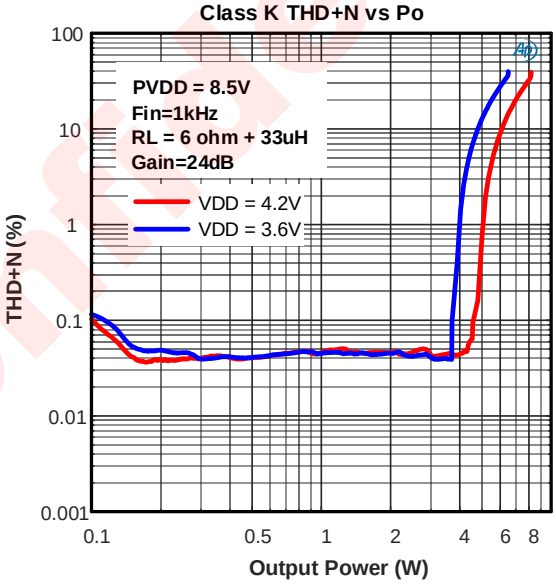

Class D THD+N vs frequency



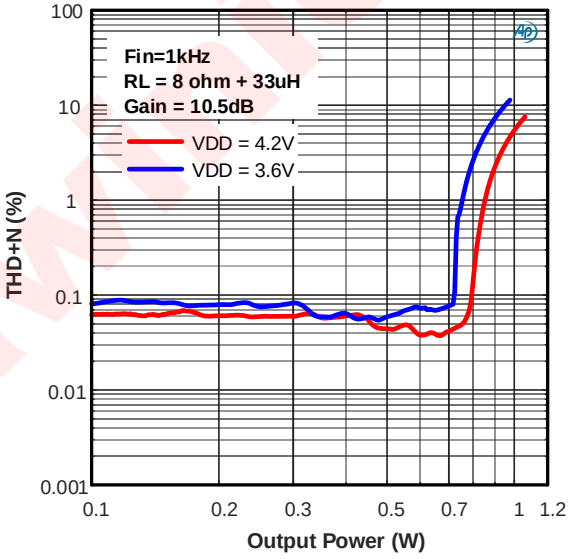

Class K THD+N vs Po



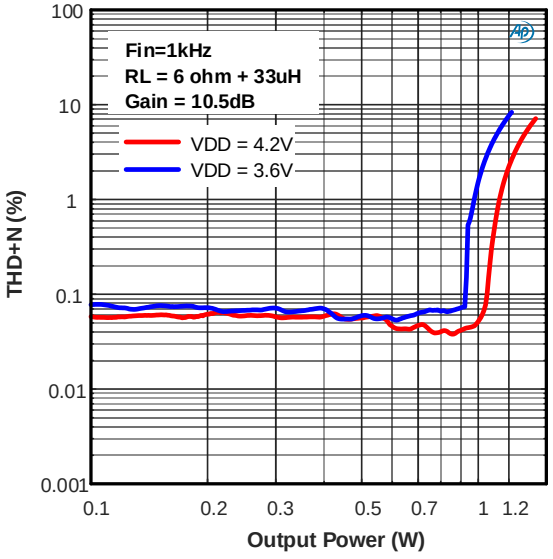

Class K THD+N vs Po




Class D THD+N vs Po




Class D THD+N vs Po

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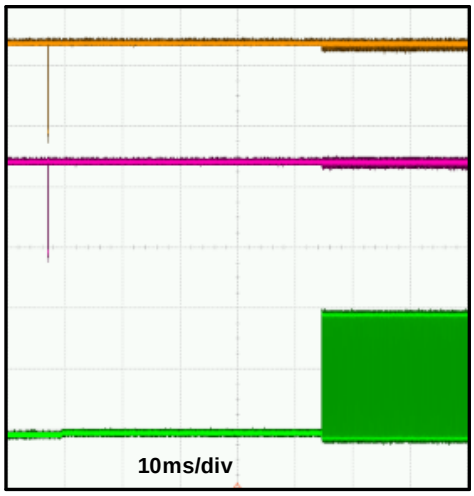
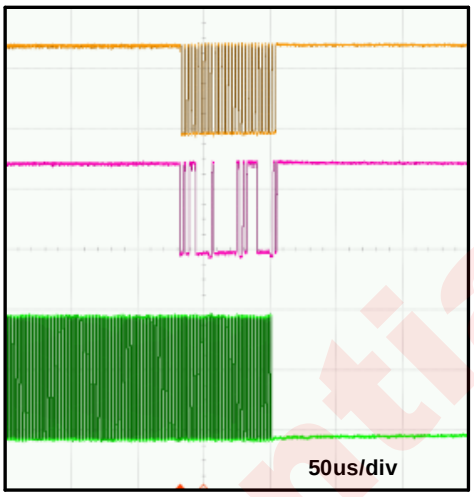
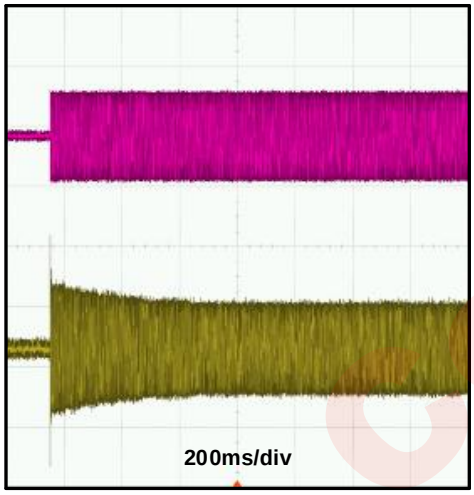
Start-up sequence



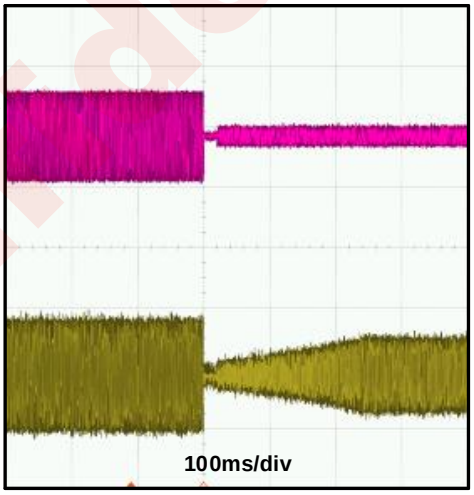

Shutdown sequence



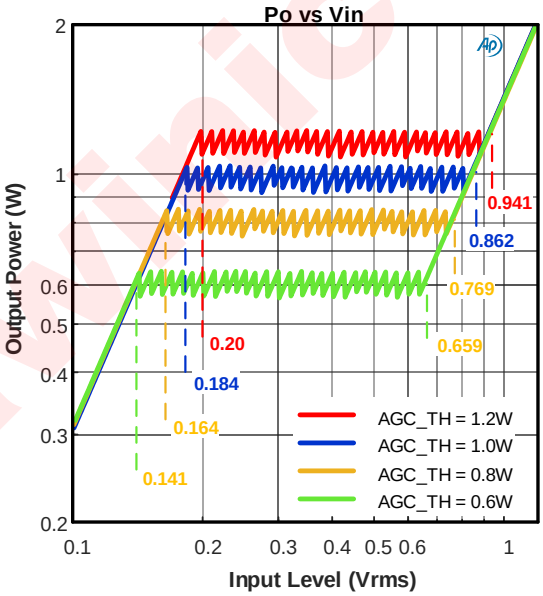

Triple-Level Triple Rate AGC Attack Timing




Triple-Level Triple Rate AGC Release Timing




Po vs Vin

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# WORKING PRINCIPLE

AW87519 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality. It is a new high efficiency, high PSRR，low noise, constant large volume, 3rd generation Smart K audio amplifier. AW87519 integrates AWINIC's proprietary Triple-Level Triple-Rate AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87519 integrates high voltage synchronous Boost with efficiency up to 88% as the class D power stage supply, significantly improving the dynamic range of music. AW87519 noise floor is as low as to 43μV at speaker mode, with 103dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.04% and unique Triple-Level Triple-Rate AGC technology bring high quality music enjoyment.

AW87519 supports speaker and receiver 2-in-1 application. In the receiver mode, its ultra-low noise is 18μV. Class D receiver also has high PSRR performance to completely suppress TDD-noise.

AW87519 controls internal registers through the I2C interface. Register parameters include boost output voltage, boost maximum input peak current, PA gain, Triple-Level Triple-Rate AGC parameters, etc.

AW87519 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87519 features small FCQFN 2.0mmX3.0mmX0.55mm-20L package.

## CONSTANT OUTPUT POWER

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually. So, it is hard to provide high quality music within the battery voltage range. AW87519 uses unique Triple-Level Triple-Rate technology, within lithium battery voltage range (3.3V~4.35V), to guarantee that output power is constant, and the output power will not drop along with the decrease of lithium battery voltage. In the process of using the phone, even if the battery voltage drops, AW87519 can still provide high quality large volume music enjoyment. The output power of AW87519 can be configured from 0.5W to 2W via $I^2C$, matching general speakers. Unique Triple-Level Triple-Rate AGC technology can bring high-quality music enjoyment.

### Triple-Level Triple-Rate AGC technology

AWINIC proprietary Triple-Level Triple-Rate AGC technology is designed for the protection of the high voltage power amplifier, which is divided into AGC1, AGC2 and AGC3 power levels, to obtain a large volume while maintaining excellent sound quality.

In practical applications, speaker can continuously work long hours at rated power, and also can work short-term at high power. For example, in the standard reliability of the loudspeaker experiment, the powder of peak power reached around four times of the rated power. For achieving larger volume and better sound quality, speakers need to work at high power for short periods of time, in order to improve the performance of the speaker. AW87519 Triple-Level Triple-Rate AGC technology can fit the speaker better and perform better overall performance. AGC1 prevents output signal clipping by detecting output voltage in a very short time after clipping, which can effectively restrain the noise clipping; AGC2 can improve the dynamic range of the music in a relatively short period of time; AGC3 can make the speaker work under rated power, which can effectively improve the volume and protect the speaker. Triple-Level Triple-Rate AGC can obtain more excellent overall performance.

Triple-Level Triple-Rate AGC detects the peak output voltage of the power amplifier, when the output peak voltage is higher than the compression threshold voltage, the amplifier gain decreases in 0.5dB step. When the output peak voltage is lower than the release threshold voltage, the amplifier gain is recovery to the initial gain in 0.5dB step. The detailed process can be described as follows:

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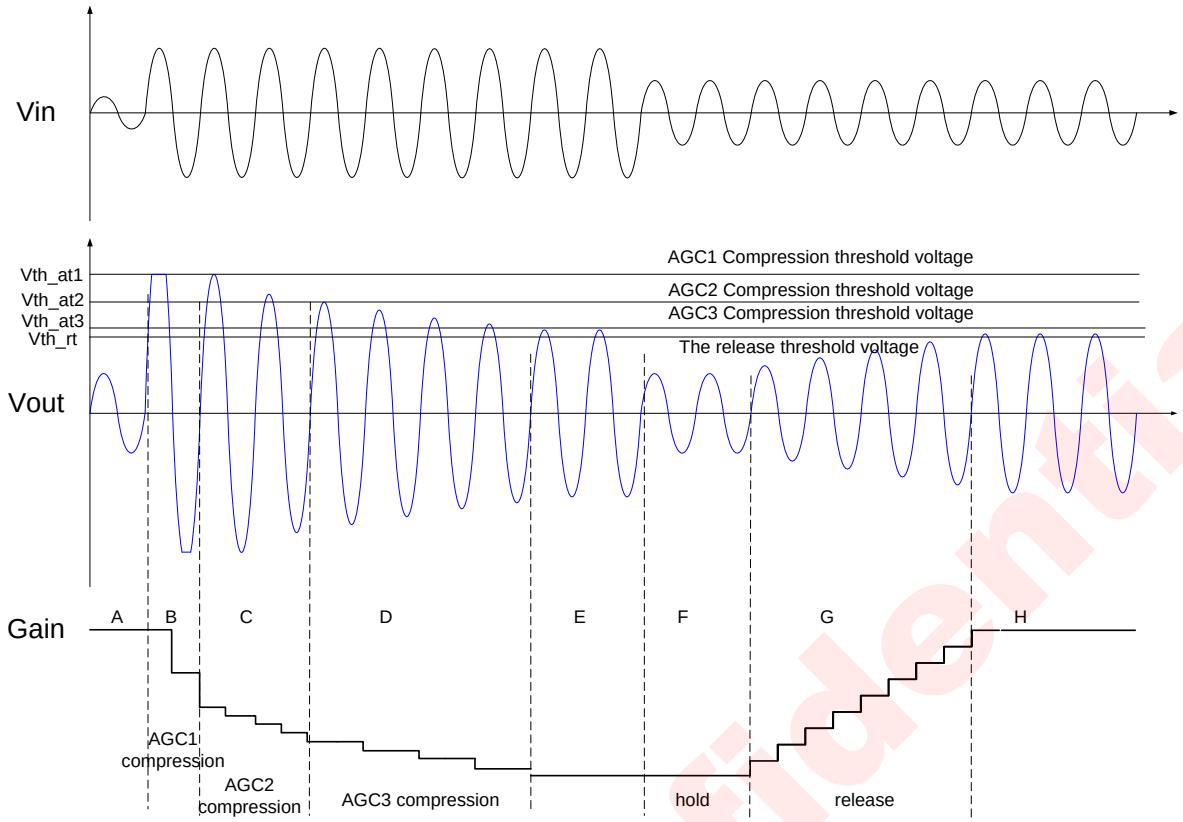


**Figure 8 Triple-Level Triple-Rate AGC Operation Principle**

A: Small input signal, the output voltage is lower than threshold voltage Vth of AGC, AGC don't work.

B: Input voltage becomes large. It leads to the output voltage clipping, AGC1 starts fast compression, the attack time is set through the I²C register 0x0Ah [2:1], when the output voltage is higher than Vth_at1, and gain register began to decrease. Gain decreases when the output signal passes through the zero. It eliminates the clipping noise as soon as possible.

C: When the output voltage is not clipping and higher than threshold voltage Vth_at2, AGC2 starts work, the attack time is set through the I²C register 0x09h [4:2], gain register begins to decrease at a certain rate. Gain register began to decrease. Gain decreases when the output signal passes through the zero. The output voltage gradually decreases to below the AGC2 attack threshold voltage Vth_at2, which can protect the speaker and enhance the sound.

D: When the output voltage is lower than the AGC2 attack threshold voltage Vth_at2 and higher than the AGC3 attack threshold voltage Vth_at3, AGC3 starts work, the attack time is set through the I²C register 0x07h [4:2], and gain register began to decrease at a certain rate. Gain decreases when the output signal passes through the zero, so the output voltage gradually decreases to below of the AGC3 attack threshold voltage Vth_at3, matching the speaker to achieve greater volume and better sound quality.

E: Triple-Level Triple-Rate AGC attack time ends, Amplifier output power is close to the speaker rated power.

F: Input voltage decreases, the output voltage becomes lower than the release threshold voltage Vth_rt, at this point, gain remains the same in the maintain time (10ms~20ms).

G: Gain increases when the time of output voltage lower than the release threshold voltage Vth_rt is longer than the holding time. The release time can be set through I²C register 0x07h [7:5].

H: Stop release when the output signal is larger than the release threshold or the gain is equal to the initial value. The output voltage remains constant.

Triple-Level Triple-Rate AGC can switch independently according to different application requirements. Such as close AGC1 and AGC2, retain only AGC3, this is the single-AGC mode, similar to AW8736 (AGC3 attack time is set to 1.28ms/dB; release time is set to 41ms/dB); Close AGC2, open AGC1 and AGC3, this is

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Multi_level AGC. It can be set similar to AW8738 (AGC1 attack time is set to 80us/dB; AGC3 attack time is set to 0.64ms/dB; release time is set to 10.24ms/dB).

## Zero-Crossing Adjustment Technology

Traditional AGC doesn't contain zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click.

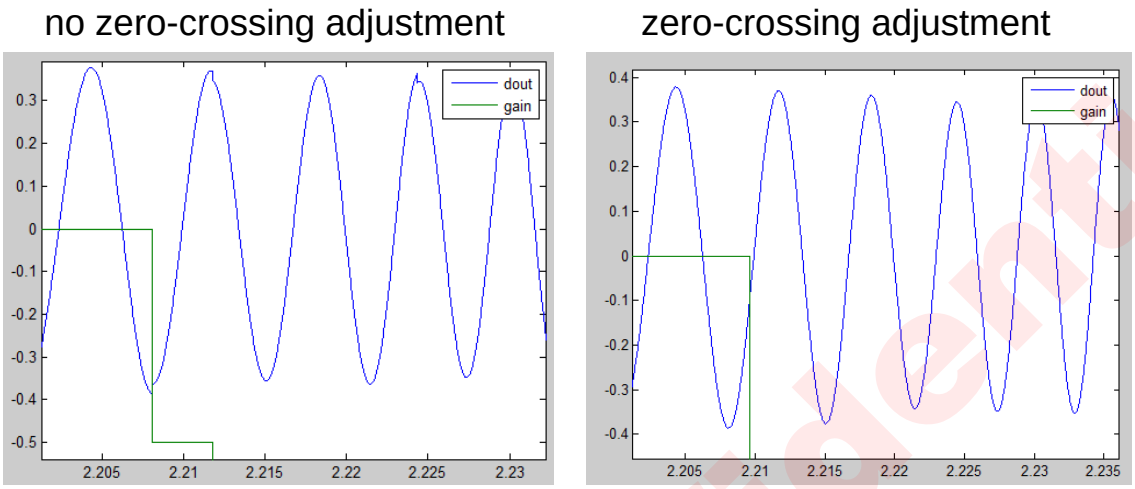


**Figure 9 Zero-adjust Comparison**

As shown above, when there is no zero-adjustment technology, it can be seen the obvious step change at the peak of large signal, the steps sound slightly perceived in special audio. Gain changes at zero. The steps disappear by using zero-crossing detection technology. Using zero detection technology can make the music pure and natural.

## Low-voltage protection AGC technology

Mobile phone battery voltage will decrease in use, but the current will increase. When the battery voltage is low, high current maybe cause the battery protection or mobile phone automatically shut down. Awinic proprietary low voltage protection AGC technology can solve the problems, to prevent high current when the battery voltage is too low.

AW87519 is built-in low voltage protection AGC technology to real-time detection the battery voltage. Gain decreases rapidly when the battery voltage is below the safety threshold, so as to decrease the output voltage and the power supply current, which effectively prevents high current.

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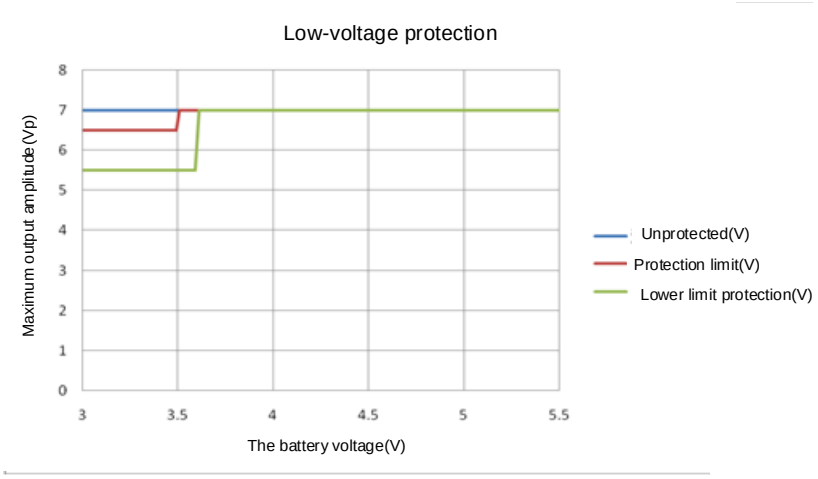


**Figure 10 Low voltage protection**

The protection safety threshold voltage is set to 3.3V~3.6V through the I²C register 0x02h [4:3]. The maximum protection output voltage is set to 5Vp ~ 6.5Vp through I²C register 0x02h [1:0].
Only when the register 0x02h [2] is set to 1, low voltage protection AGC technology is enabled.

## Synchronous Boost technology

AW87519 integrated peak current mode synchronous PWM Boost as Class D power stage supply, significantly increase the output voltage dynamic range. Reduces the size of external components and saves PCB space by using 1.6MHz switching frequency. Boost output voltage can be set through the I²C register 0x03h [4:0]; Boost current limit can be set through register 0x04h [4:2].
AW87519 synchronous Boost with soft-start function to prevent overshoot current at powering-on; integrated the output protection circuit and self-recovery function; integrated Anti-Ring circuit to reduce EMI in DCM mode; built-in substrate switching shutdown circuit, effectively preventing the input and output leakage current anti-irrigation.

## Speaker & Receiver 2-in-1 application

AW87519 built-in speaker and receiver 2-in-1 application mode, through the register settings, class D-type 2-in-1 receiver mode gain can be adjusted through the I²C register 0x05, adjustable range of 7.5~10.5dB, the application is very flexible. The 2-in-1 receiver mode uses the signal path of the speaker, with ultra-low distortion and strong drive capability, and eliminates the need for additional peripheral components, saving system cost and PCB layout space.
In the typical application case of Figure 5, the input capacitance Cin = 68nF, the gain is 24dB in the speaker application mode, the input high-pass cutoff frequency is 260Hz; In 7.5dB gain class D-type 2-in-1 receiver application mode, the output noise is 18μV, the input high-pass cut-off frequency is 78Hz, which is very suitable for high-definition voice applications. AW87519 can achieve speaker and receiver's 2-in-1 application without changing any hardware in the case.

## RNS(RF TDD Noise Suppression)

### *TDD Noise Causes*

GSM cell phones use TDMA (Time Division Multiple Access) slot sharing technology. The time is divided into periodic frames in TDMA, and each frame is subdivided into a plurality of time slots. In order to transmit signals to the base station, the signals sent from the base stations to the plurality of mobile terminals are arranged in a predetermined time slot in the transmission. In this case, each TDMA frame contains 8 time slots, the entire frame is about 4.615ms long, and each slot time is 0.577ms.
With GSM handset, the RF power amplifier will transmit once every 4.615ms (217Hz), and the signal will produce intermittent Burst current and strong electromagnetic radiation. Intermittent Burst current will form a

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power fluctuation of 217 Hz; High frequency (900MHz and 1800MHz) RF signals form a 217Hz RF envelope signal. 217Hz power fluctuations will be conducted through the conduction to the audio signal path, 217Hz RF envelope signal will be coupled through the radiation into the audio signal path, if the protection is not good, it will produce an audible TDD Noise, which includes the 217Hz noise And a harmonic noise signal of 217 Hz.

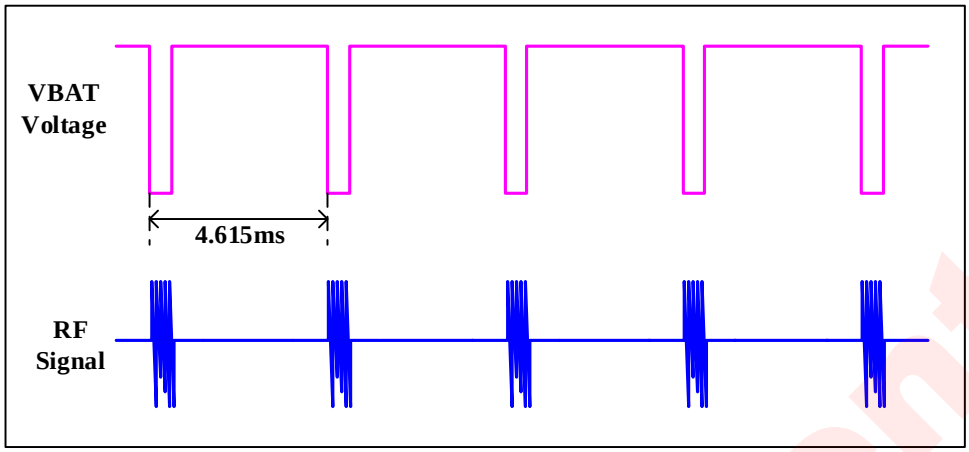


**Figure 11 Schematic Diagram of Power Supply Voltage and RF Signal during GSM RF Operation**

RNS fully inhibit the conduction and radiation interference by the AWINIC unique circuit architecture. Effectively improve the ability to suppress TDD Noise.

***Conduction noise suppression***

When the RF power amplifier is operating, it will draw the current from the battery by 217Hz frequency, Power supply will be introduced to 217Hz power ripple since the battery has a certain internal resistance, it will be coupled to the speaker through the audio power amplifier. The ability to suppress power fluctuations depends on the PSRR of the audio power amplifier.

$$PSRR = 20\log(\frac{vout_{ac}}{vdd_{ac}})$$

Due to the input and output of the fully differential amplifier is perfectly symmetrical, theoretically, the effect of the power supply fluctuation on the two outputs is exactly the same, and the differential output is completely unaffected by the power supply fluctuation. In practice, due to process bias and other factors, the amplifier will have a certain mismatch, PSRR is generally better than -60dB, it shows the output relative to the power fluctuations can be reduced by 1000 times, such as 500mVp power fluctuations, the differential output of 0.5 MV, which basically can meet the application requirements.

But in practical applications, the power amplifier may encounter conduction of TDD Noise problem even if its PSRR is -60dB or -80dB, why is this? Because we also need to consider the impact of peripheral power mismatches of audio power amplifiers

For conventional audio power amplifiers, when the input resistor Rin and the input capacitor Cin mismatch, will greatly affect the audio power amplifier PSRR indicators, in the case of 24 times the gain, PSRR will be weakened to -46dB or so if the input resistance and Capacitor with 1% mismatch. PSRR will be weakened to -28dB or so if the input resistance and input capacitance mismatch with 10% mismatch, when the power fluctuations, it is easy to produce audible TDD Noise.

In order to enhance the audio power amplifier PSRR in the input resistance and input capacitance mismatch case, AW87519 features a unique conduction noise suppression circuit, making the power amplifier to maintain a high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.


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***Radiation noise suppression***

Input traces, output traces, horn loops, and even power and ground loops are likely to be subject to RF radiation interference in the audio signal module, longer input traces and output traces similar to the antenna, especially vulnerable RF radiation effects.

The reasonable PCB layout can reduce the influence of RF radiation in the design, such as shorten the line length of input and output as much as possible; audio devices should be shielded and far away from the RF antenna, maintain the integrity of the device to audio signal pathway; to increase the small bypass capacitor RF signals in the sensitive nodes. However, in practical applications, PCB layout is difficult to fully consider the influence of RF radiation on the audio signal path, and some RF energy will still be coupled to the audio signal path to form audible TDD Noise. Therefore, AW87519 features a unique RF radiation suppression circuit, a shielding layer inside the chip, effectively prevent high frequency energy into RF chip, to ensure that the drive single of the amplifier provided to the speaker will not be affected by the antenna RF radiation, thus avoiding the antenna RF Radiation caused by TDD Noise.

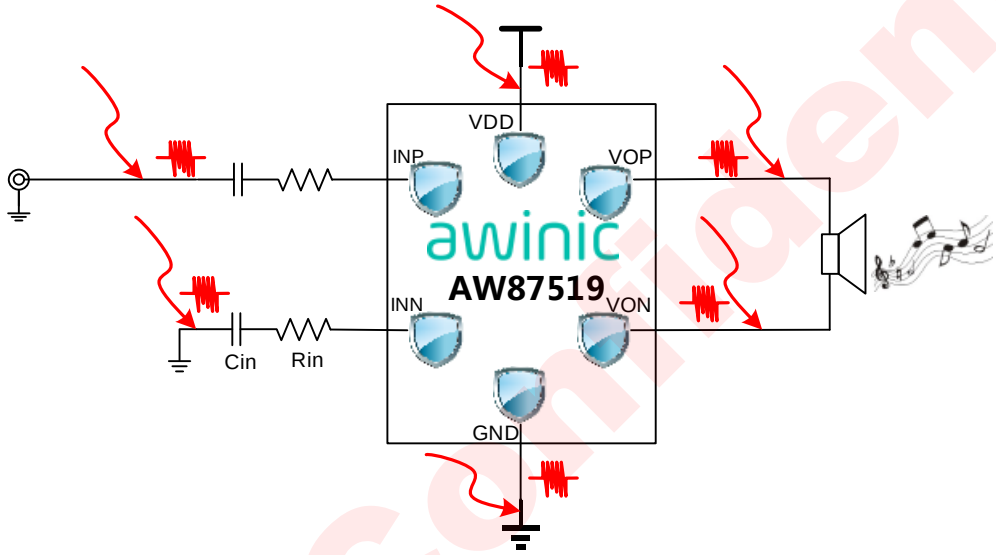


**Figure 12 RF Radiation Coupling Graph**

## Class D amplifier without filter

When the traditional class D amplifier is in idle state of no input signal, the output will have the inverse square wave, it will directly above the load of the speaker, will form a large current power switch on the speaker, therefore we need to increase the LC filter to restore the analog audio signal at the amplifier output. The LC filter increase the cost and PCB layout area, while increase the power consumption, reduce the performance of THD+N.

The AW87519 features a Class D amplifier without a filter, eliminating the need for an output LC filter. In the idle state of no input signal, the two outputs (VOP, VON) of the amplifier are in-phase square waves and not generate idle switching currents on the speaker load. When the input signal is added to the input terminal, the duty ratio of the output is changed. The duty cycle of the VOP becomes larger and the duty cycle of the VON becomes smaller, and the difference value of the output forms the differential amplified signal on the speaker.

## EEE

The AW87519 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth, fully meet FCC CLASS B specification requirements.


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## Pop-Click Suppression

The AW87519 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

## Thermal AGC/ over temperature protection

The AW87519 features the thermal AGC patented technology, can according to the chip temperature, automatically adjust the gain of the system, reduce the power consumption of the chip, to prevent damage in case of excessive temperature.

The AW87519 has an automatic temperature detection mechanism, when the chip temperature exceeds the preset threshold of thermal AGC temperature (150°C), the chip will start the automatic gain control circuit to decrease the gain of the system, thereby reducing the energy consumption of the chip, thus slow or stop chip temperature continues to rise. When the chip temperature is restored to normal operating range (below 130°C), the automatic gain control circuit will restore the system gain to the original state. When the chip operates in a fault condition, the chip temperature is too high, up to a preset temperature protection temperature threshold (160°C), the system starts overheating protection, the chip will be turned off, restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C).

## Automatic recovery of overcurrent protection

AW87519 with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, AW87519 internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting.

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## Device Address

The I²C device address (7-bit) is decided by the connection of the AD pin. The connection of AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 10110A1A0. The permitted I²C addresses are 0x58(7bit) through 0x5B(7-bit). The address information is as following table.

| AD pin | A1 | A0 | I2C address (7-bit) |
|---|---|---|---|
| Connects to GND | 0 | 0 | 0x58 |
| Connects to SCL | 0 | 1 | 0x59 |
| Connects to SDA | 1 | 0 | 0x5A |
| Connects to VDD | 1 | 1 | 0x5B |

**Table 2 AW87519 Address selection**

## I²C Timing feature

| Parameter | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| No. | Sym | Name | | | | |
| 1 | $f_{SCL}$ | SCL Clock frequency | | | 400 | kHz |
| 2 | $t_{LOW}$ | SCL Low level Duration | 1.3 | | | μs |
| 3 | $t_{HIGH}$ | SCL High level Duration | 0.6 | | | μs |
| 4 | $t_{RISE}$ | SCL, SDA rise time | | | 0.3 | μs |
| 5 | $t_{FALL}$ | SCL, SDA fall time | | | 0.3 | μs |
| 6 | $t_{SU:STA}$ | Setup time SCL to START state | 0.6 | | | μs |
| 7 | $t_{HD:STA}$ | (Repeat-start) Start condition hold time | 0.6 | | | μs |
| 8 | $t_{SU:STO}$ | Stop condition setup time | 0.6 | | | μs |
| 9 | $t_{BUF}$ | the Bus idle time START state to STOP state | 1.3 | | | μs |
| 10 | $t_{SU:DAT}$ | SDA setup time | 0.1 | | | μs |
| 11 | $t_{HD:DAT}$ | SDA hold time | 10 | | | ns |

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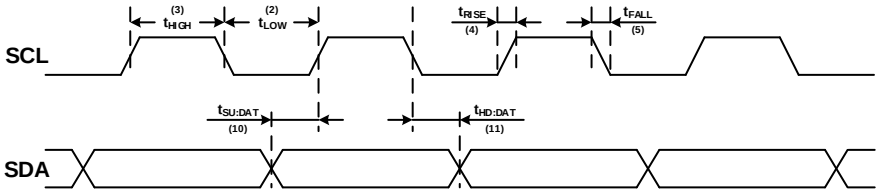


**Figure 13 SCL and SDA timing relationships in the data transmission process**

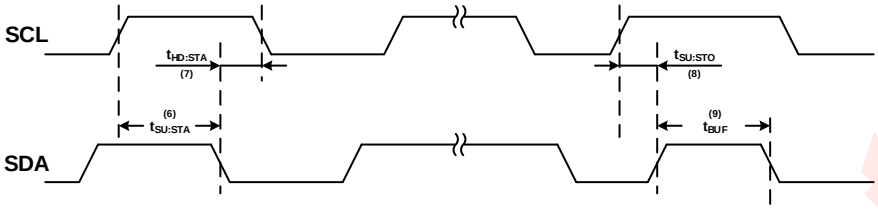


**Figure 14 the Timing Relationship between START and STOP State**

## General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 15.

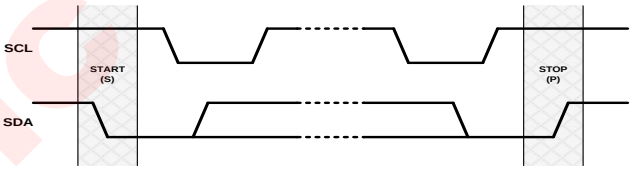


**Figure 15 START and STOP State Generation Process**

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 16. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A ), as shown in Figure 17. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

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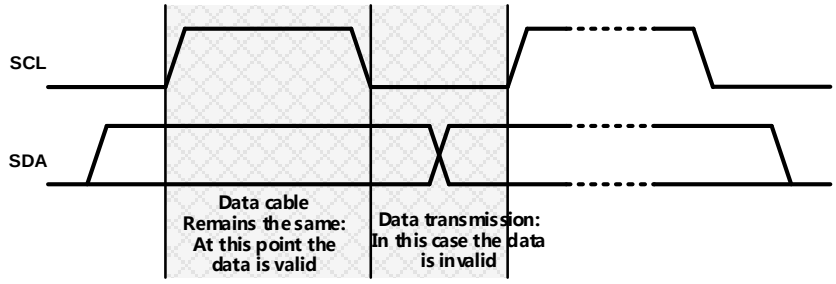


**Figure 16 The Data Transfer Rules on the I²C Bus**

The whole process of actual data transmission is shown in Figure 17. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

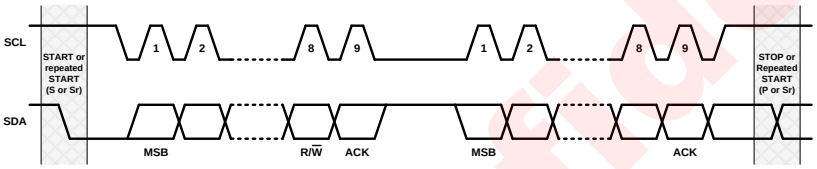


**Figure 17 Data Transmission on the I²C Bus**

## I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

## Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87519 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 18:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87519 register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87519, within AW87519 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.


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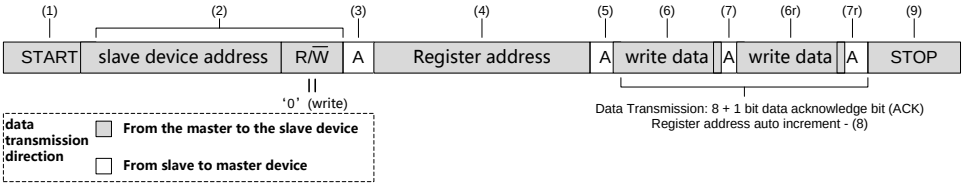


**Figure 18 Writing Process (Data Transmission Direction Remains the Same)**

## Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87519 as the slave device, the transmission process carried out by following steps listed in Figure 19:

Master device asserts a start condition;

Master device transmits the 7 bits address of AW87519, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device sends the 8bit address that the AW87519 register needs to read the data;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START.

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again.

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not.

The master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully.

AW87519 automatically increment register address once after the slave sent each acknowledge bit (ACK).

The master device generates the STOP state to end the data transmission.

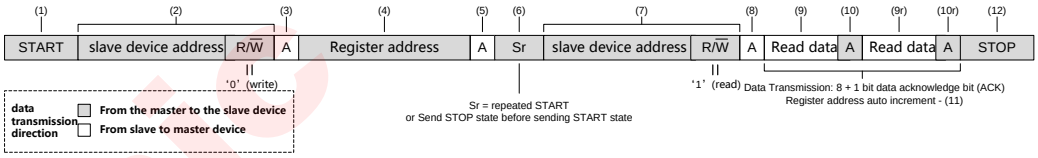


**Figure 19 Reading Process (Data Transmission Direction Remains the Same)**

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## Register List

| name | address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| Chip ID | 0x00 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| SYSCTRL | 0x01 | EN_SW | EN_CP | EN_BOOST | EN_PA | RCV_MODE (1) | 0 | 0 | 0 |
| BATSAFE | 0x02 | 0 | 0 | 0 | BAT_SFGD_VTH(2) [1] | BAT_SFGD_VTH(2) [0] | EN_BAT_SFGD | BAT_SFGD_LEVEL(3) [1] | BAT_SFGD_LEVEL(3) [0] |
| BSTVOUT | 0x03 | 1 | 1 | FORCE_BOOST | BST_VOUT(4) [4] | BST_VOUT(4) [3] | BST_VOUT(4) [2] | BST_VOUT(4) [1] | BST_VOUT(4) [0] |
| BSTCP | 0x04 | 0 | 0 | 0 | BST_IPEAK[2] | BST_IPEAK[1] | BST_IPEAK[0] | 0 | 1 |
| PAGAIN | 0x05 | 0 | 0 | 0 | PA_GAIN[4] | PA_GAIN[3] | PA_GAIN[2] | PA_GAIN[1] | PA_GAIN[0] |
| AGC3_Po | 0x06 | 0 | 1 | 0 | PD_AGC3 | AGC3_Po[3] | AGC3_Po[2] | AGC3_Po[1] | AGC3_Po[0] |
| AGC3 | 0x07 | AGC3_RT[2] | AGC3_RT[1] | AGC3_RT[0] | AGC3_AT[2] | AGC3_AT[1] | AGC3_AT[0] | 1 | 0 |
| AGC2_Po | 0x08 | 0 | 0 | 0 | 0 | AGC2_Po[3] | AGC2_Po[2] | AGC2_Po[1] | AGC2_Po[0] |
| AGC2 | 0x09 | 0 | 0 | 0 | AGC2_AT[2] | AGC2_AT[1] | AGC2_AT[0] | 0 | 0 |
| AGC1 | 0x0A | 0 | 1 | 0 | 0 | 1 | AGC1_AT[1] | AGC1_AT[0] | PD_AGC1 |

(1) RCV_MODE: enable 2-in-1 receiver application
(2) BAT_SFGD_VTH: Battery voltage when enter into battery safe_guard mode
(3) BAT_SFGD_LEVEL: Maxim output level when enter into battery safe_guard mode
(4) BST_VOUT: Boost output voltage

| register | 0x00 | 0x01 | 0x02 | 0x03 | 0x04 | 0x05 | 0x06 | 0x07 | 0x08 | 0x09 | 0x0A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Default | 0x59 | 0x70 | 0x09 | 0xC8 | 0x11 | 0x05 (RCV_MODE=1) | 0x53 | 0x4E | 0x0B | 0x08 | 0x4B |
| | | | | 0xE8 | | 0x10 (RCV_MODE=0) | 0x43 | | 0x03 | | 0x4A |

**Table 3 AW87519 Register Initial Value**

Any register address which is more than 0x0A and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87519's I²C address is 10110A2A1, as shown in Table 4, in order to avoid conflict with other I²C devices address, you can connect AD pin to GND，SCL，SDA，VDD to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | A2 | A1 | R/W |

**Table 4 AW87519 Address Byte**

***CHIP ID* Register *(address: 0x00)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7:0 | IDCODE | R | 0x59 | Chip ID will be returned after reading.<br>All configuration registers will be reset to default values after 0xAA is written. |

***SYSTEM CONTROL (SYSCTRL)* Register *(address: 0x01)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | EN_SW | R/W | 0 | Chip Software Enable |
| | | | | 0: Chip Software Disable: |


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| | | | | |
|---|---|---|---|---|
| | | | | Shutdown the whole chip except PORN.<br>1: Chip Software Enable |
| 6 | EN_CP | R/W | 1 | Chargepump Enable:<br>0: Disable Chargepump, PVDD=VBAT<br>1: Enable Chargepump |
| 5 | EN_BOOST | R/W | 1 | BOOST enable<br>0: Disable BOOST，BOOST power down<br>1: Enable BOOST |
| 4 | EN_PA | R/W | 1 | PA output Enable<br>0: Disable PA<br>1: Enable PA |
| 3 | RCV_MODE | R/W | 0 | CLASS D receiver function enable<br>0：Receiver mode disabled<br>1：Enable Receiver mode |
| 2:0 | -- | -- | 000 | Reserved and Unused |

***BATTERY SAFEGUARD (BATSAFE)*Register *(address: 0x02)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7:5 | -- | -- | 000 | Reserved and Unused |
| 4:3 | BAT_SFGD_VTH | R/W | 01 | Setting Battery Threshold Voltage for Triggering Battery Safeguard Mode:<br>00：threshold voltage is 3.3V<br>01:threshold voltage is 3.4V<br>10:threshold voltage is 3.5V<br>11:threshold voltage is 3.6V |
| 2 | EN_BAT_SFGD | R/W | 0 | Software control battery safeguard，when FORCE_BOOST=0, this bit is set to be 0.<br>0: Software control battery safeguard disable<br>1: Software control battery safeguard enable |
| 1:0 | BAT_SFGD_LEVEL | R/W | 01 | Setting Maximum Output Level when Battery Safeguard Mode Triggered<br>00: 5.0Vp<br>01: 5.5Vp<br>10: 6.0Vp<br>11: 6.5Vp |

***BOOST OUTPUT VOLTAGE (BSTVOUT)* Register *(address: 0x03)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7:6 | -- | -- | 11 | Reserved and Unused |
| 5 | FORCE_BOOST | R/W | 1 | Boost output voltage enable<br>0：direct through mode，PVDD=VBAT<br>1：force boost output voltage |
| 4:0 | BST_VOUT | R/W | 01000 | BOOST output voltage set<br>01001~11111: Unavailable<br>01000: 8.5V<br>00111: 8.25V<br>00110: 8.0V<br>00101: 7.75V<br>00100: 7.5V<br>00011: 7.25V<br>00010: 7.0V<br>00001: 6.75V<br>00000: 6.5V |

***BOOST CONTROL PARAMETER (BSTCP)* Register *(address: 0x04)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|

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| | | | | |
|---|---|---|---|---|
| 7:5 | -- | -- | 000 | Reserved and Unused |
| 4:2 | BST_IPEAK | R/W | 100 | BOOST peak current limit<br>000: 2.5A<br>001: 2.75A<br>010: 3.0A<br>011: 3.25A<br>100: 3.5A<br>101: 3.75A<br>110: 4.0A<br>111: 4.25A |
| 1:0 | -- | -- | 01 | Reserved and Unused |

**GAIN CONTROL (*Gain*) Register *(address: 0x05)***

***For RCV_MODE=1, (Speaker & Receiver 2-in-1Mode):***

| I²C Bit | Name | R/W | Default | Description | |
|---|---|---|---|---|---|
| 7:5 | -- | -- | 000 | Reserved and Unused | |
| 4:0 | Gain | R/W | 00101 | Setting Class D Amplifying Gain | |
| | | | | Gain | |
| | | | | 00000~00100 | Reserved and Unused |
| | | | | 00101: 7.5dB | $R_{ini}$=30kΩ |
| | | | | 00110: 9.0dB | $R_{ini}$=24kΩ |
| | | | | 00111: 10.5dB | $R_{ini}$=28kΩ |

***For RCV_MODE=0,(Speaker Mode):***

| I²C Bit | Name | R/W | Default | Description | |
|---|---|---|---|---|---|
| 7:5 | -- | -- | 000 | Reserved and Unused | |
| 4:0 | Gain | R/W | 10000 | Setting Class D Amplifying Gain | |
| | | | | Gain | |
| | | | | 01000: 12dB | $R_{ini}$=36.5kΩ |
| | | | | 01001: 13.5dB | $R_{ini}$=30kΩ |
| | | | | 01010: 15.0dB | $R_{ini}$=25kΩ |
| | | | | 01011: 16.5dB | $R_{ini}$=21.5kΩ |
| | | | | 01100: 18.0dB | $R_{ini}$=18kΩ |
| | | | | 01101: 19.5dB | $R_{ini}$=15.5kΩ |
| | | | | 01110: 21dB | $R_{ini}$=12.5kΩ |
| | | | | 01111: 22.5dB | $R_{ini}$=11kΩ |
| | | | | 10000: 24dB | $R_{ini}$=9kΩ |
| | | | | 10001: 25.5dB | $R_{ini}$=7.5kΩ |
| | | | | 10010: 27dB | $R_{ini}$=6.5kΩ |
| | | | | 10011~11111: Unavailable | |

***CLASS D AGC3 OUTPUT POWER (AGC3_Po)* Register *(address: 0x06)***

| I²C Bit | Name | R/W | Default | Description | |
|---|---|---|---|---|---|
| 7:5 | -- | -- | 010 | Reserved and Unused | |
| 4 | PD_AGC3 | R/W | 0 | Disable AGC3 | |
| | | | | 0:Enable AGC3 | |
| | | | | 1:Disable AGC3 | |
| 3:0 | AGC3_Po | R/W | 0011 | Setting AGC3 Output Power for Protecting Speaker and stereo Receiver | |
| | | | | 0000: 0.5W@8Ω | 0.667W@6Ω |
| | | | | 0001: 0.6W@8Ω | 0.8W@6Ω |
| | | | | 0010: 0.7W@8Ω | 0.933W@6Ω |
| | | | | 0011: 0.8W@8Ω | 1.067W@6Ω |
| | | | | 0100: 0.9W@8Ω | 1.2W@6Ω |
| | | | | 0101: 1.0W@8Ω | 1.333W@6Ω |
| | | | | 0110: 1.1W@8Ω | 1.467W@6Ω |

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| | | | | | |
|---|---|---|---|---|---|
| | | | | 0111: 1.2W@8Ω | 1.6W@6Ω |
| | | | | 1000: 1.3W@8Ω | 1.733W@6Ω |
| | | | | 1001: 1.4W@8Ω | 1.867W@6Ω |
| | | | | 1010: 1.5W@8Ω | 2.0W@6Ω |
| | | | | 1011: 1.6W@8Ω | 2.133W@6Ω |
| | | | | 1100: 1.7W@8Ω | 2.267W@6Ω |
| | | | | 1101: 1.8W@8Ω | 2.4W@6Ω |
| | | | | 1110: 1.9W@8Ω | 2.533W@6Ω |
| | | | | 1111: 2.0W@8Ω | 2.667W@6Ω |

***CLASS D AGC3 PARAMETER (AGC3)* Register *(address: 0x07)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7:5 | AGC3_RT | R/W | 010 | Setting Release Time of AGC3: |
| | | | | 000: 5.12ms/dB |
| | | | | 001: 10.24ms/dB |
| | | | | 010: 21 ms/dB |
| | | | | 011: 41 ms/dB |
| | | | | 100: 82 ms/dB |
| | | | | 101: 164 ms/dB |
| | | | | 110: 328 ms/dB |
| | | | | 111: Unavailable |
| 4:2 | AGC3_AT | R/W | 011 | Setting Attack Time of AGC3: |
| | | | | 000: 1.28ms/dB |
| | | | | 001: 2.56ms/dB |
| | | | | 010: 10.24ms/dB |
| | | | | 011: 20.48ms/dB |
| | | | | 100: 41ms/dB |
| | | | | 101: 82ms/dB |
| | | | | 110: 164ms/dB |
| | | | | 111: 328ms/dB |
| 1:0 | -- | -- | 10 | Reserved and Unused |

***CLASS D AGC2 OUTPUT POWER(AGC2_Po)* Register *(address: 0x08)***

| I²C Bit | Name | R/W | Default | Description | |
|---|---|---|---|---|---|
| 7:4 | -- | -- | 0000 | Reserved and Unused | |
| 3:0 | AGC2_Po | R/W | 0011 | Setting AGC2 Output Power: | |
| | | | | 0000: 1.0W@8Ω | 1.333W@6Ω |
| | | | | 0001: 1.2W@8Ω | 1.6W@6Ω |
| | | | | 0010: 1.4W@8Ω | 1.867W@6Ω |
| | | | | 0011: 1.6W@8Ω | 2.133W@6Ω |
| | | | | 0100: 1.8W@8Ω | 2.4W@6Ω |
| | | | | 0101: 2.0W@8Ω | 2.667W@6Ω |
| | | | | 0110: 2.2W@8Ω | 2.933W@6Ω |
| | | | | 0111: 2.4W@8Ω | 3.2W@6Ω |
| | | | | 1000: 2.6W@8Ω | 3.467W@6Ω |
| | | | | 1001: 2.8W@8Ω | 3.733W@6Ω |
| | | | | 1010: 3.0W@8Ω | 4W@6Ω |
| | | | | 1011: AGC2 OFF | |
| | | | | 1100~1111: Unavailable | |

***CLASS D AGC2 PARAMETER (AGC2)* Register *(address: 0x09)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7:5 | -- | -- | 000 | |
| 4:2 | AGC2_AT | R/W | 010 | Setting Attack Time of AGC2: |
| | | | | 000: 0.16ms/dB |
| | | | | 001: 0.32ms/ dB |


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| | | | | |
|---|---|---|---|---|
| | | | | 010: 0.64ms/dB |
| | | | | 011: 2.56ms/dB |
| | | | | 100: 10.24ms/dB |
| | | | | 101: 41ms/dB |
| | | | | 110: 82ms/dB |
| | | | | 111: 164ms/dB |
| 1:0 | -- | -- | 00 | Reserved and Unused |

***CLASS D AGC1 PARAMETER (AGC1)* Register *(address: 0x0A)***

| I²C Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7:3 | -- | -- | 01001 | Reserved and Unused |
| 2:1 | AGC1_AT | R/W | 01 | Setting Fastest Level AGC Attack Time:<br>00: 0.04ms/dB<br>01: 0.08ms/dB<br>10: 0.16ms/dB<br>11: 0.32ms/dB |
| 0 | PD_ AGC1 | R/W | 0 | AGC1 control bit<br>0: AGC1 Enable<br>1: AGC1 Disable |

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# APPLICATION INFORMATION

## EXTERNAL COMPONENTS

### *BOOST INDUCTOR SELECTION*

Selecting inductor needs to consider Inductance, size, magnetic shielding, saturation current and temperature current.

a) Inductance

Inductance value is limited by the boost converter's internal loop compensation. In order to ensure phase margin sufficient under all operating conditions, recommended 1μH inductor.

b) Size

For a certain value of inductor, the smaller the size, the greater the parasitic series resistance of the inductor DCR, the higher the loss, corresponds to the lower efficiency.

c) Magnetic shielding

Magnetic shielding can effectively prevent the inductance of the electromagnetic radiation interference. It is much better to choose inductance with magnetic shielding in the application of EMI sensitive environment.

d) Saturation current and temperature rise of current

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, on the one hand, since the magnetic core begins to saturate, inductance value will decline; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. In general, the current value is defined as the saturation current $I_{SAT}$ when the inductance value drops to 70%; the current value is defined as temperature rise current $I_{RMS}$ when inductance temperature rise 40℃.

For particular applications, need to calculate the maximum $I_{L_PEAK}$ and $I_{L_RMS}$, which is a basis of selecting the inductor. When VDD = 4.2V, PVDD=8.5V, $R_L$ = 8Ω，amplifier $R_{DSON}$ = 250mΩ, when THD = 1% (the maximum power without distortion), the output power is calculated as follows:

$$P_{OUT}=\frac{\left(V_{OUT}\times\frac{R_L}{R_L+R_{DSON}}\right)^2}{2\times R_L}=\frac{\left(8.5\times\frac{8}{8+0.25}\right)^2}{2\times 8}=4.3\text{W}$$

In such a large output power, the overall efficiency of the power amplifier is typically 80%, in order to calculate the maximum average current $I_{MAX_AVG_VDD}$ and maximum peak current $I_{MAX_PEAK_VDD}$ drawn from VDD:

$$I_{MAX_AVG_VDD}=\frac{P_{OUT}}{V_{DD}\times\eta}=\frac{4.3}{4.2\times 0.8}\text{A}=1.28\text{A}$$

$$I_{MAX_PEAK_VDD}=2\times I_{MAX_AVG_VDD}=2.56\text{A}$$

If inductor DCR is 50mΩ, the inductor power loss at this time is:

$$P_{DCR,LOSS}=1.5\cdot I_{MAX_AVG_VDD}^2\cdot DCR=1.5\times 1.28^2\times 0.05\text{W}=123\text{mW}$$

Wherein the coefficient 1.5 is the square of the ratio of the sine wave current RMS value and average value (there is no consideration of the impact of the inductor ripple, the actual DCR loss will be even greater). If the loss which is resulting from DCR is less than 1% at maximum efficiency ($P_{OUT}$ = 2.5W, η = 80%), then:

$$I_{AVG_VDD}=\frac{P_{OUT}}{V_{DD}\times\eta}=\frac{2.5}{4.2\times 0.8}=0.74\text{A}$$

$$DCR=\frac{P_{DCR,LOSS}}{1.5\cdot I_{AVG_VDD}^2}\le 0.01\times\frac{P_{OUT}}{1.5\cdot I_{AVG_VDD}^2\cdot\eta}=\frac{0.01\times 2.5}{1.5\times 0.74^2\times 0.8}\Omega=38\text{m}\Omega$$

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According to the working principle of the Boost, we can calculate the size of the inductor current ripple $\Delta_{IL}$:

$$\Delta I_L = \frac{V_{DD} \times (V_{OUT} - V_{DD})}{V_{OUT} \times f \times L} = \frac{4.2 \times (8.5 - 4.2)}{8.5 \times 1.6 \times 10^6 \times 1 \times 10^{-6}} \text{A} = 1.33\text{A}$$

Thus, the maximum peak inductor current $I_{L_PEAK}$ and maximum effective inductor current $I_{L_RMS}$ is:

$$I_{L_PEAK} = I_{MAX_PEAK_VDD} + \frac{\Delta I_L}{2} = 2.56 + \frac{1.33}{2}\text{A} = 3.23\text{A}$$

$$I_{L_RMS} = \sqrt{I_{MAX_PEAK_VDD}^2 + \frac{\Delta I_L^2}{12}} = \sqrt{2.56^2 + \frac{1.33^2}{12}}\text{A} = 2.6\text{A}$$

From the above calculation results:

1) For typical DCR about 38mΩ inductance, the efficiency loss caused by around1.5%;
2) In practice, the maximum output power of the amplifier is likely to reach 4.3W in an instant, so the selected inductor saturation current $I_{SAT}$ requires more than the maximum inductor peak current $I_{L_PEAK}$;
3) In some cases, if the $I_{L_PEAK}$ calculated according to the above method is greater than the set of input inductor current limit value $I_{LIMIT}$, shows the power amplifier is restricted by inductance input current limit, the actual maximum output power is less than the calculated value, the measured value shall prevail, and $I_{SAT}$ need greater than the set current limiting value $I_{LIMIT}$, and cannot be less than 2.56A;
4) Take PVDD = 8.5V for example, under different conditions, the typical method of selecting $I_{SAT}$ in the following table:

| **$V_{DD}$ (V)** | **PVDD (V)** | **$R_L$ (Ω)** | **$I_{LIMIT}$ (A)** | **Efficiency(η) (%)** | **$P_O$ (W)** | **$I_{L_PEAK}$ (A)** | Inductor saturation current ISAT minimum value (A) |
|---|---|---|---|---|---|---|---|
| 4.2 | 8.5 | 8 | 4 | 80 | 4.3 | 3.23 | 4.2 |
| 4.2 | 8.5 | 6 | 4 | 75 | 5.3 | 4 | 4.2 |

5) As the result of the action of AGC，amplifier will not work long hours at maximum power without distortion, the actual average inductor current is far less than the maximum inductor current effective $I_{L_RMS}$, so when selecting the inductor, the inductor temperature rise current is not usually a limiting factor;
6) Inductor Selection example: the inductor package size is 252012, inductance value is 1μH, DCR Typical value is 47mΩ, the typical saturation current $I_{SAT}$ is 4.2A, the typical temperature rise current $I_{RMS}$ is 2.8A, suitable for VDD=3.6V, PVDD=8.5V, speaker impedance $R_L$=8Ω, inductor input current limit $I_{LIMIT}$= 4.2A. If you choose $I_{SAT}$ or $I_{RMS}$ of the inductance is too small, it is possible to cause the chip don't work properly, or the temperature of the inductance is too high.

| Inductance value | size | DCR ( Ω ) | $I_{SAT}$ ( A ) | $I_{RMS}$ ( A ) |
|---|---|---|---|---|
| 1uH | 2.5×2.0×1.2mm | 0.047 | 4.2 | 2.8 |

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## Capacitor Selection

### *BOOST CAPACITOR SELECTION*

The output capacitor of chargepump is usually within the range 0.1μF~47μF, It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO3), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

***a) temperature stability***

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive. X5R capacitance change within ±15% in temperature range of 55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The output capacitance of the AW87519's chargepump recommends X5R ceramic capacitors.

***b) Voltage Stability***

Class II type capacitor has poor voltage stability ——Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V, the package size is 0805, 1206 or 0603, the capacitance value is 10μF. The capacitor's voltage stability of different types of capacitor is as shown below:

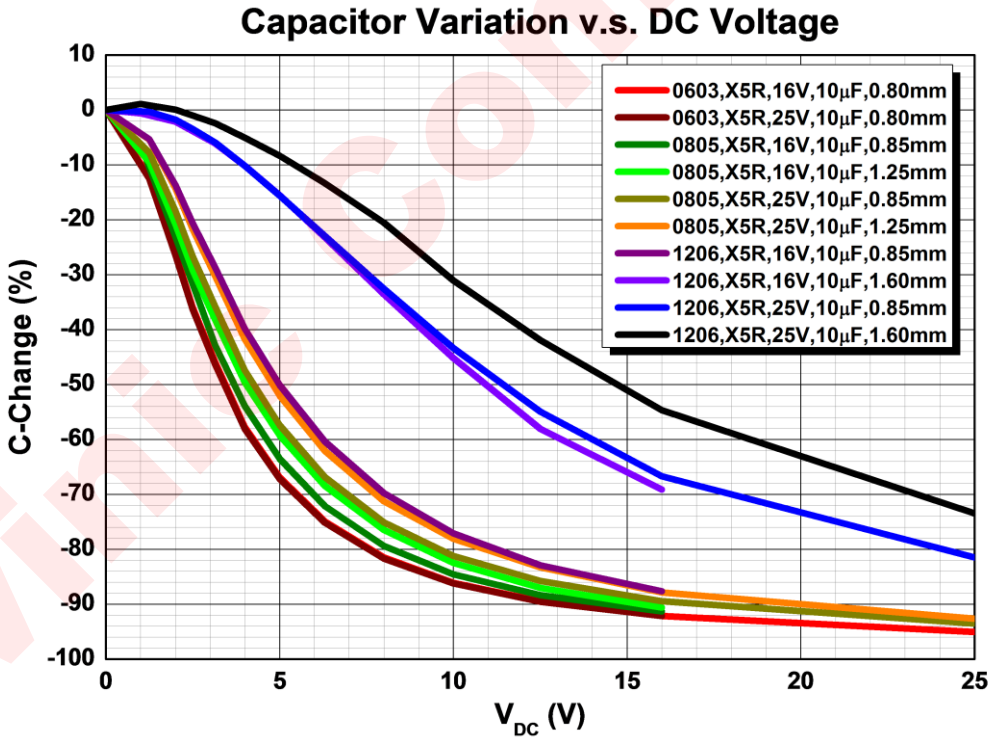


**Figure 20 Different Types of Capacitive Voltage Stability**

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. The higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of


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smaller package size (0603) capacitor change affected by the pressure value is very small.

**In AW87519 typical applications, it is necessary to ensure the output value of the PVDD capacitor ≥6μF when PVDD=8.5V.**

Take the following capacitances as the Boost of the output capacitor for example:

| value | material | size ($mm^3$) | rated voltage (V) | quantity | value@8.5V |
|---|---|---|---|---|---|
| 10uF | X5R | 1.60×0.80×0.80 (0603) | 16 | 4 | 6uF |
| 10uF | X5R | 2.00×1.25×1.25 (0805) | 25 | 3 | 6.3uF |

As for the different manufacturers' capacitors, it's important to determine the type and quantity of the capacitors through the capacitor voltage stability data provided by the manufacturer.

***Input Capacitor-$C_{in}$（input high-pass cutoff frequency）***

The input capacitors and input resistors form a high-pass filter to filter out the DC component of the input signal. The -3dB frequency points of the high pass filter is shown below：

$$f_H(-3dB)=\frac{1}{2*\pi*R_{intotal}*C_{in}}(Hz)$$

The selection of a smaller Cin capacitor in the application helps to filter out 217Hz noise, which comes from the input coupling, and the smaller capacitor is advantageous to reduce the pop-click noise when the power amplifier turn on.Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise. A capacitor value deviation of 10% or better capacitance is recommended.

Take typical application as an example, the input high-pass cutoff frequency is calculated as below:

$$f_H(-3dB)=\frac{1}{2*\pi*R_{intotal}*C_{in}}=\frac{1}{2*\pi*9k\Omega*68nF}(Hz)=260Hz$$

Class D-type speaker & receiver 2-in-1 application (Gain=9dB), the input high pass frequency is as follows:

$$f_H(-3dB)=\frac{1}{2*\pi*R_{intotal}*C_{in}}=\frac{1}{2*\pi*24k\Omega*68nF}(Hz)=98Hz$$

***Supply Decoupling Capacitor（$C_S$）***

A good decoupling capacitor can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance, the ESR value of the capacitor should be as small as possible. In AW87519 applications, low ESR (equivalent-series-resistance) X7R or X5R ceramic capacitors are recommended. Generally, 10μF ceramic capacitors are used to bypass the VDD to the ground, and the decoupling capacitor should be placed as close to the VDD chip as possible in the layout. If you want to filter out low-frequency noise better, you need to add a 10μF or greater decoupling capacitor depending on your application. Meanwhile, a 33pF~0.1μF ceramic capacitor is placed on the pin of the power supply to filter the high frequency interference on the power supply. The capacitor should be placed as close as possible to the pin3 and inductor.

***Output beads, capacitors, TVS***

Using EEE technology, in the class K mode, the AW87519 can also meet the FCC CLASS B specification


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requirements. It is recommended to Use ferrite chip beads and capacitors if device near the EMI sensitive circuits, there are long leads from amplifier to speaker, placed as close as possible to the output pin.

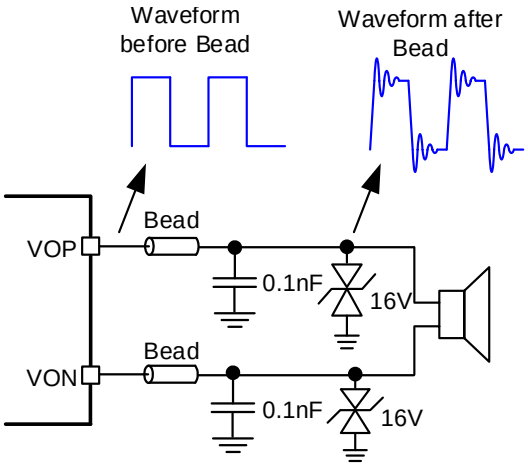


**Figure 21 Ferrite Chip Bead and Capacitor**

Amplifier output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

Power amplifier output PWM signals of high voltage to PVDD voltage, voltage to 8.5 V, will produce some ringing after bead capacitor, resulting in higher peak voltage. Recommended choose the operating voltage of 16V TVS.

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# PCB AND DEVICE LAYOUT CONSIDERATION

## EXTERNAL COMPONENTS PLACEMENT

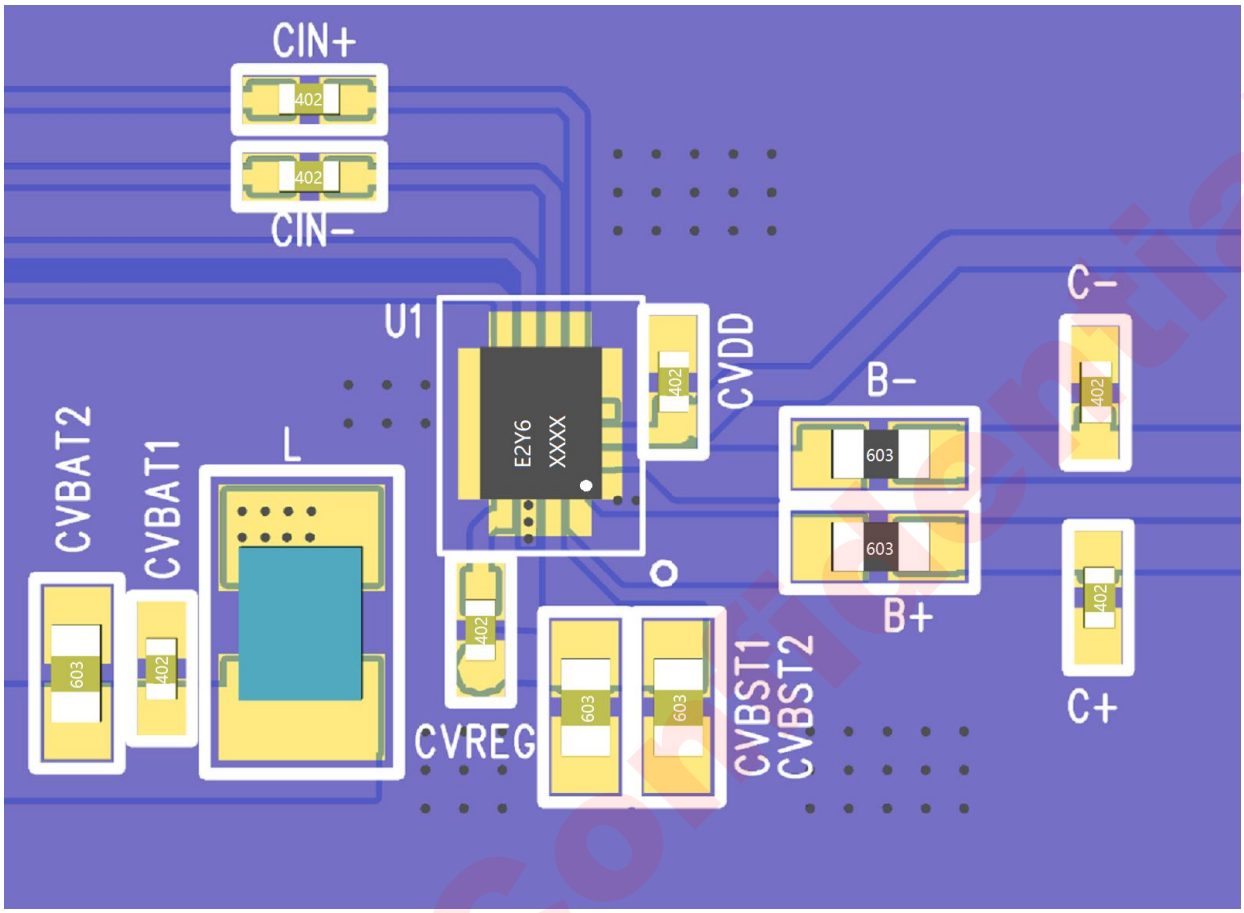


**Figure 22 AW87519 External Components Placement**

## LAYOUT CONSIDERATIONS

This device is a power a power amplifier chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

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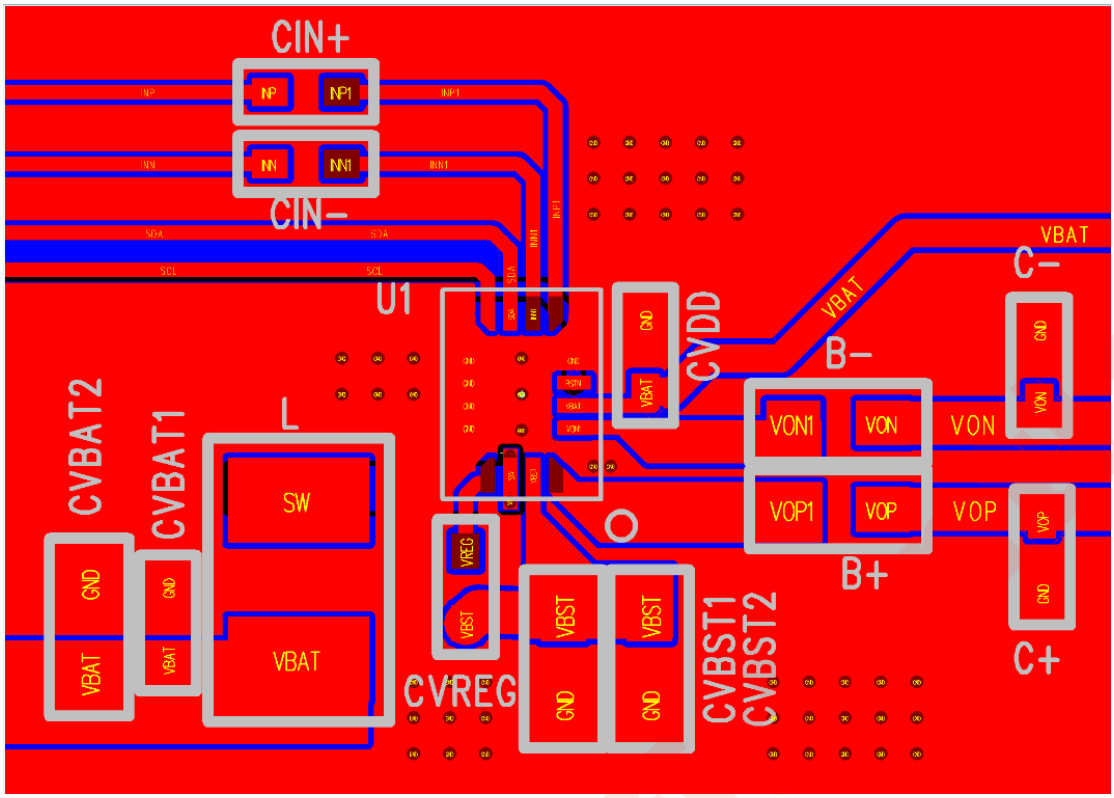


**Figure 23 AW87519 Board Layout**

In order to obtain excellent performance of AW87519, PCB layout must be carefully considered. The design consideration should follow the following principles:

1. In AW87519 peripheral device layout, you first need to guarantee the chargepump output capacitance close to VBST pin.
2. All the filter capacitors of the audio PA (including CVDD, CVBST and CVREG) should be placed close to the pins of the chip.
3. Please place the VREG capacitor close to the VBST capacitor. The parasitic inductance of the CVREG capacitor should be less than 3nH. Minimize inductance as much as possible.
4. Traces of SW pin should support currents up to device over-current limit (peak current 3.5A).
5. Try to provide a separate short and thick power line to AW87519, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin.
6. The input capacitors should be close to AW87519 INN and INP input pin, the input line should be parallel to suppress noise coupling.
7. The beads and capacitor should be placed near to AW87519 VON and VOP pin. The output line from AW87519 to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.


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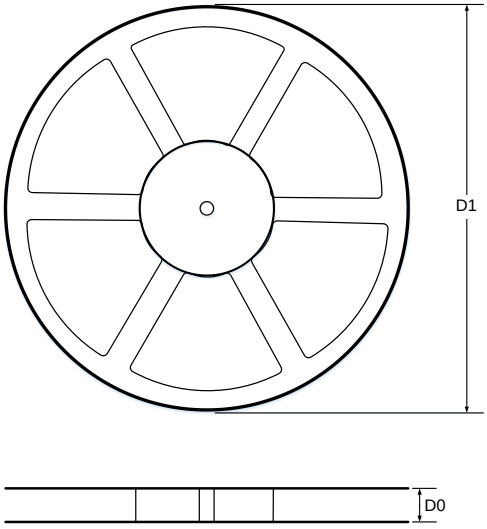
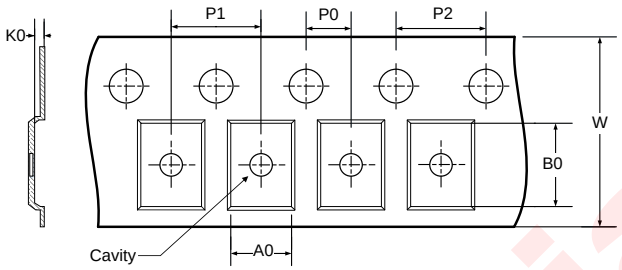
# TAPE & REEL DESCRIPTION

REEL DIMENSIONS

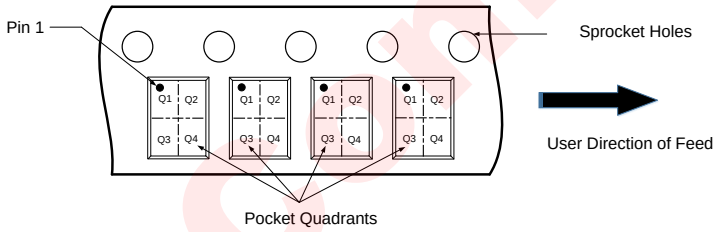



TAPE DIMENSIONS




A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




**All Dimensions are nominal**

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| 330 | 12.4 | 2.3 | 3.3 | 0.75 | 2 | 4 | 4 | 12 | Q1 |

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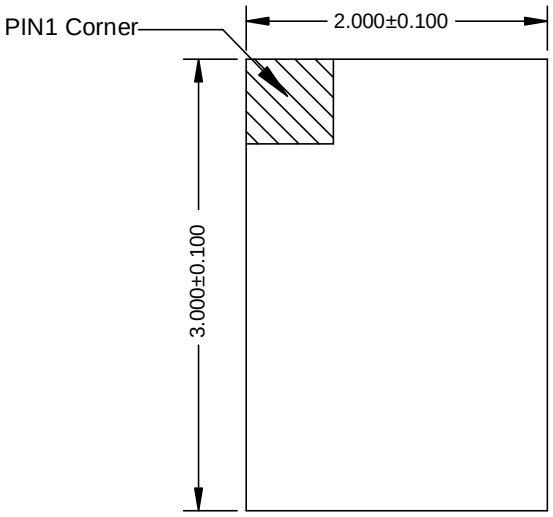
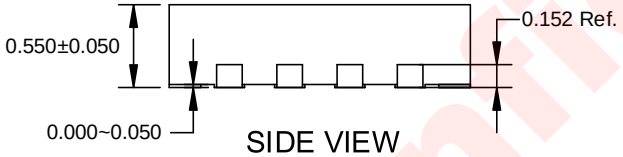
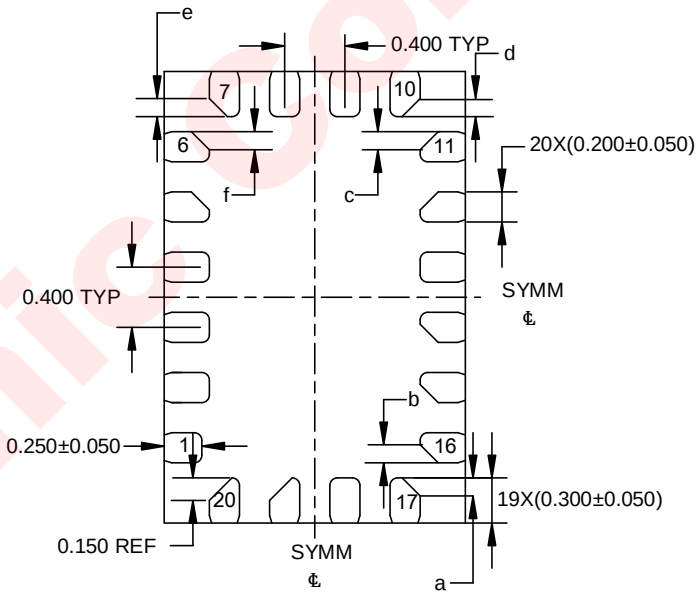
# PACKAGE DESCRIPTION




TOP VIEW




SIDE VIEW




Note: a=b=c=d=e=f=0.120mm

BOTTOM VIEW

Unit：mm

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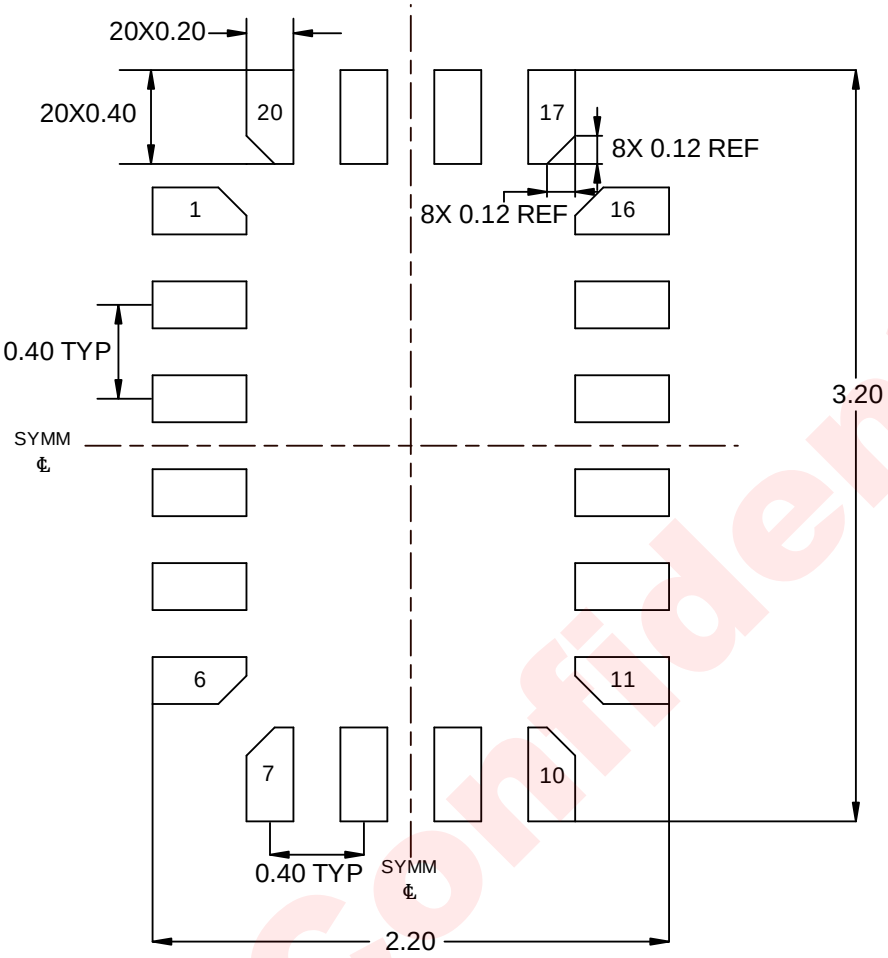
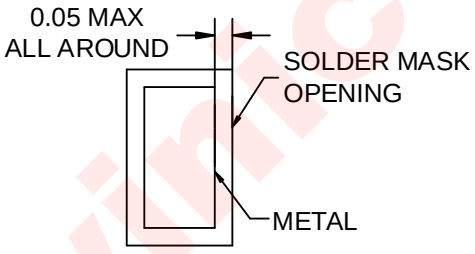
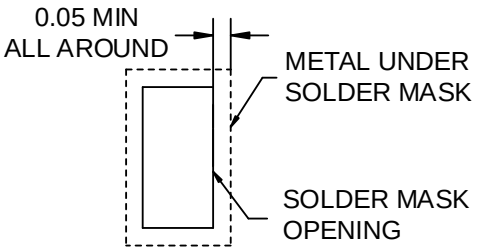
## LAND PATTERN




NON-SOLDER MASK DEFINED




SOLDER MASK DEFINED

Unit：mm

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# VERSION INFORMATION

| Version | Date | Description |
|---|---|---|
| V1.0 | 2019-01-28 | AW87519FCR datasheet V1.0 |
| V1.1 | 2019-05-24 | 1. Modify PCB and Device Layout<br>2. Modify package description and Land pattern |
| | | |
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