

ALTERA®

亞洲創新設計大賽

友晶科技 彭顯恩



大賽精神及目的

- 提供跨國界的高階設計比賽環境
 - 超過50所大專院校，近300位頂尖學生的參與，彼此觀摩及切磋
- 提供學生一個挑戰自我，超越極限的機會
 - 得獎團隊的優秀作品將刊登於「ALTERA 年度 FPGA 競賽全紀錄出版品」
 - ALTERA 美國總部大學計劃部門將推薦傑出學生進入相關領域研究深造或提供工作機會
- 提供跨領域的應用平台
 - 由 MathWorks 和 Linear Technology 全力贊助所需硬軟體

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FPGA 於科技領域之應用

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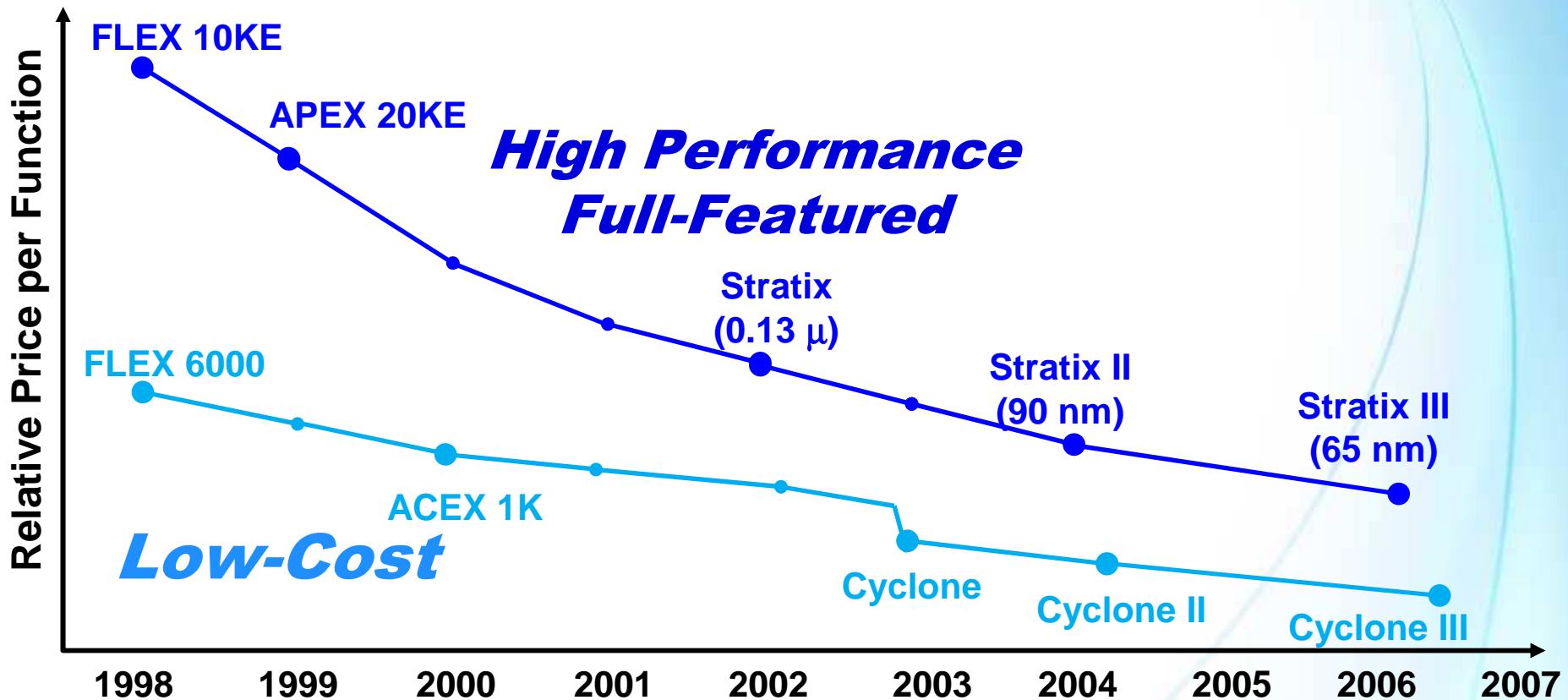
友晶科技簡介



- 2003 成立. 資本額 2 億五千萬.
- 2007 年營收兩億六千萬
- Altera 在系統設計上之戰略合作夥伴
- 獲頒 2006 年最佳 Altera 供應商獎 (TSMC, Amkor, Kinsus)
- 台大慶齡中心, 台大電機所, 工業局半導體學院開課單位.

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Altera FPGA Roadmap



Dual-Pronged FPGA Strategy

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FPGA 提供業界一個理想的產品實現方法

- 提供最高端, 工業等級之 FPGA 器件及開發平台.
- 提供豐富完整之外圍接口
- 提供許多工業等級參考設計, 加速產品開發
- 可靈活組成所需之硬軟體平台
- 使少量多樣化的產品能享受 90nm, 65nm, 45nm 等先進製程
- 提供生醫產業一個重要的研發工具

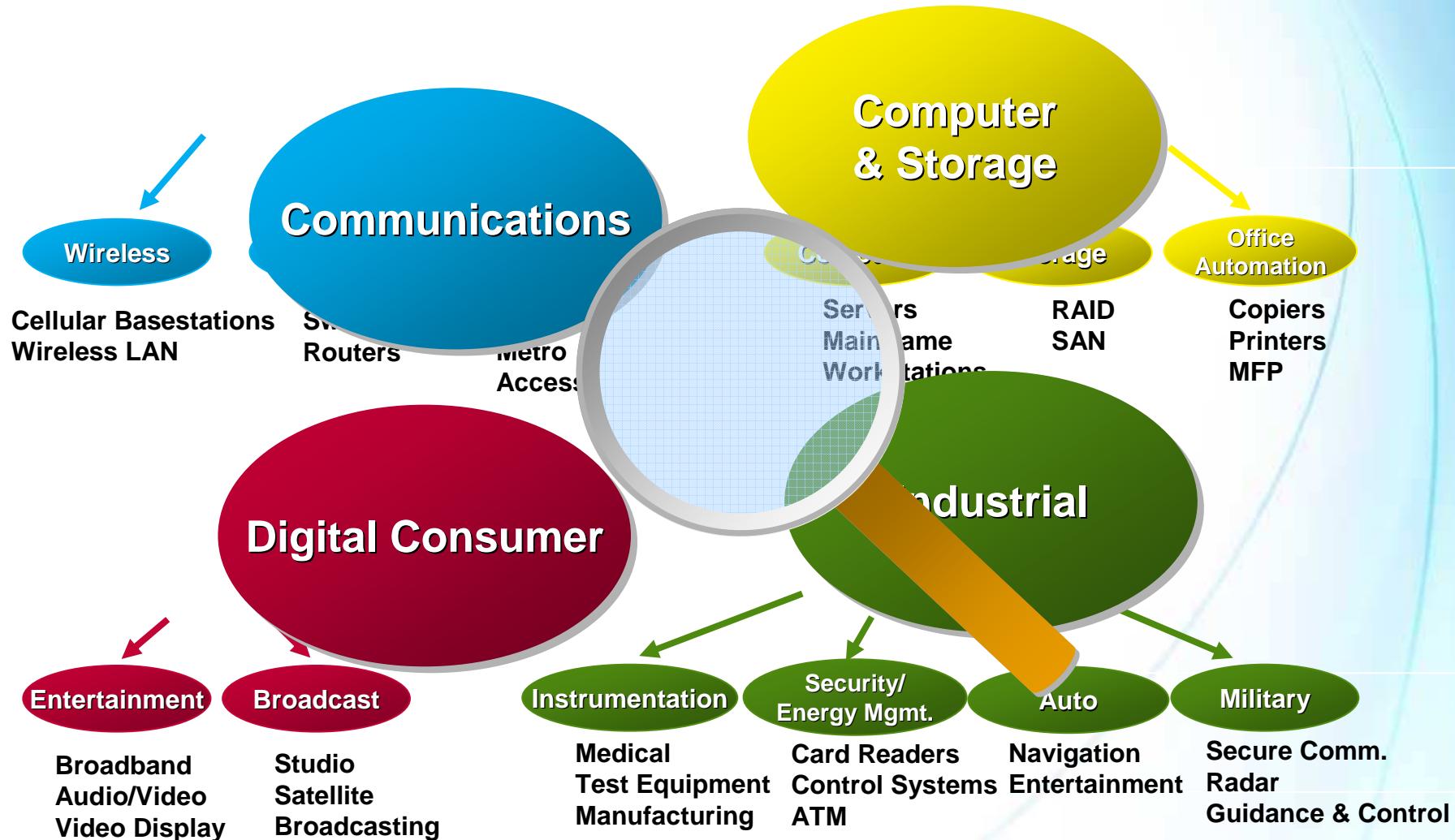
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FPGA 提供學界一個理想教學平台

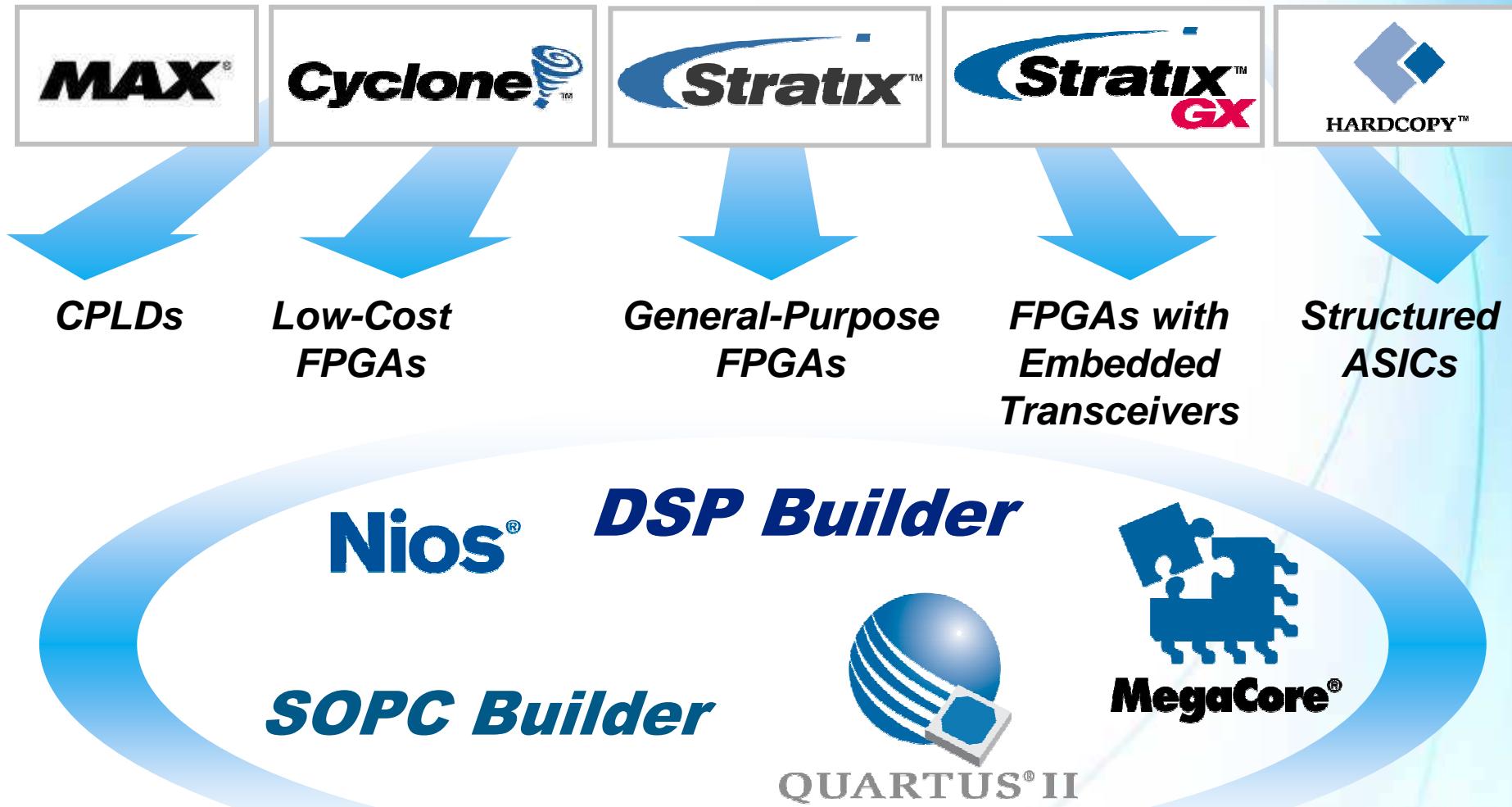
- 提供最高端, 工業等級之 FPGA 器件.
- 實作數位設計, CPU, 嵌入式系統, DSP 等課程
- 提供豐富完整之外圍接口
- Altera 教授級顧問提供全球統一同步教材
- 工業等級參考設計 - 讓學生第一天上班就有競爭力
- 全球名校教學及研究平台有共同語言
- 提供業界最完整的 FPGA/ASIC/SOPC 在職訓練平台

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End Market Focus



Product Overview



Examples (details will be provided later)



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Ultra Electronics AN/GRC-512A(V) Radio Relay



Application:

Software-Defined Radio

Industry:

Military

Altera Value Proposition:

- **Stratix II Security Solution Enables Avoidance of Costly Gate Array Conversion**
- **Stratix II Density and DSP Performance + Nios II Processor Allows Three PC Boards to Be Replaced by Single Board**

Altera Products Chosen:

Stratix® II MAX® II
Nios® II

"The security feature in the Stratix II device allows easy and inexpensive protection of our IP as we work with our manufacturers. The high capacity and exceptional digital signal processing performance of Stratix II devices combined with Nios II processors enabled us to add firmware-based support for additional waveforms, which extends our product lifetime"

—Stéphan Charbonneau, Radio Products Manager

UniTest UNI460 and UNI560 SDRAM Testers



"We chose Stratix II FPGAs because they provide the highest-performance DDR2 memory interfaces. We have achieved DDR2 interface speeds of up to 400 MHz and data rates of 800 Mbps with Stratix II FPGAs, which enables us to deliver industry-leading capabilities in our UNI460 and UNI560 SDRAM testers."

—Kang Jong Koo, Chief Research Engineer

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Application:

Memory Testers

Industry:

Test and Measurement

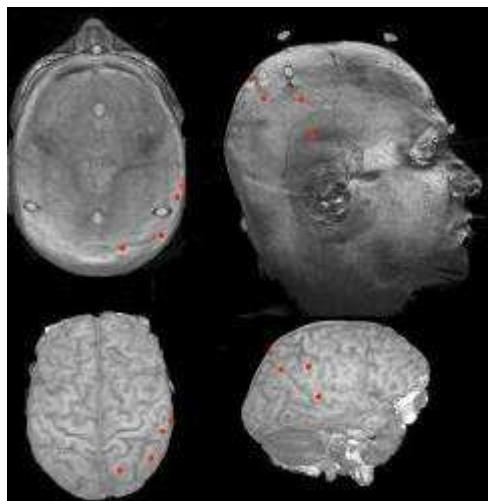
Altera Value Proposition:

- *Highest Performance DDR2 SDRAM Interface Enables Industry-Leading Memory Test Capabilities*
- *Highest-Performance Logic for Rapid Pattern Generation*
- *FPGA Reconfigurability Supports Different Testing Configurations*

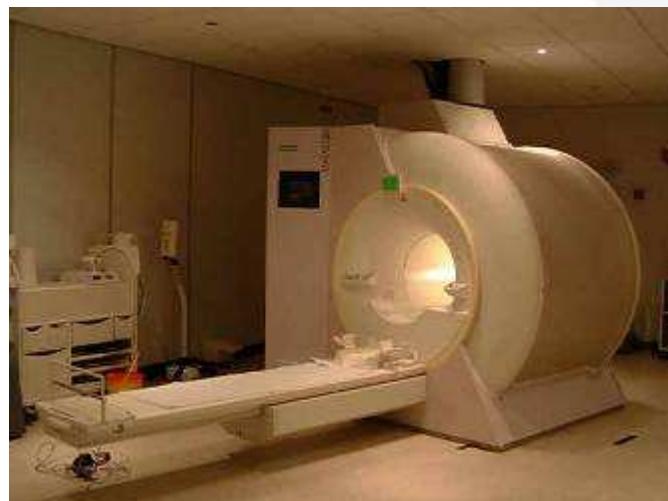
Altera Products Chosen:



Medical Imaging (X-Ray, CT, Ultrasound)



© 2007 Altera Corporation



Application:

Medical Imaging

Industry:

Altera Value Proposition:

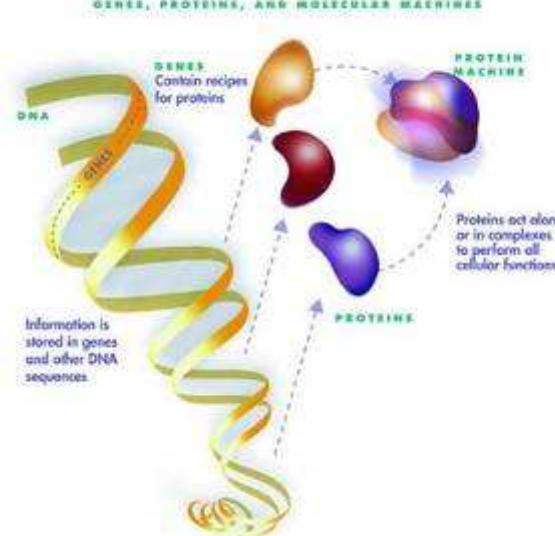
- *Highest Performance DDR2 SDRAM Interface Enables Industry-Leading Memory access Capabilities*
- *Highest-Performance Logic for Rapid Pattern Generation*
- *FPGA Reconfigurability Supports Different Testing Configurations*

 **Stratix® II**

Altera Products Chosen:

 **ALTERA.**

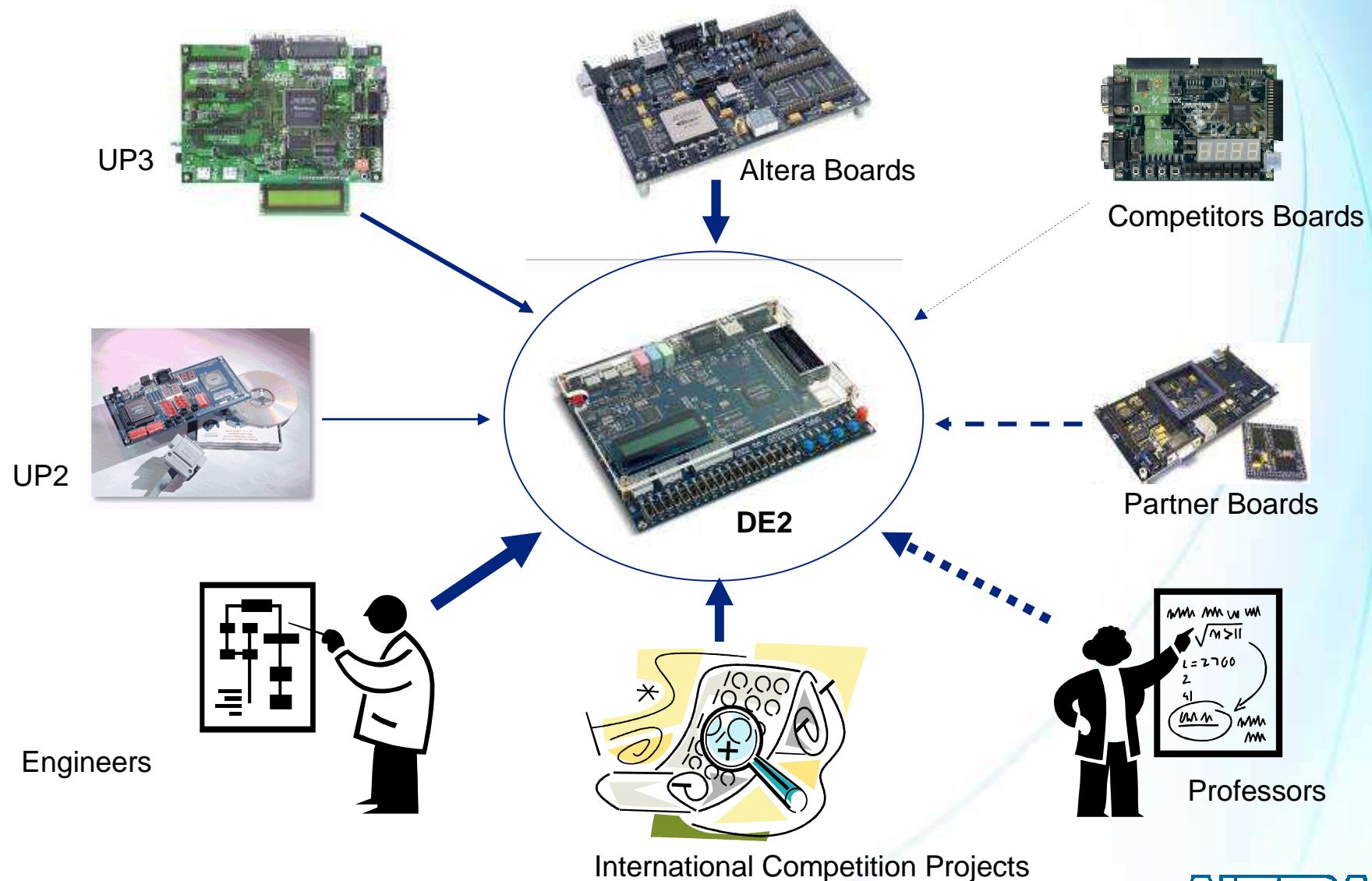
Bioinformatics (DNA, RNA, Protein, Drug Discovery)



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FPGA 平台及教材 – 滿足學界及業界所需



Altera DE2 目標 – 完整的硬軟件及教材



ALTERA DE2 Development and Education Board

The purpose of the Altera DE2 Development and Education Board is to provide the ideal vehicle for learning about digital logic, computer organization, architecture, and the latest in programmable technology. The board includes CAD tools, complete software, and professionals in a ready-to-use package. The board offers a lot of features. The board is intended for use as a laboratory instrument for university and college courses, for a variety of design projects, as well as for the development of replacement digital systems. Altera provides a wide range of supporting materials for the DE2 board, including manuals, "hands-on" laboratory exercises, and literature on various topics.

DE2 Board Features:

The DE2 board features a state-of-the-art Cyclone® II 20,000 FPGAs in a 872-pin package. All important signals, including clock, memory, and I/O, are available at the board edge. Altera's Cyclone II technology offers the lowest power consumption, the simplest design, the highest performance, and the lowest cost of ownership. The DE2 board includes a high-resolution grayscale monitor, full-function keypad, and two large and fast liquid-crystal displays. For more advanced experiments, there are VGA, S-VIDEO, and DVI-I connectors. The board also includes a 100-MHz processor and one standard serial port, such as RS-232 and PS2. The experiments that students would be able to perform include a digital oscilloscope, digital multimeter, logic analyzer, logic editor, bit-stream editor, JTAG debugger, and VGA/S-VIDEO. These features can be used for basic logic design, digital system design, and prototyping-looking designs. For large design projects, the DE2 provides 1500+ 2.5-micron-equivalent density logic and memory cells, 1000+ 18x18 macrocells, 1000+ 18x18 LDDs, and an 80 memory card connector. Finally, it is possible to connect other user-defined boards to the DE2 board by means of three expansion headers.

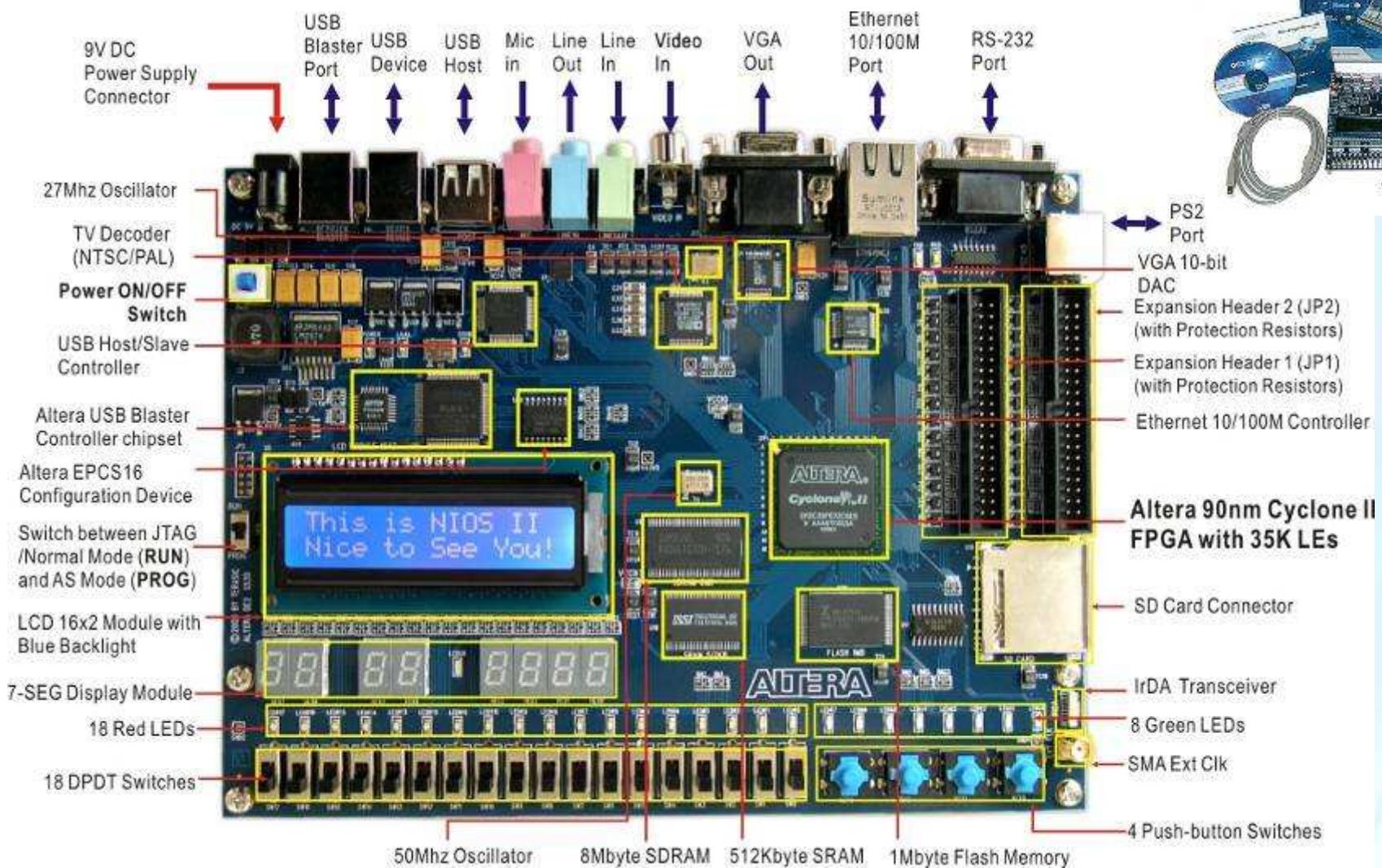
Supporting Material:

Altera provides the DE2 board featuring the Cyclone® II Web Edition CAD viewer and the Nios® II Processor Development Environment (PDE) to help students and professionals experiment with features of the board, such as memory and memory applications.

Technically, manufacturers of educational FPGA boards have provided a variety of hardware designs and software CAD tools needed to implement designs at those levels. Few were truly complete; few have offered that could be used directly for teaching purposes. Altera's DE2 board is a significant departure from this trend. In addition to the DE2 board's hardware and software, Altera Components provides a full set of associated software components that make it easy to immediately begin the typical classroom logic design and computer experiments. In effect, the DE2 board and the available software may be used as a ready-to-use platform for both university and college courses.

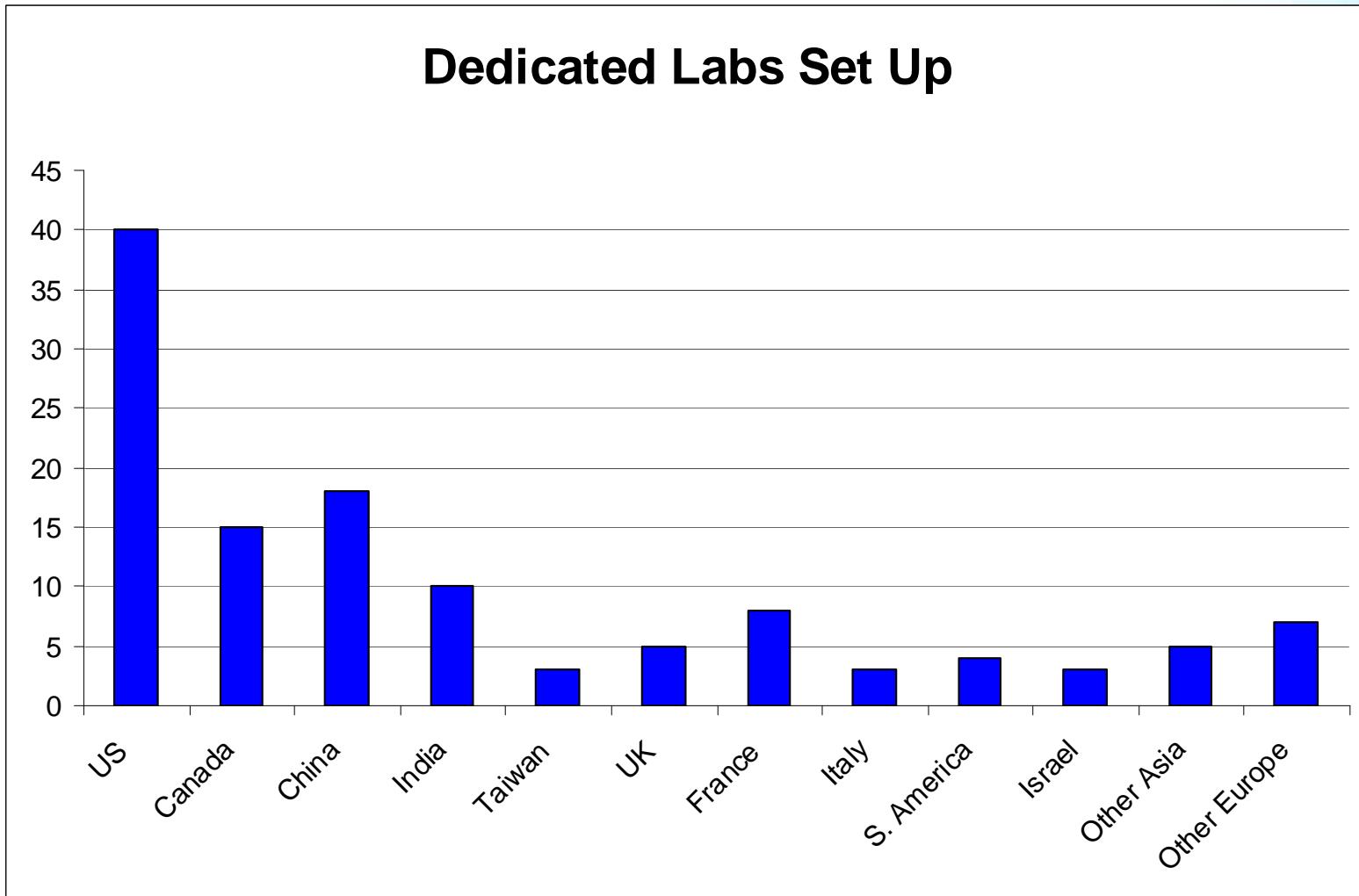
Altera Components

Altera DE2 提供豐富完整之外圍接口



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全球超過 350 個重點名校設立 DE2 實驗室



採用 DE 系列做為訓練/開發平台之單位 (僅列部份)

美國 · 麻省理工學院	
康乃爾大學 · 美國	
英國 · 剑橋大學	
史丹佛大學 · 美國	
加拿大 · 多倫多大學	
北京工業大學 · 中國	
中國 · 上海交通大學	
國立台灣大學 · 台灣	
南韓 · 首爾大學	
國立台灣科技大學 · 台灣	
台灣 · 國立交通大學	



DE2 使用單位(學校部份 – 僅列部份)

- University of Michigan, Ann Arbor
- Cornell University
- University of Mass
- Cambridge University, UK
- Stanford University
- University of Toronto
- U of Waterloo
- Caltech
- MIT
- Chalmers Technical University
- Ben Gurion University
- Tel Aviv
- Ecole Supérieure d'Electricité (ESE)
- Beijing Industrial University
- Auckland University
- Monash University
- IIT Guwahati
- Shanghai Jiaotong University
- Shandong University
- National Taiwan University.
- KWANGWOON University
- Seoul National University
- SOGANG University
- Shin Heung College
- Dong-Seoul College
- University of Incheon
- Guiling University
- Beijing IT University
- Nanjing University Aeronaut and Astronautics
- WuHan University
- China University of Mining & Technology
- Eastern China Normal University
- WUHAN University Southern Taiwan University of Technology
- National United University
- National Taiwan University of Science and Technology
- University of I-Lan
- National Chiao Tung University

DE2 使用單位(業界 – 僅列部份)

- **HP**
- **AMD**
- **LG**
- **Philips**
- **IBM**
- **Microsoft**
- **SigmaTel**
- **ATI**
- **Northrop Grumman**
- **Jabil**
- **TI**
- **Simems**
- **Juniper**
- **Nokia**
- **Wright Patterson Air Force Base**

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使用者一致推薦！

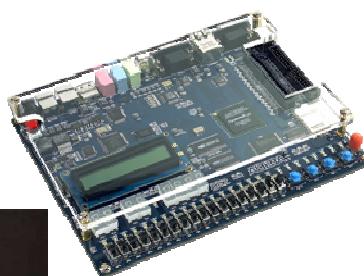
"In my opinion, the DE2 board is hands down the best board I have ever seen. It is clear from reading through documentation and inspecting the pcb this board is well thought out. **Even down to the design examples provided, it is the best documented board I have seen.**"

(這是我見過支援文件最充足的開發平台)

Douglas Hodson,

Wright Patterson AFB

(www.wpafb.af.mil) (美國空軍基地)



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課堂最好的教學平台

" We use this platform at both undergraduate and masters level for the teaching of system-on-chip. It is important to back up academic concepts with hands-on learning.

With all the flexibility offered on this platform, project are only limited by ingenuity and imagination."

(憑藉著這平台提供的彈性，
只有想像力和實作能力的不足
才會限制專題的發展!)

Dr Steven Freear, Lecturer in
System-On-Chip, University of Leeds

(www.leeds.ac.uk)

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Columbia University

DE 系列的用戶回饋!

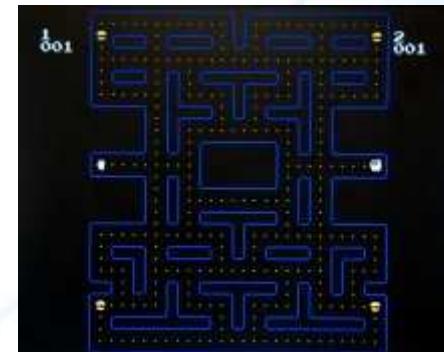
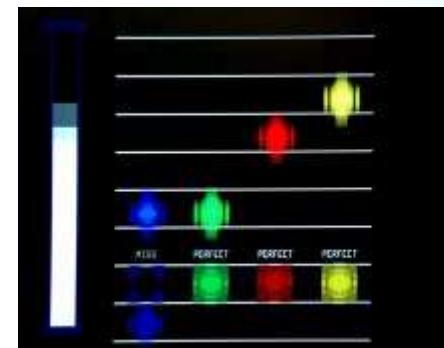
“We currently use the DE2s for the course,
and I **love them!** ...

I am **a huge fan** of your products!

Hopefully with the ability to run uclinux on
them, more opensource and hobby software
programmers will become interested in FPGA
and hardware development. “

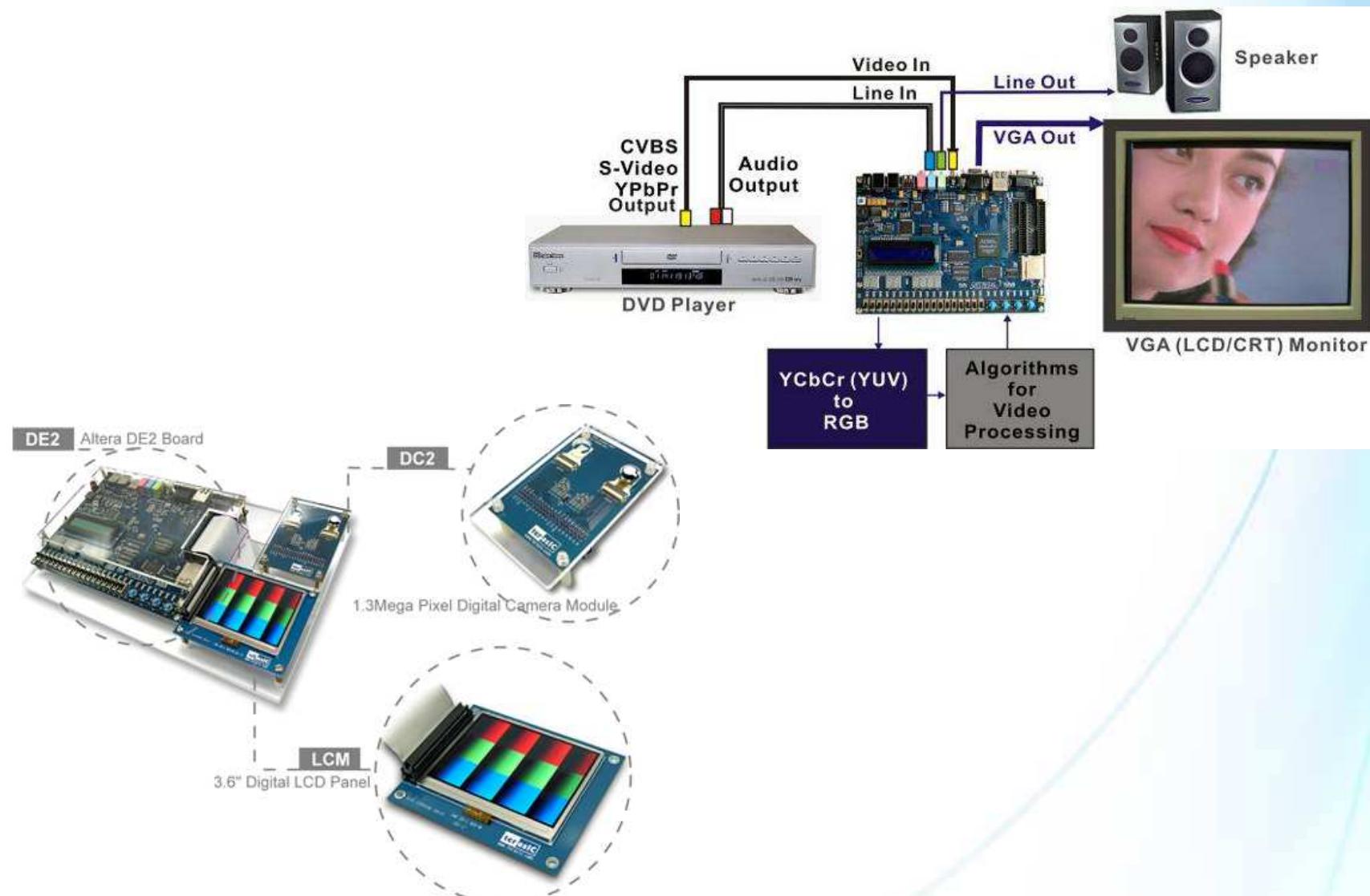
David Lariviere

**Teaching Assistant for the Embedded Systems
course at Columbia University**



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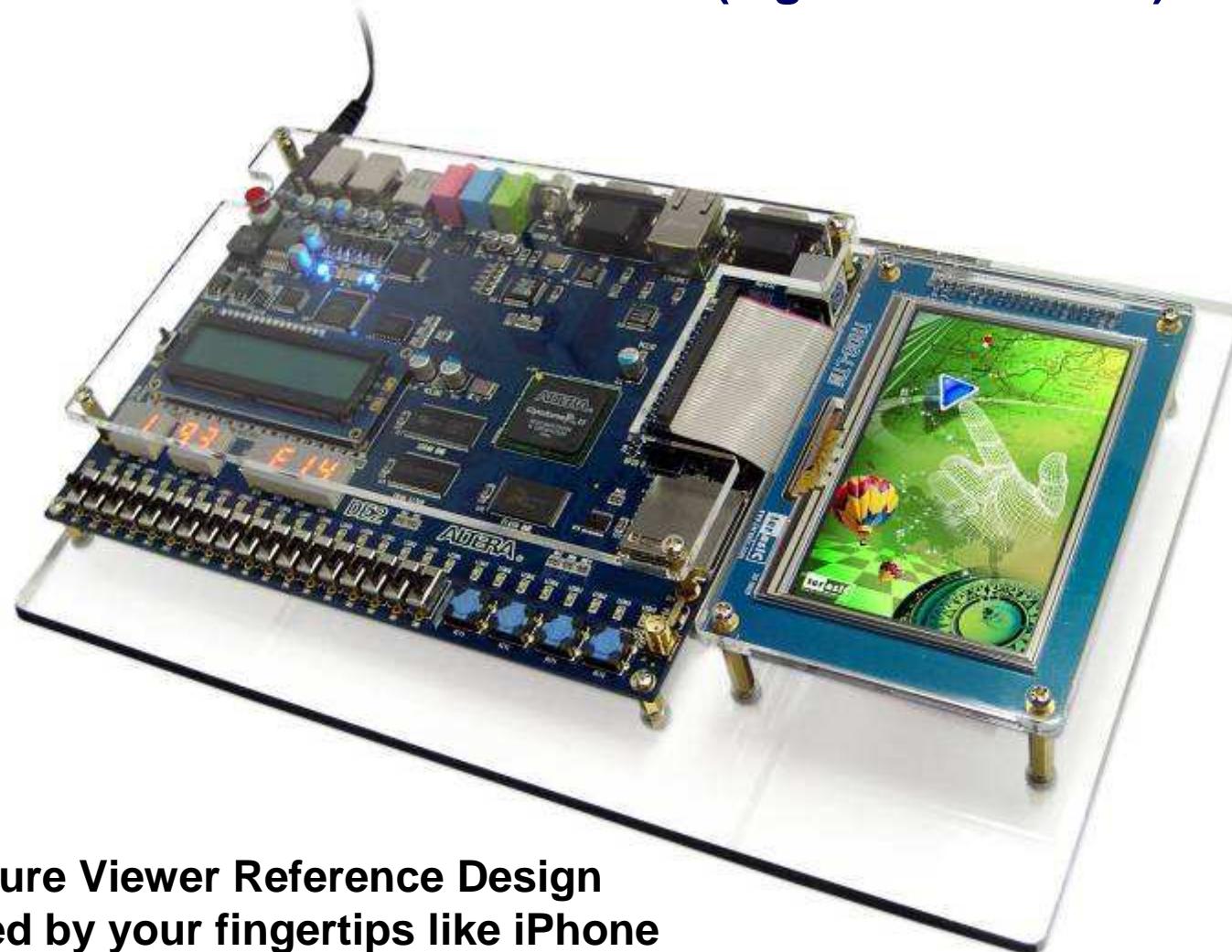
提供工業等級參考設計及相對應子卡



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DE2 高階觸控式 LCD 屏幕設計套件

- Provide 4.3" 800 x 480 Touch Panel (highest resolution)

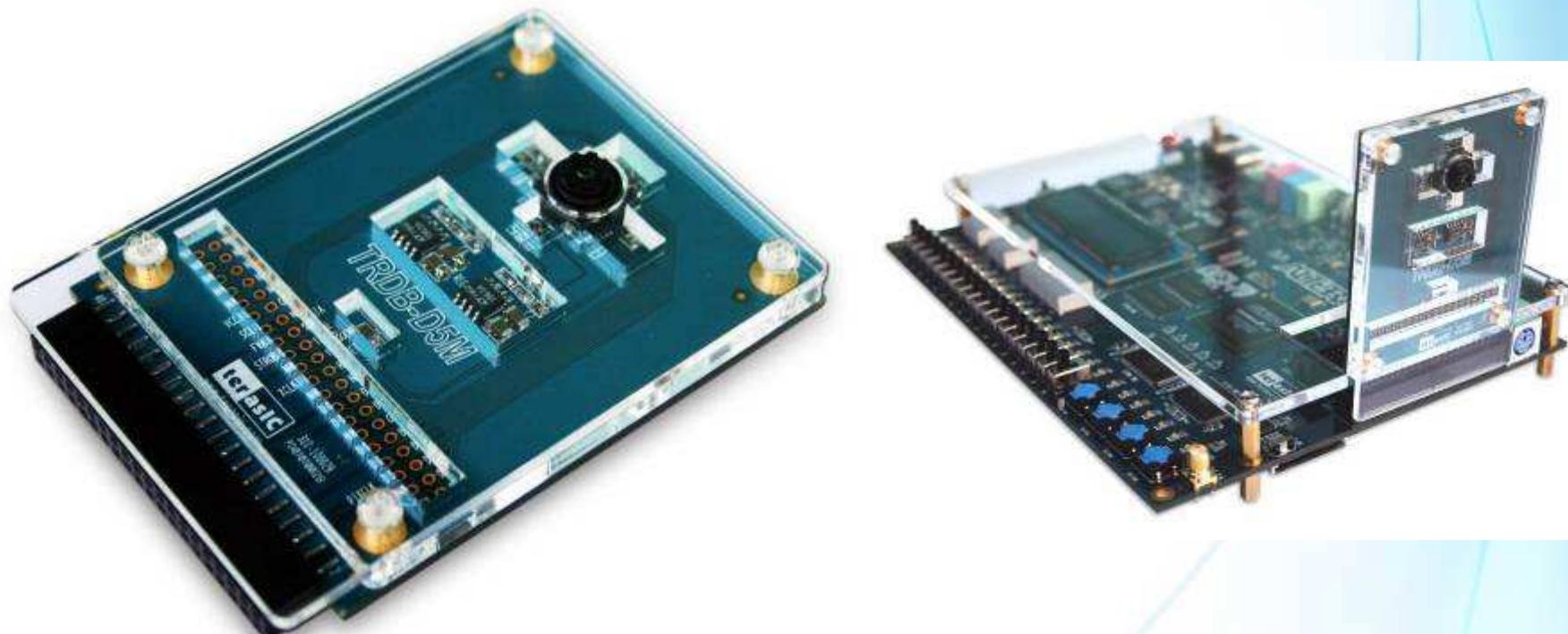


- Free Picture Viewer Reference Design
- Controlled by your fingertips like iPhone

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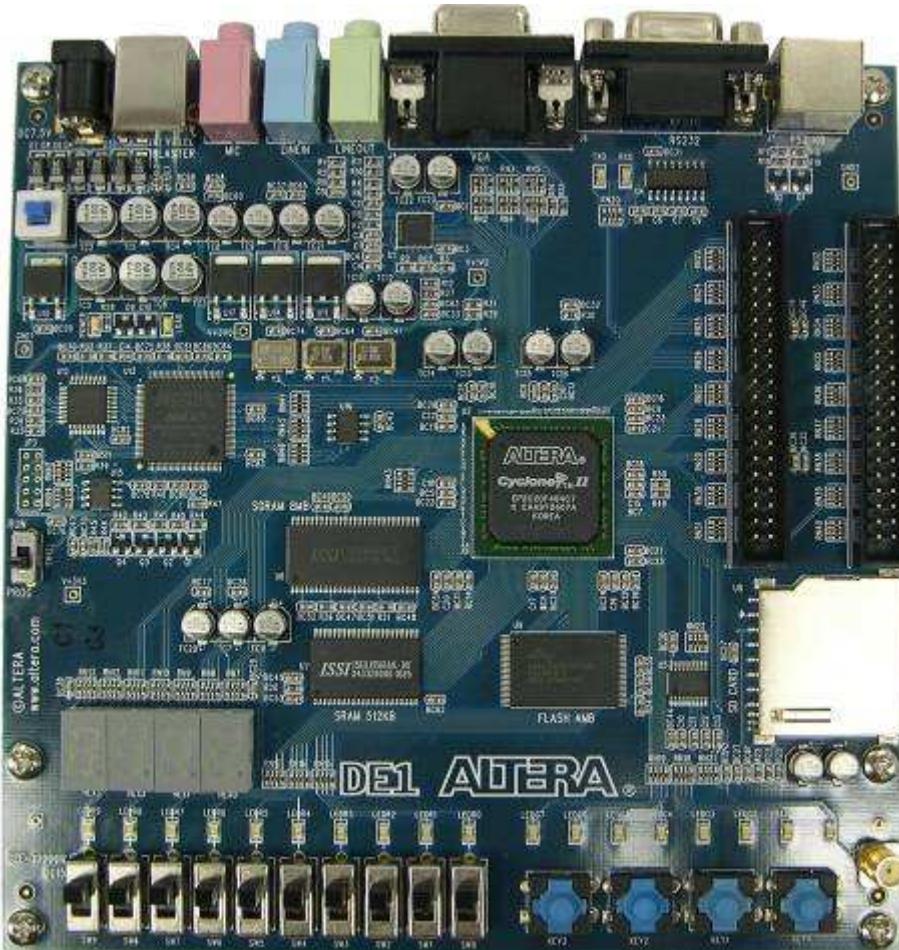
DE2 高階 5 百萬相素數碼相機開發平台

- Provide Micron 5Mega-pixel CMOS sensor
- Terasic Lens Module



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Altera DE1 – Development and Education Board

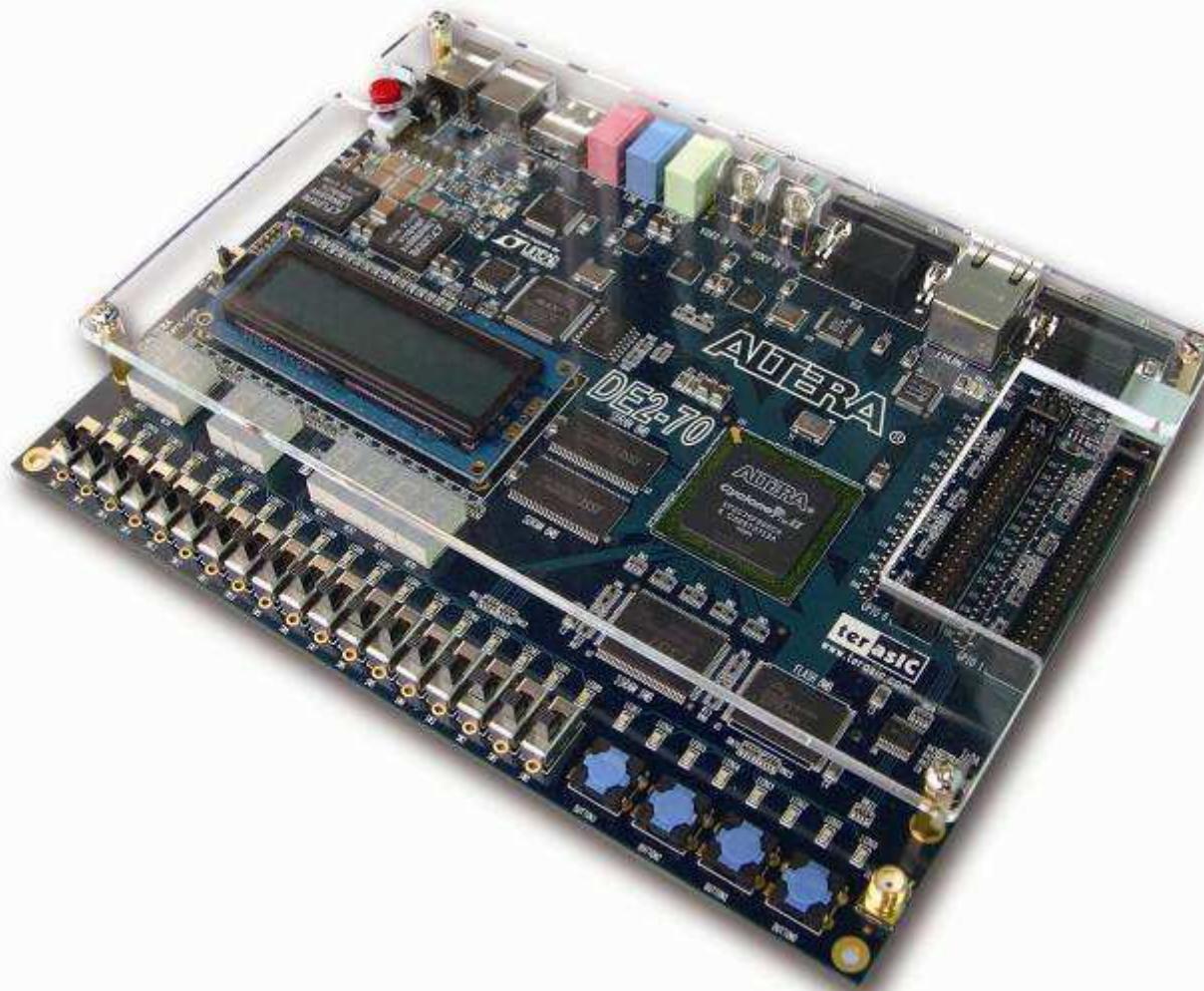


DE1 Board Feature Set

- EP2C20F484
- EPCS4 for configuration
- USB Blaster on board
- SDRAM (8Mbyte)
- SRAM (512Kb)
- Flash (4Mbyte)
- 24-bit Audio CODEC
- VGA Port
- RS-232 Port
- PS/2 Port
- SD/MMC Socket
- SMA ext clock input
- 10 Red/8 Green LEDs
- 2 x 40-pin Expansion Ports
- 4 x 7-seg display
- 10 SW & 4 Push Buttons

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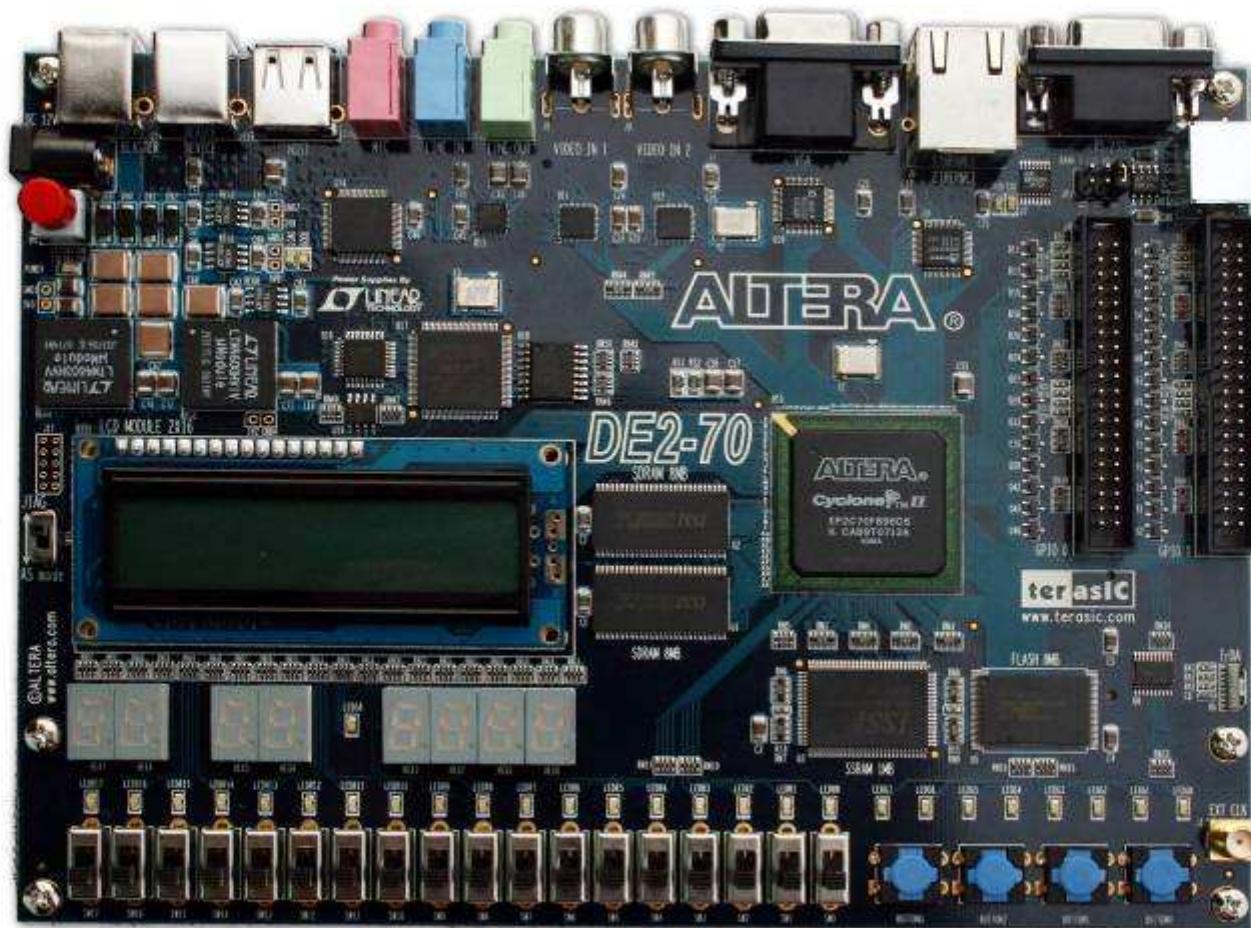
Altera DE2-70 (FPGA使用 2C70F892C6)



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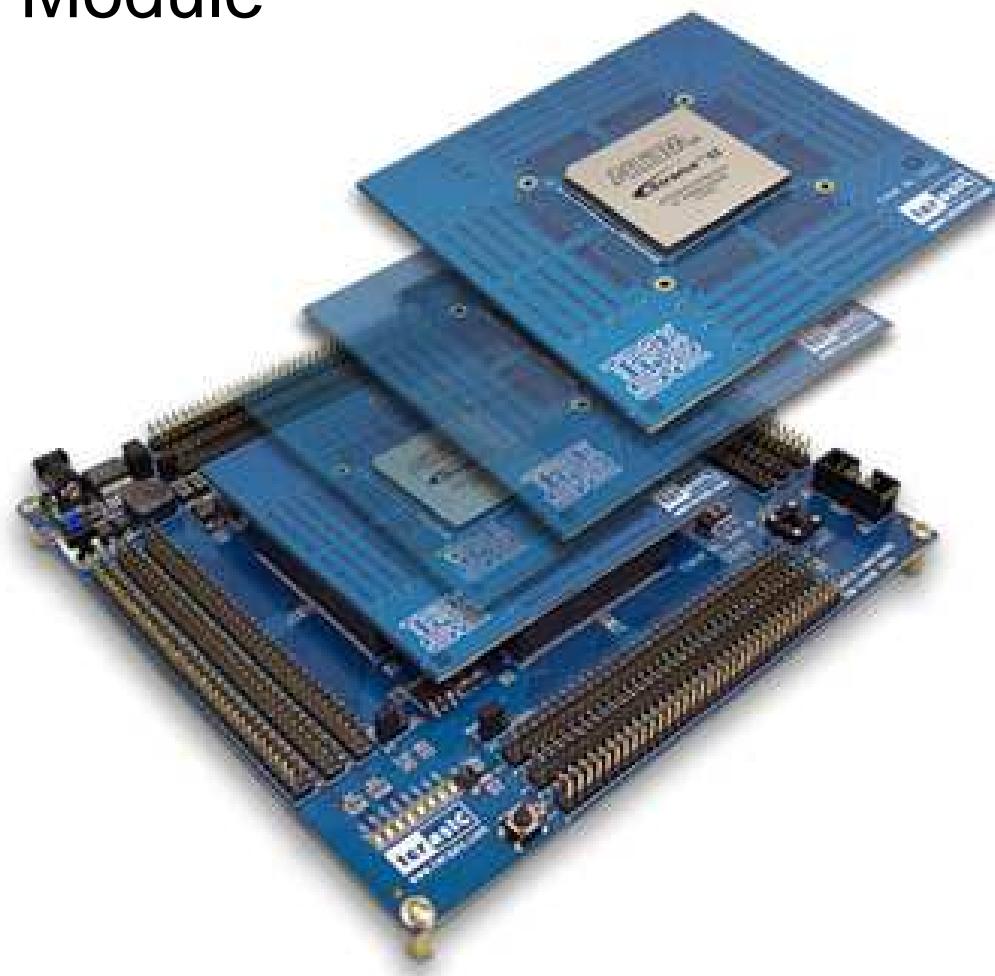
Altera DE2-70 (FPGA使用 2C70F892C6)

- 64Mbyte SDRAM, 2Mbyte SSRAM, 8Mbyte Flash, 2 x DTV input
- LVDS support on 2 x 40-pin Expansion ports



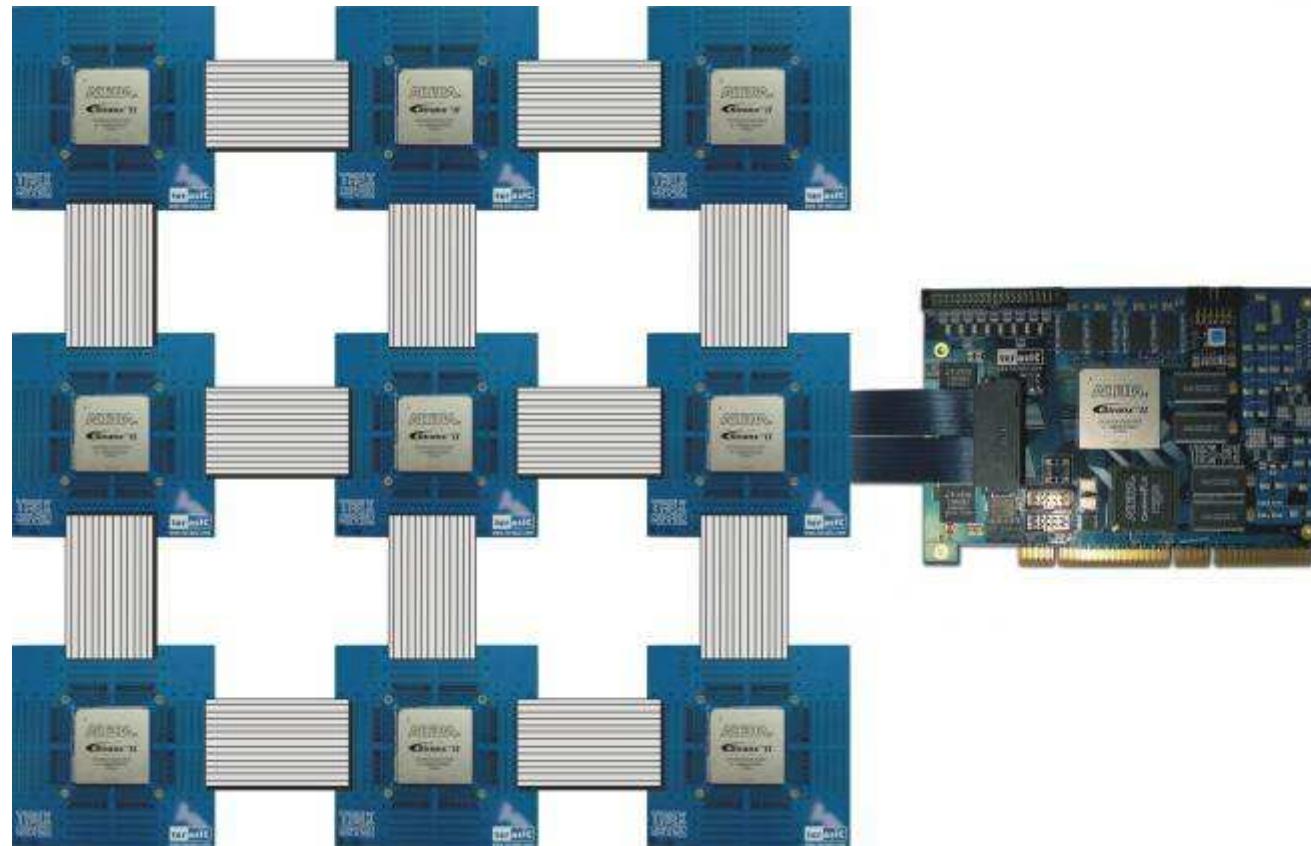
高階 Stratix II FPGA (2S60-180) 應用模組

■ TREX-S2 Module



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高階 Stratix II FPGA (2S60-180) 應用模組及下板



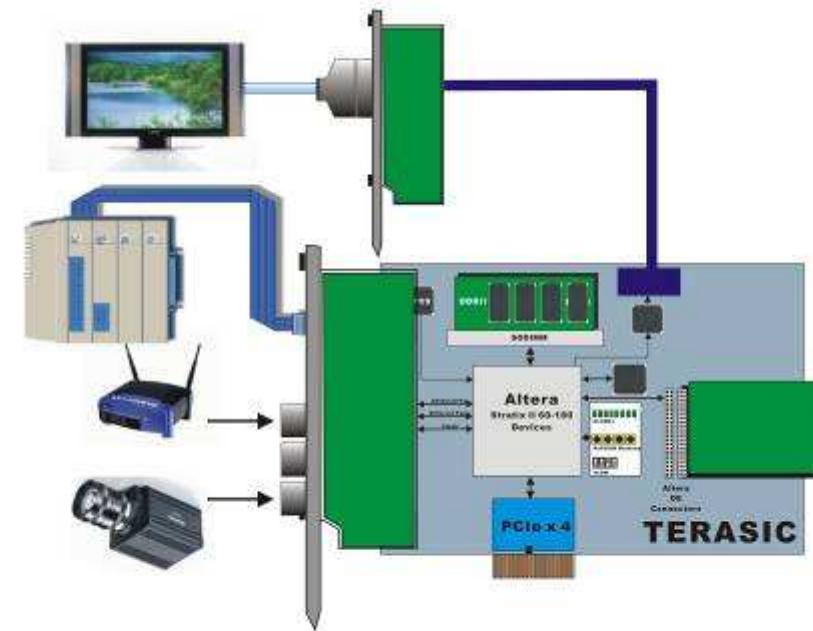
高階 Stratix II FPGA (2S60-180) PCI-X 平台

- PCI-X, DDRII, LVDS 影像平台



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高階 Stratix III FPGA 模組及 PCIe 平台 (OCT,07)



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全球第一片 **Cyclone III FPGA** 板卡

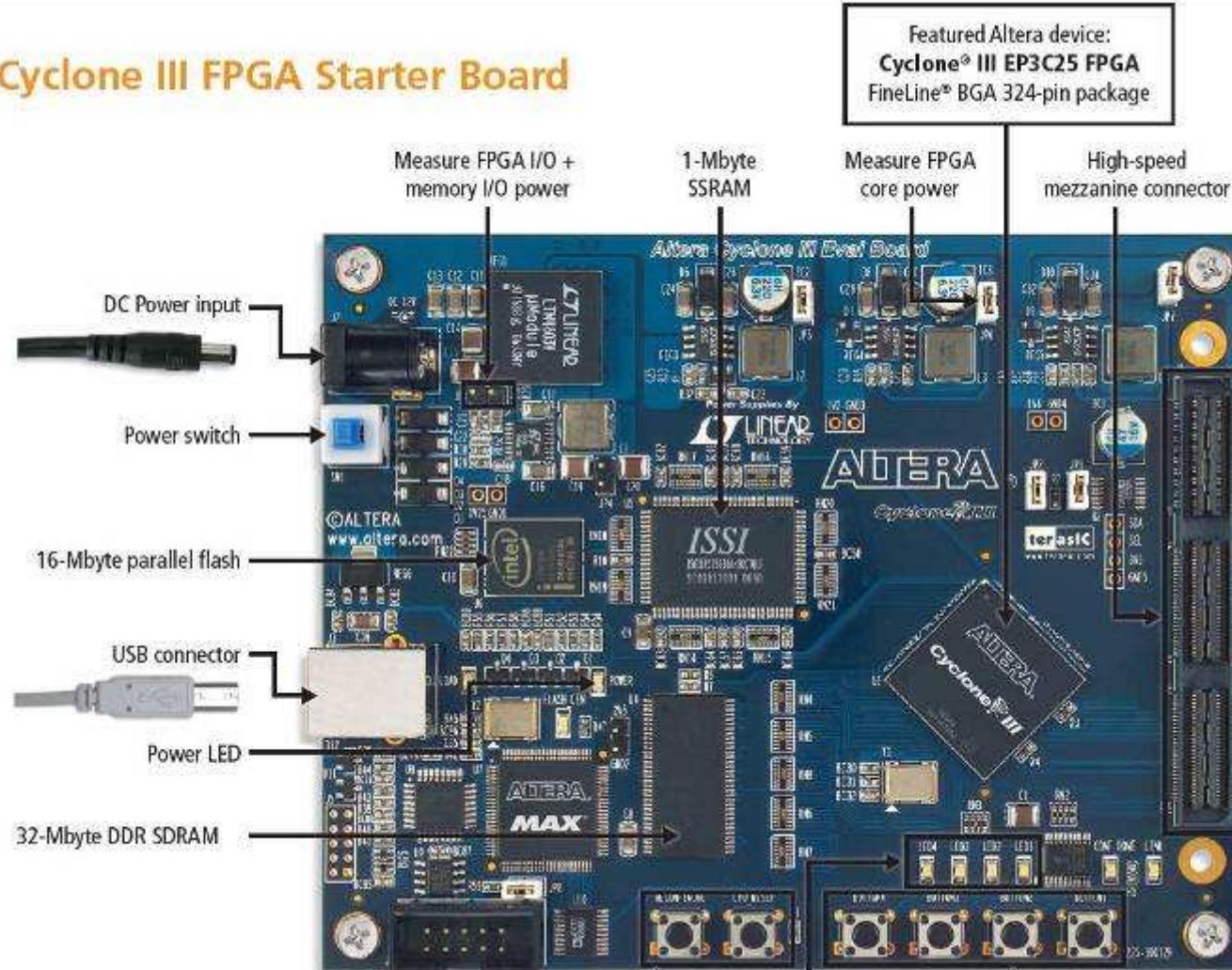
- DDR SDRAM, SSRAM, HSMC LVDS to 500Mbps



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全球第一片 Cyclone III FPGA 板卡

Cyclone III FPGA Starter Board



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Cyclone III FPGA 板卡之多媒體擴充子板



Altera Nios II 嵌入式處理套件
獲選全球 EDN 2007 年度
最佳創新產品大獎
總決賽前三名
投票給 Altera 支持友晶科技

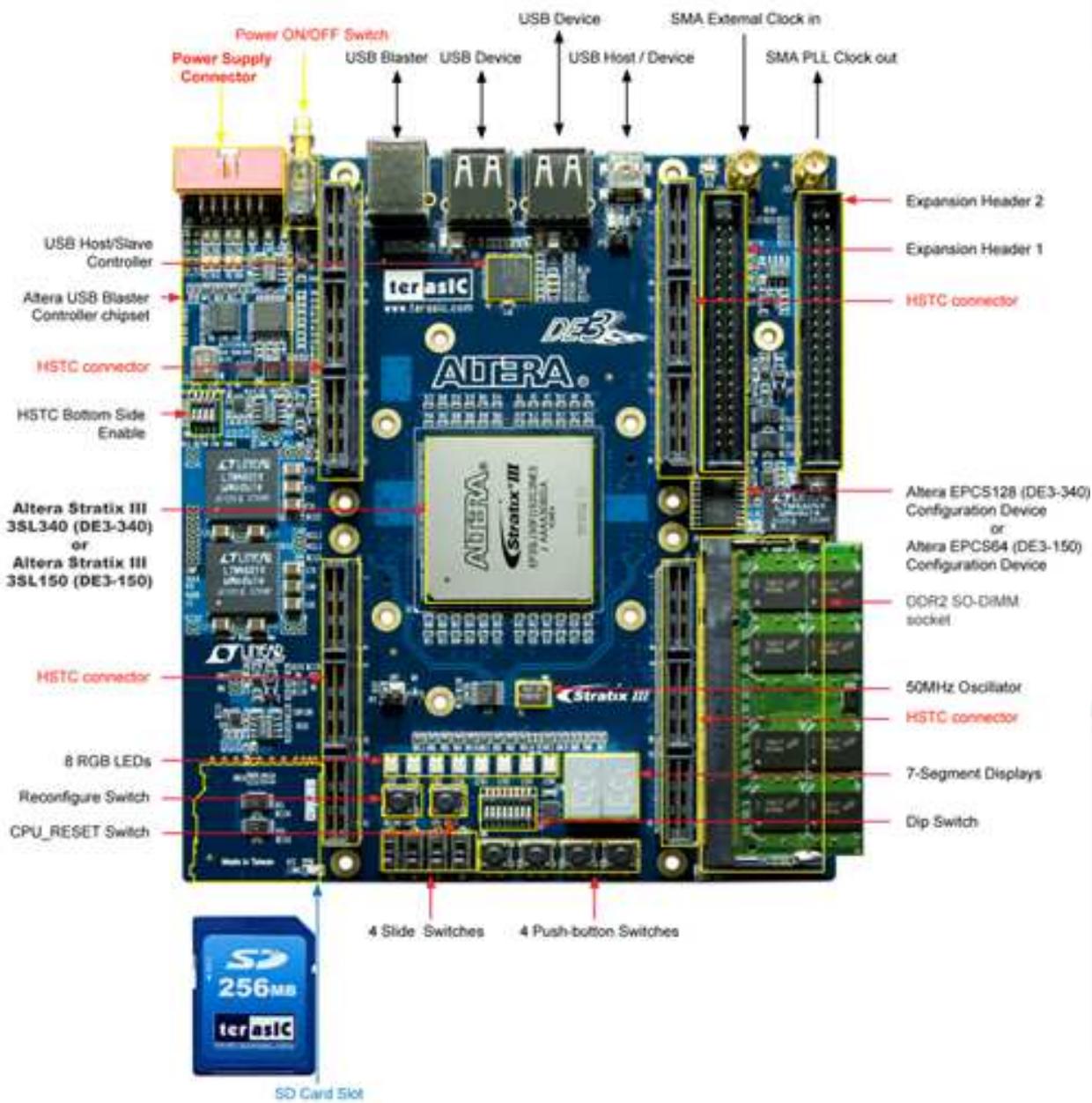
請立即投票

CIII Daughter Board

- 4.3" 800x480 LCD
- With Touch Panel
- Ethernet PHY
- 24-bit Audio Codec
- Digital TV Composite Input
- 10-bit XSGA Output
- RS-232 Port
- PS/2 Port
- SD/MMC Socket

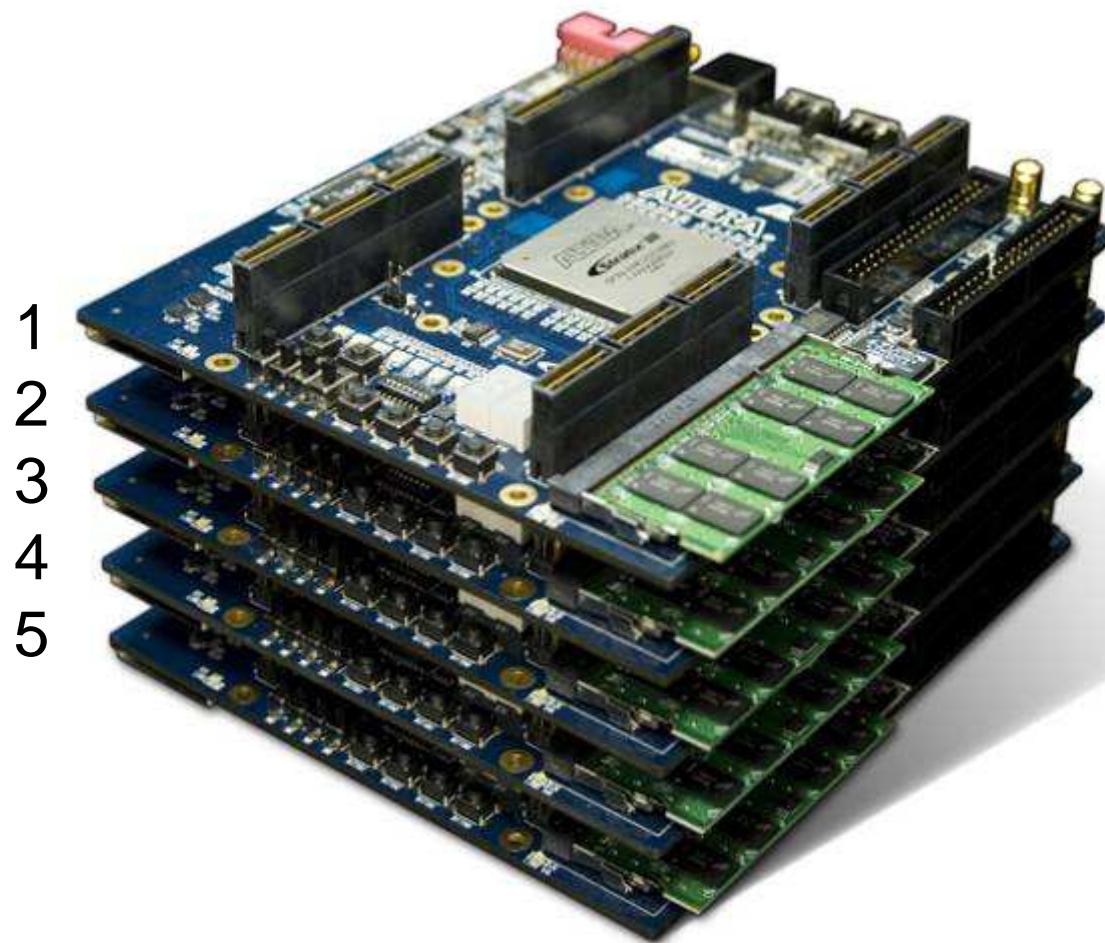
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The DE3 Board



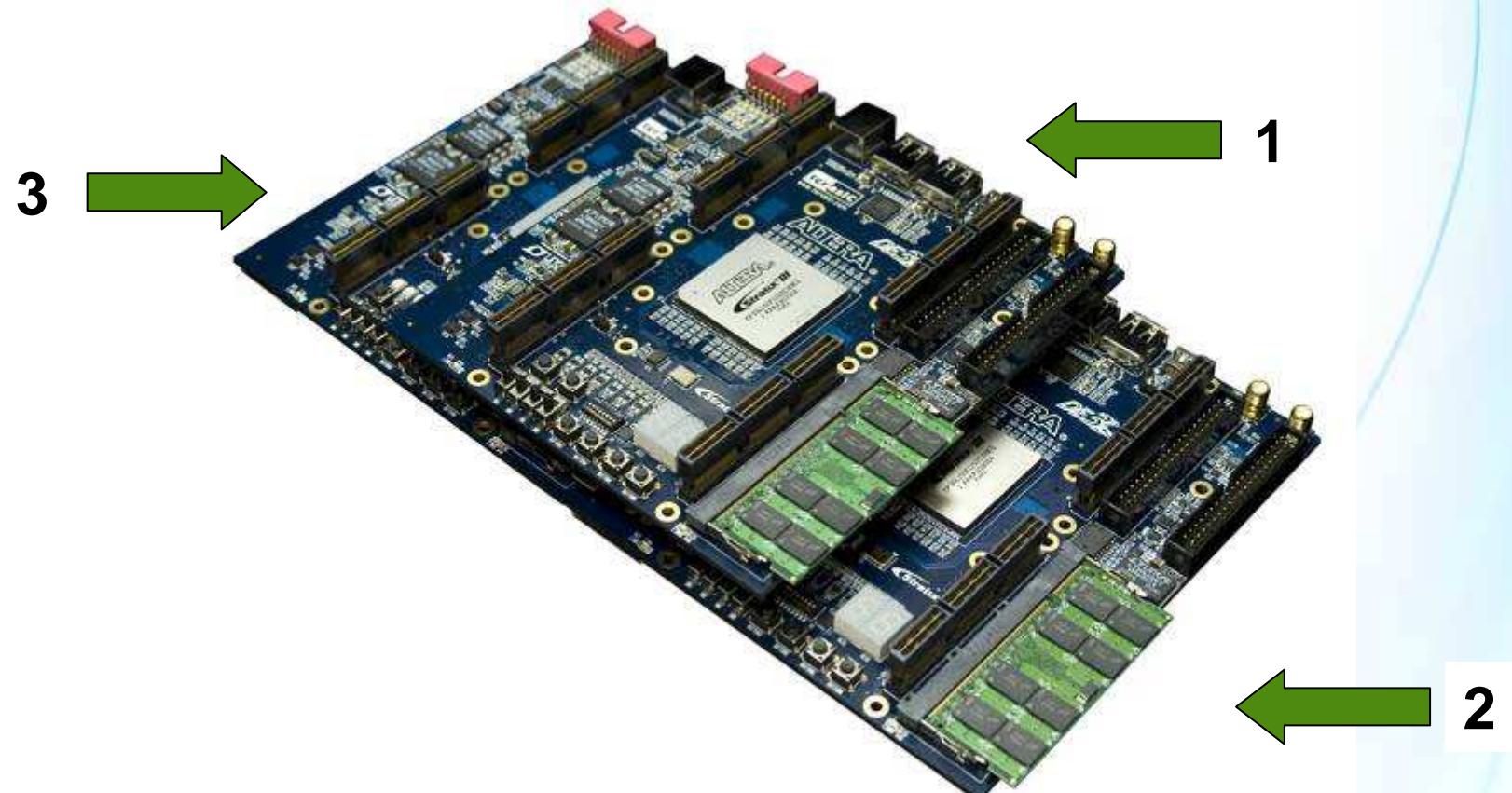
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Stackable Mechanism (240 LVDS pairs – 1Gbps)



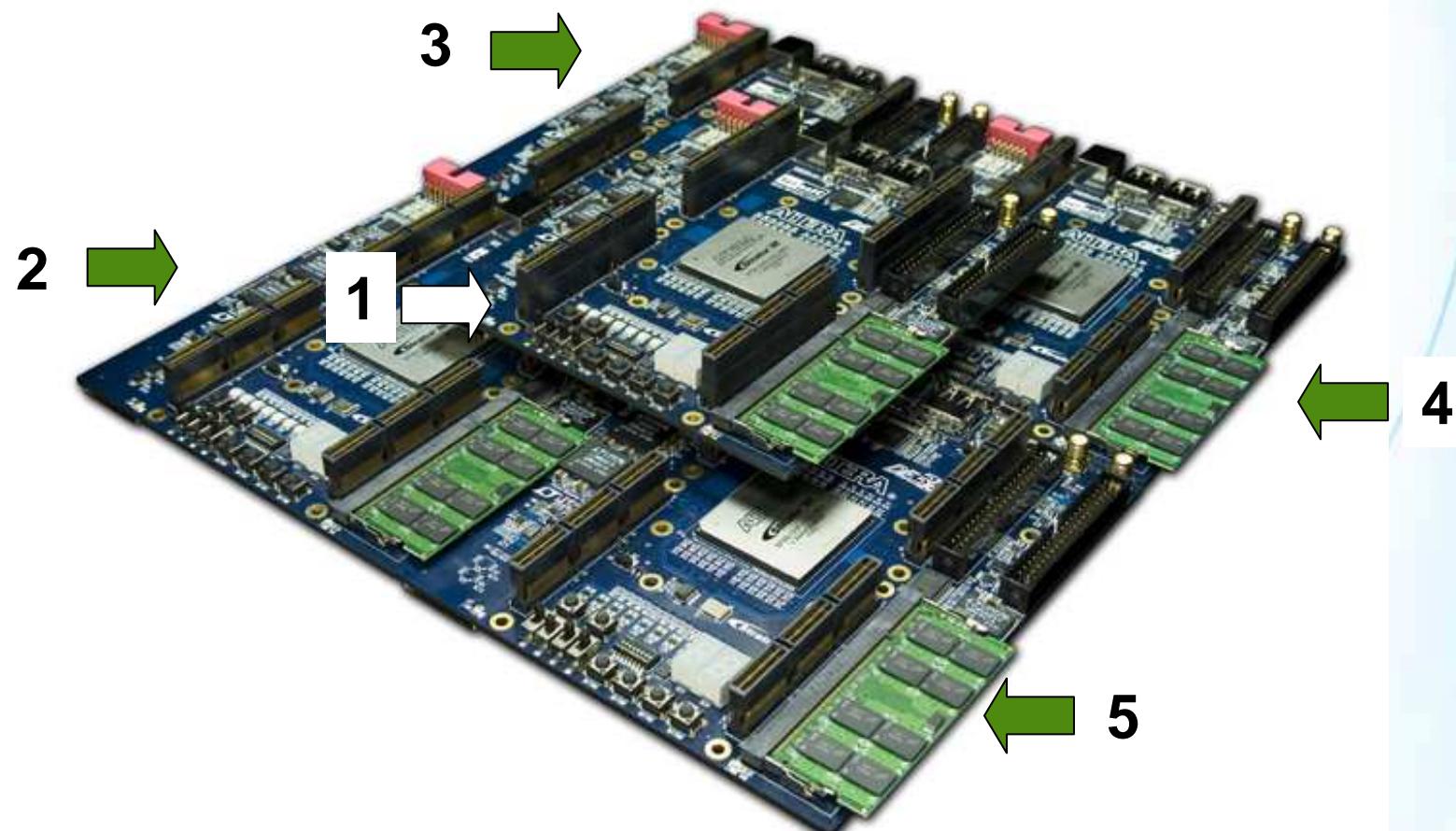
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Many ways to assemble DE3 boards into a big system (3 DE3 boards in this case)



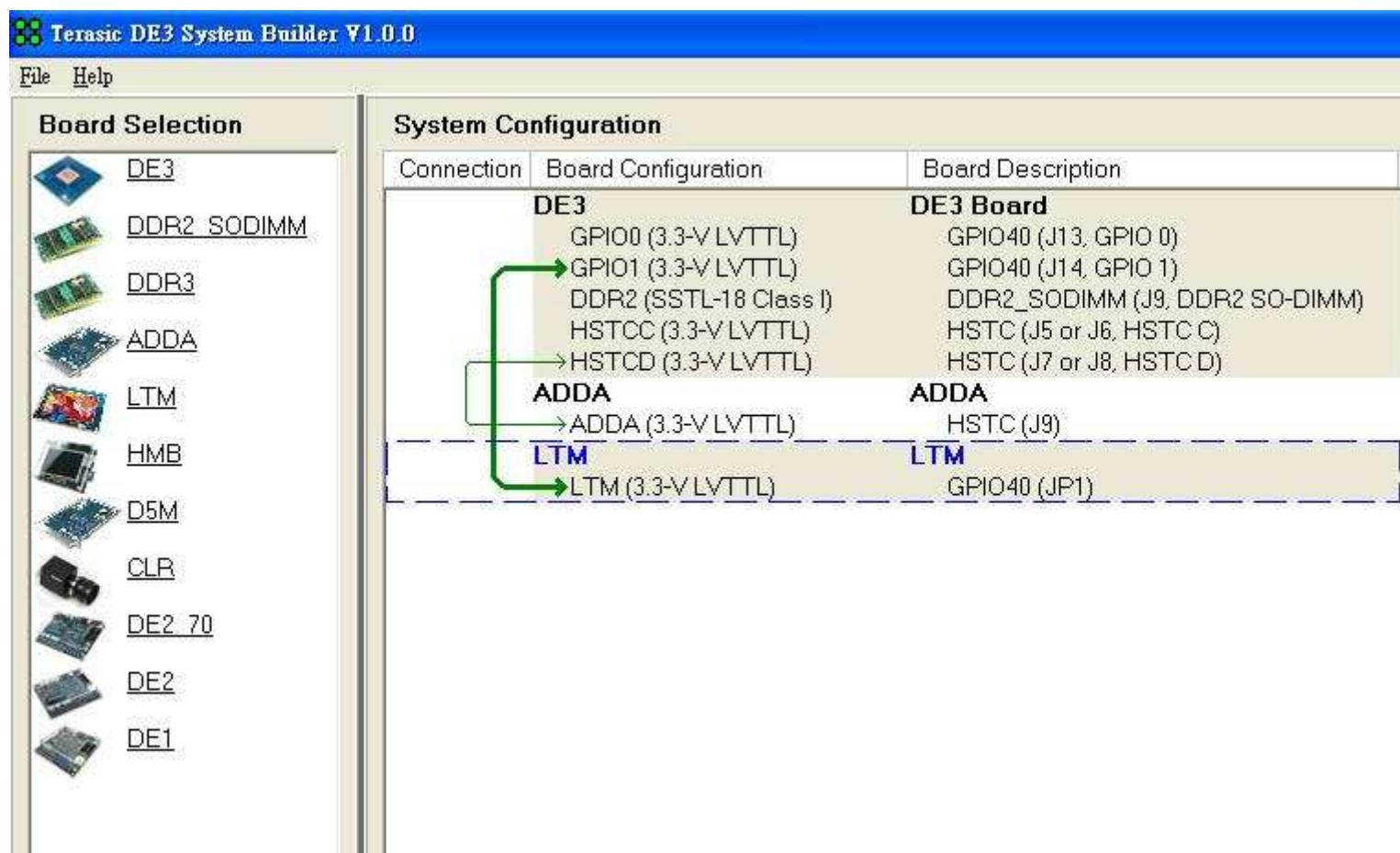
ALTERA

Many ways to assemble DE3 boards into a big system (5 DE3 boards in this case)



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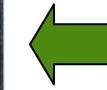
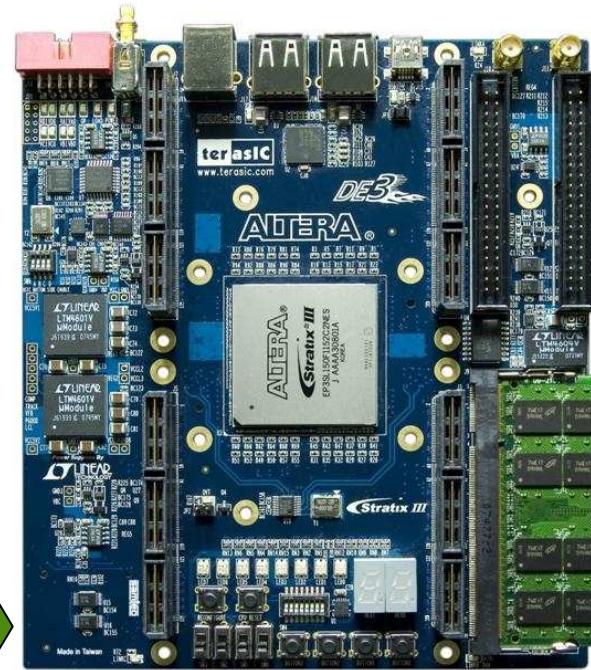
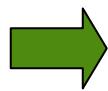
DE3 System Builder – generate Top-level project and configure bank/Connector IO Voltage using a friendly GUI (simply connect various boards using click and drag)



Many Daughter Boards Ready for DE3 (1/2)



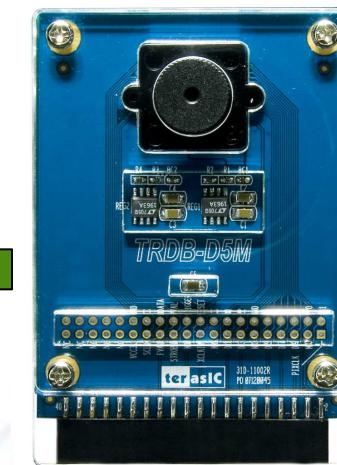
AD/DA



LTM



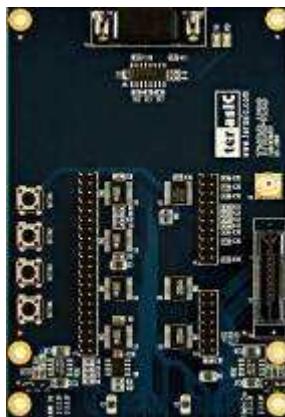
HMB (NEEK)



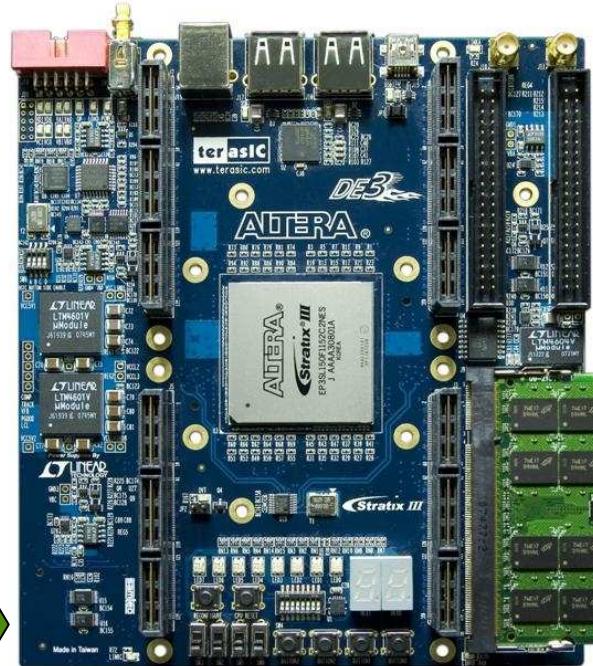
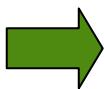
D5M

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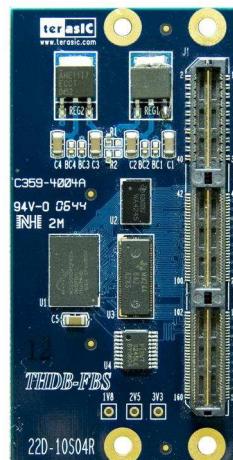
Many Daughter Boards Ready for DE3 (2/2)



H2S(HSMC to SC)



Camera Link/CCD



Flash Daughter Card

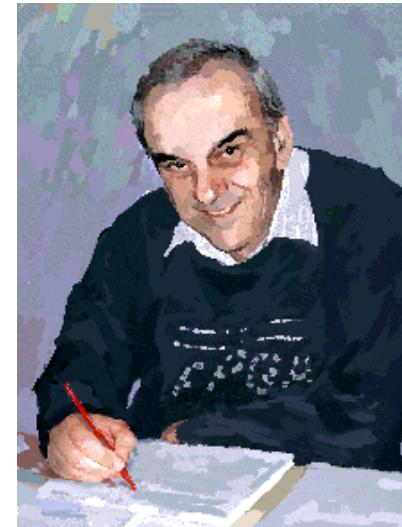


DDR3

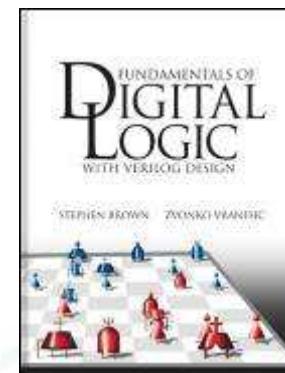
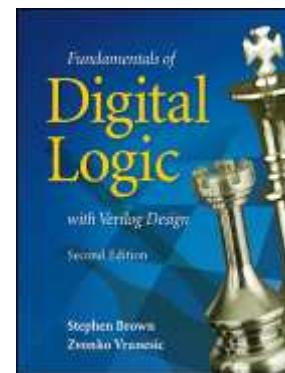
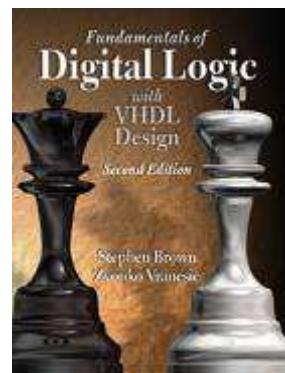
Altera 教授級顧問提供全球統一同步教材



Dr. Stephen Brown



Dr. Zvonko Vranesic



ALTERA.

Altera 教授級顧問提供全球統一同步教材

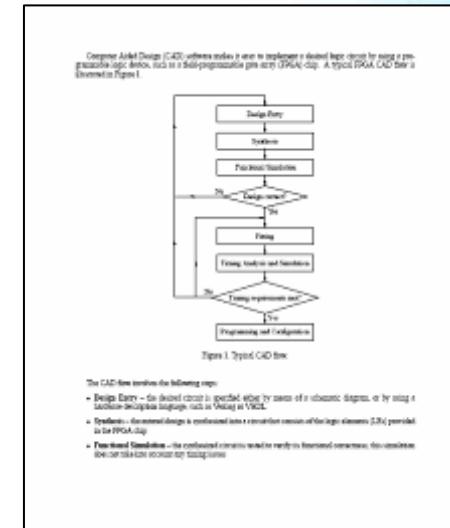
■ Tutorials

- Introduction to Quartus II ✓
- Getting Started with Altera Lab Boards ✓
- Quartus II Simulation ✓
- Using LPMs ✓
- Timing Considerations ✓
- Using Nios II and SOPC Builder (2006)

■ Ready-to-Teach Lab Experiments

- Lab experiments for Digital Logic ✓
- Lab experiments for Embedded Systems (2006)

Introduction to Quartus II



Altera 教授級顧問提供全球統一同步教材

- Ten lab exercises released on the web
 - From basic logic gates to simple processors

Laboratory Exercise 10

In Laboratory Exercise 9 we described a simple processor. In Part I of that exercise the processor itself was designed, and in Part II the processor was connected to an external counter and a memory unit. This exercise describes subsequent parts of the processor design. Note that the numbering of figures and tables in this exercise are continued from those in Parts I and II in the preceding lab exercise.

Part III

In this part you will extend the capability of the processor so that the external counter is no longer needed, and so that the processor has the ability to perform read and write operations using memory or other devices. You will add three new types of instructions to the processor, as displayed in Table 3. The **ld** (load) instruction loads data into register RX from the external memory address specified in register RY. The **st** (store) instruction stores the data contained in register RX into the memory address found in RY. Finally, the instruction **mvnz** (move if not zero) allows a **mv** operation to be executed only under a certain condition; the condition is that the current contents of register G are not equal to 0.

Operation	Function performed
ld Rx,[Ry]	$Rx \leftarrow [Ry]$
st Rx,[Ry]	$[Ry] \leftarrow Rx$
mvnz Rx,Ry	If $G \neq 0$, $Rx \leftarrow [Ry]$

Table 3. New instructions performed in the processor

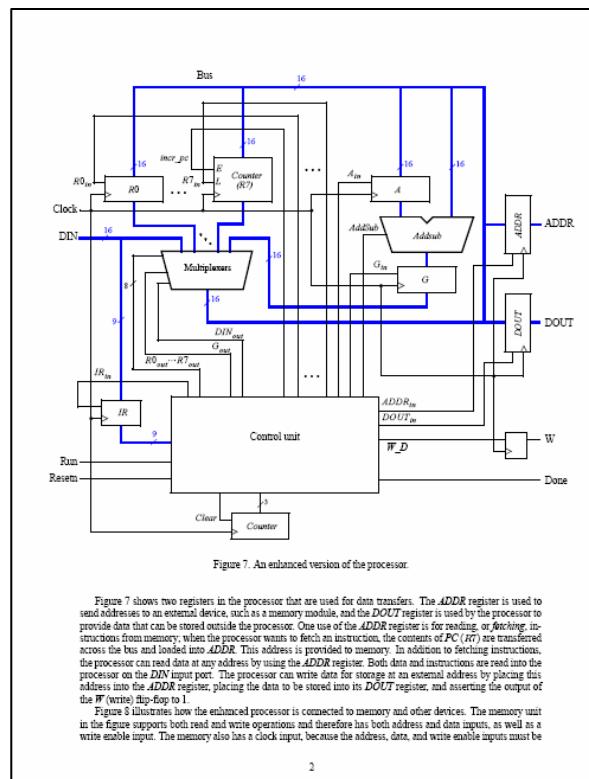
A schematic of the enhanced processor is given in Figure 7. In this figure, registers R0 to R8 are the same as in Figure 1 of Laboratory Exercise 9, but register RT has been changed to a counter. This counter is used to provide the addresses in the memory from which the processor's instructions are read; in the preceding lab exercise, a counter external to the processor was used for this purpose. We will refer to RT as the processor's program counter (PC), because this terminology is common for real processors available in the industry. When the processor is reset, PC is set to address 0. At the start of each instruction (in time step 0) the contents of PC are used as an address to read an instruction from the memory. The instruction is stored in IR and the PC is automatically incremented to point to the next instruction (in the case of **mv** the PC provides the address of the memory data to be copied against).

The processor's counter must increment PC by using the **inc_pc** signal, which is just an enable on this counter. It is also possible to directly load an address into PC (RT) by having the processor execute a **mv** or **mvz** instruction in which the destination register is specified as RT. In this case the control unit uses the signal $R7_m$ to perform a parallel load of the counter. In this way, the processor can execute instructions at any address in memory, as opposed to only being able to execute instructions that are stored in successive addresses. Similarly, the current contents of PC can be copied into another register by using a **mv** instruction. An example of code that uses the PC register to implement a loop is shown below, where the text after the % on each line is just a comment. The instruction **mv R7,R7** places the IR into the address in memory of the instruction sub R4,R2. Then, the instruction **mvnz R7,R5** causes the sub instruction to be executed repeatedly until R4 becomes 0. This type of loop could be used in a larger program as a way of creating a delay.

```

mv R2,#1
mv R4:#10000000 % binary delay value
mv R5,%              % save address of next instruction
sub R4,R2             % decrement delay count
mvnz R7,R5            % continue subtracting until delay count gets to 0

```



以 NIOS II 為主的嵌入式系統教學教材

■ Embedded Systems

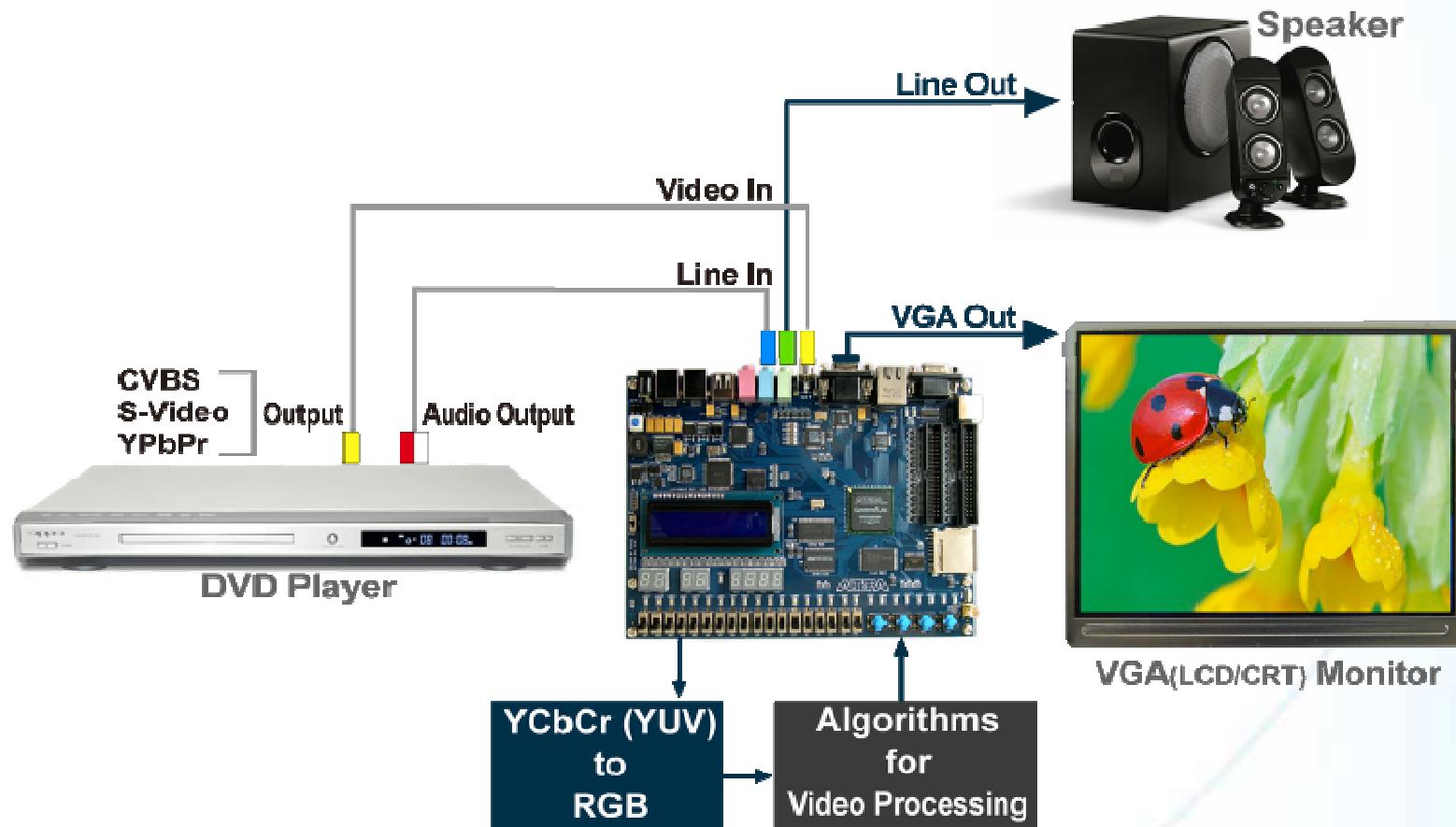
- Nios II ISA tutorial
- Nios II Monitor Program
 - Easy-to-use debugging environment
- SOPC Builder tutorial
 - Need SOPC Builder components for all DE2 devices, and need DE2 board description component
- Nios II software development tutorial
 - SOPC Builder and Nios II program examples
- University Program IPs

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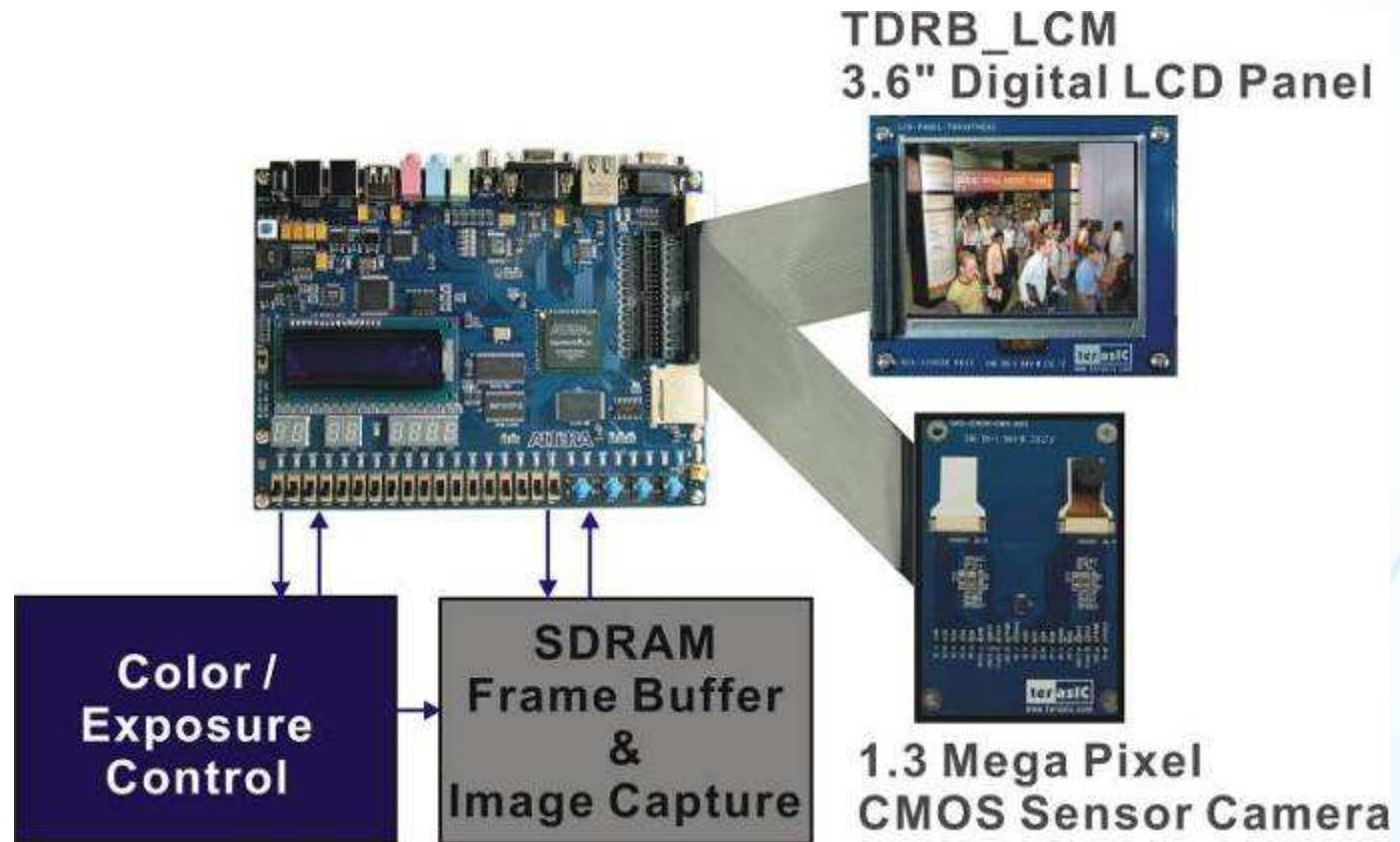
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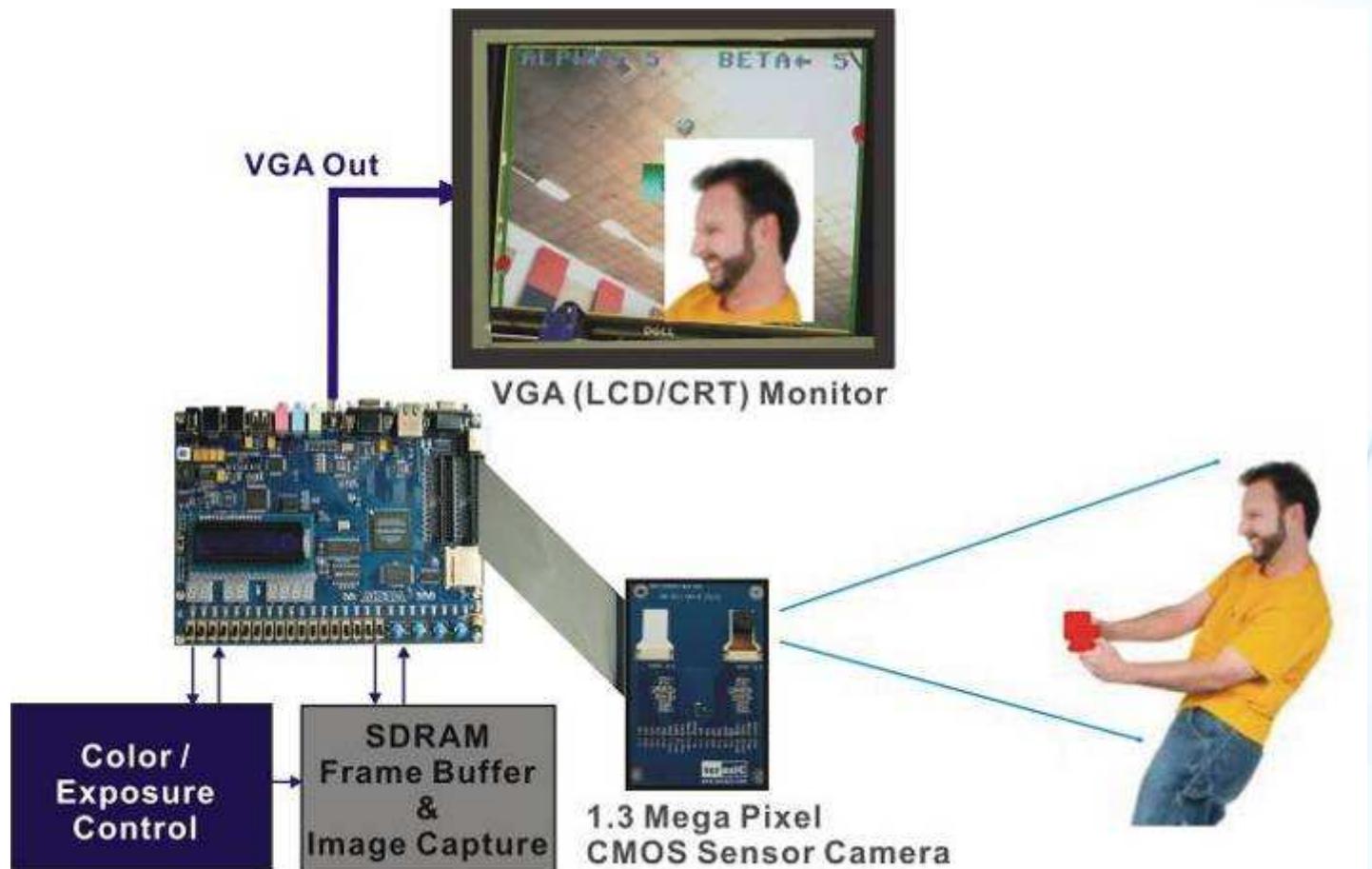
DTV Solution using Altera DE2



1.3 Mega Pixel Digital Camera with 3.6" Digital Panel

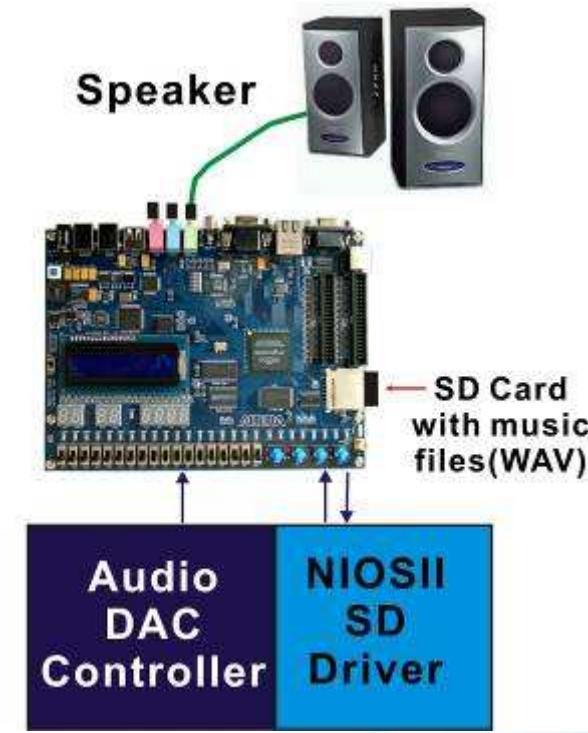
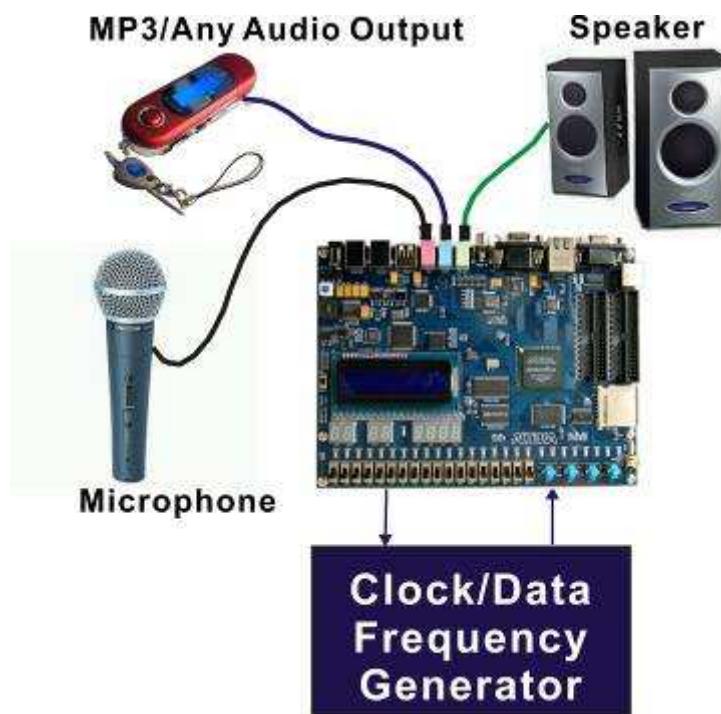


Digital Camera + Color/Motion Recognition (Pong Game)



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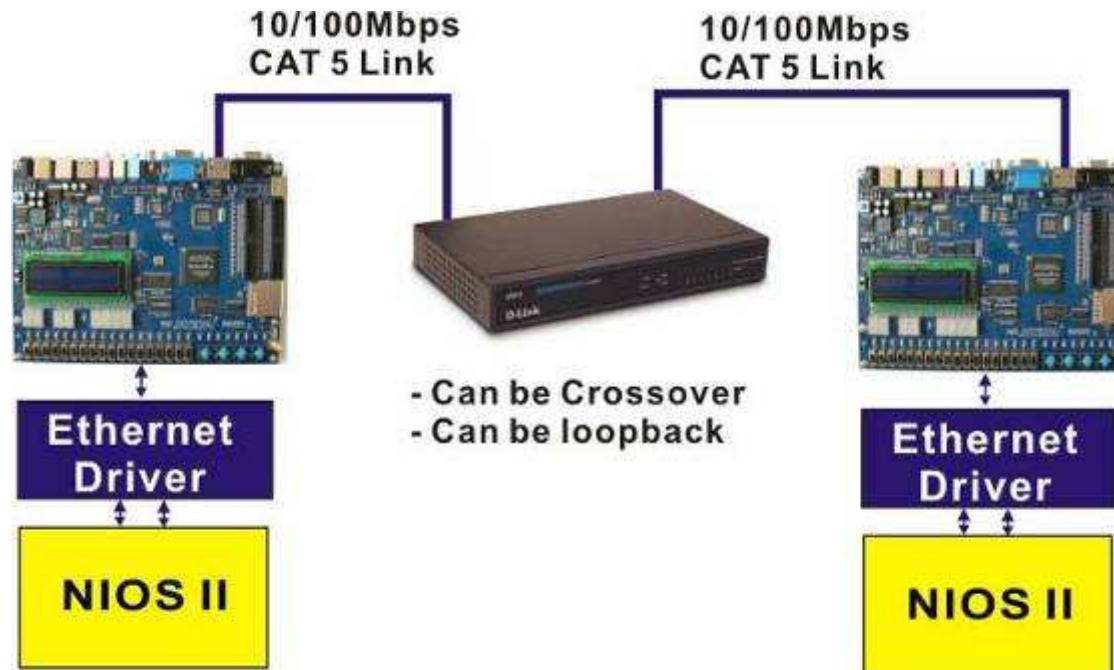
SD Card Music Player (File System Provided)



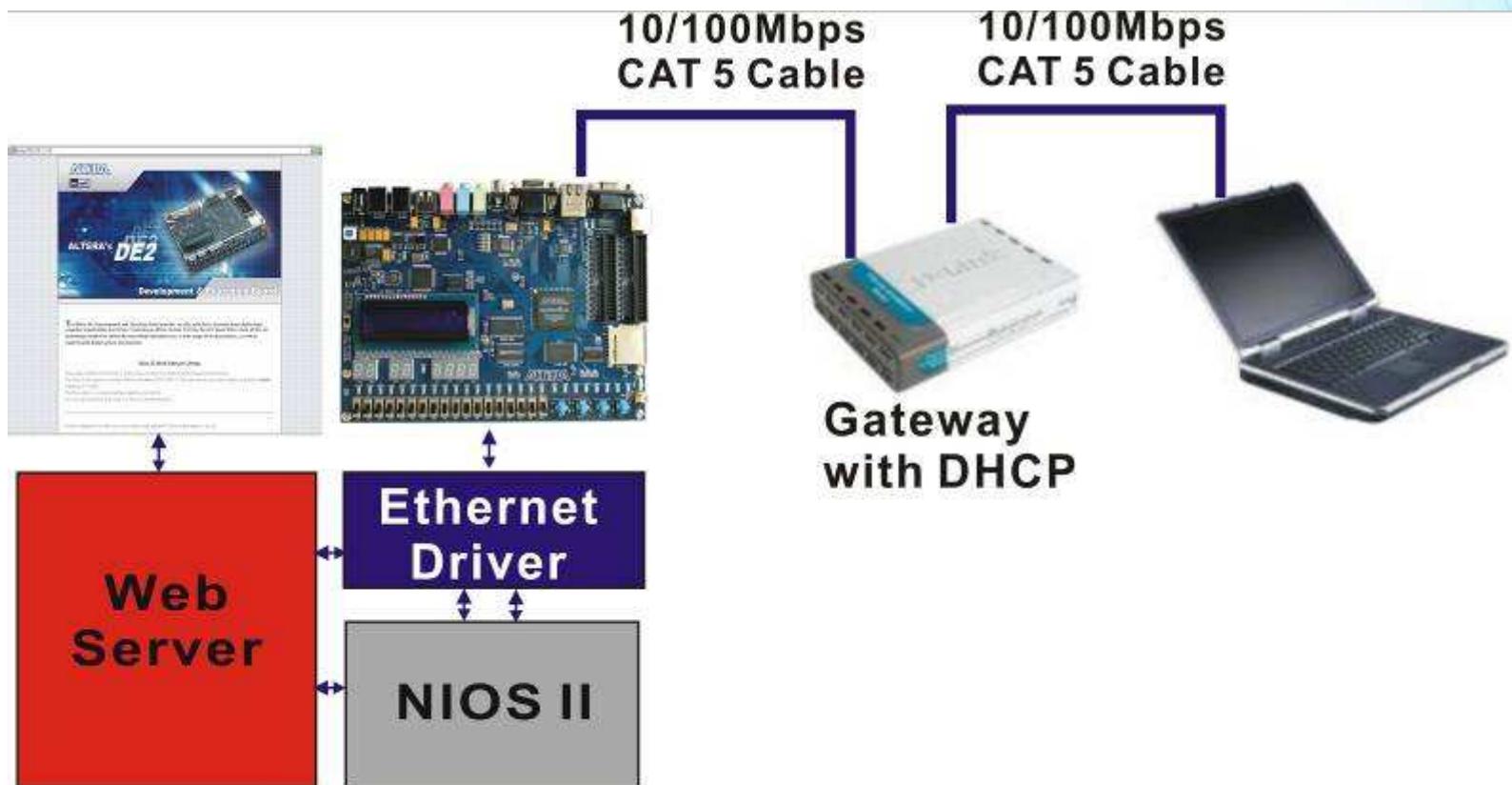
Ethernet Packets TX/RX with NIOS II Core

Key Components Used in the Lab:

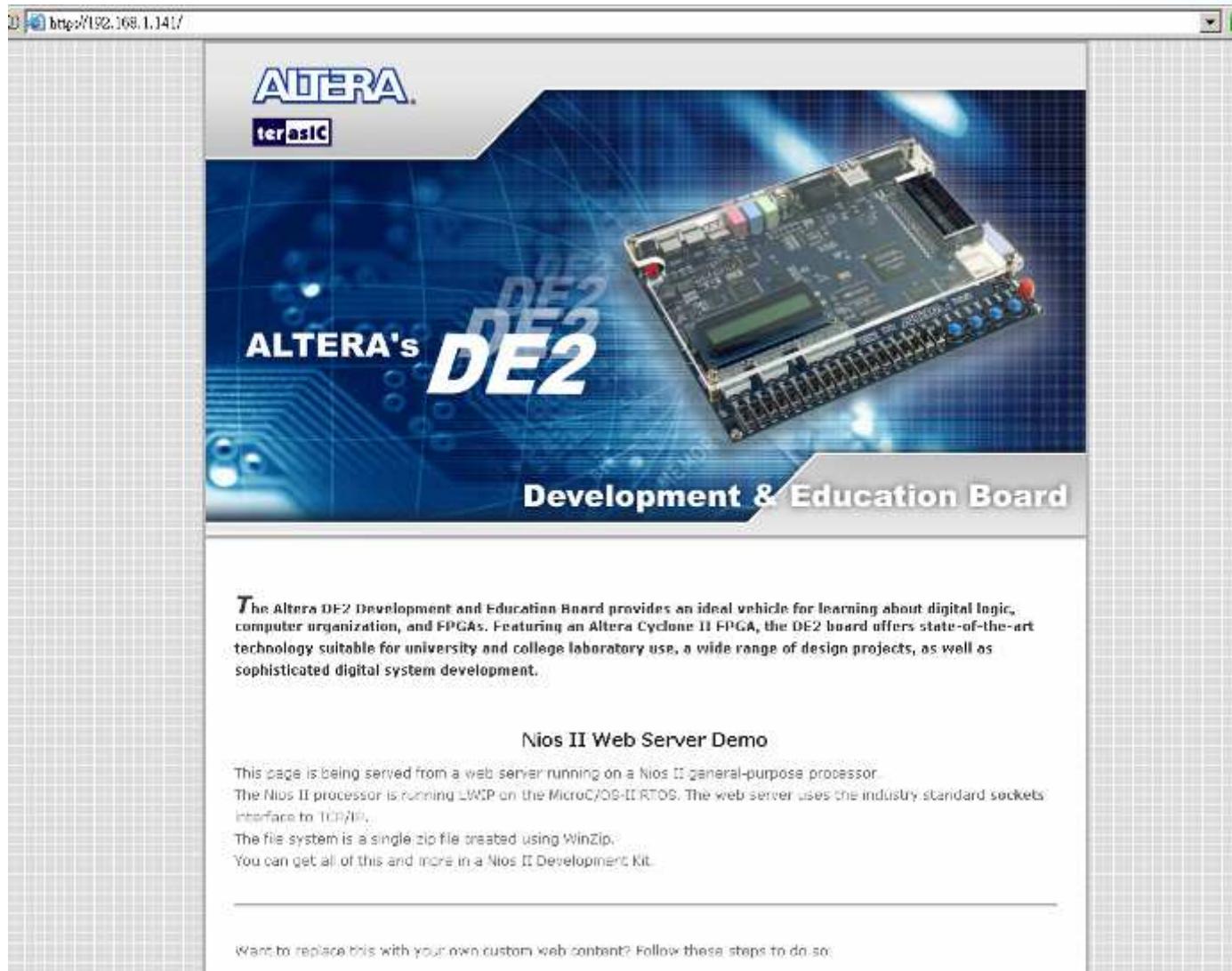
- SDRAM (NIOSII code)
- Davicom 9000a Ethernet Controller



Web Server Using DE2

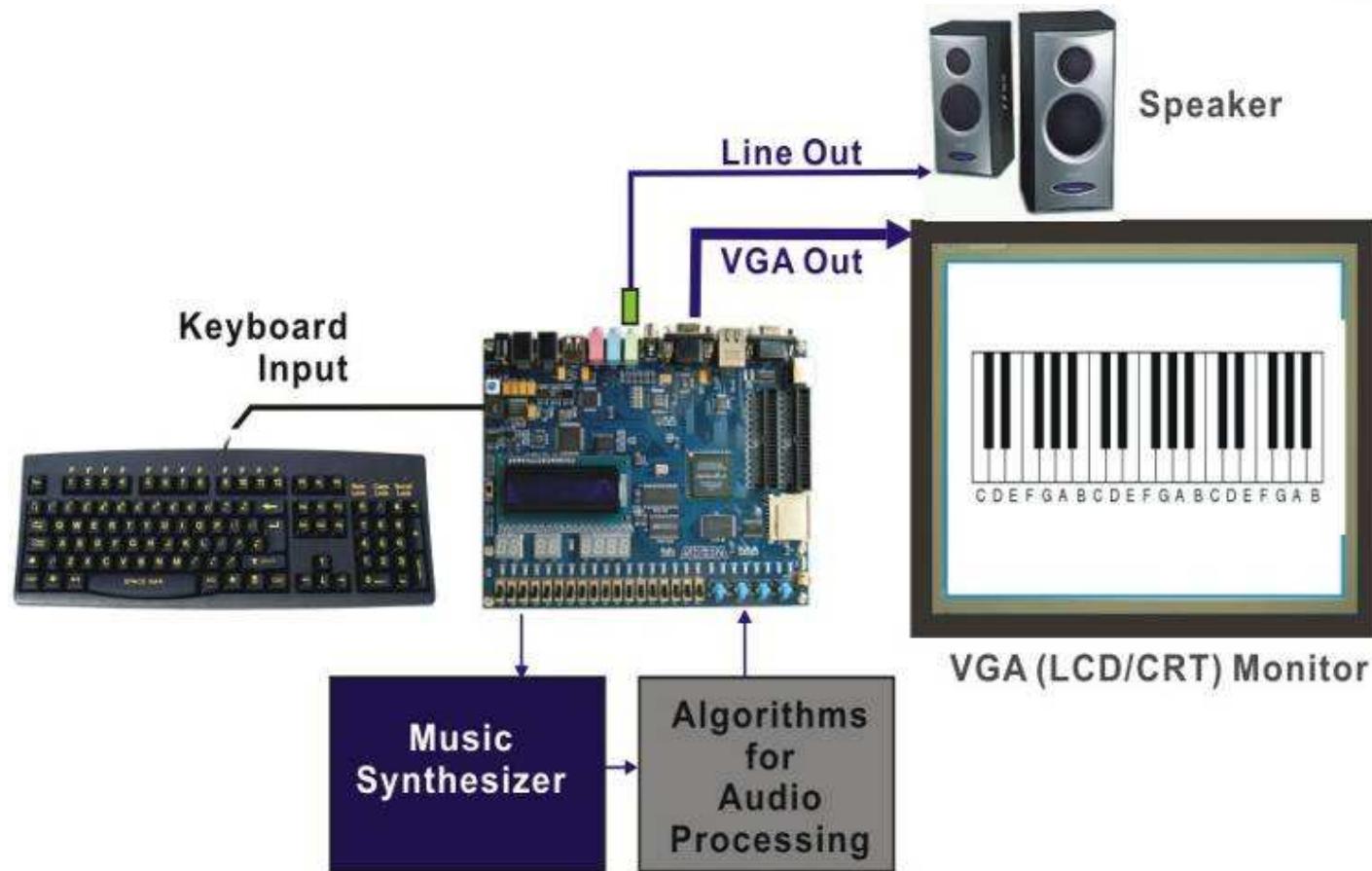


WebPage Content Limitation: 4Mbyte



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CD-Quality CASIO Keyboard (High-end Music Synthesizer)



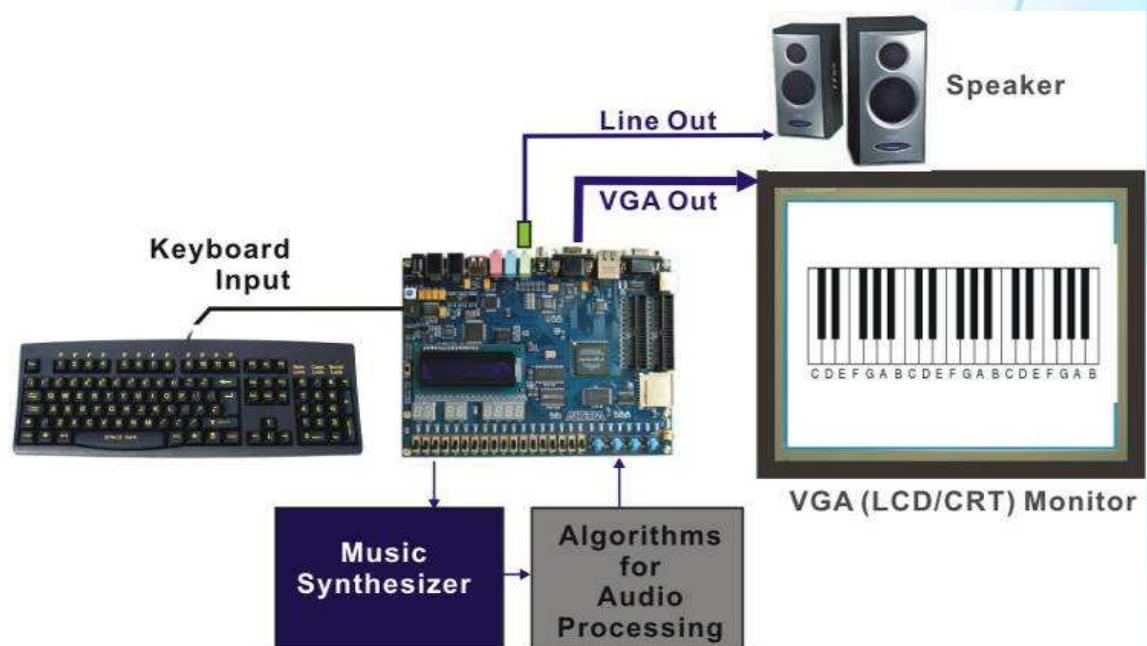
目標：
全球名校教學及研究平台使用共同語言

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University of Michigan (Ann Arbor)

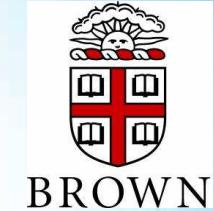


- Introduction to Computer
- Audio Processing
- Music Synthesizer Algorithm



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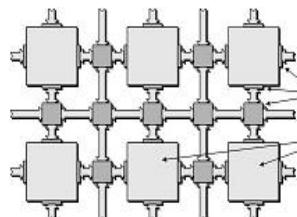
Brown University



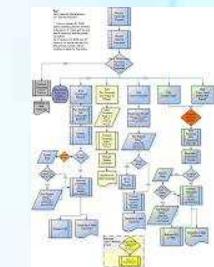
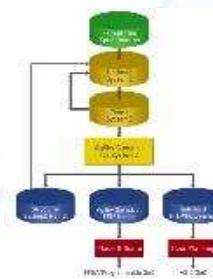
■ EN2911X 可重組化計算 (Fall 2007)

<http://ic.engin.brown.edu/classes/EN2911XF07/>

- ✓ Introduction
- ✓ RC principles: Programmable logic technology
- ✓ Verilog: A hardware definition language
- ✓ RC principles: Software
- ✓ SystemC: A system description language
- ✓ Application-driven hardware acceleration using RC



```
module mux(out, i0, i1, i2, i3, s1, s0);
output out;
input i0, i1, i2, i3;
input s1, s0;
assign out = (s1 & ~s0 & i0) |
           (~s1 & s0 & i1) |
           (s1 & s0 & i2) |
           (~s1 & ~s0 & i3);
// OR THIS WAY
assign out = s1 ? (s0 ? i3:i2) : (s0 ? i1:i0);
endmodule
```



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■ CSEE 4840 嵌入式系統設計課程

<http://www1.cs.columbia.edu/~sedwards/classes/2007/4840/index.html>

- ✓ A microprocessor-based embedded system
- ✓ A combination of C and the VHDL hardware description language

■ CSEE 4840 期末專題報告

<http://www1.cs.columbia.edu/~sedwards/classes/2007/4840/highlights.html>



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Cornell University



Cornell University

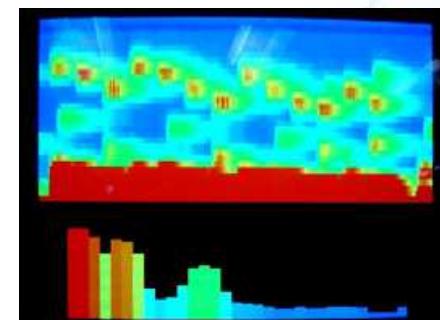
- **ECE 576 Advanced Microcontroller Systems on a Programmable Chip (Fall 2007)**

<http://instruct1.cit.cornell.edu/courses/ece576/>

- ✓ SRAM state machine. One-dimensional cellular automaton
- ✓ NiosII based, VGA video interface
- ✓ NiosII and MicroC/OS audio signal generator
- ✓ NiosII and Digital Differential Analyzer

- **Final Projects:**

<http://instruct1.cit.cornell.edu/courses/ece576/FinalProjects/>

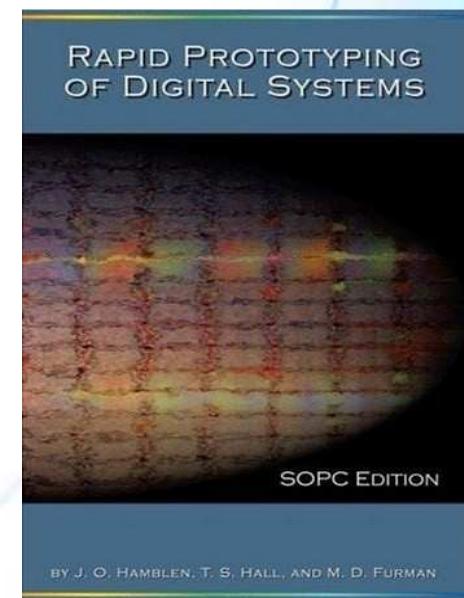
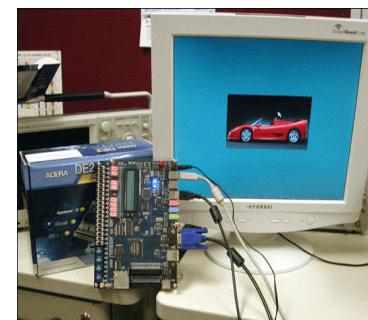


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Georgia Institute of Technology

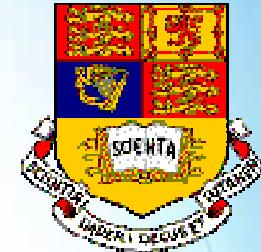
Georgia
Tech

- ECE 2031 Digital Design Laboratory
<http://users.ece.gatech.edu/~hamblen/DE2/>
- Rapid Prototyping of Digital Systems (DE2)
- Book available on Amazon on Sept, 2007
Rapid Prototyping of Digital Systems SOPC Edition
- Running the uClinux example



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Imperial College London



■ EE3 & ISE3 數位系統設計

http://www.ee.ic.ac.uk/pcheung/teaching/ee3_DSD/index.html

- ✓ How to go about designing complex, high speed digital systems
- ✓ How to use some of the modern CAD tools
- ✓ How to implement such designs using programmable logic
- ✓ 用 ALTERA 現有在 DE1/DE2 的邏輯電路與 SOPC的 Lab

<http://university.altera.com/materials/unv-lab-manual.html>

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McMaster University

■ COE3DQ4數位系統設計<http://www.ece.mcmaster.ca/~nicola/3dq4/>

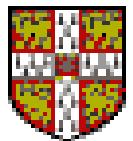
- ✓ Hardware Description Languages
- ✓ Programmable Logic Devices
- ✓ Design Synthesis using (System)Verilog
- ✓ Project - Hardware Implementation of an Image Decompressor for MP3 audio and MPEG2 audio/video decoders

■ ECE480/580 數位系統設計課程

<http://jjackson.eng.ua.edu/courses/ece480/>

- ✓ Hardware description language -Design a system, component(SSI,MSI), or processor
- ✓ Design of digital I/O interfaces possibly including parallel, serial, USB, IEEE1394 (firewire), SPI and I2C
- ✓ Design of a microprocessor
- ✓ System-on-chip (SOC) design
- ✓ NIOS II C Application – Displays a digital clock on the LCD display and Green LEDs 0.1HZ

- **Introduction to Microcomputers**
 - <http://courses.ece.ubc.ca/259/>
- Lecture notes and photographs
- Altera software install guide (DE2/DE1)
- Nios II tutorial and documentation(DE2/DE1)
- Nios II example code (DE2/DE1)
- **Homework(DE2/DE1)**



- Computer Laboratory & ECAD and Architecture Practical Classes
<http://www.cl.cam.ac.uk/teaching/0708/ECAD+Arch/>

- System-on-a-chip (SOC)
- Application Specific Instruction set Processors (ASIP).
- MPEG1-Layer3 (MP3) Player
- Lab 1 Pong - Hardware & Lab 2 - Game of Life SOPC

University of Illinois at Urbana – Champaign



- **ECE 598 BL**
Design and Synthesis for SoC Research Oriented Implementation
<http://courses.ece.uiuc.edu/ece598/bl/>

- System-on-a-chip (SOC)
- Application specific instruction set processors (ASIP).
- Platform FPGA boards and digital cameras
- Implementation - MPEG1-Layer3 (MP3) Player

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University of Leeds



■ ELEC5563 SOC數位設計

http://www.personal.leeds.ac.uk/~een5sf/ELEC5563_index.html

- ✓ Introduction to real-time embedded systems using programmable digital circuits and logic
- ✓ Digital Design for System on Chip, FIR Filter, Simple Processor, More complex processor
- ✓ Project Areas suggested by ARM & PACE



University of Massachusetts Amherst



■ ECE354 計算機結構課程

<http://python.ecs.umass.edu/%7Eece354/>

- ✓ The principles of Embedded Systems.
- ✓ To develop embedded software.
- ✓ To prototype, debug and demonstrate embedded systems combining sensors, interfaces, computation, memory and networking.
- ✓ Lab – Networked Camera

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UNIVERSITY of TORONTO

- **ECE241 Digital Systems**

<http://ccnet.utoronto.ca/20069/ece241h1f/>

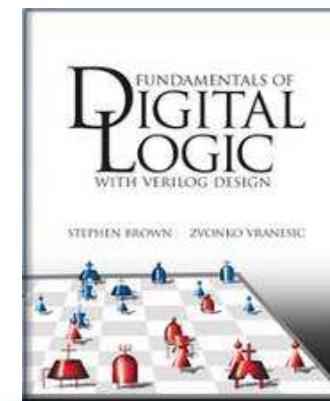
- ✓ Combinational Sequential Logic
- ✓ Complex Finite State Machines and Digital Hardware Displays

- **ECE241 Digital Systems Student Projects**

http://www.eecg.utoronto.ca/~jayar/ece241_06F/06projectvids

- Duck Shooting

- Book: Dr. Brown & Dr. Vranesic



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University of Waterloo

■ E&CE223 Digital Circuits and Systems

<http://www.ece.uwaterloo.ca/~ece223/>

- ✓ Digital Circuits – Combinational design
- ✓ A Simple Calculator
- ✓ Synchronous Sequential Design - LED DEMO

業界產品開發訓練實例

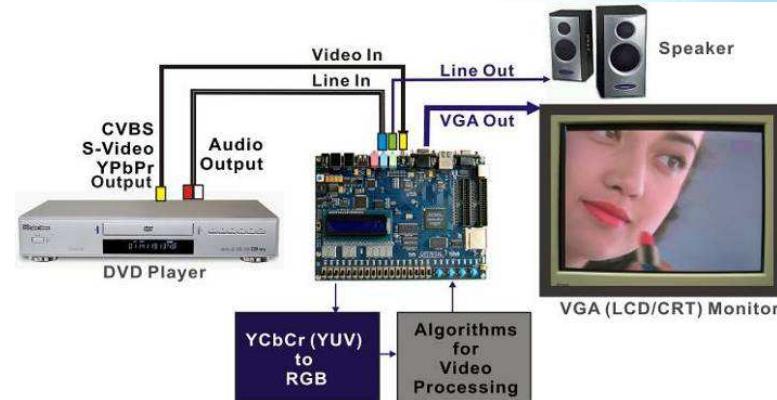
2006 / 2007 國立台灣大學電機學院為業界培訓案例

- 台灣大學電機系成立 Altera 聯合實驗室, 配有 200 套 DE2 及 20 套 TREX-S2, 及 50 套 Digital Camera/LCD 套件
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- 友晶提供師資培訓, 教材, 招生海報設計, 並授權台大使用.
- 台灣大學主辦招生, 並提供教室, 器材, 及講師.



台灣大學(台大)之聯合實驗室及專業培訓課程

- 招生期間，班班爆滿
- 學員來自業界資深研發人員
- 總共訓練約+300人 (2006)
- 平均每個課程為 30 小時



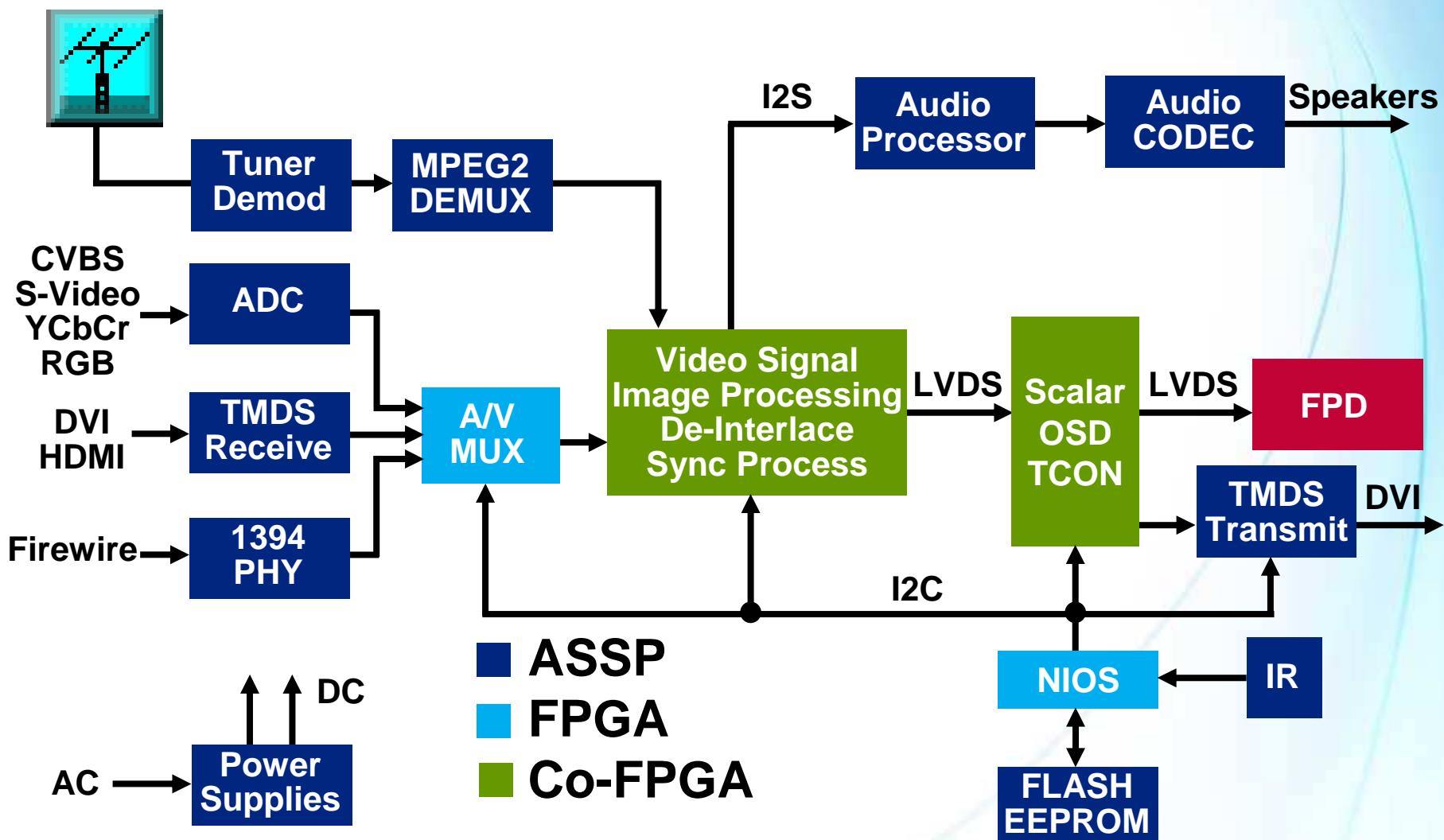
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台灣大學專業培訓課程 (機器視覺/數位相機設計 - 以 DE2 為平台)

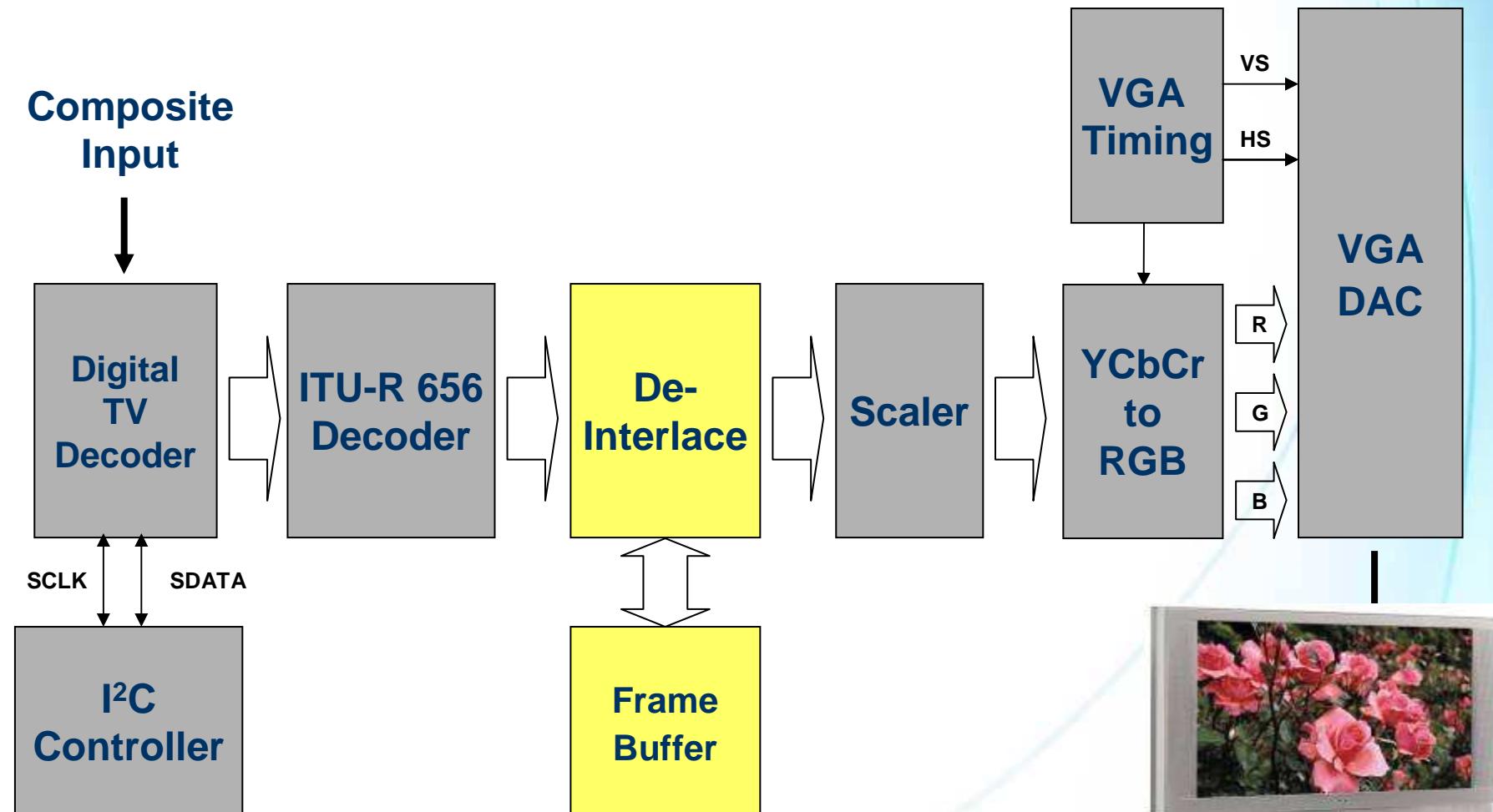


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數位電視芯片設計為實例



數位電視芯片設計 – 以 Altera DE2 平台實踐



機器視覺/數碼相機設計 – 以 **FPGA** 平台(**DE2**) 實踐

- Meet the increasingly demanded FPGA-based AOI market needs.
- Successfully create advanced FPGA-based algorithms to meet the AOI criteria for large PCB/Panel QC process.



機器視覺/數碼相機設計 – 以 **FPGA** 平台 (**DE2**) 實踐

