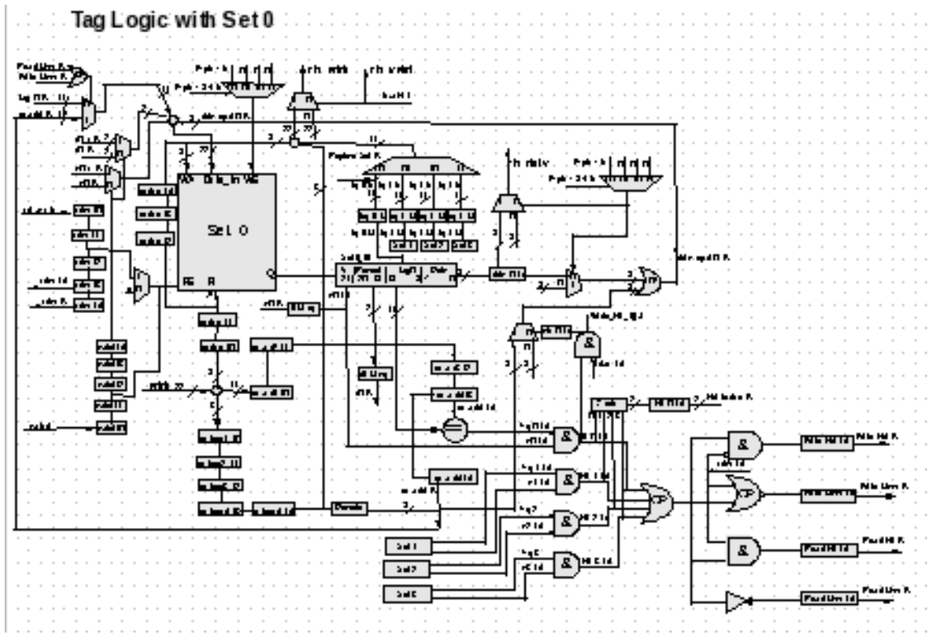
Data Cache Tag Mechanism



Designer: Todor Arnaudov
Date: 04.03.2008

Appendix to design documentation

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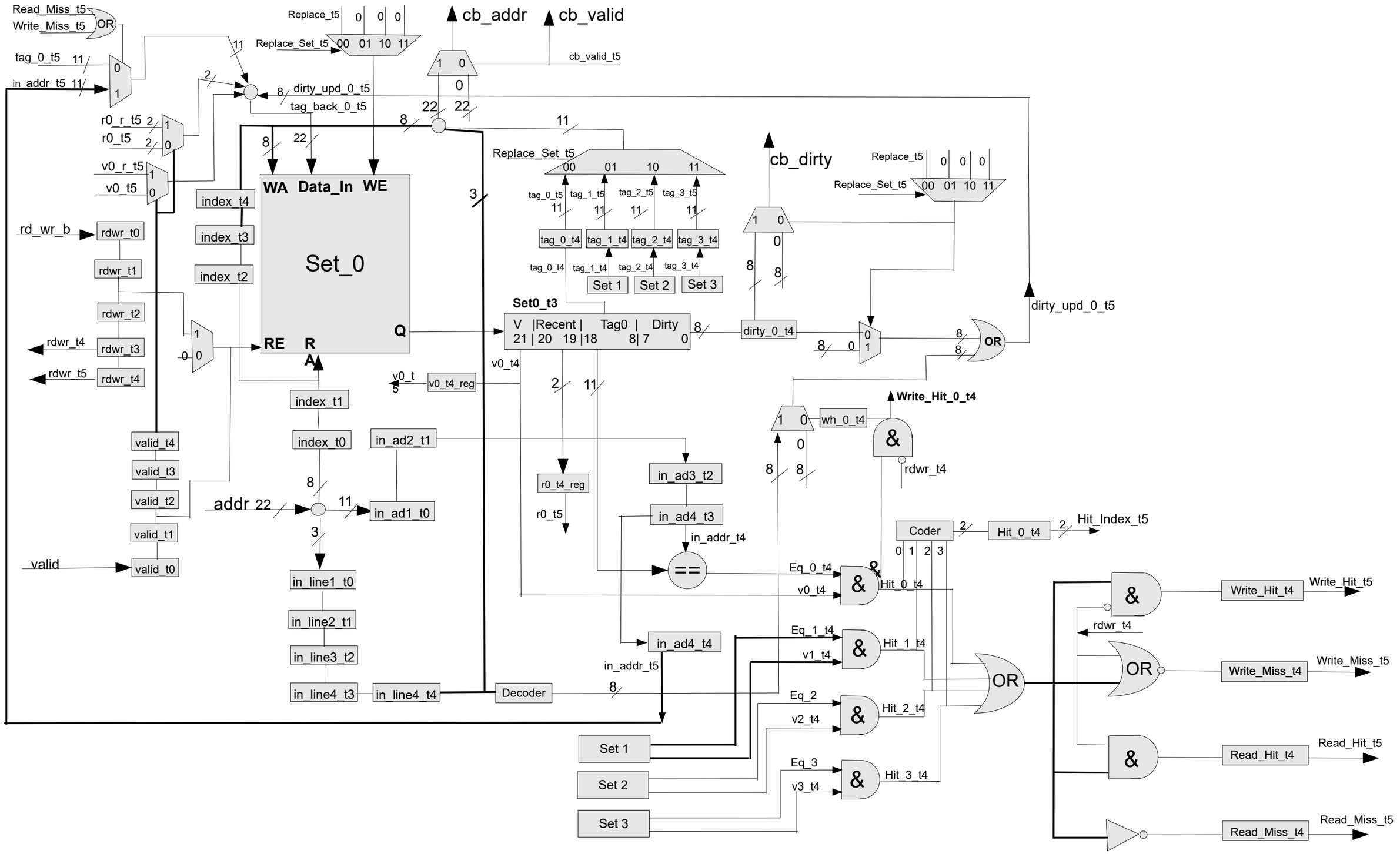
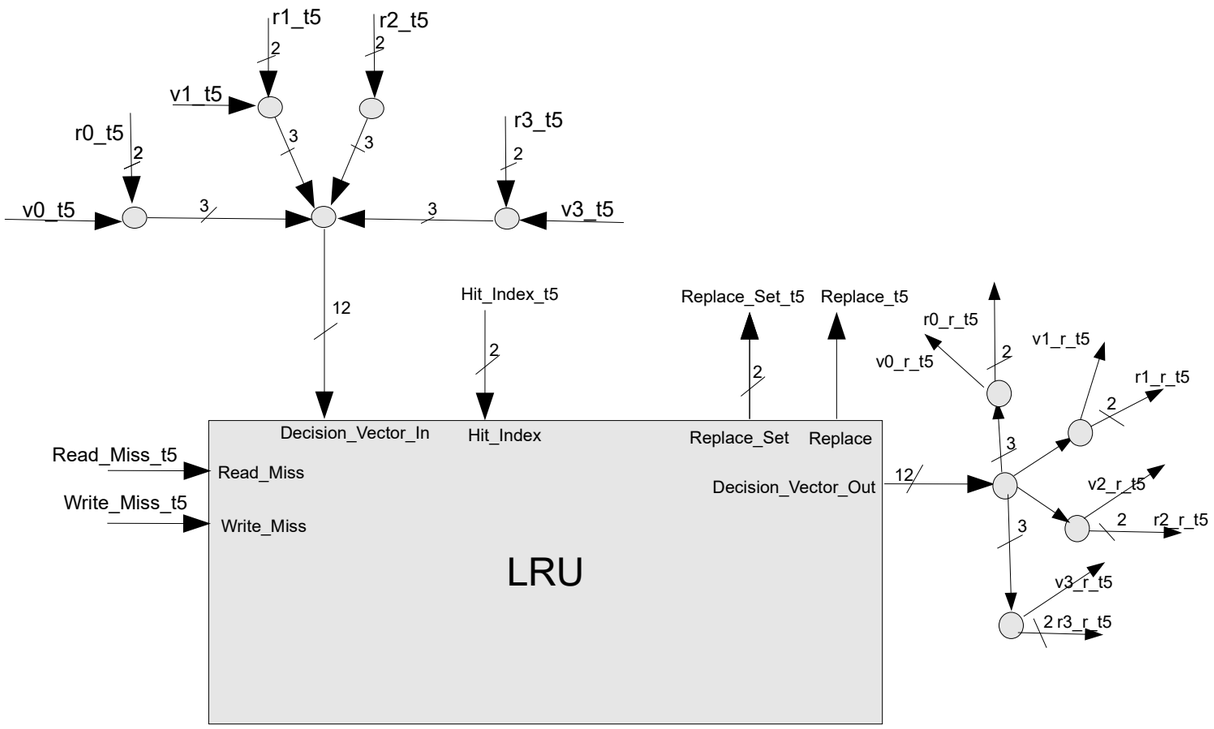
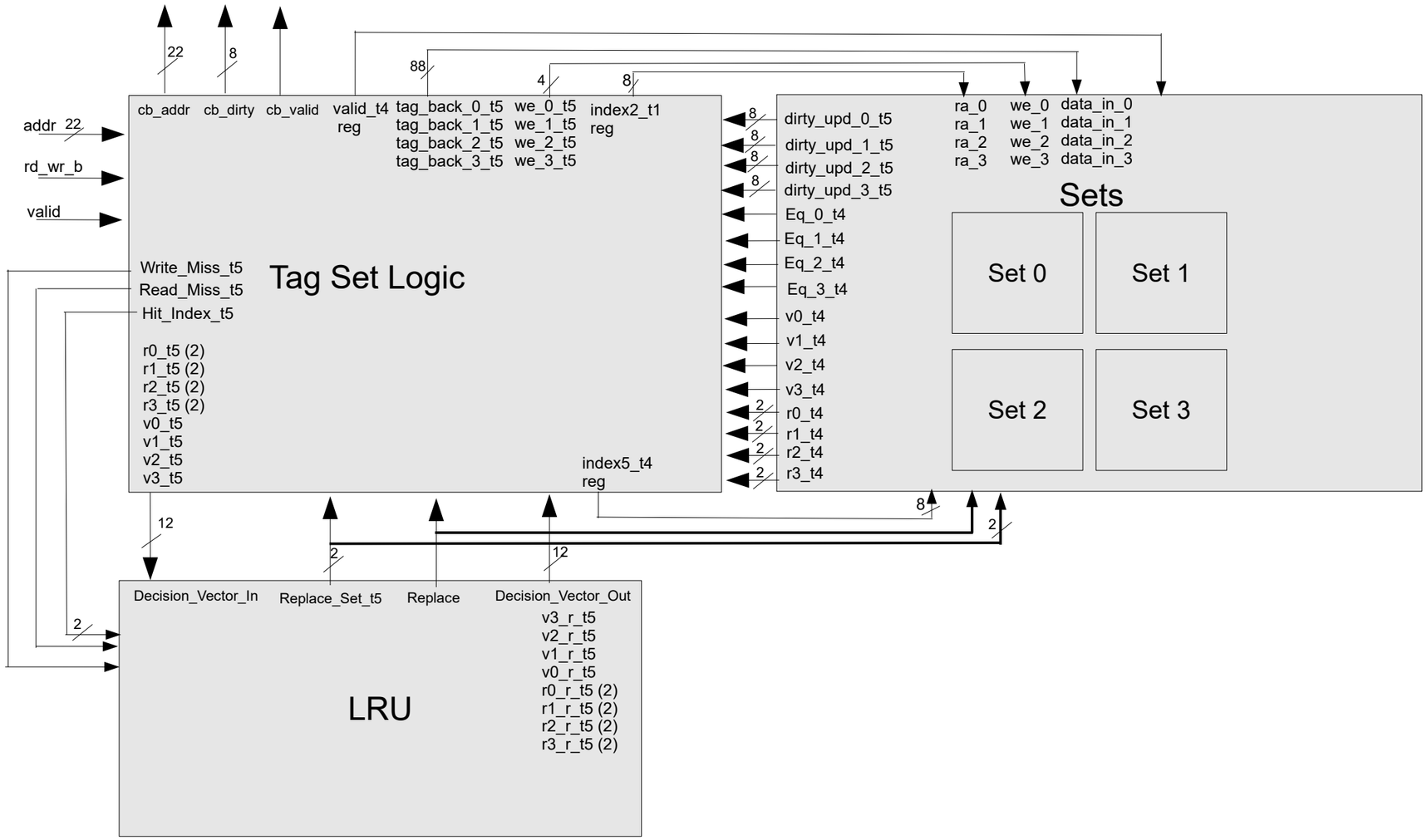
Tag Logic with Set 0



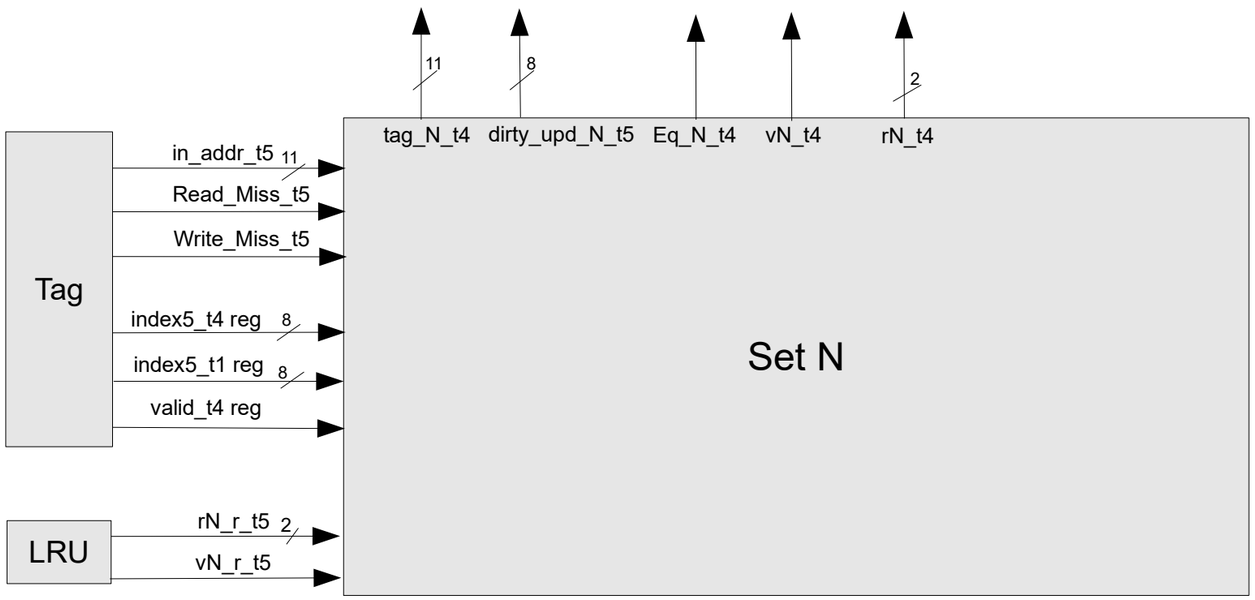
LRU Logic Interface



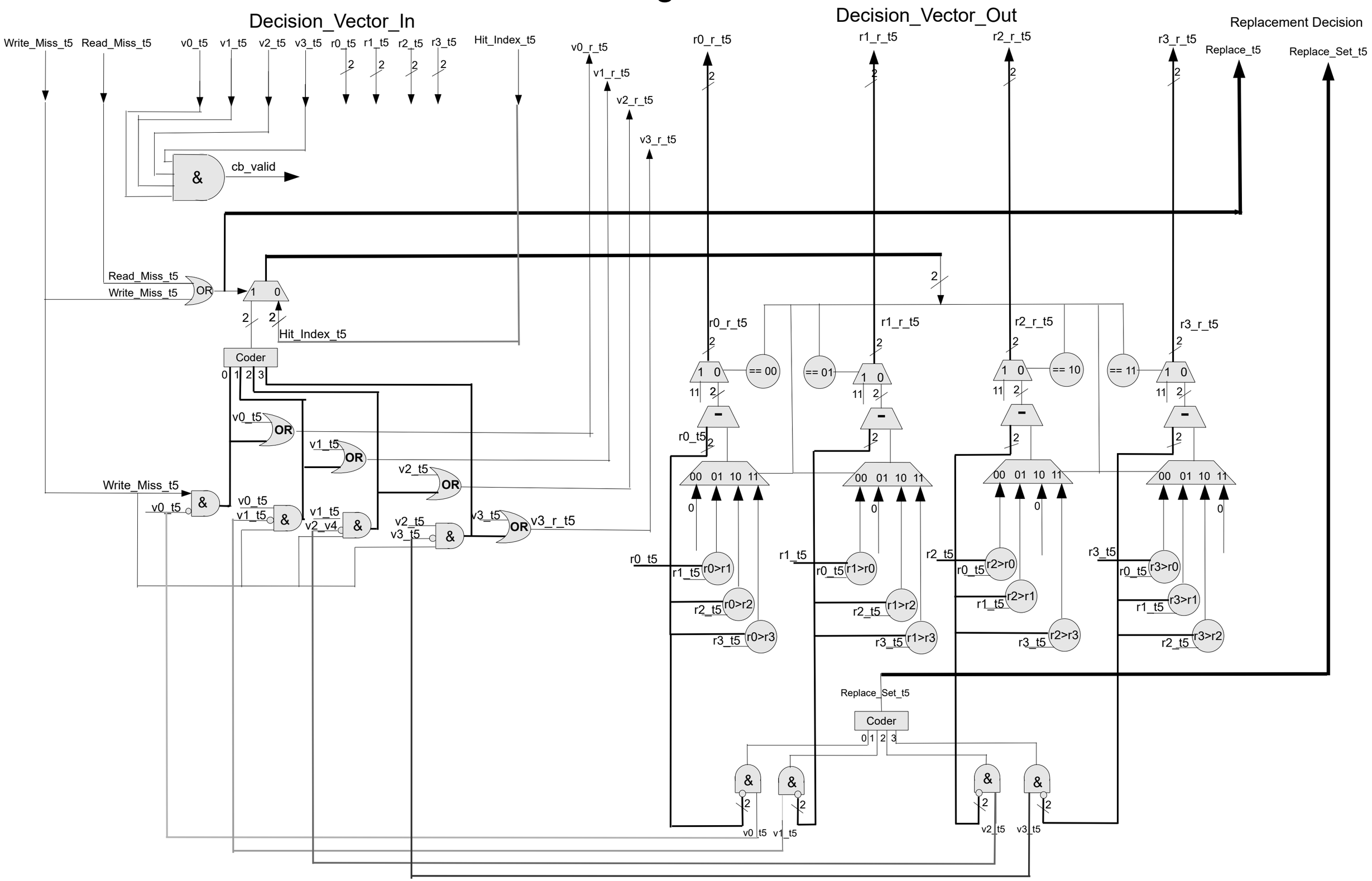
Tag Logic Interface



Set Interface for Set N [0..3]



LRU Logic


Decision_Vector_In
Decision_Vector_Out
Replacement Decision
Write_Miss_t5
Read_Miss_t5
v0_t5
v1_t5
v2_t5
v3_t5
r0_t5
r1_t5
r2_t5
r3_t5
Hit_Index_t5
Replace_t5
Replace_Set_t5
cb_valid
&
OR
Coder
v0_r_t5
v1_r_t5
v2_r_t5
v3_r_t5
v2_v4
v3_r_t5
== 00
== 01
== 10
== 11
00 01 10 11
r0>r1
r0>r2
r0>r3
r1>r0
r1>r2
r1>r3
r2>r0
r2>r1
r2>r3
r3>r0
r3>r1
r3>r2