A High-Speed, Low-Power, High-Reliability and Fully Single Event Double Node Upset Tolerant Design for Magnetic Random Access Memory

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***Abstract*— Magnetic Random Access Memory (MRAM) has enormous application potential in the aerospace field due to its nonvolatile, high speed, low power, and inherent radiation resistance characteristics. Due to its high sensing reliability, pre-charge differential sense amplifier (PCDSA) has been proposed and widely used in MRAM products. However, such PCDSA is based on traditional CMOS technology, and as the size of CMOS technology continues to shrink, its sensing result is easily affected by single event upset (SEU) or even the single event double node upset (SEDU). Recently, a TSC-PCDSA has been proposed to fully tolerate SEDU. However, it still suffers from slow speed, high power consumption and low reliability during normal sense operation. To address these issues, this paper proposes a novel PCDSA circuit that uses 6 three-input approximate C-elements (TACs) and 2 three-input standard C-elements (TSCs) to provide SEDU-tolerance. By reducing the number of transistors on the discharge path and increasing the difference in discharge current, the proposed PCDSA can achieve high speed, low power and high reliability. By using a physics-based STT-MTJ compact model and a commercial CMOS 40 nm design kit, hybrid simulations have been performed to demonstrate its functionality and evaluate its performance. Simulation results show that when the TMR is 150%, the width of N1-N12 is 480 nm and the V_{DD} is 1.1 V, the proposed PCDSA sensing error rate (SER) is close to 0% during normal sense operation, achieving a high sense speed of 123.6 ps and a low sense energy of 1.6533 fJ. Compared with the previously proposed TSC-PCDSA, the sense reliability is greatly improved, and the sense time and sense energy are reduced by 1.84 times and 1.27 times, respectively. Moreover, the proposed PCDSA can fully tolerate SEDU by optimizing the layout design. In the worst case where deposited charge Q_{inj} is 2 pC, it can achieve a shorter recover time of 1.28244 ns and a lower recover energy dissipation of 2.1604 pJ than the previously proposed TSC-PCDSA.**

***Index Terms*— Magnetic random access memory (MRAM), pre-charge differential sense amplifier (PCDSA), single event upset (SEU), single event double node upset (SEDU), three-input C-element, magnetic tunnel junction (MTJ), sensing-error-rate (SER), recover time, recover energy dissipation.**

I. Introduction

SPIN transfer torque magnetic random access memory (STT-MRAM) is an emerging storage technology that has attracted widespread attention owing to its nonvolatile, low power, fast access, and high density characteristics [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. Moreover, Magnetic tunnel junction (MTJ) as the fundamental element of STT-MRAM is inherently robust against radiation induced faults, making it have enormous potential in the aerospace field [11], [12], [13].

The MTJ consists mainly of two ferromagnetic (FM) layers and a ultra-thin oxide barrier layer sandwiched in between [14]. One of the FM layers is called the Reference Layer or Pinned Layer, and its magnetization direction is fixed. The other FM layer is called the Free Layer, and its magnetization direction can be switched by applying one large bidirectional current (exceeding its critical switching current I_{C0}) to the MTJ owing to the TMR effect [15], [16], [17], [18], [19], [20]. Depending on the relative magnetization directions of the two FM layers, one MTJ can exhibit two different resistance states, which are used to represent the binary logic information '0' and '1': when the two magnetization directions are parallel, the MTJ exhibits a low resistance state (R_P); and when the two magnetization directions are anti-parallel, the MTJ exhibits a high resistance state (R_{AP}). The resistance difference can be characterized by the tunnel magneto-resistance ratio (TMR $= (R_{AP} - R_P)/R_P$) [21], [22]. For practical applications, the sensing-error-rate (SER) is determined by the TMR. To improve the sensing reliability, researchers proposed a differential memory cell (DMC) at the expense of memory density, as shown in Fig. 1(b), where two MTJs in the complementary resistive states are used to represent 1 bit. To sense the information stored in such DMC, a pre-charged differential sense amplifier (PCDSA)

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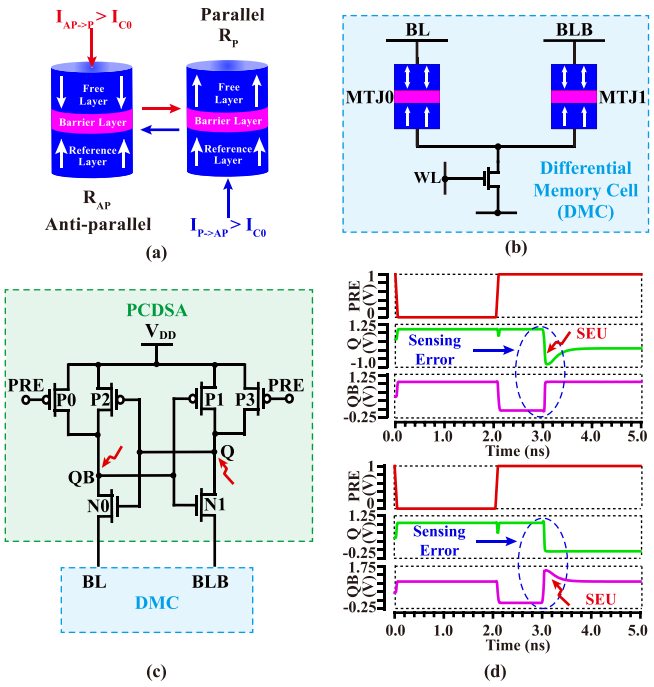


Fig. 1. (a) Structure schematic of the MTJ device and the STT write mechanism; (b) the previously proposed differential memory cell (DMC) and (c) its corresponding PCDSA circuit; (d) the effect of the SEU on the PCDSA.

circuits [23], [24], [25] was proposed in Fig.1(c) to achieve high speed, low power consumption and high reliability.

Owing to the use of magnetization direction instead of electronic charge to store data information, MTJ has natural radiation resistance [26], [27]. However, the PCDSA in STT-MRAM is based on CMOS technology, which is susceptible to energetic radiation particles [28], [29]. For example, when an energetic particle strikes on one of the sensitive nodes, i.e., the node Q and QB, a sensing error is generated as shown in Fig. 1(d). This phenomenon is knowns as single event upset (SEU) [6], [30], [31], [32], [33]. Moreover, with the shrinking CMOS technology, energetic particle strikes may even affect two adjacent sensitive nodes, resulting in a soft error called single event double upset (SEDU) [34], [35], [36].

Fig. 2(a) shows the SEDU-tolerant PCDSA proposed in [37], which uses a 6-node redundant dual interlocked storage cell (DICE) and a three-input standard C-element (TSC) to provide SEDU-tolerance, called DICE-PCDSA. However, it suffers from weak SEDU-tolerance with a maximum deposited charge of only 26 fC.

To address this issue, as shown in Fig. 2(b), a novel SEDU-tolerant PCDSA has recently been proposed, which uses 7 TSCs to provide SEDU-tolerance, referred to as TSC-PCDSA [38]. It has a maximum deposited charge of up to 2 pC, implying that it can be fully tolerant SEDU. However, as for the SEDU-Tolerant latch circuit block of the TSC-PCDSA, it suffers from larger sense delay and high sense power consumption during its normal sense operation owing to that there exits a larger number of transistors in the discharge path. Moreover, as for its output block, it is composed of only 1 TSC, leading to the asymmetry in the discharge path and then resulting in low sense reliability.

In this paper, we propose a novel fully SEDU-tolerant PCDSA for high speed, low power, high reliability sense operation. The contributions of this paper can be summarized as follows:

1) We propose a PCDSA based on 6 cross-coupled three-input approximate C-elements (TACs) and 2 cross-coupled TSCs, which can fully tolerate SEDU. And during normal sense operation, it has characteristics such as high speed, low power and high reliability. By using a physics-based STT-MTJ compact model and a commercial CMOS 40nm design kit, hybrid CMOS/MTJ simulations are performed to verify functionality of the sense radiation-hardened and evaluate relevant metrics.

2) We firstly investigate the effect of using two TSCs in the output block on the reliability, and the sense error in the proposed PCDSA is greatly reduced.

The rest of the paper is organized as follows. Section II introduces the proposed SEDU-tolerant PCDSA circuit and its mechanism in detail. Hybrid CMOS/MTJ simulations are performed to demonstrate its functionalities in Section III. Section IV presents the performance analysis. Finally, Section V concludes this paper.

II. Proposed SEDU-Tolerant PCDSA for MRAM

A. Proposed PCDSA

Fig. 3(a) shows the proposed PCDSA, which is mainly composed of four parts, i.e., the pre-charge block, the SEDU-tolerant latch circuit block, the DMC and the output block. In particular, the latch circuit block is composed of 6 cross-coupled TACs (i.e., TAC1, TAC2, TAC3, TAC4, TAC5, TAC6). And the output block is based on 2 cross-coupled TSCs (i.e., TSC1, TSC2) to tolerate the SEDU. Both TSC and TAC behave as inverters when all of their inputs have the same logic value. However, when the inputs are strike by energetic particles causing their logic values to flip, they have different fault-tolerability. In the following, we will introduce the fault-tolerability of TSC and TAC.

With TSC, if the logic value of any one node or any two nodes at the input are flipped, the output state cannot change. The fault will only propagate to the output if the logic values of all nodes at the input are flipped. The TSC can fully tolerate SEU and SEDU [39].

With TAC, if the logic value of any one node at the input is flipped, the output state cannot change. If the logic value of any two nodes at the input are flipped, when the logic value at the output of the TAC is '0', the fault will propagate to the output whenever the logic values of inputs I1 and I2 are flipped. Similarly, when the logic value at the output of the TAC is '1', the fault will propagate to the output whenever the logic values of inputs I1 and I3 are flipped. In other cases, the output state cannot change. TAC can fully tolerate SEU and partially tolerate SEDU. Fig. 3(c) shows the truth table of TSC and TAC.

B. Normal Operation

The sense operation of the proposed PCDSA is similar to the conventional PCDSA. It is divided into two phases,

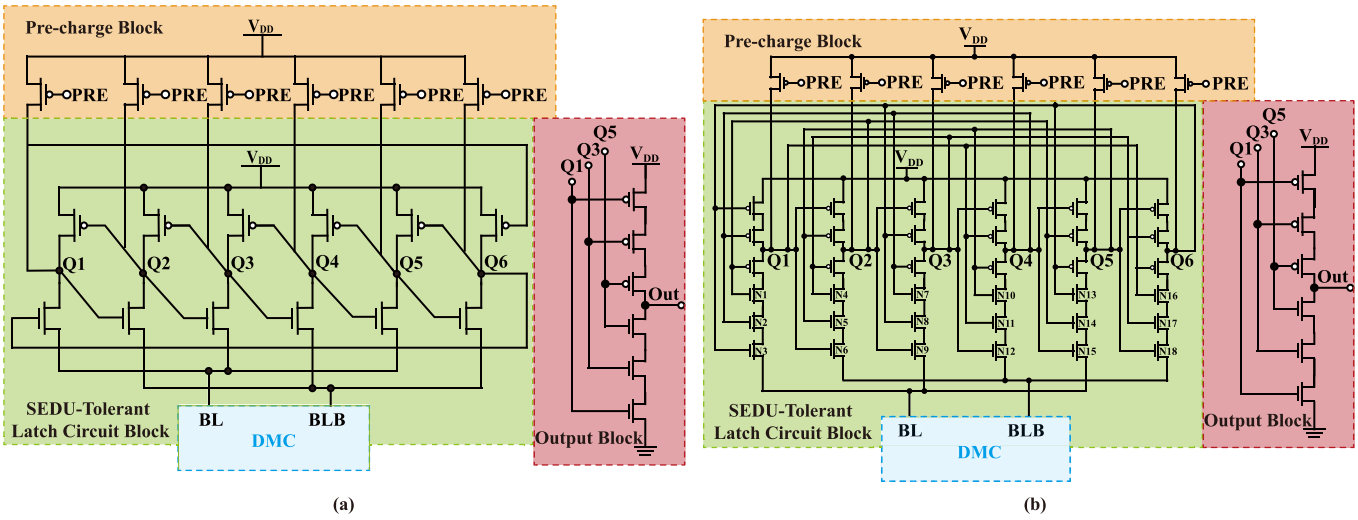
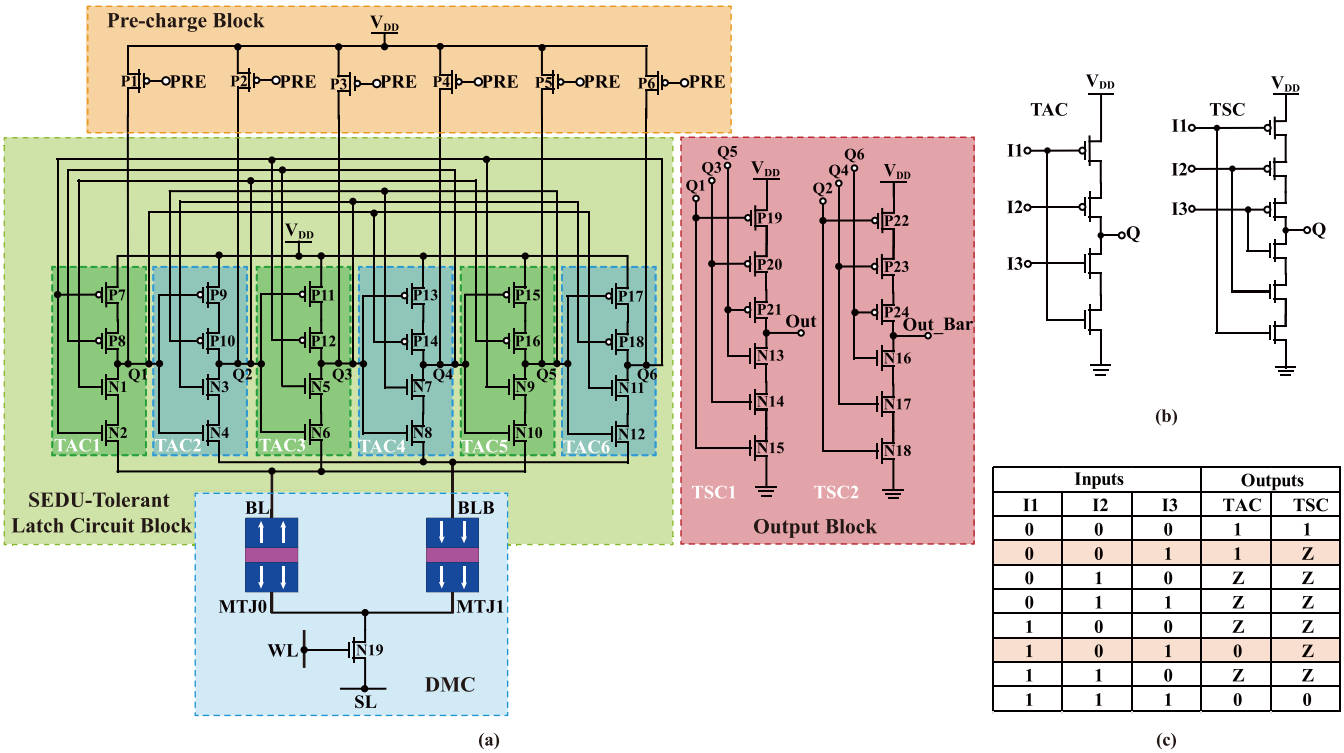


Fig. 2. Previously proposed SEDU-tolerant PCDSA. (a) DICE-PCDSA; (b) TSC-PCDSA.



Inputs			Outputs	
I1	I2	I3	TAC	TSC
0	0	0	1	1
0	0	1	1	Z
0	1	0	Z	Z
0	1	1	Z	Z
1	0	0	Z	Z
1	0	1	0	Z
1	1	0	Z	Z
1	1	1	0	0

(c)

Fig. 3. (a) Schematic of the proposed SEDU-tolerant PCDSA circuit; (b) The schematic and (c) the truth table of TAC and TSC.

i.e. the pre-charge phase and the sense phase, as shown in Fig. 4. During the pre-charge phase, both the PRE and WL signals are set to GND. Thus, the P1-P6 transistors are turned "ON" while the N19 transistor is "OFF". As a result, the nodes Q1-Q6 are pre-charged to V_{DD}. During the sense phase, both the PRE and WL signals are set to V_{DD}. Due to the different resistance of the MTJ0 and MTJ1 in the two discharge paths, the nodes Q1-Q6 begin to discharge with different speeds. When the (MTJ0, MTJ1) is in the (R_P, R_{AP}) state, the voltages of nodes(Q1, Q3, Q5) discharge faster and thus turning to GND. On the contrary, the nodes(Q2, Q4, Q6) eventually remain high. In this configuration, the node Out and the node Out_Bar of the proposed PCDSA will be eventually charged to V_{DD} and discharged to GND, respectively. When the (MTJ0, MTJ1) is in the (R_{AP}, R_P) state, the voltages of nodes(Q2, Q4, Q6) discharge faster and thus turning to GND. On the contrary, the nodes(Q1, Q3, Q5) eventually remain high. In this configuration, the node Out and the node Out_Bar of the proposed PCDSA will be eventually discharged to GND and charged to V_{DD}, respectively.

C. SEDU-Tolerance Principle

In the following, the capabilities of the SEDU-tolerant PCDSA will be investigated. It's worth noting that the SEDU will be analyzed in the sense phase for this work, since the pre-charge phase is immune to the radiation effects.

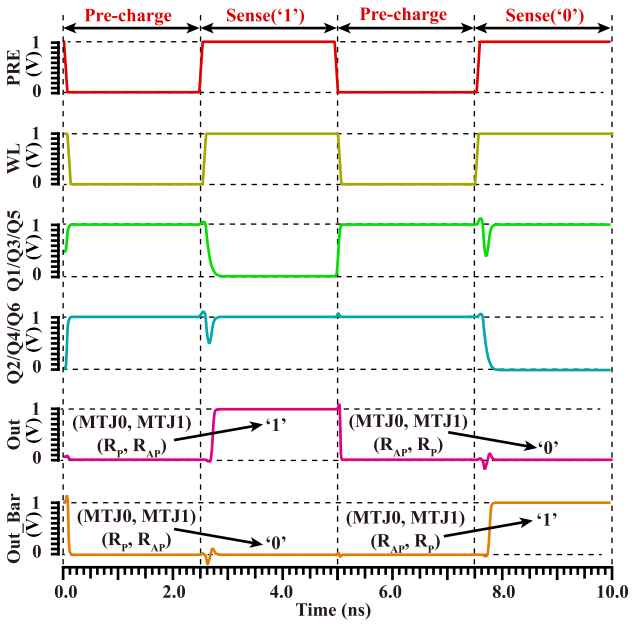


Fig. 4. Timing diagram of the sense operation of the proposed SEDU-Tolerant PCDSA.

In presence of an energetic particle affecting two sensitive nodes, the sense error may take place in three different kinds of struck node pairs. To illustrate the capability of the proposed PCDSA clearly, assume that the nodes (Q1, Q3, Q5) have the logic value of '0', the nodes (Q2, Q4, Q6) have the logic value of '1', the node (Out) has the logic value of '1', and the node (Out_Bar) has the logic value of '0'.

1) In the first case, consider the energetic particle strikes on any two nodes of the (Q1, Q3, Q5) or the (Q2, Q4, Q6) or the (Out, Out_Bar) of the proposed PCDSA and it can cause the logic value flip on these two nodes. In this case, the key node pairs include (Q1, Q3), (Q2, Q4) and (Out, Out_Bar).

If (Q1, Q3) suffers from a SEDU, according to the fault-tolerance of TAC, since the logic value of the output (Q2) of TAC2 is '1' and the logic values of the inputs I1 (Q1) and I3 (Q3) are flipped to '1', the error will be propagated to the output (Q2) of TAC2, and the logic value of Q2 is flipped to '0'. (Q4, Q5, Q6) keep their logic values unchanged. According to the fault-tolerance of TSC, (Out,Out_Bar) keep their logic values unchanged since only two nodes (Q1, Q3) are flipped at the input of TSC1 and only one node (Q2) is flipped at the input of TSC2.

If (Q2, Q4) suffers from a SEDU, according to the fault-tolerance of TAC, since the logic value of the output (Q5) of TAC5 is '0' and the logic values of the inputs I1 (Q4) and I2 (Q2) are flipped to '0', the error will be propagated to the output (Q5) of TAC5, and the logic value of Q5 is flipped to '1'. Since the inputs of TAC4 (Q3, Q1, Q5) correspond to the logic values (0, 0, 1), the output (Q4) will be charged to its initial logic value '1' in TAC4. Since the inputs of TAC5 (Q4, Q2, Q6) correspond to the logic values (1, 0, 1), the output (Q5) will be discharged to its initial logic value '0' in TAC5. Since the inputs of TAC2 (Q1, Q5, Q3) correspond to the logic values (0, 0, 0), the output (Q2) will be charged to its initial logic value '1' in TAC2. According to the fault-tolerance of TSC, (Out, Out_Bar) keep their logic values unchanged since (Q1, Q2, Q3, Q4, Q5, Q6) eventually keep their initial logic value.

If (Out, Out_Bar) suffers from a SEDU, according to the inverting feature of TSC, (Out) will be charged to its initial logic value '1' in TSC1 and (Out_Bar) will be discharged to its initial logic value '0' in TSC2 since (Q1, Q2, Q3, Q4, Q5, Q6) keep their initial logic value unchanged.

2) In the second case, consider the energetic particle strikes on one node of the (Q1, Q3, Q5) or the (Q2, Q4, Q6) and one node of the (Out, Out_Bar) of the proposed PCDSA and it can cause the logic flip on these two nodes. In this case, the key node pairs include (Q1, Out), (Q1, Out_Bar), (Q2, Out) and (Q2, Out_Bar).

If (Q1, Out) or (Q1, Out_Bar) suffers from a SEDU, according to the fault-tolerance of TAC, (Q2, Q4, Q6) keep their logic values unchanged since only one node (Q1) is flipped at the input of (TAC2, TAC4, TAC6). Since the inputs of TAC1 (Q6, Q4, Q2) correspond to the logic values (1, 1, 1), the output (Q1) will be discharged to its initial logic value '0' in TAC1. If (Q1, Out) suffers from a SEDU, according to the inverting feature of TSC, (Out) will be charged to its initial logic value '1' in TSC1 since (Q1, Q3, Q5) eventually keep the initial logic value. According to the fault-tolerance of TSC, (Out_Bar) keep its logic values unchanged since (Q2, Q4, Q6) keep their initial logic value unchanged. If (Q1, Out_Bar) suffers from a SEDU, according to the fault-tolerance of TSC, (Out) keep its logic values unchanged since (Q1, Q3, Q5) eventually keep their initial logic value. According to the inverting feature of TSC, (Out_Bar) will be discharged to its initial logic value '0' in TSC2 since (Q2, Q4, Q6) keep their initial logic value unchanged.

If (Q2, Out) or (Q2, Out_Bar) suffers from a SEDU, according to the fault-tolerance of TAC, (Q1, Q3, Q5) keep their logic values unchanged since only one node (Q2) is flipped at the input of (TAC1, TAC3, TAC5). Since the inputs of TAC2 (Q1, Q5, Q3) correspond to the logic values (0, 0, 0), the output (Q2) will be discharged to its initial logic value '1' in TAC2. If (Q2, Out) suffers from a SEDU, according to the inverting feature of TSC, (Out) will be charged to its initial logic value '1' in TSC1 since (Q1, Q3, Q5) keep their initial logic value unchanged. According to the fault-tolerance of TSC, (Out_Bar) keep its logic values unchanged since (Q2, Q4, Q6) eventually keep their initial logic value. If (Q2, Out_Bar) suffers from a SEDU, according to the fault-tolerance of TSC, (Out) keep its logic values unchanged since (Q1, Q3, Q5) keep their initial logic value unchanged. According to the inverting feature of TSC, (Out_Bar) will be discharged to its initial logic value '0' in TSC2 since (Q2, Q4, Q6) eventually keep their initial logic value.

3) In the third case, consider the energetic particle strikes on one node of the (Q1, Q3, Q5) and one node of the (Q2, Q4, Q6) of the proposed PCDSA and it can cause the logic flip on these two nodes. In this case, the key node pairs include (Q1, Q2), (Q1, Q4) and (Q1, Q6).

If (Q1, Q2) suffers from a SEDU, according to the fault-tolerance of TAC,(Q3, Q4, Q5, Q6) keep their logic values unchanged since only one node (Q1) or (Q2) are flipped

TABLE I
CRITICAL PARAMETERS FOR THE PROPOSED SEDU-TOLERANT PCDSA CIRCUIT

Parameter	Description	Default Value
L	Length of transistors	40 nm
W	Width of transistors	120 nm
D	Diameter of MTJ nanopillar	40 nm
TMR(0)	TMR ratio at 0 V_{bias}	1.5
T_{free}	Thickness of free layer	1.3 nm
T_{oxide}	Thickness of oxide layer	0.85 nm
R·A	Resistance-area product V_{bias}	$5\Omega \cdot \mu m^2$
ΔTMR	Variation of TMR ratio	0.03
ΔT_{free}	Variation of free layer thickness	0.03
ΔT_{oxide}	Variation of oxide layer thickness	0.03
a	Length of MTJ	40 nm
b	Width of MTJ	40 nm
V_{DD}	Voltage supply	1 V

at the input of (TAC3, TAC4, TAC5, TAC6). According to the fault-tolerance of TSC, (Out, Out_Bar) keep their logic values unchanged since only one node (Q1) is flipped at the input of TSC1 and only one node (Q2) is flipped at the input of TSC2.

If (Q1, Q4) suffers from a SEDU, according to the fault-tolerance of TAC, Since the inputs of TAC1 (Q6, Q4, Q2) correspond to the logic values (1, 0, 1), the output (Q1) will be discharged to its initial logic value '0' in TAC1. Since the inputs of TAC4 (Q3, Q1, Q5) correspond to the logic values (0, 0, 0), the output (Q4) will be charged to its initial logic value '1' in TAC4. According to the fault-tolerance of TSC, (Out, Out_Bar) keep their logic values unchanged since (Q1, Q2, Q3, Q4, Q5, Q6) eventually keep their initial logic value.

If (Q1, Q6) suffers from a SEDU, according to the fault-tolerance of TAC, Since the inputs of TAC6 (Q5, Q3, Q1) correspond to the logic values (0, 0, 1), the output (Q6) will be charged to its initial logic value '1' in TAC6. Since the inputs of TAC1 (Q6, Q4, Q2) correspond to the logic values (1, 1, 1), the output (Q1) will be discharged to its initial logic value '0' in TAC1. According to the fault-tolerance of TSC, (Out, Out_Bar) keep their logic values unchanged since (Q1, Q2, Q3, Q4, Q5, Q6) eventually keep their initial logic value.

III. FUNCTIONAL SIMULATION AND VERIFICATION

Based on a physics-based STT-MTJ compact model [40] and a commercial CMOS 40 nm design kit, hybrid simulations have been performed to demonstrate the functionality of the proposed SEDU-tolerate PCDSA. Table I lists the critical parameters of both the STT-MTJ and the transistors in the simulations.

A. The Radiation Current Injection Model

As shown in Fig. 5(a), the node connecting the drain of PMOS and the drain of NMOS are highly susceptible to be struck by the energetic particles. When the sensitive node is struck, its voltage will be changed to '0'(or '1'). Thus, the electric field in the reverse-biased junction depletion region of PMOS (or NMOS) can separate it into electron-hole pairs [41].

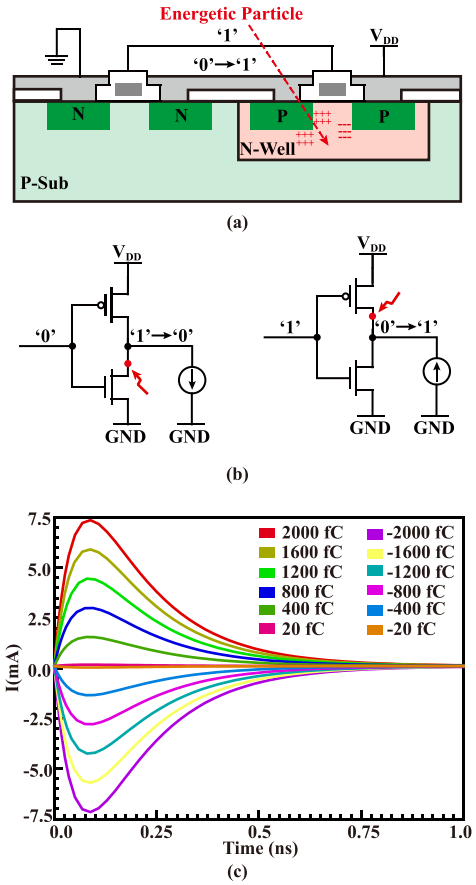


Fig. 5. (a) Charge deposition physics mechanism in an inverter; (b)when the transistor NMOS in an inverter is struck, a negative transient pulse is induced; when the transistor PMOS in an inverter is struck, a positive transient pulse is induced; (c) the shape of the transient injection current pulses striking at t = 0 with different values of Q_{inj}.

These electrons and holes drift to opposite directions and the holes are deposited in the drain of PMOS (or the electrons are deposited in the drain of NMOS), which is called charge deposition. As a result, when a radiation particle strikes the drain of PMOS transistor, only a positive transient pulse is generated. On the contrary, when a radiation particle strikes the drain of NMOS transistor, only a negative transient pulse is generated, as shown in Fig. 5(b).

Generally, such the injection current induced by the radiation effect can be described by a double exponential current source proposed in [42] as follows:

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2} \times (e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}) \quad (1)$$

where I_{inj} and Q_{inj} denote the injection current and the amount of the deposited charge in the struck node, respectively, TI and T2 are material-dependent time constants. The sign of the Q_{inj} depends on the type of the struck drain of the transistor. If it is the drain of the NMOS transistor in off state, the sign of the Q_{inj} is negative. And if it is the drain of the PMOS transistor in off state, the sign of the Q_{inj} is positive. Generally, the value of the Q_{inj} can be changed from -2 pC to $+2$ pC for simulations. Fig. 5(c) illustrates an example of a transient injection current pulse striking at t = 0 with different values

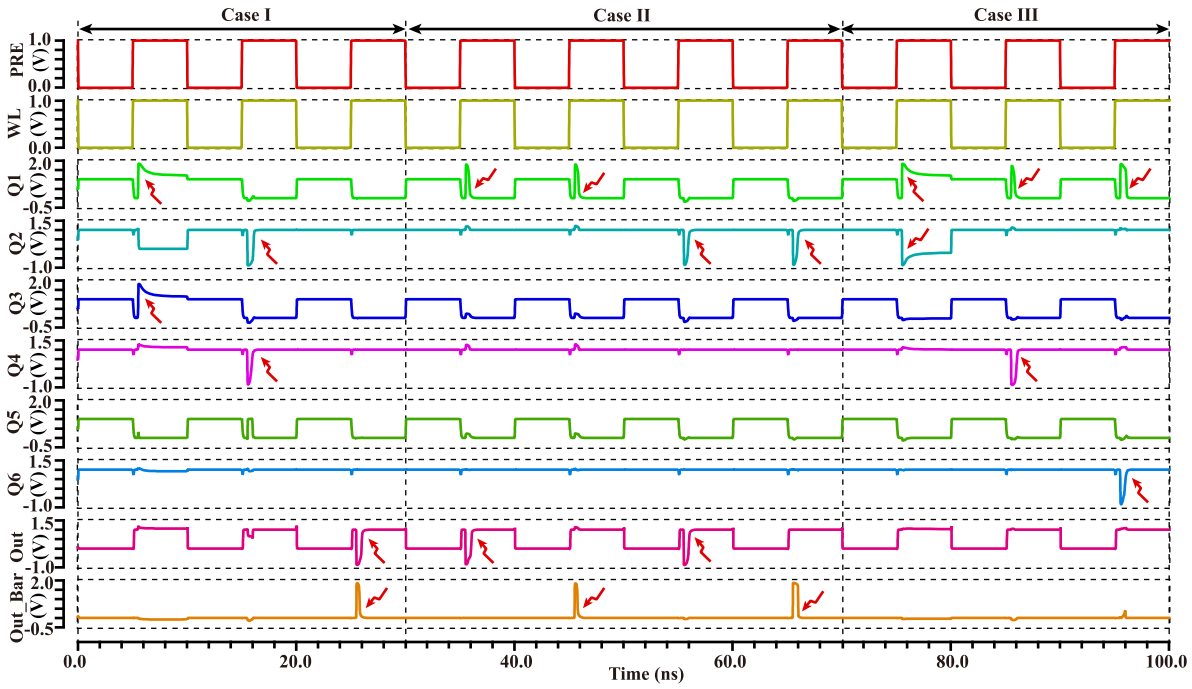


Fig. 6. The transient simulation waveforms of the proposed SEDU Tolerant PCDSA with consideration of the above illustrated three types of struck node pairs $Q_{\text{inj}} = 20$ fC in the configuration of the (MTJ0, MTJ1) in the (R_P, R_{AP}) state, i.e., the sensing result is '1'.

of the Q_{inj}, in which the T1 and T2 are set as 163 ps and 50 ps, respectively.

In the following simulations, to illustrate the effect of the SEDU on the proposed PCDSA, two radiation current pulses are applied on two sensitive nodes simultaneously. Additionally, the worst case has been considered: the energetic particles have energies at the limit of what is potentially destructive and all the particles hit the drains of transistors.

B. Functional Verification

Fig. 4 shows the transient simulation results for the normal sense operation of the proposed SEDU-tolerant PCDSA. Then, we investigate the SEDU-tolerant capability of the proposed PCDSA by considering all the different combinations of two sensitive nodes. As shown in Fig. 6, when the information stored in DMC is '1', we examined the above three different kinds of struck node pairs that may lead to sensing errors. In particular, for the case I, although the SEDU injection to the sensitive nodes (Q1, Q3) has changed their logic values and they cannot be recovered, the nodes Out and Out_Bar of the proposed PCDSA keep their logic values unchanged; although the SEDU injection to the sensitive nodes (Q2, Q4) has changed their logic values, they can be recovered after a few time and the nodes Out and Out_Bar of the proposed PCDSA always keep their logic values unchanged; although the SEDU injection to the sensitive nodes (Out, Out_Bar) has changed their logic values, they can be recovered after a few time. For the case II, the SEDU injection to the sensitive nodes (Q1, Out) or (Q1, Out_Bar) or (Q2, Out)or (Q2, Out_Bar)has changed their logic values; however, they can be recovered after a few time, i.e., the output of the proposed PCDSA is still fault free. For the case III, although the SEDU injection to the sensitive nodes (Q1, Q2) has changed their logic values and they cannot be recovered, the nodes Out and Out_Bar of the proposed PCDSA keep their logic values unchanged; although the SEDU injection to the sensitive nodes (Q1, Q4) or (Q1, Q6) has changed their logic values, they can be recovered after a few time and the nodes Out and Out_Bar of the proposed PCDSA always keep their logic values unchanged; In summary, the proposed PCDSA is immune to the SEDU.

IV. Performance Analysis

A. Reliability Analysis of Normal Operation

Firstly, as shown in Fig. 7, the difference of discharge currents (e.g., I0 of MTJ0 and I1 of MTJ1) in the proposed PCDSA without the element TSC2 is only 6.504 uA when the stored data is '1', which is much smaller than that (e.g., 9.2665 uA) when the stored data is '0'. Thus, the previous scheme with only one TSC for Out has the huge distinction in reliability when sensing different information, for the reason that extra parasitic capacitance is introduced to Q1, Q3 and Q5 and produces asymmetry to the discharge branches. As a result, both TSC1 and TSC2 for Out and Out_Bar are employed in the output block to guarantee symmetry. At this time, the difference of discharge currents is 8.2197 uA whatever the stored data is and the sensing-error-rate (SER) is balanced at the expense of area consumption. Additionally, to assure that the maximum amount of SER is described in previous schemes, the stored information is '1' in the following simulations.

To evaluate the SER of the proposed PCDSA, Monte-Carlo simulations (1000 runs per case) have been performed with consideration of the 1σ probability distributions of the CMOS transistors fixed by the CMOS process manufacturer

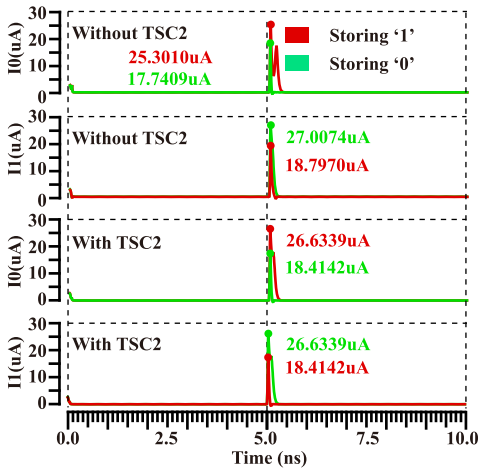


Fig. 7. The transient simulation waveforms of discharge currents (e.g.,I0 of MTJ0 and I1 of MTJ1) in the proposed PCDSA (e.g., without TSC2 or with TSC2) when the stored information is '1' or '0'.

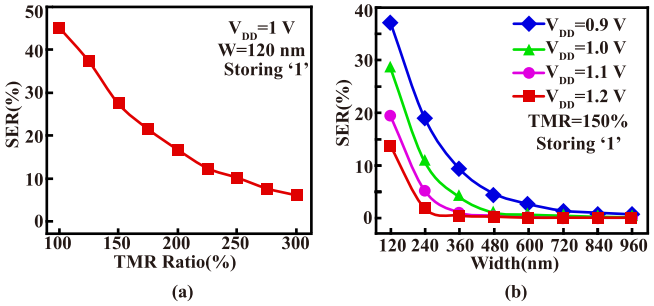


Fig. 8. Sensing-error-rate (SER) of the proposed PCDSA with respect to (a) different TMR, (b) different transistor widths with different supply voltages when the stored information is '1'.

and 3% process variations of MTJ, including TMR ratio, free layer thickness and oxide barrier thickness. Fig. 8(a) shows the influence of the TMR on the SER of the radiation-hardened schemes. As seen, the SER of the proposed PCDSA decreases greatly from 45.1% to 6% when the TMR increases from 100% to 300%, which means that increasing the TMR improves the reliability of sense operation.

Fig. 8(b) describes the SER with respect to the width of certain transistors (e.g., N1-N12 in the proposed PCDSA, N1-N18 in previously proposed TSC-PCDSA) at different supply voltages V_{DD}, where the TMR ratio is 150%. It can be seen that at a certain supply voltage V_{DD}, the SER of the proposed PCDSA decreases when the width of transistors increases, this is because with the width of transistors increase, the resistances in two discharge branches can be decreased and the difference of discharge currents can be also increased, thus the sense reliability is promoted. Similarly, the SER of the proposed PCDSA decreases at a certain width of transistors when the supply voltage V_{DD} increases, this is because with the supply voltage V_{DD} increase, the difference of discharge currents can be increased, thus the sense reliability is promoted. It is worth noting that at V_{DD} of 0.9 V or 1.0 V or 1.1 V or 1.2 V, the SER decreases to near 0% when the width of transistors increase to 840 nm, 600 nm, 480 nm, 360 nm, respectively.

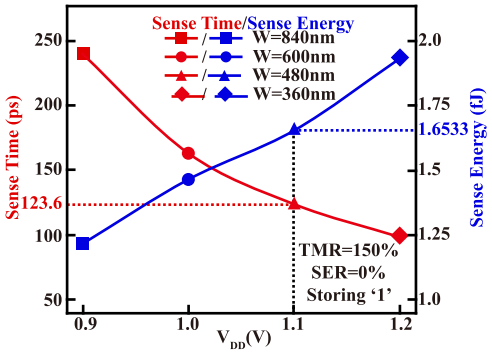


Fig. 9. Sense time and sense energy of the proposed PCDSA with respect to different supply voltages when the stored information is '1' and the sensing-error-rate (SER) is 0%.

B. Trade-Off Design Between Sense Speed and Sense Energy

We investigate the effect of the V_{DD} on both the sense time and sense energy of the proposed PCDSA. Fig. 9 shows the corresponding Monte-Carlo simulation results by varying the V_{DD} from 0.9 V to 1.2 V, where the TMR ratio is 150% and the SER is 0%. As seen, a lower supply voltage V_{DD} induces a higher sense time, but improving sense speed at the expense of sense energy. To achieve lower sense time, sense energy and area overhead, a trade-off design of the V_{DD} is 1.1 V for the proposed PCDSA with the TMR=150%, Width=480 nm, where the sense time, sense energy and SER are 123.6 ps, 1.6533 fJ and 0%, respectively. In this configuration, the sense time, sense energy and SER of previously proposed TSC-PCDSA are 227.9 ps, 2.1043 fJ and 3.1%, respectively. Simulation results show that the proposed PCDSA has higher speed, lower power consumption, and higher reliability compared to the previously proposed TSC-PCDSA, which is due to the fact that the proposed PCDSA reduces the number of transistors in the discharge path, thus increasing the discharge current difference.

C. SEDU-Tolerability Analysis

Generally, the range of SEDU deposition charge is between −2 pC-2 pC. If PCDSA can tolerate a deposition charge of 2 pC, it is considered that it can fully tolerate SEDU. As seen in Fig. 10(a) where the Q_{inj} is 2 pC, the above illustrated three different kinds of struck node pairs that may induce sensing error are examined. The simulation results show that, expect for the node pairs (Q1, Q2), the node Out and node Out_Bar still can be recovered to the initial logic value or keep the logic value unchanged when the energetic particles with a deposited charge of 2 pC strike on the other node pairs. Fig. 10(b) and Fig. 10(c) shows that when the energetic particles strike on the node pairs (Q1, Q2), the maximum deposited charge is only 33 fC. This can be further optimized in the layout design by increasing the distance between sensitive node pairs (Q1, Q2) to improve the SEDU-tolerance. Ultimately, the maximum deposited charge can reach 2 pC regardless of which node pair is impacted. This means that with further optimization of the layout design, the proposed PCDSA can fully tolerate SEDU.

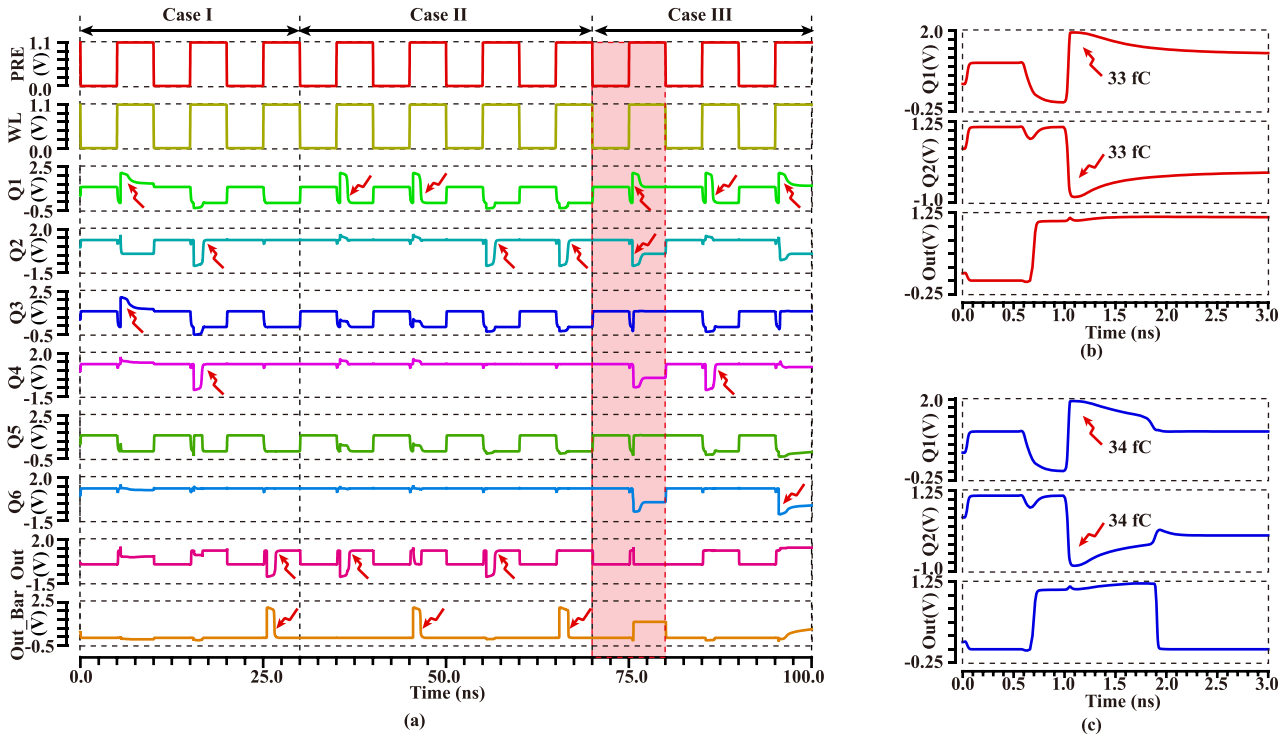


Fig. 10. (a) The transient simulation waveforms of the proposed SEDU-Tolerant PCDSA with consideration of the above illustrated three types of struck node pairs (Q_{inj} = 2 pC) in the configuration of the (MTJ0, MTJ1) in the (R_P, R_{AP}) state, i.e., the sensing result is '1'; the transient simulation waveforms of the struck nodes (Q1, Q2): (b) (Q_{inj} = 33 fC) and (c) (Q_{inj} = 34 fC).

D. Recover Time and Recover Energy Analysis

We define the recover time (T_R) from the moment when the node Out drops to 50% of V_{DD} after the energetic particle strikes to the moment when the node Out recovers to a half of its initial logic value and the recover energy (E_R) is defined as follows:

$$E_R = V_{DD} \times \int_{T_R} I_{total}(t)dt \tag{2}$$

From Fig. 10(a), it can be seen that when energetic particles strike node pairs (Q1, Out), the corresponding recover time and energy are maximized. Fig. 11 shows the maximal recover time and energy of the proposed PCDSA with respect to different Q_{inj}. As seen, the recover time increases from 513.17 ps to 1.28244 ns and the recover energy increases linearly from 4.6662 fJ to 2.1604 pJ when the Q_{inj} increases from 20 fC to 2 pC, where the TMR, width of N1-N12 and the V_{DD} are 150%, 480 nm and 1.1 V, respectively. Therefore, with the radiation intensity raising, the sense result is recovered at the expense of higher energy consumption.

E. Layout Implementation

Hybrid CMOS/MTJ process can be used to fabricate MTJs as they can be embedded above CMOS circuits. As shown in Fig. 12, MTJ fabrication can take place at the back-end of CMOS process from the first metal level (M1). Contacts are added between M1 and MTJ bottom electrode, MTJ top electrode and the second metal level (M2). Fig. 12 shows the layout of the proposed SEDU-tolerant PCDSA, which was drawn in the 40 nm layout design rules, and its effective area is about 18.946 μm^2.

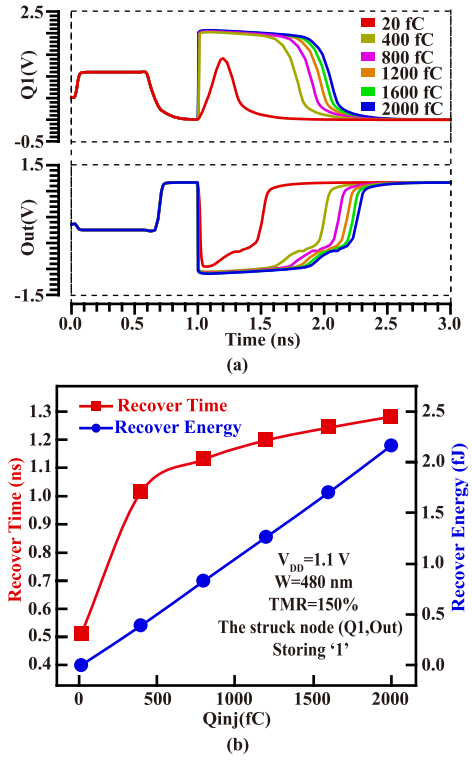


Fig. 11. (a) The transient waveforms of the node (Q1, Out) of the proposed SEDU-Tolerant PCDSA varying the Q_{inj} from 20 fC to 2 pC; (b) the effect of the Q_{inj} on the recovery time and energy dissipation.

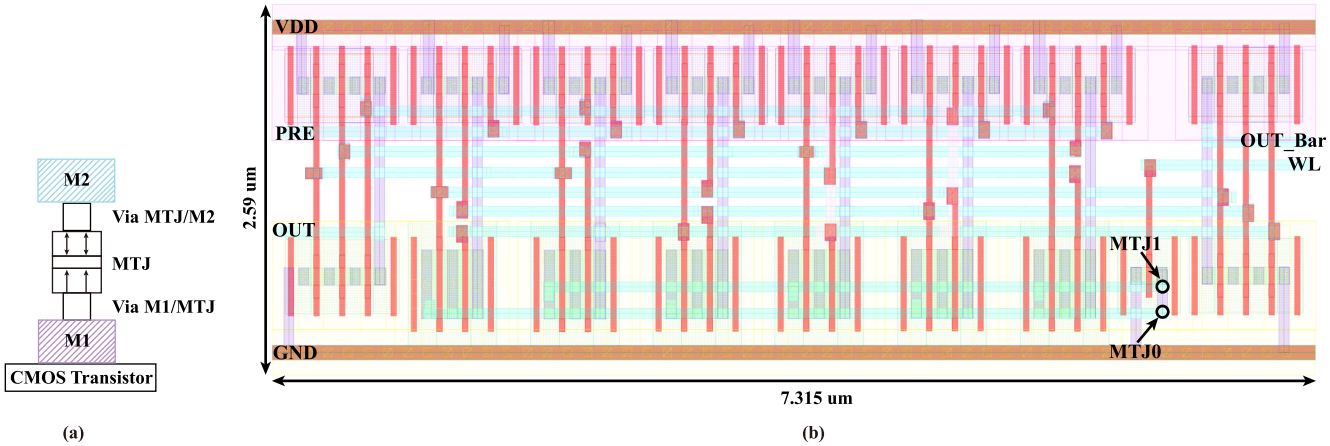


Fig. 12. Layout implementation of the proposed SEDU-tolerant PCDSA by using the CMOS 40 nm design kit.

TABLE II
PERFORMANCE COMPARISON WITH THE SAME SIMULATION CONDITIONS

Parameter	FRHR-15T [43]	TSC-PCDSA [38]	This work
Static Power	No	No	No
SER	51.10%	3.10%	0.00%
Sense Time	25.24 ps	227.9 ps	123.6 ps
Sense Energy	0.093 fJ	2.1043 fJ	1.6533 fJ
Failure node pairs @circuit level	2	0	0
$Q_{inj\text{-}max}$ of SEDU[1]	1 pC	2 pC	2 pC
Recover Time[2]	384.112 ps	539.14 ps	513.17 ps
Recover Energy[2]	11.9240 fJ	4.6838 fJ	4.6662 fJ
Cell area	6.425 μm^2	19.544 μm^2	18.946 μm^2

The TMR is 150%, the width of certain transistors is 480 nm (N1-N12 in the proposed PCDSA, N1-N18 in the previously proposed TSC-PCDSA) and the V_{DD} is 1.1 V.
[1] The $Q_{inj\text{-}max}$ of SEDU of the proposed PCDSA can reach 2 pC by optimizing its layout design.
[2] Q_{inj} is 20 fC

F. Performance Comparison

In this part, the performance of the proposed PCDSA is compared to that of the previously proposed TSC-PCDSA as well as the FRHR-15T proposed in [43], as shown in Table II. By using the same commercial CMOS 40 nm design kit and physics-based STT-MTJ compact mode, the performance of all the schemes is evaluated in the same conditions, where the TMR is 150%, the width of certain is 480 nm (N1-N12 in the proposed PCDSA, N1-N18 in the previously proposed TSC-PCDSA) and the V_{DD} is 1.1 V. For the normal sense operation, the proposed PCDSA has higher speed, lower power consumption, and higher reliability compared to the previously proposed TSC-PCDSA, which is due to the fact that the proposed PCDSA reduces the number of transistors in the discharge path, thus increasing the discharge current difference. For the recovery operation, the maximum deposited charge of the proposed PCDSA can reach up to 2 pC with further optimization of the layout design. This means that the proposed PCDSA can fully tolerate SEDU. Moreover, the proposed PCDSA has shorter recover time and lower recover energy dissipation than the previously proposed TSC-PCDSA when suffers from SEDU. The proposed PCDSA has the area overhead of 18.946 μm^2, which is similar to that (19.544 μm^2) of the previously proposed TSC-PCDSA. Compared with the FRHR-15T, the proposed PCDSA does not have failure node pairs at the circuit level, and its maximum deposited charge of the SEDU can reach up to 2 pC.

V. CONCLUSION

In this paper, a novel PCDSA circuit is proposed, which uses 6 TACs and 2 TSCs to provide SEDU-tolerance. By reducing the number of transistors on the discharge path and increasing the difference in discharge current, the proposed PCDSA can achieve high speed, low power and high reliability. To demonstrate its functionality and evaluate its performance, hybrid simulations have been performed by using a physics based STT-MTJ compact model and a commercial CMOS 40 nm design kit. Simulation results show that when the TMR is 150%, the width of N1-N12 is 480 nm and the V_{DD} is 1.1 V, the proposed PCDSA cannot occur any sense error during normal sense operation, and can achieve a high sense speed of 123.6 ps and a low sense energy of 1.6533 fJ. Compared with the previously proposed TSC-PCDSA, the sensing reliability is greatly improved. In addition, the sense time and sense energy are reduced by 1.84 times and 1.27 times, respectively. When the proposed PCDSA suffers from SEDU, it can fully tolerate SEDU by simply optimizing the layout design. Moreover, we investigate the effect of Q_{inj} on the recover time and energy dissipation. The results show that with the increase of the Q_{inj}, it can lead to longer recover time and energy dissipation. In the worst case where Q_{inj} is 2 pC, the proposed PCDSA can achieve a shorter recover time of 1.28244 ns and a lower recover energy dissipation of 2.1604 pJ than the previously proposed TSC-PCDSA. In summary, although the proposed PCDSA and the previously proposed TSC-PCDSA have the similar area overhead as shown in Table II, the former outperforms the latter in terms of the sense delay, sense power and sense reliability.

REFERENCES

[1] A. Amirany, K. Jafari, and M. H. Moaiyeri, "High-performance radiation-hardened spintronic retention latch and flip-flop for highly reliable processors," *IEEE Trans. Device Mater. Rel.*, vol. 21, no. 2, pp. 215–223, Jun. 2021.

[2] R. Rajaei, M. Fazeli, and M. Tabandeh, "Soft error-tolerant design of MRAM-based nonvolatile latches for sequential logics," *IEEE Trans. Magn.*, vol. 51, no. 6, pp. 1–14, Jun. 2015.

[3] S. Ikeda et al., "Tunnel magnetoresistance of 604% at 300K by suppression of ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature," *Appl. Phys. Lett.*, vol. 93, no. 8, pp. 67–70, Aug. 2008.

[4] W. Kang et al., "Spintronics: Emerging ultra-low-power circuits and systems beyond MOS technology," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 12, no. 2, pp. 1–42, Sep. 2015.

[5] E. Deng et al., "Synchronous 8-bit non-volatile full-adder based on spin transfer torque magnetic tunnel junction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 7, pp. 1757–1765, Jul. 2015.

[6] R. Rajaei, "Radiation-hardened design of nonvolatile MRAM-based FPGA," *IEEE Trans. Magn.*, vol. 52, no. 10, pp. 1–10, Oct. 2016.

[7] A. Amirany, K. Jafari, and M. H. Moaiyeri, "Highly reliable bio-inspired spintronic/CNTFET multi-bit per cell nonvolatile memory," *AEU Int. J. Electron. Commun.*, vol. 158, Jan. 2023, Art. no. 154452.

[8] O. Goncalves, G. Prenat, and B. Dieny, "Radiation hardened LUT for MRAM-based FPGAs," in *Proc. Int. Semiconductor Conf. Dresden-Grenoble (ISCDG)*, Sep. 2012, pp. 33–36.

[9] A. Amirany, K. Jafari, and M. H. Moaiyeri, "High-performance and soft error immune spintronic retention latch for highly reliable processors," in *Proc. 28th Iranian Conf. Electr. Eng. (ICEE)*, Aug. 2020, pp. 1–5.

[10] A. K. Shukla, S. Soni, and B. K. Kaushik, "Novel radiation hardened DSOT-MRAM read peripheral circuit with reduced sensitive nodes," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 11, pp. 4236–4240, Sep. 2023.

[11] G. Wakimura, T. Matsuoka, and Y. Kamakura, "A simulation study on soft error rate in STT-MRAM," in *Proc. IEEE Int. Meeting Future Electron Devices, Kansai (IMFEDK)*, Jun. 2015, pp. 104–105.

[12] J. Lopes, G. Di Pendina, E. Zianbetov, E. Beigne, and L. Torres, "Radiative effects on MRAM-based non-volatile elementary structures," in *Proc. IEEE Comput. Soc. Annu. Symp. (VLSI)*, Jul. 2015, pp. 321–326.

[13] J. Yang et al., "Radiation-induced soft error analysis of STT-MRAM: A device to circuit approach," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 3, pp. 380–393, Mar. 2016.

[14] Y. Wang, Y. Zhang, E. Y. Deng, J. O. Klein, L. A. B. Naviner, and W. S. Zhao, "Compact model of magnetic tunnel junction with stochastic spin transfer torque switching for reliability analyses," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 1774–1778, Sep. 2014.

[15] M. Wang et al., "Field-free switching of a perpendicular magnetic tunnel junction through the interplay of spin–orbit and spin-transfer torques," *Nature Electron.*, vol. 1, no. 11, pp. 582–588, 2018.

[16] S. S. P. Parkin, R. Bhadra, and K. P. Roche, "Oscillatory magnetic exchange coupling through thin copper layers," *Phys. Rev. Lett.*, vol. 66, no. 16, pp. 2152–2155, Apr. 1991.

[17] T. Miyazaki, T. Yaoi, and S. Ishio, "Large magnetoresistance effect in 82Ni-Fe/Al-Al_2O_3/Co magnetic tunneling junction," *J. Magn. Magn. Mater.*, vol. 98, nos. 1–2, pp. L7–L9, Jul. 1991.

[18] R. Schad, C. D. Potter, P. Beliën, G. Verbanck, V. V. Moshchalkov, and Y. Bruynseraede, "Giant magnetoresistance in Fe/Cr superlattices with very thin Fe layers," *Appl. Phys. Lett.*, vol. 64, no. 25, pp. 3500–3502, Jun. 1994.

[19] T. Miyazaki, "Giant magnetic tunneling effect in Fe/Al_2O_3/Fe junction," *J. Magn. Magn. Mater.*, vol. 139, no. 3, pp. l231–l234, Jan. 1995.

[20] W. H. Butler, X.-G. Zhang, T. C. Schulthess, and J. M. MacLaren, "Spin-dependent tunneling conductance ofFelMgOlFesandwiches," *Phys. Rev. B, Condens. Matter*, vol. 63, no. 5, Jan. 2001, Art. no. 054416.

[21] X. Fong, Y. Kim, R. Venkatesan, S. H. Choday, A. Raghunathan, and K. Roy, "Spin-transfer torque memories: Devices, circuits, and systems," *Proc. IEEE*, vol. 104, no. 7, pp. 1449–1488, Jul. 2016.

[22] D. Apalkov et al., "Spin-transfer torque magnetic random access memory (STT-MRAM)," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 9, no. 2, pp. 1–35, 2013.

[23] W. Zhao, C. Chappert, V. Javerliac, and J.-P. Noziere, "High speed, high stability and low power sensing amplifier for MTJ/CMOS hybrid logic circuits," *IEEE Trans. Magn.*, vol. 45, no. 10, pp. 3784–3787, Oct. 2009.

[24] C. Wang, D. Zhang, L. Zeng, E. Deng, J. Chen, and W. Zhao, "A novel MTJ-based non-volatile ternary content-addressable memory for high-speed, low-power, and high-reliable search operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 4, pp. 1454–1464, Apr. 2019.

[25] C. Wang, D. Zhang, L. Zeng, and W. Zhao, "Design of magnetic non-volatile TCAM with priority-decision in memory technology for high speed, low power, and high reliability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 2, pp. 464–474, Feb. 2020.

[26] F. Ren, A. Jander, P. Dhagat, and C. Nordman, "Radiation tolerance of magnetic tunnel junctions with MgO tunnel barriers," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 3034–3038, Dec. 2012.

[27] D. Kobayashi et al., "Influence of heavy ion irradiation on perpendicular-anisotropy CoFeB-MgO magnetic tunnel junctions," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1710–1716, Aug. 2014.

[28] R. Rajaei, M. Tabandeh, and M. Fazeli, "Low cost circuit-level soft error mitigation techniques for combinational logic," *Scientia Iranica Trans. Comput. Sci. Eng. Elect. Eng. (D)*, vol. 22, no. 6, pp. 2401–2414, 2015.

[29] R. Rajaei, M. Tabandeh, and M. Fazeli, "Soft error rate estimation for combinational logic in presence of single event multiple transients," *J. Circuits, Syst. Comput.*, vol. 23, no. 6, Jul. 2014, Art. no. 1450091.

[30] W. Kang et al., "A radiation hardened hybrid spintronic/CMOS non-volatile unit using magnetic tunnel junctions," *J. Phys. D, Appl. Phys.*, vol. 47, no. 40, Oct. 2014, Art. no. 405003.

[31] R. Rajaei, M. Tabandeh, and M. Fazeli, "Single event multiple upset (SEMU) tolerant latch designs in presence of process and temperature variations," *J. Circuits, Syst. Comput.*, vol. 24, no. 1, Jan. 2015, Art. no. 1550007.

[32] P. K. Mukku and R. Lorenzo, "A soft error upset hardened 12T-SRAM cell for space and terrestrial applications," *Memories Mater., Devices, Circuits Syst.*, vol. 6, Dec. 2023, Art. no. 100092.

[33] R. Sharma, D. Mondal, and A. P. Shah, "Radiation hardened 12T SRAM cell with improved writing capability for space applications," *Memories Mater., Devices, Circuits Syst.*, vol. 5, Oct. 2023, Art. no. 100071.

[34] A. Yan, H. Liang, Z. Huang, and C. Jiang, "High-performance, low-cost, and highly reliable radiation hardened latch design," *Electron. Lett.*, vol. 52, no. 2, pp. 139–141, Jan. 2016.

[35] R. Rajaei, B. Asgari, M. Tabandeh, and M. Fazeli, "Design of robust SRAM cells against single-event multiple effects for nanometer technologies," *IEEE Trans. Device Mater. Rel.*, vol. 15, no. 3, pp. 429–436, Sep. 2015.

[36] M. Karmakar, S. F. Naz, and A. P. Shah, "Fault-tolerant reversible logic gate-based RO-PUF design," *Memories Mater., Devices, Circuits Syst.*, vol. 4, Jul. 2023, Art. no. 100055.

[37] R. Rajaei, "Single event double node upset tolerance in MOS/spintronic sequential and combinational logic circuits," *Microelectron. Rel.*, vol. 69, pp. 109–114, Feb. 2017.

[38] D. Zhang et al., "Fully single event double node upset tolerant design for magnetic random access memory," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[39] M. Shams, J. C. Ebergen, and M. I. Elmasry, "Modeling and comparing CMOS implementations of the C-element," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 6, no. 4, pp. 563–567, Dec. 1998.

[40] Y. Zhang et al., "Compact modeling of perpendicular-anisotropy CoFeB/MgO magnetic tunnel junctions," *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 819–826, Mar. 2012.

[41] J. Guo, L. Xiao, and Z. Mao, "Novel low-power and highly reliable radiation hardened memory cell for 65 nm CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 1994–2001, Jul. 2014.

[42] M. Singh and I. Koren, "Fault-sensitivity analysis and reliability enhancement of analog-to-digital converters," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 5, pp. 839–852, Oct. 2003.

[43] A. K. Shukla, S. Soni, and B. K. Kaushik, "High radiation tolerant SOT-MRAM read peripheral circuit with fast data recovery," *Phys. Scripta*, vol. 98, no. 12, Dec. 2023, Art. no. 125301.

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