A Dual-Domain Dynamic Reference Sensing for Reliable Read Operation in SOT-MRAM

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***Abstract*— Although spin orbit torque magnetic random access memory (SOT-MRAM) is one of the strong candidates for next-generation embedded memories, the degradation of read margin due to low tunnel magnetoresistance ratio (TMR) with process variations has been a large concern. In this paper, we present the dual-domain dynamic reference (DDDR) sensing scheme, where the reference voltage can be dynamically changed based on the combined voltage and time domain sensing to increase the sensing margin. The Half Schmitt trigger and sample & hold circuits are efficiently employed to generate data-dependent reference voltages and to store the sampled voltage levels at different times, respectively. According to the simulations using 28nm CMOS technology with 128 by 128 SOT-MRAM array, the proposed DDDR approach achieves a 243mV of sensing margin under 6.08E-8 bit-error-rate (BER) at 1.76ns, which is 2X larger margin with more than 100 times lower BER compared to the conventional read scheme. When scaling down the pre-charge voltage, the proposed scheme achieves more than 50% of the read energy savings under 1E-5 target BER condition.**

***Index Terms*— Sensing circuit, sensing margin, dual-domain, dynamic reference, spintronics.**

I. Introduction

EVEN through the conventional memories such as static random access memory (SRAM) and dynamic random access memory (DRAM) have shown the unprecedented degree of integration with technology scaling, the aggressive scaling of CMOS device incurs several serious issues, like large leakage current and reliability degradation [1]–[3]. To relieve those scaling burdens, various non-volatile random access memories (NVRAMs)[4]–[9] have been actively studied. Among the next generation NVRAMs, spin-transfer torque magnetic random access memory (STT-MRAM) [10]–[12] has been considered as one of the promising candidates to replace the conventional memories thanks to its non-volatility, smaller area, low leakage power, and CMOS compatibility. Despite the advantages, STT-MRAM suffers from large write delays and energy [13], [14]. Recently, spin orbit torque magnetic random access memory (SOT-MRAM) [15]–[17] has been developed to address those write issues. SOT device can effectively reduce the write delay and energy based on spin hall effect (SHE) [18], [19] and the decoupled read-write path [20]. Although the write issues have been addressed in SOT-MRAM, another inherent issue encountered in MRAM is the relatively small read sensing margin due to low tunnel magnetoresistance (TMR) ratio [21]–[23], which results in large read energy to guarantee reliable read operations [24], [25].

Recently, in order to improve the read energy, the voltage mode sensing has been studied [26]. Compared to the current mode sensing, where continuous read current is wasted, the bit-line (BL) pre-charging has been employed to reduce unnecessary current wastes in voltage mode sensing [26]. Although the read energy has been improved in voltage mode sensing, the read reliability issue still exists due to inherent low TMR with process variations. The recent works in [27] and [28] have tried to increase the low sensing margin. Reliable read operations are enabled in [27] using the built-in self-test (BIST) circuits and the repetitive operations of sense amplifiers, while two reference voltages from different reference cells are adopted in [28] to improve the read reliability. Even though the sensing margin has been improved in the works [27], [28], one of the difficulties encountered is significantly large energy consumption owing to the repetitive operations of double sense amplifiers or the additional pre-charge BL, which dilutes the advantages of the voltage mode sensing.

In this paper, we present a highly reliable and energy-efficient dual-domain dynamic reference (DDDR) sensing technique for SOT-MRAM. The proposed DDDR sensing can dynamically change reference voltages depending on the data stored in a target cell, thus increasing the sensing margin during read operations. The time domain detection (TDD) unit employing half Schmitt trigger is also effectively adopted to generate data-dependent reference voltages by changing the sampling time. Sample & hold (S&H) circuits finally store the voltage levels sampled at different times for reliable voltage detection of a sense amplifier. The proposed DDDR sensing scheme has been simulated using 128 × 128 SOT-MRAM macros with Monte Carlo simulations. The simulation results show significant improvement of sensing margin as well as BERs. The rest of this paper is organized as follows.

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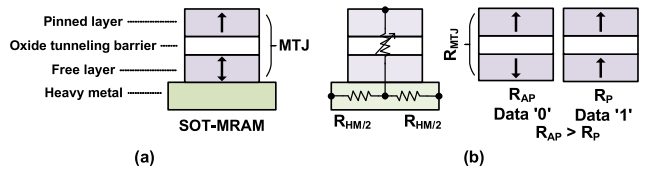


Fig. 1. (a) SOT device, (b) equivalent resistive models of SOT device.

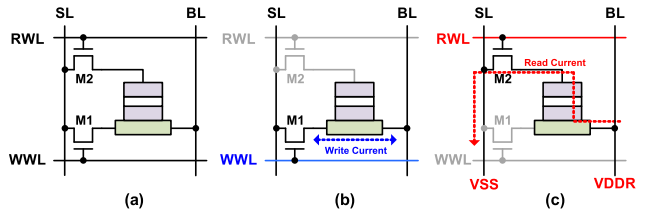


Fig. 2. (a) 2T-1MTJ SOT-MRAM cell, (b) write operation of SOT-MRAM, (c) read operation of SOT-MRAM.

Section II presents the basics of SOT-MRAM and the conventional voltage mode sensing schemes. The main idea and the details of the proposed DDDR sensing scheme are presented in Section III. Section IV shows the simulation results with evaluation, and the conclusions are drawn in Section V.

II. Preliminaries

A. SOT Device and SOT-MRAM

As shown in Fig. 1 (a), SOT device consists of magnetic tunnel junction (MTJ) and heavy metal (HM). The MTJ consists of three layers, where two ferromagnetic layers separated by one thin oxide tunneling barrier. Among the two ferromagnetic layers, the layer that changes magnetization is called free layer, while the fixed layer is called the pinned layer [29]. Fig 1. (b) shows the equivalent resistive model of SOT device. Depending on the relative magnetizations of the two ferromagnetic layers, the MTJ states are divided into antiparallel ('AP', high resistance) and parallel ones ('P', low resistance), which can be detected by comparing MTJ resistance with the reference ($R_{REF} = ((R_{AP} + R_P)/2)$. The state of MTJ is switched by flowing the switching current through HM [19].

Fig. 2 shows the structure and the operation of the conventional SOT-MRAM cell [15], which is composed of two transistors and one SOT device. For the write operation, the M1 transistor is switched on and the write current flows through HM. The source line (SL) and bit-line (BL) voltages are determined depending on the write data. For the read operation, SL and BL are applied with VSS and VDDR, respectively, and the M2 transistor is switched on to flow the read current through MTJ. Here, VDDR means the read voltage applied to the BLs.

B. The Conventional Voltage Mode Sensing Schemes in The Voltage Domain and The Time Domain

Fig. 3 presents the circuits and the operation of the voltage mode (VM) sensing scheme [26] for read operation. The

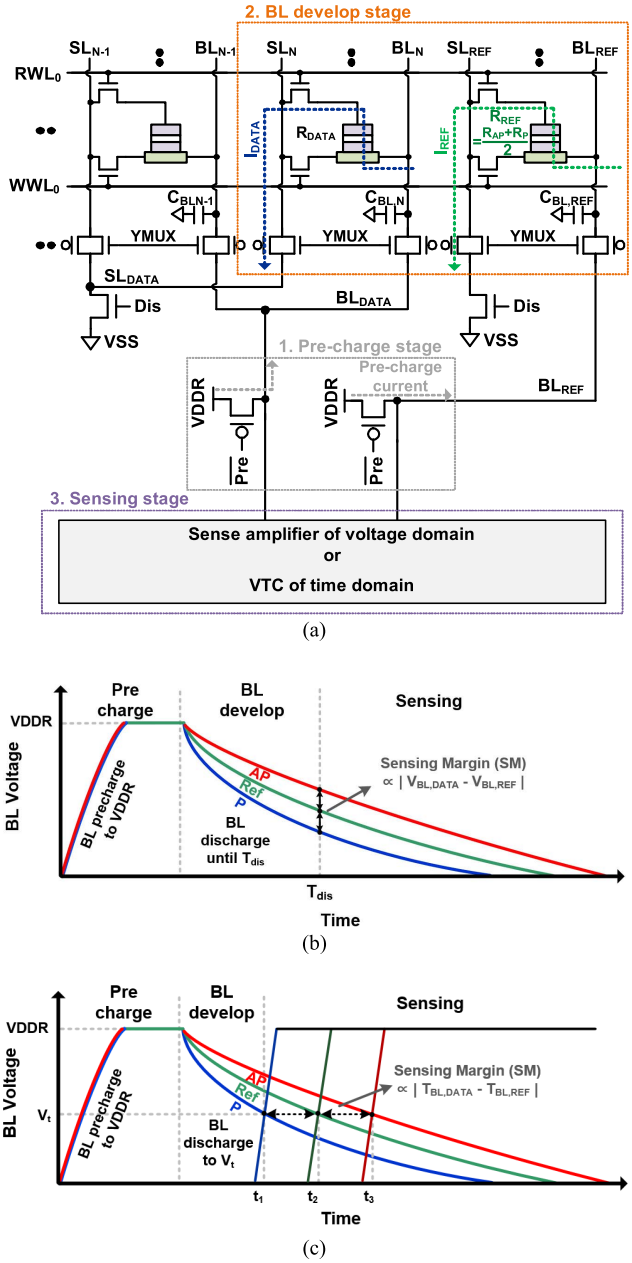


Fig. 3. (a) The voltage mode (VM) Sensing circuits [26]. The conceptual waveforms of VM sensing in (b) Voltage domain and (c) Time domain.

procedure of the voltage mode sensing is as follows: 1) pre-charge, 2) bit line (BL) develop, and 3) sensing stages. In the pre-charge stage, BL (BL_{DATA}, BL_{REF}) and SL (SL_{DATA}, SL_{REF}) in Fig. 3 (a) are pre-charged to VDDR and discharged to VSS, respectively. In the next BL develop stage, the pre-charge is stopped, and the read word-line (RWL) is activated for the read current (I_{DATA}, I_{REF}) to flow through SOT device. BL is also discharged by the read current. In the sensing stage, using the voltage level of BL, a sensing circuitry detects the state of the target SOT cell. Depending on the sensing circuit operations, VM sensing scheme is classified as voltage domain sensing [26] and time domain sensing [30].

In the voltage domain sensing [26], the BL voltage difference between BL_{DATA} voltage ($V_{BL,DATA}$) and BL_{REF} voltage

($V_{BL,REF}$), is detected using the sense amplifier at a fixed time as shown in Fig. 3 (b). BL voltages can be analyzed as RC circuit model [31] and it can be expressed as

$$V_{BL,DATA} = VDDR \cdot e^{-\frac{T_{dev}}{R_D C}},$$
$$V_{BL,REF} = VDDR \cdot e^{-\frac{T_{dev}}{R_R C}}, \quad (1)$$

where VDDR is initial pre-charged voltage level in BL, C is the total capacitance of BL. T_{dev} is the BL discharge time by read current, and R_D (R_R) is the total resistance of the read current-path flowing from BL_{DATA} (BL_{REF}). If the target SOT cell is 'AP' ('P') state, R_D becomes larger (smaller) than R_R, leading to larger (smaller) $V_{BL,DATA}$ than $V_{BL,REF}$. As shown in Fig. 3 (b), BLs, pre-charged to VDDR, are discharged in BL develop stage. According to (1), the decreasing slopes of the BL voltages are in the order of 'P', 'REF', and 'AP'. At T_{dis}, the sense amplifier is turned on to compare $V_{BL,REF}$ and $V_{BL,DATA}$. The larger the difference between two voltages, the more reliable becomes the read operation.

In the time domain sensing [30], the read operation is performed by detecting the BL discharge time at which the BL voltage reaches the pre-defined threshold voltage (V_t). By modifying (1), the discharge time can be expressed as

$$T_{BL,DATA} = R_D C \ln \frac{VDDR}{V_t},$$
$$T_{BL,REF} = R_R C \ln \frac{VDDR}{V_t}. \quad (2)$$

According to (2), when SOT device is 'AP' ('P') state, a longer (shorter) discharge time ($T_{BL,DATA}$) is needed for V_{BL} to reach V_t compared to $T_{BL,REF}$. As presented in Fig. 3 (c), t_2 is the time when $V_{BL,REF}$ reaches V_t, and t_1 (t_3) is the time when $V_{BL,DATA}$ reaches V_t in the SOT device state of the 'P' ('AP'). Read operation is performed by determining whether $T_{BL,DATA}$ is faster or slower than $T_{BL,REF}$. As the time difference between t_1 (t_3) and t_2 increases, more reliable read operation can be provided. Please note that to detect the time difference, voltage to time converter (VTC) [32], [33] is needed instead of a sense amplifier.

C. Challenge of The VM Sensing in Voltage and Time Domains

Fig. 4 shows the sensing margin of $V_{BL,DATA}$ ($V_{BL,P}$, $V_{BL,AP}$) over the discharge time during the read operation of VM in the voltage domain (VM_V) sensing. The sensing margin [34] in Fig. 4 is expressed as

$$SM = \left| V_{BL,DATA} - V_{BL,REF} - V_{offset} \right|, \quad (3)$$

where $V_{BL,DATA}$ and $V_{BL,REF}$ are the BL voltages, and V_{offset} is the offset voltage of sense amplifier. As illustrated in Fig. 4, for VM_V, the time at which the sensing margin has its maximum value is different depending on the SOT state [27]. For example, when SOT state is 'P', the sensing margin reaches its maximum earlier than the time when the SOT state is 'AP'. Since the sense amplifier is activated at one fixed time, the sensing time has to be decided at a point in the middle considering both states, as shown in Fig. 4.

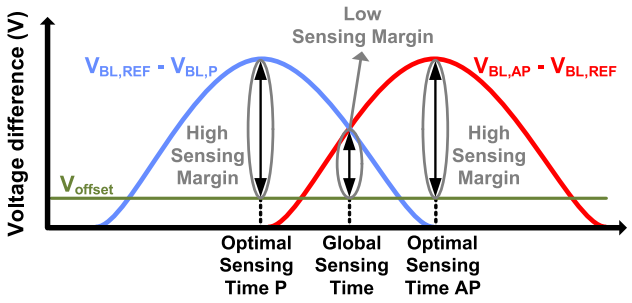


Fig. 4. The BL voltage difference over the discharge time.

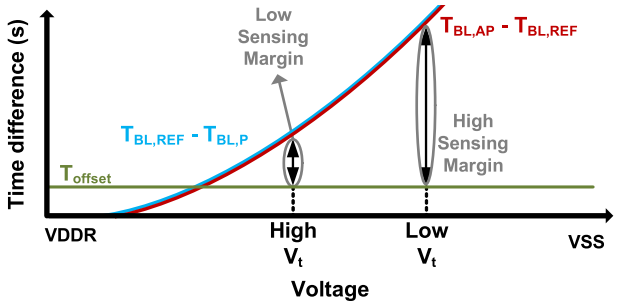


Fig. 5. The BL time difference over the voltage.

So, VM_V approach suffers from the inherent discrepancy in sensing margin depending on the SOT states.

Fig. 5 shows the sensing margin during the read operation of VM in the time domain (VM_T) sensing. Considering that the sensing margin can be obtained by the time difference between BL voltages reaching the pre-decided threshold voltage (V_t), the sensing margin in the time domain [35] can be expressed as

$$SM_{time} = \left| T_{BL,DATA} - T_{BL,REF} - T_{offset} \right|, \quad (4)$$

where $T_{BL,DATA}$ and $T_{BL,REF}$ are the discharge times when the BL voltage reaches V_t, and T_{offset} means the offset time of the VTC. Unlike VM_V, VM_T generally achieves a higher sensing margin since the sensing margins of both cases (the SOT states of 'P' and 'AP') have similar values at the same V_t. However, in order to guarantee a high sensing margin, V_t should be set to low, which considerably degrades the read speed.

As presented earlier, the main drawbacks of the conventional voltage mode sensing in voltage domain (VM_V) and time domain (VM_T) are the different sensing margins depending on SOT states and the read speed degradation to guarantee large sensing margin, respectively. In addition to the drawbacks, if we consider process variations, the situation is even aggravated due to wide range fluctuations of $V_{BL,DATA}$, $V_{BL,REF}$ and read current. In order to get over the main issues of the conventional read schemes, in the next section, we present DDDR sensing approach, where the reference voltages can be adaptively changed by combining the voltage domain and time domain (dual domain) voltage mode sensing.

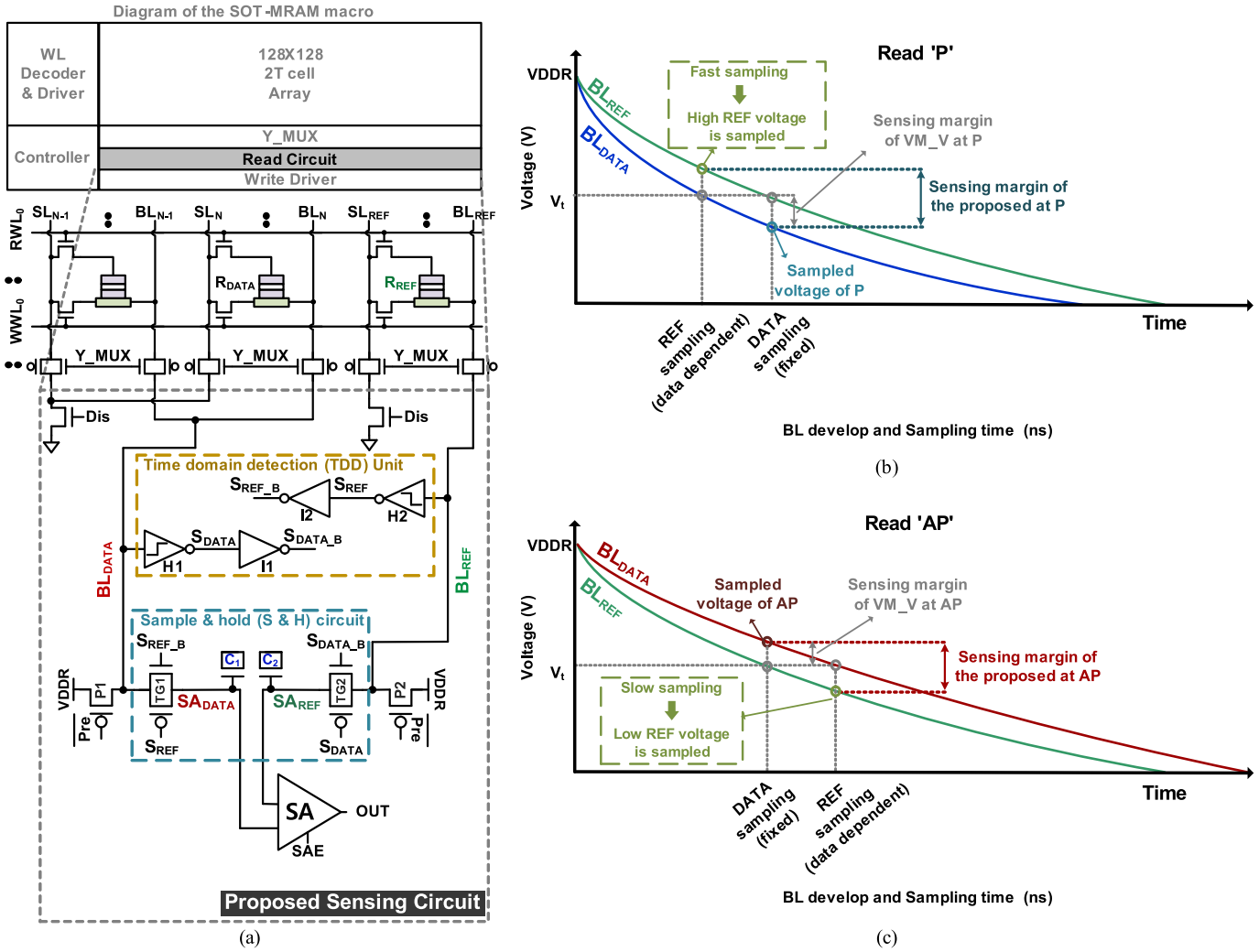


Fig. 6. (a) The proposed DDDR sensing circuits in SOT-MRAM Macro. The conceptual sensing margins for VM_V with DDDR in (b) P state and (c) AP state.

III. The Proposed Dynamic Reference Based Dual-Domain Sensing Scheme

In this section, we present the dual-domain dynamic reference (DDDR) sensing scheme with which dual-domain dynamic reference voltage can be generated to guarantee reliable sensing even with fast read time. The detailed circuit diagram and its operations including design issues are presented in this section.

A. The Proposed Dual-Domain Sensing Scheme

Fig. 6 (a) shows the proposed DDDR sensing circuits, which include time domain detection (TDD) unit, the sample and hold (S&H) circuits and a sense amplifier. The TDD unit consists of half-Schmitt triggers (H1, H2) [36] and inverters (I1, I2). As shown in Fig. 6 (a), H1 and H2 with a predefined threshold voltage V_t have BL_{DATA} and BL_{REF} as inputs, respectively. The S & H circuits, which are controlled by the outputs of the TDD unit (S_{DATA}, S_{DATA_B}, S_{REF}, S_{REF_B}), is composed of transmission gates (TG1, TG2) and sampling capacitors (C1, C2).

Fig. 6 (b) and (c) presents the conceptual waveforms and the basic operations of the DDDR sensing when the SOT cell has P and AP states, respectively. In the read operation, BL is initially pre-charged VDDR like the conventional VM_V and VM_T. After that, the BL develop stage and the sampling stage follows. During the BL develop stage, BL is discharged, and when the stored data is 'P', as R_{DATA} has smaller resistance than R_{REF} in Fig. 6 (b), the current on BL_{DATA} is larger than the one on BL_{REF}. So, $V_{BL,DATA}$ reaches V_t earlier, where V_t is the predefined threshold voltage on H1. At the moment when $V_{BL,DATA}$ reaches V_t, S_{DATA} is enabled and $V_{BL,REF}$ is sampled and stored in the sampling cap (SA_{REF}) as presented in the lower waveform of Fig. 6 (b). Here, the voltage on SA_{REF} is being applied to one end of sense amplifier shown in Fig. 6 (a). Afterwards, the slowly discharged (due to smaller current on BL_{REF}) $V_{BL,REF}$ also reaches to V_t. Then, S_{REF} is activated, and $V_{BL,DATA}$ is sampled and stored in the sampling cap (SA_{DATA}) that is applied to the other end of the sense amplifier. As presented in Fig. 6 (b), since those two voltages on SA_{REF} and SA_{DATA} nodes are sampled at different times due to different discharge speeds, it considerably increases the sensing margin.

When the stored data is 'AP', likewise, as R_{DATA} has larger resistance than R_{REF} in Fig. 6 (c), the current on BL_{REF} is larger than the one on BL_{DATA}. So, $V_{BL,REF}$ reaches V_t earlier, where V_t is the predefined threshold voltage on H2. At the moment when $V_{BL,REF}$ reaches V_t, $S_{REF}$is enabled, and $V_{BL,DATA}$ is sampled and stored in the sampling cap (SA_{DATA}) as presented in the lower waveform of Fig. 6 (c). Afterwards, the slowly discharged (due to smaller current on BL_{DATA}) $V_{BL,DATA}$ also reaches to V_t. Then, S_{DATA} is activated, and $V_{BL,REF}$ is sampled and stored in the sampling cap (SA_{REF}). Please note that the time when $V_{BL,REF}$ reaches the threshold voltage does not change regardless of the data stored in the target cell, and only the time at which $V_{BL,DATA}$ reaches the threshold voltage, varies depending on the data.

Fig. 7 shows the transient waveforms of the proposed DDDR sensing scheme when the target SOT cell has 'AP' state. The simulations are performed with 128 by 128 SOT-MRAM Macro when using 32 to 1 column MUX. In the pre-charge stage, Y- MUX is turned on and *Pre* signal in Fig. 6 (a) is enabled. By turning on the pre-charge transistors (P1, P2), BL_{DATA} and BL_{REF} are pre-charged to VDDR. Simultaneously, SA_{DATA} and SA_{REF} also are set to VDDR as TG1 and TG2 are on. Here, since VDDR is higher than V_t, S_{DATA} and S_{REF} are applied to VSS.

The BL develop and sampling stage starts with lowering the *Pre* signal. The low *Pre* signal turns off P1 and P2 to stop pre-charging. After that, the BL_{DATA} and BL_{REF} voltages are discharged by activating one of RWL_N. When the voltages of SA_{DATA} ($V_{SA,DATA}$) and SA_{REF} ($V_{SA,REF}$) are still higher than V_t, TG1 and TG2 are being turned on, and $V_{SA,DATA}$ ($V_{SA,REF}$) is discharged like $V_{BL,DATA}$ ($V_{BL,REF}$). Here, due to the high resistance of 'AP', $V_{BL,DATA}$ is discharged slower, and when $V_{BL,REF}$ reaches V_t (t_1), S_{REF} and S_{REF_B} are set to VDD and VSS, respectively. TG1 that is connected to BL_{DATA} is turned off as well. In this way, $V_{BL,DATA}$, which is higher than V_t, is sampled in $V_{SA,DATA}$. After t_1 passes and at the moment when $V_{BL,DATA}$ reaches V_t (t_2), S_{DATA} and S_{DATA_B} are set to VDD and VSS, respectively, and $V_{SA,REF}$ is sampled to $V_{BL,REF}$. Since $V_{SA,REF}$ is sampled later, $V_{SA,REF}$ is lower than $V_{SA,DATA}$. Finally, the sense amplifier, whose both ends are applied with $V_{SA,DATA}$ and $V_{SA,REF}$, is activated by the sense amplifier enable (SAE) signal, and the data '0' is readout.

In the DDDR sensing, thanks to the adaptively changing sampling voltages and times depending on the data stored in the target cell, it can achieve larger sensing margin compared to the conventional one. In addition, since the proposed DDDR sensing simply creates a dynamic reference through sampling, the area and energy overhead are very small, which will be discussed in Section IV.

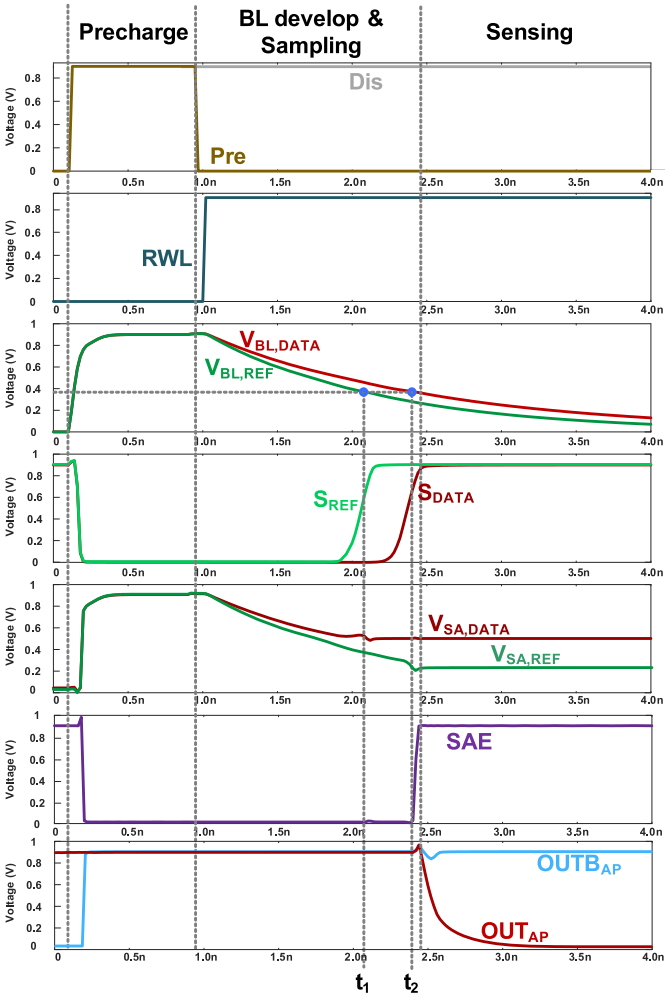


Fig. 7. The transient simulation waveforms of the proposed DDDR sensing scheme in 'AP' state.

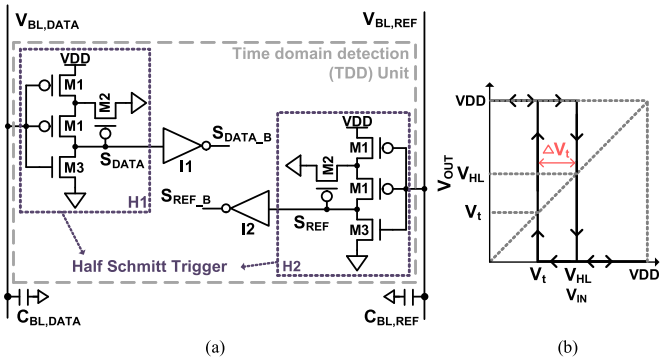


Fig. 8. (a) The schematic of the TDD unit in the proposed DDDR Aensing. (b) The voltage transfer curve (VTC) of half Schmitt trigger.

B. TDD Unit and Sense Amplifier Design

In the DDDR sensing, one of the most important design issues is how to set the threshold voltage V_t, since the sampling voltages and sensing margin are mainly decided by V_t. Fig. 8 (a) presents the detailed schematic of the TDD unit, which is composed of half-Schmitt triggers (H1, H2) and inverters (I1, I2). In the figure, $C_{BL,DATA}$ and $C_{BL,REF}$ mean the total capacitance of BL_{DATA} and BL_{REF}, respectively. The half Schmitt trigger [36], [37] schematic in the TDD unit is presented in Fig. 8 (a). We can notice from Fig. 8 (b) that V_t can be changed by controlling the transistor size of M1, M2, and M3. The half Schmitt trigger decreases the threshold

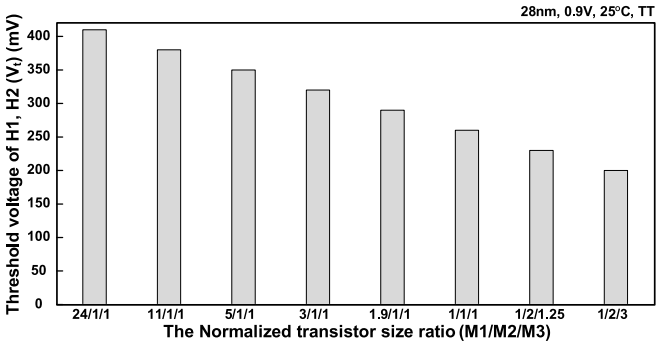


Fig. 9. The threshold voltage of H1, H2 (V_t) according to the various transistor size ratio.

voltage through the feedback of the M2 in the BL develop stage. Here, V_t can be expressed as following [36]–[38]:

$$\begin{aligned} V_t &= V_{HL} - \Delta V_t \\ &= \frac{VDD - \left|V_{thp1}\right| + \sqrt{\frac{2\beta_3}{\beta_1}} \cdot V_{thn3}}{\left(1 + \sqrt{\frac{2\beta_3}{\beta_1}}\right)} \\ &\quad - \frac{VDD - \left|V_{thp1}\right|}{\left(1 + \sqrt{\frac{\beta_1}{\beta_2}}\right)\left(1 + \sqrt{\frac{2\beta_3}{\beta_1}}\right)}, \end{aligned} \tag{5}$$

where $\beta_1, \beta_2, \beta_3$ are the transconductance coefficients [39], [40] of M1, M2, M3, respectively, and V_{thp1} and V_{thn3} are the threshold voltage of M1 and M3, respectively. Fig. 9 shows the changes of the threshold voltage (V_t) with varying the transistor size obtained from SPICE simulation using 28nm CMOS technology. As shown in the figure, V_t decreases as the M1 transistor becomes smaller and the M2 and M3 transistors become larger, which is the same tendency with (5).

The difference (ΔV_{SA}) of the sampling voltages ($V_{SA,DATA}$, $V_{SA,REF}$) that is changed with V_t, can be expressed as follows:

$$\begin{aligned} \Delta V_{SA} &= \left| V_{READ} e^{-\frac{t_R}{R_D C}} - V_{READ} e^{-\frac{t_D}{R_R C}} \right| \\ &= \left| V_{READ} \times \left(e^{-\frac{R_R C \ln\left(\frac{VDDR}{V_t}\right)}{R_D C}} - e^{-\frac{R_D C \ln\left(\frac{VDDR}{V_t}\right)}{R_R C}} \right) \right| \\ &= \left| V_{READ} \times \left(\left(\frac{VDDR}{V_t}\right)^{-\frac{R_R}{R_D}} - \left(\frac{VDDR}{V_t}\right)^{-\frac{R_D}{R_R}} \right) \right|, \end{aligned} \tag{6}$$

where t_R and t_D are the discharge times when $V_{BL,REF}$ and $V_{BL,DATA}$ become V_t, respectively. Considering that ΔV_{SA} is directly proportional to sensing margin, increasing ΔV_{SA} as large as possible is important. When V_t is set too high, since t_R and t_D become smaller, the voltages are sampled too early without sufficiently enlarging the BL voltage differences. If V_t is set too low, since t_R and t_D increases, samplings are performed too late after BL voltages becomes very low. In both of the cases, large sensing margins are not observed. Fig. 10 presents ΔV_{SA} depending on the transistor size ratios with various VDDRs. As shown in the figure, the transistor

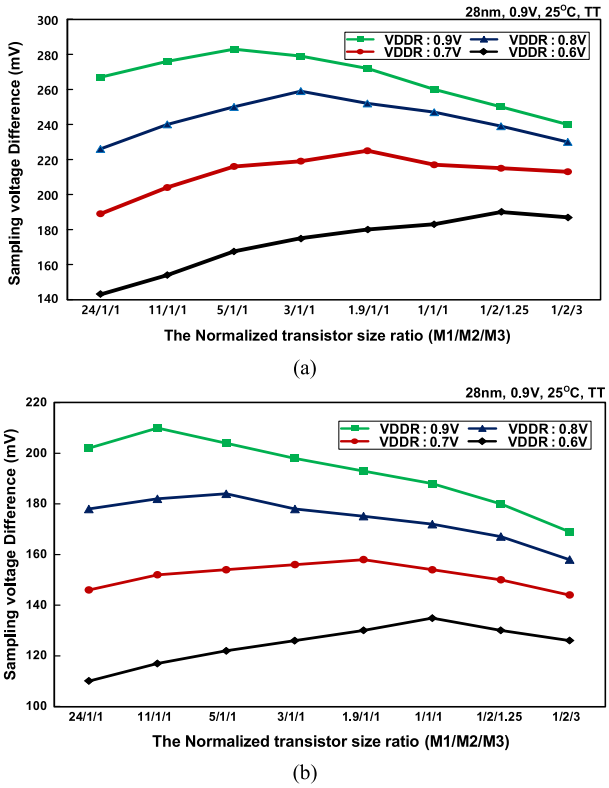
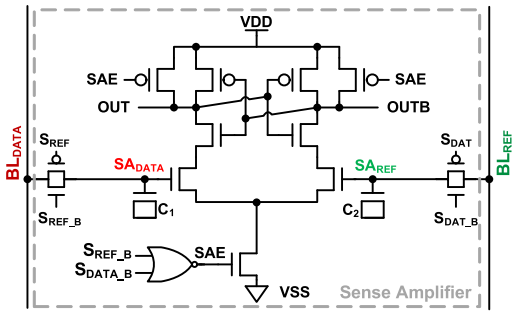


Fig. 10. The sampling voltage differences of (a) 'P' state and (b) 'AP' state with different the transistor size ratios and various VDDRs.

size ratios (M1/M2/M3) having large ΔV_{SA} are different depending on the data type on the target cell. When 0.9V of pre-charge voltage VDDR is used, 'AP' state has 210mV of ΔV_{SA} at 11/1/1 ratio, while 'P' state has 283mV of ΔV_{SA} at 5/1/1 ratio. Since 'AP' state has a relatively smaller ΔV_{SA} compared to 'P' due to (6), H1 and H2 should be designed such that large ΔV_{SA} in 'AP' state is observed to improve read reliability. With decreasing VDDR, ΔV_{SA} becomes smaller as well according to (6). In addition, the transistor size ratios (M1/M2/M3) where ΔV_{SA} is maximum, also is affected by VDDR. For example, when the VDDR is 0.7V, ΔV_{SA} of the 'AP' shows its largest of 158mV with (M1/M2/M3) of 1.9/1/1, while the largest ΔV_{SA} of the 'AP'state is 135mV with (M1/M2/M3) ratio of 1/1/1 when VDDR is 0.6V. As shown in Fig. 10, since the 'P' state shows relatively larger sampling voltage differences than the 'AP' state, TDD unit is designed such that it has the large sampling voltage difference on the 'AP' state. So, in order to guarantee a relatively large sensing margin, (M1/M2/M3) of 11/1/1 (5/1/1) is employed when VDDR is 0.9 V (0.8V), and (M1, M2, M3) of 1.9/1/1 (1/1/1) is employed when VDDR is 0.7 V (0.6V).

As a sense amplifier (SA) in our design, a voltage-latched sense amplifier [41] is adopted,which is shown in Fig. 11. Unlike the conventional sense amplifier enable (SAE) signal, which is enabled at a fixed time, SAE of the proposed DDDR scheme becomes active at varying time that is controlled by the TDD unit. Since SAE is the output of the NOR Gate which has S_{REF_B} and S_{DATA_B} as inputs, the sense amplifier operates immediately after all the sample and hold operations are completed on BLs. Fig. 12. (a) presents the layout of DDDR



S_{DATA}	S_{DATA_B}	S_{REF}	S_{REF_B}	Sample & Hold Complete voltage	SAE
0	1	0	1	-	0
1	0	0	1	SA_{REF}	0
0	1	1	0	SA_{DATA}	0
1	0	1	0	SA_{REF}, SA_{DATA}	1

Fig. 11. The Voltage-Latched sense amplifier with SAE signal under possible sampling conditions.

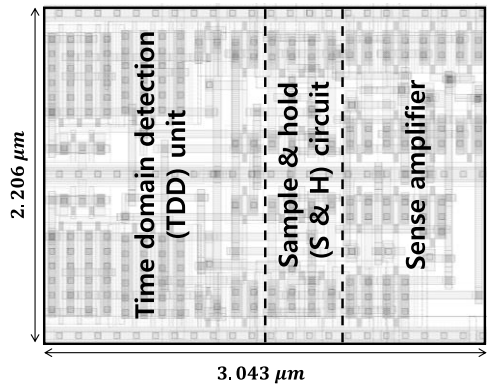


Fig. 12. The Layout of DDDR Sensing Circuit.

sensing circuit using 28nm CMOS technology. Considering one 2T-SOT-MRAM cell area drawn with the MRAM layout method [42], the proposed sensing circuit occupies only 0.34% of the 128 by 128 cell array area.

IV. Numerical Results and Comparisons

A. Simulation Setup

128 by 128 SOT MRAM macros with the proposed DDDR sensing scheme has been designed using 28nm CMOS process. The same size of SOT MRAM macros with the conventional VM_V and VM_T sensing schemes have been also designed for comparisons. The parameters of SOT device used in our simulations are summarized in Table I, where the SOT device model with perpendicular magnetic anisotropy is based on [43]. The tunnel magnetoresistance (TMR) ratio, which means the relative resistance difference between the 'AP' and 'P' states of an MTJ, is assumed 150%. In order to simulate the read bit error rates (BERs) of the read operations, 10K HSPICE Monte-Carlo simulations using the statistical models for both SOT devices and CMOS are performed under process variations. For SOT device, the area and thickness are assumed to have Gaussian distributions according to the experimental data in [44]. The variability of the SOT device resistance is assumed 5% with 1σ. The simulations are performed with 128 by 128 SOT-MRAM macro having 32 to 1 column MUX

TABLE I
SOT Device Parameter

Parameter	Value
Free layer dimension (nm^3)	70 × 70 × 0.6
Spin hall metal dimension (nm)	100, 70, 2 (length, width, thickness)
Spin hall metal resistivity (μΩ.cm) [19]	180
Spin hall angle [19]	0.3
Damping factor α [19]	0.5
Bias magnetic field (mT) [19]	30
Sat. magnetization (A/m)	1.0×10^6
TMR_0	150%
Nominal R_{MTJ} at P (AP) (Ω)	9 kΩ (22.5 k)
Variation in device dimension	5%
Switching current (Pulse-width)	77 μA (2 ns)

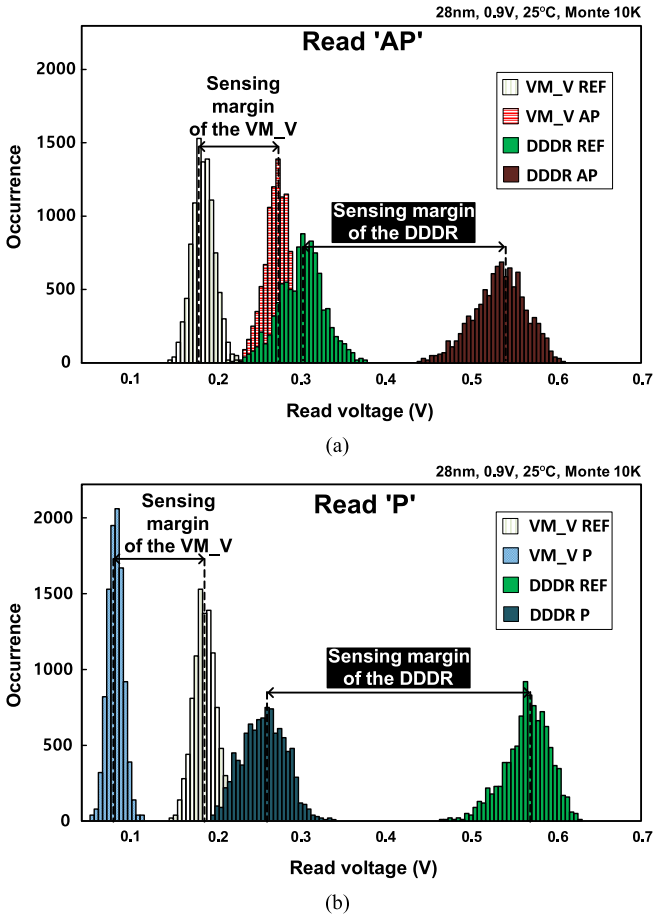


Fig. 13. The distributions of the read voltages obtained by 10k Monte-Carlo simulations for both the proposed and conventional sensing schemes in (a) The 'AP' state and (b) 'P' state.

using typical supply voltage of 0.9V. As previously presented in Fig. 2, SOT-MRAM cell inside the macro consists of two access transistors that are 2.5 times larger than the minimum channel width.

B. Sensing Margin Analysis

Fig. 13 illustrates the distributions of the read voltages obtained from 10K Monte-Carlo simulations for both of the proposed and conventional sensing schemes in the 'AP' and

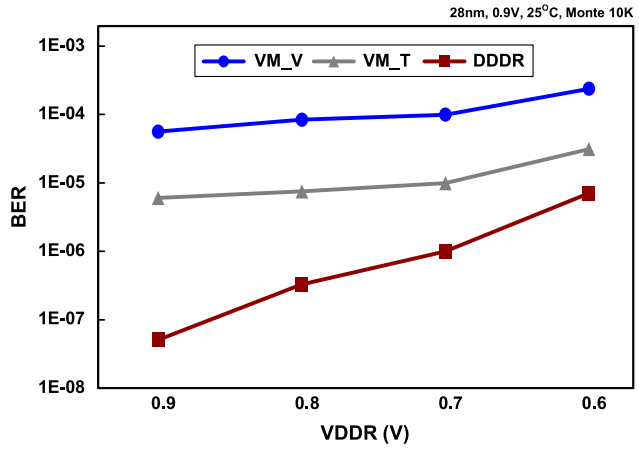


Fig. 14. The BERs of VM_V, VM_T, DDDR at various VDDRs.

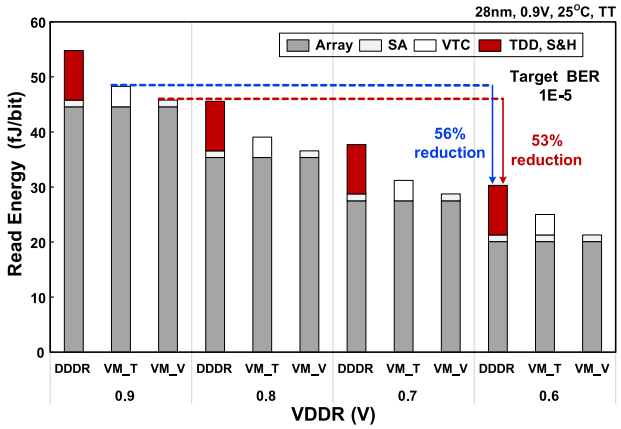


Fig. 15. The energy of VM_V, VM_T, DDDR at various VDDRs.

'P' states. The distributions of VM_V are extracted from BL at the time having the lowest read BER of 5.58E-5, which is obtained using (9) [28], [34], [35], [45]. The distributions of DDDR are extracted from the sampled voltages when V_t is set to 380mV. As shown in Fig. 13, although the fluctuations are slightly larger due to the variations of the TDD unit and the S&H circuits, the sensing margin of the proposed DDDR approach is much higher than that of the conventional scheme. The conventional sensing scheme shows an average sensing margin of 98.5mV, while the proposed scheme has more than 2× larger sensing margin of 243mV. As mentioned earlier, the larger the difference between the reference voltages for the 'P' ('AP') voltage, the more reliable the read operations can be provided.

C. Simulation Result

Based on Monte Carlo simulations, the read BER of each sensing scheme has been obtained. Here, the BERs have been obtained using the mean and standard deviation of sensing margin in (3), which are expressed as:

$$\mu_{SM} = \left|\mu_{V_{BL}} - \mu_{V_{REF}} - \mu_{V_{offset}}\right|, \tag{7}$$

$$\sigma_{SM} = \sqrt{\sigma^2_{V_{BL}} + \sigma^2_{V_{REF}} + \sigma^2_{V_{offset}}}, \tag{8}$$

where $\mu_{V_{BL}}$, $\mu_{V_{REF}}$, $\mu_{V_{offset}}$ are the mean values of $V_{BL,DATA}$, $V_{BL,REF}$, and V_{offset}, respectively, and $\sigma_{V_{BL}}$, $\sigma_{V_{REF}}$, $\sigma_{V_{offset}}$ mean the standard deviations of $V_{BL,DATA}$, $V_{BL,REF}$, and V_{offset}, respectively. $\mu_{V_{offset}}$ is typically set to zero [46], and it is assumed that the variations of V_{offset}, V_{REF}, V_{BL} are uncorrelated. Using the mean and standard deviation values, BER can be calculated as follows [28], [34], [35], [45]:

$$BER = \frac{1}{2} \times \left(1 + erf\left(-\frac{1}{\sqrt{2}} \frac{1}{\frac{\sigma_{SM}}{\mu_{SM}}}\right)\right), \tag{9}$$

where $erf(x)$ is the Gauss error function. According to (9), BER generally improves with smaller standard deviations and large mean values. For example, the σ_{SM}/μ_{SM} of 0.3 (0.2) leads to the BER of 4.2E-4 (2.87E-7).

Based on 10K Monte Carlo simulations, the BERs of various sensing approaches including VM_V, VM_T, DDDR with different VDDRs have been obtained, and Fig. 14 presents the simulation results. In the BER calculations, $\sigma_{V_{offset}}$ and $\sigma_{T_{offset}}$ are set to 10mV and 0.14ns, respectively, which are obtained from the simulation results of the sense amplifier and the voltage to time converter (VTC) that are designed with the same area [27]. As shown in Fig. 14, thanks to the higher sensing margin, the proposed DDDR sensing shows much lower BERs than the conventional schemes in all VDDRs. The DDDR scheme has the BER of 5.08E-8 at 0.9V and that of 7.03E-6 at 0.6V. As VDDR decreases, the BERs of all the sensing schemes increases with decreasing μ_{SM}. The BER of

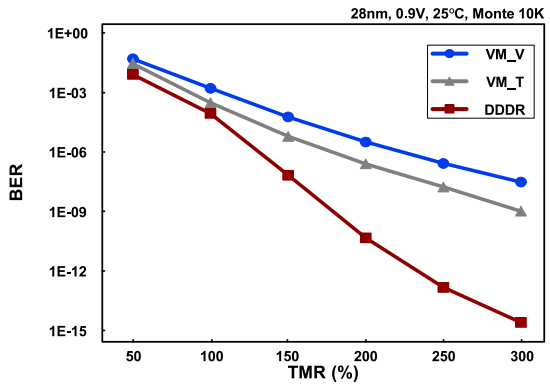


Fig. 16. The BERs of VM_V, VM_T, DDDR with varying TMR ratios.

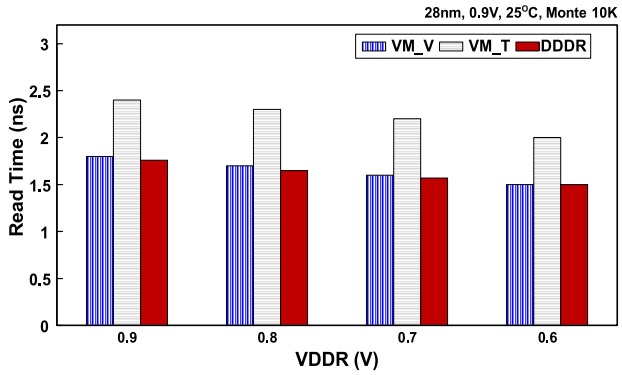


Fig. 17. The read speed of VM_V, VM_T, DDDR at various VDDRs.

TABLE II
COMPARISONS AMONG VARIOUS SENSING SCHEMES

	VM_V	VM_T	OCTS [24]	DDRS [25]	ST-VSS [27]	SMCR [28]	This work		
Feature	-	-	Offset Cancellation , Dual-reference	Dynamic dual reference	BIST, Cyclic double SA	Dual-reference	Dual domain , Dynamic reference		
CMOS Technology	28nm	28nm	45nm	40nm	28nm	28nm	28nm		
Mode	Voltage mode	Voltage mode	Current mode	Current mode	Voltage mode	Voltage mode	Voltage mode		
VDDR (V)	0.9	0.9	1.0	1.0	0.9	0.9	0.9	0.9	0.6
Variability of MTJ (%)	5	5	4	5	5	5	4	5	5
BER	5.58E-5	6.02E-6	9.86E-10	9.75E-2	1.95E-5	6.48E-8	7.12E-10	6.08E-8	7.03E-6
Read Energy (fJ/bit)	45.8	48.3	395.5	77	136.1	81.9	54.8		30.3
Read time (ns)	1.8	2.4	6.4	2.3	1.2	1.6	1.76		1.5

DDDR sensing at 0.6V is still less than 1E-5, which is lower than or similar to those of other schemes at 0.9V.

Since the DDDR sensing scheme shows lower BER, VDDR can be lowered down as long as the target BER is satisfied. So, we perform the energy simulations of 128 by 128 SOT MRAM macros by reducing VDDR of the DDDR, VM_V, and VM_T sensing schemes. Fig. 15 shows the energy simulations with different VDDRs. In the simulations, the energy consumed only in the cell array and sensing circuits is considered, excluding the energy consumed in peripheral circuits such as decoders and timing circuits, which can be designed in different ways. The array energy that is needed to pre-charge BL is same for different sensing schemes, but the energy consumed from the following BL develop stage varies depending on which sensing scheme is used. As shown in Fig. 15, DDDR sensing consumes larger read energy than other schemes at the same VDDR due to TDD unit and sense amplifier. However, since the array energy takes a significant portion of the read energy and reducing VDDR considerably reduces the array energy, the total read energy of DDDR scheme is reduced by 45 % by reducing VDDR from 0.9V to 0.6V under the target BER of 1E-5.

Changing TMR ratio ($=((R_{AP} - R_P)/ R_P) \times 100$) also has a large effect on read BER. Fig. 16 shows the BER changes with varying TMR ratio. As shown in the figure, BER decreases with increasing TMR as increasing $\Delta R(= |R_{DATA} - R_{REF}|)$ leads to sensing margin increase according to (3), (4), (6). As presented in Fig. 16, the proposed DDDR sensing shows lower BERs compared to the conventional sensing schemes. The difference is not noticeable at low TMR, but it is getting much larger at high TMR, which is because the dynamic reference created with very small BL voltage differences does not have a significant effect at low TMR. At the highest TMR of 300%, BER of VM_V and VM_T are 3.00E-8 and 1.02E-9 respectively, while that of DDDR reaches 2.50E-15.

Fig. 17 also presents the read speed comparisons of various sensing schemes with varying VDDR. In the figure, read time means the read time from the activating RWL to data out. As presented in Fig. 17, VM_T shows the longest read delay since it should wait for BL to be discharged to low threshold voltage V_t. The DDDR approach shows the read delay of 1.5ns to 1.76ns from VDDR of 0.6V to 0.9V, respectively, which are similar or slightly shorter than those of VM_V sensing. Please note that when the faster read operation is needed, V_t can be increased. However, increasing V_t results in decreasing sensing margin.

Table II shows the comparisons of the DDDR sensing scheme with different previous works [24], [25], [27], [28] in terms of BER, read energy, read time. In offset canceling triple stage (OCTS) sensing [24], the read operations are performed in current mode by continuously flowing a read current. BER is greatly improved with OCTS sensing, but increasing read time incurs large energy consumption due to additional phase for offset canceling. The dual dynamic reference sensing (DDRS) [25] show a relatively large read BER with low energy consumption. With increasing read delay, lower read BER can be achieved at the expense of considerably large read energy consumption. The read operations in the self-timed voltage mode sensing (ST-VSS) [27] and the self-matching complementary reference (SMCR) sensing [28] are performed in voltage modes. ST-VSS shows relatively large read energy consumption due to the detection flag circuits and the periodic sense amplifiers operation. An additional phase is also needed to measure the offset of the sense amplifier using built in static test (BIST) before read operations. In SMCR, lower BER is achieved by adopting dual references, but read energy increases as the number of charged bit lines increases as well. The proposed DDDR sensing shows the lowest BER among all other sensing scheme without large energy overhead since it creates a dynamic reference by utilizing a simple sampling method in the dual domain. Even with VDDR scaling down to 0.6V, the read BER of 7.03E-6 BER is observed with much smaller read energy consumption.

V. CONCLUSION

In this paper, we present a dual-domain dynamic reference (DDDR) sensing scheme that can provides reliable read operations with short read delays in SOT-MRAM. The main feature of the proposed scheme is to sample the dynamically changing reference voltages depending on the data stored in

a target cell by using dual domains. The half Schmitt trigger based time domain detection (TDD) unit and sample and hold (S & H) circuits are also efficiently exploited to design the dynamic reference approach. The proposed DDDR sensing achieves almost two times larger sensing margin compared to the conventional schemes. In addition, since the proposed sensing does not need an additional phase and it takes a shorter bit-line (BL) discharge time to sample a proper voltage difference, read delay is not affected. Compared to the conventional voltage mode in voltage domain sensing and voltage mode in time domain sensing, more than 100 times lower read BER has been obtained with the same read delays. The idea presented in this paper can assist the SOT-MRAM design and implementation for reliable and low-power applications. In addition, the proposed sensing scheme can be applied to various nonvolatile resistive memories.

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