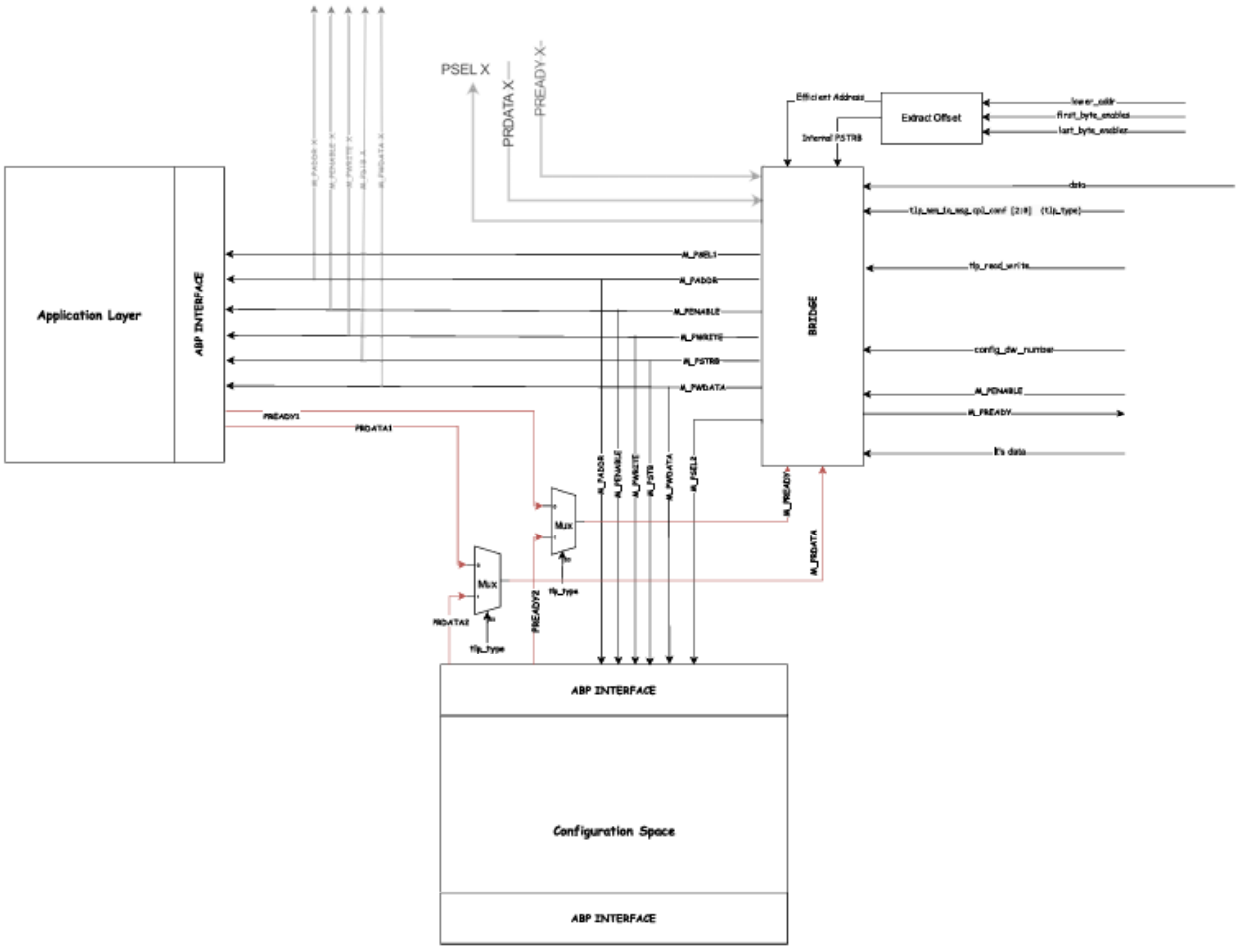
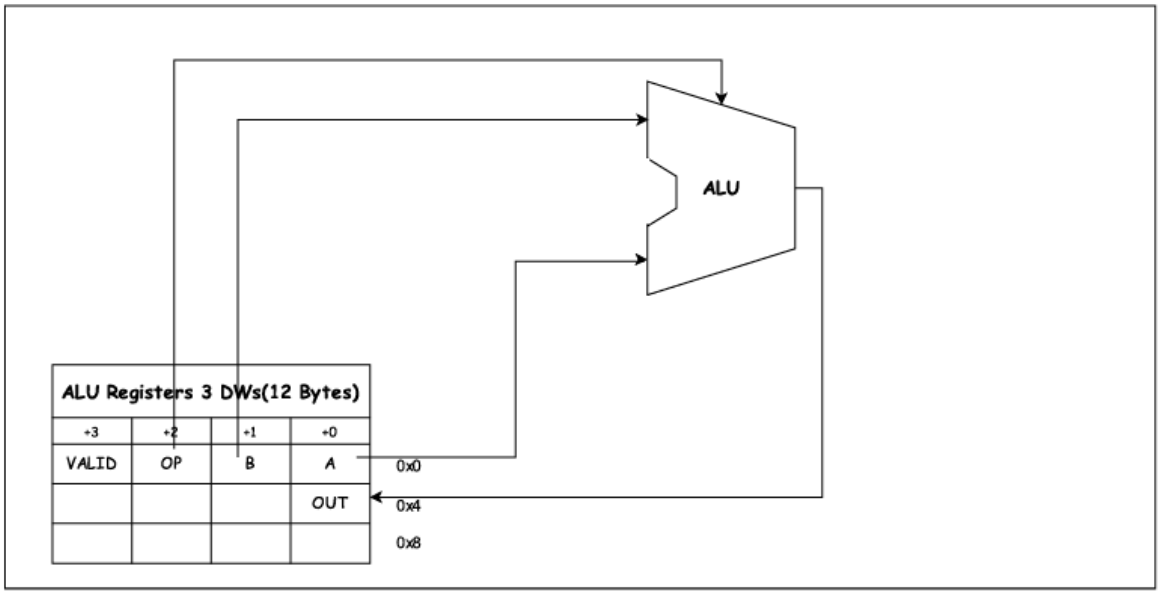
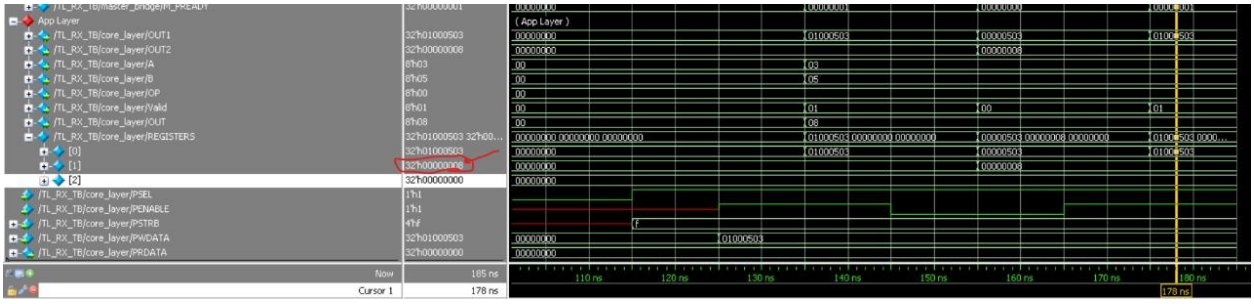

PSEL X
PRDATA X
PREADY X
Application Layer
ABP INTERFACE
Effiicient Address
Extract Offset
lower_addr
first_byte_enables
last_byte_enables
Internal PSTRB
BRIDGE
data
tlp_sent_to_reg_cpl_conf [2:0] {tlp_type}
tlp_read_write
config_dw_number
M_PENABLE
M_PREADY
It's data
M_PSEL1
M_PADDR
M_PENABLE
M_PWRITE
M_PSTRB
M_PWDATA
PREADY1
PRDATA1
Mux
Mux
tlp_type
tlp_type
PRDATA2
PREADY2
M_PREADY
M_PRDATA
ABP INTERFACE
Configuration Space
ABP INTERFACE

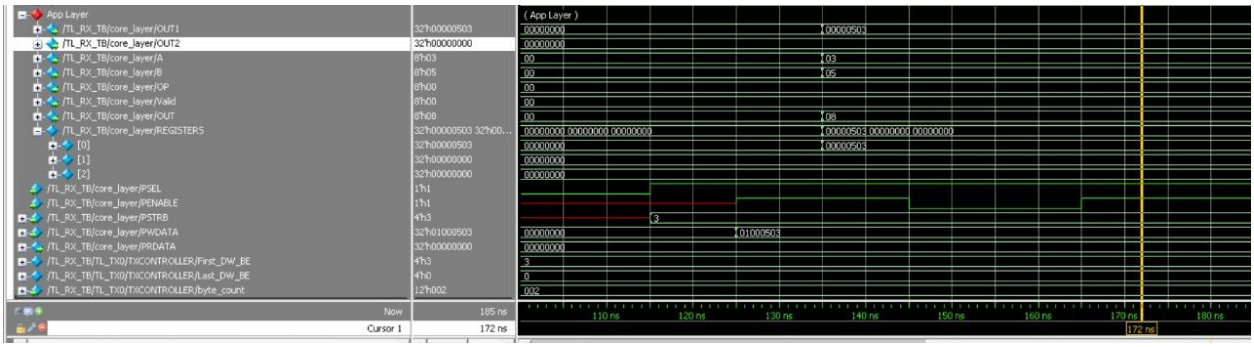

ALU
ALU Registers 3 DWs(12 Bytes)
+3
+2
+1
+0
VALID
OP
B
A
OUT
0x0
0x4
0x8

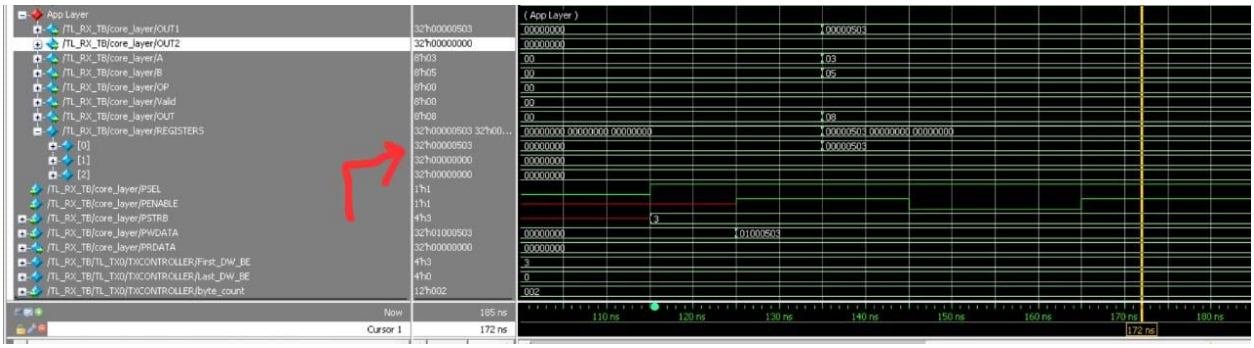
APB_ALU.sv | MASTER_BRIDGE.sv | TL_RX_DECODER.sv | TL_RX_TB.sv | PNPC_BUFF.sv | DUO_BUFFER.sv | TL_TX_TB.sv | TL_TX.sv

Test1 > TL_RX_TB.sv

```
357
358  initial begin
359      rst <= 0;
360      //RD_EN <= 0;
361      //(1) ###################### NON-POSTED 2-BYTES 32-BIT IO READ TLP ##########################
362      @(posedge clk)
363      rst <= 1;
364     //(2) ############### POSTED MEMORY 2-BYTES 32-BIT MEMORY WRITE TLP ##########################
365      @(posedge clk)
366      tlp_mem_io_msg_cpl_conf <= 0;     //0: memory, 1: io, 2: completion
367      tlp_address_32_64  <= 0;     //0: 32-bit, 1: 64-bit
368      tlp_read_write     <= 1;     //0: read, 1: write
369
370      //Number Of Written Bytes
371      byte_count <= 2;
372
373      //Destination
374      lower_addr <= 32'h0000_0000;
375      upper_addr <= 32'h0000_0000;
376
377      dest_bdf_id <= 16'h0000;
378      config_dw_number <= 10'd0;
379
380      data <= 32'h0100_0503;
381
382      valid <= 1;         //Initiate Transaction Generation FSM
383
384      @(posedge clk)      //Store All These Signals In Their Registers.
385
386      // #### 3 DW Header, 1 DW Data ####
387      @(posedge clk)      // IDLE => H0
388      valid <= 0;
389      repeat(5)           // H0 => H1_REQ => H_ADDR32 => DATA => FINISH => IDLE
390      begin
391          @(posedge clk);
392      end
```




App Layer
/TL_RX_TB/core_layer/OUT1
/TL_RX_TB/core_layer/OUT2
/TL_RX_TB/core_layer/A
/TL_RX_TB/core_layer/B
/TL_RX_TB/core_layer/OP
/TL_RX_TB/core_layer/Valid
/TL_RX_TB/core_layer/OUT
/TL_RX_TB/core_layer/REGISTERS
[0]
[1]
[2]
/TL_RX_TB/core_layer/PSEL
/TL_RX_TB/core_layer/PENABLE
/TL_RX_TB/core_layer/PSTRB
/TL_RX_TB/core_layer/PWDATA
/TL_RX_TB/core_layer/PRDATA
/TL_RX_TB/TL_TX0/TXCONTROLLER/First_DW_BE
/TL_RX_TB/TL_TX0/TXCONTROLLER/Last_DW_BE
/TL_RX_TB/TL_TX0/TXCONTROLLER/byte_count
32'h00000503
32'h00000000
8'h03
8'h05
8'h00
8'h00
8'h08
32'h00000503 32'h00...
32'h00000503
32'h00000000
32'h00000000
1'h1
1'h1
4'h3
32'h01000503
32'h00000000
4'h3
4'h0
12'h002
Now
185 ns
Cursor 1
172 ns
(App Layer)
110 ns
120 ns
130 ns
140 ns
150 ns
160 ns
170 ns
180 ns
172 ns


App Layer
/TL_RX_TB/core_layer/OUT1
/TL_RX_TB/core_layer/OUT2
/TL_RX_TB/core_layer/A
/TL_RX_TB/core_layer/B
/TL_RX_TB/core_layer/OP
/TL_RX_TB/core_layer/Valid
/TL_RX_TB/core_layer/OUT
/TL_RX_TB/core_layer/REGISTERS
[0]
[1]
[2]
/TL_RX_TB/core_layer/PSEL
/TL_RX_TB/core_layer/PENABLE
/TL_RX_TB/core_layer/PSTRB
/TL_RX_TB/core_layer/PWDATA
/TL_RX_TB/core_layer/PRDATA
/TL_RX_TB/TL_TX0/TXCONTROLLER/First_DW_BE
/TL_RX_TB/TL_TX0/TXCONTROLLER/Last_DW_BE
/TL_RX_TB/TL_TX0/TXCONTROLLER/byte_count
32'h00000503
32'h00000000
8'h03
8'h05
8'h00
8'h00
8'h08
32'h00000503 32'h00...
32'h00000503
32'h00000000
32'h00000000
1'h1
1'h1
4'h3
32'h01000503
32'h00000000
4'h3
4'h0
12'h002
Now
185 ns
Cursor 1
172 ns
(App Layer)
110 ns
120 ns
130 ns
140 ns
150 ns
160 ns
170 ns
180 ns
172 ns