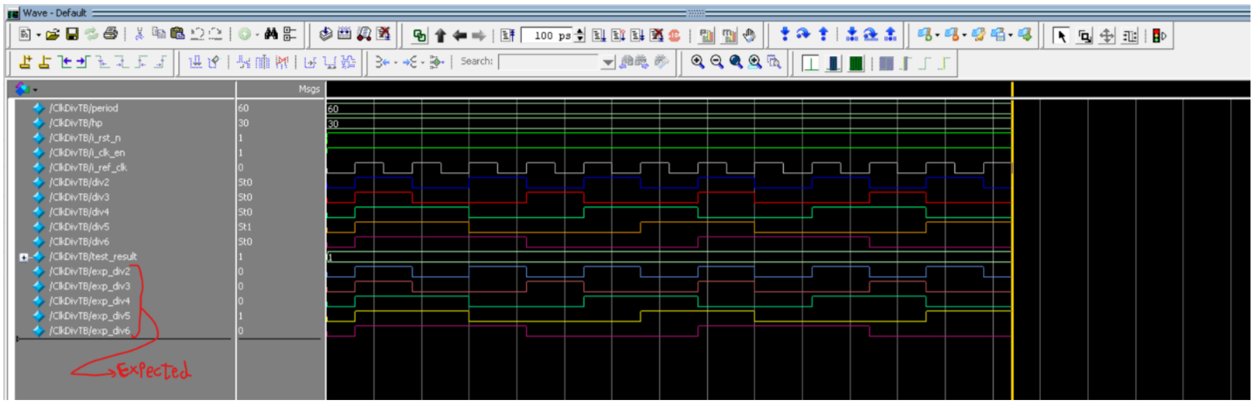
Waveform:



Testbench Log:

```
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Div2 Clock Matches The Expected Output
# Div3 Clock Matches The Expected Output
# Div4 Clock Matches The Expected Output
# Div5 Clock Matches The Expected Output
# Div6 Clock Matches The Expected Output
# Clock Divider Operate Fine at all Dividing Ratios
# Break in Module ClkDivTB at C:/Users/amrel/Desktop/Diploma/Systems/ClockDivider/ClkDivTB.v line 208
VSIM 91> run -over
# Next activity is in 30 ns.

VSIM 92>
```

Simulating Expected Signals:

```
102  initial
103  begin
104      @(posedge i_ref_clk);
105      fork
106
107      forever begin
108          #(hp*2) exp_div2= ~exp_div2;
109        //#(hp*2) exp_div2= ~exp_div2; (optional)
110      end
111
112      forever begin
113
114          #(hp*2) exp_div3= ~exp_div3;
115          #(hp*2 + hp*2) exp_div3= ~exp_div3;
116      end
117
118      forever begin
119
120          #(hp*4) exp_div4= ~exp_div4;
121        //#(hp*4) exp_div4= ~exp_div4; (optional)
122      end
123
124      forever begin
125
126          #(hp*4) exp_div5= ~exp_div5;
127          #(hp*4 + hp*2) exp_div5= ~exp_div5;
128      end
129
130      forever begin
131
```

hp: half period = period/2

Test Cases

```
                /////////////////////////////////////////
               /////////////////////////////////////////
              ///////////                ///////////////
  ///////////////////////   Initial     //////////////////////////////
 ///////////////////////               //////////////////////////////
///////////////////////     Block     //////////////////////////////
           ///////////                ///////////////
          /////////////////////////////////////////
         /////////////////////////////////////////
integer test_result=1;
initial
begin
    i_rst_n = 0;
    #(i_rst_n/100) i_rst_n =1;
    i_ref_clk=0;

    i_clk_en=1;

    repeat(12)
    begin
        @(negedge i_ref_clk);
        if(div2 != exp_div2)
        begin
            test_result=0;
            $display("Div2 Failed!");
        end
        else
            $display("Div2 Clock Matches The Expected Output");

        if(div3 != exp_div3)
        begin
            test_result=0;
            $display("Div3 Failed!");
        end
        else
            $display("Div3 Clock Matches The Expected Output");

        if(div4 != exp_div4)
        begin
            test_result=0;
            $display("Div4 Failed!");
        end
```