4 bit full adder

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2. **4-Bit Full Adder Design**
   I. **Carry ripple**
   II. **Carry look ahead**
3. **Conclusion**

Introduction

- **A 4-bit full adder is a fundamental digital circuit that performs the addition of two 4-bit binary numbers and produces a sum along with a carry-out.**

- **It forms the building block for more complex arithmetic units in digital systems.**

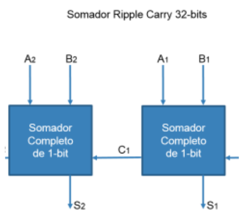
Introduction

- **Two common methods for designing a 4-bit full adder are the carry ripple adder and the carry look-ahead adder.**

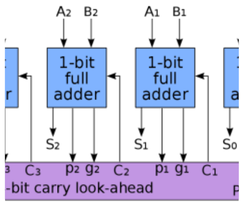
- **These methods differ in their approach to generating the carry signals, impacting the overall speed and efficiency of the addition process.**

Introduction

4 bit full adder


Somador Ripple Carry 32-bits
A2
B2
A1
B1
Somador Completo de 1-bit
C1
Somador Completo de 1-bit
S2
S1

Carry Ripple Adder



Carry Look-Ahead Adder

Introduction

1. Carry Ripple Adder:

- **The carry ripple adder is a straightforward approach to designing a full adder.**

- **It relies on a cascaded arrangement of full adder cells, where the carry-out of one stage serves as the carry-in for the next stage.**

Introduction

1. **Carry Ripple Adder:**

- **While conceptually simple, the carry ripple adder's drawback is that the addition process is sequential, leading to a linear increase in propagation delay with the number of bits.**

- **As a result, this method may not be optimal for high-speed applications where quick computation is essential.**

Introduction

2. Carry Look-Ahead Adder:

- **In contrast, the carry look-ahead adder is designed to overcome the sequential nature of the carry ripple adder, providing a more efficient solution for parallel addition.**

- **This method utilizes additional logic to compute the carry-out signals for all stages simultaneously, eliminating the need for a ripple carry.**

Introduction

2. **Carry Look-Ahead Adder:**

By doing so, the carry look-ahead adder reduces the propagation delay associated with the carry generation, making it more suitable for applications requiring high-speed arithmetic operations.

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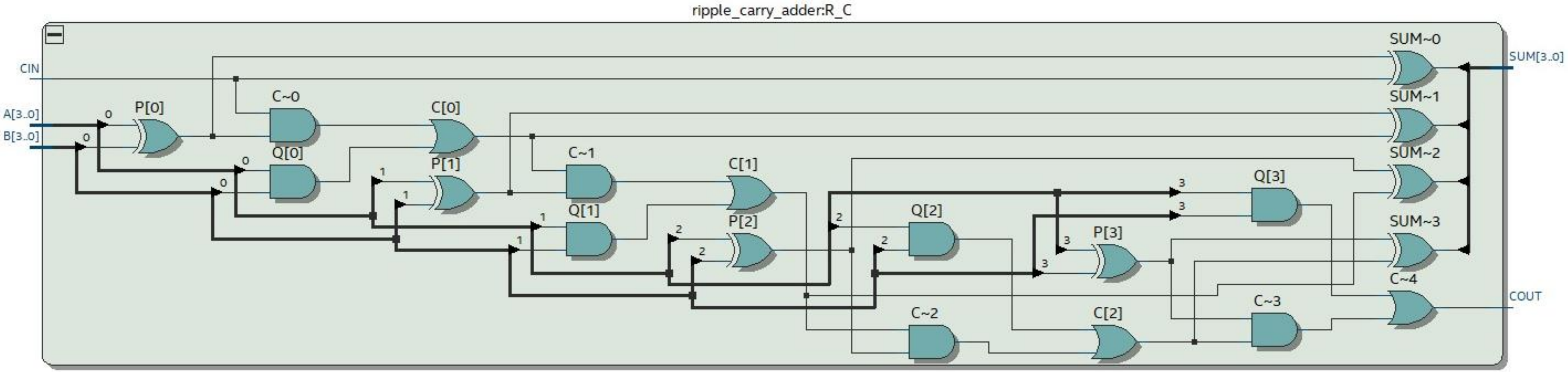
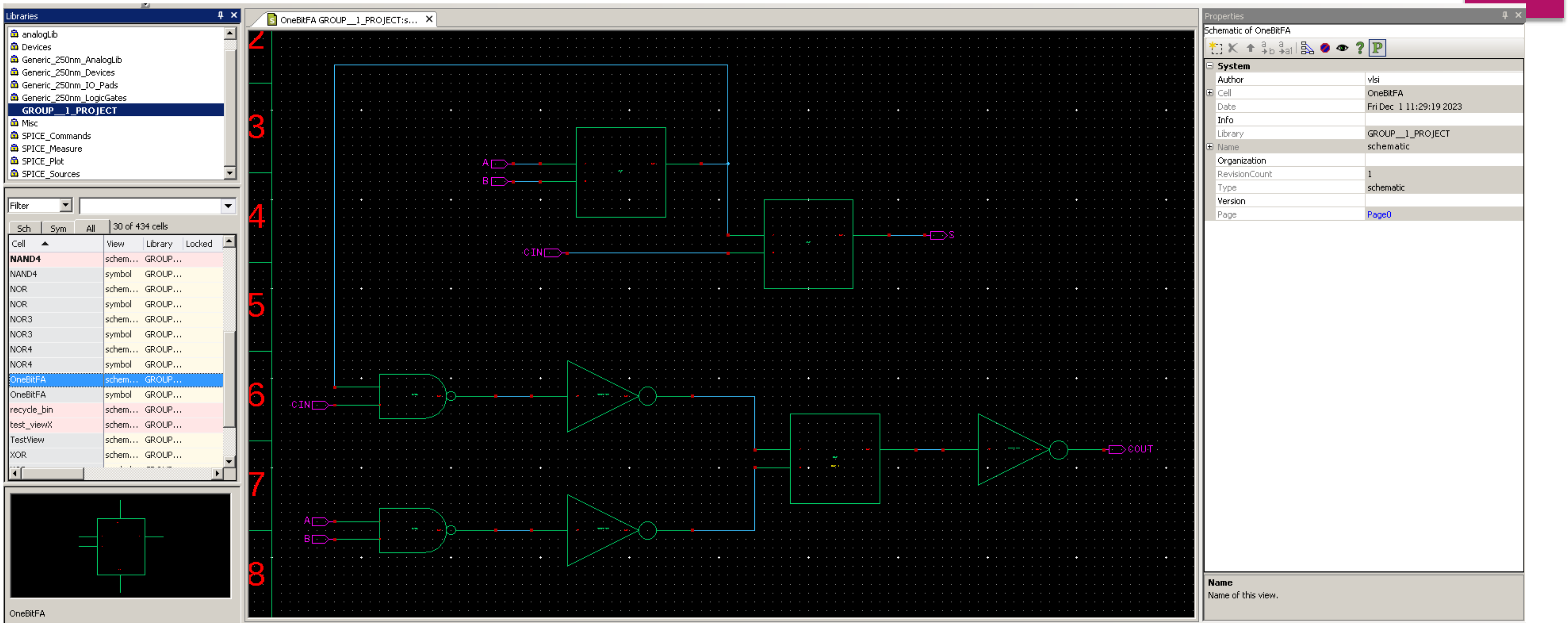
2. **4-Bit Full Adder Design**
   I. **Carry ripple**
   II. Carry look ahead
3. Conclusion
4. Questions

4-Bit Full Adder Design Net List



4 bit full adder Carry ripple Net List

4-Bit Full Adder Design Schematic



Libraries

- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- GROUP__1_PROJECT
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch Sym All 30 of 434 cells

Cell	View	Library	Locked
NAND4	schem...	GROUP...	
NAND4	symbol	GROUP...	
NOR	schem...	GROUP...	
NOR	symbol	GROUP...	
NOR3	schem...	GROUP...	
NOR3	symbol	GROUP...	
NOR4	schem...	GROUP...	
NOR4	symbol	GROUP...	
OneBitFA	schem...	GROUP...	
OneBitFA	symbol	GROUP...	
recycle_bin	schem...	GROUP...	
test_viewX	schem...	GROUP...	
TestView	schem...	GROUP...	
XOR	schem...	GROUP...	

OneBitFA

OneBitFA GROUP__1_PROJECT:s...

Properties

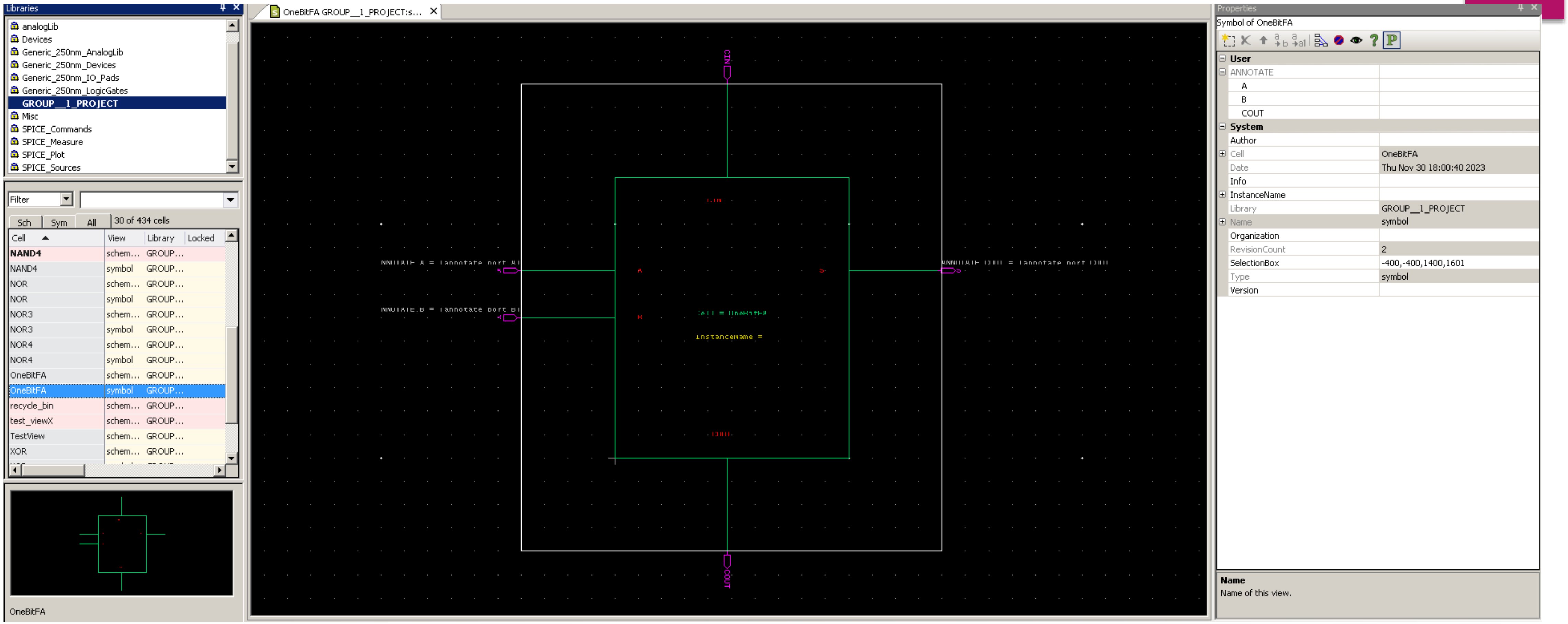
Schematic of OneBitFA

System	
Author	vlsi
Cell	OneBitFA
Date	Fri Dec 1 11:29:19 2023
Info	
Library	GROUP__1_PROJECT
Name	schematic
Organization	
RevisionCount	1
Type	schematic
Version	
Page	Page0

Name
Name of this view.

1 bit full adder Carry ripple schematic

4-Bit Full Adder Design Schematic



Libraries

- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- GROUP__1_PROJECT
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch | Sym | All | 30 of 434 cells

Cell	View	Library	Locked
NAND4	schem…	GROUP…	
NAND4	symbol	GROUP…	
NOR	schem…	GROUP…	
NOR	symbol	GROUP…	
NOR3	schem…	GROUP…	
NOR3	symbol	GROUP…	
NOR4	schem…	GROUP…	
NOR4	symbol	GROUP…	
OneBitFA	schem…	GROUP…	
OneBitFA	symbol	GROUP…	
recycle_bin	schem…	GROUP…	
test_viewX	schem…	GROUP…	
TestView	schem…	GROUP…	
XOR	schem…	GROUP…	

OneBitFA

OneBitFA GROUP__1_PROJECT:s…

CIN
ANNOTATE.A = {annotate port A}
ANNOTATE.B = {annotate port B}
ANNOTATE.COUT = {annotate port COUT}
CIN
A
B
S
Cell = OneBitFA
InstanceName =
COUT
COUT

Properties

Symbol of OneBitFA

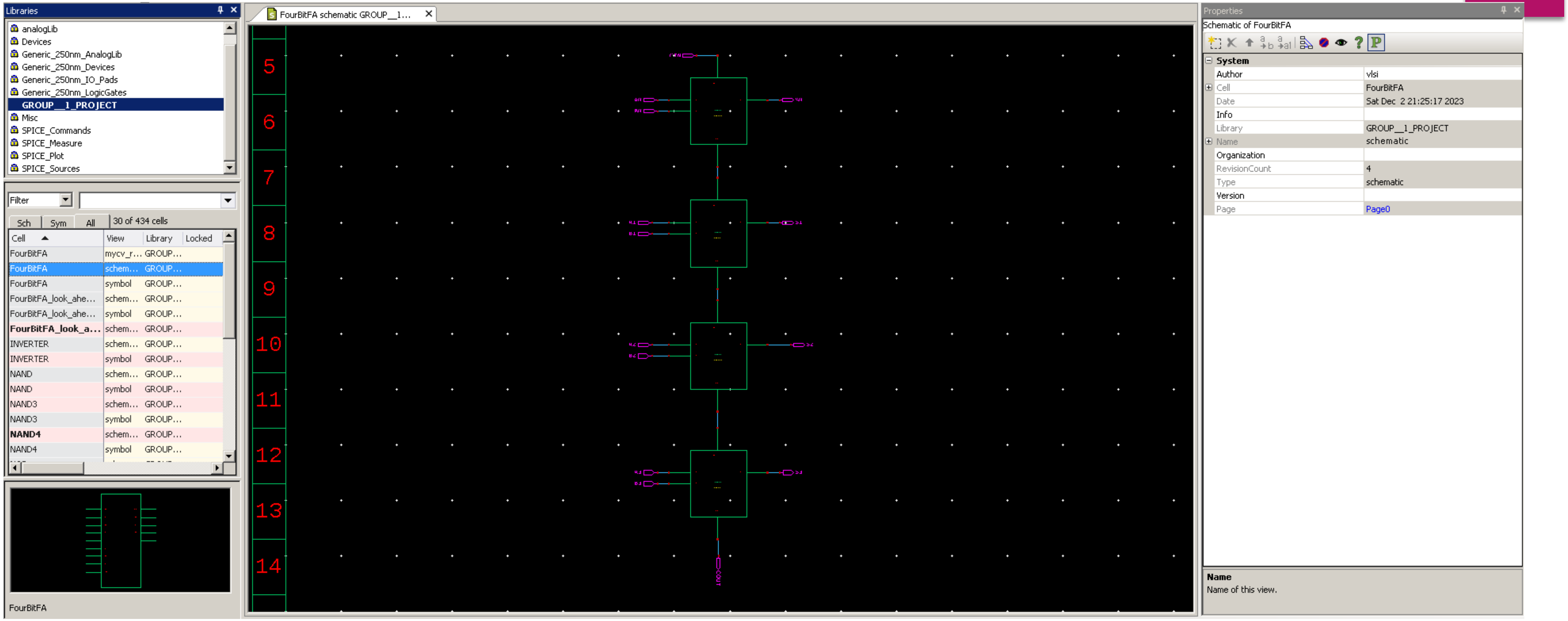
Property	Value
User	
ANNOTATE	
A	
B	
COUT	
System	
Author	
Cell	OneBitFA
Date	Thu Nov 30 18:00:40 2023
Info	
InstanceName	
Library	GROUP__1_PROJECT
Name	symbol
Organization	
RevisionCount	2
SelectionBox	-400,-400,1400,1601
Type	symbol
Version	

Name

Name of this view.

1 bit full adder Carry ripple symbol

4-Bit Full Adder Design Schematic



Libraries

- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- GROUP__1_PROJECT
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch | Sym | All — 30 of 434 cells

Cell	View	Library	Locked
FourBitFA	mycv_r…	GROUP…	
FourBitFA	schem…	GROUP…	
FourBitFA	symbol	GROUP…	
FourBitFA_look_ahe…	schem…	GROUP…	
FourBitFA_look_ahe…	symbol	GROUP…	
FourBitFA_look_a…	schem…	GROUP…	
INVERTER	schem…	GROUP…	
INVERTER	symbol	GROUP…	
NAND	schem…	GROUP…	
NAND	symbol	GROUP…	
NAND3	schem…	GROUP…	
NAND3	symbol	GROUP…	
NAND4	schem…	GROUP…	
NAND4	symbol	GROUP…	

FourBitFA

FourBitFA schematic GROUP__1…

Properties

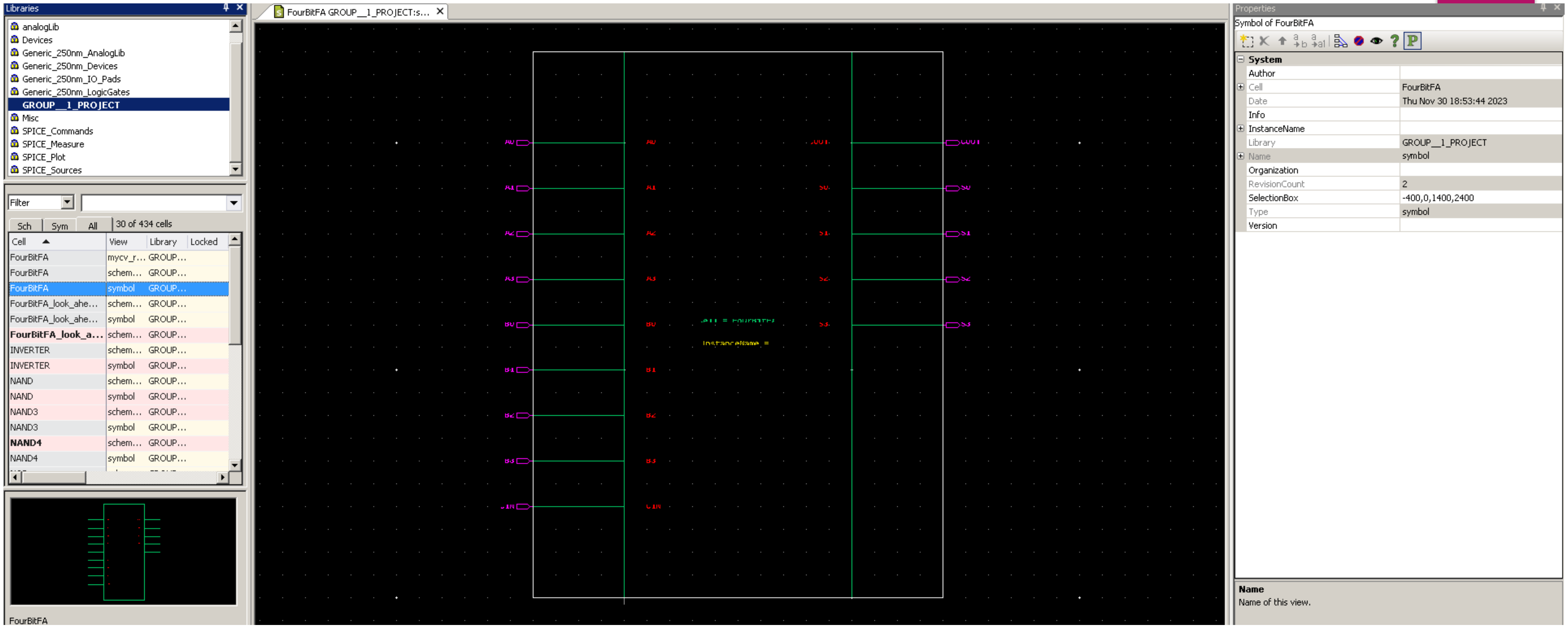
Schematic of FourBitFA

System	
Author	vlsi
Cell	FourBitFA
Date	Sat Dec 2 21:25:17 2023
Info	
Library	GROUP__1_PROJECT
Name	schematic
Organization	
RevisionCount	4
Type	schematic
Version	
Page	Page0

Name
Name of this view.

4 bit full adder Carry ripple schematic

4-Bit Full Adder Design Schematic



Libraries

- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- **GROUP__1_PROJECT**
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch | Sym | All | 30 of 434 cells

Cell	View	Library	Locked
FourBitFA	mycv_r...	GROUP...	
FourBitFA	schem...	GROUP...	
FourBitFA	symbol	GROUP...	
FourBitFA_look_ahe...	schem...	GROUP...	
FourBitFA_look_ahe...	symbol	GROUP...	
FourBitFA_look_a...	schem...	GROUP...	
INVERTER	schem...	GROUP...	
INVERTER	symbol	GROUP...	
NAND	schem...	GROUP...	
NAND	symbol	GROUP...	
NAND3	schem...	GROUP...	
NAND3	symbol	GROUP...	
NAND4	schem...	GROUP...	
NAND4	symbol	GROUP...	

FourBitFA

FourBitFA GROUP__1_PROJECT:s...

Properties

Symbol of FourBitFA

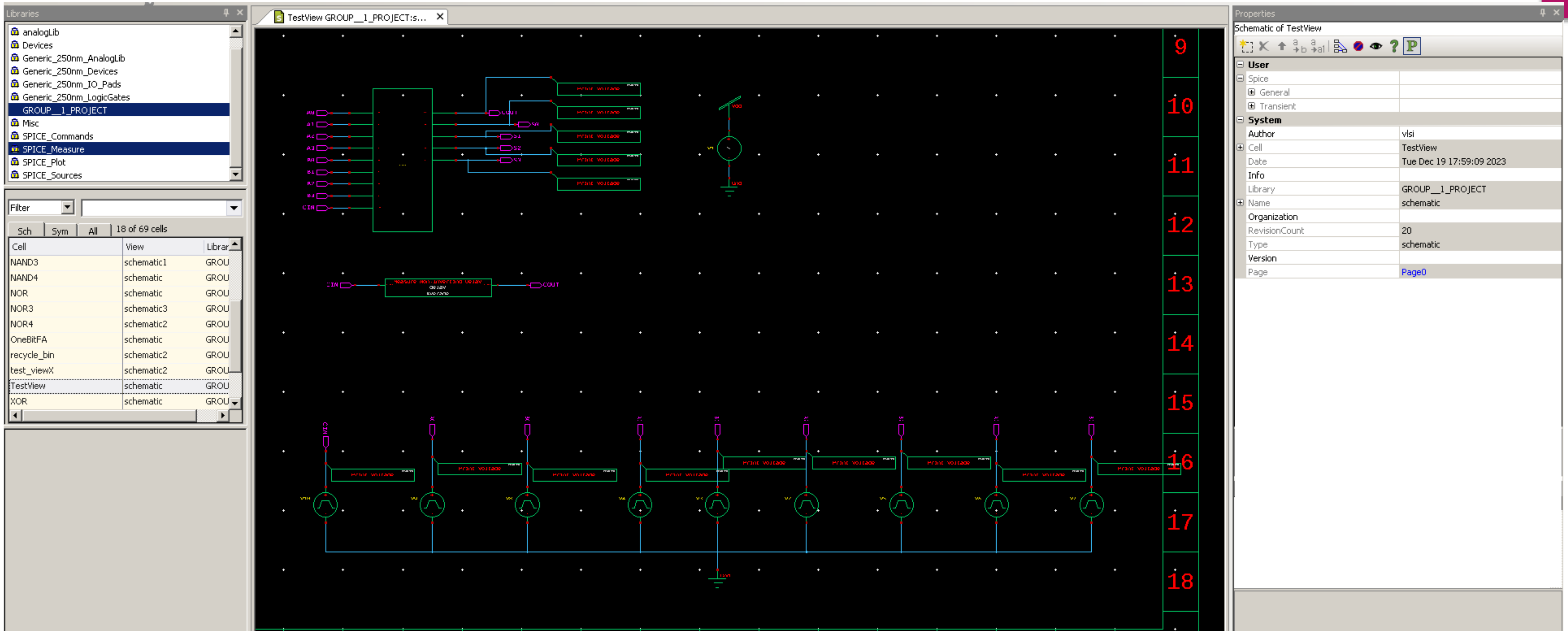
System	
Author	
Cell	FourBitFA
Date	Thu Nov 30 18:53:44 2023
Info	
InstanceName	
Library	GROUP__1_PROJECT
Name	symbol
Organization	
RevisionCount	2
SelectionBox	-400,0,1400,2400
Type	symbol
Version	

Name

Name of this view.

4 bit full adder Carry ripple symbol

4-Bit Full Adder Design Schematic



Libraries

- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- GROUP__1_PROJECT
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch Sym All 18 of 69 cells

Cell	View	Librar
NAND3	schematic1	GROU
NAND4	schematic	GROU
NOR	schematic	GROU
NOR3	schematic3	GROU
NOR4	schematic2	GROU
OneBitFA	schematic	GROU
recycle_bin	schematic2	GROU
test_viewX	schematic2	GROU
TestView	schematic	GROU
XOR	schematic	GROU

TestView GROUP__1_PROJECT:s...

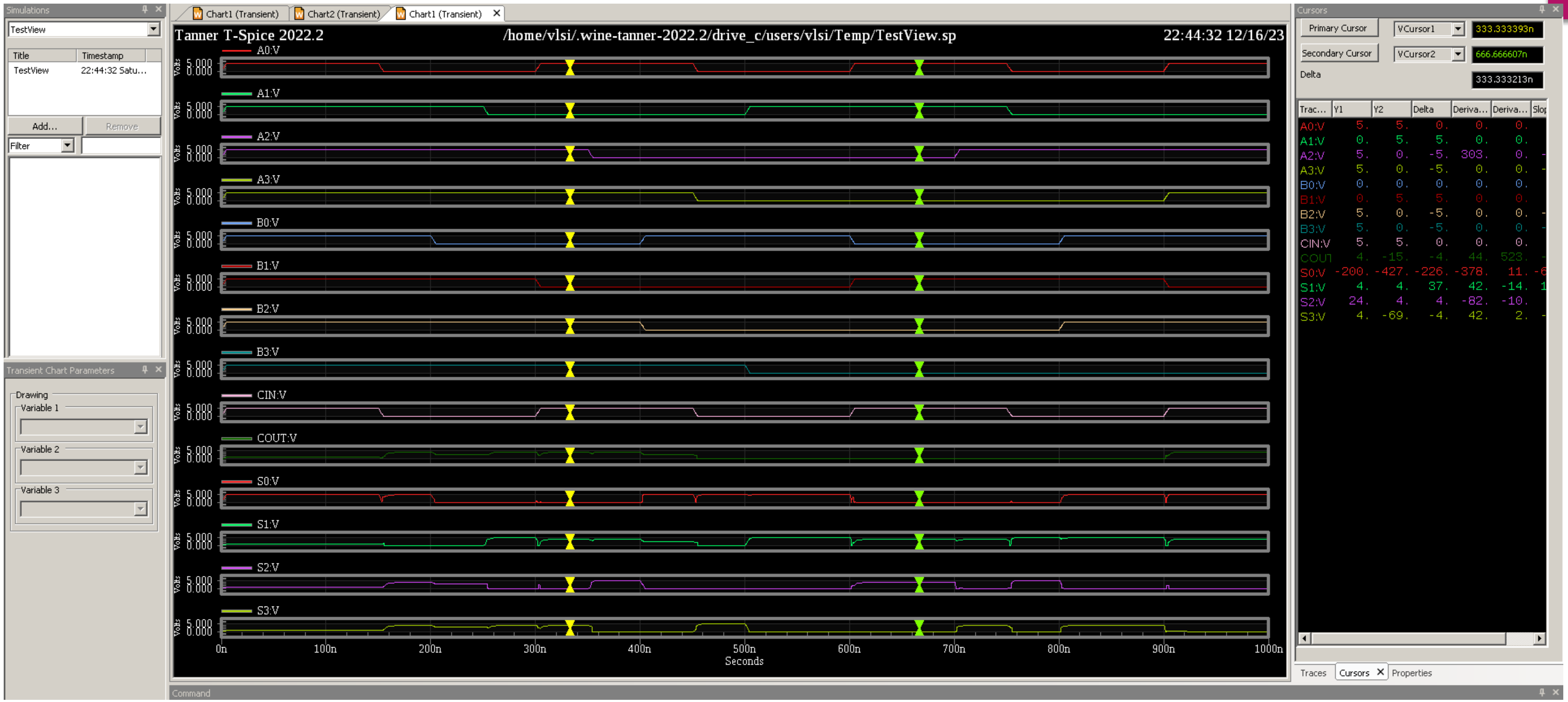
Properties

Schematic of TestView

User	
Spice	
General	
Transient	
System	
Author	vlsi
Cell	TestView
Date	Tue Dec 19 17:59:09 2023
Info	
Library	GROUP__1_PROJECT
Name	schematic
Organization	
RevisionCount	20
Type	schematic
Version	
Page	Page0

4 bit full adder Carry ripple test bench

4-Bit Full Adder Design wave



Title	Timestamp
TestView	22:44:32 Satu...

Tanner T-Spice 2022.2 /home/vlsi/.wine-tanner-2022.2/drive_c/users/vlsi/Temp/TestView.sp 22:44:32 12/16/23

Cursors

Primary Cursor VCursor1 333.333393n

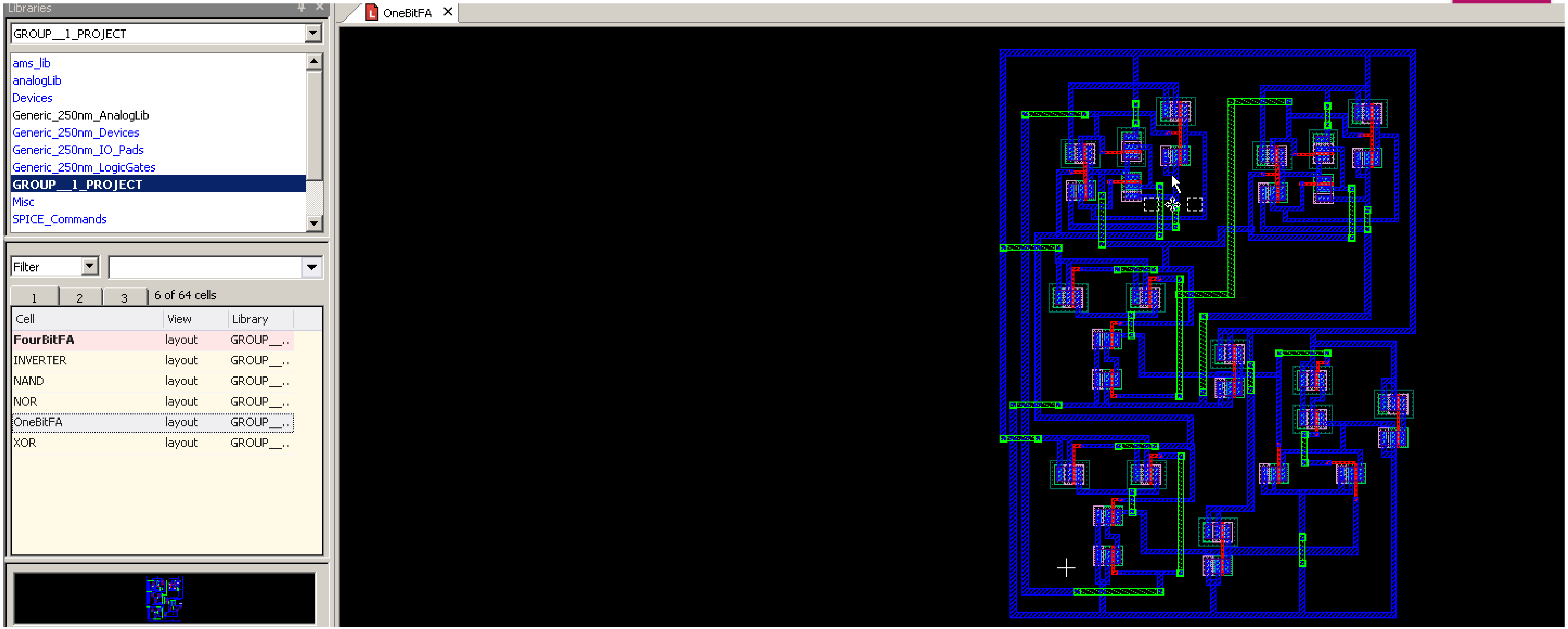
Secondary Cursor VCursor2 666.666607n

Delta 333.333213n

Trac...	Y1	Y2	Delta	Deriva...	Deriva...	Slop
A0:V	5.	5.	0.	0.	0.	
A1:V	0.	5.	5.	0.	0.	
A2:V	5.	0.	-5.	303.	0.	-
A3:V	5.	0.	-5.	0.	0.	-
B0:V	0.	0.	0.	0.	0.	
B1:V	0.	5.	5.	0.	0.	
B2:V	5.	0.	-5.	0.	0.	-
B3:V	5.	0.	-5.	0.	0.	-
CIN:V	5.	5.	0.	0.	0.	
COUT	4.	-15.	-4.	44.	523.	-
S0:V	-200.	-427.	-226.	-378.	11.	-6
S1:V	4.	4.	37.	42.	-14.	1
S2:V	24.	4.	4.	-82.	-10.	
S3:V	4.	-69.	-4.	42.	2.	-

4 bit full adder Carry ripple test bench wave

4-Bit Full Adder Design Layout



Libraries

GROUP__1_PROJECT

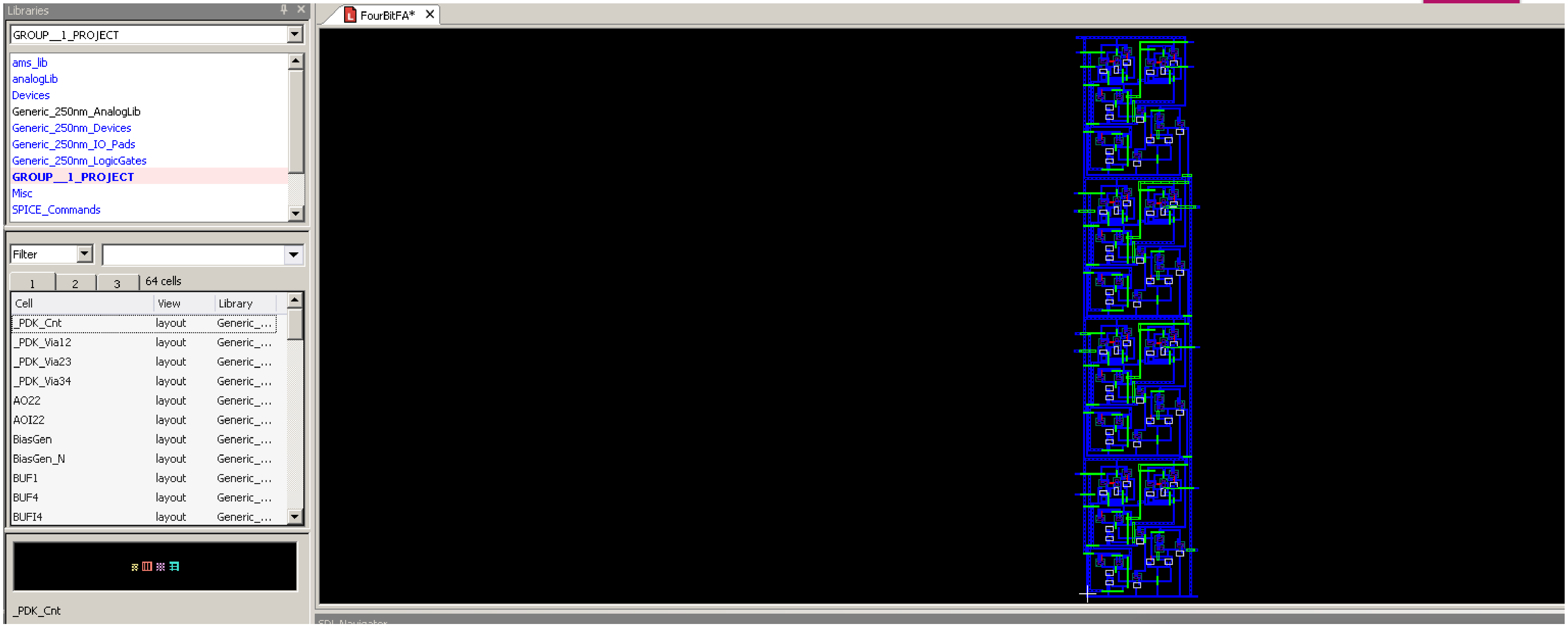
ams_lib
analogLib
Devices
Generic_250nm_AnalogLib
Generic_250nm_Devices
Generic_250nm_IO_Pads
Generic_250nm_LogicGates
GROUP__1_PROJECT
Misc
SPICE_Commands

6 of 64 cells

Cell	View	Library
FourBitFA	layout	GROUP__..
INVERTER	layout	GROUP__..
NAND	layout	GROUP__..
NOR	layout	GROUP__..
OneBitFA	layout	GROUP__..
XOR	layout	GROUP__..

1 bit full adder Carry ripple
layout

4-Bit Full Adder Design Layout



Libraries

GROUP__1_PROJECT

- ams_lib
- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- **GROUP__1_PROJECT**
- Misc
- SPICE_Commands

Filter

1 2 3 64 cells

Cell	View	Library
_PDK_Cnt	layout	Generic_...
_PDK_Via12	layout	Generic_...
_PDK_Via23	layout	Generic_...
_PDK_Via34	layout	Generic_...
AO22	layout	Generic_...
AOI22	layout	Generic_...
BiasGen	layout	Generic_...
BiasGen_N	layout	Generic_...
BUF1	layout	Generic_...
BUF4	layout	Generic_...
BUFI4	layout	Generic_...

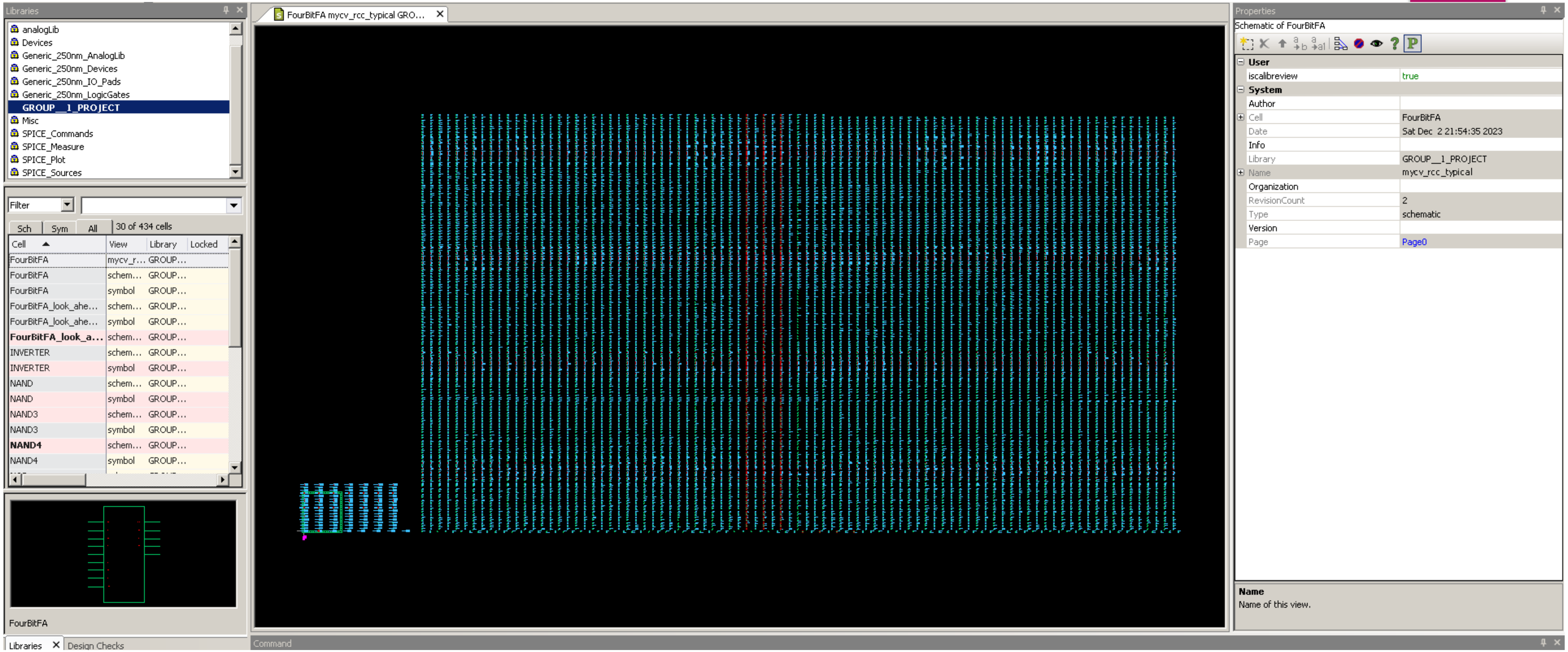
_PDK_Cnt

FourBitFA*

SDL Navigator

4 bit full adder Carry ripple layout

4-Bit Full Adder Design Layout



- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- GROUP__1_PROJECT
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch Sym All 30 of 434 cells

Cell	View	Library	Locked
FourBitFA	mycv_r...	GROUP...	
FourBitFA	schem...	GROUP...	
FourBitFA	symbol	GROUP...	
FourBitFA_look_ahe...	schem...	GROUP...	
FourBitFA_look_ahe...	symbol	GROUP...	
FourBitFA_look_a...	schem...	GROUP...	
INVERTER	schem...	GROUP...	
INVERTER	symbol	GROUP...	
NAND	schem...	GROUP...	
NAND	symbol	GROUP...	
NAND3	schem...	GROUP...	
NAND3	symbol	GROUP...	
NAND4	schem...	GROUP...	
NAND4	symbol	GROUP...	

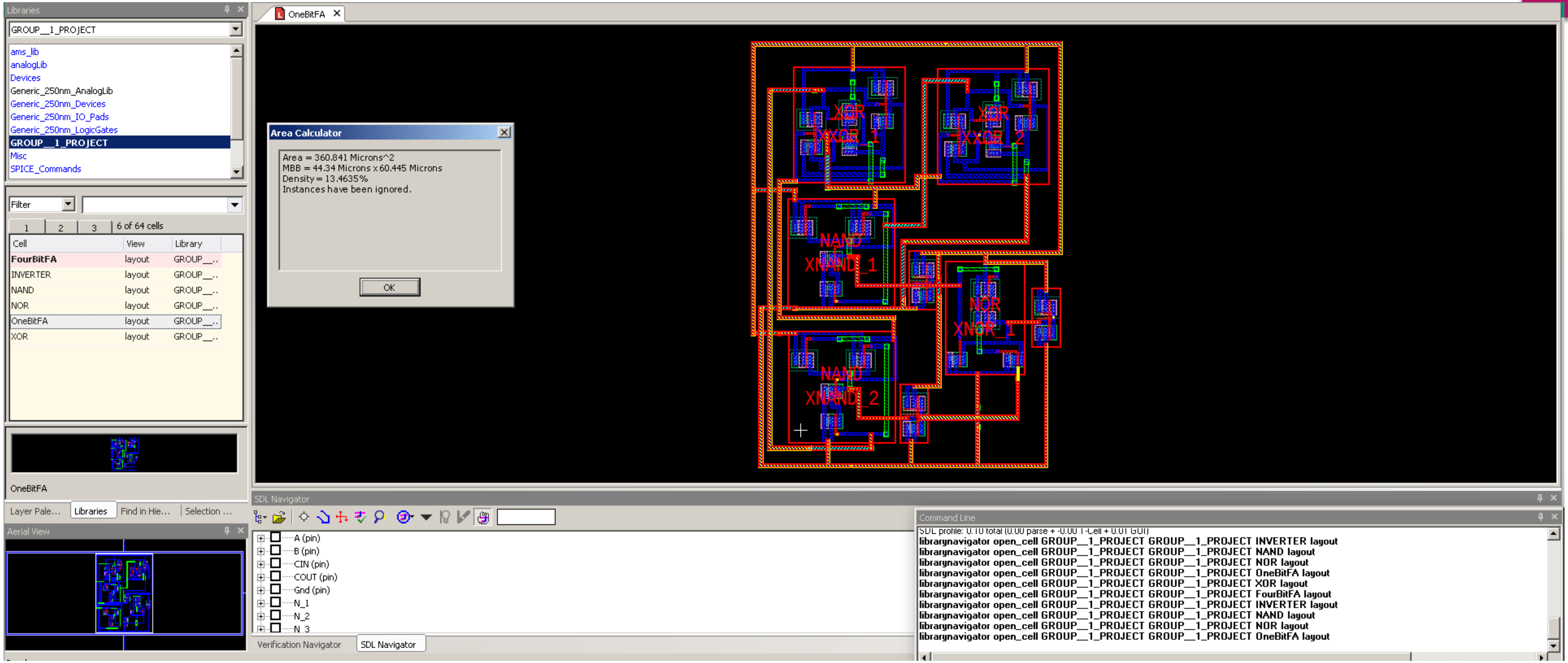
Schematic of FourBitFA

User	
iscalibreview	true
System	
Author	
Cell	FourBitFA
Date	Sat Dec 2 21:54:35 2023
Info	
Library	GROUP__1_PROJECT
Name	mycv_rcc_typical
Organization	
RevisionCount	2
Type	schematic
Version	
Page	Page0

Name
Name of this view.

4 bit full adder Carry ripple parasitic capacitance

4-Bit Full Adder Design Area



Cell	View	Library
FourBitFA	layout	GROUP__..
INVERTER	layout	GROUP__..
NAND	layout	GROUP__..
NOR	layout	GROUP__..
OneBitFA	layout	GROUP__..
XOR	layout	GROUP__..

Area Calculator

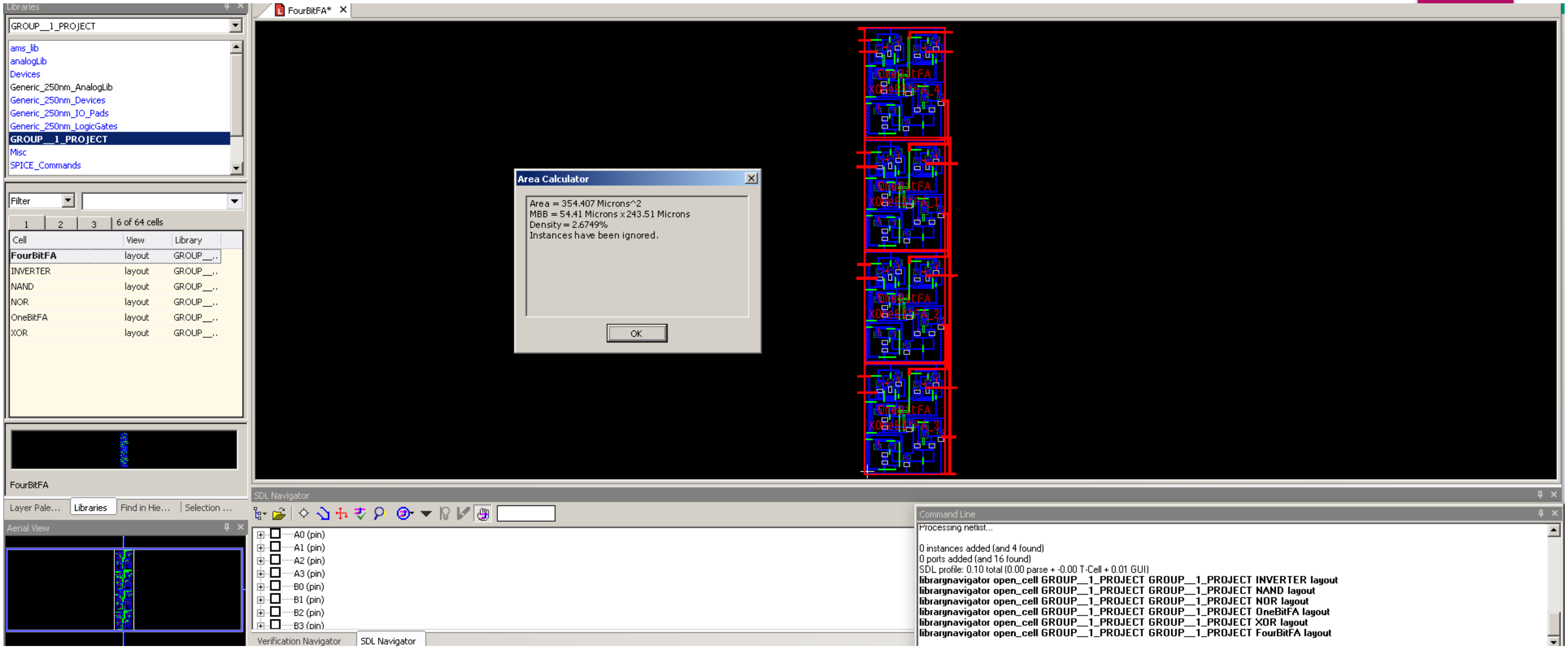
```
Area = 360.841 Microns^2
MBB = 44.34 Microns x 60.445 Microns
Density = 13.4635%
Instances have been ignored.
```

OK

```
SDL profile: 0.10 total (0.00 parse + -0.00 T-Cell + 0.01 GUI)
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT INVERTER layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT NAND layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT NOR layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT OneBitFA layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT XOR layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT FourBitFA layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT INVERTER layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT NAND layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT NOR layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT OneBitFA layout
```

1 bit full adder Carry ripple
layout area

4-Bit Full Adder Design Area



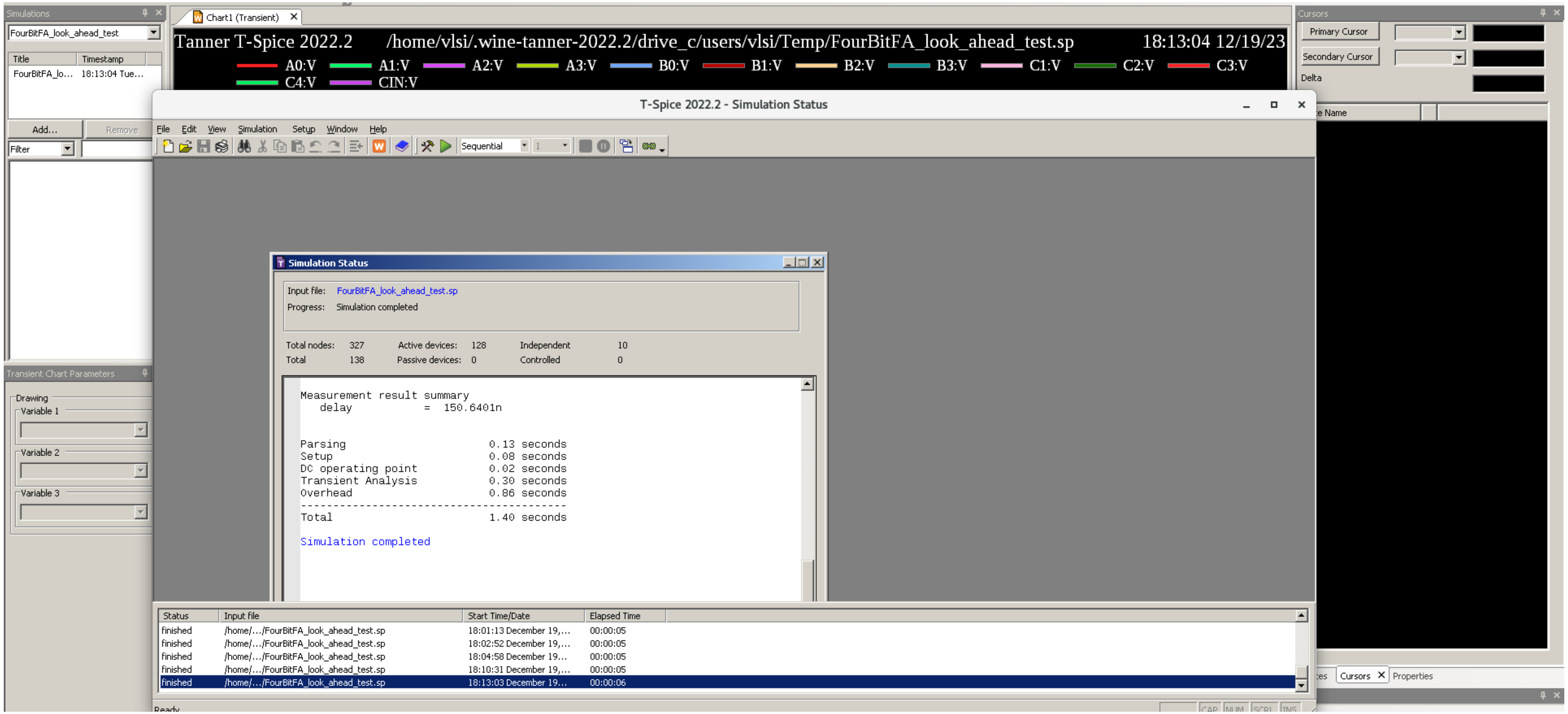
Cell	View	Library
FourBitFA	layout	GROUP__..
INVERTER	layout	GROUP__..
NAND	layout	GROUP__..
NOR	layout	GROUP__..
OneBitFA	layout	GROUP__..
XOR	layout	GROUP__..

```
Area = 354.407 Microns^2
MBB = 54.41 Microns x 243.51 Microns
Density = 2.6749%
Instances have been ignored.
```

```
Processing netlist...

0 instances added (and 4 found)
0 ports added (and 16 found)
SDL profile: 0.10 total (0.00 parse + -0.00 T-Cell + 0.01 GUI)
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT INVERTER layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT NAND layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT NOR layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT OneBitFA layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT XOR layout
librarynavigator open_cell GROUP__1_PROJECT GROUP__1_PROJECT FourBitFA layout
```

4 bit full adder Carry ripple layout area

4-Bit Full Adder Design Delay



Simulation Status

Input file: FourBitFA_look_ahead_test.sp
Progress: Simulation completed

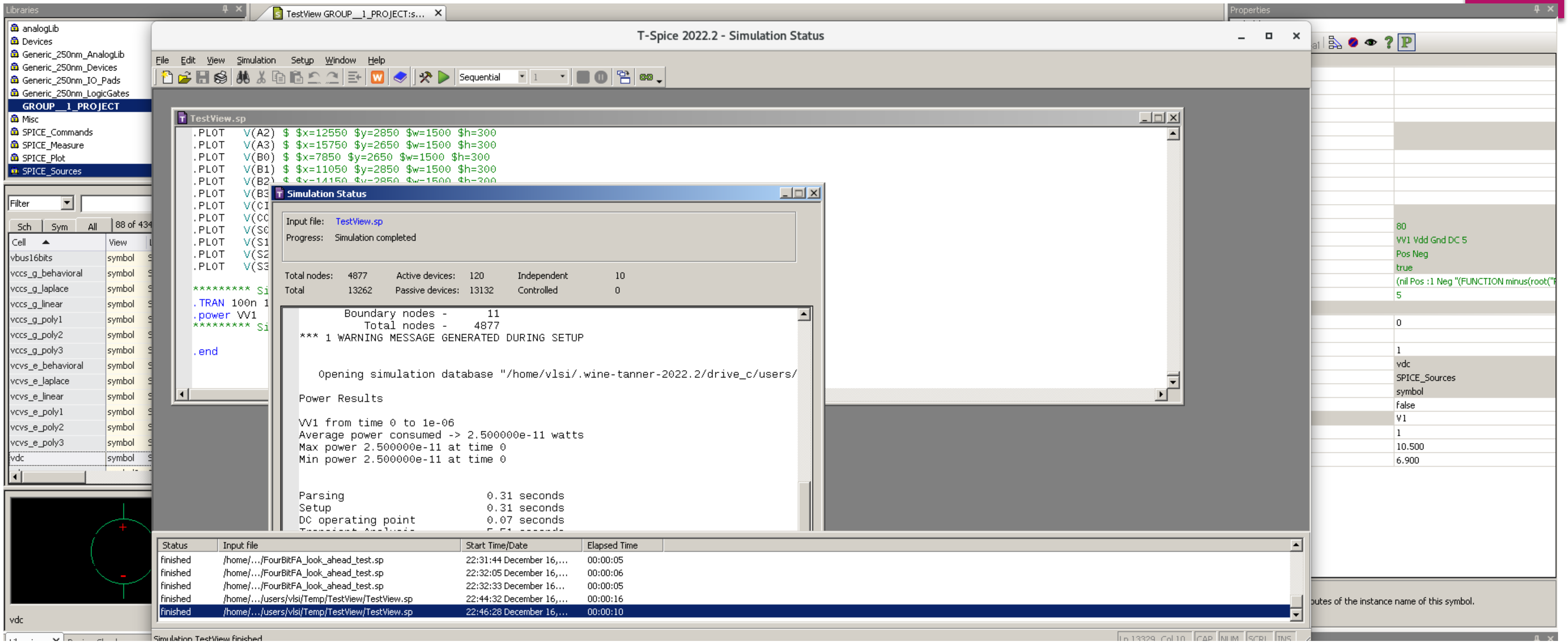
Total nodes: 327   Active devices: 128   Independent 10
Total 138   Passive devices: 0   Controlled 0

```
Measurement result summary
   delay            =  150.6401n


Parsing                        0.13 seconds
Setup                          0.08 seconds
DC operating point             0.02 seconds
Transient Analysis             0.30 seconds
Overhead                       0.86 seconds
-----------------------------------------
Total                          1.40 seconds

Simulation completed
```

Status	Input file	Start Time/Date	Elapsed Time
finished	/home/.../FourBitFA_look_ahead_test.sp	18:01:13 December 19,...	00:00:05
finished	/home/.../FourBitFA_look_ahead_test.sp	18:02:52 December 19,...	00:00:05
finished	/home/.../FourBitFA_look_ahead_test.sp	18:04:58 December 19...	00:00:05
finished	/home/.../FourBitFA_look_ahead_test.sp	18:10:31 December 19,...	00:00:05
finished	/home/.../FourBitFA_look_ahead_test.sp	18:13:03 December 19...	00:00:06

4 bit full adder Carry ripple delay

4-Bit Full Adder Design Power



Cell	View
vbus16bits	symbol
vccs_g_behavioral	symbol
vccs_g_laplace	symbol
vccs_g_linear	symbol
vccs_g_poly1	symbol
vccs_g_poly2	symbol
vccs_g_poly3	symbol
vcvs_e_behavioral	symbol
vcvs_e_laplace	symbol
vcvs_e_linear	symbol
vcvs_e_poly1	symbol
vcvs_e_poly2	symbol
vcvs_e_poly3	symbol
vdc	symbol

TestView.sp

```
.PLOT   V(A2) $ $x=12550 $y=2850 $w=1500 $h=300
.PLOT   V(A3) $ $x=15750 $y=2650 $w=1500 $h=300
.PLOT   V(B0) $ $x=7850 $y=2650 $w=1500 $h=300
.PLOT   V(B1) $ $x=11050 $y=2850 $w=1500 $h=300
.PLOT   V(B2) $ $x=14150 $y=2850 $w=1500 $h=300
.PLOT   V(B3
.PLOT   V(CI
.PLOT   V(CC
.PLOT   V(SC
.PLOT   V(S1
.PLOT   V(S2
.PLOT   V(S3

********* Si
.TRAN 100n 1
.power VV1
********* Si

.end
```

Simulation Status

Input file: TestView.sp

Progress: Simulation completed

Total nodes:	4877	Active devices:	120	Independent	10
Total	13262	Passive devices:	13132	Controlled	0

```
        Boundary nodes -       11
           Total nodes -     4877
*** 1 WARNING MESSAGE GENERATED DURING SETUP


   Opening simulation database "/home/vlsi/.wine-tanner-2022.2/drive_c/users/

Power Results

VV1 from time 0 to 1e-06
Average power consumed -> 2.500000e-11 watts
Max power 2.500000e-11 at time 0
Min power 2.500000e-11 at time 0


Parsing                      0.31 seconds
Setup                        0.31 seconds
DC operating point           0.07 seconds
```

Status	Input file	Start Time/Date	Elapsed Time
finished	/home/…/FourBitFA_look_ahead_test.sp	22:31:44 December 16,…	00:00:05
finished	/home/…/FourBitFA_look_ahead_test.sp	22:32:05 December 16,…	00:00:06
finished	/home/…/FourBitFA_look_ahead_test.sp	22:32:33 December 16…	00:00:05
finished	/home/…/users/vlsi/Temp/TestView/TestView.sp	22:44:32 December 16,…	00:00:16
finished	/home/…/users/vlsi/Temp/TestView/TestView.sp	22:46:28 December 16,…	00:00:10

```
80
VV1 Vdd Gnd DC 5
Pos Neg
true
(nil Pos :1 Neg "(FUNCTION minus(root("
5
0
1
vdc
SPICE_Sources
symbol
false
V1
1
10.500
6.900
```

butes of the instance name of this symbol.

4 bit full adder Carry ripple power

Table of contents

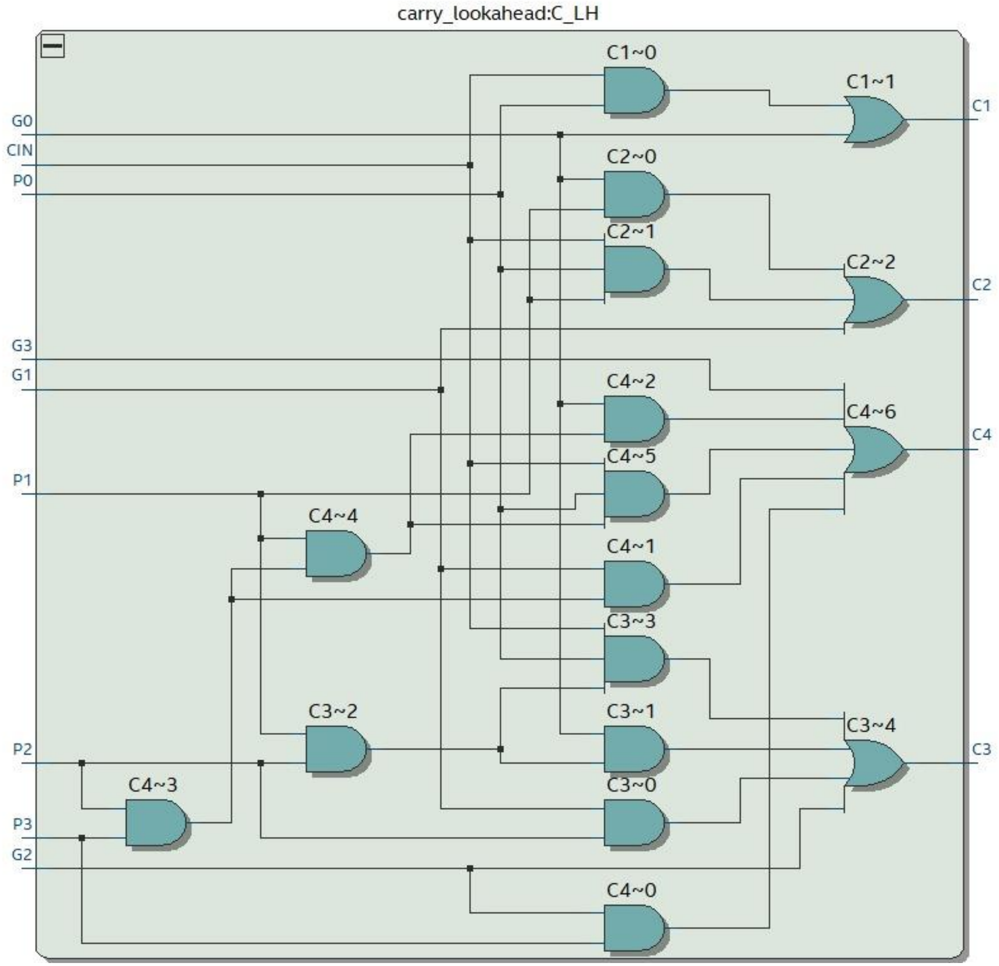
1. Introduction
2. **4-Bit Full Adder Design**
   - I. Carry ripple
   - **II. Carry look ahead**
3. Conclusion

4-Bit Full Adder Design Equations

$Gi = Ai \text{ AND } Bi$
$Pi = Ai \text{ XOR } Bi$

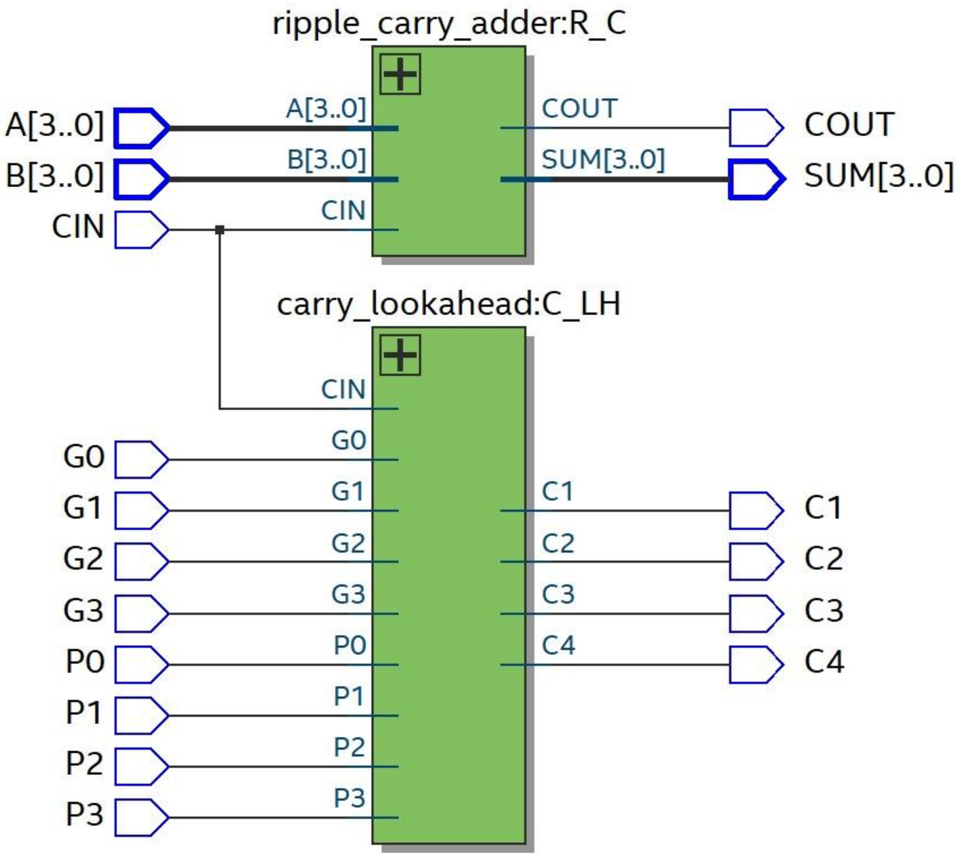
$C1 = G0 + (P0 * Cin)$
$C2 = G1 + (P1 * G0) + (P1 * P0 * Cin)$
$C3 = G2 + (P2 * G1) + (P2 * P1 * G0) + (P2 * P1 * P0 * Cin)$
$C4 = G3 + (P3 * G2) + (P3 * P2 * G1) + (P3 * P2 * P1 * G0) + (P3 * P2 * P1 * P0 * Cin)$

4-Bit Full Adder Design Net List



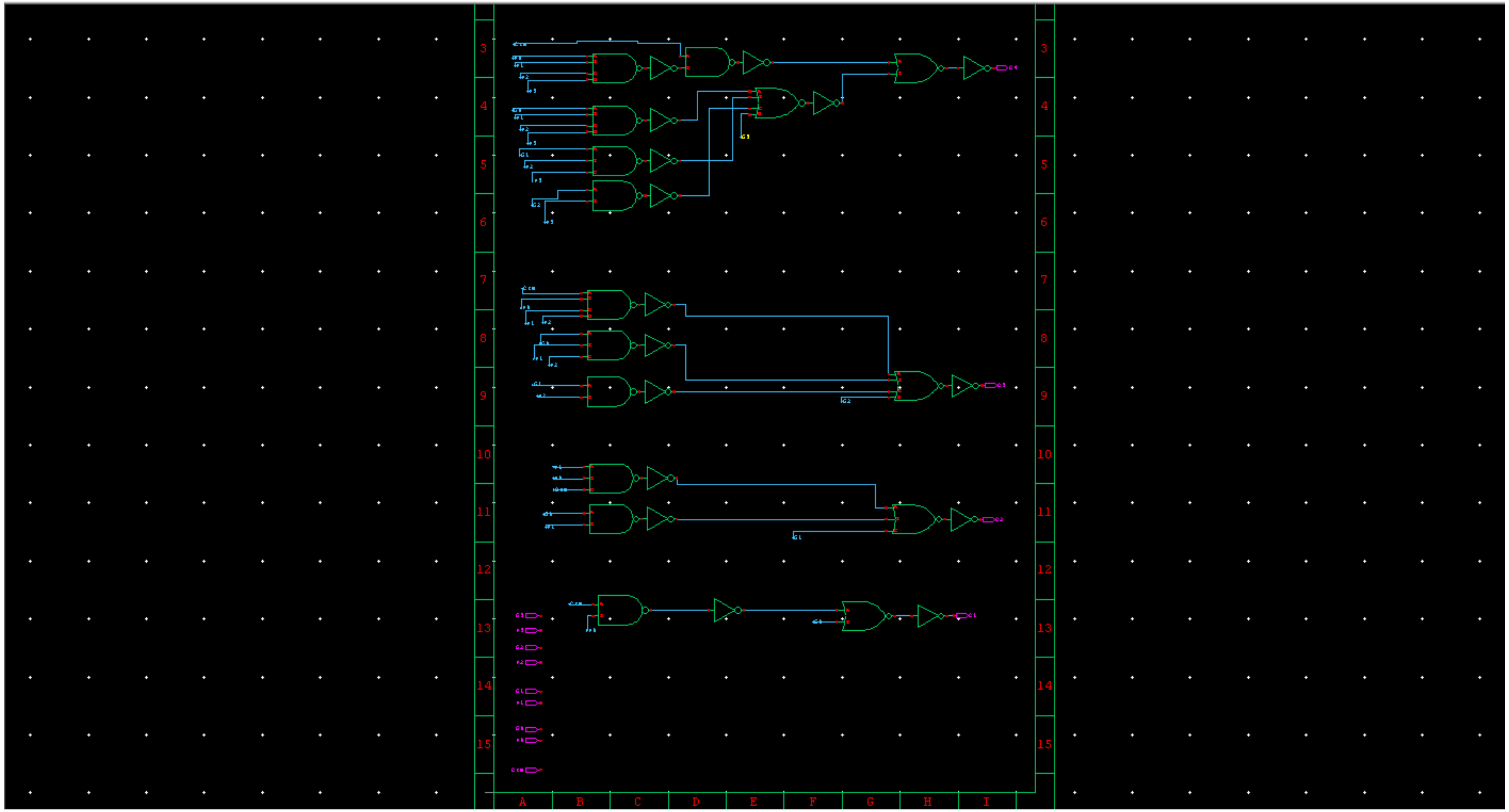
4 bit full adder Carry look ahead Net List

4-Bit Full Adder Design Net List



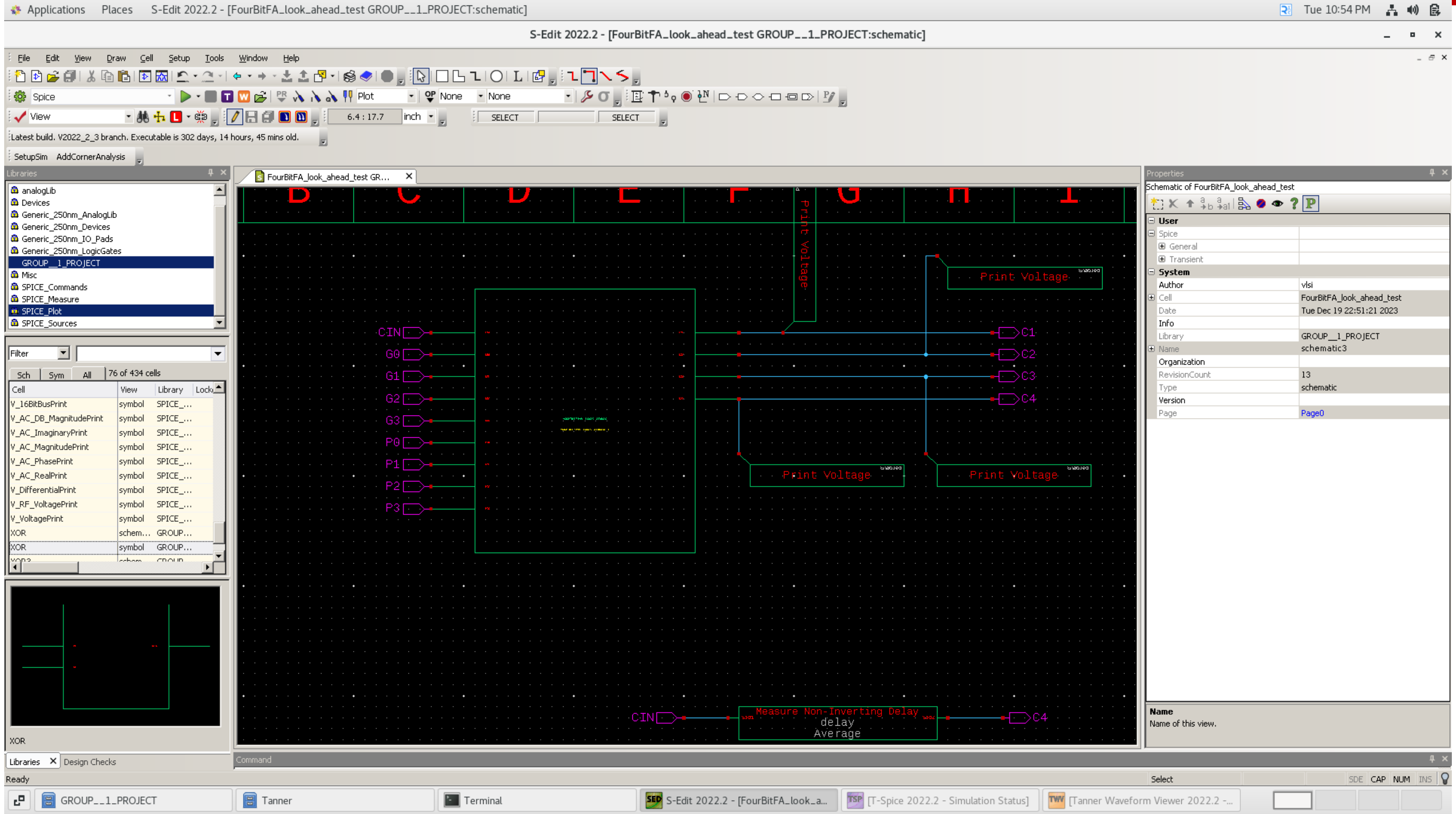
4 bit full adder Carry look ahead Net List main

4-Bit Full Adder Design Schematic



4 bit full adder Carry look ahead schematic

4-Bit Full Adder Design Schematic



Latest build. V2022_2_3 branch. Executable is 302 days, 14 hours, 45 mins old.

Properties

Schematic of FourBitFA_look_ahead_test

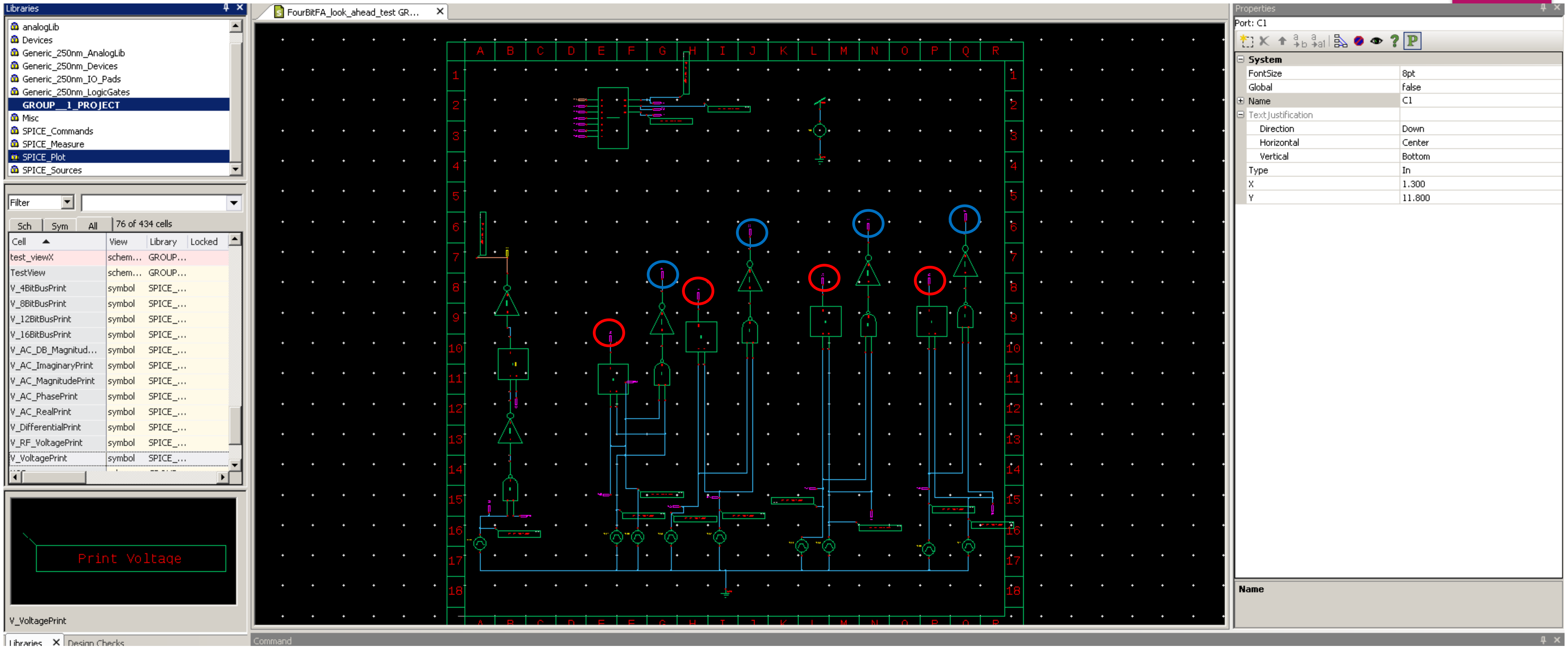
User
Spice
General
Transient
System

Author	vlsi
Cell	FourBitFA_look_ahead_test
Date	Tue Dec 19 22:51:21 2023
Info	
Library	GROUP__1_PROJECT
Name	schematic3
Organization	
RevisionCount	13
Type	schematic
Version	
Page	Page0

Name
Name of this view.

4 bit full adder Carry look ahead test bench

Carry Lookahead Testbench



Libraries

- analogLib
- Devices
- Generic_250nm_AnalogLib
- Generic_250nm_Devices
- Generic_250nm_IO_Pads
- Generic_250nm_LogicGates
- GROUP__1_PROJECT
- Misc
- SPICE_Commands
- SPICE_Measure
- SPICE_Plot
- SPICE_Sources

Filter

Sch Sym All 76 of 434 cells

Cell	View	Library	Locked
test_viewX	schem...	GROUP...	
TestView	schem...	GROUP...	
V_4BitBusPrint	symbol	SPICE_...	
V_8BitBusPrint	symbol	SPICE_...	
V_12BitBusPrint	symbol	SPICE_...	
V_16BitBusPrint	symbol	SPICE_...	
V_AC_DB_Magnitud...	symbol	SPICE_...	
V_AC_ImaginaryPrint	symbol	SPICE_...	
V_AC_MagnitudePrint	symbol	SPICE_...	
V_AC_PhasePrint	symbol	SPICE_...	
V_AC_RealPrint	symbol	SPICE_...	
V_DifferentialPrint	symbol	SPICE_...	
V_RF_VoltagePrint	symbol	SPICE_...	
V_VoltagePrint	symbol	SPICE_...	

Print Voltage

V_VoltagePrint

Libraries Design Checks

FourBitFA_look_ahead_test GR...

Command

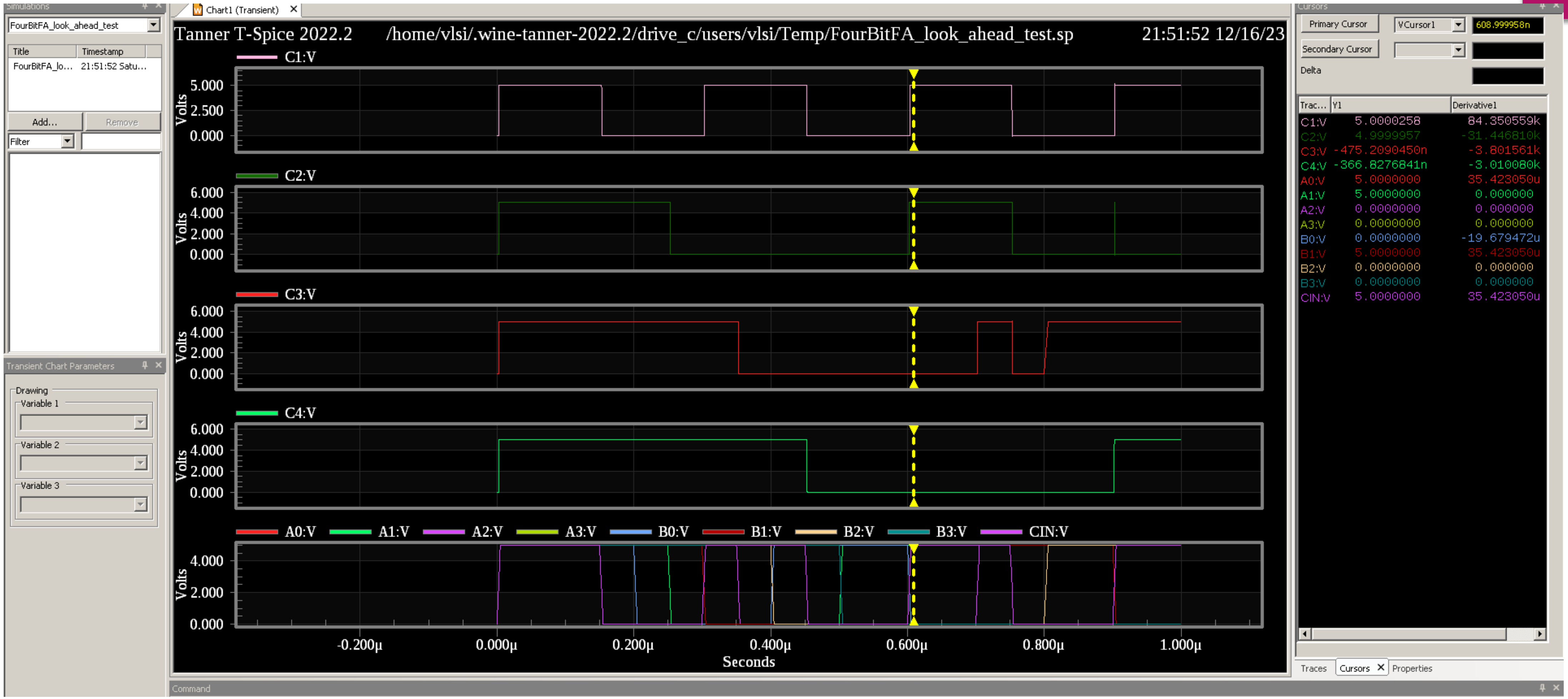
Properties

Port: C1

System	
FontSize	8pt
Global	false
Name	C1
TextJustification	
Direction	Down
Horizontal	Center
Vertical	Bottom
Type	In
X	1.300
Y	11.800

Name

4-Bit Full Adder Design wave



FourBitFA_look_ahead_test

Title	Timestamp
FourBitFA_lo...	21:51:52 Satu...

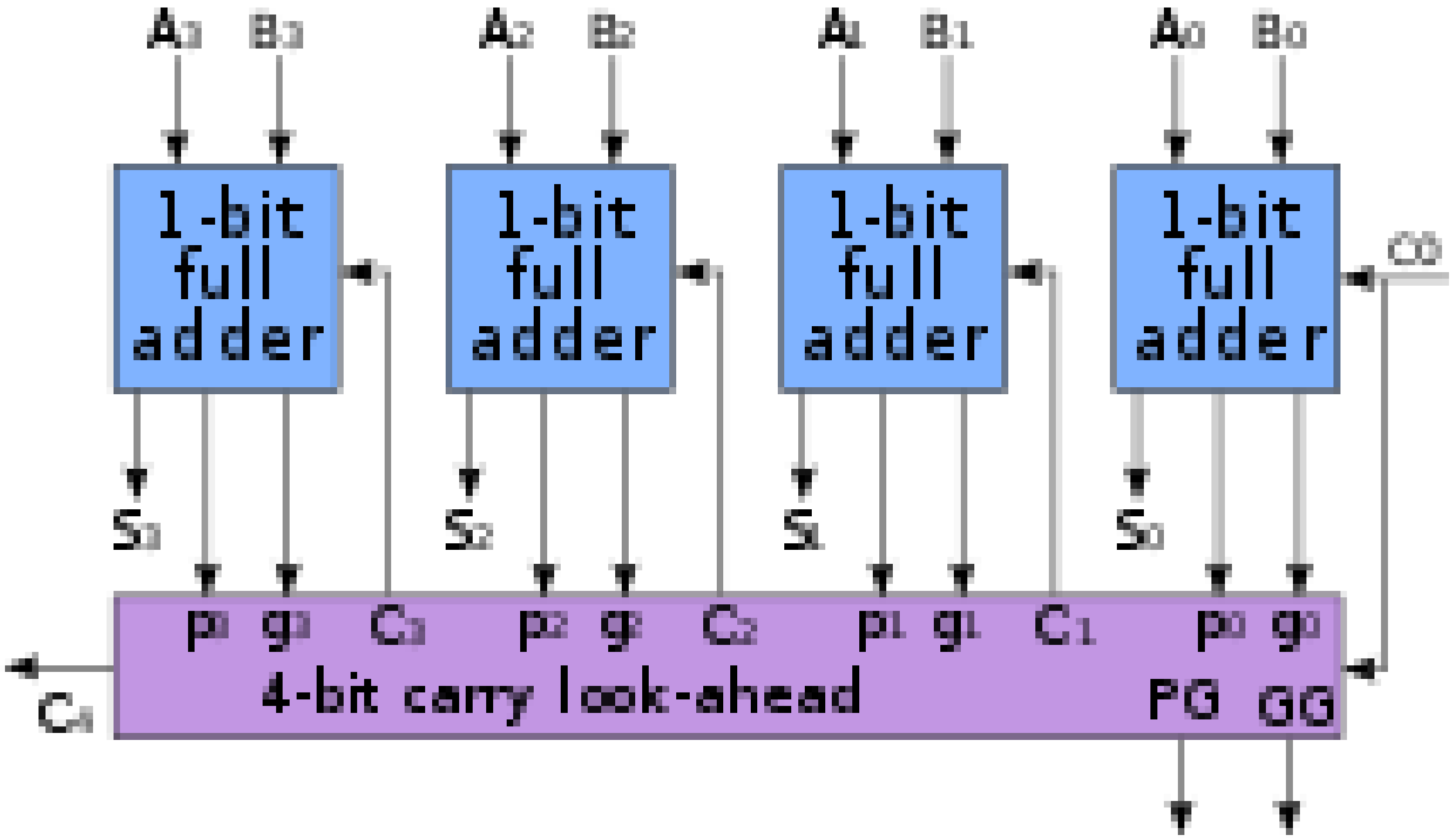
Tanner T-Spice 2022.2 /home/vlsi/.wine-tanner-2022.2/drive_c/users/vlsi/Temp/FourBitFA_look_ahead_test.sp 21:51:52 12/16/23

Primary Cursor: VCursor1 608.999958n

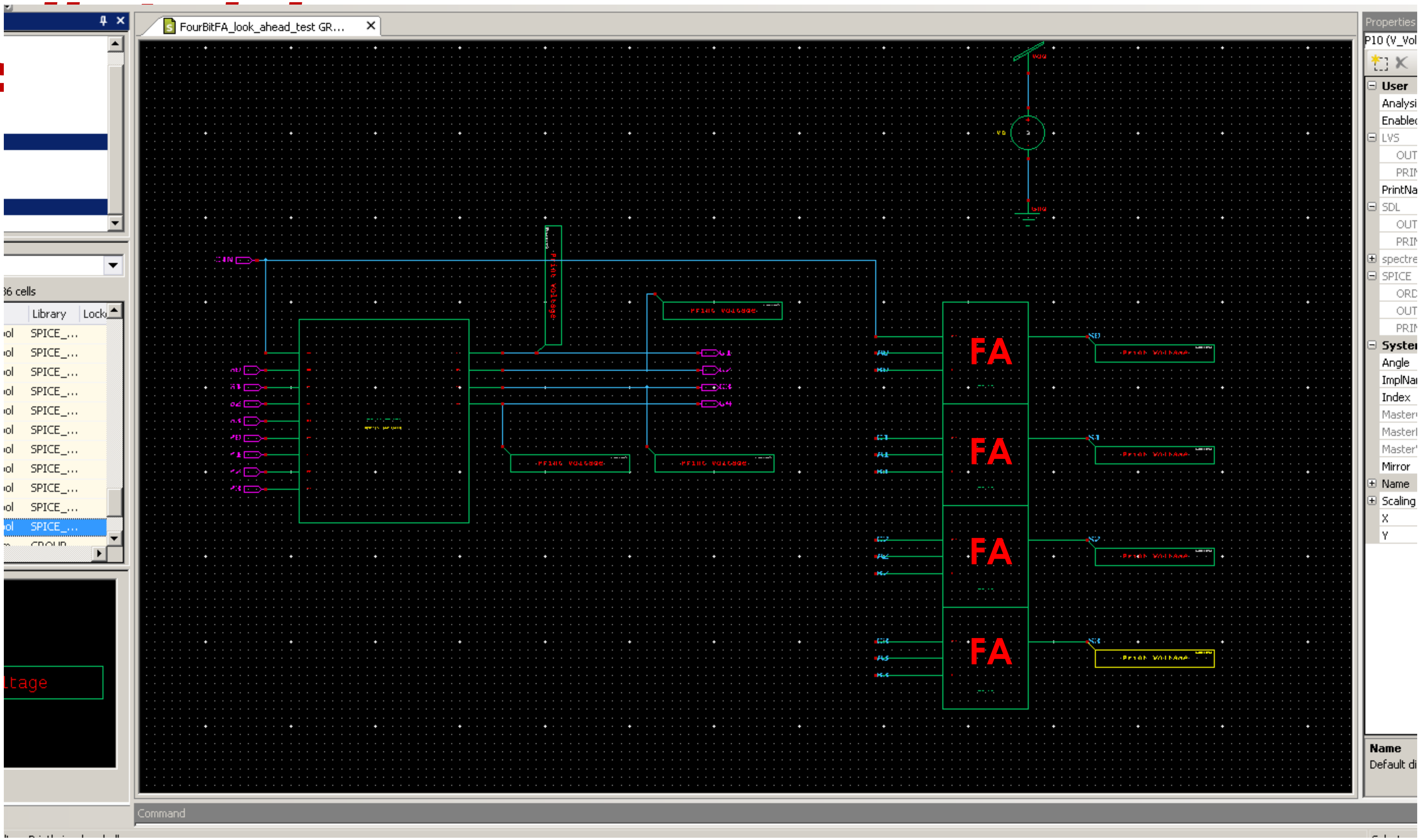
Trac...	Y1	Derivative1
C1:V	5.0000258	84.350559k
C2:V	4.9999957	-31.446810k
C3:V	-475.2090450n	-3.801561k
C4:V	-366.8276841n	-3.010080k
A0:V	5.0000000	35.423050u
A1:V	5.0000000	0.000000
A2:V	0.0000000	0.000000
A3:V	0.0000000	0.000000
B0:V	0.0000000	-19.679472u
B1:V	5.0000000	35.423050u
B2:V	0.0000000	0.000000
B3:V	0.0000000	0.000000
CIN:V	5.0000000	35.423050u

4 bit full adder Carry look ahead test bench wave

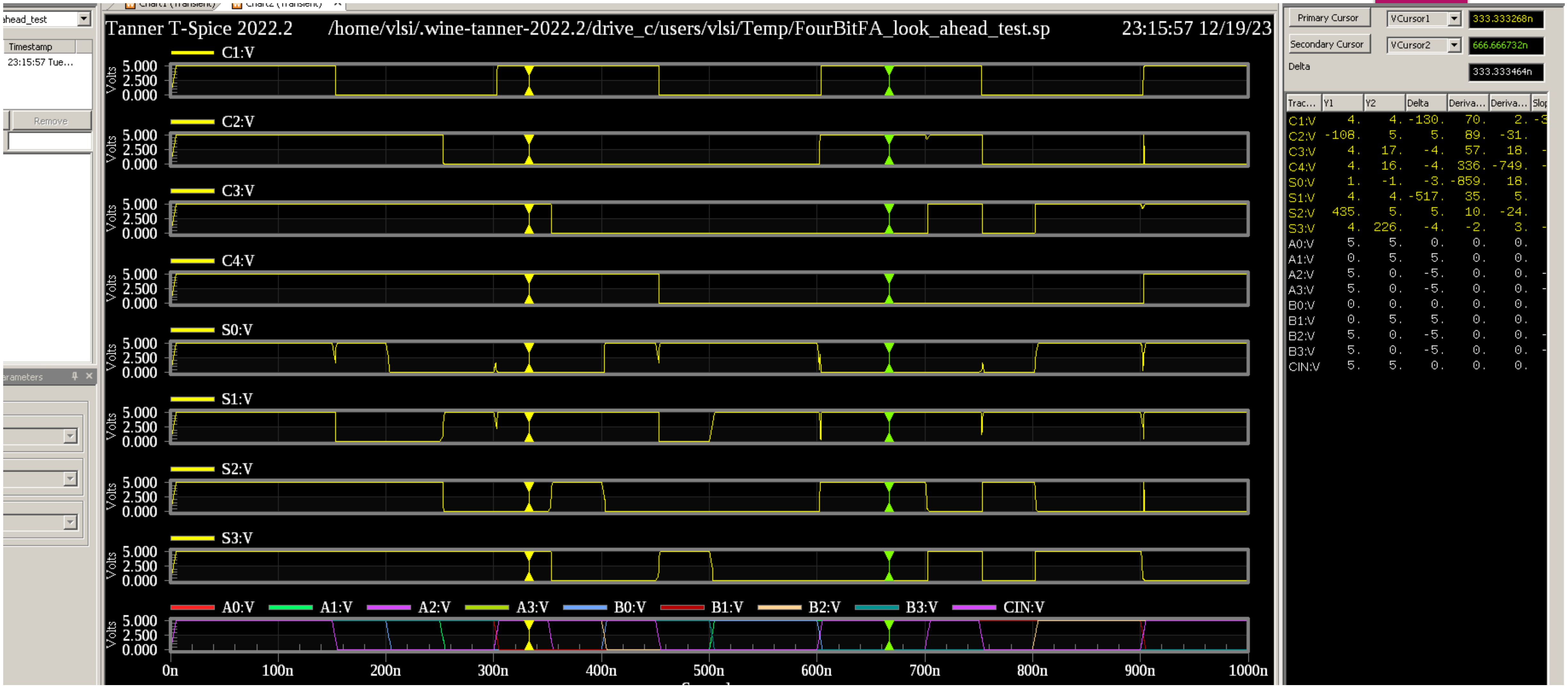
Add One-Bit Full Adders To Make 4-Bit Full Adder



Add One-Bit Full Adders To Make 4-Bit Fu



4-Bit Full Adder Simulation Results



Tanner T-Spice 2022.2 /home/vlsi/.wine-tanner-2022.2/drive_c/users/vlsi/Temp/FourBitFA_look_ahead_test.sp 23:15:57 12/19/23

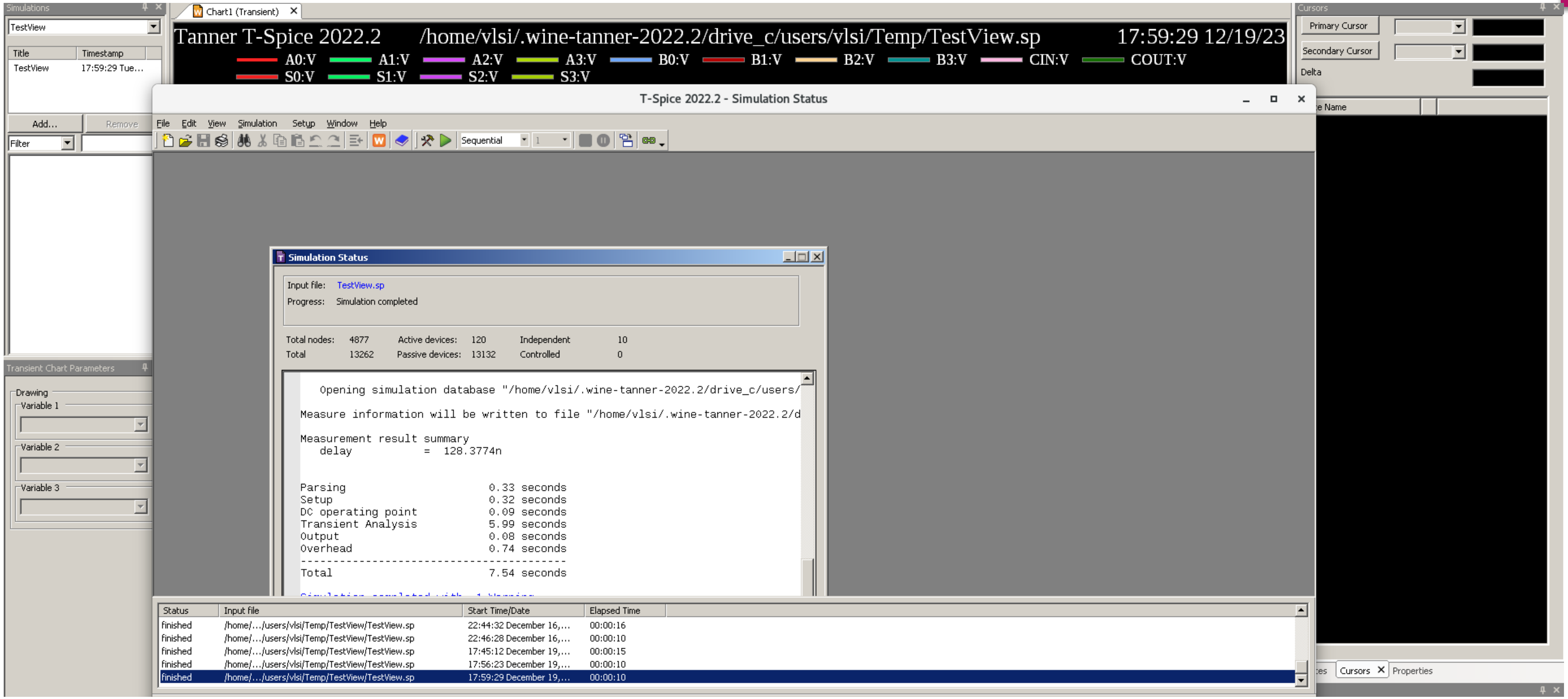
Primary Cursor: VCursor1 333.333268n

Secondary Cursor: VCursor2 666.666732n

Delta: 333.333464n

Trac...	Y1	Y2	Delta	Deriva...	Deriva...	Slop
C1:V	4.	4.	-130.	70.	2.	-3
C2:V	-108.	5.	5.	89.	-31.	
C3:V	4.	17.	-4.	57.	18.	-
C4:V	4.	16.	-4.	336.	-749.	-
S0:V	1.	-1.	-3.	-859.	18.	
S1:V	4.	4.	-517.	35.	5.	
S2:V	435.	5.	5.	10.	-24.	
S3:V	4.	226.	-4.	-2.	3.	-
A0:V	5.	5.	0.	0.	0.	
A1:V	0.	5.	5.	0.	0.	
A2:V	5.	0.	-5.	0.	0.	-
A3:V	5.	0.	-5.	0.	0.	-
B0:V	0.	0.	0.	0.	0.	
B1:V	0.	5.	5.	0.	0.	
B2:V	5.	0.	-5.	0.	0.	-
B3:V	5.	0.	-5.	0.	0.	-
CIN:V	5.	5.	0.	0.	0.	

4-Bit Full Adder Design Delay



Tanner T-Spice 2022.2 /home/vlsi/.wine-tanner-2022.2/drive_c/users/vlsi/Temp/TestView.sp 17:59:29 12/19/23

T-Spice 2022.2 - Simulation Status

Simulation Status

Input file: TestView.sp

Progress: Simulation completed

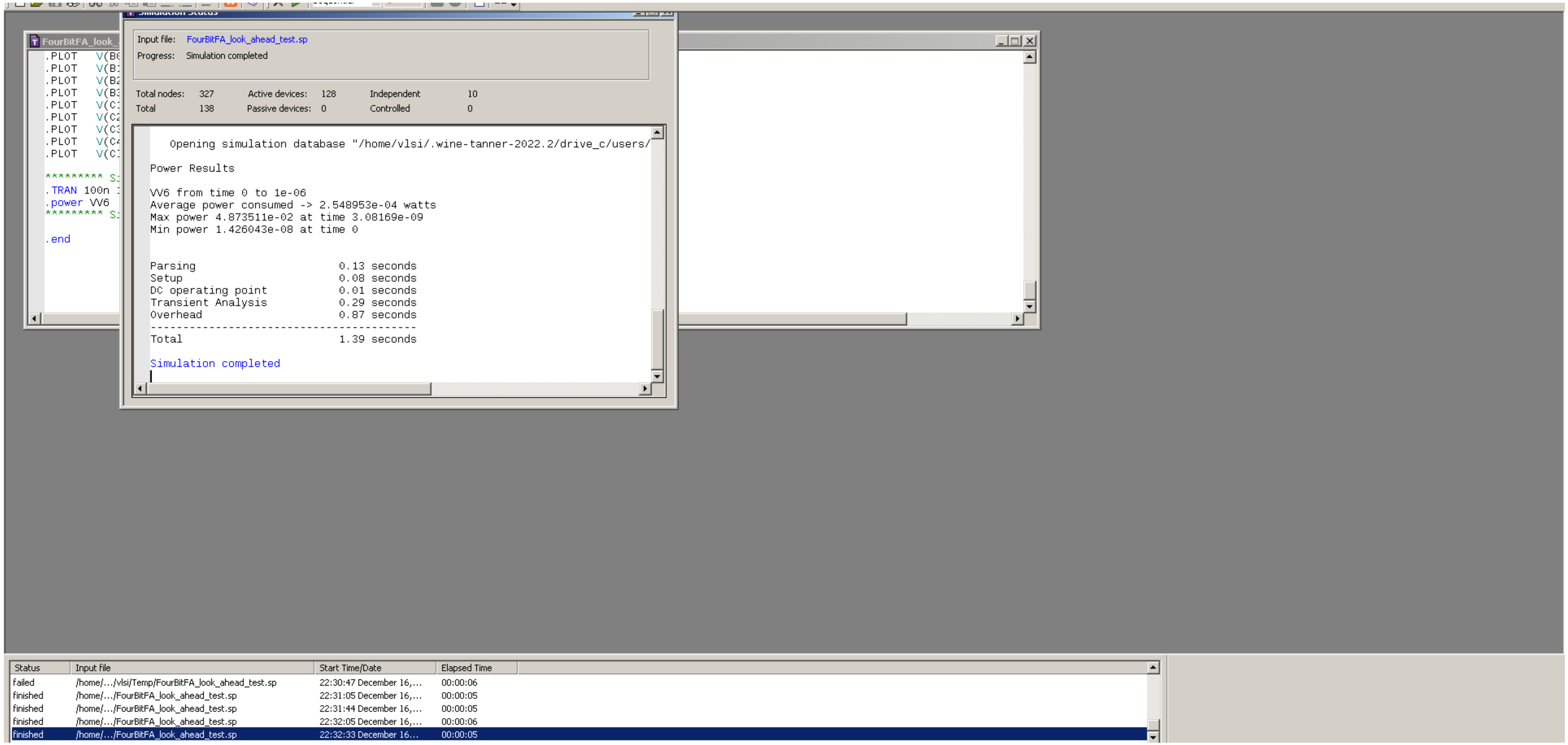
Total nodes:	4877	Active devices:	120	Independent	10
Total	13262	Passive devices:	13132	Controlled	0

```
   Opening simulation database "/home/vlsi/.wine-tanner-2022.2/drive_c/users/

Measure information will be written to file "/home/vlsi/.wine-tanner-2022.2/d

Measurement result summary
   delay          =  128.3774n


Parsing                      0.33 seconds
Setup                        0.32 seconds
DC operating point           0.09 seconds
Transient Analysis           5.99 seconds
Output                       0.08 seconds
Overhead                     0.74 seconds
-----------------------------------------
Total                        7.54 seconds
```

Status	Input file	Start Time/Date	Elapsed Time
finished	/home/.../users/vlsi/Temp/TestView/TestView.sp	22:44:32 December 16,...	00:00:16
finished	/home/.../users/vlsi/Temp/TestView/TestView.sp	22:46:28 December 16,...	00:00:10
finished	/home/.../users/vlsi/Temp/TestView/TestView.sp	17:45:12 December 19,...	00:00:15
finished	/home/.../users/vlsi/Temp/TestView/TestView.sp	17:56:23 December 19,...	00:00:10
finished	/home/.../users/vlsi/Temp/TestView/TestView.sp	17:59:29 December 19,...	00:00:10

4 bit full adder Carry look ahead delay

4-Bit Full Adder Design Power



```
.PLOT   V(B0
.PLOT   V(B1
.PLOT   V(B2
.PLOT   V(B3
.PLOT   V(C1
.PLOT   V(C2
.PLOT   V(C3
.PLOT   V(C4
.PLOT   V(C1

********* S
.TRAN 100n 1
.power VV6
********* S

.end
```

Input file: FourBitFA_look_ahead_test.sp

Progress: Simulation completed

```
Total nodes:   327     Active devices:   128     Independent    10
Total          138     Passive devices:  0       Controlled     0
```

```
   Opening simulation database "/home/vlsi/.wine-tanner-2022.2/drive_c/users/

Power Results

VV6 from time 0 to 1e-06
Average power consumed -> 2.548953e-04 watts
Max power 4.873511e-02 at time 3.08169e-09
Min power 1.426043e-08 at time 0


Parsing                         0.13 seconds
Setup                           0.08 seconds
DC operating point              0.01 seconds
Transient Analysis              0.29 seconds
Overhead                        0.87 seconds
-----------------------------------------
Total                           1.39 seconds

Simulation completed
```

Status	Input file	Start Time/Date	Elapsed Time
failed	/home/.../vlsi/Temp/FourBitFA_look_ahead_test.sp	22:30:47 December 16,...	00:00:06
finished	/home/.../FourBitFA_look_ahead_test.sp	22:31:05 December 16,...	00:00:05
finished	/home/.../FourBitFA_look_ahead_test.sp	22:31:44 December 16,...	00:00:05
finished	/home/.../FourBitFA_look_ahead_test.sp	22:32:05 December 16,...	00:00:06
finished	/home/.../FourBitFA_look_ahead_test.sp	22:32:33 December 16...	00:00:05

4 bit full adder Carry look ahead test bench wave

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1. Introduction
2. 4-Bit Full Adder Design
   I. Carry ripple
   II. Carry look ahead
3. Conclusion

Conclusion

In this exploration of the 4-bit full adder utilizing the Carry Ripple and Carry Look-Ahead methods, we have delved into the intricacies of two distinct approaches to achieving binary addition. Each method carries its own set of advantages and trade-offs, contributing to the rich tapestry of digital circuit design.

Conclusion

Carry Ripple Adder:

The Carry Ripple Adder, with its sequential ripple propagation, embodies simplicity in its design. It offers a clear and intuitive implementation of a full adder, making it accessible and easy to comprehend.

Conclusion

Carry Ripple Adder:

While its straightforward nature facilitates ease of construction, it comes at the cost of increased propagation delay, limiting its suitability for applications that demand high-speed arithmetic computations.

Conclusion

Carry Look-Ahead Adder:

Contrastingly, the Carry Look-Ahead Adder presents a more sophisticated solution to the challenge of carry generation. By computing carry-out signals in parallel, this method significantly reduces propagation delay, making it a compelling choice for applications requiring swift and efficient arithmetic operations. However, the enhanced speed comes with increased complexity in logic design, demanding careful consideration of trade-offs.

Conclusion

Carry Look-Ahead Adder:

Contrastingly, the Carry Look-Ahead Adder presents a more sophisticated solution to the challenge of carry generation. By computing carry-out signals in parallel.

Conclusion

Carry Look-Ahead Adder:

This method significantly reduces propagation delay, making it a compelling choice for applications requiring swift and efficient arithmetic operations. However, the enhanced speed comes with increased complexity in logic design, demanding careful consideration of trade-offs.

THANK
YOU