EE537 Circuit Simulation Lab
Experiment 1

Name: Twinkel Manna
ID Number: 2024EEM1037

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AIM: Design of basic gain stages using MOS transistors.

1 Design a Common-Source (CS) amplifier stage

Design the following configurations of CS amplifier with total current consumption of 100 μA, output voltage swing of 500 mV, CL = 5 pF, fugb > 20 MHz and maximize the voltage gain. Overdrive of the input transistor should be greater than 200 mV. Show the DC operating point simulation and annotate Id, gm, region and overdrive(vdsat). Show the achieved specifications using transient and AC analysis.

1.1 With a Resistive Load

We sketched the schematic for the ac analysis and by maintaing the given requirement we find the value of resistive load R_D which is coming around 13.5K Ω.

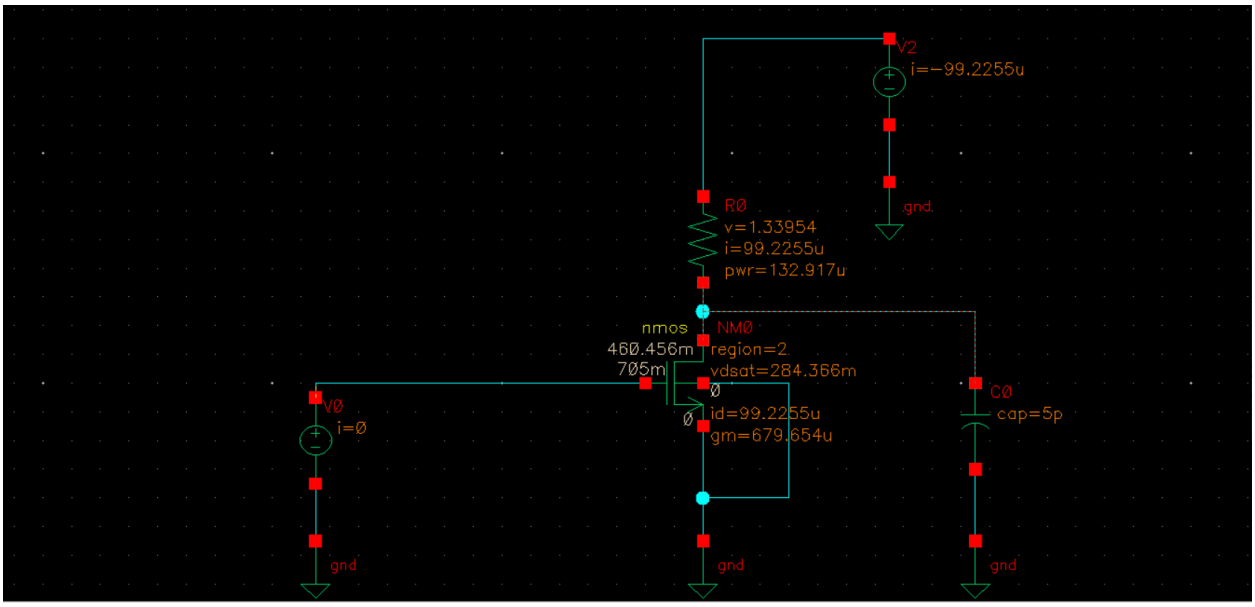

Figure 1: Schematic of CS amplifier with a Resistive Load

According to given condition ,

$$f_{\text{ugh}} > 20MHz \tag{1}$$

$$\frac{g_{\text{m}}}{2\pi C_{\text{L}}} > 20MHz \tag{2}$$

then $g_m > 0.628$mA/V Overall Gain of the amplifier $A_v = -g_m R_D$
If we put the value of g_m and R_D from to plot fig 2 then the gain is 18.8349 dB

Figure 2: Gain of the amplifier

For the Transient analysis,
if I_D=100 μA and R_D = 13.5K Ω and V_D=1.8V then

$$V_{\text{out}} = V_{\text{DD}} - I_{\text{D}}R_{\text{D}} = 1.8 - (100X13.5X10^{-}3) = 0.4V = 450mV \tag{3}$$

We can see from the plot, the output voltage V_{out} is coming around 452mV.

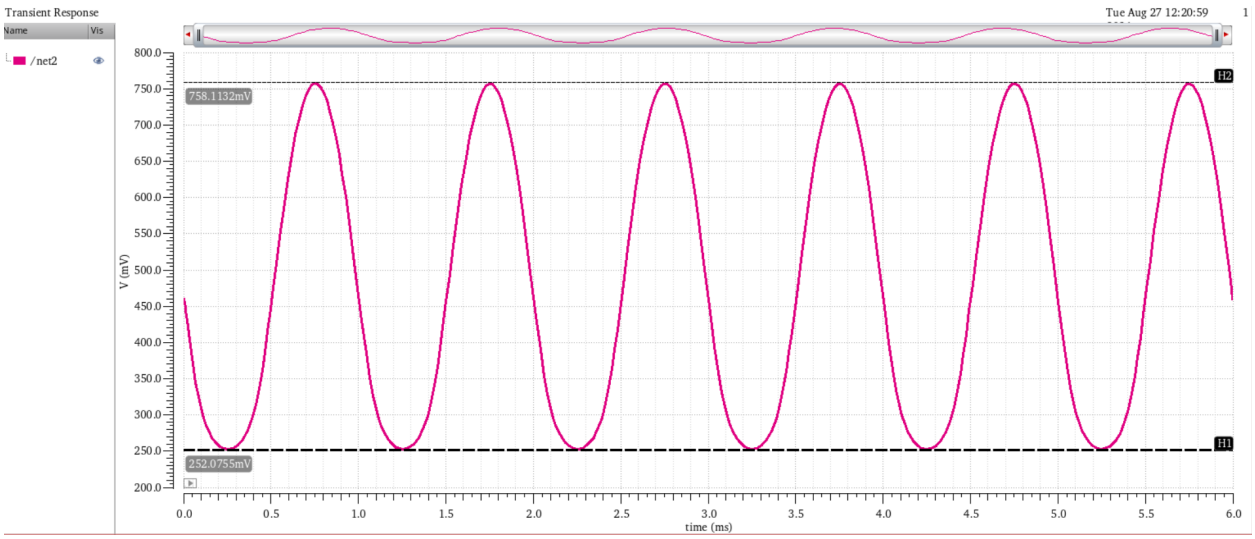

Figure 3: Output voltage in transient analysis

We take a sin pulse of 35mV and plot the output voltage in the fig 3 with the 500mV swing.

1.2 With a diode connected PMOS load.

We make the schematic of the NMOS amplifier with a diode connected PMOS load which acts as a resistive load here and its resistance can be given by $\frac{1}{g_m}$ where g_m is the gain of the PMOS amplifier.

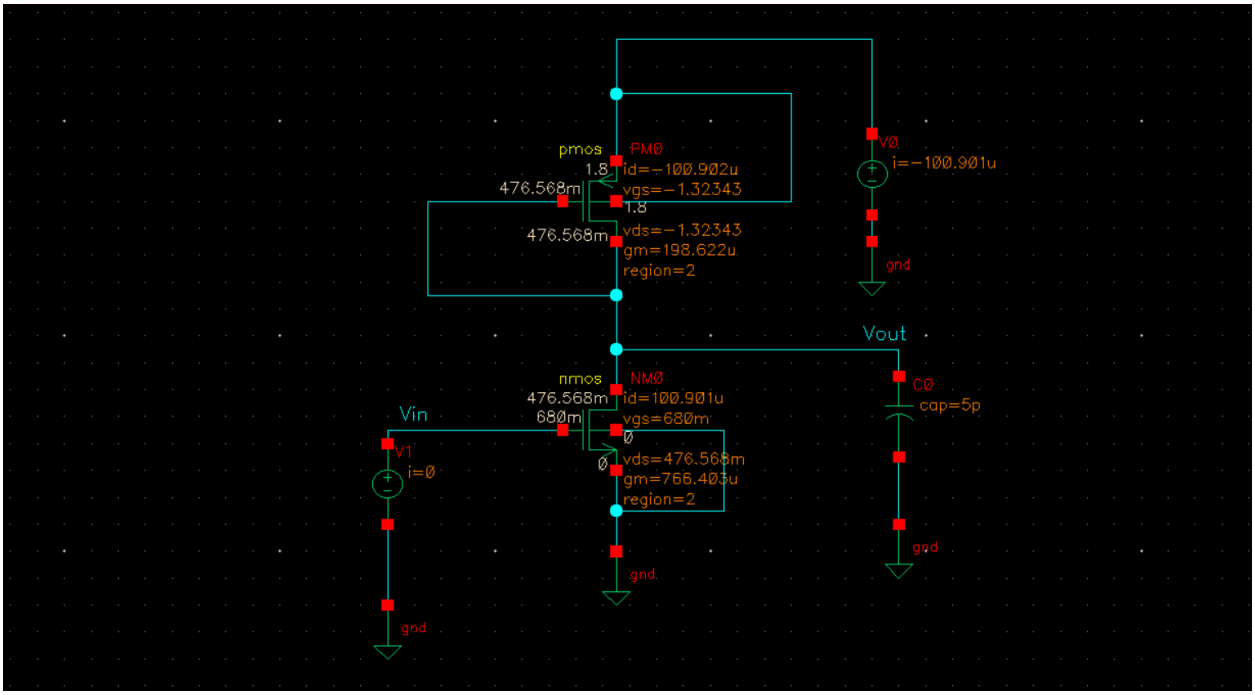

Figure 4: Schematic of CS amplifier with a diode connected PMOS load

The overall gain of the amplifier is given by $A_v = \frac{g_{m_{nmos}}}{g_{m_{pmos}}}$ and if we put the value of the gain of the pmos and nmos from the fig 4 it is coming around 3.85. The gain in dB = 20log(3.85) = 11.72 which is shown in the fig5. Also we maintain the unity gain bandwidth f_{ugh}.

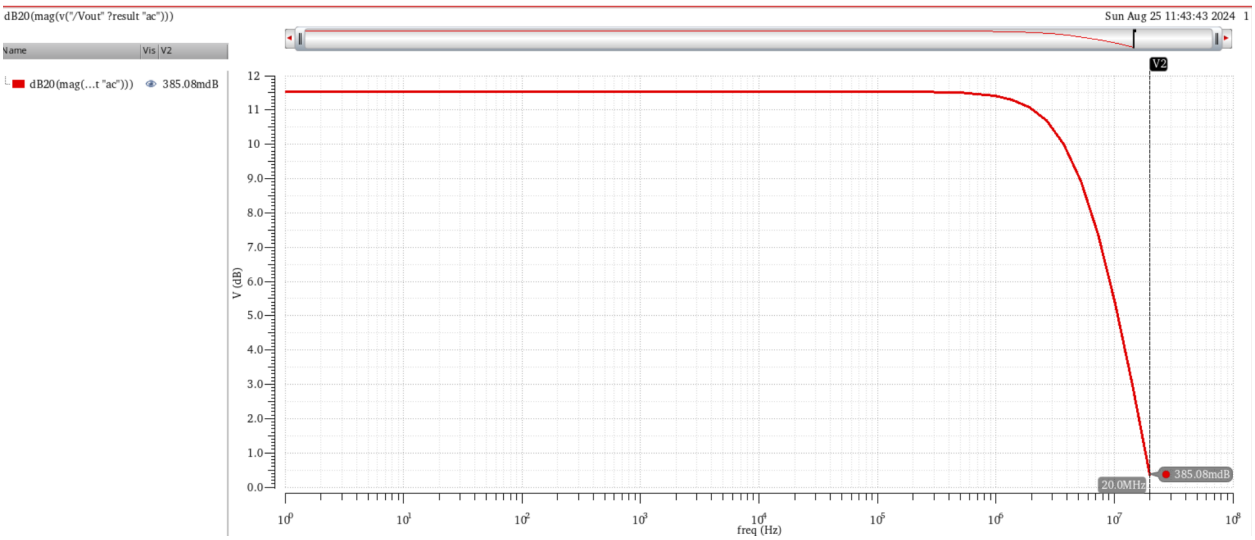

Figure 5: Gain of the amplifier

For the Transient analysis we take a sin pulse of as a voltage source and see the output voltage Vout mentioned in the schematic fig 6

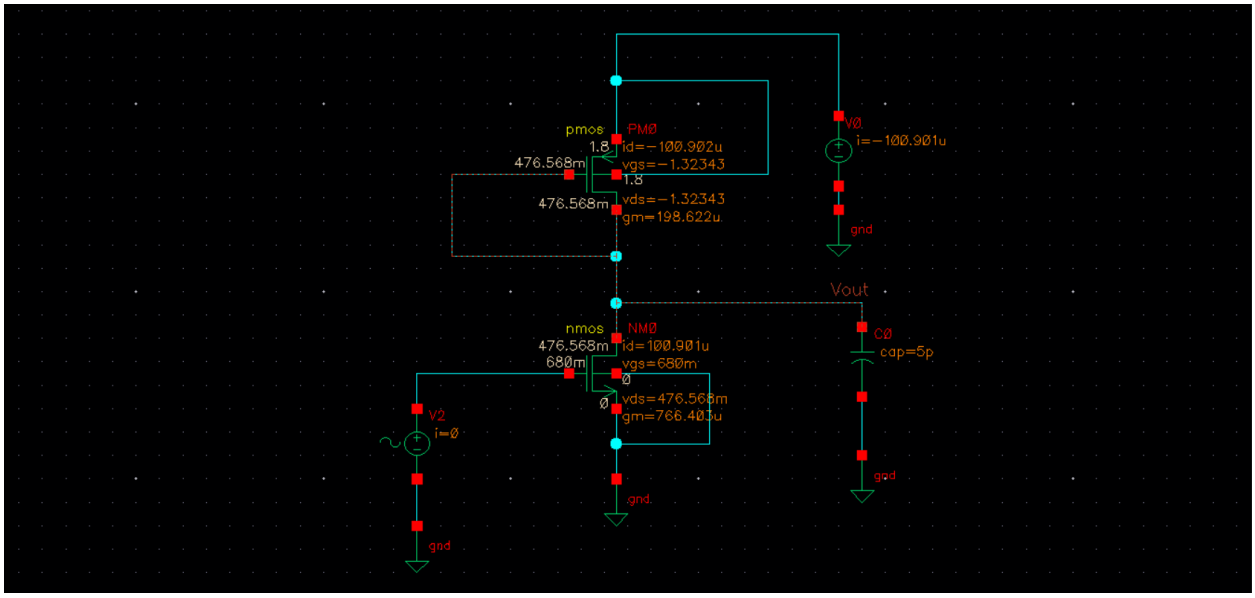

Figure 6: Schematic for the Transient analysis

For the Transient analysis,
if I_D=100 μA and here $R_D = \frac{1}{g_{pmos}} and V_D = 1.8V$ then

$$V_{out} = V_{DD} - \frac{I_D}{g_{pmos}} \tag{4}$$

We can see from the plot, the output voltage V_{out} is coming around 475mV.

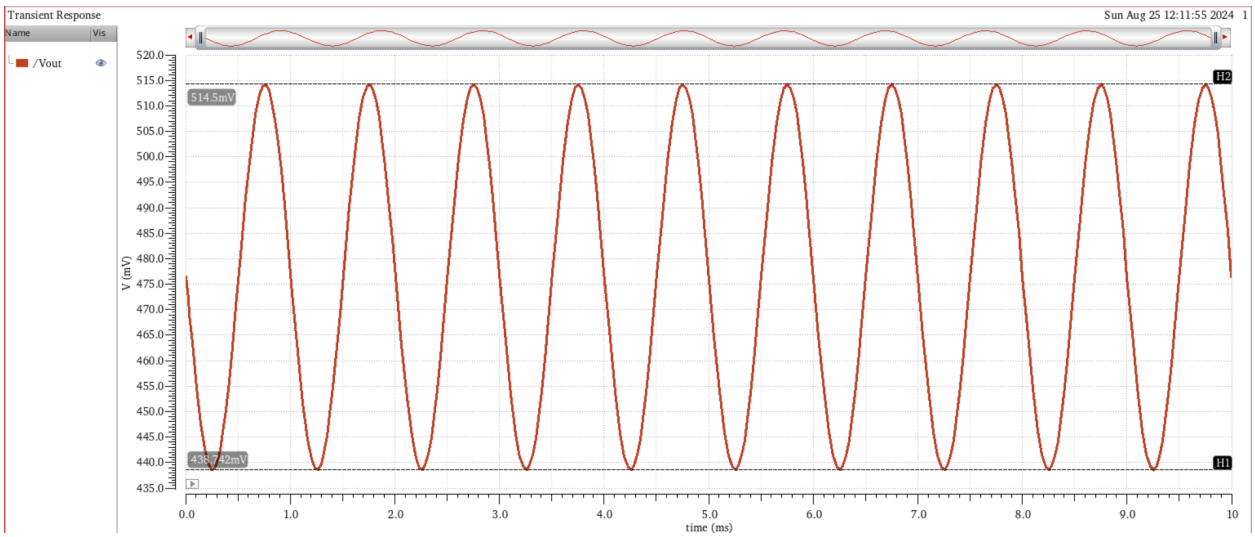

Figure 7: Output Voltage plot in transient analysis

1.3 With a diode connected NMOS load.

We make the schematic of the NMOS amplifier with a diode connected NMOS load which acts as a resistive load here and its resistance can be given by $\frac{1}{g_m}$ where g_m is the gain of the NMOS amplifier.

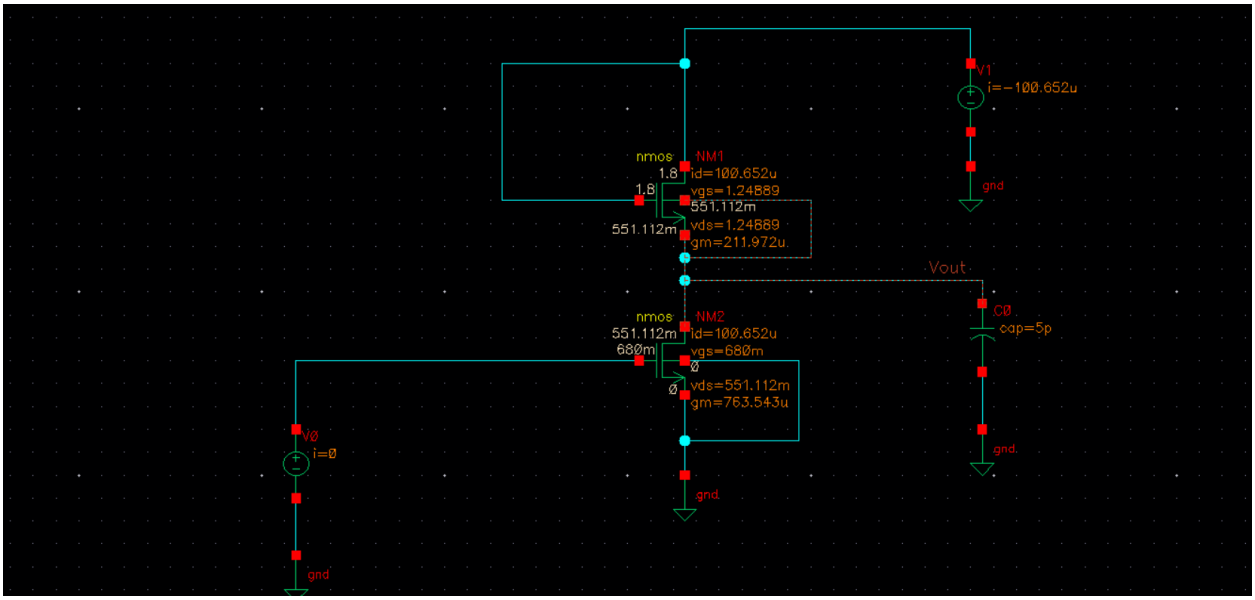

Figure 8: Schematic of the CS amplifier with a diode connected NMOS load

The overall gain of the amplifier is given by $A_v = \frac{gm_{nmos2}}{gm_{nmos1}}$ and if we put the value of the gain of the pmos and nmos from the fig 8 the it is coming around 3.61. The gain in dB = 20log(3.85) = 11.13 which is shown in the fig 9. Also we maintain the unity gain bandwidth f_{ugh}.

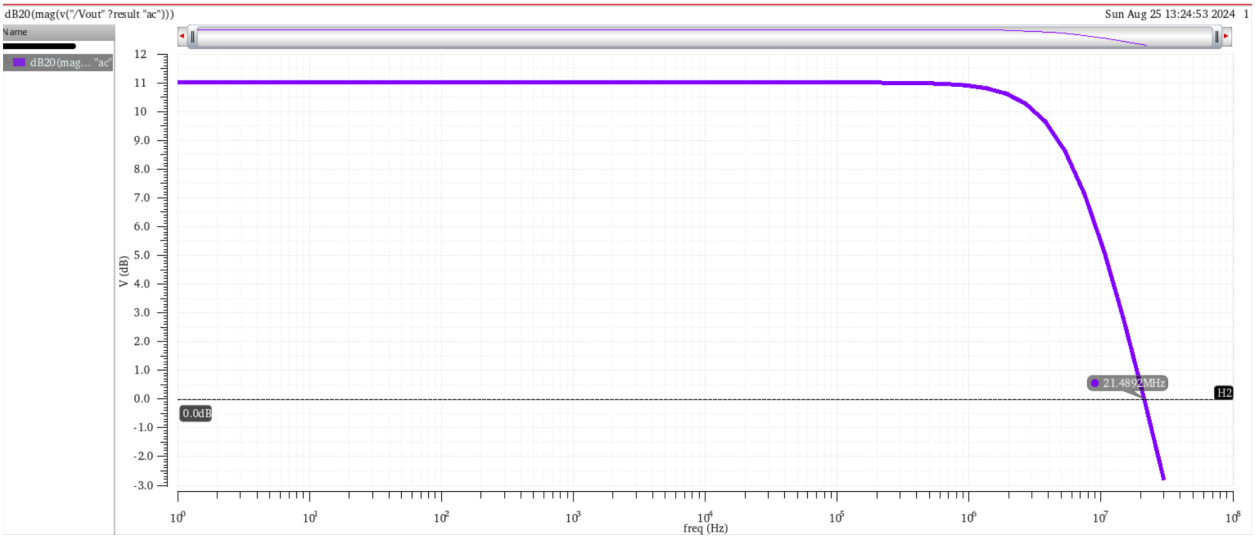

Figure 9: Gain of the amplifier

For the Transient analysis we take a sin pulse of as a voltage source and see the output voltage Vout mentioned in the schematic fig 10.

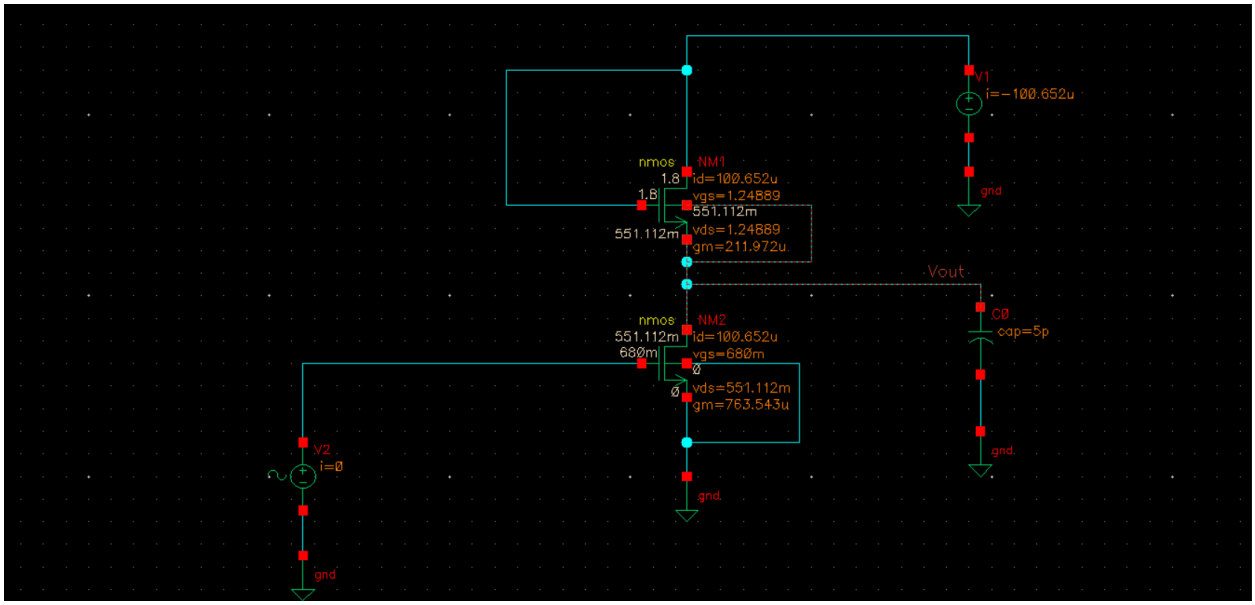

Figure 10: Output Voltage plot in transient analysis

For the Transient analysis,
if I_D=100 μA and here $R_D = \frac{1}{g_{nmos}} and V_D = 1.8V$ then

$$V_{out} = V_{DD} - \frac{I_D}{g_{nmos}} \tag{5}$$

We can see from the plot, the output voltage V_{out} is coming around 550mV.

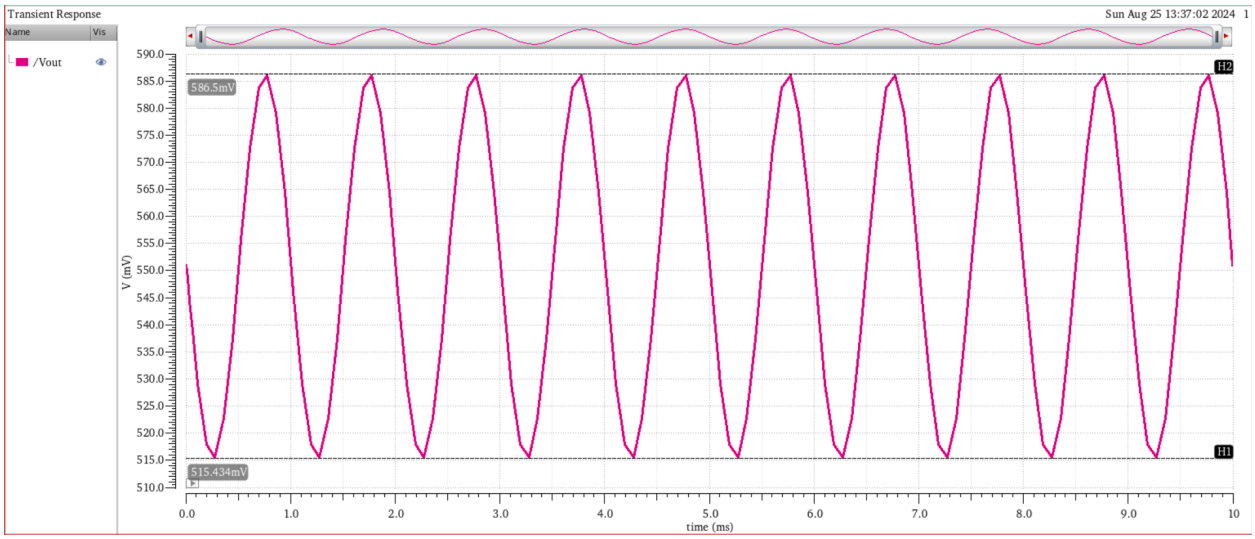

Figure 11: Schematic for the Transient analysis

1.4 With a PMOS current source as load.

We make the schematic of the NMOS amplifier with a PMOS current source as load which acts as a current source here.

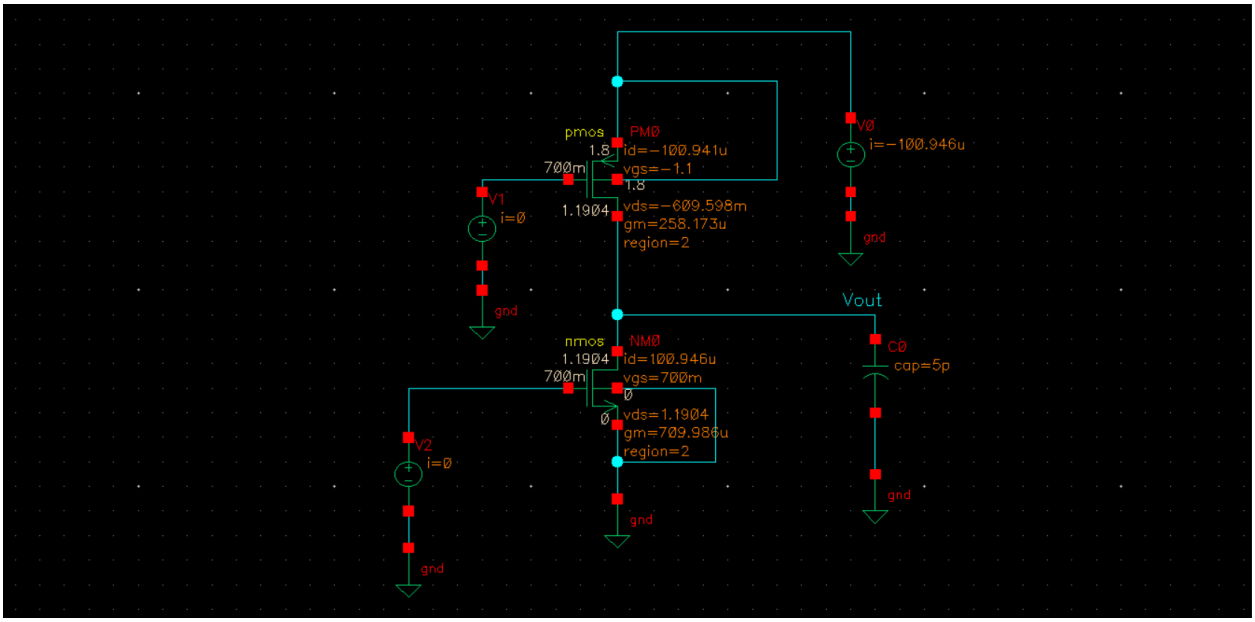

Figure 12: schematic of the CS amplifier with a PMOS current source as load

The overall gain of the amplifier is given by $A_{\mathrm{v}} = g_{\mathrm{nmos}}(r_{01}||r_{02})$ where r_{01} and r_{02} is coming due to channel length modulation .

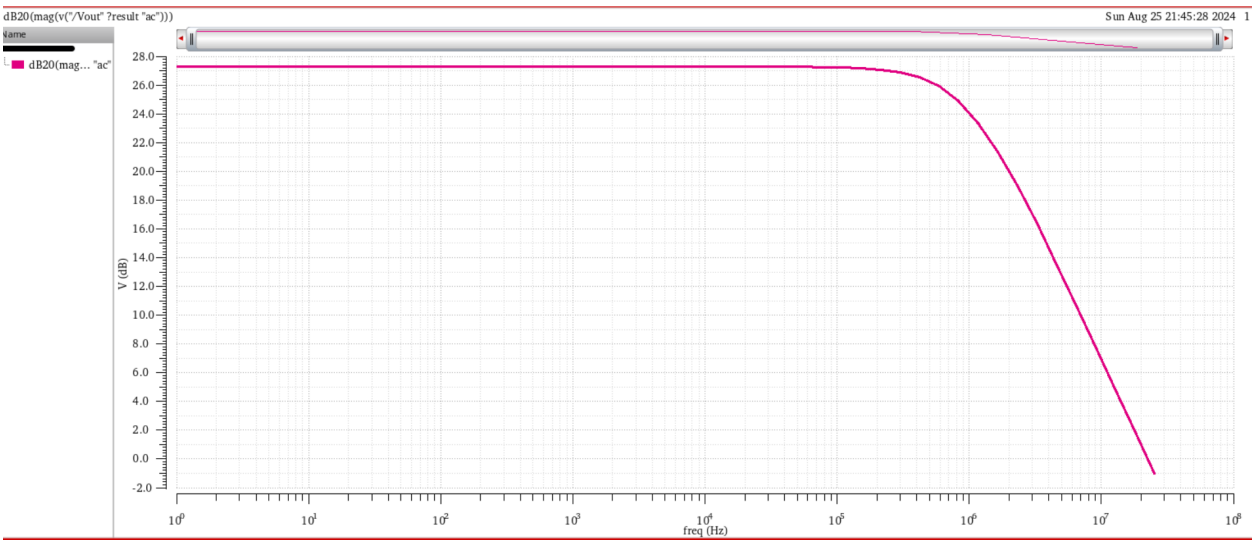

Figure 13: Gain of the amplifier

For the Transient analysis we take a sin pulse of as a voltage source and see the output voltage Vout mentioned in the schematic fig 14

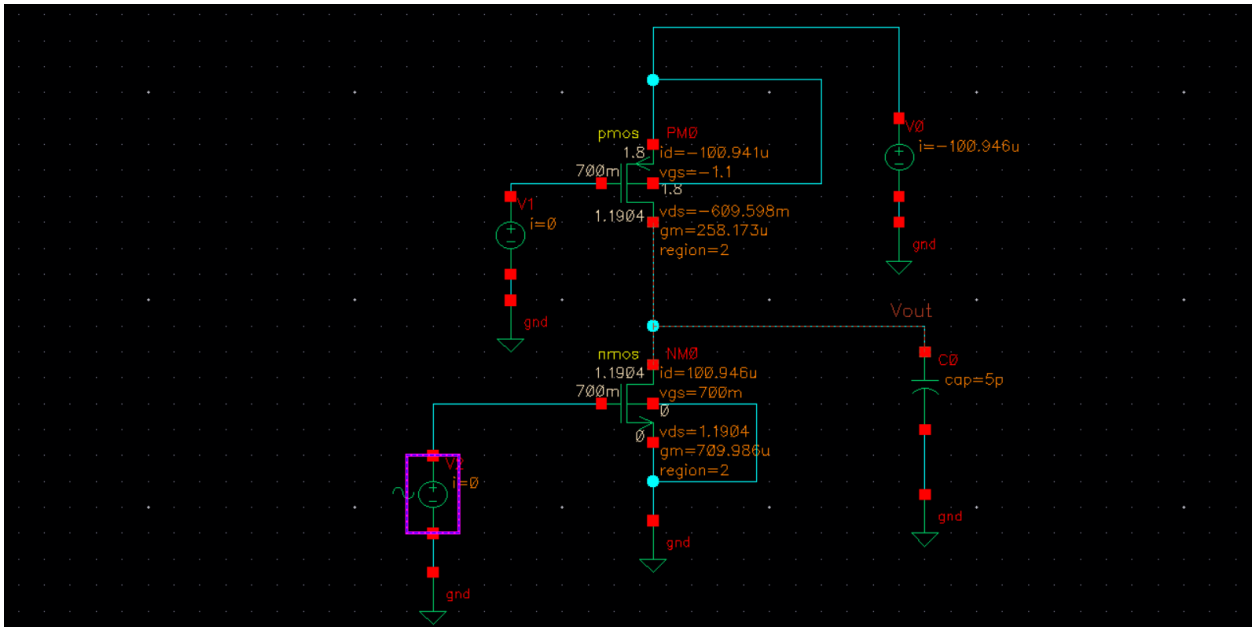

Figure 14: Schematic for the Transient analysis

The output plot for the transient analysis,

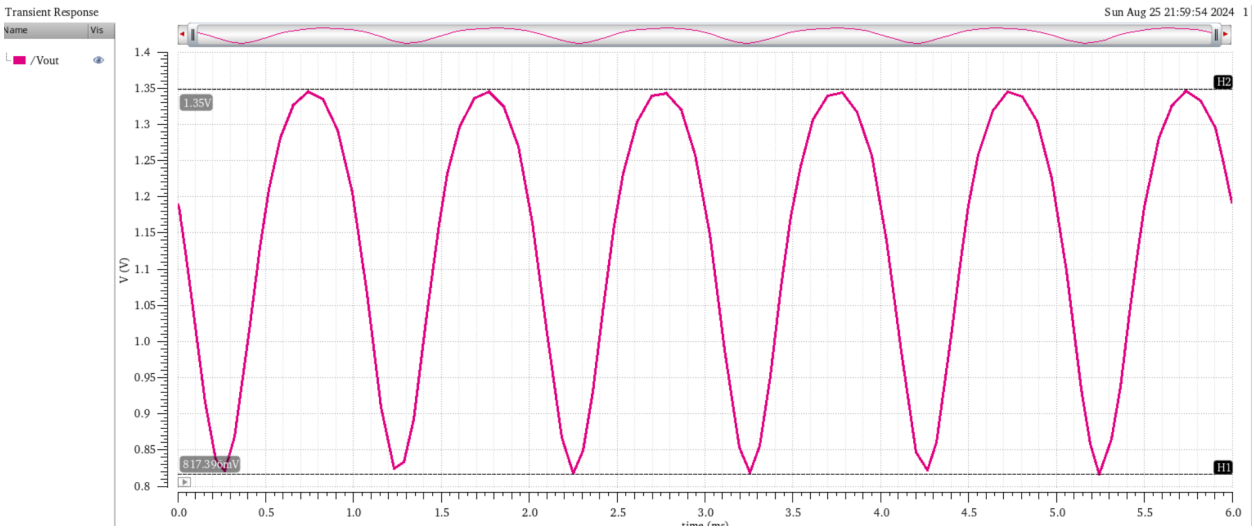

Figure 15: Output Voltage plot in transient analysis

1.5 With a resistive load and source degeneration.

We make the schematic of the NMOS amplifier with a resistive load of 1K Ω and source degeneration.

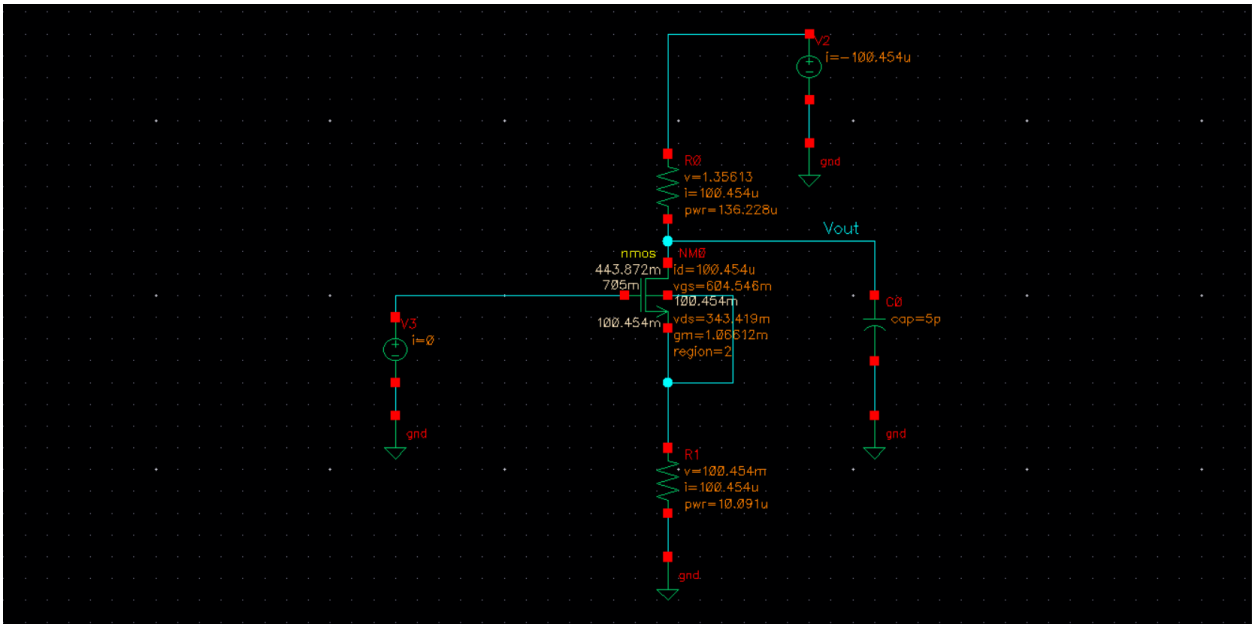

Figure 16: schematic of the CS amplifier with a resistive load and source degeneration

The overall gain of the amplifier is given by $A_v = -\frac{R_D}{\frac{1}{g_m}+R_s}$ where g_m=1.06612 mA/V , R_D = 13.5KΩ and R_s =1K Ω The gain is also coming around 16.85 dB which matches with the value in the plot 17.

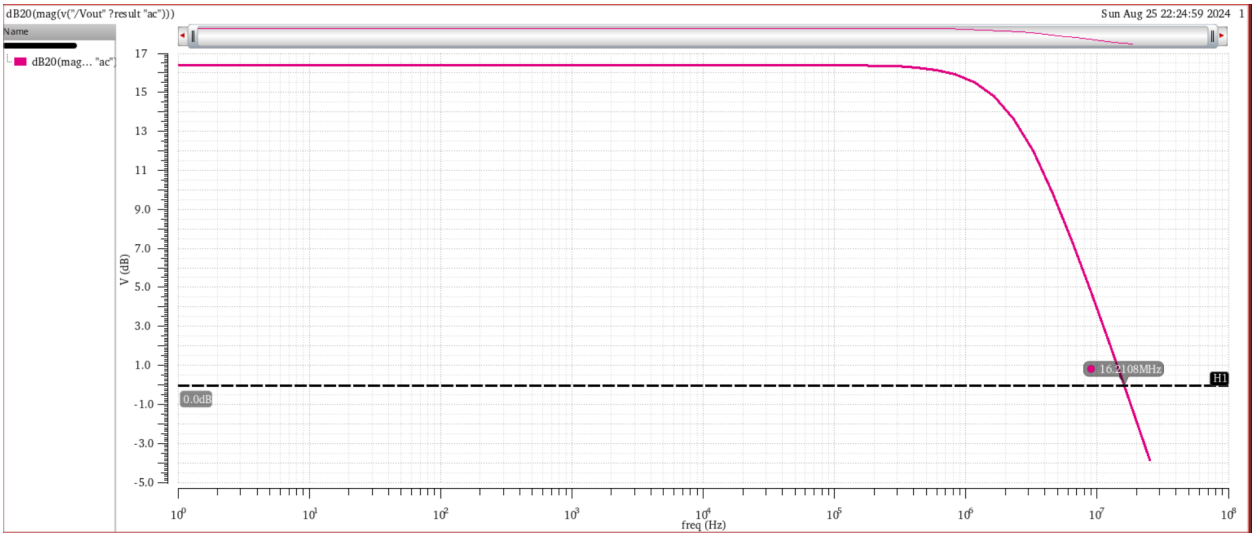

Figure 17: Gain of the amplifier

For the Transient analysis we take a sin pulse of as a voltage source and see the output voltage Vout mentioned in the schematic fig 18

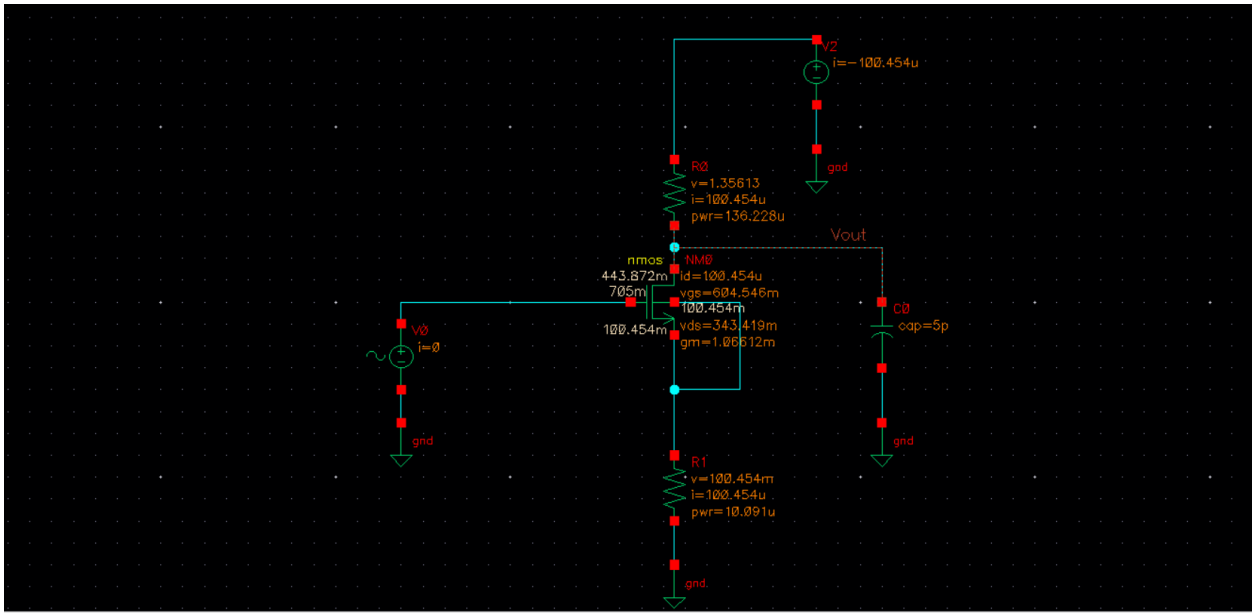

Figure 18: Schematic for the Transient analysis

The output plot for the transient analysis,

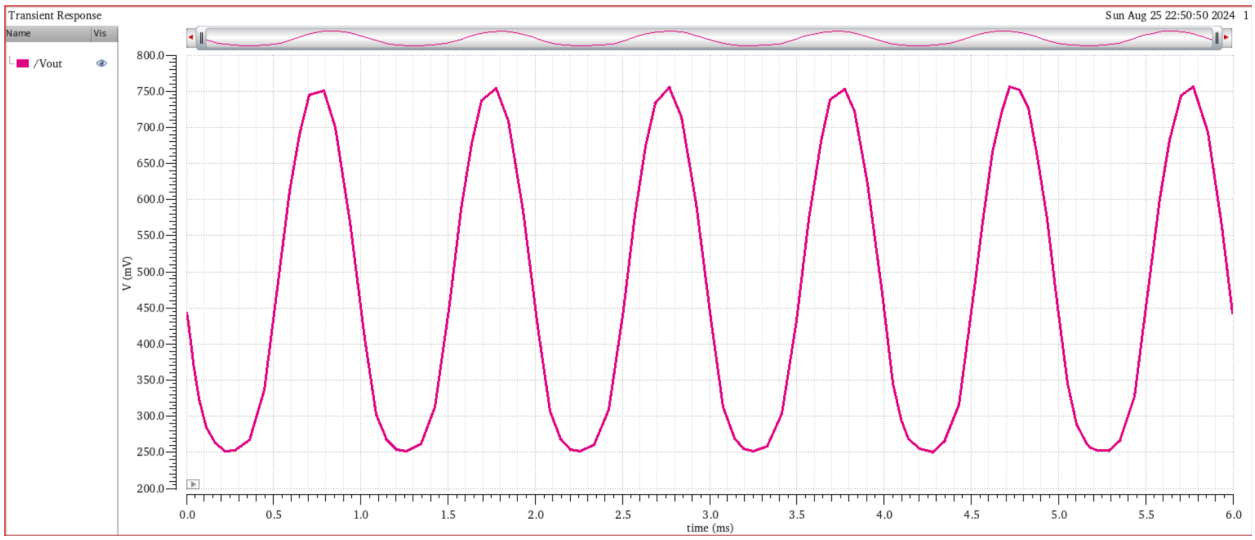

Figure 19: Output Voltage plot in transient analysis

Here for calculating the output impedance , we take a test ac source of 1V and calculate impedance i.e. $\frac{outputcurrent}{outputvoltage}$

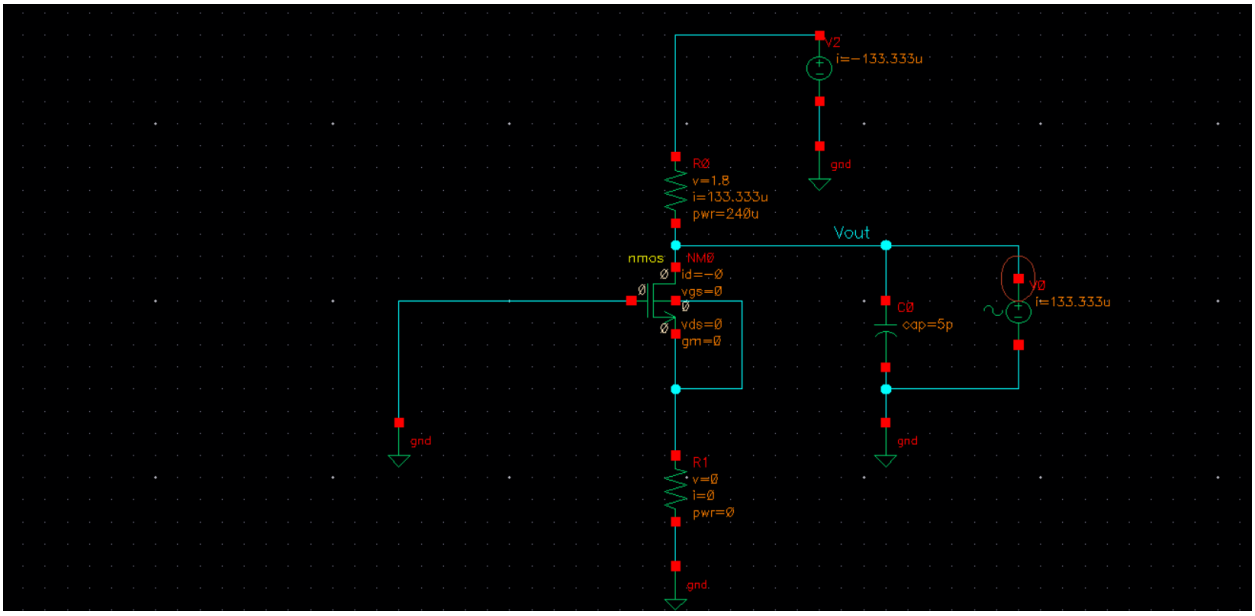

Figure 20: Schematic for finding output impedance

We plot the $\frac{1}{current}$ so we get the impedance at the output node.

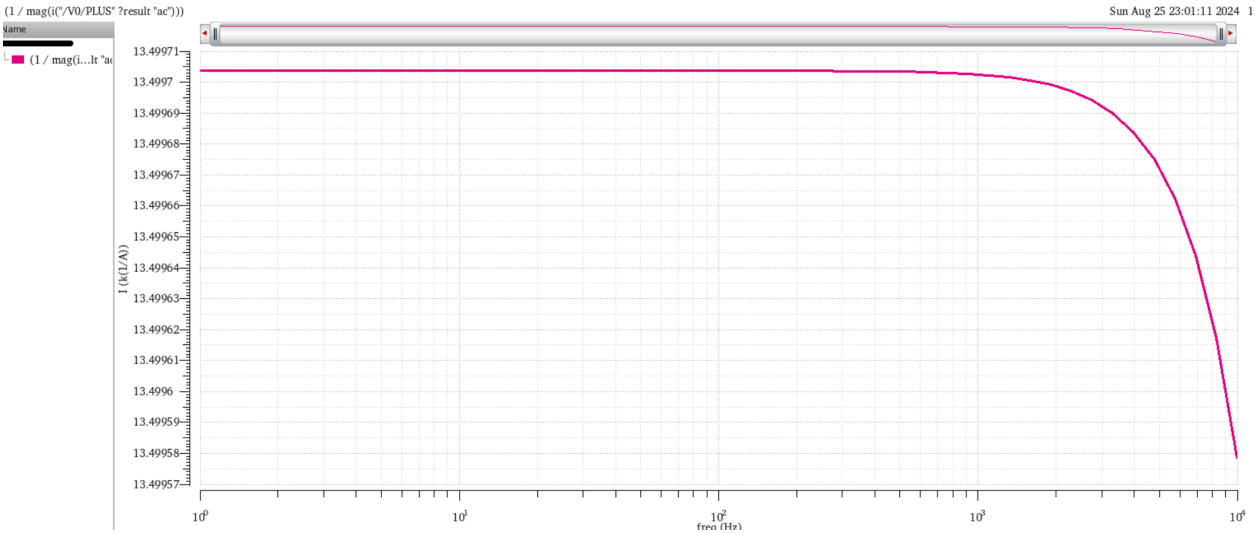

Figure 21: Output impedance

2 Design a Common-Gate (CG) amplifier stage

2.1 CG amplifier with resistive load

Design the CG amplifier with resistive load, total current consumption of 100 μA, output voltage swing of 500 mV, CL = 5 pF, fugb > 20 MHz and maximize the voltage gain. Overdrive of the input transistor should be greater than 200 mV. Source of the amplifier is driven by an ideal voltage source. Show the DC operating point simulation and annotate Id, gm, region and overdrive(vdsat). Show the achieved specifications using transient and AC analysis.

We make the schematic of the common gate NMOS amplifier with a resistive load. We take it as 5kΩ

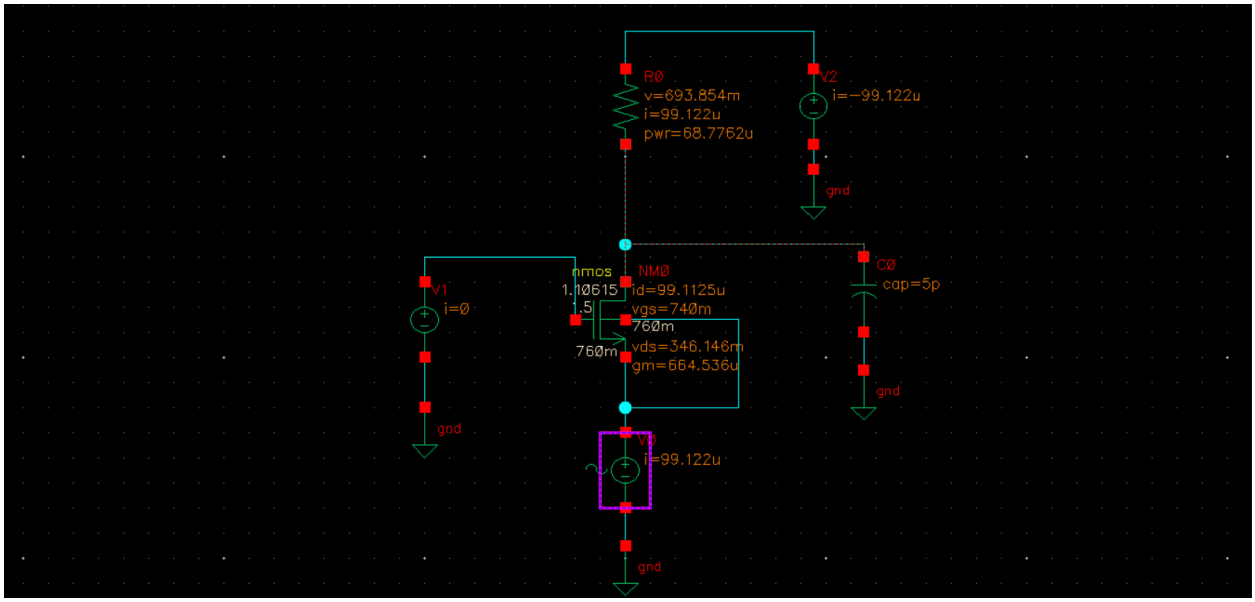

Figure 22: schematic of the CG amplifier with a resistive load

Here the overall gain at the output node, $A_{\mathrm{v}} = g_{\mathrm{nmos}} R_{\mathrm{D}} (1 + \eta)$

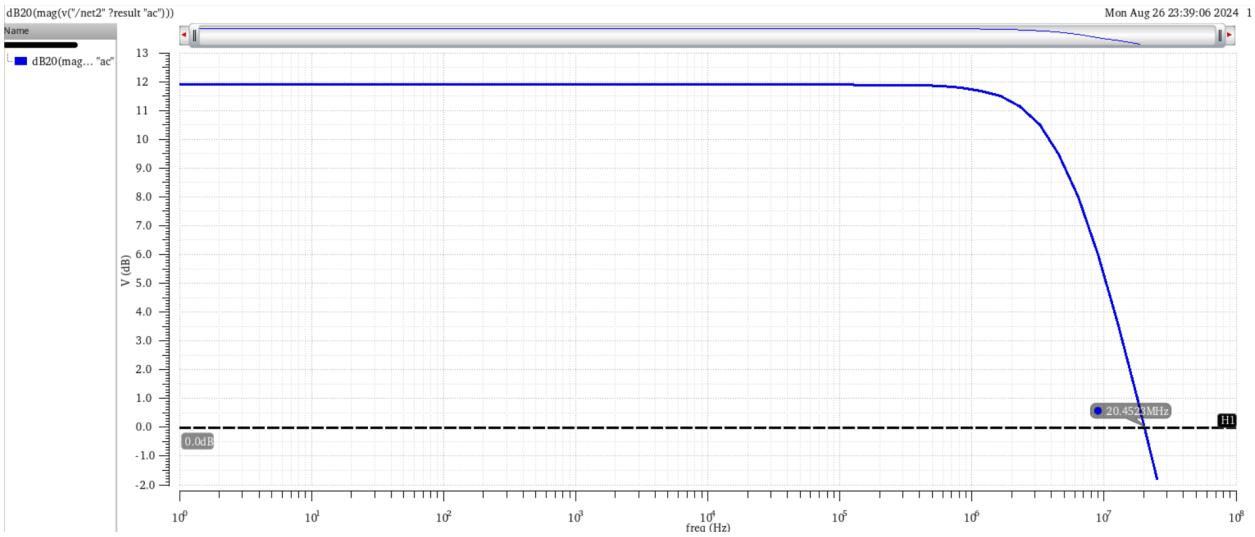

Figure 23: Gain of the amplifier

The transient analysis for the give problem,

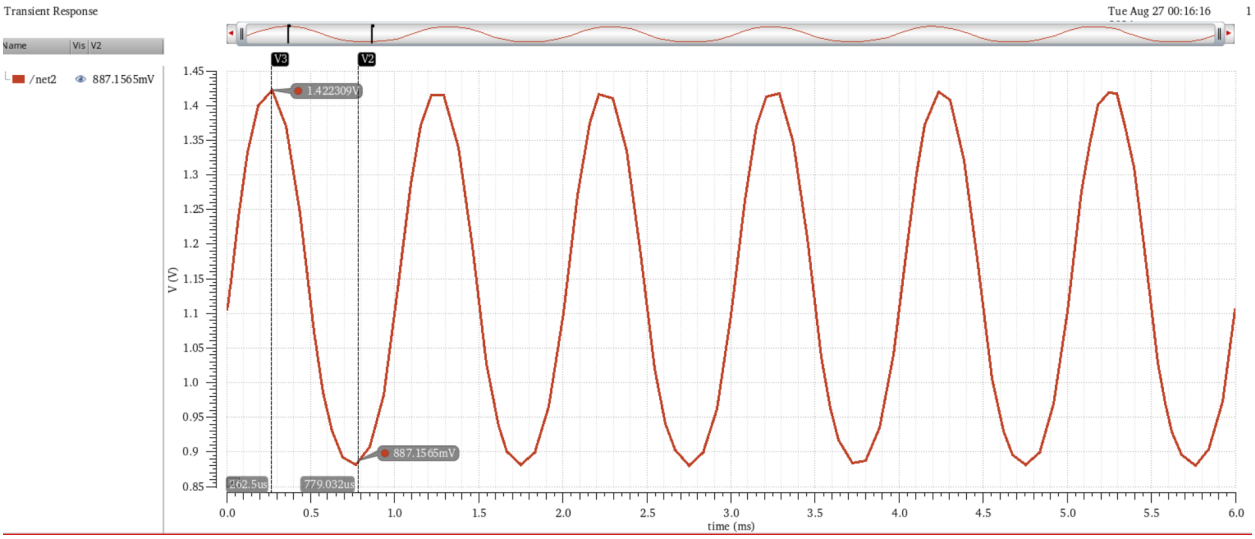

Figure 24: Output Voltage plot in transient analysis

2.2 Determine the input impedance by simulation and verify the same by hand calculations.

Input Impedance is given by,

$$R_{\text{in}} = \frac{r_0 + R_{\text{D}}}{1 + (g_{\text{m}} + g_{\text{mb}})r_0} \tag{6}$$

if we neglect channel length modulation and body effect then the R_{in} comes around 7.51 by putting the value of g_m and R_D from the fig 22 and it comes around 7.51 which matches with the plot in fig 25.

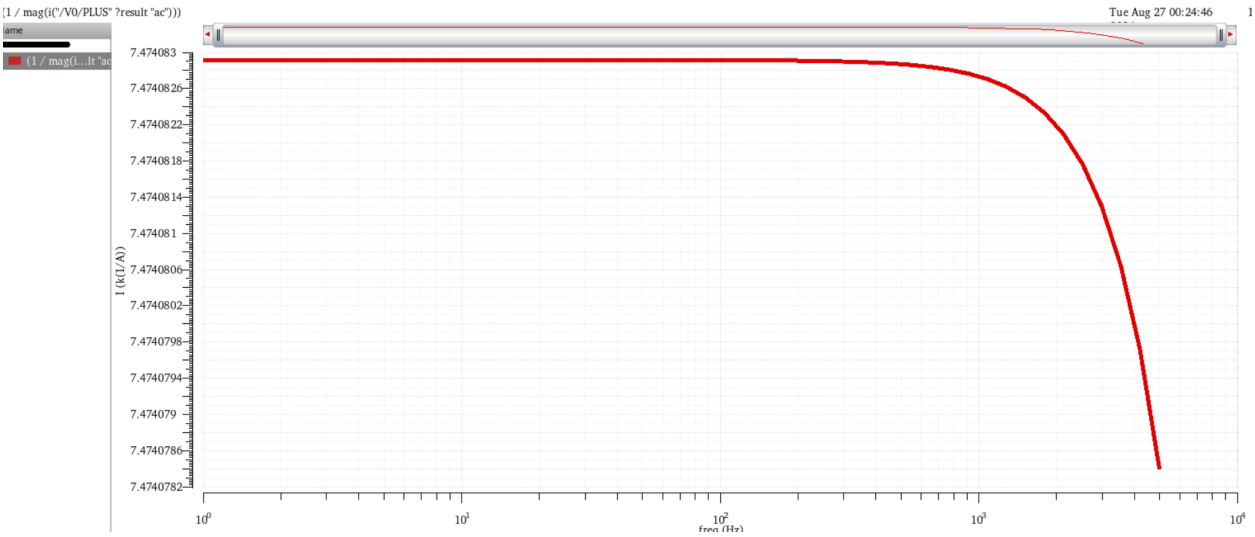

Figure 25: Input Impedance plot

2.3 overall gain of the amplifier

Find out the overall gain of the amplifier when the amplifier is driven by a voltage source having source resistance of 1 KΩ. Modify the gate bias voltage to maintain same overdrive and current of the transistor. Explain the difference (if any) between gain using ideal voltage source and gain using voltage source with source resistance.

We make the schematic of the common gate NMOS amplifier with a resistive load of 5kΩ and a resistance at source node .

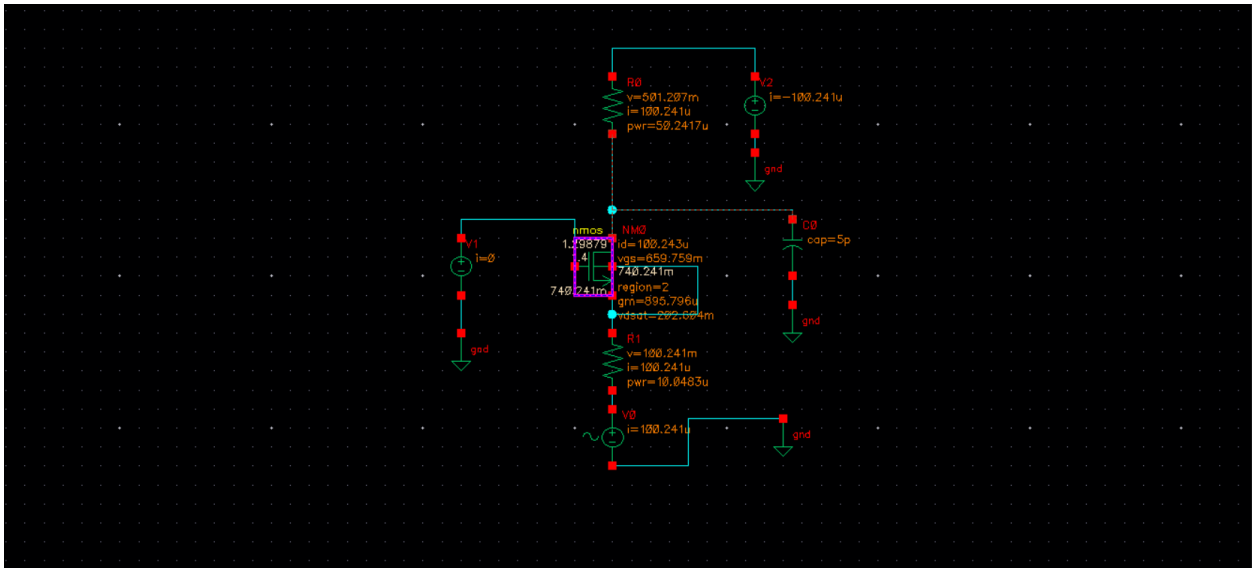

Figure 26: Schematic of a CG amplifier with resistive load and a source connected load

The overall gain of the amplifier is $A_v = \frac{g_m R_D}{1+g_m R_s}$ where g_m=895.796 μA/V , R_D = 5KΩ and R_s =1K Ω The gain is also coming around 7.467 dB which matches with the value in the plot 27.

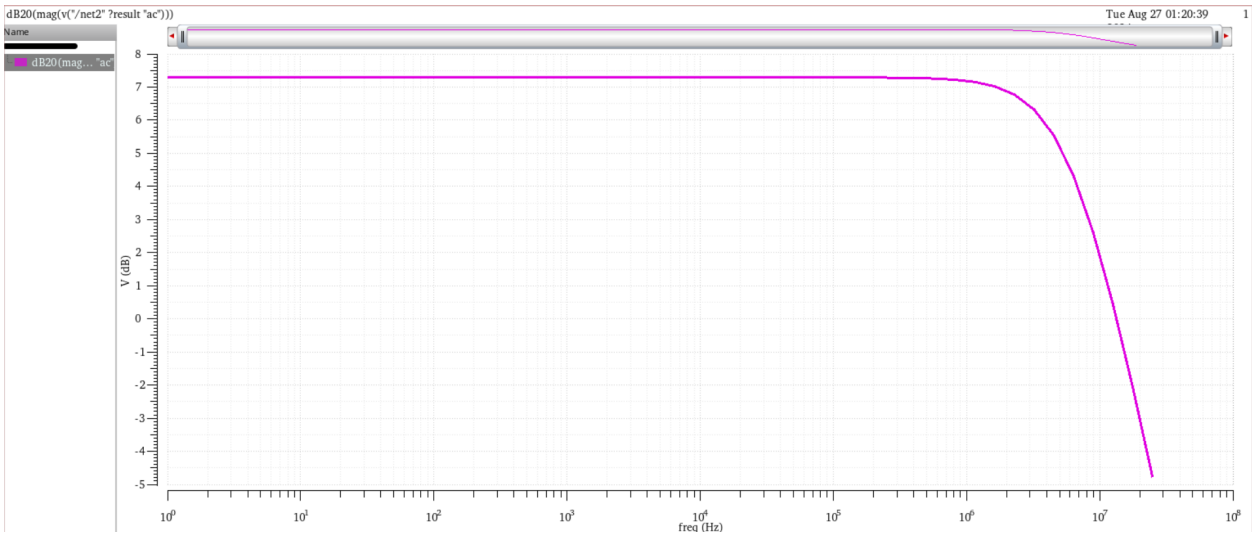

Figure 27: Gain of the amplifier

There is a difference in between the gain from the previous case because in this case the input impedance is increased from previous case so the overall gain is reduced.