CA-IS305x 5kVRMS Isolated CAN Transceiver

1Product Features

• Compliant with ISO 11898-2 physical layer standard •

Integrated protection features support reliable data communications

ÿ Provides 3.75kVRMS (DUB8) or 5kVRMS (wide-body SOIC) isolation

Withstand voltage ÿ ±150kV/ÿs typical CMTI

ÿIsolation barrier life: > 40 years ÿ ±58V

fault protection on CANH, CANL bus pins ÿ ±30V extended common mode input

range (CMR) ÿTransmitter timeout detection avoids bus

lockup, allowing minimum transmission rate of 5.5 kbps ÿThermal shutdown • Data rate

up to 1Mbps • Ultra-low

latency: 150ns (typ),

210ns (max) • 2.5V to 5.5V logic side supply

range, can directly interface with 2.7V,

3V, 3.3V or 5V CAN controller

• When unpowered, the device maintains an ideal passive behavior and does not generate any

• Wide

operating temperature range: -40 °C to 125 °C • Available in 8-pin and 16-

pin wide-body SOIC packages, and small 8-pin DUB packages • Safety certifications: ÿ VDE in

accordance with DIN VDE V

0884-17 (VDE V 0884-17)

Certification

ÿUL 1577 certified, 5 kVRMS @ 1 minuteÿIEC 62368-1 and IEC 61010-1

certified for 5kVRMS reinforced isolationÿCQC certified for GB 4943.1-2011 and GB

8898-2011 for

reinforced isolation

2 Typical Applications

• Industrial field networks •

Building automation •

Security systems •

Transportation

equipment • Medical equipment

• Telecommunications systems

• HVAC

3 Overview

The CA-IS305x is an isolated controller area network (CAN) transceiver that complies with the ISO11898-2 physical layer specification. The logic input and output buffers in this series of devices are isolated by a silicon dioxide (SiO2) insulation barrier, which can withstand an isolation voltage of up to 5000VRMS (60s) (wide-body SOIC package) and a typical CMTI of ±150kV/ÿs. The insulation barrier blocks the ground loop between the logic side and the bus side, which helps reduce the noise caused by the high ground potential difference between the ports and ensures the correct transmission of data.

The CA-IS305x uses a single 2.5V to +5.5V power supply on the logic side, which is convenient for connecting CAN controllers with different voltages. With an external isolated power supply, a complete isolated CAN port can be formed. The transceiver supports a transmission rate of up to 1Mbps, and provides current limiting protection, thermal protection, and ±58V overvoltage protection at the transmitter output. The dominant state timeout detection can avoid bus lockout caused by controller errors or TXD input failures. In addition, the CAN receiver input of this series of devices has a common mode input range (CMR) of ±30V, which is far beyond the -2V to +7V range defined in the ISO 11898 specification. Provide reliable protection for the system.

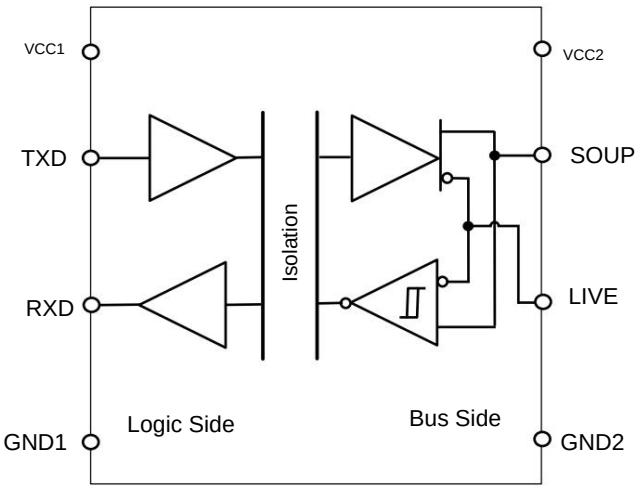
Both CA-IS3050 and CA-IS3052 are available in wide-body 8-pin wide-body SOIC and 16-pin wide-body SOIC packages, compatible with most industry-standard isolation

CAN transceiver; In addition, the CA-IS3050 is available in a small footprint, 8-pin SOP package (DUB8) with an isolation voltage rating of 3750VRMS. All devices operate over the –40°C to 125°C temperature range.

Device information

Device Model	package	Package size (nominal value)
CA-IS3050G	SOIC8-WB	5.85mm*7.50mm
CA-IS3052G		
CA-IS3050W	SOIC16-WB	10.30mm*7.50mm
CA-IS3052W		
CA-IS3050U	DUB8	6.35mm*9.20mm

Simplified Functional Block Diagram



4Ordering Information

Table **4-1** Valid ordering device models

model	VCC1(V)	VCC2(V)	transfer speed (Kbps)	Electrical isolation (VRMS)	Encapsulation
CA-IS3050G	2.5~5.5	4.5~5.5	1000	5000	SOIC8-WB
CA-IS3052G	2.5~5.5	4.5~5.5	1000	5000	SOIC8-WB
CA-IS3050W	2.5~5.5	4.5~5.5	1000	5000	SOIC16-WB
CA-IS3052W	2.5~5.5	4.5~5.5	1000	5000	SOIC16-WB
CA-IS3050U	2.5~5.5	4.5~5.5	1000	3750	DUB8

Table of contents

5 Revision History

Revision Number	modify the content	Revision Date	page number
Revision 0 Initial Version Update 7.2 ESD Rating			N/A
Revision A	Updated Isolation Characteristics,		6
	DTI updated from 14um to 19um CMTI Typical updated to 150kV/us CMTI		7
	Minimum updated to 100kV/us		7
			7
Revision B Updated 7.6 related safety certification information Revision C Added			8
DUB8 package part number			2
Revision D	Updated VISO of CA-IS3050U to 3750V Updated VIOTM of		7
	CA-IS3050U to 5300V Revision E Changed taping data, added		7
soldering information Updated 6.1 DUB8 pin configuration Updated 7.1 Bus side			22, 23
Revision F	maximum voltage to ground is ±58V,		4
	maximum differential voltage is ±58V Updated 7.2 Bus to ground ESD HBM Updated 7.3 TXD input high and low		6
	voltage, differential input voltage Updated 7.3		6
	Thermal shutdown temperature, receiver high and low level output current is		6
	±4mA Updated Table 7-7 ICC2 current typical value Updated Table 7-7 VO(D) bus output voltage		6
	(dominant); IOS(SS) short circuit steady state		9
	output current Updated Table 7-7 Receiver input threshold voltage Updated Table 7-7 Bus input capacitance		9
	Updated Table 7-8 Driver and receiver timing characteristics		9
	Deleted Figure 8-12 Updated application		9
	information block diagram N/A Version 1.01 Updated DUB8 package		10
	size diagram		14
			17
Version 1.00			N/A
			19

Version 1.02	VIORM Table*6-1ÿ* Table*6-2* Pin Definition		4, 5
	value *9-2* transmitter truth table		15
to 1414V, the VIOWM AC RMS value to 1000V, and			18
the DC value to 1414V.			7
Version 1.05 Updated VCC1 and VCC2 UVLO Version 1.06 Updated			9
POD and taping information Version 1.07 Updated UVLO description,		2022/12/20	19,20,21,23
added upper and lower limits		2023/04/27	9
Version 1.08 Update VDE certification information		2023/11/13	7,8

6 Pin Function Description

6.1 CA-IS3050x Pin Configuration and Function Description

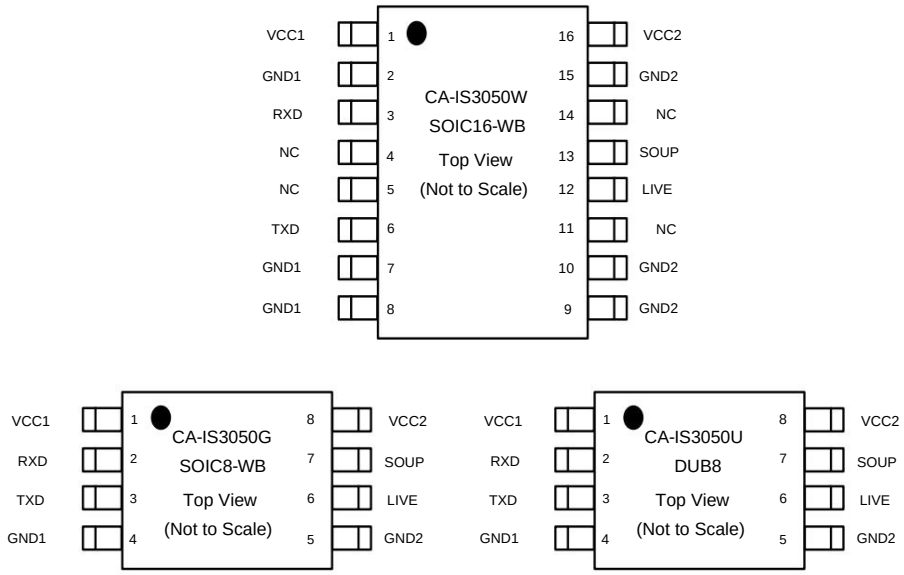
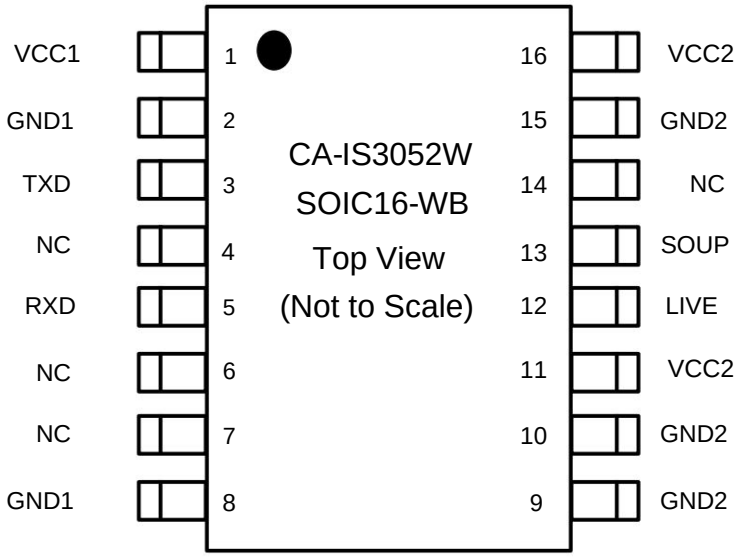


Figure **6-1 CA-IS3050** pin configuration

Table **6.1-1 CA-IS3050** pin function description

Pin Name	Pin Number		type	describe
	SOIC16	**SOIC8/DUB8**		
VCC1	1	1	power supply	Logic side power supply, to power the logic side. Connect at least one A 0.1ÿF bypass capacitor should be installed close to the power pin.
GND1	2, 7, 8	4	land	Logic side ground, ground reference point for logic side signals.
RXD	3	2	Number I/O	Receiver data output terminal, when the bus is in recessive state, RXD outputs high level; when the bus is explicit In the active state, RXD outputs a low level.
NC	4, 5, 11, 14	-	-	Floating, do not connect these pins externally, leave them floating.
TXD	6	3	Number I/O	Transmitter data input terminal. When TXD is low, CANH and CANL outputs are dominant. state; when TXD is high level, CANH and CANL outputs are recessive state.
GND2	9, 10, 15	5		Bus side ground, GND2 is the reference point for CAN bus side signals.
LIVE	12	6	Ground Bus I/	CAN bus differential input/output, low level logic terminal.
SOUP	13	7	O Bus I/O	CAN bus differential input/output, high level logic terminal.
VCC2	16	8	power supply	Bus side power supply, to power the bus side circuit. Connect at least one A 0.1ÿF bypass capacitor should be installed close to the power pin.



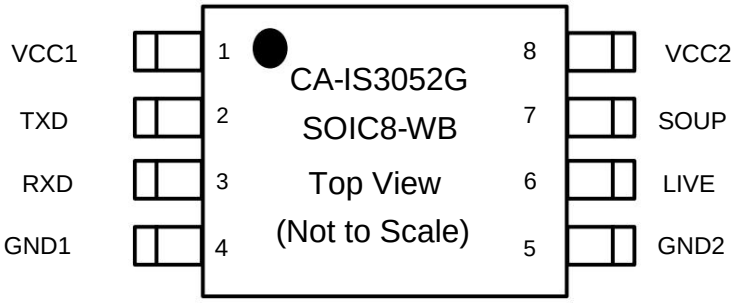


Figure **6-2 CA-IS3052** pin configuration

Table **6.2-2 CA-IS3052** pin function description

Pin Name	Pin Number		type	describe
	SOIC16	**SOIC8**		
VCC1	1	1	power supply	Logic side power supply, to power the logic side. Connect an external capacitor of at least 0.1ÿF between VCC1 and GND1 . The bypass capacitor should be installed close to the power pin.
GND1	2, 8	4	land	Logic side ground, ground reference point for logic side signals.
TXD	3	2	Number I/O	Transmitter data input terminal. When TXD is low, CANH and CANL outputs are dominant. state; when TXD is high level, CANH and CANL outputs are recessive state.
NC	4, 6, 7, 14	-	-	Floating, do not connect these pins externally, leave them floating.
RXD	5	3	Number I/O	Receiver data output terminal, when the bus is in recessive state, RXD outputs high level; when the bus is dominant In the status, RXD outputs low level.
GND2	9, 10, 15	5		Bus side ground, GND2 is the reference point for CAN bus signals.
LIVE	12	6	Ground Bus I/	CAN bus differential input/output, low level logic terminal.
SOUP	13	7	O Bus I/O	CAN bus differential input/output, high level logic terminal.
VCC2	11, 16	8	power supply	Bus side power supply, to power the bus side circuit. Connect at least one A 0.1ÿF bypass capacitor should be installed close to the power pin.

7.1 Absolute Maximum Ratings 1

parameter		Minimum Maximum Unit		
VCC1 or VCC2	Power supply	–0.5	6.0	IN
WE	voltage 2 Logic side signal input voltage	–0.5	VCC1 + 0.53	IN
VCANH or VCANL	(TXD) Bus side signal voltage (CANH, CANL) Bus	–58	58	IN
VCANH to VCANL	side differential signal voltage VID	-58	58	
IO	Receiver output current	–15	15	mA
TJ	Junction		150	°C
TSTG	temperature Storage temperature range	–65	150	°C

Note:

1. Operating conditions equal to or exceeding those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are device ratings, not operating conditions, and cannot be inferred from them.
   Whether the product can work normally. If the device works beyond the maximum rating for a long time, it will affect the reliability of the product and even cause product damage.
2. Except for the bus differential output/input voltage, all voltage values are relative to the local ground (GND1 or GND2) and are peak voltage values.
3. The maximum voltage must not exceed 6 V.

7.2 ESD Rating

		Numerical Unit	
VESD Electrostatic Discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, CAN bus (CANH, CANL) to GND21 Human Body Model (HBM), per ANSI/	±8000	IN
	ESDA/JEDEC JS-001, all other pins Charged Device Model (CDM), per JEDEC JESD22-C101, all pins2 [1]	±4000	
		±1500	

Note:

1. JEDEC document JEP155 states that 500V HBM allows safe production in accordance with standard ESD control processes.
2. JEDEC document JEP157 states: 250V CDM allows safe production in accordance with standard ESD control processes.

7.3 Recommended working conditions

parameter			Min Typ Max Unit			
VCC1	Logic side power supply		2.5	3.3	5.5	IN
VCC2	voltage Bus side power		4.5	5	5.5	IN
VI or VIC	supply voltage Bus pin voltage (single-ended		–30		30	IN
HIV	or common mode) High	Driver (TXD) Driver	0.7*VCC1			IN
WILL	level input voltage Low level	(TXD)			0.3*VCC1	IN
AT	input voltage Differential input voltage		–12		12	IN
John	Output current @ high level	Driver Receiver Driver	–70			mA
		Receiver	–4			
IOL	Output current @ low level				70	mA
					4	
FACING	Ambient temperature		–40		125	°C
TJ	Junction		–40		150	°C
PD	temperature	VCC1 = 5.5VÿVCC2 = 5.25VÿTA = 125°Cÿ			200	mW
PD1	Total power consumption	RL = 60ÿ, TXD input signal is 500 kHz			25	mW
	Logic side power	Square wave (50% duty cycle)			175	mW
consumption Bus side power consumption PD2 TJ (shutdown) Thermal				190		°C

shutdown temperature 1 Note:

1. Operating temperatures above the thermal shutdown temperature may affect device reliability.

7.4 Isolation Characteristics

parameter	Test Conditions	Numeric		unit
		W/G	IN	
CLR External air gap (clearance) 1	Measure the shortest distance between input and output through air	8	6.1	mm
CPG External creepage distance 1	Measure the shortest distance between input and output along the shell	8	6.8	mm
DTI Isolation Distance	Minimum internal clearance (internal distance)	28	28	ÿm
CTI Comparative Tracking Index Material	DIN EN 60112 (VDE 0303-11); IEC 60112 According to IEC	>600	>600	IN
Group	60664-1 Rated mains			
IEC 60664-1 Overvoltage Category	voltage ÿ 150 VRMS Rated mains voltage	I-IV	I-IV	
	ÿ 300 VRMS Rated mains voltage ÿ 600	I-IV	I-III	
	VRMS Rated mains voltage ÿ 1000 VRMS	I-IV	N/A	
		I-III	N/A	
DIN V VDE V 0884-17:2021-102				
VIORM Maximum Repetitive Peak Isolation Voltage	AC Voltage (Bipolar) AC	1414	566	VPK
VIOWM maximum operating isolation voltage	Voltage; Time Dependent Dielectric Breakdown (TDDB) Test DC Voltage	1000	400	VRMS
		1414	566	VDC
VIOTM Maximum transient isolation voltage	VTEST = VIOTM, t = 60 s (certification); VTEST = 1.2 × VIOTM, t = 1 s (100% production test)	7070	5300	VPK
VIOSM Maximum Surge Isolation Voltage 3	Test method according to IEC 60065, 1.2/50 ÿs waveform, VTEST = 1.6 × VIOSM (certification, CA-IS3052) VTEST = 1.3 × VIOSM (certification, CA-IS3050)	8000 (CA-IS3052) 6250(CA-IS3050)	4070 (CA-IS3050)	VPK
QPD characterization of charge 4	Method a, after input/output safety test subclass 2/3, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIORM, tm = 10 s	ÿ5	ÿ5	pC
	Method a, environmental test subclass 1, after Vini = VIOTM, tini = 60 s; Vpd(m) = 1.6 × VIORM, tm = 10 s	ÿ5	ÿ5	
	Method b1, conventional testing (100% production testing) and pre-Preprocessing Vini = 1.2 × VIOTM, tini = 1 s; Vpd(m) = 1.875 × VIORM, tm = 1 s (certification, CA-IS3052) Vpd(m) = 1.5 × VIORM, tm = 1 s (certification, CA-IS3050)	ÿ5	ÿ5	
CIO Gate capacitance, input to output5	VIO = 0.4× sin (2ÿft), f = 1 MHz	~0.5	~0.5	pF
RIO Insulation Resistance 5	VIO = 500 V, TA = 25°C	>1012	>1012	Oh
	VIO = 500 V, 100°C ÿ TA ÿ 125°C	11 >10	>1011	
	VIO = 500 V at TS = 150°C	>109	>109	
Pollution		2	2	
UL 1577				
VISO maximum isolation voltage	VTEST = VIS . t = 60 s (certification), VTEST = 1.2 × VIS . t = 1 s (100% production tested)	5000	3750	VRMS

Note:

1. Creepage and clearance requirements should be based on the isolation standards of specific devices in specific applications. Circuit board design should pay attention to maintaining creepage and clearance distances to ensure that the isolator is placed on the printed circuit board.
   The pads on the board do not shorten this distance. Creepage distances and clearances on a printed circuit board are in some cases the same. These distances can be increased by inserting grooves in the board.
   index.
2. This standard applies only to the maximum operating rating range. Compliance with safety-related specifications should be ensured through appropriate protection circuits.
3. Tests are conducted in air or oil to determine the inherent surge suppression of the isolation barrier.
4. Characteristic charge is the discharge charge caused by partial discharge (pd).
5. All pins on either side of the insulated gate are connected together to form a two-terminal device.

Related safety certification

VDE	UL	CQC	TUV
DIN V VDE V 0884-17:2021-10 Certification	UL1577 Device Program Certification	GB4943.1-2011 and GB 8898-2011 certified	EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017 Certification
CA-IS3052 (W/G, reinforced isolation) Maximum transient isolation voltage: 7070Vpk Maximum repetitive peak isolation voltage: 1414Vpk Maximum surge isolation voltage: 8000Vpk CA-IS3050 (W/G, basic isolation) (enhanced isolation pending) Maximum transient isolation voltage: 7070Vpk Maximum repetitive peak isolation voltage: 1414Vpk Maximum surge isolation voltage: 6250Vpk CA-IS3050 (U, basic isolation) Maximum transient isolation voltage: 5300Vpk Maximum repetitive peak isolation voltage: 566Vpk Maximum surge isolation	SOIC8-WB: 5000 VRMSÿ SOIC16-WB: 5000 VRMS DUB8ÿ3750VRMS	reinforced isolation, maximum working voltage 600 VRMS; (only applicable at altitudes of 5000 meters and below)	EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017 certified, maximum working voltage 600 VRMS; 5000 VRMS Enhanced Isolation
voltage: 4070Vpk Reinforced insulation: 40057278 Basic insulation: 40052786	Certificate No.: E511334	Certificate No SOIC8-WB: CQC20001257122 SOIC16-WB: CQC20001257121	CB Certificate No.: JPTUV-112092ÿDE 2-028117 AK Certificate Number: AK 50476720 0001ÿ AND 50476727 0001

Thermal Parameters

Thermal parameters		SOIC8-WB	SOIC16-WB	DUB8 Unit	
RÿJA	Thermal resistance from chip junction to ambient	110.1	86.5	73.3	°C/W
RÿJC(top)	Thermal resistance from chip junction to case (top) Thermal	51.7	49.6	63.2	°C/W
RÿJB	resistance from chip junction to board Thermal	66.4	49.7	43.0	°C/W
ÿJT	resistance from chip junction to top Characteristic parameters	16.0	32.3	27.4	°C/W
ÿJB	from chip junction to board Characteristic parameters from	64.5	49.2	42.7	°C/W
RÿJC(bottom)	chip junction to case (bottom) Thermal resistance from chip junction to	n/a	n/a	n/a	°C/W

7.7 Electrical Characteristics

Unless otherwise noted, all voltages are referenced to their respective grounds, 3 V ÿ VCC1 ÿ 5.5 V, 4.5 V ÿ VCC2 ÿ 5.5 V. All min/max specifications apply over the entire recommended operating range.

Where otherwise noted, all typical specifications are at TA = 25°C, VCC1 = VCC2 = 5 V.

parameter		Test Conditions	Min	Typ	Max	Unit
Supply voltage						
VCC1_UVLO+ UVLO chip power-on start voltage		VCC1	1.95	2.24	2.375	IN
VCC1_UVLO- UVLO chip power-off reset voltage		VCC1	1.88	2.10	2.325	IN
VCC2_UVLO+ UVLO chip power-on start voltage		VCC2	3.9	4.2	4.4	IN
VCC2_UVLO- UVLO chip power-off reset voltage		VCC2	3.8	4.0	4.25	IN
current						
ICC1 logic side supply current		VI = 0 V or VCC1, VCC1 = 3.3 V VI = 0 V or		1.8	2.8	mA
		VCC1, VCC1 = 5 V		2.3	3.6	mA
ICC2 bus side supply current	Dominant	VI = 0 VÿRL = 60 ÿ		44	73	mA
	and Implicit	VI = VCC1		3	12	mA
driver						
VO(D) bus output voltage (dominant)	SOUP	VI = 0 V, RL = 60 ÿ; see Figure 8-1	2.75	3.4	4.5	IN
	LIVE		0.5		2.25	IN
VO(R) bus output voltage (recessive)		VI = 2 V, RL = 60 ÿ; see Figure 8-1	2	2.5	3	IN
VOD(D) differential output voltage (dominant)		VI = 0 V, RL = 60 ÿ; see Figure 8-1 Figure 8-2	1.5		3	IN
		VI = 0 V, RL = 45 ÿ; see Figure 8-1 Figure 8-2	1.4		3	IN
VOD(R) differential output voltage (recessive)		VI = 3 V, RL = 60 ÿ; see Figure 8-1	–12		12	mV
		VI = 3 V, no load	–0.5		0.05	IN
VOC(D) common mode output voltage (dominant)		See Figure 8-6	2	2.5	3	IN
VOC(pp) common mode output voltage peak to peak				0.3		IN
IIH High level input current, TXD input		VI = 2V			20	µA
IIL low level input current, TXD input		VI = 0.8 V	–20			µA
IOS(SS) short circuit output current		TXD = low, VCANH = –30 V, CANL open; see Figure	–105	-72		mA
		8-9 TXD = High, VCANH = 30V, CANL open; see Figure 8-9		3	5	mA
		TXD = High, VCANL = –30 V, CANH open; see Figure	-5	-1.5		mA
		8-9 TXD = low, VCANL = 30V, CANH open; see Figure 8-9		90	105	mA
CMTI Common Mode Transient		VI = 0 V or VCC1; see Figure 8-10	100	150		kV/µs
Immunity Receiver						
VIT+ High level input threshold voltage		-20V ÿ VCMÿ20V			0.9	IN
VIT - Low level input threshold voltage			0.5			IN
VIT+ High level input threshold voltage		-30V ÿ VCMÿ -20V			1.0	

VIT - Low level input threshold voltage	20V ÿ VCMÿ 30V	0.4			
VHYS Input Voltage Hysteresis Window			120		mV
VOH logic high output voltage, VCC1 = 5 V	IOH = –4 mA; see Notes 1, 2; Figure 8-5 IOH = –	VCC1 – 0.8	4.6		IN
	20 µA; see Notes 1, 2; Figure 8-5 IOH = –4 mA;	VCC1 – 0.1	5		
VOH logic high output voltage, VCC1 = 3.3 V	see Notes 1, 2; Figure 8-5 IOH = –20 µA; see	VCC1 – 0.8	3.1		IN
	Notes 1, 2; Figure 8-5 IOL = 4 mA; see Notes 1,	VCC1 – 0.1	3.3		
VOL logic low level output voltage	2; Figure 8-5 IOL = 20 µA; see Notes 1, 2;		0.2	0.4	IN
	Figure 8-5 TXD is 3 V, VI = 0.4xsin(2ÿft) + 2.5		0	0.1	
THERE CANH, CANL input capacitance to ground	V, f = 1MHz		20		pF
CID Differential input capacitance	TXD ÿ 3VÿVI = 0.4xsin(2ÿft) ÿ f = 1MHz		10		pF
RIN CANH, CANL input resistance	TXD is 3V	15		40	kÿ
RID Differential input resistance	TXD is 3V	30		80	kÿ
RI(m) input resistance matching (1 – [RIN(CANH) / RIN(CANL)])	VCANH = VCANL	–5%	0%	5%	
CMTI Common Mode Transient Immunity	VI = 0 V or VCC1; see Figure 8-10	100	150		kV/µs

7.8 Timing Characteristics

Unless otherwise noted, all voltages are referenced to their respective grounds, 3 V ÿ VCC1 ÿ 5.5 V, 4.5 V ÿ VCC2 ÿ 5.5 V. All min/max specifications apply over the recommended operating range.

Note: All typical specifications are at TA = 25°C, VCC1 = VCC2 = 5 V.

parameter	Test Conditions	Min Typ Max Unit			
transceiver					
tloop1 Total loop delay, driver input to receiver Output, implicit to explicit	See Figure 8-7	110		210	ns
tloop2 Total loop delay, driver input to receiver Output, explicit to implicit		110		210	ns
driver					
tPLH propagation delay, output changes from recessive to dominant	See Notes 1, 2; Figure 8-2		50		ns
tPHL Propagation delay, output changes from dominant to recessive			65		
tr Differential output signal rise time tf Differential			55		
output signal fall time tTXD_DTO1 Dominant timeout			60		
time	CL = 100 pF; see Notes 1, 2; Figure 8-8	2	5	8	ms
tPLH propagation delay, output changes from low level to high level Level	See Notes 1, 2; Figure 8-5		105		ns
tPHL propagation delay, output changes from high level to low level Level			75		
tr Output signal rise time tf Output signal fall			5		
time Note:			5		

1. Once the driver enters the dominant state for more than tTXD_DTO, the dominant timeout function will shut down the driver to release the bus into the recessive state to prevent the bus from being locked by the local node. The driver can only resume the transmission function of dominant level after entering recessive state.

Co., Ltd. **8** parameter test circuit

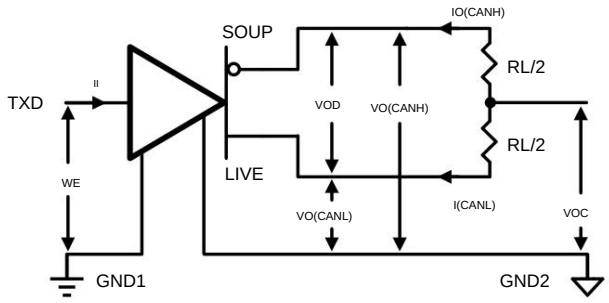


Figure **8-1** Definition of driver voltage and current indicators

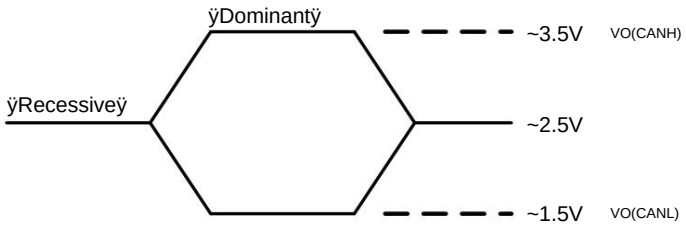


Figure **8-2** Voltage definition of bus logic state

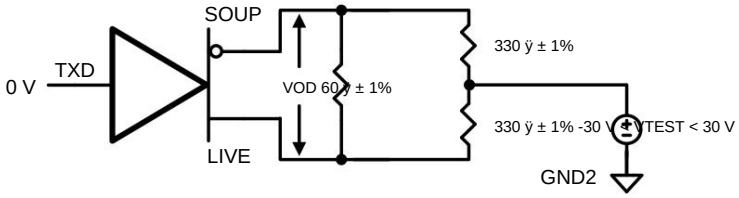
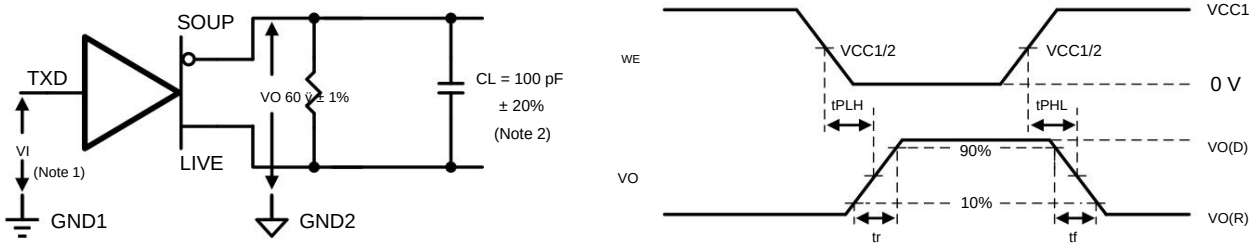


Figure **8-2** Driver **VOD voltage test circuit (with common mode load)**



Note: 1. The input pulse generated by the signal source has the following requirements: pulse repetition rate PRR ÿ 125 kHz, 50% duty cycle, rise time tr ÿ 6 ns, fall time tf ÿ 6 ns, output impedance ZO = 50 ÿ; 2. The load capacitance CL includes the parasitic capacitance of the instrument and fixture.

Figure **8-3** Driver measurement circuit and voltage waveform

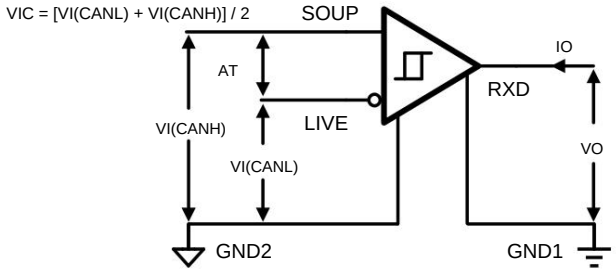
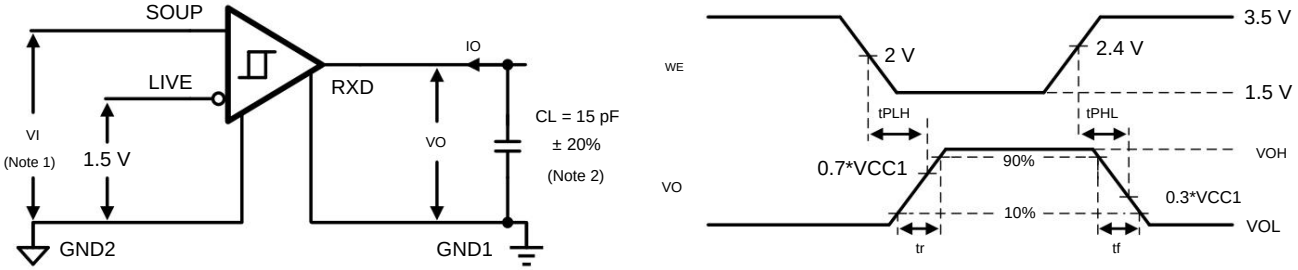


Figure **8-4** Receiver output voltage and current test conditions



Note: **1.** The input pulse generated by the signal source has the following requirements: pulse repetition rate PRR ÿ 125 kHz, 50% duty cycle, rise time tr ÿ 6 ns, fall time tf ÿ 6 ns, output impedance ZO = 50 ÿ; **2.** The load capacitance CL includes the parasitic capacitance of the instrument and fixture.

Figure **8-5** Receiver measurement circuit and voltage waveform

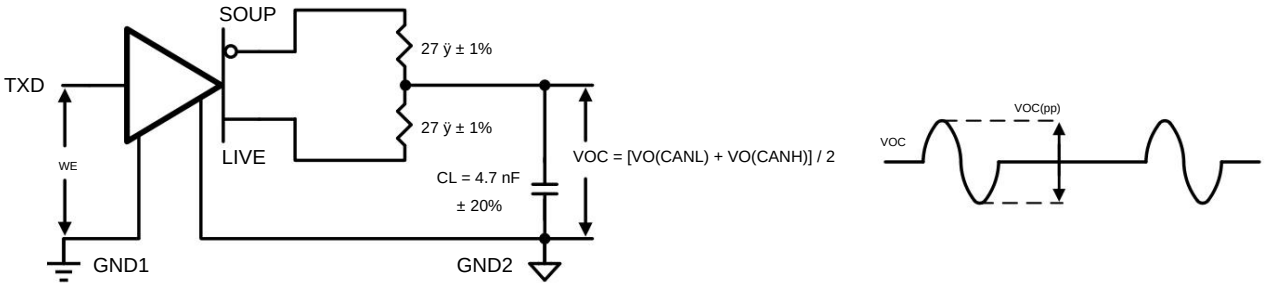


Figure **8-6** Driver output voltage peak measurement circuit and waveform

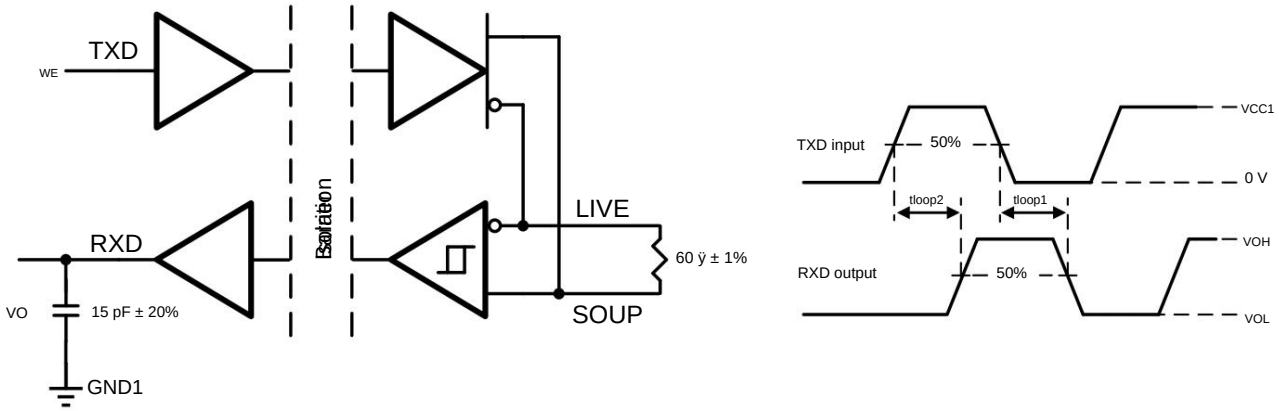
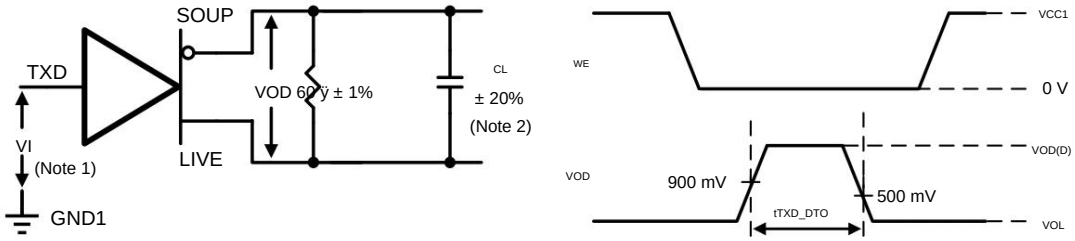


Figure **8-7 TXD --- RXD** loop delay



Note: **1.** The input pulse generated by the signal source has the following requirements: pulse repetition rate PRR ÿ 125 kHz, 50% duty cycle, rise time tr ÿ 6 ns, fall time tf ÿ 6 ns, output impedance ZO = 50 ÿ; **2.** The load capacitance CL includes the parasitic capacitance of the instrument and fixture.

Figure **8-8** Dominant timeout function measurement circuit and voltage waveform

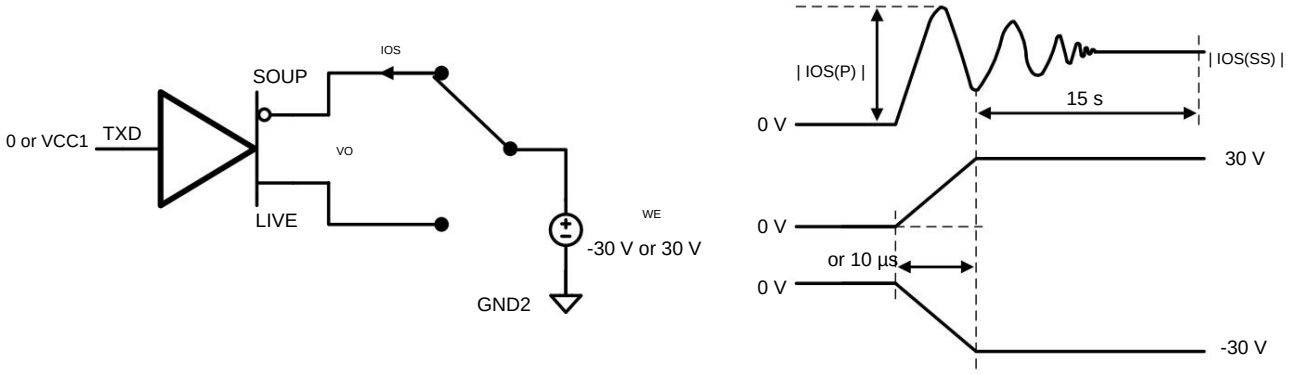


Figure **8-9** Output short-circuit current measurement circuit and waveform

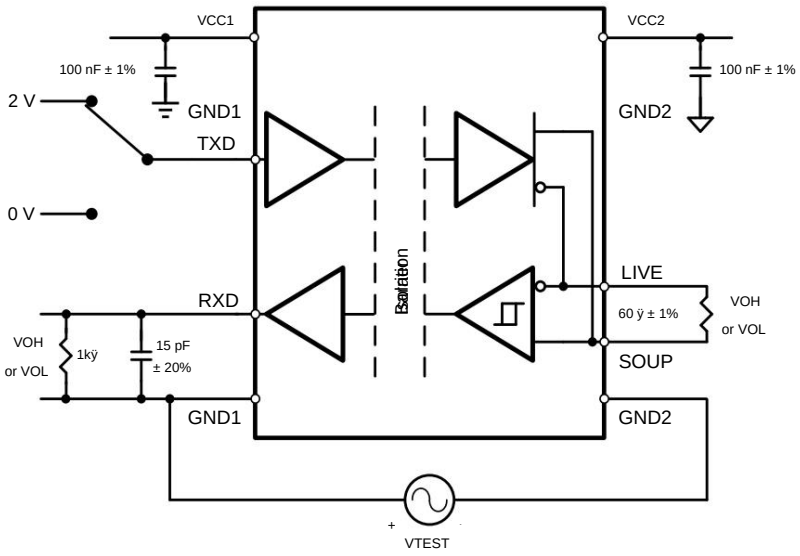


Figure **8-10 Common-mode transient immunity (CMTI) measurement circuit**

9 Detailed description

The CA-IS305x isolated CAN transceivers provide up to 3.75kVRMS (SOP8 package) or 5kVRMS (wide

The device features 150kV/ÿs common-mode transient immunity, allowing data rates up to 1Mbps to be transmitted across the insulation barrier.

The reliable isolation characteristics and high-speed communication capabilities enable the CA-IS305x to ensure reliable data transmission in noisy environments and is suitable for inverters, HVAC, motor drives,

CA-IS305x can accept a supply voltage range of 2.5V to 5.5V (VCC1) on the logic side.

The bus side is powered by an independent 4.5V to 5.5V isolated power supply (VCC2).

The receiver input of CA-IS305x allows ±30V common-mode input, far exceeding the -2V to +7V range defined by ISO 11898 specification; bus pins CANH, CANL

It can withstand fault voltages up to ±58V, providing effective overvoltage protection for the system. In addition, when a short circuit fault occurs in the output stage, the transmitter's current limiting protection circuit

The thermal shutdown protection immediately puts the device into a protection state, while the thermal shutdown protection forces the transmitter output into a high impedance state when the device is detected to be overheated, preventing the device from generating excessive power.

The transmitter time-out detection circuit is used to prevent bus lockup.

9.1 CAN bus status

The CAN bus has two logical states: dominant state and recessive state. In the dominant state (representing the "0" data bit, used to determine the priority of information transmission),

The differential voltage between CANH and CANL is between 1.5V and 3V (higher than 0.9V), which corresponds to the logic "0" of TXD/RXD; in the recessive state (representing the "1" digital

The bus is pulled to the bus side power supply VCC2/2 through internal resistors, and the differential voltage between CANH-CANL is between -120mV and +12mV.

or close to 0V (less than 0.5V, depending on bus load), corresponding to logic "1" on TXD/RXD, see picture *8-2ÿ*

9.2 Receiver

The receiver converts the differential input (CANH and CANL) of the bus into the single-ended output signal RXD required by the CAN controller. The internal comparator detects the differential voltage.

VDIFF = (VCANH-VCANL), the threshold voltage is about 0.7V. If VDIFF > 0.9V, the RXD pin outputs a logic low level; if VDIFF < 0.5V, the RXD pin outputs a logic low level.

The common-mode input voltage range of CANH and CANL is ±30V. When CANH and CANL are short-circuited or in idle state, RXD outputs high voltage.

Flat, see surface *9-1ÿ*

Table **9-1** Receiver truth table

WID=VCANH-VCANL	Bus Status	RXD
VID ÿ 0.9V	Dominant	Low level
0.5V < VID <0.9V	uncertain	uncertain
WID ÿ 0.5V	Hidden	High level
Open circuit (VID ÿ 0V)	open circuit	High level

9.3 Transmitter

The transmitter converts the single-ended input signal (TXD) from the CAN controller into differential outputs CANH and CANL. The truth table is shown in Table 9-2. Internal Transmitter

The timeout detection ensures that the transceiver is in normal working state under the premise that the dominant level does not exceed tTXD_DTO . CANH and CANL outputs have short-circuit current limiting protection and thermal

Shutdown further limits the maximum power dissipation of the device.

Table **9-2** Transmitter truth table

VCC1	VCC2	enter	TXD low level time	Output		Bus Status
		TXD		SOUP	LIVE	
Power-on	Power-on	L	< tTXD_DTO	H	L	Dominant
		L	> tTXD_DTO	VCC2/2	VCC2/2	Hidden
		H or open circuit	X	VCC2/2	VCC2/2	Hidden
Power-on	Power outage	X	X	Hi-Z	Hi-Z	Hi-Z
Power outage	Power-on	X	X	VCC2/2	VCC2/2	Hidden

Note:

1. X = Don't care; H = High level; L = Low level; Hi-Z = High impedance.

2. The TXD input has an internal weak pull-up.

9.4 Protection Function

9.4.1 Signal Isolation and Protection The

CA-IS305x device integrates a digital isolator, using the capacitive isolation technology of Chuantu Microelectronics. The internal on/off keying (OOK) modulator transmits digital signals in two different power domains, which are isolated by a silicon dioxide (SiO2) insulation layer. Among them, the digital isolation transmitter sends a high-frequency carrier to the isolation side for one logic input state (for example, logic "1"), and does not transmit any signal to the isolation side for another logic state (logic "0"); at the receiving end of the isolator, the high-frequency carrier signal across the insulation layer is converted to logic "1", and when there is no high-frequency signal, a logic "0" is generated. As a result, the received signal from the controller or bus is demodulated and restored on the isolation side, achieving electrical isolation of up to 5kVRMS between the logic side and the bus side (wide-body SO package device). The CAN transceiver on the bus side realizes the conversion between the CAN bus differential signal and the single-ended logic signal. In addition, the transmitter output/receiver input on the bus side can withstand ±8kV ESD protection (human body model).

9.4.2 Thermal Shutdown

The CA-IS305x has internal integrated thermal shutdown protection. When the junction temperature of the device exceeds the thermal shutdown threshold TJ(shutdown) (190°C, typical value), the driver will be turned off, blocking the connection between the driver output TXD and the bus. During thermal shutdown, the CAN bus is biased at a recessive level, and the receiver remains in an effective working state. Once the junction temperature drops to the normal operating range, the device automatically exits thermal shutdown and resumes normal operation.

9.4.3 Current Limiting

Protection The transmitter of the CA-IS305x device also provides output short-circuit protection. Once the output is short-circuited to the power supply or short-circuited to the ground, the driver will limit the output current. Of course, since it is in the maximum current limiting state at this time, it may consume a large power supply current, and the thermal shutdown function provides secondary protection for output short circuits. Once the short-circuit fault is removed, the transmitter will exit the current limiting protection and enter the effective working state.

9.4.4 Transmitter Timeout Detection The

CA-IS305x CAN transceiver has a dominant timeout detection function with a timeout period of tTXD_DTO, which prevents the bus from being clamped at a low level (the bus is in a dominant state) due to a CAN controller fault. When TXD remains at the dominant state corresponding level (low level) for more than tTXD_DTO , the device will turn off the transmitter and release the bus to a recessive state. After the timeout fault is removed, the transmitter is re-enabled at the rising edge of the signal received by TXD, and the transceiver resumes normal operation. The transmitter timeout period limits the minimum data transmission rate of the CA-IS305x. According to the CAN bus communication protocol, 11 dominant bits are allowed to be sent continuously under the worst working environment. Based on this, it can be estimated that the minimum rate allowed by the CA-IS305x is: 11bits /tTXD_DTO = 11/ 2ms = 5.5kbps, that is, the minimum rate of the CA-IS305x is limited to 5.5kbps.

Application Information

The CAN interface is widely used in the industrial field due to its flexible priority management and excellent arbitration capabilities, and most factory automation systems work in different Isolation becomes a necessary option to provide necessary protection for devices working on the low-voltage side. CA-IS305x is an ideal choice for such applications, not only providing signal The signal is isolated and the isolated power supply is integrated . Only a few external power bypass capacitors are needed to form *a* complete isolation interface. picture Road shown.

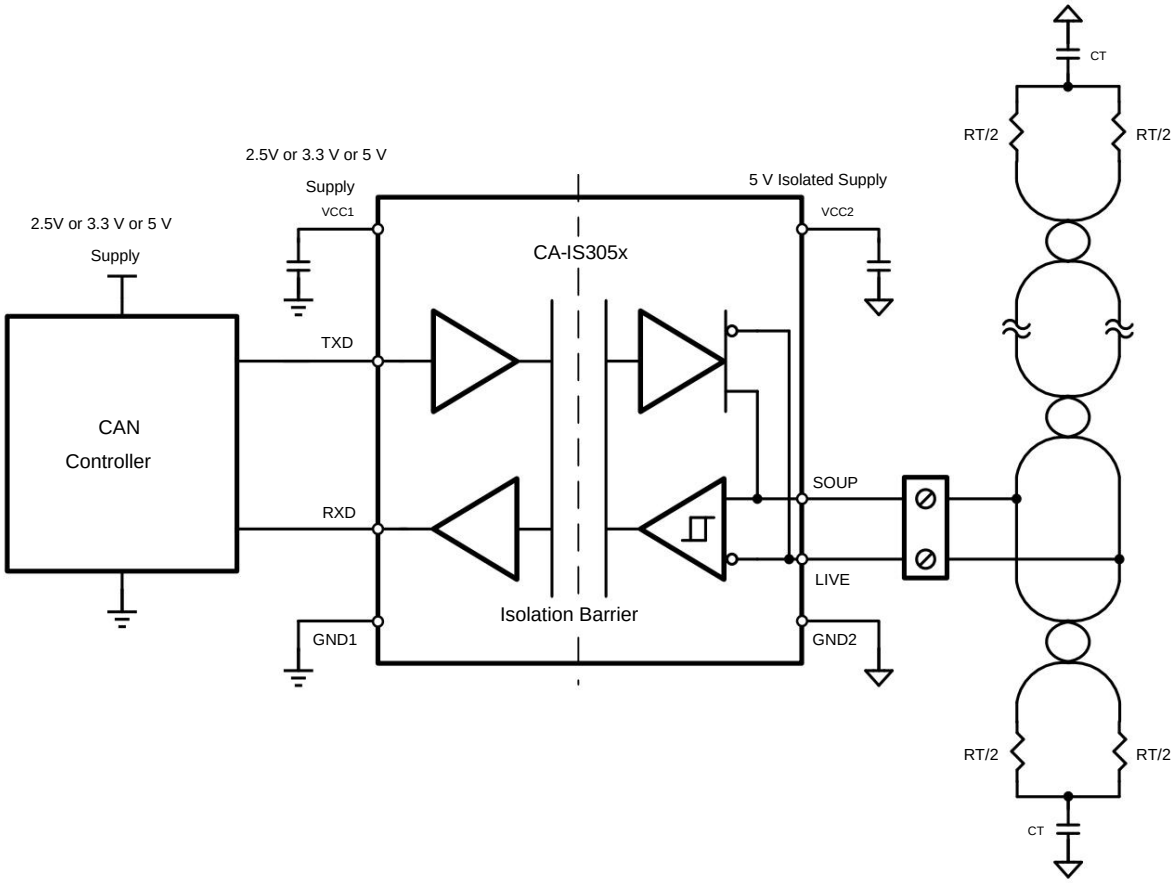


Figure **10-1** Typical isolated **CAN** node based on **CA-IS305x**

CA-IS305x can support data transmission rates up to 1Mbps. Of course, the maximum rate of the bus network is also limited by the bus load, number of nodes, and cable length. When designing a CAN bus network, you must consider the signal transmission loss on the cable, parasitic load, delay, network imbalance, Ground potential deviation and signal integrity, therefore, the highest rate and the longest transmission distance in the actual system are often lower than the theoretical value. According to the ISO11898 standard, The maximum number of nodes on the CAN bus is 30, taking into account the high input impedance of the CA-IS305x (minimum 30kÿ) and the fact that the driver is capable of operating at 60ÿ bus load. Provides a minimum 1.5V differential drive voltage (at least 1.4V differential output with a 45ÿ bus load), allowing up to 110 The nodes are connected to the same CAN bus.

In a multi-node CAN bus network, it is very important to keep the line impedance uniform, so proper terminal matching is required. The network topology cannot use star, Tree or ring topology, any node connected between the two farthest ends of the network will create a "joint", and high-speed signals are connected to these cables. Signal reflection will occur on the "connector", which will introduce interference on the bus. In the design, it is necessary to use the shortest possible cable to connect each node, especially for high-speed *10-2* shows the typical topology of the CAN bus. A single 120ÿ resistor (RT) can be used to match the bus at both ends of the bus . Add common mode filtering, or split it into two 60ÿ resistors for terminal matching, such as picture As shown in *10-2* .

to keep an isolation channel away from the ground line and signal line under the isolator. Any electrical connection or metal connection between the cable side and the logic side is

To ensure reliable operation of the device at any data rate, it is recommended to connect at least one external resistor between VCC1 and GND1, and between VCC2 and GND2 .

0.1ÿF low ESR decoupling capacitors should be placed close to the corresponding power pins of the device.

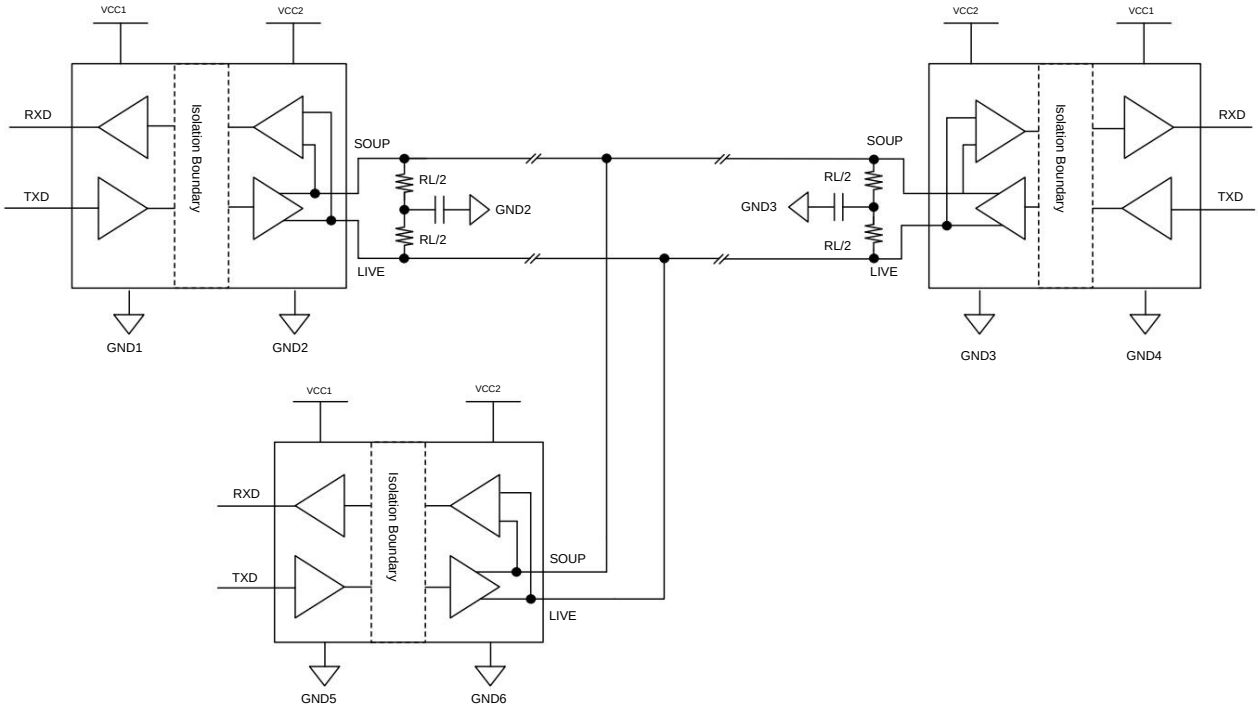


Figure **10-2** Typical **CAN** bus topology based on **CA-IS305x**

11Packaging Information

SOIC8-WB Dimensions

The following figure shows the dimensions of the CA-IS305x series isolated CAN transceiver in SOIC8-WB package and the recommended pad dimensions. Dimensions are in millimeters.

unit.

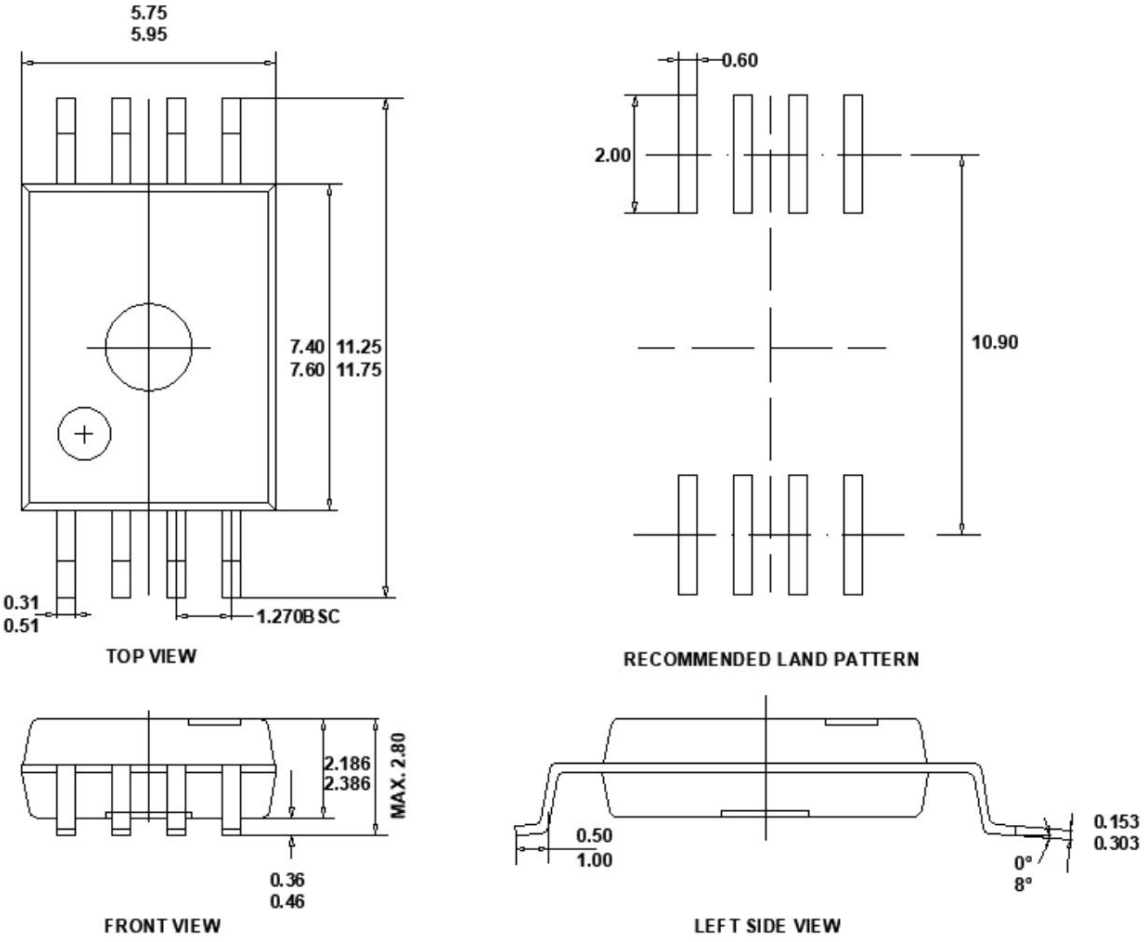


Figure **11-1 SOIC8-WB** dimensions

Ltd. **DUB8** dimensions

The following figure shows the dimensions of the CA-IS3050 isolated CAN transceiver in DUB8 package and the recommended pad dimensions. Dimensions are in millimeters.

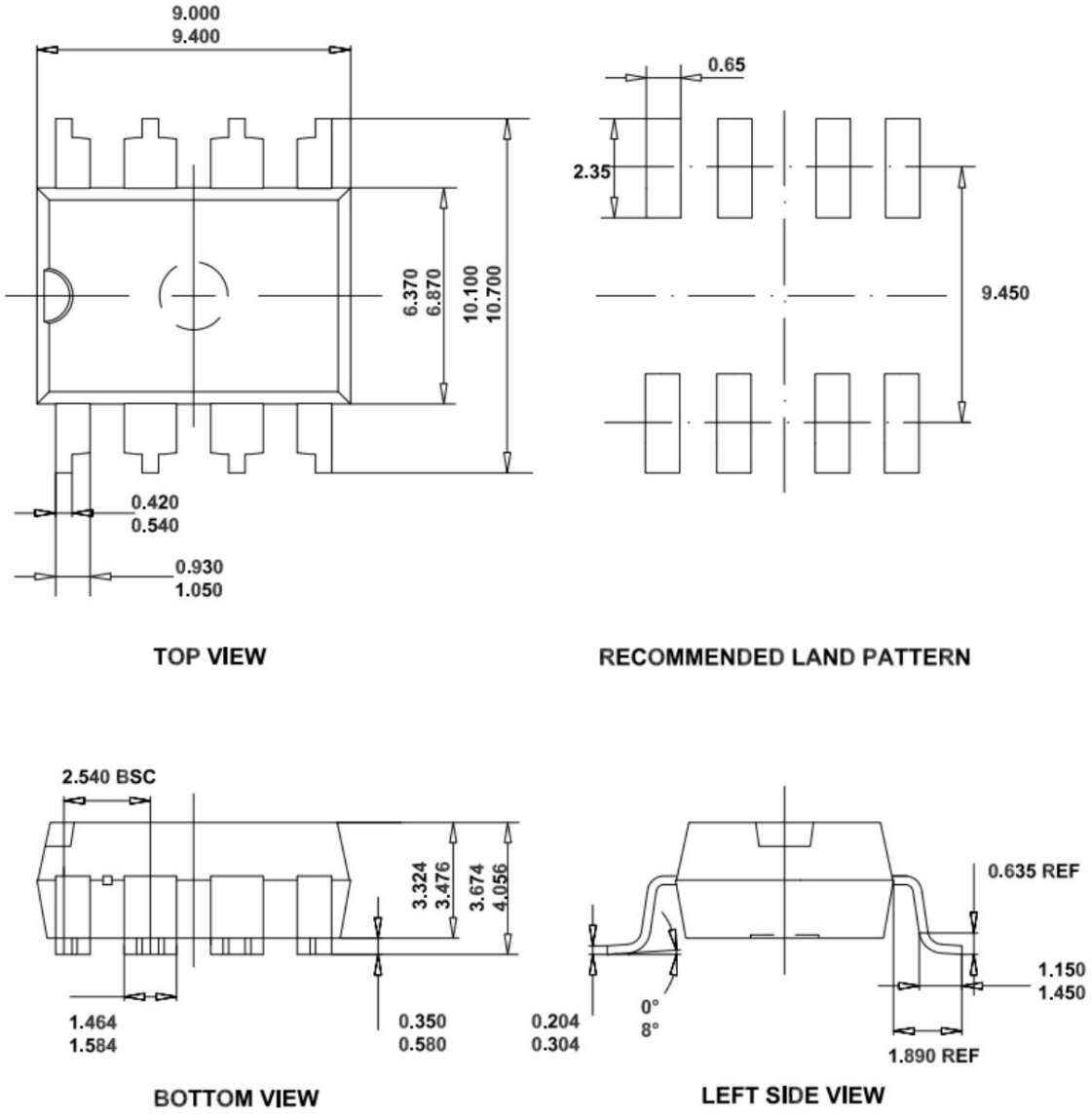


Figure **11-2 DUB8** dimensions

dimensions

The following figure shows the dimensions of the CA-IS305x series isolated CAN transceiver in SOIC16-WB package and the recommended pad dimensions. Dimensions are in millimeters.

unit.

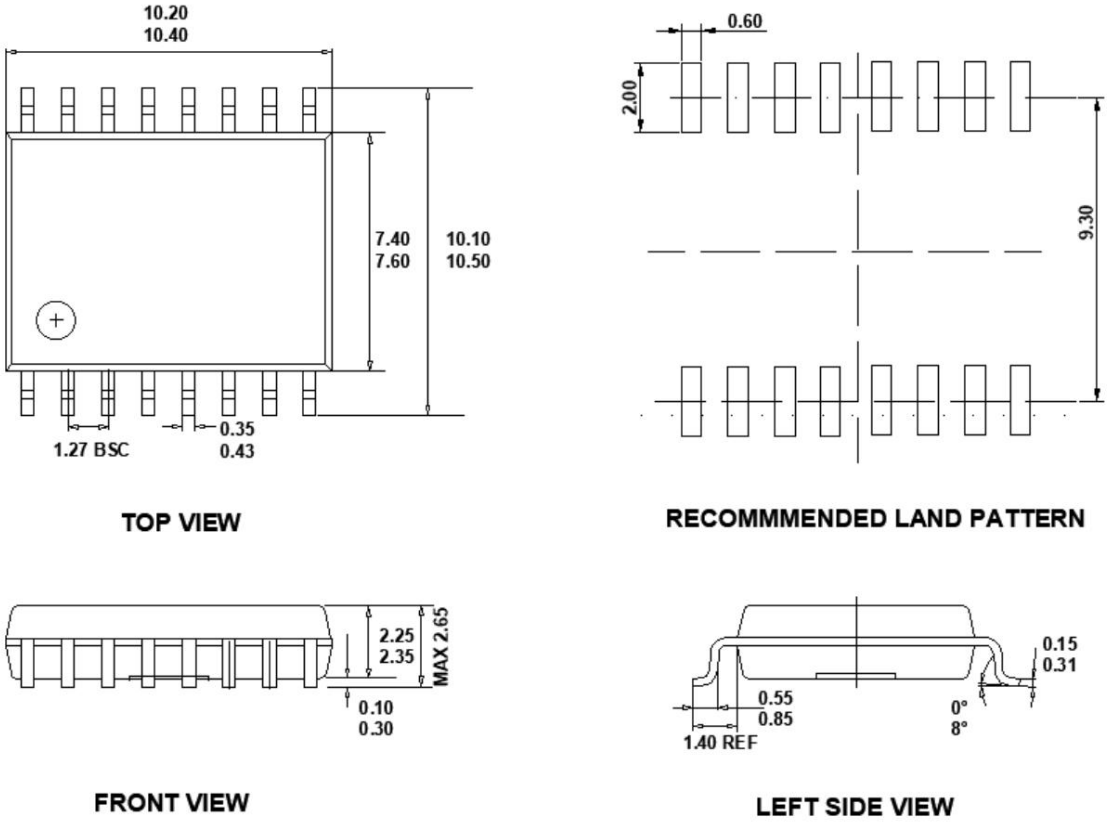


Figure **11-3 SOIC16-WB** dimensions

Ltd. **12** welding information

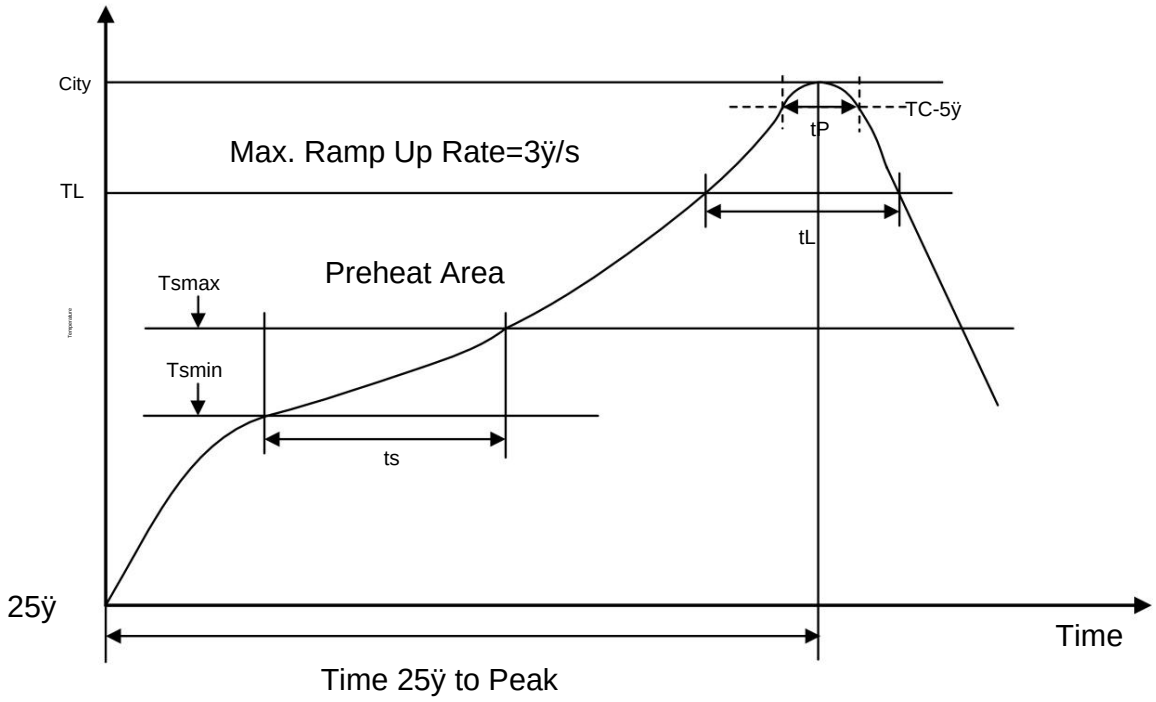


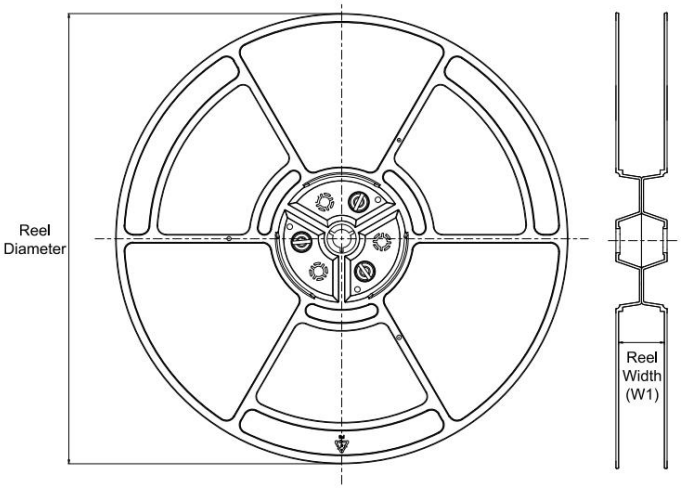
Figure **12-1** Welding temperature curve

Table **12-1** Welding temperature parameters

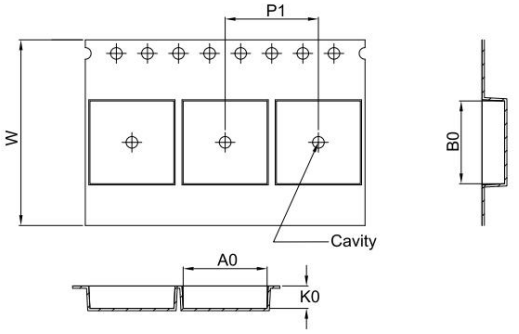
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ÿ to Peak)	3ÿ/second max
Time of Preheat temp(from 150 ÿ to 200 ÿ)	60-120 second
Time to be maintained above 217 ÿ	60-150 second
Peak temperature	260 +5/-0 ÿ
Time within 5 ÿof actual peak temp	30 second
Ramp-down rate	6 ÿ/second max.
Time from 25ÿ to peak temp	8 minutes max

13 Tape Information

REEL DIMENSIONS

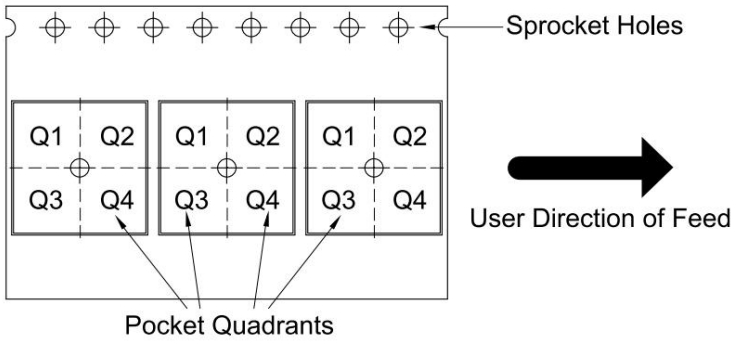


TAPE DIMENSIONS



A0 Dimension designed to accommodate the component width
B0 Dimension designed to accommodate the component length
K0 Dimension designed to accommodate the component thickness
W Overall width of the carrier tape
P1 Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	IN (mm)	Pin1 Quadrant
CA-IS3050W	SOC W 16	1000			330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3050G	SEC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3052W	SOC W 16	1000			330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3052G	SEC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3050U	DUB	IN	8	800	330	24.4	10.90	9.60	4.30	16.00	24.00	Q1

The above information is for reference only and is used to assist Chipanalog customers in design and development. Chipanalog reserves the right to

The company reserves the right to change the above information due to technological innovation.

All Chipanalog products are factory tested. Customers are responsible for self-evaluation and determination of suitability for specific applications.

The authorization for customers to use the resources is limited to developing applications related to the Chipanalog products involved. Otherwise, the resources may not be copied or displayed.

Chipanalog shall not be liable for any claims, damages, costs, losses, liabilities, etc. arising out of the use of the resources described.

Trademark Information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

http://www.chipanalog.com