Andy, Yu-Guang Chen

EE6094 CAD for VLSI Design
Workstation Information

Document Credit: Wei Chang、Li-Cheng Zheng

Basic Information:

System: CentOS 6.10

Host: 140.115.71.233

Port: 22 (Please use SSH to connect to the machine)

Default account/password: Your Student_ID

Software:

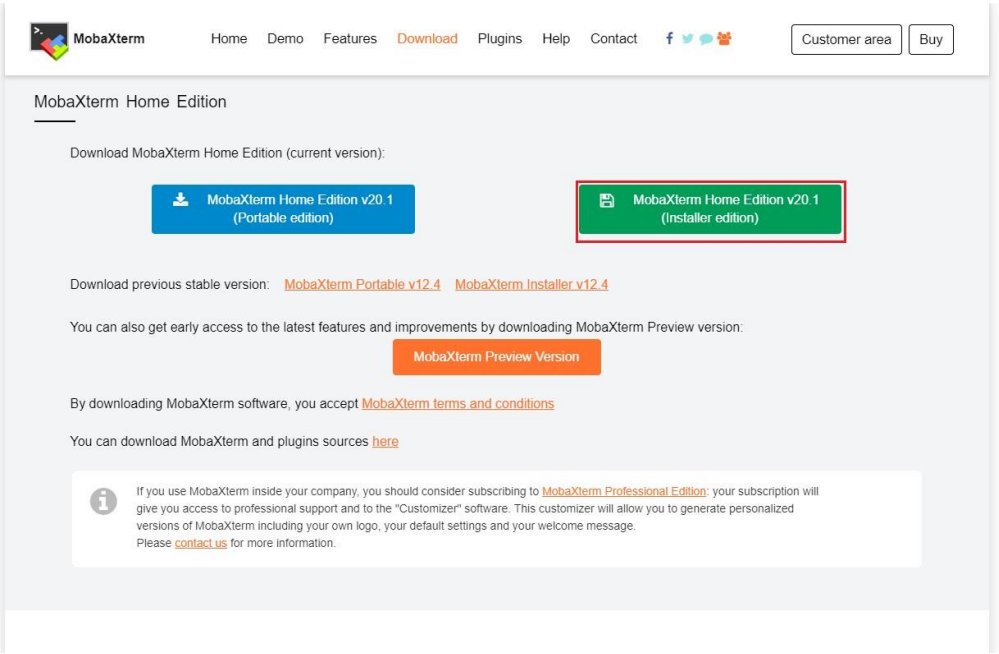
Software	Version
gcc/g++	4.8.2 (C++ 11 supported)
GNU Make	3.81
tmux	1.6

IP Restriction:

To easily manage the server for this course, you're only allowed to connect our server through IPs of NCU domain (under 140.115.xxx.xxx). If you need to connect the server through any IP other than NCU domain, please email to TA and let him know the IP you usually use. He can manually add the IP to our server.

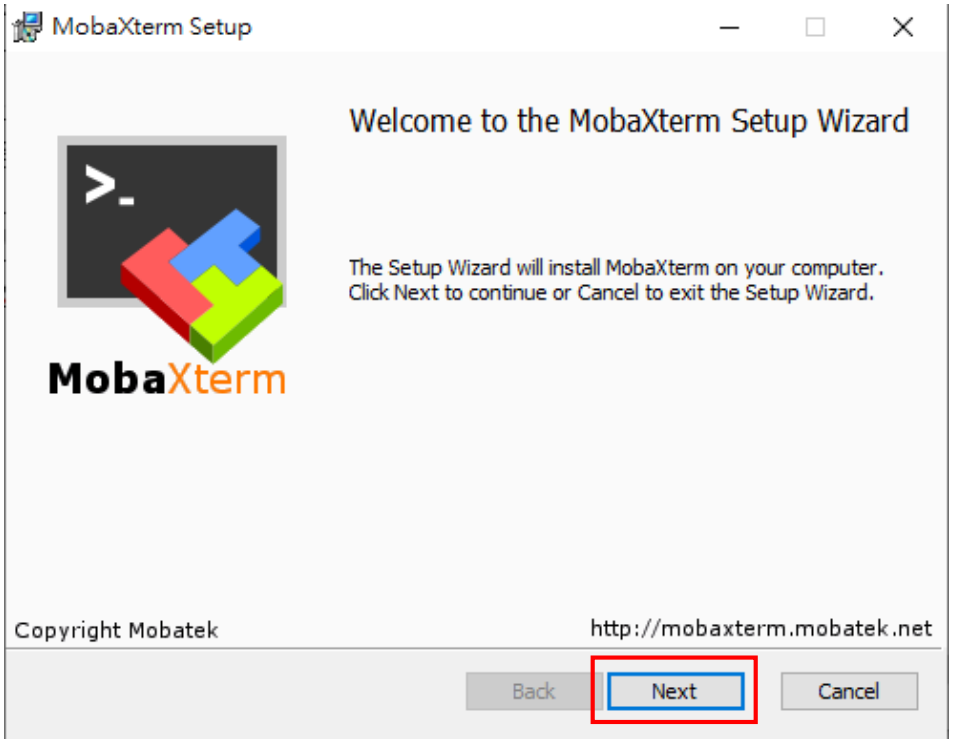
How to connect to the server:

Step1. Download MobaXterm via https://mobaxterm.mobatek.net/download-home-edition.html



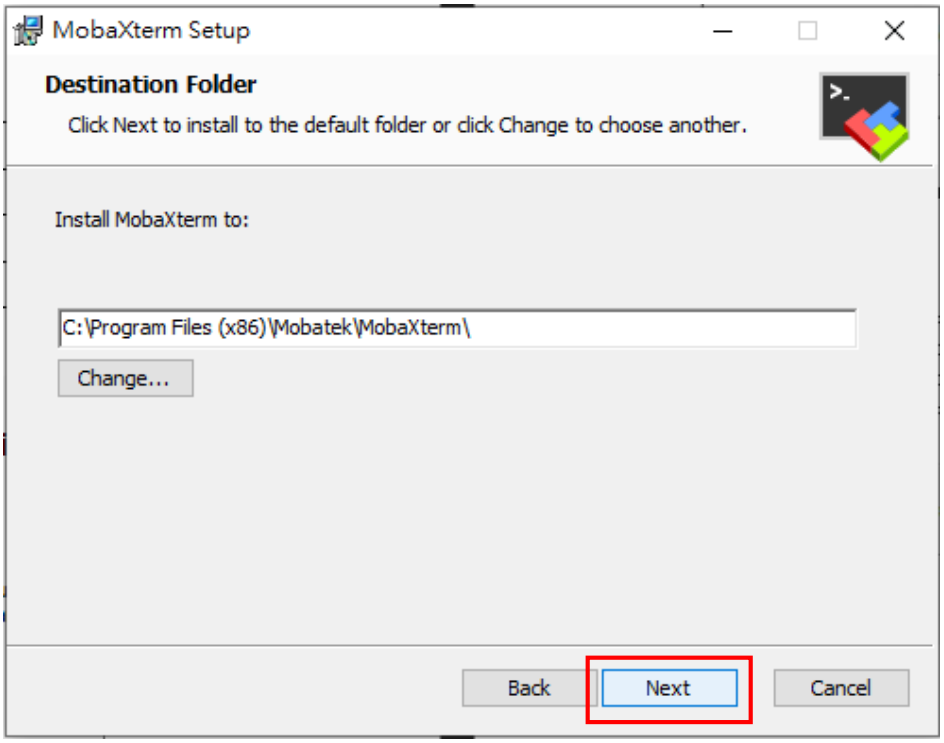
Step2. Install MobaXterm with following steps

Step2.1

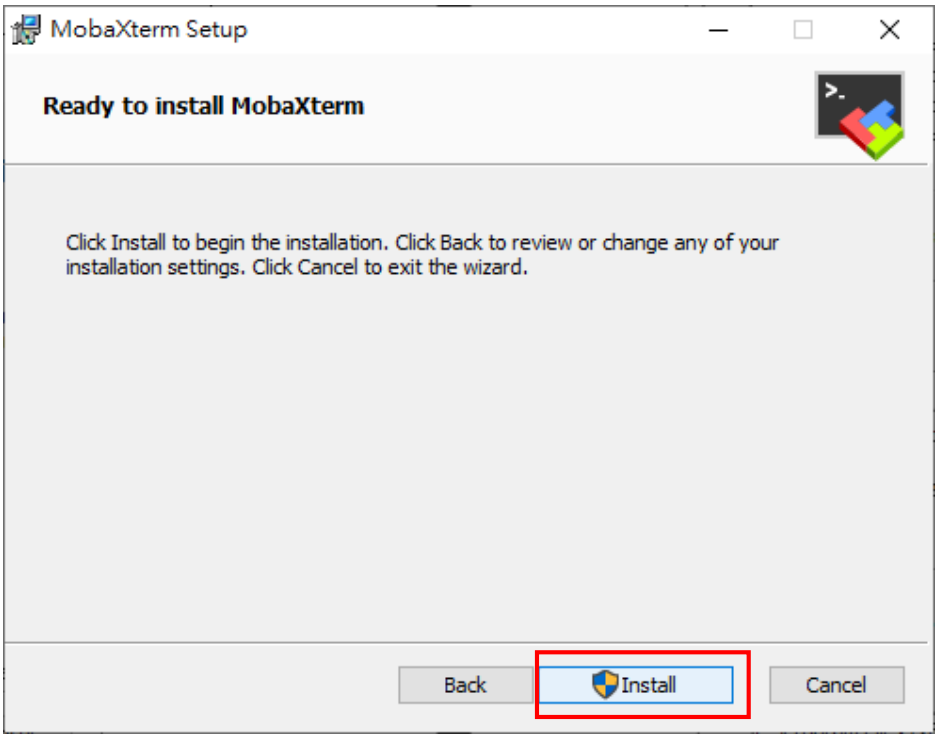


Step2.2

Step2.3



Step2.4



Step3. Launch MobaXterm then connect to the server

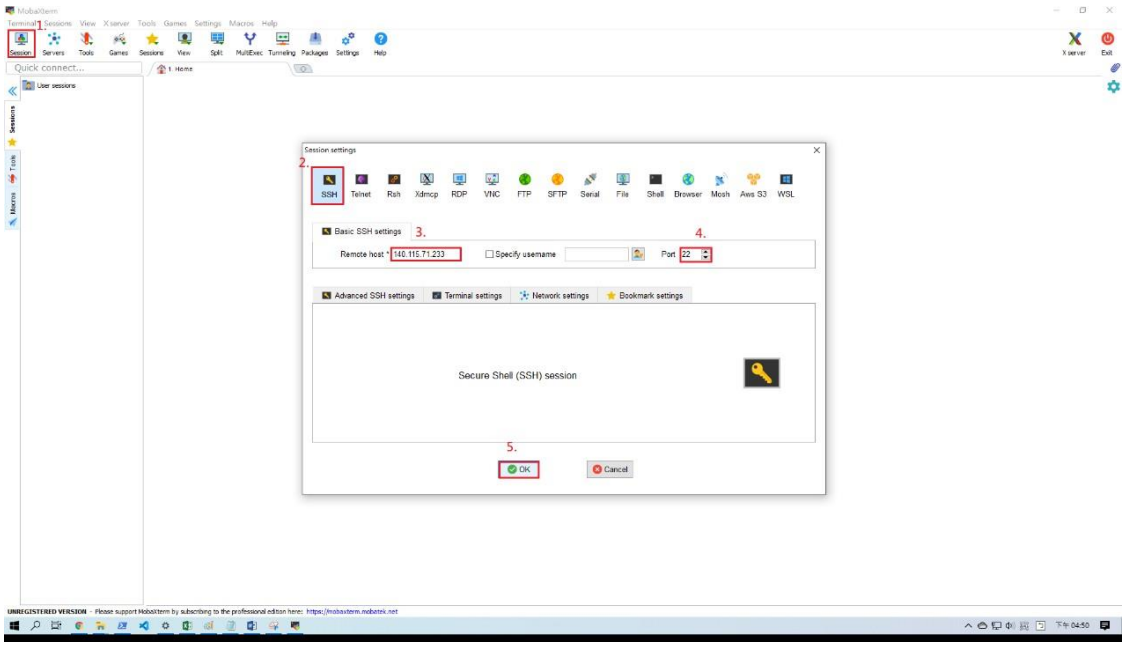
Step3.1 Click session to create a new session

Step3.2 Click ssh to create a new SSH session

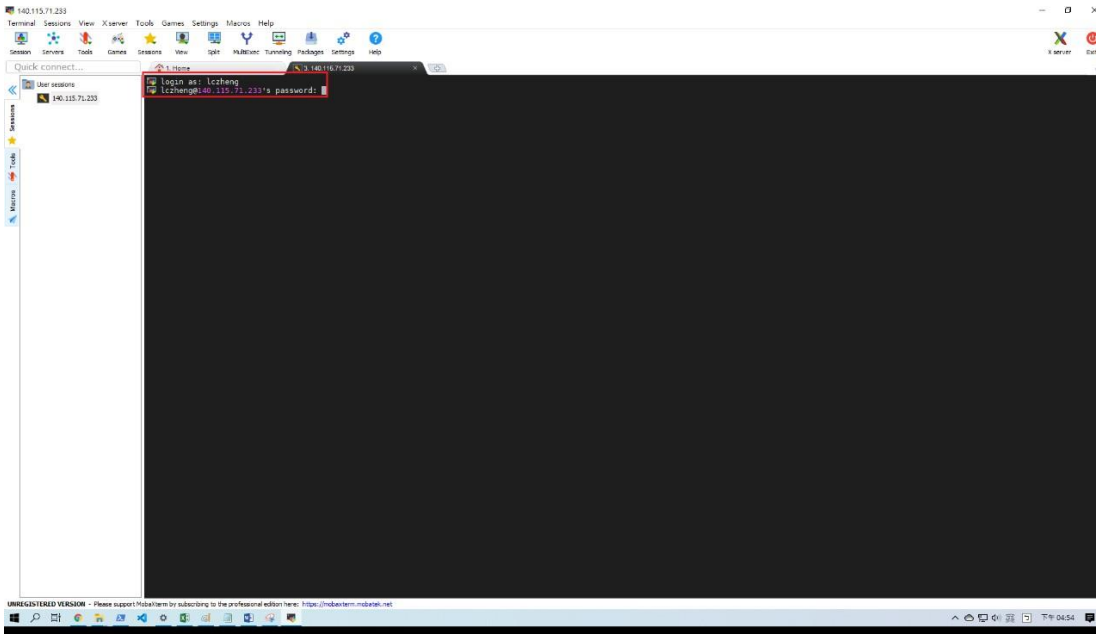
Step3.3 Fill in the given Host to the Host field

Step3.4 set the port number to 22

Step3.5 Click ok



Step3.6 Key in your account and password



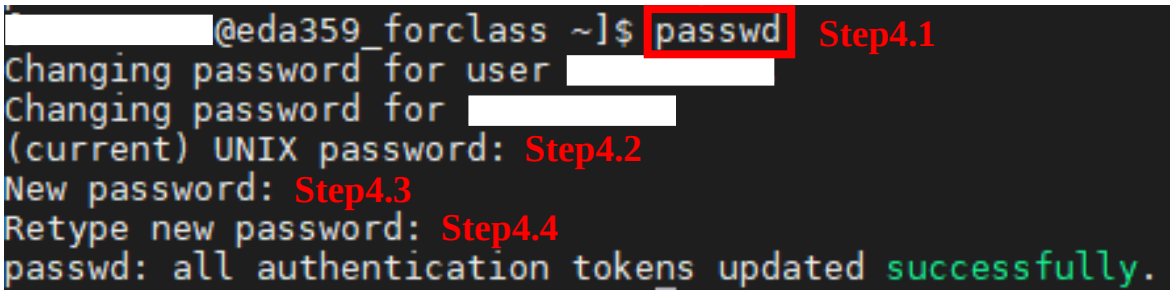
Step4(recommend) Change your password

Step4.1 Key in “ passwd ”

Step4.2 Key in your current password

Step4.3 Key in your new password

Step4.4 Retype your new password again



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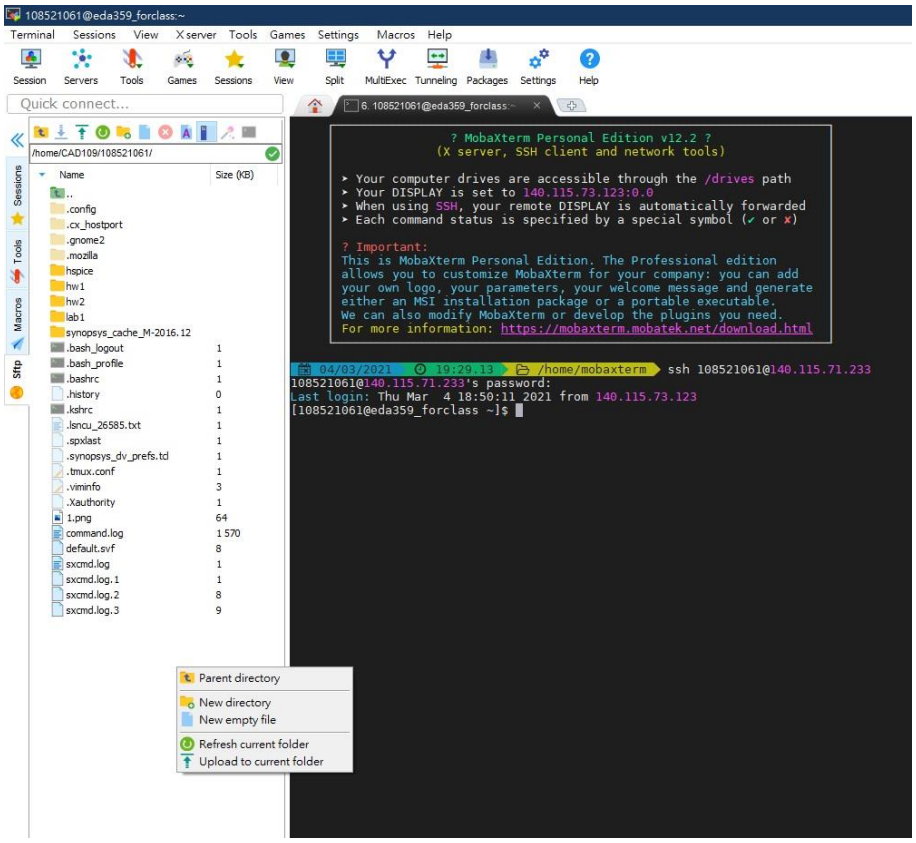
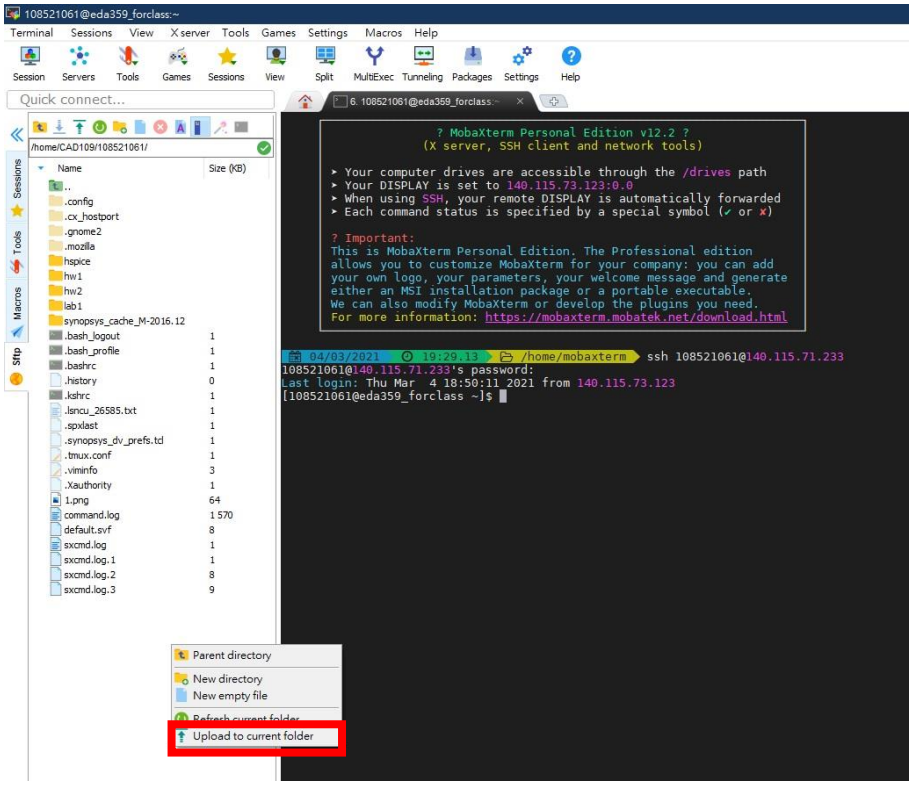
How to upload your source code file to MobaXterm:

There are two ways to upload your file:

1. Right click on your mouse



Click “Upload to current folder”

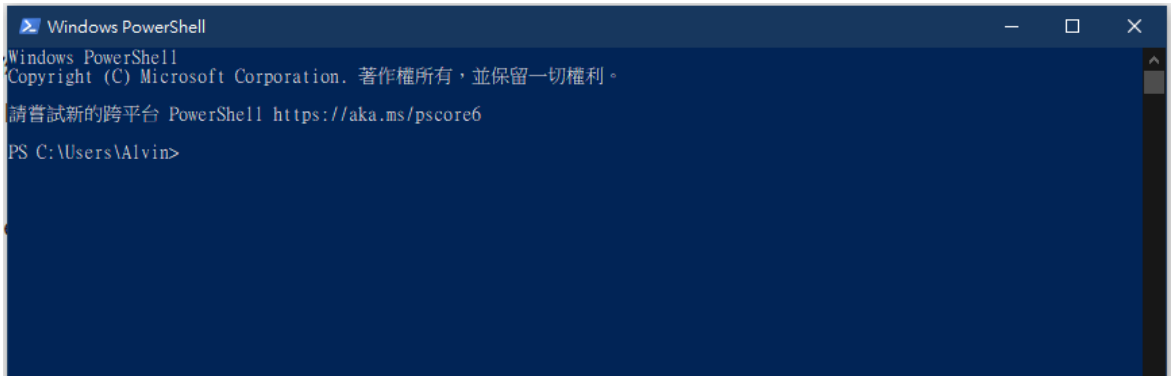


Choose the file you would like to upload

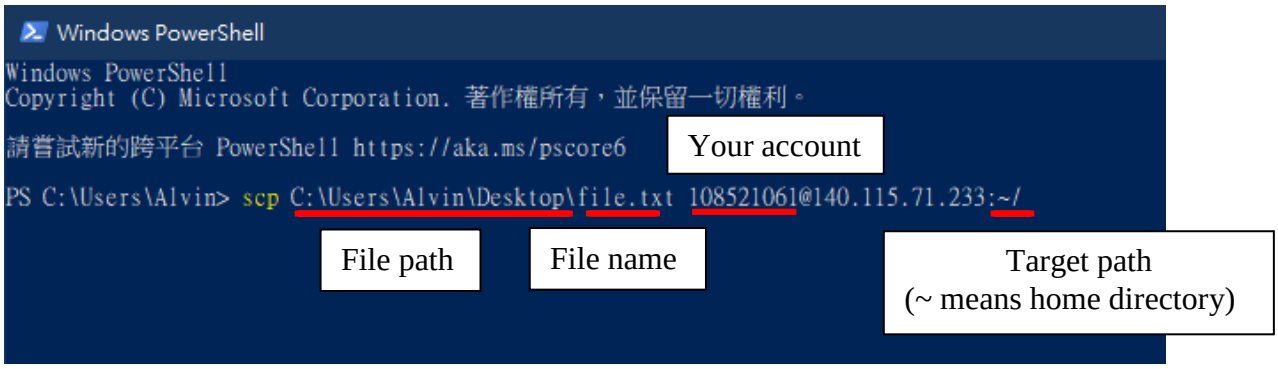
Or you can simply drag your file to the left window of MobaXterm.

2. Use Windows PowerShell (It's useful when your MobaXterm screen freezes)

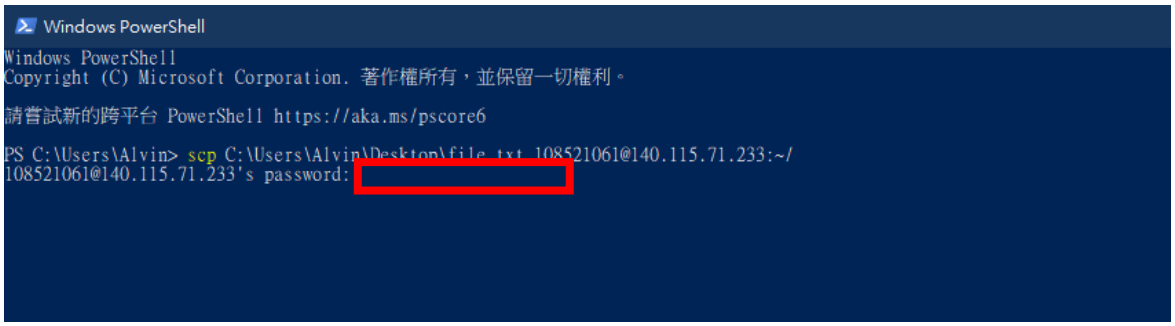
Step1 Open Windows PowerShell



Step2 Use "scp" command



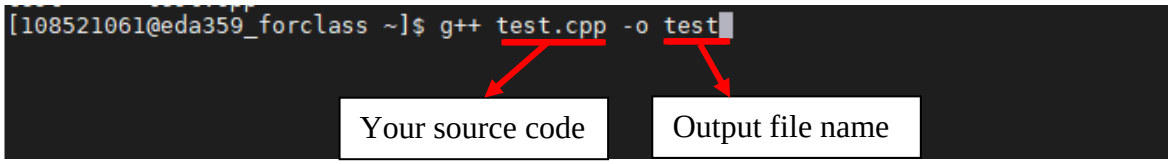
Step2.1 Key in your password



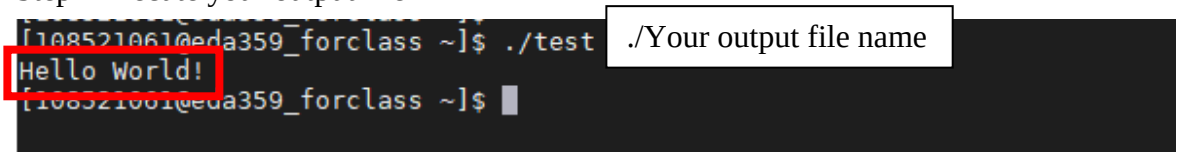
Done!

How to compile and execute your source code on MobaXterm

Step1 Use "g++" command



Step2 Execute your output file



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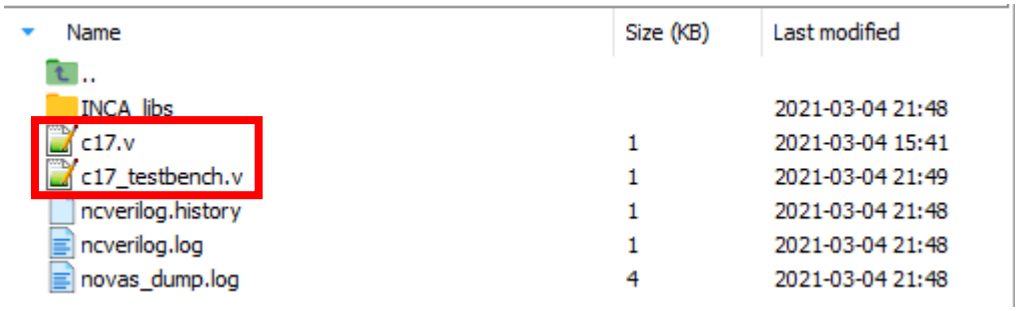
How to use NCverilog

Step1 Make sure you put your verilog code and testbench code files at the same folder (Take c17 as an example)



Step2 Key in the following commands

source /usr/cad/cadence/CIC/incisiv.cshrc

source /usr/cad/synopsys/CIC/verdi.cshrc

```
[108521118@eda359_forclass PA1]$ source /usr/cad/cadence/CIC/incisiv.cshrc
[108521118@eda359_forclass PA1]$ source /usr/cad/synopsys/CIC/verdi.cshrc
```

Step3 Use “ncverilog” command

```
[108521118@eda359_forclass PA1]$ ncverilog +access+r c17.v c17_testbench.v
```

Verilog code file

Testbench code file

Result :

```
[108521118@eda359_forclass PA1]$ ncverilog +access+r c17.v c17_testbench.v
ncverilog: 15.20-s039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Recompiling... reason: file './c17_testbench.v' is newer than expected.
        expected: Thu Mar  4 21:48:39 2021
        actual:   Thu Mar  4 21:49:44 2021
file: c17_testbench.v
        module worklib.c17_tb:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.c17_tb:v <0x5ca70917>
                        streams:   7, words: 12208
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                2       2
                Primitives:             6       1
                Registers:              6       6
                Scalar wires:           5       -
                Initial blocks:         1       1
                Simulation timescale:  1ps
        Writing initial simulation snapshot: worklib.c17_tb:v
Loading snapshot worklib.c17_tb:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
 input pattern = 00000 --> golden value = 00
 your answer = 00
 input pattern = 10101 --> golden value = 11
 your answer = 11
 input pattern = 01010 --> golden value = 11
 your answer = 11
 input pattern = 11011 --> golden value = 11
 your answer = 11
 input pattern = 11111 --> golden value = 10
 your answer = 10
You're all correct!!!
  ***    ***
 *****  *****
**************
 ************
  **********
   ********
    ******
     ****
      **
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
```

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Note:

For the unstable connection of the network of NCU, TA cannot guarantee that you can stably connect to the server. In case you are disconnected to server due to internet interrupt, the running processes will be killed by the OS and you may lost the source code and/or executing results if you do not save them. Therefore, TA strongly recommend you to use the tool, **tmux**, to help you finish your homework. This tool can create network-independent terminals, then you can run programs on them. When a disconnection is occurred, **tmux** will remain the terminals on the server. Therefore, after reconnecting to the server, you can still have the program you executed before the disconnection.

Learning resource:

tmux: https://larrylu.blog/tmux-33a24e595fbc