Andy, Yu-Guang Chen

EE6094 CAD for VLSI Design
Programming Assignment 1 (Due: 23:59:59, 2021/03/09)

You are asked to implement a Verilog generator. The Verilog generator is an EDA tool which can automatically convert a benchmark to the Verilog format for logic synthesis and verification.

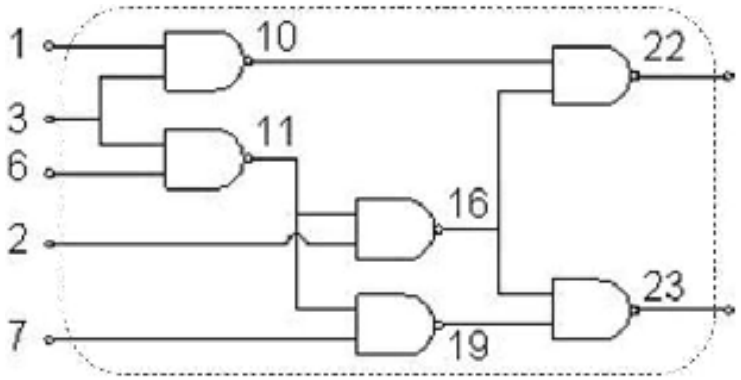
Input file format: Your program will take a benchmark (.bench) file as input. An example is shown as follows:

```
# c17
# 5 inputs
# 2 outputs
# 0 inverter
# 6 gates ( 6 NANDs )

INPUT(1)
INPUT(2)
INPUT(3)
INPUT(6)
INPUT(7)

OUTPUT(22)
OUTPUT(23)

10 = NAND(1, 3)
11 = NAND(3, 6)
16 = NAND(2, 11)
19 = NAND(11, 7)
22 = NAND(10, 16)
23 = NAND(16, 19)
```



C17 circuit structure

The first 5 lines starting with # are the comment lines. These comment lines provide basic information of the benchmark. Then a blank line appears. After that, all the input ports are specified one per line. Then a blank line appears again, follows by all the output ports. A blank line appears again, follows by logic gate connection information.

Output file format: Your program will generate a synthesizable gate-level Verilog (.v) file. An example is shown as follows:

```
module c17 (N1,N2,N3,N6,N7,N22,N23);

input N1,N2,N3,N6,N7;

output N22,N23;

wire N10,N11,N16,N19;

nand NAND2_1 (N10, N1, N3);
nand NAND2_2 (N11, N3, N6);
nand NAND2_3 (N16, N2, N11);
nand NAND2_4 (N19, N11, N7);
nand NAND2_5 (N22, N10, N16);
nand NAND2_6 (N23, N16, N19);

endmodule
```

The first line starts with module as key word, follows by the benchmark name. Then, all the inputs and outputs are printed with the increasing order with a leading "N". Then a blank line appears, follows by the input specification. A blank line appears again, follows by the input specification. A blank line appears again. After that, all the wires (internal connections) used in the benchmark is specified. A blank line appears, follows by circuit descriptions with different gates. Finally, a blank line shows up, follows by keyword endmodule.

Data structure: You can use any data structure to realize your program.

Requirement: You have to write this program in C or C++. I will verify your program on a workstation (info will be released later) with the following command:
$PA1_studID.out c17.bench c17.v
where the first term is the executable file, the second term is the input file name, and the third term is the output file name. Name you file as PA1_studID.cpp.

You should also write a report which should at least include a description of the algorithm you used and how to execute your program. Upload your code and report to ee-class. Some test input files will be announced on the ee-class. The workstation information will be announced later.

Score: Your assignment will be ranked and scored according to (1) the correctness of your solution, (2) the readability of your source code, (3) the report you wrote, and (4) the demo session.