# SH1107

## 128 X 128 Dot Matrix OLED/PLED Segment/Common Driver with Controller

### Features

n Support maximum 128 X 128 dot matrix panel

n Embedded 128 X 128 bits SRAM

n Operating voltage:

- Logic voltage supply: $V_{DD}$ = 1.65V - 3.5V

- DC-DC voltage supply: $AV_{DD}$ = 2.4V -3.5V

- OLED Operating voltage supply: Vpp=7.0V - 16.5V

n Maximum segment output current: 500µA

n Maximum common sink current: 64mA

n 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, and 3-wire & 4-wire serial peripheral interface.

n 400KHz fast I$^2$C bus interface

n Programmable frame frequency and multiplexing ratio

n Row re-mapping and column re-mapping

n Vertical scrolling

n On-chip oscillator

n Available internal DC-DC converter

n 256-step contrast control on monochrome passive OLED panel

n Low power consumption

- Sleep mode: <5µA

n Wide range of operating temperatures: -40 to +85°C

n Available in COG form.

### General Description

SH1107 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1107 consists of 128 segments, 128 commons that can support a maximum display resolution of 128 X 128. It is designed for Common Cathode type OLED panel.

SH1107 embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1107 is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.
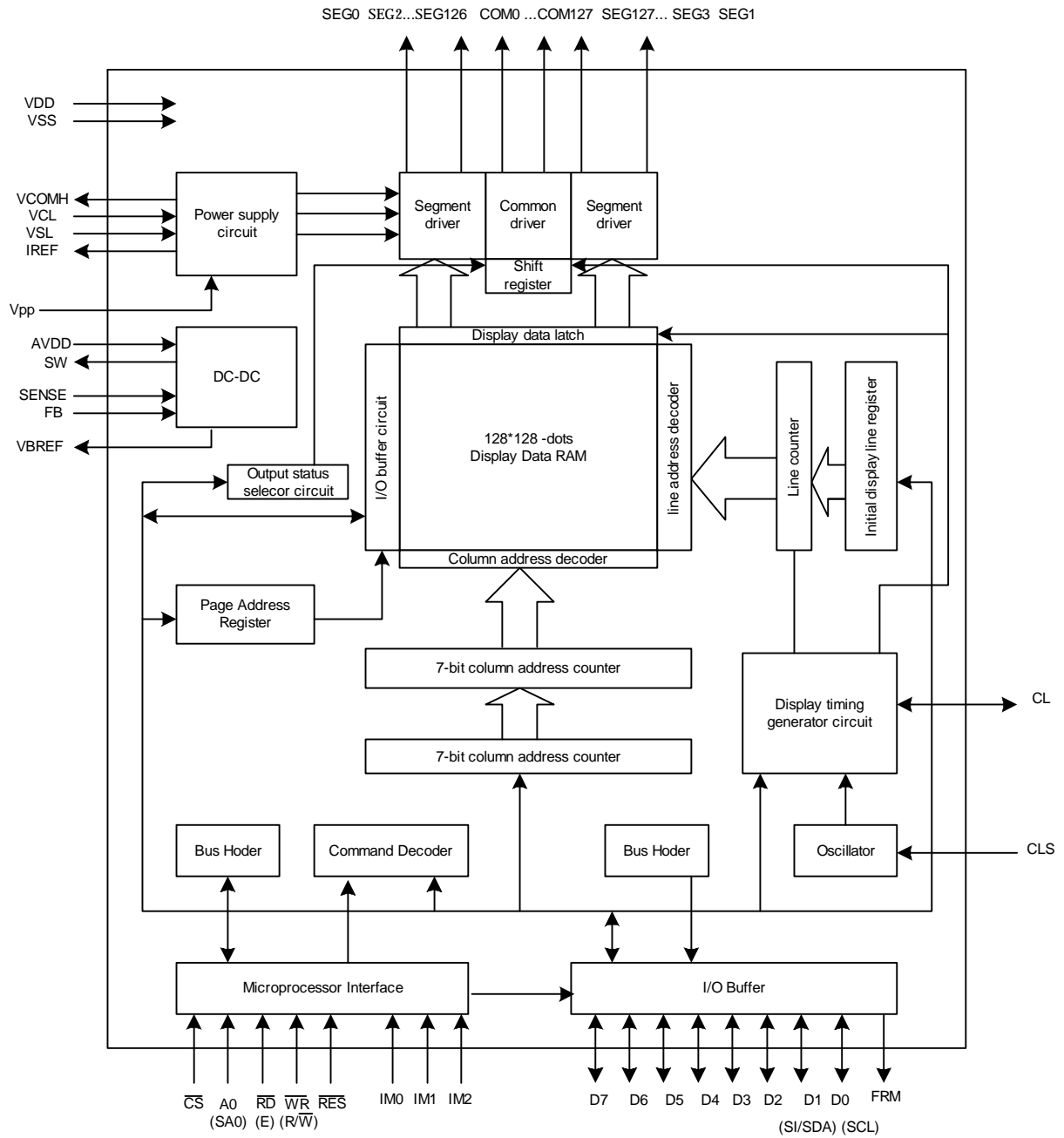
**Block Diagram**

SEG0 SEG2...SEG126   COM0 ...COM127   SEG127... SEG3 SEG1

VDD
VSS

VCOMH
VCL
VSL
IREF

Power supply circuit

Segment driver

Common driver

Segment driver

Shift register

Vpp

AVDD
SW
SENSE
FB
VBREF

DC-DC

Display data latch

Output status selecor circuit

I/O buffer circuit

128*128 -dots
Display Data RAM

line address decoder

Line counter

Initial display line register

Column address decoder

Page Address Register

7-bit column address counter

7-bit column address counter

Display timing generator circuit

CL

Bus Hoder

Command Decoder

Bus Hoder

Oscillator

CLS

Microprocessor Interface

I/O Buffer

$\overline{CS}$   A0   $\overline{RD}$ $\overline{WR}$ $\overline{RES}$   IM0 IM1 IM2        D7   D6   D5   D4   D3   D2   D1   D0   FRM
        (SA0) (E) (R/$\overline{W}$)                                                                    (SI/SDA) (SCL)

**Figure 1 SH1107 Block Diagram**

## Pad Description

### Power Supply

| Pad NO. | Symbol | I/O | Description |
|---|---|---|---|
| 34，35 | V_DD | Supply | 1.65 - 3.5V Power supply for logic and input. |
| 39 | V_DD | O | V_DD output for pad option. |
| 16，17 | AV_DD | Supply | 2.4 - 3.5V power supply for the internal buffer of the DC-DC voltage converter. |
| 25 | V_SS | Supply | Ground for analog. |
| 26 | V_SS | Supply | Ground for logic. |
| 2-6,27 68-72 | V_SS | Supply | Ground for buffer. |
| 37，41 | V_SS | O | Ground output for pad option. |
| 23，24 | V_SL | Supply | This is a segment voltage reference pad. This pad should be connected to V_SS externally. |
| 28-32 | V_CL | Supply | This is a common voltage reference pad. This pad should be connected to V_SS externally. |
| 7-10 21-22 64-67 | V_PP | Supply | This is the most positive voltage supply pad of the chip. It should be supplied externally. |

### OLED Driver Supplies

| Pad NO. | Symbol | I/O | Description |
|---|---|---|---|
| 42-43 | I_REF | O | This is a segment current reference pad. A resistor should be connected between this pad and V_SS. Set the current at 15.625μA. |
| 11-13 | V_COMH | O | This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and V_SS. |
| 18 | V_BREF | O | This is an internal voltage reference pad for booster circuit. A capacitor should be connected between this pad and V_SS. |
| 14-15 | SW | O | This is an output pad driving the gate of the external NMOS of the booster circuit. |
| 19 | FB | I | This is a feedback resistor input pad for the booster circuit. It is used to adjust the booster output voltage level, VPP |
| 20 | SENSE | I | This is a source current pad of the external NMOS of the booster circuit. |

**System Bus Connection Pads**

| Pad NO. | Symbol | I/O | Description |
|---------|--------|-----|-------------|
| 48 | CL | I/O | This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source. |
| 33 | CLS | I | This is the internal clock enable pad. <br> CLS = "H": Internal oscillator circuit is enabled. <br> CLS = "L": Internal oscillator circuit is disabled (require external input). <br> When CLS = "L", an external clock source must be connected to the CL pad for normal operation. |
| 36<br>38<br>40 | IM0<br>IM1<br>IM2 | I | These are the MPU interface mode select pads. <br> <table><tr><td></td><td>8080</td><td>I²C</td><td>6800</td><td>4-wire SPI</td><td>3-wire SPI</td></tr><tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table> |
| 49 | $\overline{CS}$ | I | This pad is the chip select input. When $\overline{CS}$ = "L", then the chip select becomes active, and data/command I/O is enabled. |
| 50 | $\overline{RES}$ | I | This is a reset signal input pad. When $\overline{RES}$ is set to "L", the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level. |
| 51 | A0<br>(SA0) | I | This is the Data/Command control pad that determines whether the data bits are data or a command. <br> A0 = "H": the inputs at D0 to D7 are treated as display data. <br> A0 = "L": the inputs at D0 to D7 are transferred to the command registers. <br> In I²C interface, this pad serves as SA0 to distinguish the different address of OLED driver. |
| 52 | $\overline{WR}$<br>($R/\overline{W}$) | I | This is a MPU interface input pad. <br> When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. <br> When connected to a 6800 Series MPU: This is the read/write control signal input terminal. <br> When $R/\overline{W}$ = "H": Read. <br> When $R/\overline{W}$ = "L": Write. |
| 53 | $\overline{RD}$<br>(E) | I | This is a MPU interface input pad. <br> When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the data bus is in an output status when this signal is "L". <br> When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU. |
| 54-61 | D0 - D7<br>(SCL)<br>(SI/SDA) | I/O<br>I<br>I/O | This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. <br> When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. <br> When the I²C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance. |
| 47 | FRM | O | This pad is No Connection pad, Its signal varies with the frame frequency. Its voltage is equal to VDD when the last common output of every frame is active, and is equal to Vss during other time. |

**OLED Drive Pads**

| Pad NO. | Symbol | I/O | Description |
|---|---|---|---|
| 271-334 | SEG126,124,……4,2,0 | O | These pads are even Segment signal output for OLED display. |
| 75-138 | SEG1,3,……125,127 | O | These pads are odd Segment signal output for OLED display. |
| 140-220 223-269 | COM127- 0 | O | These pads are Common signal output for OLED display. |

**Test Pads**

| Pad NO. | Symbol | I/O | Description |
|---|---|---|---|
| 44 | TEST1 | I | Test pad, internal pull low, no connection for user. |
| 45 | TEST2 | O | Test pad, no connection for user. |
| 46 | TEST3 | I | Test pad, no connection for user. |
| 1，62，63，73，74，139，221，222，270，335 | Dummy | - | Dummy pads, no connection for user |

**Pad Configuration**
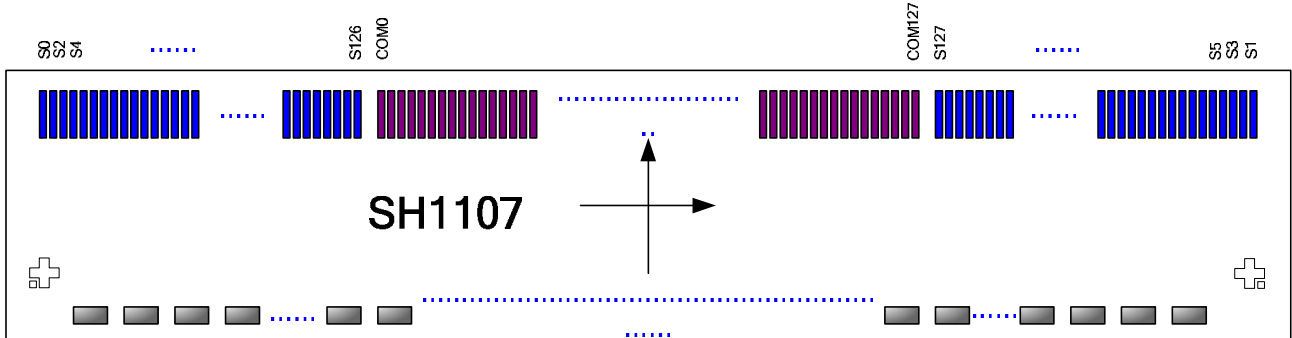


**Chip Outline Dimensions**

| Item | Pad No. | Size (μm) | |
|---|---|---|---|
| | | **X** | **Y** |
| Chip boundary | - | 8256 | 732 |
| Chip height | All pads | 300 | |
| Bump size | I/O | 95 | 40 |
| | SEG | 15 | 110 |
| | COM | 15 | 110 |
| Pad pitch | COM | 30 | |
| | SEG | 28 | |
| | I/O | 110 | |
| Bump height | All pads | $9\pm2$ | |

**Alignment Mark Location**                                          Unit:   μm

| NO | X | Y |
|---|---|---|
| ALK_L | -3960 | -163 |
| ALK_R | 3960 | -163 |



ALK_L                              ALK_R
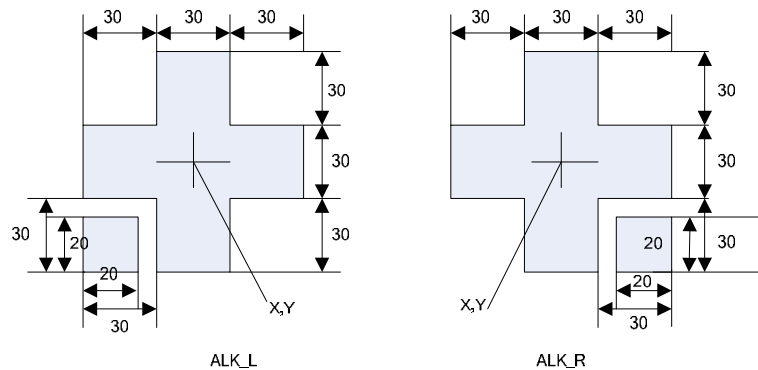
## Pad Location (Total:    pads)

unit:    μm

| Pad No. | Designation | X | Y | Pad No. | Designation | X | Y | Pad No. | Designation | X | Y | Pad No. | Designation | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | DUMMY | -3960 | -283 | 82 | SEG[15] | 3823 | 252 | 163 | COM[104] | 1350 | 252 | 244 | COM[25] | -1290 | 252 |
| 2 | GND | -3850 | -283 | 83 | SEG[17] | 3795 | 252 | 164 | COM[103] | 1320 | 252 | 245 | COM[24] | -1320 | 252 |
| 3 | GND | -3740 | -283 | 84 | SEG[19] | 3767 | 252 | 165 | COM[102] | 1290 | 252 | 246 | COM[23] | -1350 | 252 |
| 4 | GND | -3630 | -283 | 85 | SEG[21] | 3739 | 252 | 166 | COM[101] | 1260 | 252 | 247 | COM[22] | -1380 | 252 |
| 5 | GND | -3520 | -283 | 86 | SEG[23] | 3711 | 252 | 167 | COM[100] | 1230 | 252 | 248 | COM[21] | -1410 | 252 |
| 6 | GND | -3410 | -283 | 87 | SEG[25] | 3683 | 252 | 168 | COM[99] | 1200 | 252 | 249 | COM[20] | -1440 | 252 |
| 7 | VPP | -3300 | -283 | 88 | SEG[27] | 3655 | 252 | 169 | COM[98] | 1170 | 252 | 250 | COM[19] | -1470 | 252 |
| 8 | VPP | -3190 | -283 | 89 | SEG[29] | 3627 | 252 | 170 | COM[97] | 1140 | 252 | 251 | COM[18] | -1500 | 252 |
| 9 | VPP | -3080 | -283 | 90 | SEG[31] | 3599 | 252 | 171 | COM[96] | 1110 | 252 | 252 | COM[17] | -1530 | 252 |
| 10 | VPP | -2970 | -283 | 91 | SEG[33] | 3571 | 252 | 172 | COM[95] | 1080 | 252 | 253 | COM[16] | -1560 | 252 |
| 11 | VCOMH | -2860 | -283 | 92 | SEG[35] | 3543 | 252 | 173 | COM[94] | 1050 | 252 | 254 | COM[15] | -1590 | 252 |
| 12 | VCOMH | -2750 | -283 | 93 | SEG[37] | 3515 | 252 | 174 | COM[93] | 1020 | 252 | 255 | COM[14] | -1620 | 252 |
| 13 | VCOMH | -2640 | -283 | 94 | SEG[39] | 3487 | 252 | 175 | COM[92] | 990 | 252 | 256 | COM[13] | -1650 | 252 |
| 14 | SW | -2530 | -283 | 95 | SEG[41] | 3459 | 252 | 176 | COM[91] | 960 | 252 | 257 | COM[12] | -1680 | 252 |
| 15 | SW | -2420 | -283 | 96 | SEG[43] | 3431 | 252 | 177 | COM[90] | 930 | 252 | 258 | COM[11] | -1710 | 252 |
| 16 | AVDD | -2310 | -283 | 97 | SEG[45] | 3403 | 252 | 178 | COM[89] | 900 | 252 | 259 | COM[10] | -1740 | 252 |
| 17 | AVDD | -2200 | -283 | 98 | SEG[47] | 3375 | 252 | 179 | COM[88] | 870 | 252 | 260 | COM[9] | -1770 | 252 |
| 18 | VBREF | -2090 | -283 | 99 | SEG[49] | 3347 | 252 | 180 | COM[87] | 840 | 252 | 261 | COM[8] | -1800 | 252 |
| 19 | FB | -1980 | -283 | 100 | SEG[51] | 3319 | 252 | 181 | COM[86] | 810 | 252 | 262 | COM[7] | -1830 | 252 |
| 20 | SENSE | -1870 | -283 | 101 | SEG[53] | 3291 | 252 | 182 | COM[85] | 780 | 252 | 263 | COM[6] | -1860 | 252 |
| 21 | VPP | -1760 | -283 | 102 | SEG[55] | 3263 | 252 | 183 | COM[84] | 750 | 252 | 264 | COM[5] | -1890 | 252 |
| 22 | VPP | -1650 | -283 | 103 | SEG[57] | 3235 | 252 | 184 | COM[83] | 720 | 252 | 265 | COM[4] | -1920 | 252 |
| 23 | VSL | -1540 | -283 | 104 | SEG[59] | 3207 | 252 | 185 | COM[82] | 690 | 252 | 266 | COM[3] | -1950 | 252 |
| 24 | VSL | -1430 | -283 | 105 | SEG[61] | 3179 | 252 | 186 | COM[81] | 660 | 252 | 267 | COM[2] | -1980 | 252 |
| 25 | GND(ana) | -1320 | -283 | 106 | SEG[63] | 3151 | 252 | 187 | COM[80] | 630 | 252 | 268 | COM[1] | -2010 | 252 |
| 26 | GND(logic) | -1210 | -283 | 107 | SEG[65] | 3123 | 252 | 188 | COM[79] | 600 | 252 | 269 | COM[0] | -2040 | 252 |
| 27 | GND(buf) | -1100 | -283 | 108 | SEG[67] | 3095 | 252 | 189 | COM[78] | 570 | 252 | 270 | DUMMY | -2070 | 252 |
| 28 | VCL | -990 | -283 | 109 | SEG[69] | 3067 | 252 | 190 | COM[77] | 540 | 252 | 271 | SEG[126] | -2255 | 252 |
| 29 | VCL | -880 | -283 | 110 | SEG[71] | 3039 | 252 | 191 | COM[76] | 510 | 252 | 272 | SEG[124] | -2283 | 252 |
| 30 | VCL | -770 | -283 | 111 | SEG[73] | 3011 | 252 | 192 | COM[75] | 480 | 252 | 273 | SEG[122] | -2311 | 252 |
| 31 | VCL | -660 | -283 | 112 | SEG[75] | 2983 | 252 | 193 | COM[74] | 450 | 252 | 274 | SEG[120] | -2339 | 252 |
| 32 | VCL | -550 | -283 | 113 | SEG[77] | 2955 | 252 | 194 | COM[73] | 420 | 252 | 275 | SEG[118] | -2367 | 252 |
| 33 | CLS | -440 | -283 | 114 | SEG[79] | 2927 | 252 | 195 | COM[72] | 390 | 252 | 276 | SEG[116] | -2395 | 252 |
| 34 | VCC | -330 | -283 | 115 | SEG[81] | 2899 | 252 | 196 | COM[71] | 360 | 252 | 277 | SEG[114] | -2423 | 252 |
| 35 | VCC | -220 | -283 | 116 | SEG[83] | 2871 | 252 | 197 | COM[70] | 330 | 252 | 278 | SEG[112] | -2451 | 252 |
| 36 | IM0 | -110 | -283 | 117 | SEG[85] | 2843 | 252 | 198 | COM[69] | 300 | 252 | 279 | SEG[110] | -2479 | 252 |
| 37 | GND | 0 | -283 | 118 | SEG[87] | 2815 | 252 | 199 | COM[68] | 270 | 252 | 280 | SEG[108] | -2507 | 252 |
| 38 | IM1 | 110 | -283 | 119 | SEG[89] | 2787 | 252 | 200 | COM[67] | 240 | 252 | 281 | SEG[106] | -2535 | 252 |
| 39 | VCC | 220 | -283 | 120 | SEG[91] | 2759 | 252 | 201 | COM[66] | 210 | 252 | 282 | SEG[104] | -2563 | 252 |
| 40 | IM2 | 330 | -283 | 121 | SEG[93] | 2731 | 252 | 202 | COM[65] | 180 | 252 | 283 | SEG[102] | -2591 | 252 |
| 41 | GND | 440 | -283 | 122 | SEG[95] | 2703 | 252 | 203 | COM[64] | 150 | 252 | 284 | SEG[100] | -2619 | 252 |
| 42 | IREF | 550 | -283 | 123 | SEG[97] | 2675 | 252 | 204 | COM[63] | 120 | 252 | 285 | SEG[98] | -2647 | 252 |
| 43 | IREF | 660 | -283 | 124 | SEG[99] | 2647 | 252 | 205 | COM[62] | 90 | 252 | 286 | SEG[96] | -2675 | 252 |
| 44 | TEST1 | 770 | -283 | 125 | SEG[101] | 2619 | 252 | 206 | COM[61] | 60 | 252 | 287 | SEG[94] | -2703 | 252 |
| 45 | TEST2 | 880 | -283 | 126 | SEG[103] | 2591 | 252 | 207 | COM[60] | 30 | 252 | 288 | SEG[92] | -2731 | 252 |
| 46 | TEST3 | 990 | -283 | 127 | SEG[105] | 2563 | 252 | 208 | COM[59] | 0 | 252 | 289 | SEG[90] | -2759 | 252 |
| 47 | FRM | 1100 | -283 | 128 | SEG[107] | 2535 | 252 | 209 | COM[58] | -30 | 252 | 290 | SEG[88] | -2787 | 252 |
| 48 | CL | 1210 | -283 | 129 | SEG[109] | 2507 | 252 | 210 | COM[57] | -60 | 252 | 291 | SEG[86] | -2815 | 252 |
| 49 | CSB | 1320 | -283 | 130 | SEG[111] | 2479 | 252 | 211 | COM[56] | -90 | 252 | 292 | SEG[84] | -2843 | 252 |
| 50 | RESB | 1430 | -283 | 131 | SEG[113] | 2451 | 252 | 212 | COM[55] | -120 | 252 | 293 | SEG[82] | -2871 | 252 |
| 51 | A0 | 1540 | -283 | 132 | SEG[115] | 2423 | 252 | 213 | COM[54] | -150 | 252 | 294 | SEG[80] | -2899 | 252 |
| 52 | WRB | 1650 | -283 | 133 | SEG[117] | 2395 | 252 | 214 | COM[53] | -180 | 252 | 295 | SEG[78] | -2927 | 252 |
| 53 | RDB | 1760 | -283 | 134 | SEG[119] | 2367 | 252 | 215 | COM[52] | -210 | 252 | 296 | SEG[76] | -2955 | 252 |
| 54 | D[0] | 1870 | -283 | 135 | SEG[121] | 2339 | 252 | 216 | COM[51] | -240 | 252 | 297 | SEG[74] | -2983 | 252 |
| 55 | D[1] | 1980 | -283 | 136 | SEG[123] | 2311 | 252 | 217 | COM[50] | -270 | 252 | 298 | SEG[72] | -3011 | 252 |
| 56 | D[2] | 2090 | -283 | 137 | SEG[125] | 2283 | 252 | 218 | COM[49] | -300 | 252 | 299 | SEG[70] | -3039 | 252 |
| 57 | D[3] | 2200 | -283 | 138 | SEG[127] | 2255 | 252 | 219 | COM[48] | -330 | 252 | 300 | SEG[68] | -3067 | 252 |
| 58 | D[4] | 2310 | -283 | 139 | DUMMY | 2070 | 252 | 220 | COM[47] | -360 | 252 | 301 | SEG[66] | -3095 | 252 |
| 59 | D[5] | 2420 | -283 | 140 | COM[127] | 2040 | 252 | 221 | DUMMY | -390 | 252 | 302 | SEG[64] | -3123 | 252 |
| 60 | D[6] | 2530 | -283 | 141 | COM[126] | 2010 | 252 | 222 | DUMMY | -630 | 252 | 303 | SEG[62] | -3151 | 252 |
| 61 | D[7] | 2640 | -283 | 142 | COM[125] | 1980 | 252 | 223 | COM[46] | -660 | 252 | 304 | SEG[60] | -3179 | 252 |
| 62 | DUMMY | 2750 | -283 | 143 | COM[124] | 1950 | 252 | 224 | COM[45] | -690 | 252 | 305 | SEG[58] | -3207 | 252 |
| 63 | DUMMY | 2860 | -283 | 144 | COM[123] | 1920 | 252 | 225 | COM[44] | -720 | 252 | 306 | SEG[56] | -3235 | 252 |
| 64 | VPP | 2970 | -283 | 145 | COM[122] | 1890 | 252 | 226 | COM[43] | -750 | 252 | 307 | SEG[54] | -3263 | 252 |
| 65 | VPP | 3080 | -283 | 146 | COM[121] | 1860 | 252 | 227 | COM[42] | -780 | 252 | 308 | SEG[52] | -3291 | 252 |
| 66 | VPP | 3190 | -283 | 147 | COM[120] | 1830 | 252 | 228 | COM[41] | -810 | 252 | 309 | SEG[50] | -3319 | 252 |
| 67 | VPP | 3300 | -283 | 148 | COM[119] | 1800 | 252 | 229 | COM[40] | -840 | 252 | 310 | SEG[48] | -3347 | 252 |
| 68 | GND | 3410 | -283 | 149 | COM[118] | 1770 | 252 | 230 | COM[39] | -870 | 252 | 311 | SEG[46] | -3375 | 252 |
| 69 | GND | 3520 | -283 | 150 | COM[117] | 1740 | 252 | 231 | COM[38] | -900 | 252 | 312 | SEG[44] | -3403 | 252 |
| 70 | GND | 3630 | -283 | 151 | COM[116] | 1710 | 252 | 232 | COM[37] | -930 | 252 | 313 | SEG[42] | -3431 | 252 |
| 71 | GND | 3740 | -283 | 152 | COM[115] | 1680 | 252 | 233 | COM[36] | -960 | 252 | 314 | SEG[40] | -3459 | 252 |
| 72 | GND | 3850 | -283 | 153 | COM[114] | 1650 | 252 | 234 | COM[35] | -990 | 252 | 315 | SEG[38] | -3487 | 252 |
| 73 | DUMMY | 3960 | -283 | 154 | COM[113] | 1620 | 252 | 235 | COM[34] | -1020 | 252 | 316 | SEG[36] | -3515 | 252 |
| 74 | DUMMY | 4047 | 252 | 155 | COM[111] | 1590 | 252 | 236 | COM[33] | -1050 | 252 | 317 | SEG[34] | -3543 | 252 |
| 75 | SEG[1] | 4019 | 252 | 156 | COM[110] | 1560 | 252 | 237 | COM[32] | -1080 | 252 | 318 | SEG[32] | -3571 | 252 |
| 76 | SEG[3] | 3991 | 252 | 157 | COM[109] | 1530 | 252 | 238 | COM[31] | -1110 | 252 | 319 | SEG[30] | -3599 | 252 |
| 77 | SEG[5] | 3963 | 252 | 158 | COM[108] | 1500 | 252 | 239 | COM[30] | -1140 | 252 | 320 | SEG[28] | -3627 | 252 |
| 78 | SEG[7] | 3935 | 252 | 159 | COM[107] | 1470 | 252 | 240 | COM[29] | -1170 | 252 | 321 | SEG[26] | -3655 | 252 |
| 79 | SEG[9] | 3907 | 252 | 160 | COM[106] | 1440 | 252 | 241 | COM[28] | -1200 | 252 | 322 | SEG[24] | -3683 | 252 |
| 80 | SEG[11] | 3879 | 252 | 161 | COM[106] | 1410 | 252 | 242 | COM[27] | -1230 | 252 | 323 | SEG[22] | -3711 | 252 |
| 81 | SEG[13] | 3851 | 252 | 162 | COM[105] | 1380 | 252 | 243 | COM[26] | -1260 | 252 | 324 | SEG[20] | -3739 | 252 |

| Pad No. | Designation | X | Y |
|---------|-------------|-------|-----|
| 325 | SEG[18] | -3767 | 252 |
| 326 | SEG[16] | -3795 | 252 |
| 327 | SEG[14] | -3823 | 252 |
| 328 | SEG[12] | -3851 | 252 |
| 329 | SEG[10] | -3879 | 252 |
| 330 | SEG[8] | -3907 | 252 |
| 331 | SEG[6] | -3935 | 252 |
| 332 | SEG[4] | -3963 | 252 |
| 333 | SEG[2] | -3991 | 252 |
| 334 | SEG[0] | -4019 | 252 |

## Functional Description

### Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) or I$^2$C Interface can be selected by different selections of IM0~2 as shown in Table 1.

**Table 1**

| Interface | Config | | | Data signal | | | | | | | | Control signal | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IM0 | IM1 | IM2 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E/$\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | A0 | $\overline{RES}$ |
| **6800** | 0 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E | $R/\overline{W}$ | $\overline{CS}$ | A0 | $\overline{RES}$ |
| **8080** | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | A0 | $\overline{RES}$ |
| **4-Wire SPI** | 0 | 0 | 0 | Hz（Note1) | | | | | | SI | SCL | Pull High or Low | | $\overline{CS}$ | A0 | $\overline{RES}$ |
| **3-Wire SPI** | 1 | 0 | 0 | Hz（Note1) | | | | | | SI | SCL | Pull High or Low | | $\overline{CS}$ | Pull Low | $\overline{RES}$ |
| **I$^2$C** | 0 | 1 | 0 | Hz（Note1) | | | | | | SDA | SCL | Pull High or Low | | Pull Low | SA0 | $\overline{RES}$ |

Note1: When Serial Interface (SPI) or I$^2$C Interface is selected, D7~D2 is Hz. D7~D2 is recommended to connect the VDD or VSS. It is also allowed to leave D7~D2 unconnected.

### 6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ ($R/\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. When $\overline{WR}$ ($R/\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ ($R/\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table 2.

**Table 2**

| IM0 | IM1 | IM2 | Type | $\overline{CS}$ | A0 | $\overline{RD}$ | $\overline{WR}$ | D0 to D7 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 6800 microprocessor bus | $\overline{CS}$ | A0 | E | $R/\overline{W}$ | D0 to D7 |

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure 2 below.

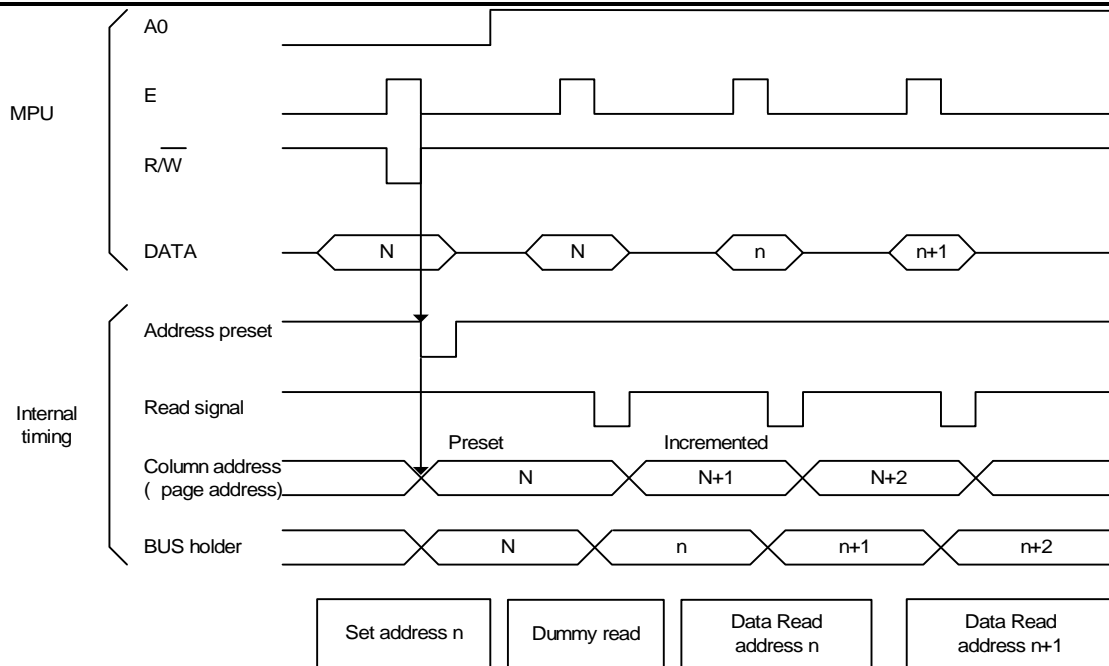**Figure 2**

**8080-series Parallel Interface**

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ ( $R/\overline{W}$ ), $\overline{RD}$ (E), A0 and $\overline{CS}$ . The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by A0 signal. The $\overline{WR}$ ( $R/\overline{W}$ ) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table 3.

**Table 3**

| IM0 | IM1 | IM2 | Type | $\overline{CS}$ | A0 | $\overline{RD}$ | $\overline{WR}$ | D0 to D7 |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 8080 microprocessor bus | $\overline{CS}$ | A0 | $\overline{RD}$ | $\overline{WR}$ | D0 to D7 |

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

**Data Bus Signals**

The SH1107 identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ ( $R/\overline{W}$ ) signals.

**Table 4**

| Common | 6800 processor | 8080 processor | | Function |
|---|---|---|---|---|
| A0 | ( $R/\overline{W}$ ) | $\overline{RD}$ | $\overline{WR}$ | |
| 1 | 1 | 0 | 1 | Reads display data. |
| 1 | 0 | 1 | 0 | Writes display data. |
| 0 | 1 | 0 | 1 | Reads status. |
| 0 | 0 | 1 | 0 | Writes control data in internal register. (Command) |

**4 Wire Serial Interface (4-wire SPI)**

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$ . SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6 … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM (A0=1) or command register (A0=0) in the same clock. See Figure 3.

**Table 5**

| IM0 | IM1 | IM2 | Type | $\overline{CS}$ | A0 | $\overline{RD}$ | $\overline{WR}$ | D0 | D1 | D2 to D7 |
|-----|-----|-----|------|------|----|------|------|-----|-----|----------|
| 0 | 0 | 0 | 4-wire SPI | $\overline{CS}$ | A0 | - | - | SCL | SI | (Hz) |

Note: "-" pin must always be HIGH or LOW. D7~D2 is recommended to connect the VDD or VSS. It's also allowed to leave D7~D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on

$\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the

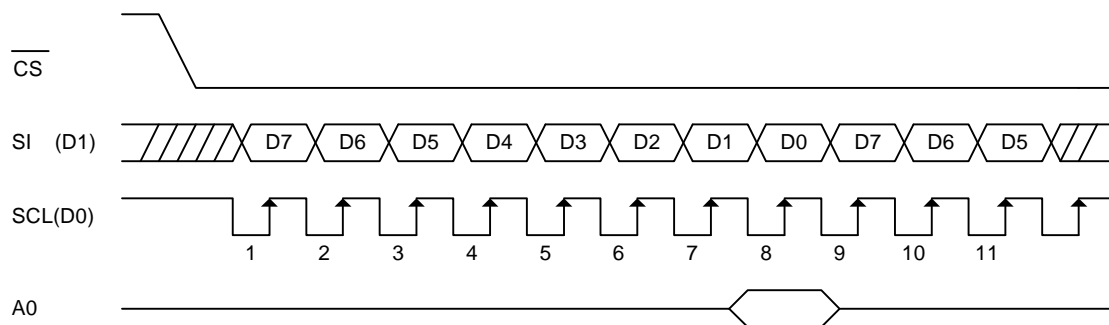$\overline{CS}$ always keep low, but it is not recommended.



**Figure 3   4-wire SPI data transfer**

**l**     When the chip is not active, the shift registers and the counter are reset to their initial statuses.

**l**     Read is not possible while in serial interface mode.

**l**     Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

**3 Wire Serial Interface (3-wire SPI)**

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into a 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6 … D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0). See Figure 4.

**Table 6**

| IM0 | IM1 | IM2 | Type | $\overline{CS}$ | A0 | $\overline{RD}$ | $\overline{WR}$ | D0 | D1 | D2 to D7 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 3-wire SPI | $\overline{CS}$ | Pull Low | - | - | SCL | SI | (Hz) |

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or VSS. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.
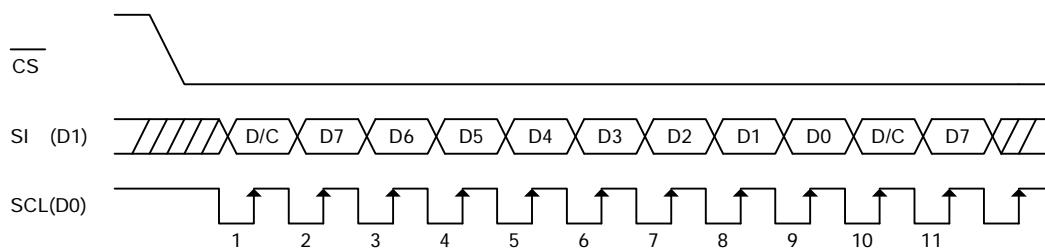


**Figure 4    3-wire SPI data transfer**

l    When the chip is not active, the shift registers and the counter are reset to their initial statuses.

l    Read is not possible while in serial interface mode.

l    Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

**I²C-bus Interface**

The SH1107 can transfer data via a standard I²C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

**Table 7**

| IM0 | IM1 | IM2 | Type | $\overline{CS}$ | A0 | $\overline{RD}$ | $\overline{WR}$ | D0 | D1 | D2 to D7 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | I²C Interface | Pull Low | SA0 | - | - | SCL | SDA | (Hz) |

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or VSS. It is also allowed to leave D7~ D2 unconnected.

$\overline{CS}$ Signal could always pull low in I²C-bus application.

**Characteristics of the I²C-bus**

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

**Note: The positive supply of pull-up resistor must equal to the value of VDD.**

**Bit Transfer**

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.
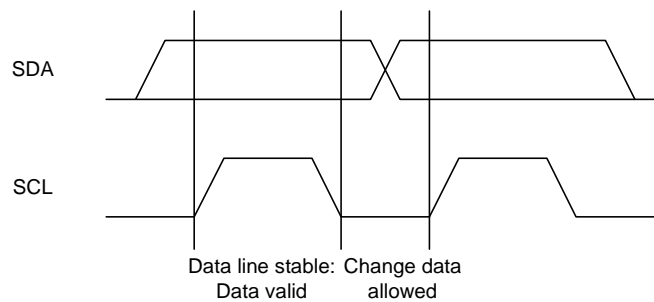


Data line stable: Change data
Data valid allowed

**Figure 5   Bit Transfer**

**Start and Stop conditions**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).
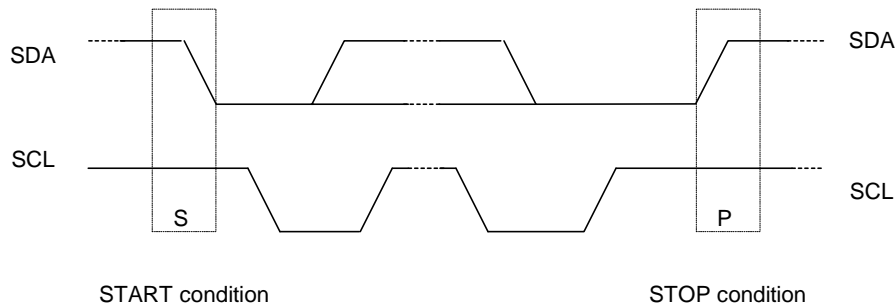
SDA                            SDA

SCL                            SCL

S                            P

START condition                       STOP condition

**Figure 6    Start and Stop conditions**

**System configuration**

**I**   Transmitter: The device that sends the data to the bus.

**I**   Receiver: The device that receives the data from the bus.

**I**   Master: The device that initiates a transfer generates clock signals and terminates a transfer.

**I**   Slave: The device addressed by a master.

**I**   Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message

**I**   Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

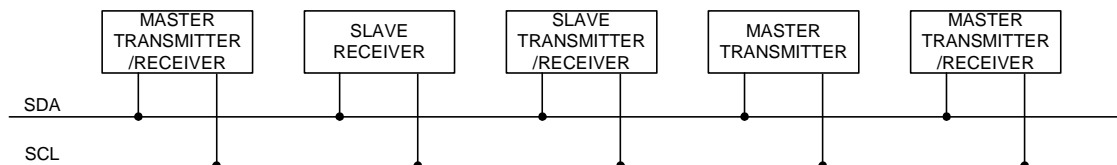**I**   Synchronization: Procedure to synchronize the clock signals of two or more devices.

| MASTER TRANSMITTER /RECEIVER | SLAVE RECEIVER | SLAVE TRANSMITTER /RECEIVER | MASTER TRANSMITTER | MASTER TRANSMITTER /RECEIVER |

SDA

SCL

**Figure 7    System configuration**

**Acknowledge**

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.
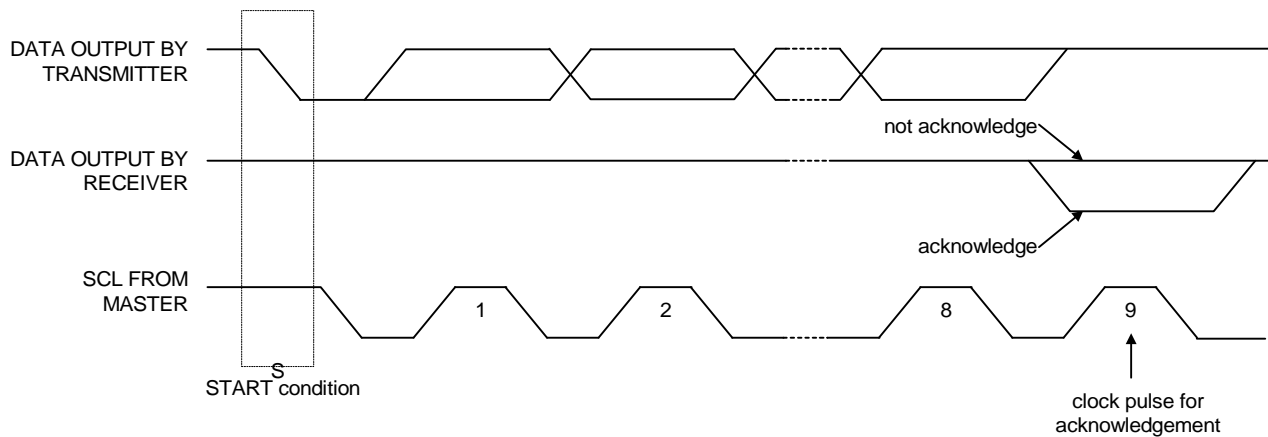
**Figure 8    Acknowledge**

**Protocol**

The SH1107 supports both read and write access. The $R/\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I²C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1107. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1 (VDD). The I²C-bus protocol is illustrated in Fig.7. The sequence is initiated with a START condition (S) from the I²C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and $D/\overline{C}$ (note1), plus a data byte (see Fig.9). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the $D/\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1107 device. If the $D/\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a stop condition (P). If the $R/\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the $D/\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.
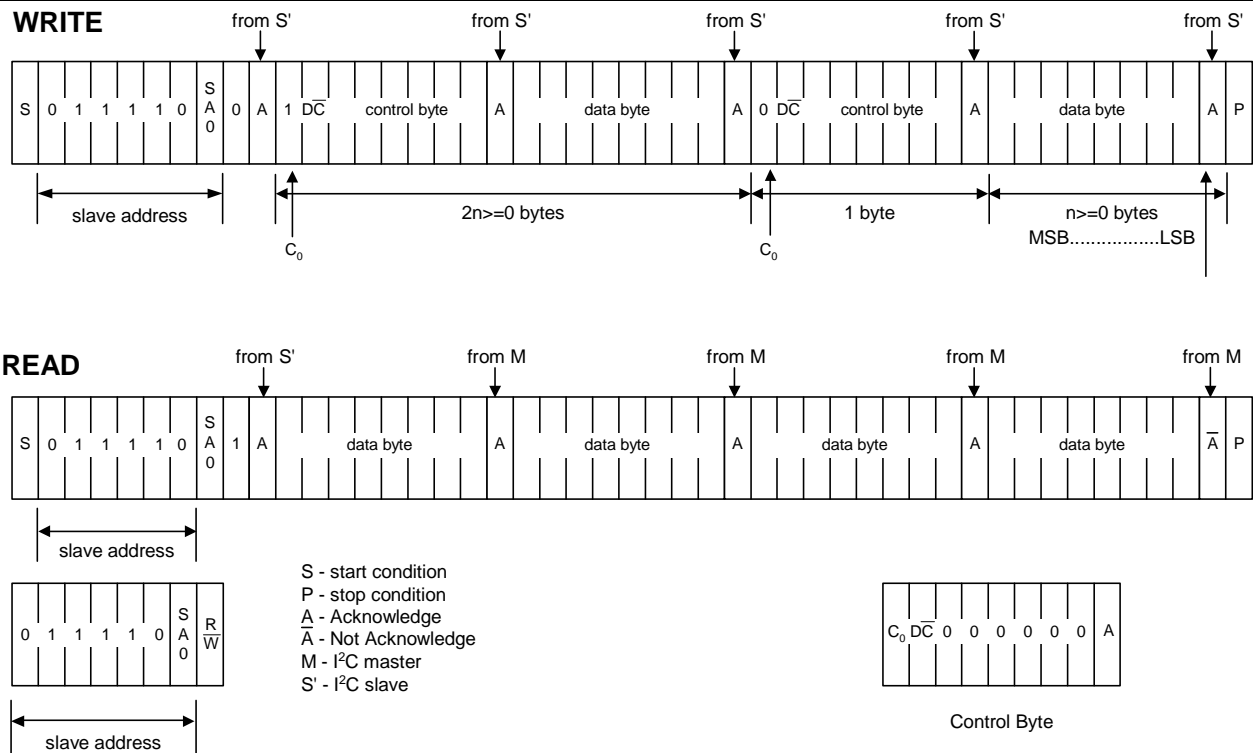
**WRITE**

from S'  from S'  from S'  from S'  from S'

| S | 0 | 1 | 1 | 1 | 1 | 0 | S A 0 | 0 | A | 1 | D$\overline{\text{C}}$ | control byte | A | data byte | A | 0 | D$\overline{\text{C}}$ | control byte | A | data byte | A | P |

slave address   2n>=0 bytes   1 byte   n>=0 bytes MSB.................LSB

$C_0$     $C_0$

**READ**

from S'  from M  from M  from M  from M

| S | 0 | 1 | 1 | 1 | 1 | 0 | S A 0 | 1 | A | data byte | A | data byte | A | data byte | A | data byte | $\overline{\text{A}}$ | P |

slave address

| 0 | 1 | 1 | 1 | 1 | 0 | S A 0 | R $\overline{\text{W}}$ |

slave address

S - start condition
P - stop condition
A - Acknowledge
$\overline{\text{A}}$ - Not Acknowledge
M - I$^2$C master
S' - I$^2$C slave

| $C_0$ | D$\overline{\text{C}}$ | 0 | 0 | 0 | 0 | 0 | 0 | A |

Control Byte

**Figure 9   I$^2$C Protocol**

**Note1：**

1. Co＝ "0"：The last control byte , only data bytes to follow,
   Co＝ "1"：Next two bytes are a data byte and another control byte;

2. D/$\overline{\text{C}}$ ＝ "0"：The data byte is for command operation,
   D/$\overline{\text{C}}$ ＝ "1"：The data byte is for RAM operation.

**Access to Display Data RAM and Internal Registers**

This module determines whether the input data is interpreted as data or command. When A0 = "H", the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = "L", the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

**Display Data RAM**

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 X 128 bits.

For mechanical flexibility, re-mapping on segment and the direction of common outputs can be selected by software.

**The Page Address Circuit**

As shown in Figure 10, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access in page addressing mode and it is incremented (+1) with each display data read/write command in vertical addressing mode.

**The Column Address Circuit**

As shown in Figure 10, the display data RAM column address is specified by the Column Address Set command. The specified column address or page address (it depends on the mode of RAM addressing) is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 7FH to page 1 column 00H in page addressing mode, it is necessary to re-specify both the page address and the column address.

**The Display Address Circuit**

The display address circuit, as shown in Figure 10, specifies the display address relating to the common output when the contents of the display data RAM are displayed. (This is the COM0 output when the common output mode is normal and the COM127 output for SH1107 when the common output mode is reversed. The display area is a 128-line area for the SH1107 from the first display address. As shown in Table 8, the common driver direction select command can be used to reverse the relationship between the display data RAM display address and the common output.

**Table 8**

| Common Output Scan Direction | COM0 | … | COM127 |
|---|---|---|---|
| D= "0" | 0 (H) à | Display Address | à 7F (H) |
| D= "1" | 7F (H) ß | Display Address | ß 0 (H) |

**Figure 10（a）RAM map example: ADC=0(POR)**

| Common output | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D=1 | 7fH | 7eH | 7dH | 7cH | 7bH | 7aH | 79H | 78H | 77H | 76H | 75H | 74H | 73H | 72H | 71H | 70H | ····· | 03H | 02H | 01H | 00H |
| D=0 | 00H | 01H | 02H | 03H | 04H | 05H | 06H | 07H | 08H | 09H | 0aH | 0bH | 0cH | 0dH | 0eH | 0fH | ····· | 7cH | 7dH | 7eH | 7fH |

Display address: 00H 01H 02H 03H 04H 05H 06H 07H 08H 09H 0aH 0bH 0cH 0dH 0eH 0fH ····· 7cH 7dH 7eH 7fH

| Page address | | | | | | Segment output(ADC=1) |
|---|---|---|---|---|---|---|

Page address:
- D3 D2 D1 D0 = 1 1 1 1 → page15
- D3 D2 D1 D0 = 1 1 1 0 → page14
- D3 D2 D1 D0 = 1 1 0 1 → page13
- ⋮
- D3 D2 D1 D0 = 0 0 0 1 → page1
- D3 D2 D1 D0 = 0 0 0 0 → page0

Segment output(ADC=1): Seg0, Seg1, Seg2, Seg3, Seg4, Seg5, Seg6, Seg7, Seg8, Seg9, Seg10, Seg11, Seg12, Seg13, Seg14, Seg15, ⋮, Seg120, Seg121, Seg122, Seg123, Seg124, Seg125, Seg126, Seg127

Column address: Column0 Column1 Column2 Column3 Column4 Column5 Column6 Column7 Column8 Column9 Column10 Column11 Column12 ····· Column125 Column126 Column127

**Figure 10（b）RAM map example: ADC=1(Seg remap)**

**The Oscillator Circuit**

This is a RC type oscillator (Figure 11) that produces the display clock. The oscillator circuit is only enabled when CLS = "H".

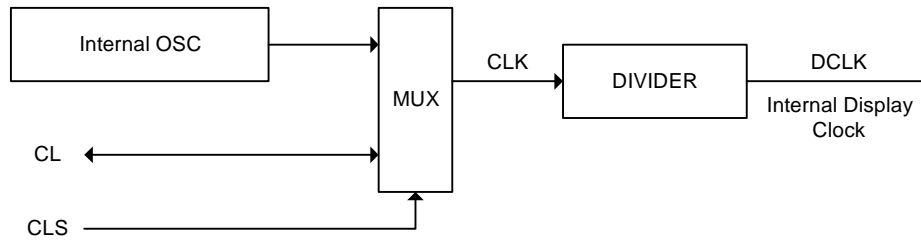When CLS = "L", the oscillation stops and the display clock is inputted through the CL terminal.



**Figure 11**

**DC-DC Voltage Converter**

It is a switching voltage generator circuit, designed for hand held applications. In SH1107, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure 12) can generate a high voltage supply VPP from a low voltage supply input AVDD. VPP is the voltage supply to the OLED driver block
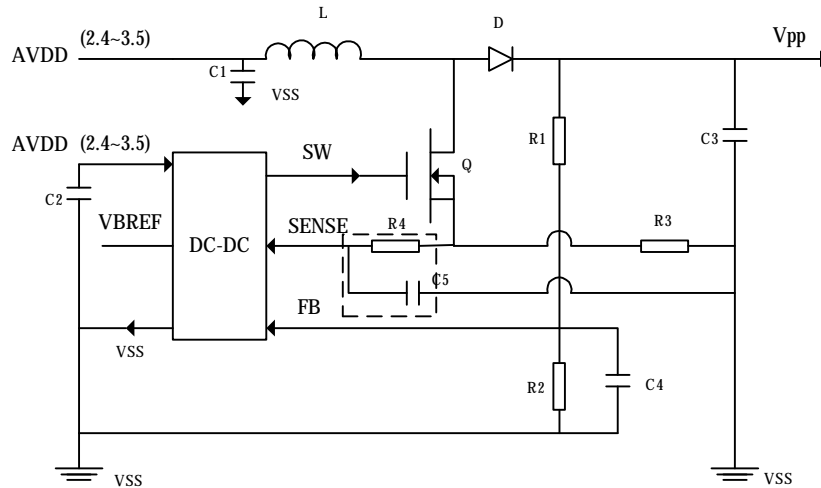


**Figure 12**

$$V_{PP} = (1 + \frac{R1}{R2}) \times V_{BREF}, (R2: 80 - 120k\Omega)$$

**Note:** R4&C5 are optional; they can increase the efficiency of inductance

**Current Control and Voltage Control**

This block is used to derive the incoming power sources into different levels of internal use voltage and current. VPP and VDD are external power supplies. IREF is a reference current source for segment current drivers, it can change the brightness of the screen and the value depends on the resistance of $R_{ref}$ and Vpp:

When Vpp=15V, contrast = 0xff, the value of resistor $R_{ref}$ can be found as Table 9:

**Table 9**

| IREF | 15.625µA | 11.25µA | 6.25µA |
|---|---|---|---|
| $I_{seg}$(Max) | 500µA | 360µA | 200µA |
| $R_{ref}$ | 750 KΩ | 1MΩ | 1.8MΩ |

**Common Drivers/Segment Drivers**

Segment drivers deliver 128 current sources to drive OLED panel. The driving current can be adjusted up to 500µA with 256 steps. Common drivers generate voltage scanning pulses.

**Reset Circuit**

When the $\overline{\text{RES}}$ input falls to "L", these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.

2. 128 X 128 Display mode.

3. Normal segment and display data mapping (SEG0 is mapped to the top line of the display).

4. Shift register data clear in serial interface.

5. Column address counter is set at 0.

6. Contrast control register is set at 80H.

7. Normal common scan direction

8. Internal DC-DC is selected.

**Commands**

The SH1107 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ ( R / $\overline{W}$ ) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R / $\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below. When the serial interface is selected, input data starting from D7 in sequence.

**Command Set**

**1. Set Lower Column Address: (00H - 0FH)**

**2. Set Higher Column Address: (10H - 17H)**

Specify column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 127 is accessed (In page addressing mode).The page address is not changed during this time.

|  | A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| High bits | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | A6 | A5 | A4 |
| Low bits | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A3 | A2 | A1 | A0 |

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | Display address |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0(POR) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | | | : | | | | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

**Note:** Don't use any commands not mentioned above.

**3. Set Memory addressing mode (20H - 21H)**

There are two different memory addressing modes in SH1107: page addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes, "COL" means column.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ (R / $\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | D |

n    Page addressing mode (20H) (POR)

In page addressing mode, after the display RAM is read/ written, the column address is increased automatically by 1. If the column address reaches column end address, the column address is reset to column start address and page address is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the page and column address for page addressing mode is shown in Figure 13-1 and Figure 13-2.
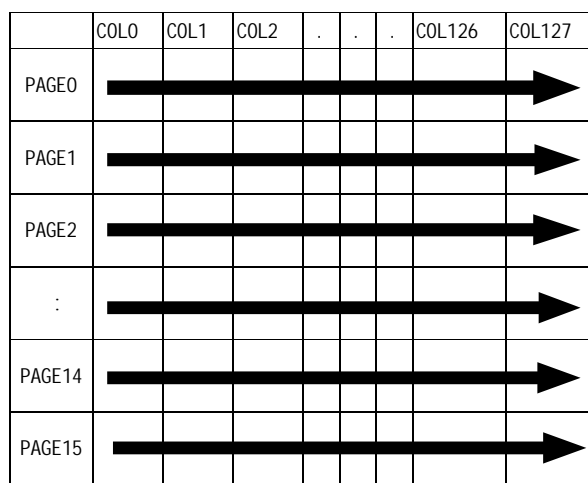


Figure13-1(a)
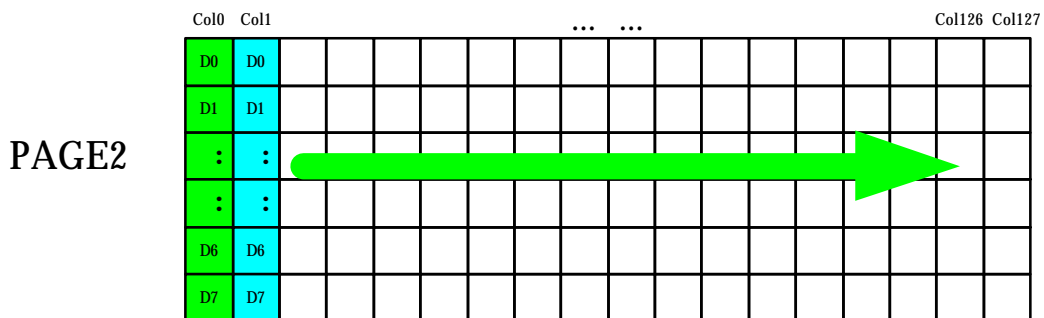


Figure13-1(b)
Figure13-1 page addressing mode (Seg remap=0)

|  | COL0 | COL1 | COL2 | . | . | . | COL126 | COL127 |
|---|---|---|---|---|---|---|---|---|
| **PAGE15** | | | | | | | | → |
| **PAGE14** | | | | | | | | → |
| **PAGE13** | | | | | | | | → |
| **:** | | | | | | | | → |
| **PAGE1** | | | | | | | | → |
| **PAGE0** | | | | | | | | → |

Figure13-2(a)

PAGE2

Figure13-2(b)

Figure13-2 page addressing mode (Seg remap=1)

**n**    Vertical addressing mode: (21H)

In vertical addressing mode, after the display RAM is read/ written, the page address is increased automatically by 1. If the page address reaches the page end address, the page address is reset to page start address and column address is not changed. Users have to set the new page and column addresses in order to access the next column. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the page and column address for vertical addressing mode is shown in Figure 13-3 and Figure 13-4.
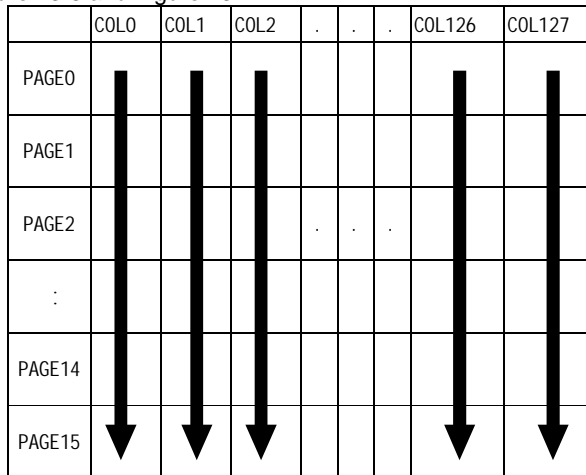


Figure 13-3 (a)
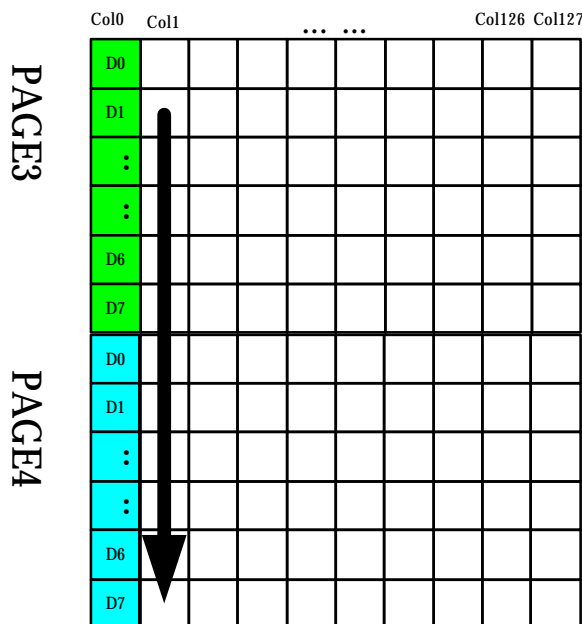


Figure13-3 (b)
Figure 13-3 Vertical addressing mode (Seg remap=0)

| | COL0 | COL1 | COL2 | . | . | . | COL126 | COL127 |
|---|---|---|---|---|---|---|---|---|
| PAGE15 | | | | | | | | |
| PAGE14 | | | | | | | | |
| PAGE13 | | | | . | . | . | | |
| : | | | | | | | | |
| PAGE1 | | | | | | | | |
| PAGE0 | | | | | | | | |
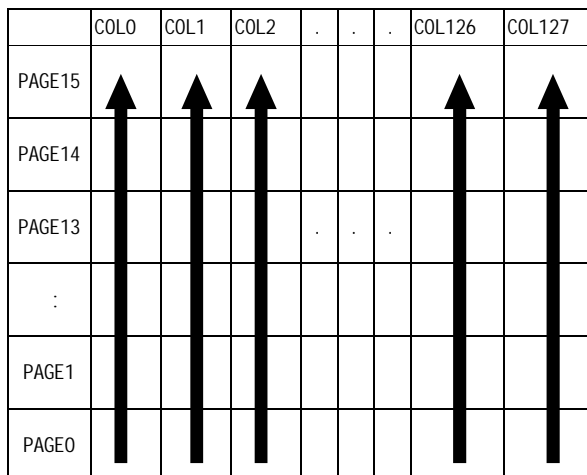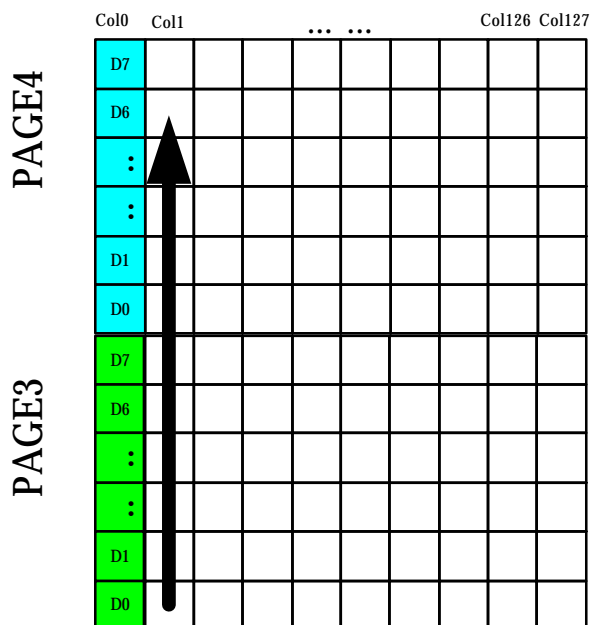
Figure13-4 (a)

Figure13-4 (b)
13-4 Vertical addressing mode (Seg remap=1)

**4. Set Contrast Control Register: (Double Bytes Command)**

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: ISEG = $\alpha$/256 X IREF X scale factor

Where: $\alpha$ is contrast step; IREF is reference current equals 15.625µA; Scale factor = 32

**n** The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**n** Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

| A0 | $\dfrac{E}{(\overline{RD})}$ | $\dfrac{R / \overline{W}}{(\overline{WR})}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | I<sub>SEG</sub> |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Small |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | POR |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Large |

**5. Set Segment Re-map: (A0H - A1H)**

Change the relationship between RAM page address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the page address section of Figure 10. When display data is written or read, the column address or page address (depends on the memory addressing mode) is incremented by 1 as shown in Figure 2.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC |

When ADC = "L", the down rotates (normal direction). (POR)

When ADC = "H", the up rotates (reverse direction).

The display examples of Segment Re-map command are showed in Figure 14



Image        Display (normal scan direction)        Display (reverse scan direction)

**(a) ADC=0**



Image        Display (normal scan direction)        Display (reverse scan direction)

**(b) ADC=1(segment remap)**
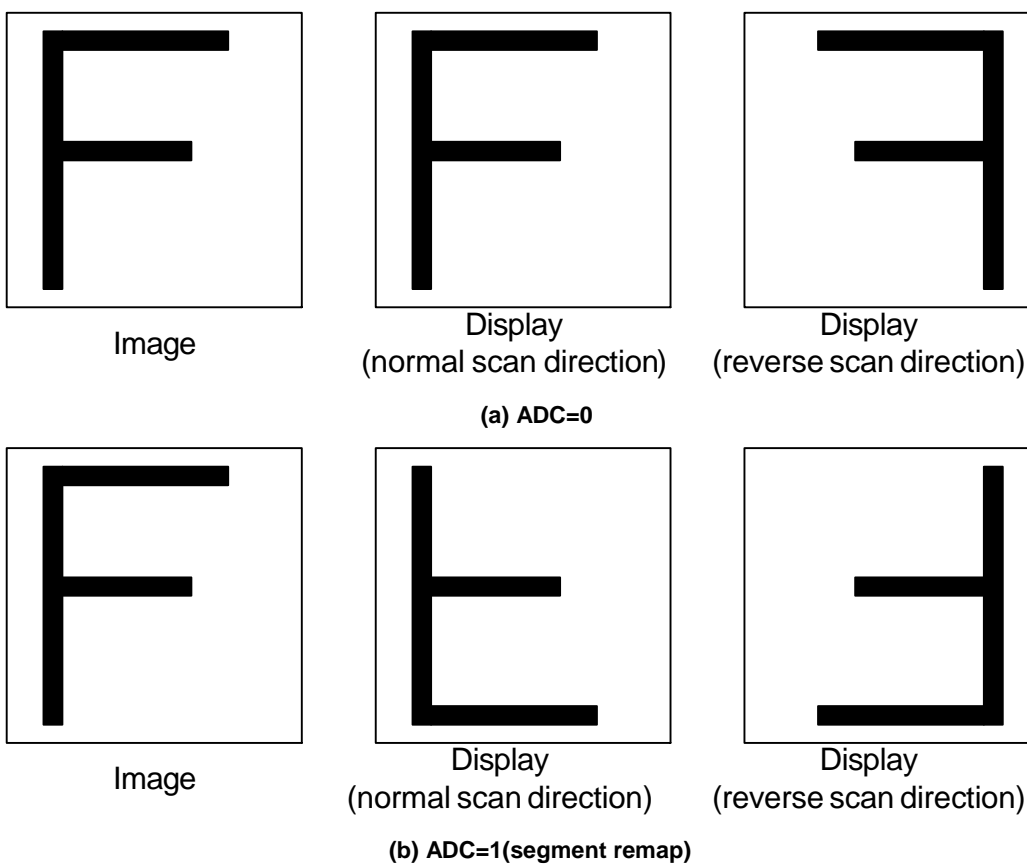
**Figure 14 the display example of Set Segment Re-map and common scan direction command**

**6. Set Multiplex Ration: (Double Bytes Command)**

This command switches default 128 multiplex modes to any multiplex ratio from 1 to 128. The output pads COM0-COM127 will be switched to corresponding common signal.

n Multiplex Ration Mode Set: (A8H)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

n Multiplex Ration Data Set: (00H - 7FH)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Multiplex Ratio |
|----|------|------|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | * | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | * | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | * | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 127 |
| 0 | 1 | 0 | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128 (POR) |

**7. Set Entire Display OFF/ON: (A4H - A5H)**

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D |

When D = "L", the normal display status is provided. (POR)

When D = "H", the entire display ON status is provided.

**8. Set Normal/Reverse Display: (A6H -A7H)**

Reverse the display ON/OFF status without rewriting the contents of the display data RAM.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R $/\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|----------|----|----|----|----|----|----|----|----|
| 0  | 1    | 0        | 1  | 0  | 1  | 0  | 0  | 1  | 1  | D  |

When D = "L", the RAM data is high, being OLED ON potential (normal display). (POR)

When D = "H", the RAM data is low, being OLED ON potential (reverse display)

The display example of Entire display off/on and normal/reverse command are showed in Figure 15



(a)Image

(b) Display off (0xAE)    (c) Entire display on (0xA5)    (d) Normal display (0xA6)    (e) Reverse display (0xA7)
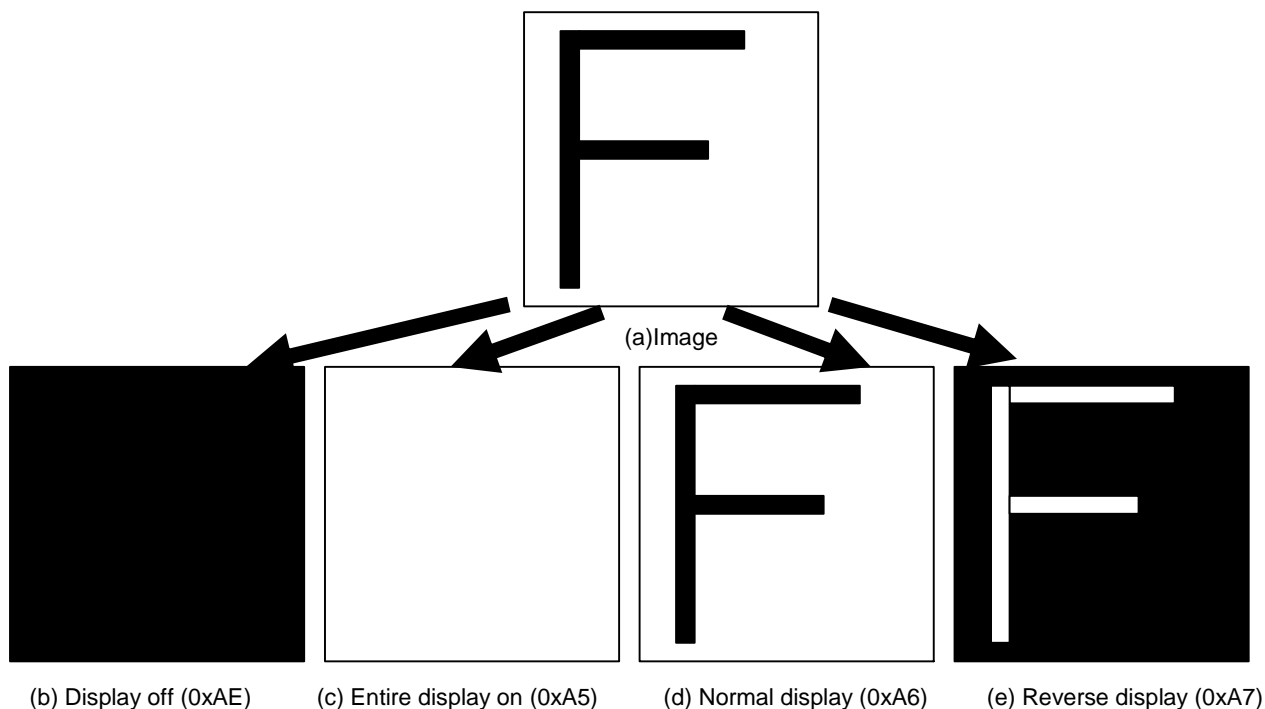
**Figure 15: display example of entire display on and normal/reverse**

**9. Set Display Offset: (Double Bytes Command)**

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-127. For example, if COM0 is the display start line, the value is 00H; while if COM16 is the display start line, then the value should be 10H.

Display Offset Mode Set: (D3H)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

**n** Display Offset Data Set: (00H – 7FH)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | COMx |
|----|------|------|----|----|----|----|----|----|----|----|------|
| 0 | 1 | 0 | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 (POR) |
| 0 | 1 | 0 | * | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | * | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | * | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 126 |
| 0 | 1 | 0 | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

**Note:** "*" stands for "Don't care"

**10. Set DC-DC Setting: (Double Bytes Command)**

This command is to control the DC-DC voltage converter status and the switch frequency. Issuing this command then display ON command will turn on the converter. The panel display must be off while issuing this command.

**n** DC-DC Control Mode Set: (ADH)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

**n** DC-DC ON/OFF Mode Set: (8AH - 8BH)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | F2 | F1 | F0 | D |

When D = "L", DC-DC is disable.

When D = "H", DC-DC will be turned on when display on. (POR)

| DC-DC STATUS | DISPLAY ON/OFF STATUS | Description |
|--------------|-----------------------|-------------|
| 0 | 0 | Sleep mode |
| 0 | 1 | External V$_{PP}$ must be used. |
| 1 | 0 | Sleep mode |
| 1 | 1 | Built-in DC-DC is used, Normal Display |

| F2 | F1 | F0 | Switch Frequency |
|----|----|----|------------------|
| 0 | 0 | 0 | 0.6SF (POR) |
| 0 | 0 | 1 | 0.7SF |
| 0 | 1 | 0 | 0.8SF |
| 0 | 1 | 1 | 0.9SF |
| 1 | 0 | 0 | 1.0SF |
| 1 | 0 | 1 | 1.1SF |
| 1 | 1 | 0 | 1.2SF |
| 1 | 1 | 1 | 1.3SF |

500KHz-25%<SF<500KH**z**+35%

**11. Display OFF/ON: (AEH - AFH)**

Alternatively turns the display on and off.

| A0 | $\overline{RD}$(E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

When D = "L", Display OFF OLED. (POR)

When D = "H", Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1)  Stops the oscillator circuit and DC-DC circuit.

(2)  Stops the OLED drive and outputs Hz as the segment/common driver output.

(3)  Holds the display data and operation mode provided before the start of the sleep mode.

(4)  The MPU can access to the built-in display RAM.

**12. Set Page Address: (B0H - BFH)**

Specify page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

| A0 | $\overline{RD}$(E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | A3 | A2 | A1 | A0 |

| A3 | A2 | A1 | A0 | Page Address |
|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 0(POR) |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| . | . | . | . | . |
| . | . | . | . | . |
| . | . | . | . | . |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |

**Note:** Don't use any commands not mentioned above for user.

**13. Set Common Output Scan Direction: (C0H - C8H)**

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R/$\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | * | * | * |

When D = "L", Scan from COM0 to COM [N -1]. (POR)

When D = "H", Scan from COM [N -1] to COM0.

**14. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)**

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row and oscillator frequency.

n Divide Ratio/Oscillator Frequency Mode Set: (D5H)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

n Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

| A0 | $\dfrac{E}{\overline{RD}}$ | $\dfrac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

A3 - A0 defines the divide ration of the display clocks (DCLK). Divide Ration = A[3:0] +1.

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | Divide Ration |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 (POR) |
|  |  | : |  | : |
| 1 | 1 | 1 | 1 | 16 |

A7 - A4 sets the oscillator frequency. Oscillator frequency increases with the value of A[7:4] and vice versa.

| $A_7$ | $A_6$ | $A_5$ | $A_4$ | Oscillator Frequency of $f$osc |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | -25% |
| 0 | 0 | 0 | 1 | -20% |
| 0 | 0 | 1 | 0 | -15% |
| 0 | 0 | 1 | 1 | -10% |
| 0 | 1 | 0 | 0 | -5% |
| 0 | 1 | 0 | 1 | $f$osc (POR) |
| 0 | 1 | 1 | 0 | +5% |
| 0 | 1 | 1 | 1 | +10% |
| 1 | 0 | 0 | 0 | +15% |
| 1 | 0 | 0 | 1 | +20% |
| 1 | 0 | 1 | 0 | +25% |
| 1 | 0 | 1 | 1 | +30% |
| 1 | 1 | 0 | 0 | +35% |
| 1 | 1 | 0 | 1 | +40% |
| 1 | 1 | 1 | 0 | +45% |
| 1 | 1 | 1 | 1 | +50% |

**15. Set Dis-charge/Pre-charge Period: (Double Bytes Command)**

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK.

POR is 2 DCLKs.

n Pre-charge Period Mode Set: (D9H)

| A0 | $\overline{RD}$(E) | $\overline{WR}$(R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

n Dis-charge/Pre-charge Period Data Set: (00H - FFH)

| A0 | $\overline{RD}$(E) | $\overline{WR}$(R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

Pre-charge Period Adjust: (A3 - A0)

| A3 | A2 | A1 | A0 | Pre-charge Period |
|----|----|----|----|----|
| 0 | 0 | 0 | 0 | Note |
| 0 | 0 | 0 | 1 | 1 DCLKs |
| 0 | 0 | 1 | 0 | 2 DCLKs (POR) |
| | | : | | : |
| 1 | 1 | 1 | 0 | 14 DCLKs |
| 1 | 1 | 1 | 1 | 15 DCLKs |

Dis-charge Period Adjust: (A7 - A4)

| A7 | A6 | A5 | A4 | Dis-charge Period |
|----|----|----|----|----|
| 0 | 0 | 0 | 0 | INVALID |
| 0 | 0 | 0 | 1 | 1 DCLKs |
| 0 | 0 | 1 | 0 | 2 DCLKs (POR) |
| | | : | | : |
| 1 | 1 | 1 | 0 | 14 DCLKs |
| 1 | 1 | 1 | 1 | 15 DCLKs |

**Note:**

When set A[3:0] =0, the period for display will increase 2 DCLKs. And there is no pre-charge period so that it will save power consumption.

## 16. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

n  VCOM Deselect Level Mode Set: (DBH)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |

n  VCOM Deselect Level Data Set: (00H - FFH)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

$V_{COMH} = \beta_1 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

| A[7:0] | $\beta_1$ | A[7:0] | $\beta_1$ |
|---|---|---|---|
| 00H | 0.430 | 20H | 0.635 |
| 01H | 0.436 | 21H | 0.642 |
| 02H | 0.442 | 22H | 0.648 |
| 03H | 0.449 | 23H | 0.654 |
| 04H | 0.456 | 24H | 0.661 |
| 05H | 0.462 | 25H | 0.667 |
| 06H | 0.468 | 26H | 0.674 |
| 07H | 0.475 | 27H | 0.680 |
| 08H | 0.481 | 28H | 0.687 |
| 09H | 0.488 | 29H | 0.693 |
| 0AH | 0.494 | 2AH | 0.699 |
| 0BH | 0.501 | 2BH | 0.706 |
| 0CH | 0.507 | 2CH | 0.712 |
| 0DH | 0.513 | 2DH | 0.719 |
| 0EH | 0.520 | 2EH | 0.725 |
| 0FH | 0.526 | 2FH | 0.731 |
| 10H | 0.533 | 30H | 0.738 |
| 11H | 0.539 | 31H | 0.744 |
| 12H | 0.525 | 32H | 0.751 |
| 13H | 0.552 | 33H | 0.757 |
| 14H | 0.558 | 34H | 0.764 |
| 15H | 0.565 | 35H | 0.770 (POR) |
| 16H | 0.571 | 36H | 0.776 |
| 17H | 0.578 | 37H | 0.783 |
| 18H | 0.584 | 38H | 0.789 |
| 19H | 0.590 | 39H | 0.796 |
| 1AH | 0.596 | 3AH | 0.802 |
| 1BH | 0.603 | 3BH | 0.808 |
| 1CH | 0.610 | 3CH | 0.815 |
| 1DH | 0.616 | 3DH | 0.821 |
| 1EH | 0.622 | 3EH | 0.828 |
| 1FH | 0.629 | 3FH | 0.834 |
| 40H - FFH | 1 | | |

## 15.—16. Blank

**17. Set Display Start Line:（Double Bytes Command）**

Specify Column address to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the Column address, the smooth scrolling or page change takes place.

**n** The Display Start line Mode Set: (DCH)

| A0 | $\overline{RD}$(E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|----|----|----|----|----|----|----|
| 0  | 1    | 0    | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 0  |

**n** The Display Start line Register Set: (00H – 7FH)

| A0 | $\overline{RD}$(E) | $\overline{WR}$ (R/$\overline{W}$) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Column address |
|----|------|------|----|----|----|----|----|----|----|----|----------------|
| 0  | 1    | 0    | *  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0(POR) |
| 0  | 1    | 0    | *  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1 |
| 0  | 1    | 0    | *  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2 |
| 0  | 1    | 0    | *  |    |    |    | :  |    |    |    | : |
| 0  | 1    | 0    | *  |    |    |    |    |    |    |    |   |
| 0  | 1    | 0    | *  |    |    |    | :  |    |    |    | : |
| 0  | 1    | 0    | *  | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 7E |
| 0  | 1    | 0    | *  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 7F |

**18. Read-Modify-Write: (E0H)**

A pair of Read-Modify-Write and End commands must always be used. In page addressing mode, once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. In vertical addressing mode, once read-modify-write is issued, page address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address or page address (it depends on the addressing mode) returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

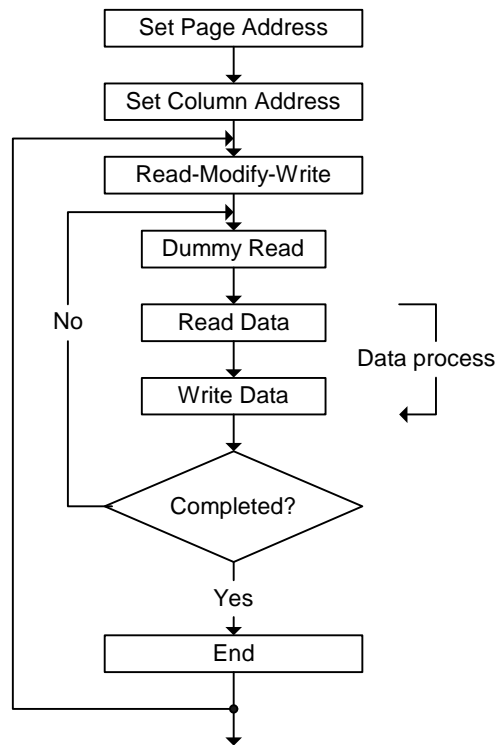| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|-----|-----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Cursor display sequence:



**Figure 16**

**19. End: (EEH)**

Cancel Read-Modify-Write mode and return column address or page address (it depends on the RAM addressing mode) to the original address (when Read-Modify-Write is issued.)

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
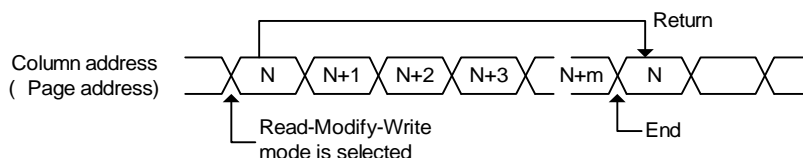


**Figure 17**

**20. NOP: (E3H)**

No Operation Command.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

**21. Write Display Data**

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | Write RAM data |

**22. Read ID**

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | BUSY | ON/OFF | ID |

BUSY:    When high, the SH1107 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF:    Indicates whether the display is on or off. When it goes low, the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command.

ID：    These bits contain the information of the chip. They output bits 000111(it means 07).

**23. Read Display Data**

Read 8-bit data from display RAM area specified by column address and page address. As the column address or page address (depends on the mode of memory addressing) is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

| A0 | $\overline{RD}$ (E) | $\overline{WR}$ ( R / $\overline{W}$ ) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | Read RAM data |

**Command Table**

| Command | A0 | $\overline{RD}$ | $\overline{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1. Set Column Address 4 lower bits | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Lower column address | | | | Sets 4 lower bits of column address of display RAM in register. (POR = 00H) |
| 2. Set Column Address 4 higher bits | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | Higher column address | | | Sets 4 higher bits of column address of display RAM in register. (POR = 10H) |
| 3. Set memory addressing mode | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | D | D = 1, Vertical Addressing Mode<br>D = 0, Page Addressing Mode (POR=20H) |
| 4. The Contrast Control Mode Set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | This command is to set Contrast Setting of the display. |
| Contrast Data Register Set | 0 | 1 | 0 | Contrast Data | | | | | | | | The chip has 256 contrast steps from 00 to FF. (POR = 80H) |
| 5. Set Segment Re-map (ADC) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC | The down (0) or up (1) rotation. (POR = A0H) |
| 6. Set Multiplex Ration | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | This command switches multiplex mode to any multiplex ratio from 1 to 128. (POR = 7FH ) |
| | 0 | 1 | 0 | - | Multiplex Ratio | | | | | | | |
| 7. Set Entire Display OFF/ON | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D | Selects normal display (0) or Entire Display ON (1). (POR = A4H) |
| 8. Set Normal/Reverse Display | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D | Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H) |
| 9. Set display offset | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | This is a double byte command that specifies the mapping of display start line to one of COM0 -127. (POR = 00H) |
| | 0 | 1 | 0 | - | COMx | | | | | | | |
| 10. DC-DC Control Mode Set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 81H) |
| DC-DC Setting Mode Set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | F2 | F1 | F0 | D | |

## Command Table (Continued)

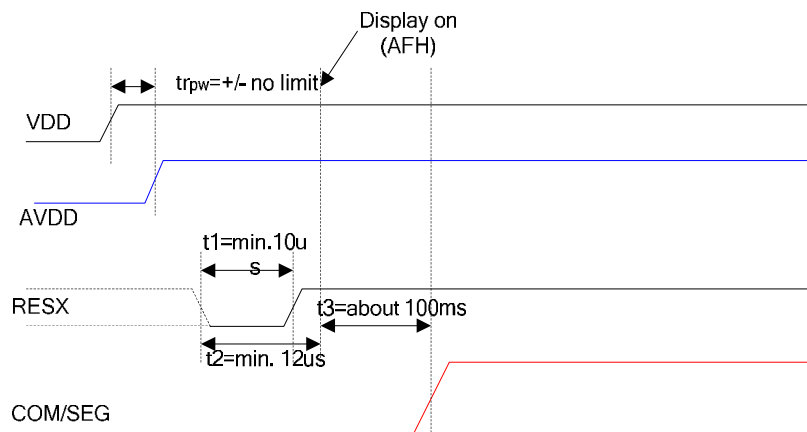| Command | A0 | $\overline{RD}$ | $\overline{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Code | | | | | |
| 11. Display OFF/ON | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D | Turns on OLED panel (1) or turns off (0). (POR = AEH) |
| 12. Set Page Address | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page Address | | | | Specifies page address to load display RAM data to page address register. (POR = B0H) |
| 13 Set Common Output Scan Direction | 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | * | * | * | Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H) |
| 14. Set Display Divide Ratio/Oscillator Frequency Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | This command is used to set the frequency of the internal display clocks. (POR = 50H) |
| Divide Ratio/Oscillator Frequency Data Set | 0 | 1 | 0 | Oscillator Frequency | | | | Divide Ratio | | | | |
| 15. Dis-charge / Pre-charge Period Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H) |
| Dis-charge /Pre-charge Period Data Set | 0 | 1 | 0 | Dis-charge Period | | | | Pre-charge Period | | | | |
| 16. VCOM Deselect Level Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | This command is to set the common pad output voltage level at deselect stage. (POR = 35H) |
| VCOM Deselect Level Data Set | 0 | 1 | 0 | $VCOM = (\beta_1 \times V_{REF})$ | | | | | | | | |
| 17. Set Display Start Line | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Specify RAM display line for COM0. |
| | 0 | 1 | 0 | - | Start line | | | | | | | |
| 18. Read-Modify-Write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Read-Modify-Write start. |
| 19. End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Read-Modify-Write end. |
| 20. NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Non-Operation Command |
| 21 Write Display Data | 1 | 1 | 0 | Write RAM data | | | | | | | | |
| 22 Read ID | 0 | 0 | 1 | BUSY | ON/ OFF | ID | | | | | | |
| 23. Read Display Data | 1 | 0 | 1 | Read RAM data | | | | | | | | |

**Note:** Do not use any other command, or the system malfunction may result.

**1. Power On/Off and Initialization**

**1.1. Built-in DC-DC pump power is being used immediately after turning on the power:**

```
┌─────────────────────────┐
│  VDD is off             │
│  AVDD is off            │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────────────────┐
│ Turn on the VDD and AVDD power,     │
│ keep the  RES pin="L"(>10us)        │
└─────────────────────────────────────┘
            │
            ▼
┌─────────────────────────────────────┐
│ Release the reset state (RES pin="H")│
│ Reset timing depends on SH1107 data sheet│
└─────────────────────────────────────┘
            │
            ▼
┌─────────────────────────────────────┐
│ Initialized state(Default)          │
└─────────────────────────────────────┘
            │
            ▼
┌─────────────────────────────────────┐
│ Set up initial code (user setup)    │
└─────────────────────────────────────┘
            │
            ▼
┌─────────────────────────────────────┐
│ Clear internal RAM to "00H"         │
└─────────────────────────────────────┘
            │
            ▼
┌─────────────────────────────────────┐
│ Set display on: AFH                 │
└─────────────────────────────────────┘
            │ Wait 100ms
            ▼
┌─────────────────────────────────────┐
│ Send display data                   │
└─────────────────────────────────────┘
```

Power on sequence：

Display on (AFH)

tr$_{pw}$=+/- no limit

VDD

AVDD

t1=min.10us

RESX

t3=about 100ms

t2=min. 12us

COM/SEG

**1.2. External power is being used immediately after turning on the power:**

```
        ┌──────────────────────────────┐
        │   VDD is off                 │
        │   External power VPP is off  │
        └──────────────┬───────────────┘
                       │
        ┌──────────────▼───────────────┐
        │ Turn on the VDD1 and VPP power,│
        │ keep the  RES pin="L"(>10us)  │
        └──────────────┬───────────────┘
                       │
        ┌──────────────▼───────────────┐
        │ Release the reset state (RES pin="H" )│
        │ Reset timing depends on SH1107 data sheet│
        └──────────────┬───────────────┘
                       │
        ┌──────────────▼───────────────┐
        │   Initialized state(Default)  │
        └──────────────┬───────────────┘
                       │
        ┌──────────────▼───────────────┐
        │  Set up initial code (user setup)│
        └──────────────┬───────────────┘
                       │
        ┌──────────────▼───────────────┐
        │   Clear internal RAM to "00H" │
        └──────────────┬───────────────┘
                       │
        ┌──────────────▼───────────────┐
        │     Set display on: AFH       │
        └──────────────┬───────────────┘
                       │ Wait 100ms
        ┌──────────────▼───────────────┐
        │     Send display data         │
        └──────────────────────────────┘
```
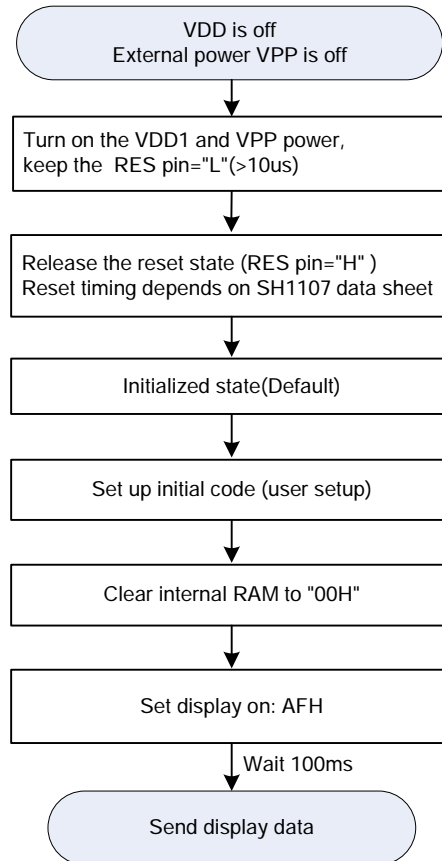
**Power on sequence：**

### 1.3  Power Off

```
┌─────────────────────────────────────────┐
│              Optional status             │
└─────────────────────────────────────────┘
                    │
                    ▼
┌─────────────────────────────────────────┐
│           Set Display OFF: AEH           │
└─────────────────────────────────────────┘
                    │
                    ▼
┌─────────────────────────────────────────┐
│       Turn off the AVDD or VPP power     │
└─────────────────────────────────────────┘
                    │  Wait 100 ms
                    ▼
┌─────────────────────────────────────────┐
│            Turn off VDD power            │
└─────────────────────────────────────────┘
```
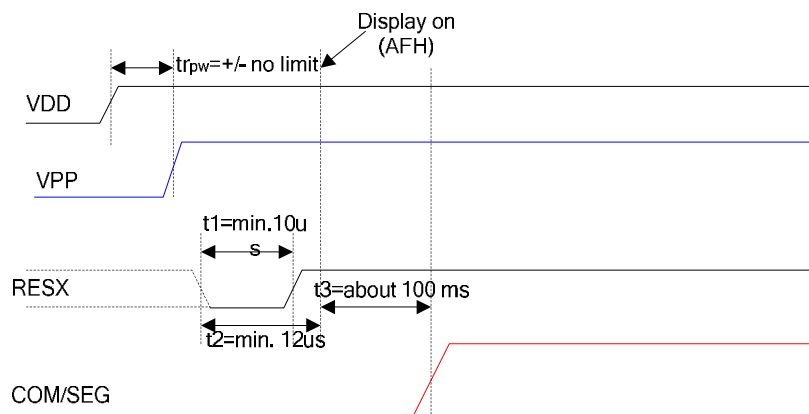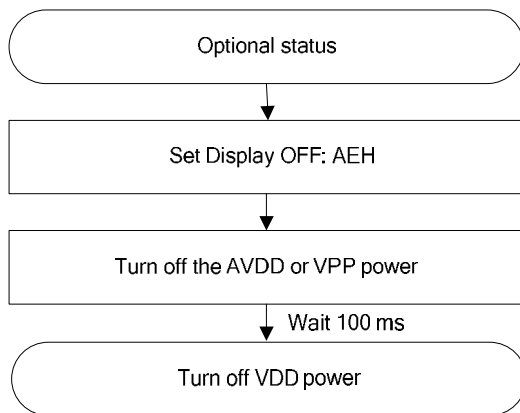
Power off sequence：
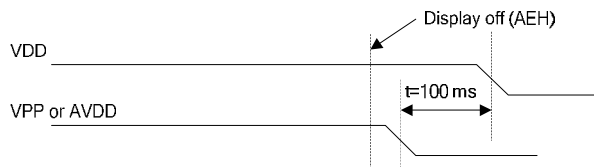


Note：There will be no damages to the display module if the power sequences are not met.

**Absolute Maximum Rating***

DC Supply Voltage (V$_{DD}$) . . . . . . . . . . .... . -0.3V to +3.6V

DC Supply Voltage (V$_{PP}$) . . . . . . . . . . . . . . . -0.3V to +17V

Input Voltage . . . . . . . . . .. . . . . . . . . . -0.3V to V$_{DD}$ + 0.3V

Operating Ambient Temperature . . . . . . . . . -40°C to +85°C

Storage Temperature . . . . . . . . . .. . . . . . . . -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

**DC Characteristics (VSS = 0V, VDD = 1.65 - 3.5V AVDD=2.4-3.5V, TA =+25°C, unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| V$_{DD}$ | Operating voltage | 1.65 | - | 3.5 | V | |
| AV$_{DD}$ | DC-DC voltage | 2.4 | 3.0 | 3.5 | V | |
| V$_{PP}$ | OLED Operating voltage | 7 | 15 | 16.5 | V | |
| V$_{BREF}$ | Internal voltage reference | 1.15 | 1.20 | 1.25 | V | |
| I$_{DD1}$ | Dynamic current consumption 1(in V$_{DD}$) | - | 110 | 160 | μA | V$_{DD}$ = 3V, AV$_{DD}$=3V, I$_{REF}$ = -15.625μA, Contrast $\alpha$ = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached. |
| I$_{DD2}$ | Dynamic current consumption 2 (in AVDD) | - | 190 | 285 | μA | V$_{DD}$=3V, AV$_{DD}$=3V, I$_{REF}$ = -15.625μA, Contrast $\alpha$ = 256, Bulid-in DC-DC ON, VPP=15V, Display ON, display data = All ON, No panel attached. |
| I$_{PP}$ | OLED dynamic current consumption | - | 1 | 1.27 | mA | V$_{DD}$ = 3V, AV$_{DD}$ =3V ,V$_{PP}$ = 15V, IREF = -15.625μA, Contrast $\alpha$ = 256, Display ON, Display data = All ON, No panel attached |
| I$_{SP}$ | Sleep mode current consumption in V$_{DD}$ & AVDD | - | 0.01 | 5 | μA | During sleep, T$_A$ = +25°C, V$_{DD}$ = 3V,AV$_{DD}$=3V |
| | Sleep mode current consumption in V$_{PP}$ | - | 0.01 | 5 | μA | During sleep, T$_A$ = +25°C, V$_{PP}$ = 15V (External ) |
| I$_{SEG}$ | Segment output current | - | -500 | - | μA | V$_{DD}$ = 3V, V$_{PP}$ = 15V, I$_{REF}$ = -15.625μA, R$_{LOAD}$ = 20kΩ, Display ON. Contrast $\alpha$ = 256. |
| | | - | -343.75 | - | μA | V$_{DD}$ = 3V, V$_{PP}$ = 15V, I$_{REF}$ = -15.625μA, R$_{LOAD}$ = 20kΩ, Display ON. Contrast $\alpha$ = 176. |
| | | - | -187.5 | - | μA | V$_{DD}$ = 3V, V$_{PP}$ = 15V, I$_{REF}$ = -15.625μA, R$_{LOAD}$ = 20kΩ, Display ON. Contrast $\alpha$ = 96. |
| | | - | -31.25 | - | μA | V$_{DD}$ = 3V, V$_{PP}$ = 15V, I$_{REF}$ = -15.625μA, R$_{LOAD}$ = 20kΩ, Display ON. Contrast $\alpha$ = 16 |
| $\Delta$I$_{SEG1}$ | Segment output current uniformity | - | - | ±3 | % | $\Delta$I$_{SEG1}$ = (I$_{SEG}$ - I$_{MID}$)/I$_{MID}$ X 100% I$_{MID}$ = (I$_{MAX}$ + I$_{MIN}$)/2 I$_{SEG}$ [0:131] at contrast $\alpha$ = 256. |
| $\Delta$I$_{SEG2}$ | Adjacent segment output current uniformity | - | - | ±2 | % | $\Delta$I$_{SEG2}$ = (I$_{SEG}$ [N] - I$_{SEG}$ [N+1])/(I$_{SEG}$ [N] + I$_{SEG}$ [N+1]) X 100% I$_{SEG}$ [0:131] at contrast $\alpha$ = 256. |

**DC Characteristics (Continued)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| V$_{IHC}$ | High-level input voltage | 0.8 X V$_{DD}$ | - | V$_{DD}$ | V | A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ ( R / $\overline{W}$ ), $\overline{CS}$, CLS, CL, IM0~2 and $\overline{RES}$. | |
| V$_{ILC}$ | Low-level input voltage | V$_{SS}$ | - | 0.2 X V$_{DD}$ | V | | |
| V$_{OHC}$ | High-level output voltage | 0.8 X V$_{DD}$ | - | V$_{DD}$ | V | I$_{OH}$ = -0.5mA (D0 - D7, and CL). | |
| V$_{OLC}$ | Low -level output voltage | V$_{SS}$ | - | 0.2 X V$_{DD}$ | V | I$_{OL}$ = 0.5mA (D0, D2 - D7, and CL) | |
| V$_{OLCS}$ | SDA low -level output voltage | V$_{SS}$ | - | 0.2 X V$_{DD}$ | V | VDD<2V | I$_{OL}$=2mA (SDA) |
| | | | | 0.4 | | VDD>2V | I$_{OL}$=3mA (SDA) |
| I$_{LI}$ | Input leakage current | -1.0 | - | 1.0 | μA | V$_{IN}$ = V$_{DD}$ or V$_{SS}$ (A0, $\overline{RD}$ (E), $\overline{WR}$ ( R / $\overline{W}$ ), $\overline{CS}$, CLS, IM0~2 and $\overline{RES}$ ). | |
| I$_{Hz}$ | Hz leakage current | -1.0 | - | 1.0 | μA | When the D0 - D7, and CL are in high impedance. | |
| f$_{OSC}$ | Oscillation frequency | - | 720 | - | kHz | T$_A$ = +25°C.VDD=3V | |
| f$_{FRM}$ | Frame frequency for 128 Commons | - | 104 | - | Hz | When f$_{OSC}$ = 720kHz, Divide ratio = 1, common width = 54 DCLKs. | |
| R$_{ON1}$ | Common switch resistance | - | 15 | - | Ω | V$_{pp}$=15V,V$_{com}$=V$_{ss}$+0.4V | |
| R$_{ON2}$ | Common switch resistance | - | 500 | - | Ω | V$_{pp}$=15V,V$_{COM}$=0.770×V$_{pp}$-0.4V | |

**AC Characteristics**

**(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)**
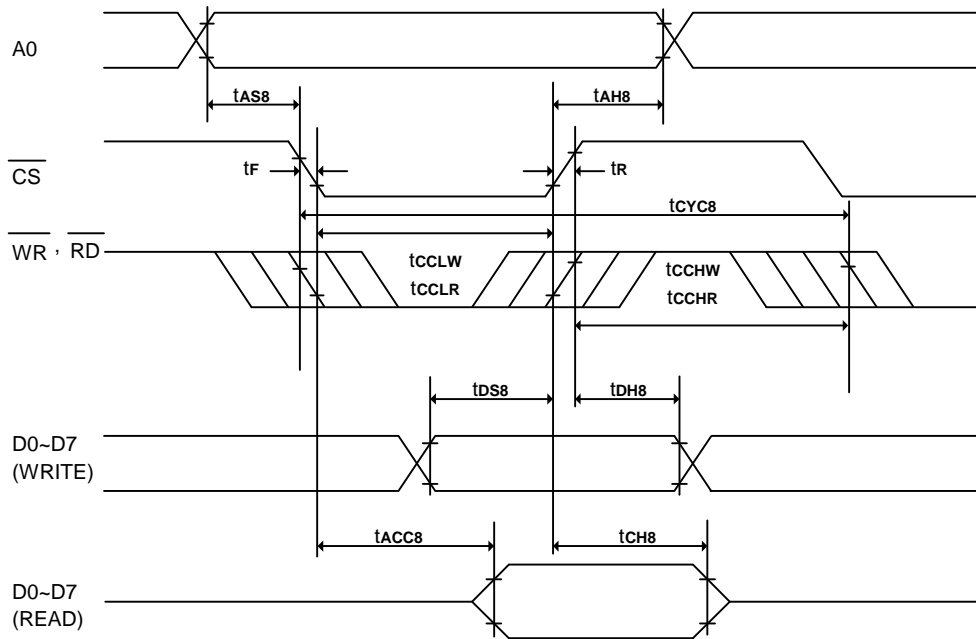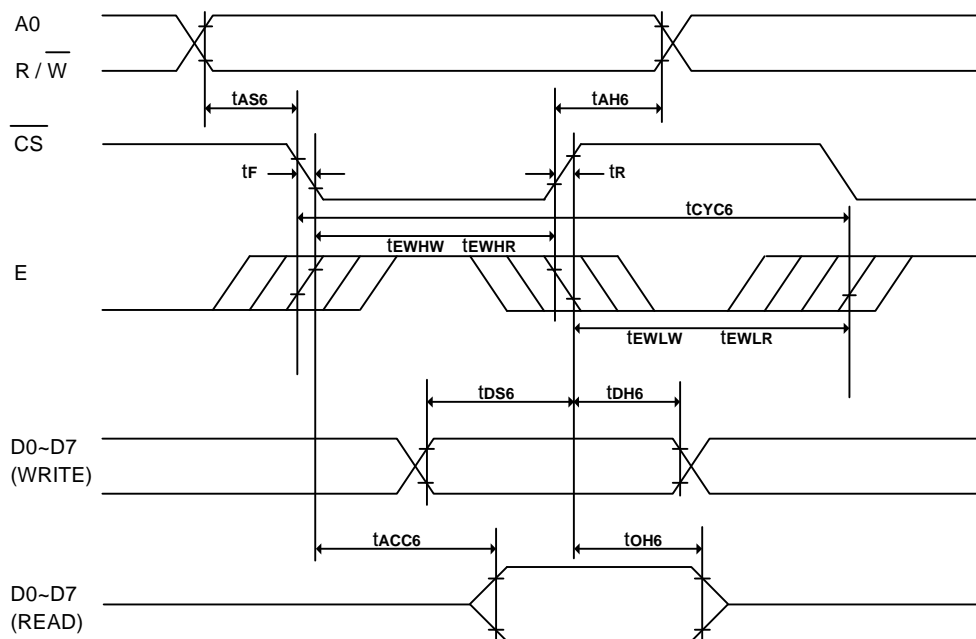


$(V_{DD} = 1.65V - 2.4V, T_A = +25°C)$

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------|------|------|------|------|-----------|
| t$_{CYC8}$ | System cycle time | 300 | - | - | ns | |
| t$_{AS8}$ | Address setup time | 0 | - | - | ns | |
| t$_{AH8}$ | Address hold time | 0 | - | - | ns | |
| t$_{DS8}$ | Data setup time | 40 | - | - | ns | |
| t$_{DH8}$ | Data hold time | 30 | - | - | ns | |
| t$_{CH8}$ | Output disable time | 10 | - | 70 | ns | C$_L$ = 100pF |
| t$_{ACC8}$ | $\overline{RD}$ access time | - | - | 280 | ns | C$_L$ = 100pF |
| t$_{CCLW}$ | Control L pulse width (WR) | 100 | - | - | ns | |
| t$_{CCLR}$ | Control L pulse width (RD) | 120 | - | - | ns | |
| t$_{CCHW}$ | Control H pulse width (WR) | 100 | - | - | ns | |
| t$_{CCHR}$ | Control H pulse width (RD) | 100 | - | - | ns | |
| t$_R$ | Rise time | - | - | 15 | ns | |
| t$_F$ | Fall time | - | - | 15 | ns | |

($V_{DD}$ = 2.4V – 3.5V, $T_A$ = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------|------|------|------|------|-----------|
| $t_{CYC8}$ | System cycle time | 300 | - | - | ns | |
| $t_{AS8}$ | Address setup time | 0 | - | - | ns | |
| $t_{AH8}$ | Address hold time | 0 | - | - | ns | |
| $t_{DS8}$ | Data setup time | 40 | - | - | ns | |
| $t_{DH8}$ | Data hold time | 15 | - | - | ns | |
| $t_{CH8}$ | Output disable time | 10 | - | 70 | ns | $C_L$ = 100pF |
| $t_{ACC8}$ | $\overline{RD}$ access time | - | - | 140 | ns | $C_L$ = 100pF |
| $t_{CCLW}$ | Control L pulse width (WR) | 100 | - | - | ns | |
| $t_{CCLR}$ | Control L pulse width (RD) | 120 | - | - | ns | |
| $t_{CCHW}$ | Control H pulse width (WR) | 100 | - | - | ns | |
| $t_{CCHR}$ | Control H pulse width (RD) | 100 | - | - | ns | |
| $t_R$ | Rise time | - | - | 15 | ns | |
| $t_F$ | Fall time | - | - | 15 | ns | |

**(2)  System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)**



(V$_{DD}$ = 1.65 – 2.4V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------|------|------|------|------|-----------|
| tCYC6 | System cycle time | 300 | - | - | ns | |
| tAS6 | Address setup time | 0 | - | - | ns | |
| tAH6 | Address hold time | 0 | - | - | ns | |
| tDS6 | Data setup time | 40 | - | - | ns | |
| tDH6 | Data hold time | 30 | - | - | ns | |
| tOH6 | Output disable time | 10 | - | 70 | ns | C$_L$ = 100pF |
| tACC6 | Access time | - | - | 280 | ns | C$_L$ = 100pF |
| tEWHW | Enable H pulse width (Write) | 100 | - | - | ns | |
| tEWHR | Enable H pulse width (Read) | 120 | - | - | ns | |
| tEWLW | Enable L pulse width (Write) | 100 | - | - | ns | |
| tEWLR | Enable L pulse width (Read) | 100 | - | - | ns | |
| tR | Rise time | - | - | 15 | ns | |
| tF | Fall time | - | - | 15 | ns | |

(V<sub>DD</sub> = 2.4 – 3.5V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------|------|------|------|------|-----------|
| tCYC6 | System cycle time | 300 | - | - | ns | |
| tAS6 | Address setup time | 0 | - | - | ns | |
| tAH6 | Address hold time | 0 | - | - | ns | |
| tDS6 | Data setup time | 40 | - | - | ns | |
| tDH6 | Data hold time | 15 | - | - | ns | |
| tOH6 | Output disable time | 10 | - | 70 | ns | C<sub>L</sub> = 100pF |
| tACC6 | Access time | - | - | 140 | ns | C<sub>L</sub> = 100pF |
| tEWHW | Enable H pulse width (Write) | 100 | - | - | ns | |
| tEWHR | Enable H pulse width (Read) | 120 | - | - | ns | |
| tEWLW | Enable L pulse width (Write) | 100 | - | - | ns | |
| tEWLR | Enable L pulse width (Read) | 100 | - | - | ns | |
| tR | Rise time | - | - | 15 | ns | |
| tF | Fall time | - | - | 15 | ns | |

**(3) System buses Write characteristics 3 (For 4 wire SPI)**
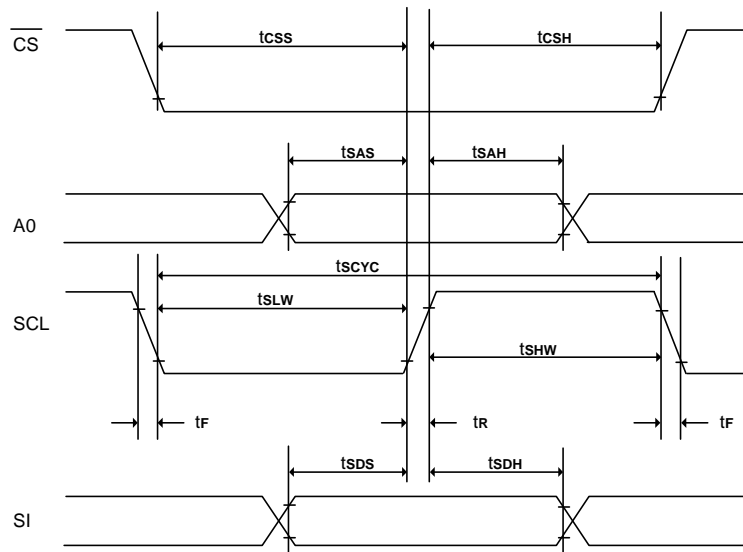


(V$_{DD1}$ = 1.65 – 2.4V, T$_A$ = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| t$_{SCYC}$ | Serial clock cycle | 500 | - | - | ns | |
| t$_{SAS}$ | Address setup time | 300 | - | - | ns | |
| t$_{SAH}$ | Address hold time | 300 | - | - | ns | |
| t$_{SDS}$ | Data setup time | 200 | - | - | ns | |
| t$_{SDH}$ | Data hold time | 200 | - | - | ns | |
| t$_{CSS}$ | $\overline{CS}$ setup time | 240 | - | - | ns | |
| t$_{CSH}$ | $\overline{CS}$ hold time time | 120 | - | - | ns | |
| t$_{SHW}$ | Serial clock H pulse width | 200 | - | - | ns | |
| t$_{SLW}$ | Serial clock L pulse width | 200 | - | - | ns | |
| t$_R$ | Rise time | - | - | 30 | ns | |
| t$_F$ | Fall time | - | - | 30 | ns | |

(V$_{DD1}$ = 2.4 - 3.5V, T$_A$ = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| t$_{SCYC}$ | Serial clock cycle | 250 | - | - | ns | |
| t$_{SAS}$ | Address setup time | 150 | - | - | ns | |
| t$_{SAH}$ | Address hold time | 150 | - | - | ns | |
| t$_{SDS}$ | Data setup time | 100 | - | - | ns | |
| t$_{SDH}$ | Data hold time | 100 | - | - | ns | |
| t$_{CSS}$ | $\overline{CS}$ setup time | 120 | - | - | ns | |
| t$_{CSH}$ | $\overline{CS}$ hold time time | 60 | - | - | ns | |
| t$_{SHW}$ | Serial clock H pulse width | 100 | - | - | ns | |
| t$_{SLW}$ | Serial clock L pulse width | 100 | - | - | ns | |
| t$_R$ | Rise time | - | - | 15 | ns | |
| t$_F$ | Fall time | - | - | 15 | ns | |

**(4) System buses Write characteristics 4(For 3 wire SPI)**
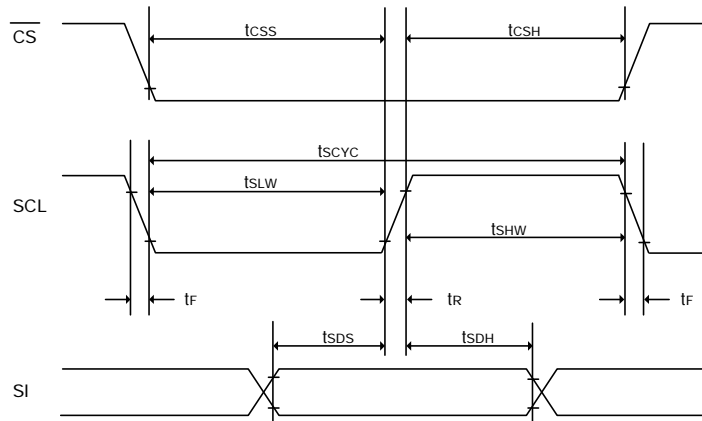


(V$_{DD1}$ = 1.65 – 2.4V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| t$_{SCYC}$ | Serial clock cycle | 500 | - | - | ns | |
| t$_{SDS}$ | Data setup time | 200 | - | - | ns | |
| t$_{SDH}$ | Data hold time | 200 | - | - | ns | |
| t$_{CSS}$ | $\overline{CS}$ setup time | 240 | - | - | ns | |
| t$_{CSH}$ | $\overline{CS}$ hold time time | 120 | - | - | ns | |
| t$_{SHW}$ | Serial clock H pulse width | 200 | - | - | ns | |
| t$_{SLW}$ | Serial clock L pulse width | 200 | - | - | ns | |
| t$_R$ | Rise time | - | - | 30 | ns | |
| t$_F$ | Fall time | - | - | 30 | ns | |

(V$_{DD1}$ = 2.4 - 3.5V, T$_A$ = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| t$_{SCYC}$ | Serial clock cycle | 250 | - | - | ns | |
| t$_{SDS}$ | Data setup time | 100 | - | - | ns | |
| t$_{SDH}$ | Data hold time | 100 | - | - | ns | |
| t$_{CSS}$ | $\overline{CS}$ setup time | 120 | - | - | ns | |
| t$_{CSH}$ | $\overline{CS}$ hold time time | 60 | - | - | ns | |
| t$_{SHW}$ | Serial clock H pulse width | 100 | - | - | ns | |
| t$_{SLW}$ | Serial clock L pulse width | 100 | - | - | ns | |
| t$_R$ | Rise time | - | - | 15 | ns | |
| t$_F$ | Fall time | - | - | 15 | ns | |

**(5) I²C interface characteristics**
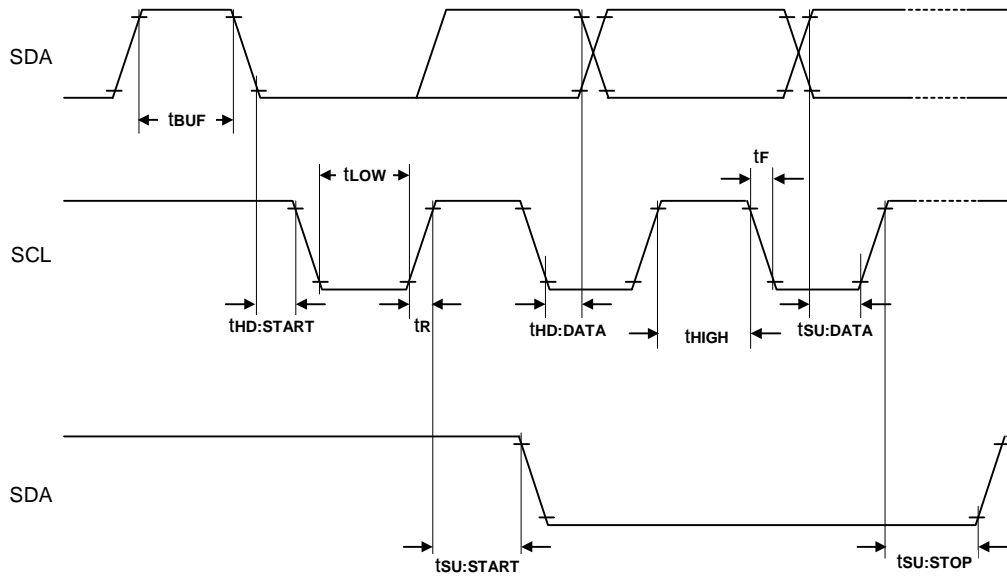


(V$_{DD}$ = 1.65 - 3.5V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------|------|------|------|------|-----------|
| fSCL | SCL clock frequency | DC | - | 400 | kHz | |
| TLOW | SCL clock Low pulse width | 1.3 | - | - | μs | |
| THIGH | SCL clock H pulse width | 0.6 | - | - | μs | |
| TSU:DATA | data setup time | 100 | - | - | ns | |
| THD:DATA | data hold time | 0 | - | 0.9 | μs | |
| TR | SCL，SDA rise time | 20+0.1Cb | - | 300 | ns | |
| TF | SCL，SDA fall time | 20+0.1Cb | - | 300 | ns | |
| Cb | Capacity load on each bus line | - | - | 400 | pF | |
| TSU:START | Setup timefor re-START | 0.6 | - | - | μs | |
| THD:START | START Hold time | 0.6 | - | - | μs | |
| TSU:STOP | Setup time for STOP | 0.6 | - | - | μs | |
| TBUF | Bus free times between STOP and START condition | 1.3 | - | - | μs | |

**(6) Reset Timing**



RES

Internal circuit status

During reset

End of reset
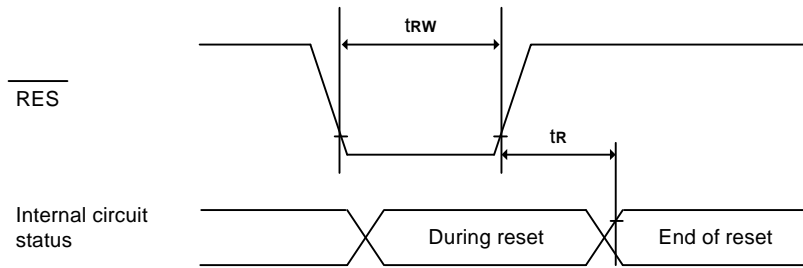
(V<sub>DD</sub> = 1.65 - 3.5V, T<sub>A</sub> = +25°C)

$(V_{DD} = 1.65 - 3.5V, T_{A} = +25°C)$

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------|------|------|------|------|-----------|
| t$_R$ | Reset time | - | - | 2.0 | μs | |
| t$_{RW}$ | Reset low pulse width | 10.0 | - | - | μs | |

**Application Circuit (for reference only)**

**Reference Connection to MPU:**

**1. 8080 series interface: (Internal oscillator, External Vpp)**
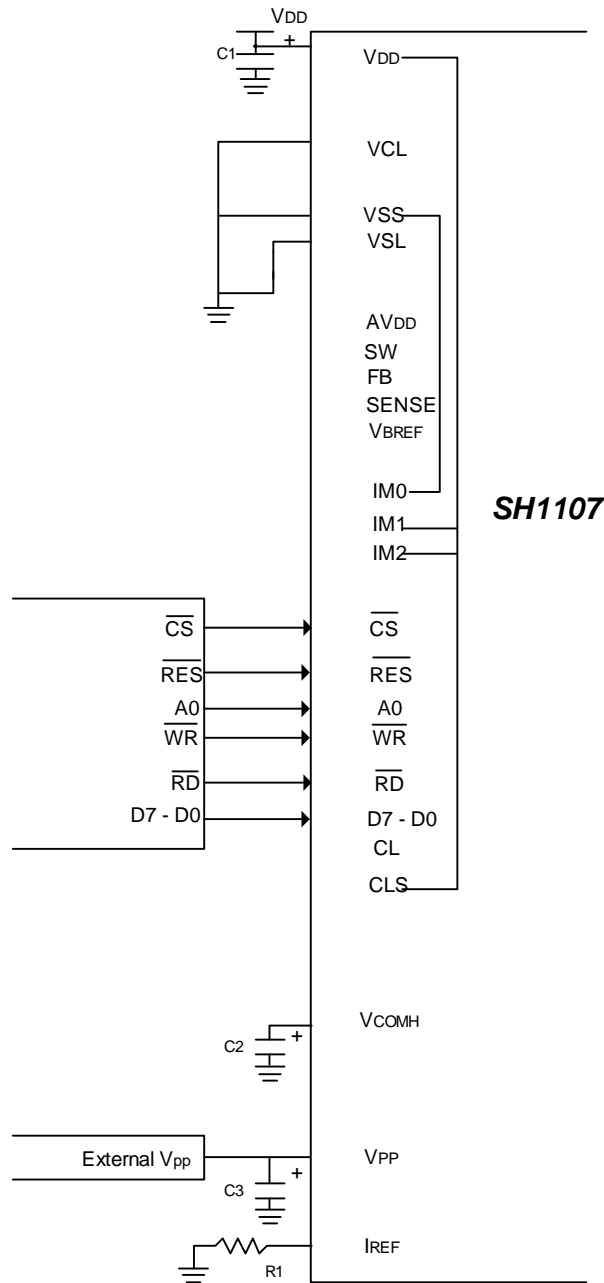


**Figure 18-1**

**Note:**

$C_1 - C_3$: 4.7μF.

$R_1$: about 750KΩ **(Refer to the** table8**)**, $R_1$ = (Voltage at $I_{REF}$ - $V_{SS}$)/$I_{REF}$

**2. 6800 Series Interface: (Internal oscillator, Built-in DC-DC)**
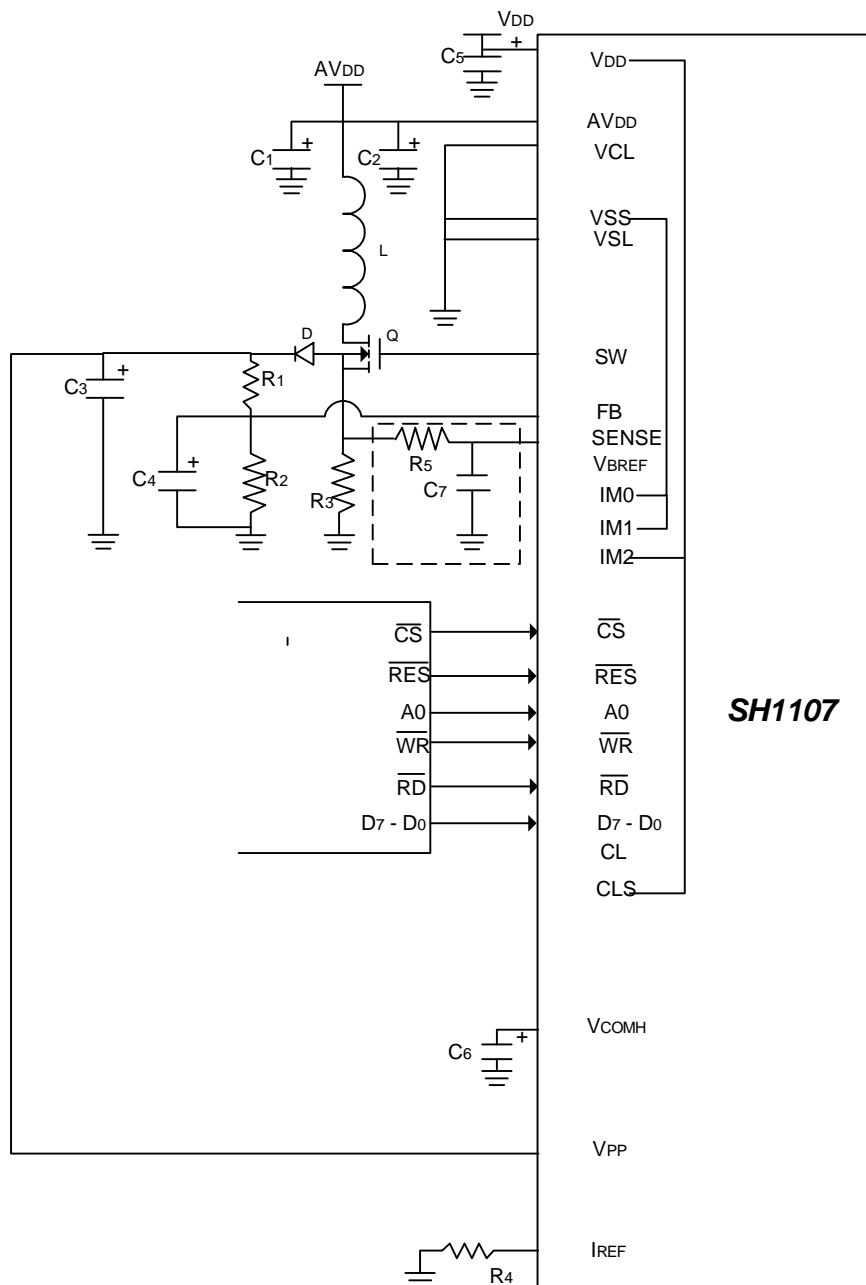


**Figure 18-2**

**Note:**
L, D, Q, R1, R2, R3, R5 and C1---C4, C7: Please refer to following description of DC-DC module.
C6:4.**7** μ F
R4: about 750KΩ  **(Refer to the** table8**)**, R4 = (Voltage at IREF - VSS)/IREF

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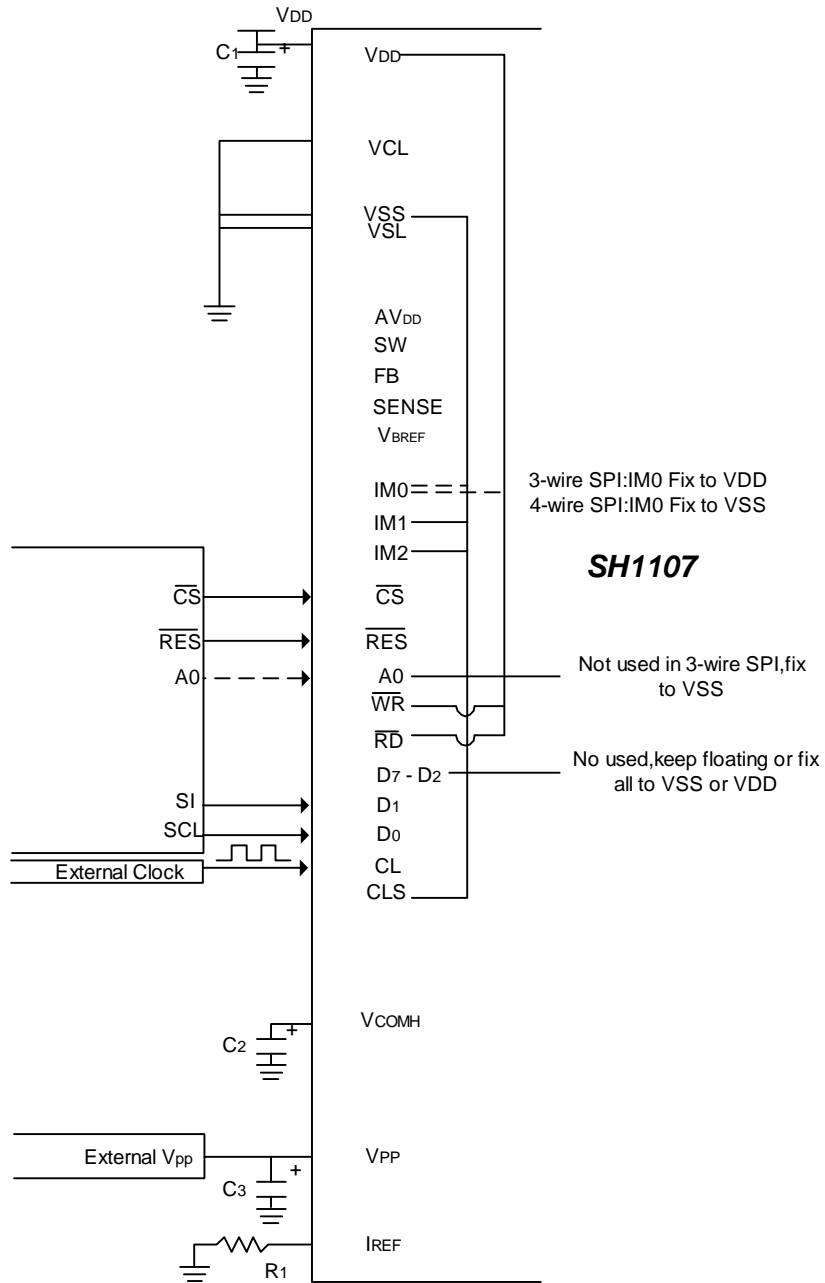**3. Serial Interface (3-wire or 4-wire SPI): (External oscillator, External Vpp, Max 16.5V)**



**Figure 18-3**

**Note:**
C1---C3: 4.7μF
R1: Recommend 750KΩ (Refer to the table8 )

![SH1107 logo]

# SH1107

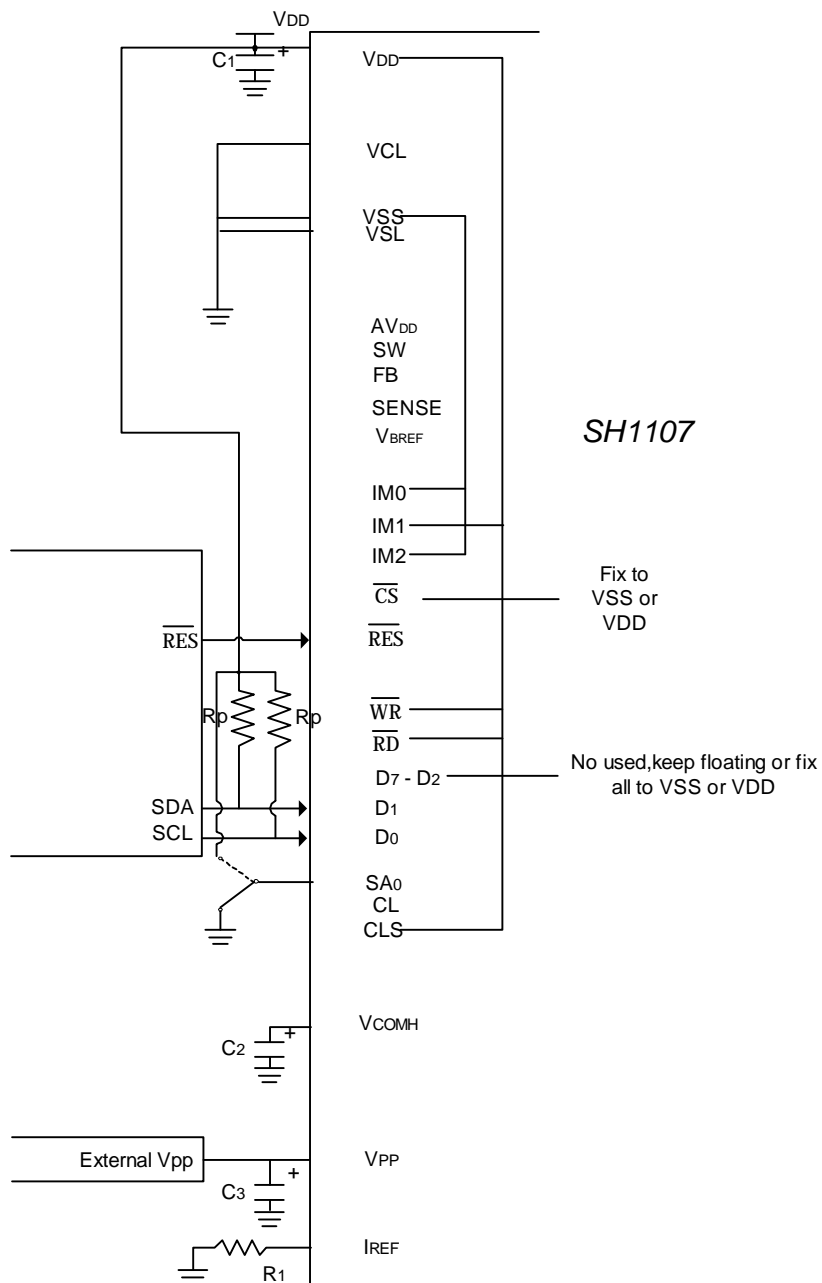**4. I²C Interface (Internal oscillator, External VPP, Max 16.5V)**



**Figure 18-4**

**Note:**
C1---C3:4.7 μF
R1: Recommend 750KΩ (Refer to the table8 )
The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1(VDD)
The positive supply of pull-up resistor must equal to the value of VDD
Recommend the value of resistor Rp equal to 1.5 KΩ

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## DC-DC

Below application circuit is an example for the input voltage of 3V AVDD to generate Vpp of about 15V@10mA-25mA application
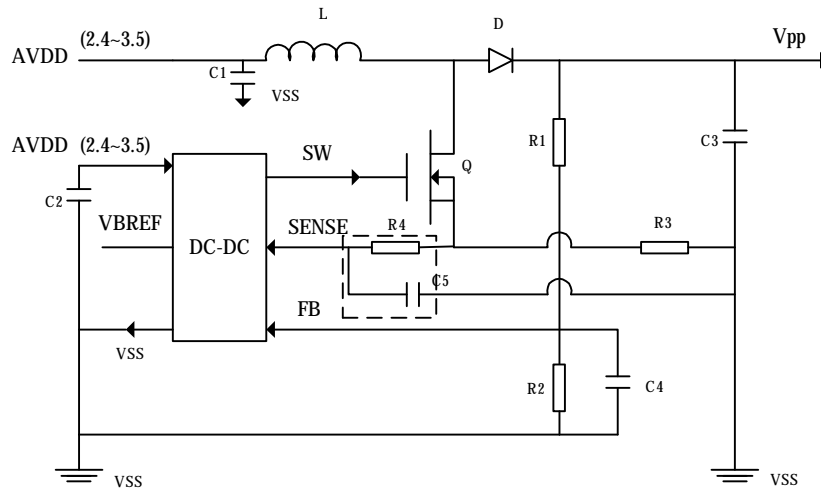


**Figure 19**

| Symbol | Value | Recommendation |
|--------|-------|----------------|
| L | 10 $\mu$H | |
| D | SCHOTTKY DIODE | 20V@0.5A, MBR0520 |
| Q | MOSFET | N-FET with low RDS(ON),MGSF1N02LT1 |
| R1 | 1.1M | 1%,1/8W |
| R2 | 100K | 1%,1/8W |
| R3 | 0.12 | 1%,1/2W |
| R4 | 10K | 1%,1/8W |
| C1 | 22 $\mu$F | Ceramic/16V |
| C2 | 0.1 $\mu$F | Ceramic/16V |
| C3 | 10 $\mu$F | Low ESR/16V |
| C4 | 56pF | Ceramic/16V |
| C5 | 220pF | Ceramic/16V |

**Note:** R4&C5 are optional; they can increase the efficiency of inductance

**Ordering Information**

| Part No. | Package |
|---|---|
| SH1107G | Gold bump on chip tray |

**Data Sheet History**

| Version | Contents | Date |
|---------|----------|------|
| 2.1 | P1: Added "multiplexing ratio and Vertical scrolling" description.<br>P30: Added command "Multiplex Raiton".<br>P31: Added command "Display Offset".<br>P38: Added command "Set Display Start Line".<br>P42: Modify command list. | Dec.2014 |
| 2.0 | P31: modify the max. value of SF<br>P46: modify the the value of IOL when VDD1<2V | Dec. 2013 |
| 1.0 | Original | Jun. 2013 |