Solution to points 2-4 of the Exercise of Nov. 2016, NUMA/UMA protocols.

2)

C2 PrRd on variable X0
C0 PrWr on variable X0

X0 is S + sharers{P0}
X0 is S in cache 0

C2 performs PrRd

Processor c2: Processor performs a read : PrRd
Snoopy Cache 1: This Read is a miss. Snoopy performs BusRd.
Bus Local Numa Node: BusRd goes to the Hub Local Node.
Hub/LocalNode: This Hub, which is also Home node will not modify sharers since it is the same node, and will do a Dreply(data).
Bus Local Numa Node: Dreply(data) arrives to Snoopy Cache 1.
Snoopy Cache 1 set the state to S.
Snoopy Cache 0 maintains the state to S.

C0: PrWr on variable X0

Processor c0: Processor performs write : PrWr
Snoopy Cache 0: This Write is hit… but the state is shared. Then, snoopy performs BusWr to invalidate other caches.
Snoopy Cache 1: Reads BusWr of the same address of one of its line. Invalidates it. So, it state will be I .
Bus Local Node: BusWr will arrive to Hub Local Node.
Hub/Local Node: This Hub, which is also Home node will not modify sharers since it is the same node. In addition, there is not more sharers so that it will not send invalidates to other hubs. However, it will modify the state to make it M. It will return the Dreply(data) (following strictly the protocol).
Bus Local Node: Dreply(data) arrives to Snoopy Cache 0.

3) C14 performs PrRd on variable X1

Processor c14: Processor C14 performs PrRd
Snoopy Cache 7: Miss in cache. Snoopy performs BusWr.
Bus Local Node: BusWr arrives to Hub Local Node. No other caches has this address, so , no invalidates.
Hub/Local Node: This hub is not the home node. OS indicates where the data is so this Hub local node will do a RdReq to the home node (MM1) .
Hub/Home Node: This hub has the memory in S. So, it will add to sharers hub Numa Node 3. Now sharers are {3,2,1}. Send Dreply(data) to hub/local node.
Hub/Local Node: This forward the data to the bus
Bus Local Node: Data is broadcasted.
Snoopy Cache 7: receives data and changes the state to S.

4) C4 performs PrWr on variable X2.
X2 is in MM2 and shared by 3, 2.

Processor c4: Processor C4 performs PrWr.
Snoopy Cache 2: Miss. Performs a BusRdX to Bus.
Bus Local Node: broadcasts the BusRdX… nobody has the data.
Hub/Local Node: This is not the home node. It resends a WrReq to the home node.
Hub/Home Node: Receives the WrReq. For each share node (hub node 3 I 2) send an invalidate.
Hub Node 2 : is the same as the home node… it forces a BusRdX broadcast in the bus.
Bus Numa Node 2: broadcast the BusRdx.
Snoopy Cache 5: invalidate X2 line.
Hub Node 3: receives the Invalidate. It forces a BusRdx broadcast in its bus.
Bus Numa Node 3: broadcast the BusRd.
Snoopy Cache 6: invalidate X2 line.
Hub/Home Node: Modifies the list of sharers. Now, it is Modified. The only shader is Numa Node 1. It send a Dreply(data) to Hub/Local node (1).
Hub/Local Node (1): forward the data to the bus.
Bus Local Node: broadcasts the data.
Snoopy Cache 2: read it and set the cache line to M.