EE526 Homework #3
CML Ring Oscillator

Design a 3-stage CML ring oscillator to give an oscillation frequency of 7GHz (+/- 5%). Fig 1 shows one stage of the ring. Use Vdd=1.8V, R=1.2kohms, Iss=400uA.

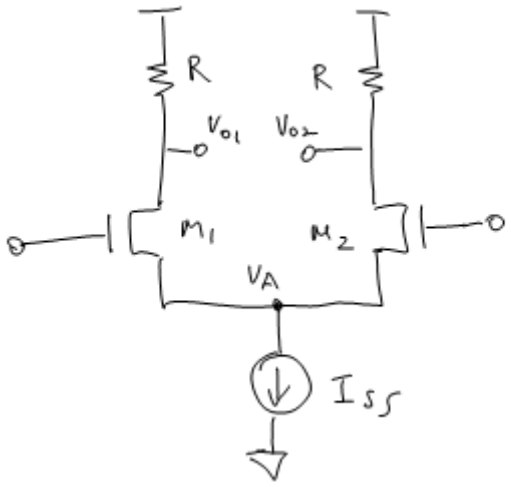

Fig.1 – One stage of the ring oscillator

a. To simplify the design, we use an ideal current source Iss rather than an actual current mirror. However, you still need to ensure that V_A is greater than 550mV during the operation of the oscillator.
b. When running your transient simulation, use a 'Stop time' of 200/BR and 'Maximum timestep' of 0.01/BR, where bitrate (BR) = 5Gbit/s. (Note that when we specify an expression in spice, we need to enclose them in {} brackets).
c. Note that although you can measure the frequency by first measuring the period using the LTspice cursors and taking the inverse, an alternate way is by using FFT. To do FFT, zoom in on the steady-state portion of the waveform (showing at least 10 cycles of oscillation), right click on the waveform, choose 'view', 'FFT', select 'Use current zoom extent', and click 'ok'. This will show you the FFT, i.e. spectrum, of the waveform. The highest peak of the spectrum represents the fundamental frequency of your waveform.
d. What is the oscillation frequency of your circuit? Include the FFT plot. Use the cursor function to show the frequency peak.
e. Include a plot of Vo1, Vo2, and V_A from one of the stages. Plot Vo1 and Vo2 in one pane, and V_A in another pane. Zoom in on the waveform near the simulation end so that we see only around 5 cycles of oscillations.
f. Include a print-out of the schematic and netlist in your report.