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Is Moore's Law Really Dead?

The principle behind Moore's law was first introduced in 1965, and since then it has driven innovation in the electrical engineering industry. This principle asserts that the performance of leading computer processors doubles roughly every one and a half years and it was proposed originally by Gordon E. Moore. In his 1965 paper he talked about the decreasing space between, size of, and cost of transistors found on integrated circuits. He stated, "With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip" (G. E. Moore). A number in the range of 65,000 may have been a bold claim in 1965, but the recent flagship processor from Intel – the core i9 13900k – boasts up to 26 billion transistors on a single chip. This dramatic increase, albeit spanning several decades, shows that the original claims from Moore have been able to hold true since its inception. Despite the constant growth that has been prevalent over many years, Moore's law has seemed to slow down more and more in the recent years. As components get smaller and smaller, we encounter physical boundaries and roadblocks which present many difficulties in the manufacturing processes of newer and faster chips.

With chips being manufactured in the nanometer scale, we encounter some new problems that have never been encountered before. Findings from an article showed that "Further reduction in insulator thickness would have resulted in unacceptable (and exponential) increases in gate leakage current through direct quantum tunneling" (Theis and Wong). Direct quantum tunneling of electrons through oxide thickness is a phenomenon that shows that even if advances are made in finding processes to allow the manufacturing of smaller and smaller components, other physical limitations will likely arise which can prevent the functionality of ever-smaller components. Another physical challenge that is presented with minute components is the difficulty to discern between activated and deactivated currents. From the same article we learn that, "Further reduction in operating voltage swing would have resulted in either unacceptably low channel current in the "on" state (unacceptable decreases in switching speed) or increased leakage current in the "off" state (unacceptable increases in passive power)" (Theis and Wong). With these presented difficulties, in order for a future continuation of Moore's law, the future advances in manufacturing technology will have to present unique solutions. Until this point, the increases in computing power have come from placing more, smaller transistors on the same size chip. Due to these difficulties, solutions will have to come from unique innovations.

At the present time, the most-explored solution for this problem is to expand the design of integrated circuits to the third dimension. In an article by Samuel K. Moore, we find a few examples of 3D integrated circuit design that are in practice today. In the consumer space, the most notable of the examples is the use of 3D V-Cache in AMD's most recent consumer processors. By stacking cache modules directly on top the other components in their top-of-the-line gaming/productivity CPU's they were able to achieve an increase of performance of up to 15 percent. Another notable example of 3D chip design being used today is Intel's Ponte Vecchio Supercomputer chip, which was also highlighted in this same article. "Using both 2.5D and 3D technologies, Intel squeezed 3,100 square millimeters of silicon—nearly equal to four Nvidia A100 GPUs—into a 2,330-mm^2 footprint" (S. K. Moore). These innovations allowed Intel's supercomputer chip to finally "pierce the exaflop barrier" (S. K. Moore).

Techniques for 3D chip design expand beyond stacking cache on top of other components. The pioneers of 3D integrated circuit design have found ways to stack CMOS components directly atop one another. Researchers were able to find a configuration of CMOS components that allowed the design of an inverter that had a footprint half the size of a typical inverter designed by placing components side-by-side. "Combined with appropriate interconnects, the 3D-stacked CMOS approach effectively cuts the inverter footprint in half, doubling the area density and further pushing the limits of Moore's Law" (Radosavljevic and Kavalieros). Their research in the area has led to several advances in the development of 3D silicon chips, certainly beyond vertical inverter configurations. They've successfully made entire integrated circuits featuring 3D circuit constructions, stating, "We've made wafers where the smallest distance between two sets of stacked devices is only 55 nm. While the device performance results we achieved are not records in and of themselves, they do compare well with individual nonstacked control devices built on the same wafer with the same processing" (Radosavljevic and Kavalieros).

New innovations and solutions in the realm of processor design are being presented constantly, and if we're to expect a continuation in Moore's law and computation performance increases in the future, the solutions that are presented will need to take a different shape from the solutions that have been presented through the first 40 years of the existence of Moore's law as a concept. Further innovations in the realm of newer magnetic memory, computation techniques, and overall rethinking of modern computation technologies are being considered and studied each day. With the increase of technologies and devices that require more demanding computation power, the development of more efficient and computationally effect devices will surmise, but whether it will keep up with the development claims of Moore's law will only be told by the future.

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