CHAPTER 6

Bipolar Junction Transistors (BJTs)

IN THIS CHAPTER YOU WILL LEARN

1. The physical structure of the bipolar transistor and how it works.
2. How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current–voltage characteristics.
3. How to analyze and design circuits that contain bipolar transistors, resistors, and dc sources.
4. How the transistor can be used to make an amplifier.
5. How to obtain linear amplification from the fundamentally nonlinear BJT.
6. The three basic ways for connecting a BJT to be able to construct amplifiers with different properties.
7. Practical circuits for bipolar-transistor amplifiers that can be constructed by using discrete components.

Introduction

In this chapter, we study the other major three-terminal device: the bipolar junction transistor (BJT). The presentation of the material in this chapter parallels but does not rely on that for the MOSFET in Chapter 5; thus, if desired, the BJT can be studied before the MOSFET.

Three-terminal devices are far more useful than two-terminal ones, such as the diodes studied in Chapter 4, because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source, which as we learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. The switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits, which led to electronics changing the way we work, play, and indeed, live. The invention of the BJT also eventually led to the dominance of information technology and the emergence of the knowledge-based economy.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known

very early on, it was not until the 1970s and 1980s that it became a serious competitor to the BJT. By 2009, the MOSFET was undoubtedly the most widely used electronic device, and CMOS technology the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications. For instance, the reliability of BJT circuits under severe environmental conditions makes them the dominant device in certain automotive applications.

The BJT remains popular in discrete-circuit design, in which a very wide selection of BJT types are available to the designer. Here we should mention that the characteristics of the bipolar transistor are so well understood that one is able to design transistor circuits whose performance is remarkably predictable and quite insensitive to variations in device parameters.

The BJT is still the preferred device in very demanding analog circuit applications, both integrated and discrete. This is especially true in very-high-frequency applications, such as radio-frequency (RF) circuits for wireless systems. A very-high-speed digital logic-circuit family based on bipolar transistors, namely, emitter-coupled logic, is still in use. Finally, bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors. The resulting technology is known as BiCMOS, and it is finding increasingly larger areas of application (see Chapters 7, 8, 12, and 14).

In this chapter, we shall start with a description of the physical operation of the BJT. Though simple, this physical description provides considerable insight regarding the performance of the transistor as a circuit element. We then quickly move from describing current flow in terms of electrons and holes to a study of the transistor terminal characteristics. Circuit models for transistor operation in different modes will be developed and utilized in the analysis and design of transistor circuits. The main objective of this chapter is to develop in the reader a high degree of familiarity with the BJT. Thus, by the end of the chapter, the reader should be able to perform rapid first-order analysis of transistor circuits and to design single-stage transistor amplifiers.

6.1 Device Structure and Physical Operation

6.1.1 Simplified Structure and Modes of Operation

Figure 6.1 shows a simplified structure for the BJT. A practical transistor structure will be shown later (see also Appendix A, which deals with fabrication technology).

As shown in Fig. 6.1, the BJT consists of three semiconductor regions: the emitter region (*n* type), the base region (*p* type), and the collector region (*n* type). Such a transistor is called an *npn* transistor. Another transistor, a dual of the *npn* as shown in Fig. 6.2, has a *p*-type emitter, an *n*-type base, and a *p*-type collector, and is appropriately called a *pnp* transistor.

A terminal is connected to each of the three semiconductor regions of the transistor, with the terminals labeled **emitter** (E), **base** (B), and **collector** (C).

The transistor consists of two *pn* junctions, the **emitter–base junction** (EBJ) and the **collector–base junction** (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 6.1. The **active mode** is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the **cutoff mode** and the **saturation mode**. As the name implies, in the cutoff mode no current flows because both junctions are reverse biased.

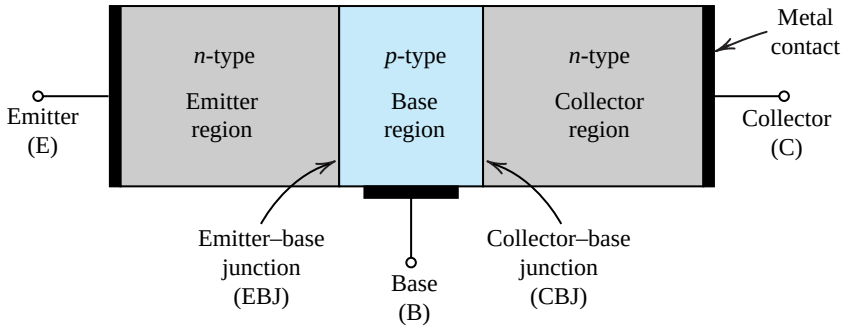


Figure 6.1 A simplified structure of the *npn* transistor.

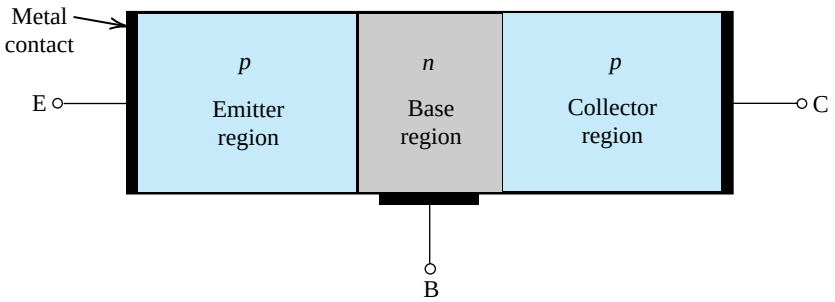


Figure 6.2 A simplified structure of the *pnp* transistor.

Table 6.1 BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

As we will see shortly, charge carriers of both polarities—that is, electrons and holes—participate in the current-conduction process in a bipolar transistor, which is the reason for the name *bipolar*.[1]

6.1.2 Operation of the *npn* Transistor in the Active Mode

Of the three modes of operation of the BJT, the active mode is the most important. Therefore, we begin our study of the BJT by considering its physical operation in the active mode.[2] This situation is illustrated in Fig. 6.3 for the *npn* transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage

[1]This should be contrasted with the situation in the MOSFET, where current is conducted by charge carriers of one type only; electrons in *n*-channel devices or holes in *p*-channel devices. In earlier days, some referred to FETs as unipolar devices.

[2]The material in this section assumes that the reader is familiar with the operation of the *pn* junction under forward-bias conditions (Section 3.5).

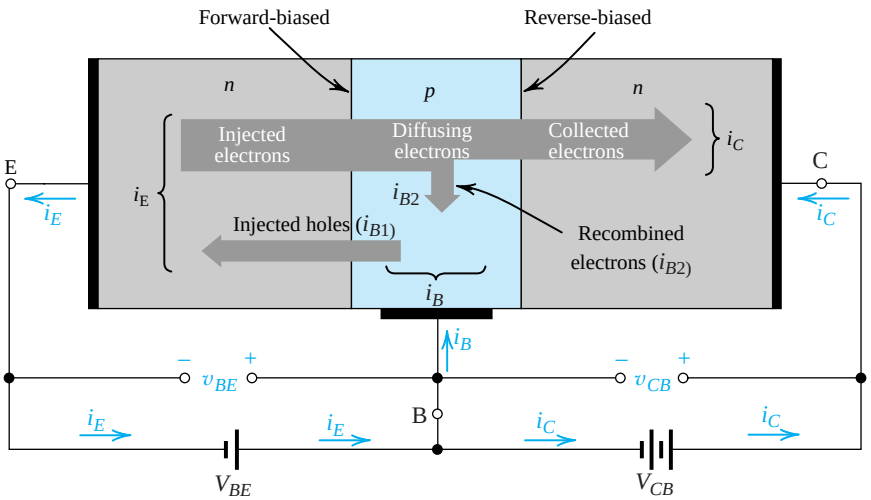


Figure 6.3 Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

V_{BE} causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward-biasing the emitter–base junction. The collector–base voltage V_{CB} causes the *n*-type collector to be at a higher potential than the *p*-type base, thus reverse-biasing the collector–base junction.

Current Flow The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) at a much higher level than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

The current that flows across the emitter–base junction will constitute the emitter current i_E, as indicated in Fig. 6.3. The direction of i_E is "out of" the emitter lead, which, following the usual conventions, is in the direction of the positive-charge flow (hole current) and opposite to the direction of the negative-charge flow (electron current), with the emitter current i_E being equal to the sum of these two components. However, since the electron component is much larger than the hole component, the emitter current will be dominated by the electron component.

Let us now consider the electrons injected from the emitter into the base. These electrons will be **minority carriers** in the *p*-type base region. Because the base is usually very thin, in the steady state the excess minority carrier (electron) concentration in the base will have an almost-straight-line profile, as indicated by the solid straight line in Fig. 6.4. The electron concentration will be highest [denoted by $n_p(0)$] at the emitter side and lowest (zero) at the collector side.[3] As in the case of any forward-biased *pn* junction (Section 3.5), the concentration $n_p(0)$ will be proportional to e^{v_{BE}/V_T},

[3]This minority carrier distribution in the base results from the boundary conditions imposed by the two junctions. It is not an exponentially decaying distribution, which would result if the base region were infinitely thick. Rather, the thin base causes the distribution to decay linearly. Furthermore, the reverse bias on the collector–base junction causes the electron concentration at the collector side of the base to be zero.

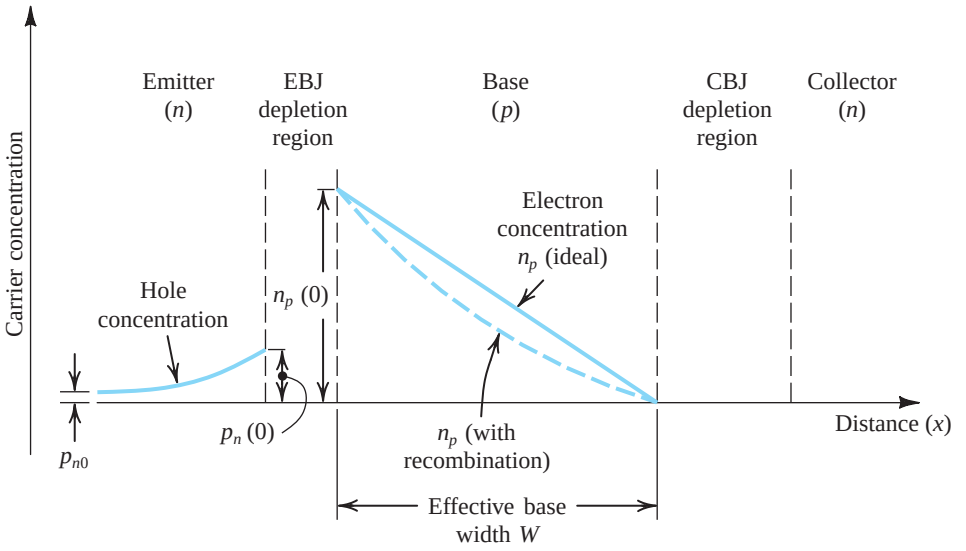


Figure 6.4 Profiles of minority-carrier concentrations in the base and in the emitter of an *npn* transistor operating in the active mode: $v_{BE} > 0$ and $v_{CB} \geq 0$.

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \tag{6.1}$$

where n_{p0} is the thermal-equilibrium value of the minority carrier (electron) concentration in the base region, v_{BE} is the forward base–emitter bias voltage, and V_T is the thermal voltage, which is equal to approximately 25 mV at room temperature. The reason for the zero concentration at the collector side of the base is that the positive collector voltage v_{CB} causes the electrons at that end to be swept across the CBJ depletion region.

The tapered minority-carrier concentration profile (Fig. 6.4) causes the electrons injected into the base to diffuse through the base region toward the collector. This electron diffusion current I_n is directly proportional to the slope of the straight-line concentration profile,

$$\begin{aligned} I_n &= A_E q D_n \frac{dn_p(x)}{dx} \\ &= A_E q D_n \left(-\frac{n_p(0)}{W} \right) \end{aligned} \tag{6.2}$$

where A_E is the cross-sectional area of the base–emitter junction (in the direction perpendicular to the page), q is the magnitude of the electron charge, D_n is the electron diffusivity in the base, and W is the effective width of the base. Observe that the negative slope of the minority carrier concentration results in a negative current I_n across the base; that is, I_n flows from right to left (in the negative direction of x), which corresponds to the usual convention, namely, opposite to the direction of electron flow.

Some of the electrons that are diffusing through the base region will combine with holes, which are the majority carriers in the base. However, since the base is usually very thin and lightly doped, the proportion of electrons "lost" through this **recombination process** will be quite small. Nevertheless, the recombination in the base region causes the excess minority carrier concentration profile to deviate from a straight line and take the slightly concave shape indicated by the broken line in Fig. 6.4. The slope of the concentration profile at the EBJ is

slightly higher than that at the CBJ, with the difference accounting for the small number of electrons lost in the base region through recombination.

The Collector Current From the description above we see that most of the diffusing electrons will reach the boundary of the collector–base depletion region. Because the collector is more positive than the base (by v_{CB} volts), these successful electrons will be swept across the CBJ depletion region into the collector. They will thus get "collected" to constitute the collector current i_C. Thus $i_C = I_n$, which will yield a negative value for i_C, indicating that i_C flows in the negative direction of the x axis (i.e., from right to left). Since we will take this to be the positive direction of i_C, we can drop the negative sign in Eq. (6.2). Doing this and substituting for $n_p(0)$ from Eq. (6.1), we can thus express the collector current i_C as

$$i_C = I_S e^{v_{BE}/V_T} \tag{6.3}$$

where the **saturation current** I_S is given by

$$I_S = A_E q D_n n_{p0} / W$$

Substituting $n_{p0} = n_i^2 / N_A$, where n_i is the intrinsic carrier density and N_A is the doping concentration in the base, we can express I_S as

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \tag{6.4}$$

An important observation to make here is that the magnitude of i_C is independent of v_{CB}. That is, as long as the collector is positive with respect to the base, the electrons that reach the collector side of the base region will be swept into the collector and register as collector current.

The saturation current I_S is inversely proportional to the base width W and is directly proportional to the area of the EBJ. Typically I_S is in the range of 10^{-12} A to 10^{-18} A (depending on the size of the device). Because I_S is proportional to n_i^2, it is a strong function of temperature, approximately doubling for every 5°C rise in temperature. (For the dependence of n_i^2 on temperature, refer to Eq. 3.37.)

Since I_S is directly proportional to the junction area (i.e., the device size), it will also be referred to as the **scale current**. Two transistors that are identical except that one has an EBJ area, say, twice that of the other will have saturation currents with that same ratio (i.e., 2). Thus for the same value of v_{BE} the larger device will have a collector current twice that in the smaller device. This concept is frequently employed in integrated-circuit design.

The Base Current The base current i_B is composed of two components. The first component i_{B1} is due to the holes injected from the base region into the emitter region. This current component is proportional to e^{v_{BE}/V_T}. The second component of base current, i_{B2}, is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process. Because i_{B2} is proportional to the number of electrons injected into the base, it also will be proportional to e^{v_{BE}/V_T}. Thus the total base current, $i_B = i_{B1} + i_{B2}$, will be proportional to e^{v_{BE}/V_T}, and can be expressed as a fraction of the collector current i_C as follows:

$$i_B = \frac{i_C}{\beta} \tag{6.5}$$

That is,

$$i_B = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T} \tag{6.6}$$

where β is a transistor parameter.

For modern *npn* transistors, β is in the range 50 to 200, but it can be as high as 1000 for special devices. For reasons that will become clear later, the parameter β is called the **common-emitter current gain**.

The above description indicates that the value of β is highly influenced by two factors: the width of the base region, W, and the relative dopings of the base region and the emitter region, N_A/N_D. To obtain a high β (which is highly desirable since β represents a gain parameter) the base should be thin (W small) and lightly doped and the emitter heavily doped (making N_A/N_D small). For modern integrated circuit fabrication technologies, W is in the nanometer range.

The Emitter Current Since the current that enters a transistor must leave it, it can be seen from Fig. 6.3 that the emitter current i_E is equal to the sum of the collector current i_C and the base current i_B; that is,

$$i_E = i_C + i_B \tag{6.7}$$

Use of Eqs. (6.5) and (6.7) gives

$$i_E = \frac{\beta+1}{\beta} i_C \tag{6.8}$$

That is,

$$i_E = \frac{\beta+1}{\beta} I_S e^{v_{BE}/V_T} \tag{6.9}$$

Alternatively, we can express Eq. (6.8) in the form

$$i_C = \alpha i_E \tag{6.10}$$

where the constant α is related to β by

$$\alpha = \frac{\beta}{\beta+1} \tag{6.11}$$

Thus the emitter current in Eq. (6.9) can be written

$$i_E = (I_S/\alpha) e^{v_{BE}/V_T} \tag{6.12}$$

Finally, we can use Eq. (6.11) to express β in terms of α, that is,

$$\beta = \frac{\alpha}{1-\alpha} \tag{6.13}$$

It can be seen from Eq. (6.11) that α is a constant (for a particular transistor) that is less than but very close to unity. For instance, if $\beta = 100$, then $\alpha \simeq 0.99$. Equation (6.13) reveals an important fact: Small changes in α correspond to very large changes in β. This mathematical observation manifests itself physically, with the result that transistors of the same type

may have widely different values of β. For reasons that will become apparent later, α is called the **common-base current gain**.

Recapitulation and Equivalent-Circuit Models We have presented a first-order model for the operation of the *npn* transistor in the active mode. Basically, the forward-bias voltage v_{BE} causes an exponentially related current i_C to flow in the collector terminal. The collector current i_C is independent of the value of the collector voltage as long as the collector–base junction remains reverse biased; that is, $v_{CB} \geq 0$. Thus in the active mode the collector terminal behaves as an ideal constant-current source where the value of the current is determined by v_{BE}. The base current i_B is a factor $1/\beta$ of the collector current, and the emitter current is equal to the sum of the collector and base currents. Since i_B is much smaller than i_C (i.e., $\beta \gg 1$), $i_E \simeq i_C$. More precisely, the collector current is a fraction α of the emitter current, with α smaller than, but close to, unity.

This first-order model of transistor operation in the active mode can be represented by the equivalent circuit shown in Fig. 6.5(a). Here, diode D_E has a scale current I_{SE} equal to (I_S/α) and thus provides a current i_E related to v_{BE} according to Eq. (6.12). The current of the controlled source, which is equal to the collector current, is controlled by v_{BE} according to the exponential relationship indicated, a restatement of Eq. (6.3). This model is in essence a nonlinear voltage-controlled current source. It can be converted to the current-controlled current-source model shown in Fig. 6.5(b) by expressing the current of the controlled source as αi_E. Note that this model is also nonlinear because of the exponential

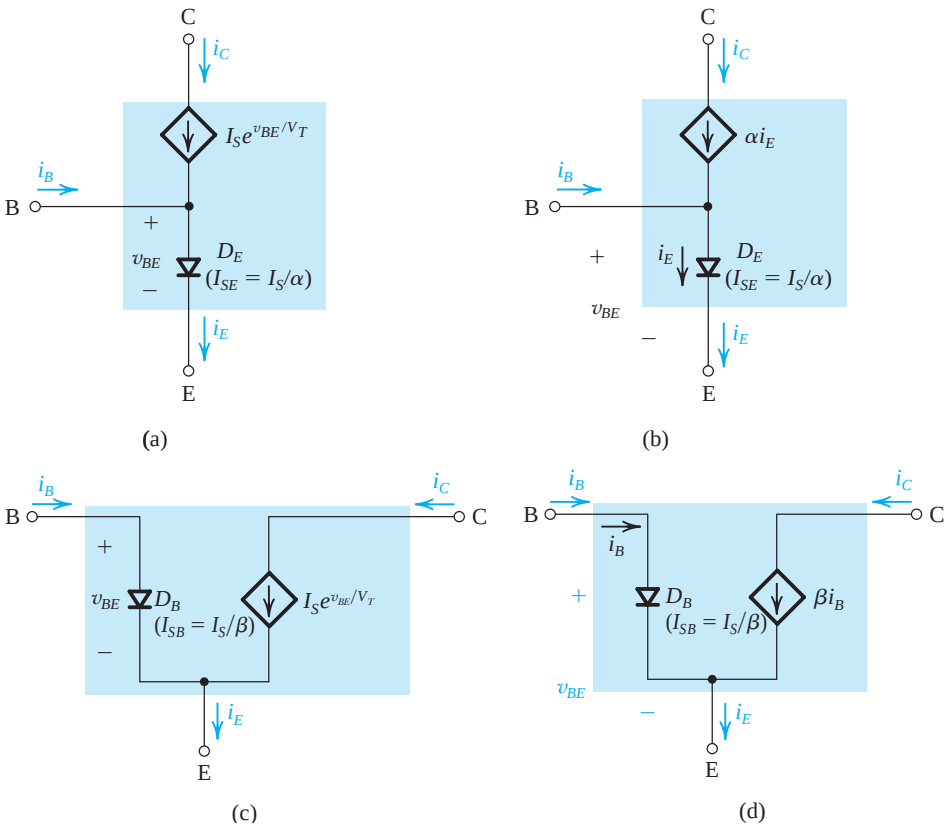


Figure 6.5 Large-signal equivalent-circuit models of the *npn* BJT operating in the forward active mode.

relationship of the current i_E through diode D_E and the voltage v_{BE}. From this model we observe that if the transistor is used as a two-port network with the input port between E and B and the output port between C and B (i.e., with B as a common terminal), then the current gain observed is equal to α. Thus α is called the common-base current gain.

Two other equivalent circuit models, shown in Fig. 6.5(c) and (d), may be used to represent the operation of the BJT. The model of Fig. 6.5(c) is essentially a voltage-controlled current source. However, here diode D_B conducts the base current and thus its current scale factor is I_S/β, resulting in the i_B–v_{BE} relationship given in Eq. (6.6). By simply expressing the collector current as βi_B we obtain the current-controlled current-source model shown in Fig. 6.5(d). From this latter model we observe that if the transistor is used as a two-port network with the input port between B and E and the output port between C and E (i.e., with E as the common terminal), then the current gain observed is equal to β. Thus β is called the common-emitter current gain.

Finally, we note that the models in Fig. 6.5 apply for any positive value of v_{BE}. That is, unlike the models we will be discussing in Section 6.5, here there is no limitation on the size of v_{BE}, and thus these models are referred to as **large-signal models**.

Example 6.1

An *npn* transistor having $I_S = 10^{-15}$A and $\beta = 100$ is connected as follows: The emitter is grounded, the base is fed with a constant-current source supplying a dc current of 10 μA, and the collector is connected to a 5-V dc supply via a resistance R_C of 3 kΩ. Assuming that the transistor is operating in the active mode, find V_{BE} and V_{CE}. Use these values to verify active-mode operation. Replace the current source with a resistance connected from the base to the 5-V dc supply. What resistance value is needed to result in the same operating conditions?

Solution

If the transistor is operating in the active mode, it can be represented by one of the four possible equivalent-circuit models shown in Fig. 6.5. Because the emitter is grounded, either the model in Fig. 6.5(c) or that in Fig. 6.5(d) would be suitable. Since we know the base current I_B, the model of Fig. 6.5(d) is the most suitable.

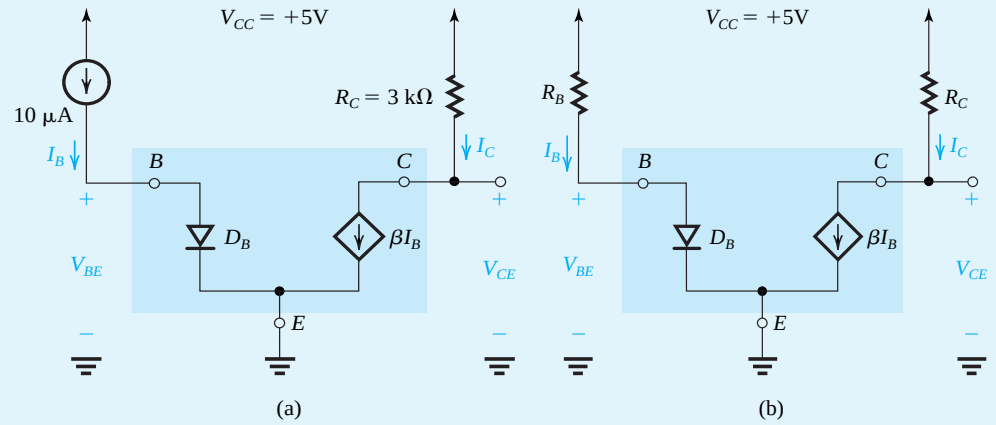


Figure 6.6 Circuits for Example 6.1.

Example 6.1 *continued*

Figure 6.6(a) shows the circuit as described with the transistor represented by the model of Fig. 6.5(d). We can determine V_{BE} from the exponential characteristic of D_B as follows:

$$V_{BE} = V_T \ln \frac{I_B}{I_S/\beta}$$

$$= 25 \ln\left(\frac{10 \times 10^{-6}}{10^{-17}}\right)$$

$$= 690 \text{ mV} = 0.69 \text{ V}$$

Next we determine the value of V_{CE} from

$$V_{CE} = V_{CC} - R_C I_C$$

where

$$I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 10^{-3} \text{ A} = 1 \text{ mA}$$

Thus,

$$V_{CE} = 5 - 3 \times 1 = +2 \text{ V}$$

Since V_C at +2 V is higher than V_B at 0.69 V, the transistor is indeed operating in the active mode.

Now, replacing the 10-μA current source with a resistance R_B connected from the base to the 5-V dc supply V_{CC}, as in Fig. 6.6(b), the value of R_B must be

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{5 - 0.69}{10 \text{ μA}} = 431 \text{ kΩ}$$

EXERCISES

6.1 Consider an *npn* transistor with $v_{BE} = 0.7$ V at $i_C = 1$ mA. Find v_{BE} at $i_C = 0.1$ mA and 10 mA.
Ans. 0.64 V; 0.76 V

6.2 Transistors of a certain type are specified to have β values in the range 50 to 150. Find the range of their α values.
Ans. 0.980 to 0.993

6.3 Measurement of an *npn* BJT in a particular circuit shows the base current to be 14.46 μA, the emitter current to be 1.460 mA, and the base–emitter voltage to be 0.7 V. For these conditions, calculate α, β, and I_S.
Ans. 0.99; 100; 10^{-15} A

6.4 Calculate β for two transistors for which $\alpha = 0.99$ and 0.98. For collector currents of 10 mA, find the base current of each transistor.
Ans. 99; 49; 0.1 mA; 0.2 mA

6.5 A transistor for which $I_S = 10^{-16}$ A and $\beta = 100$ is conducting a collector current of 1 mA. Find v_{BE}. Also, find I_{SE} and I_{SB} for this transistor.
Ans. 747.5 mV; 1.01×10^{-16} A ; 10^{-18} A

6.6 For the circuit in Fig. 6.6(a) analyzed in Example 6.1, find the maximum value of R_C that will still result in active-mode operation.
Ans. 4.31 kΩ

6.1.3 Structure of Actual Transistors

Figure 6.7 shows a more realistic (but still simplified) cross section of an *npn* BJT. Note that the collector virtually surrounds the emitter region, thus making it difficult for the electrons injected into the thin base to escape being collected. In this way, the resulting α is close to unity and β is large. Also, observe that the device is *not* symmetrical, and thus the emitter and collector cannot be interchanged.[4] For more detail on the physical structure of actual devices, the reader is referred to Appendix A.

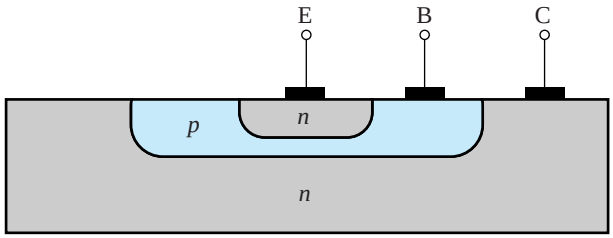


Figure 6.7 Cross-section of an *npn* BJT.

The structure in Fig. 6.7 indicates also that the CBJ has a much larger area than the EBJ. Thus the CB diode D_C has a saturation current I_{SC} that is much larger than the saturation current of the EB diode D_E. Typically, I_{SC} is 10 to 100 times larger than I_{SE} (recall that $I_{SE} = I_S/\alpha \simeq I_S$).

EXERCISE

6.7 A particular transistor has $I_S = 10^{-15}$ A and $\alpha \simeq 1$. If the CBJ area is 100 times the area of the EBJ, find the collector scale current I_{SC}.
Ans. 10^{-13} A

[4] If the emitter and collector are reversed—that is, the CBJ is forward biased and the EBJ is reverse biased—the device operates in a mode called the "reverse-active mode." The resulting values of α and β, denoted α_R and β_R (with R denoting reverse), are much lower than the values of α and β, respectively, obtained in the "forward" active mode discussed above. Hence, the reverse-active mode has no practical application. The MOSFET, on the other hand, being a perfectly symmetrical device, can operate equally well with its drain and source terminals interchanged.

6.1.4 Operation in the Saturation Mode[5]

As mentioned above, for the BJT to operate in the active mode, the CBJ must be reverse biased. Thus far, we have stated this condition for the *npn* transistor as $v_{CB} \geq 0$. However, we know that a *pn* junction does not effectively become forward biased until the forward voltage across it exceeds approximately 0.4 V. It follows that one can maintain active-mode operation of an *npn* transistor for negative v_{CB} down to approximately –0.4 V. This is illustrated in Fig. 6.8, which is a sketch of i_C versus v_{CB} for an *npn* transistor operated with a constant emitter current I_E. As expected, i_C is independent of v_{CB} in the active mode, a situation that extends for v_{CB} going negative to approximately –0.4 V. Below this value of v_{CB}, the CBJ begins to conduct sufficiently that the transistor leaves the active mode and enters the saturation mode of operation, where i_C decreases.

To see why i_C decreases in saturation, we can construct a model for the saturated *npn* transistor as follows. We augment the model of Fig. 6.5(c) with the forward-conducting CBJ diode D_C, as shown in Fig. 6.9. Observe that the current i_{BC} will subtract from the controlled-source current, resulting in the reduced collector current i_C given by

$$i_C = I_S e^{v_{BE}/V_T} - I_{SC} e^{v_{BC}/V_T} \tag{6.14}$$

The second term will play an increasing role as v_{BC} exceeds 0.4 V or so, causing i_C to decrease and eventually reach zero.

Figure 6.9 also indicates that in saturation the base current will increase to the value

$$i_B = (I_S/\beta) e^{v_{BE}/V_T} + I_{SC} e^{v_{BC}/V_T} \tag{6.15}$$

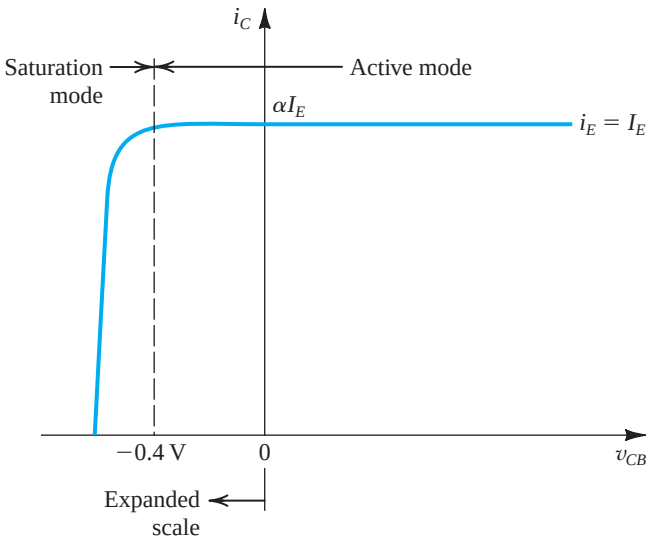


Figure 6.8 The i_C–v_{CB} characteristic of an *npn* transistor fed with a constant emitter current I_E. The transistor enters the saturation mode of operation for $v_{CB} < -0.4$ V, and the collector current diminishes.

[5]Saturation in a BJT means something completely different from that in a MOSFET. The saturation mode of operation of the BJT is analogous to the triode region of operation of the MOSFET. On the other hand, the saturation region of operation of the MOSFET corresponds to the active mode of BJT operation.

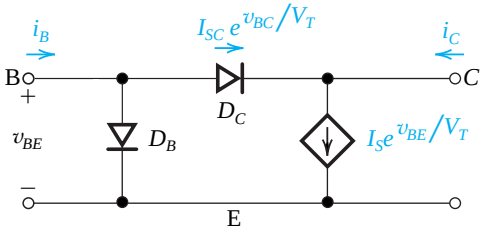


Figure 6.9 Modeling the operation of an *npn* transistor in saturation by augmenting the model of Fig. 6.5(c) with a forward conducting diode D_C. Note that the current through D_C increases i_B and reduces i_C.

Equations (6.14) and (6.15) can be combined to obtain the ratio i_C/i_B for a saturated transistor. We observe that this ratio will be *lower* than the value of β. Furthermore, the ratio will decrease as v_{BC} is increased and the transistor is driven deeper into saturation. Because i_C/i_B of a saturated transistor can be set to any desired value lower than β by adjusting v_{BC}, this ratio is known as **forced** β and denoted β_{forced},

$$\beta_{\text{forced}} = \left.\frac{i_C}{i_B}\right|_{\text{saturation}} \leq \beta \tag{6.16}$$

As will be shown later, in analyzing a circuit we can determine whether the BJT is in the saturation mode by either of the following two tests:

1. Is the CBJ forward biased by more than 0.4 V?
2. Is the ratio i_C/i_B lower than β?

The collector-to-emitter voltage v_{CE} of a saturated transistor can be found from Fig. 6.9 as the difference between the forward-bias voltages of the EBJ and the CBJ,

$$V_{CE\text{sat}} = V_{BE} - V_{BC} \tag{6.17}$$

Recalling that the CBJ has a much larger area than the EBJ, V_{BC} will be smaller than V_{BE} by 0.1 to 0.3 V. Thus,

$$V_{CE\text{sat}} \simeq 0.1 \text{ to } 0.3 \text{ V}$$

Typically we will assume that a transistor at the edge of saturation has $V_{CE\text{sat}} = 0.3$ V, while a transistor deep in saturation has $V_{CE\text{sat}} = 0.2$ V.

EXERCISES

6.8 Use Eq. (6.14) to show that i_C reaches zero at

$$V_{CE} = V_T \ln(I_{SC}/I_S)$$

Calculate V_{CE} for a transistor whose CBJ has 100 times the area of the EBJ.
Ans. 115 mV

6.9 Use Eqs. (6.14), (6.15), and (6.16) to show that a BJT operating in saturation with $V_{CE} = V_{CE\text{sat}}$ has a forced β given by

$$\beta_{\text{forced}} = \beta \frac{e^{V_{CE\text{sat}}/V_T} - I_{SC}/I_S}{e^{V_{CE\text{sat}}/V_T} + \beta I_{SC}/I_S}$$

Find β_{forced} for $\beta = 100$, $I_{SC}/I_S = 100$, and $V_{CE\text{sat}} = 0.2$ V.
Ans. 22.2

6.1.5 The *pnp* Transistor

The *pnp* transistor operates in a manner similar to that of the *npn* device described above. Figure 6.10 shows a *pnp* transistor biased to operate in the active mode. Here the voltage V_{EB} causes the *p*-type emitter to be higher in potential than the *n*-type base, thus forward-biasing the emitter–base junction. The collector–base junction is reverse biased by the voltage V_{BC}, which keeps the *p*-type collector lower in potential than the *n*-type base.

Unlike the *npn* transistor, current in the *pnp* device is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage V_{EB}. Since the component of emitter current contributed by electrons injected from base to emitter is kept small by using a lightly doped base, most of the emitter current will be due to holes. The electrons injected from base to emitter give rise to the first component of base current, i_{B1}. Also, a number of the holes injected into the base will recombine with the majority carriers in the base (electrons) and will thus be lost. The disappearing base electrons will have to be replaced from the external circuit, giving rise to the second component of base current, i_{B2}. The holes that succeed in reaching the boundary of the depletion region of the collector–base junction will be attracted by the negative voltage on the collector. Thus these holes will be swept across the depletion region into the collector and appear as collector current.

It can easily be seen from the above description that the current–voltage relationship of the *pnp* transistor will be identical to that of the *npn* transistor except that v_{BE} has to be replaced by v_{EB}. Also, the large-signal, active-mode operation of the *pnp* transistor can be modeled by any of four equivalent circuits similar to those for the *npn* transistor in Fig. 6.5. Two of these four circuits are shown in Fig. 6.11. Finally, we note that the *pnp* transistor can operate in the saturation mode in a manner analogous to that described for the *npn* device.

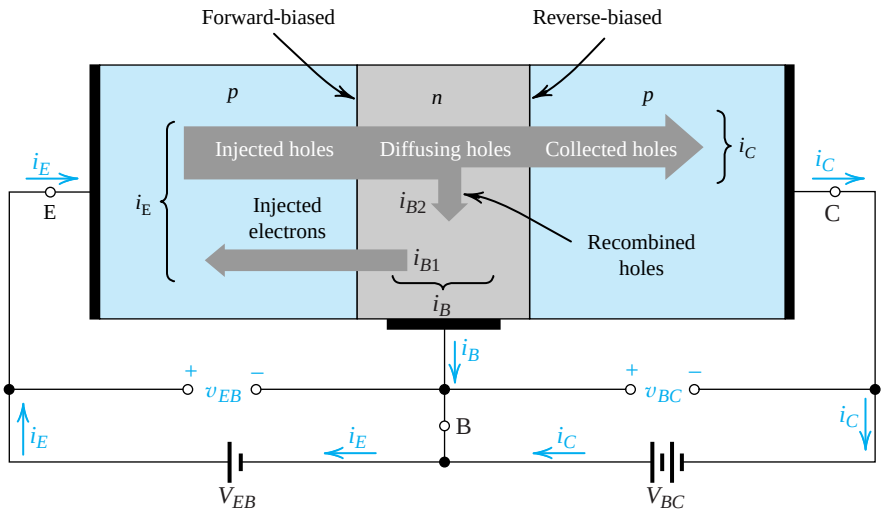


Figure 6.10 Current flow in a *pnp* transistor biased to operate in the active mode.

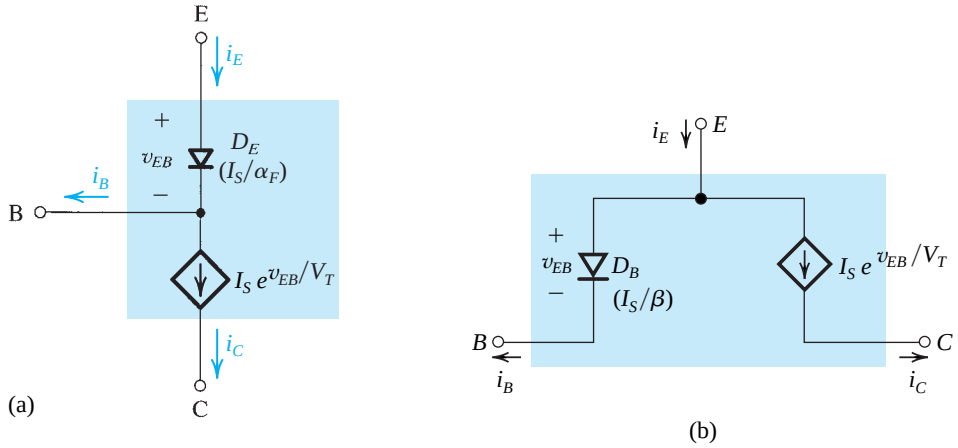


Figure 6.11 Two large-signal models for the *pnp* transistor operating in the active mode.

EXERCISES

6.10 Consider the model in Fig. 6.11(a) applied in the case of a *pnp* transistor whose base is grounded, the emitter is fed by a constant-current source that supplies a 2-mA current into the emitter terminal, and the collector is connected to a −10-V dc supply. Find the emitter voltage, the base current, and the collector current if for this transistor $\beta = 50$ and $I_S = 10^{-14}$ A.
Ans. 0.650 V; 39.2 μA; 1.96 mA

6.11 For a *pnp* transistor having $I_S = 10^{-11}$ A and $\beta = 100$, calculate v_{EB} for $i_C = 1.5$ A.
Ans. 0.643 V

6.2 Current–Voltage Characteristics

6.2.1 Circuit Symbols and Conventions

The physical structure used thus far to explain transistor operation is rather cumbersome to employ in drawing the schematic of a multitransistor circuit. Fortunately, a very descriptive and convenient circuit symbol exists for the BJT. Figure 6.12(a) shows the symbol for the *npn* transistor; the *pnp* symbol is given in Fig. 6.12(b). In both symbols the emitter is distinguished by an arrowhead. This distinction is important because, as we have seen in the last section, practical BJTs are not symmetric devices.

The polarity of the device—*npn* or *pnp*—is indicated by the direction of the arrowhead on the emitter. This arrowhead points in the direction of normal current flow in the emitter, which is also the forward direction of the base–emitter junction. Since we have adopted a drawing convention by which currents flow from top to bottom, we will always draw *pnp* transistors in the manner shown in Fig. 6.12(b) (i.e., with their emitters on top).

Figure 6.13 shows *npn* and *pnp* transistors biased to operate in the active mode. It should be mentioned in passing that the biasing arrangement shown, utilizing two dc voltage sources,

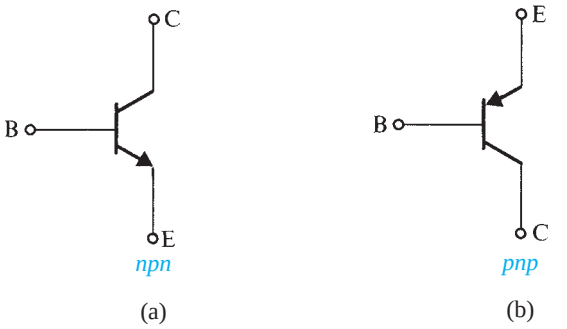


Figure 6.12 Circuit symbols for BJTs.

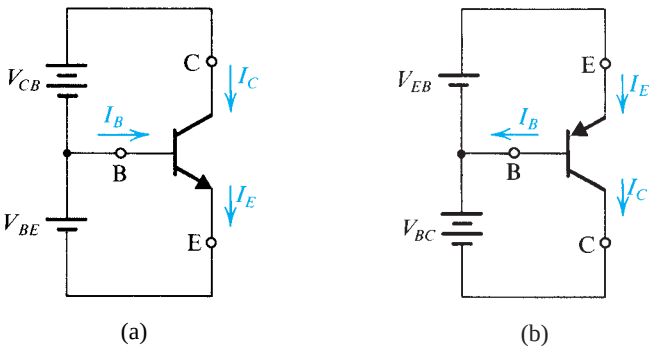


Figure 6.13 Voltage polarities and current flow in transistors biased in the active mode.

is not a usual one and is used here merely to illustrate operation. Practical biasing schemes will be presented in Section 6.7. Figure 6.13 also indicates the reference and actual directions of current flow throughout the transistor. Our convention will be to take the reference direction to coincide with the normal direction of current flow. Hence, normally, we should not encounter a negative value for i_E, i_B, or i_C.

The convenience of the circuit-drawing convention that we have adopted should be obvious from Fig. 6.13. Note that currents flow from top to bottom and that voltages are higher at the top and lower at the bottom. The arrowhead on the emitter also implies the polarity of the emitter–base voltage that should be applied in order to forward bias the emitter–base junction. Just a glance at the circuit symbol of the *pnp* transistor, for example, indicates that we should make the emitter higher in voltage than the base (by v_{EB}) in order to cause current to flow into the emitter (downward). Note that the symbol v_{EB} means the voltage by which the emitter (E) is higher than the base (B). Thus for a *pnp* transistor operating in the active mode v_{EB} is positive, while in an *npn* transistor v_{BE} is positive.

From the discussion of Section 6.1 it follows that an *npn* transistor whose EBJ is forward biased will operate in the active mode *as long as the collector voltage does not fall below that of the base by more than approximately 0.4 V*. Otherwise, the transistor leaves the active mode and enters the saturation region of operation.[6]

Table 6.2 Summary of the BJT Current–Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1-\alpha) i_E = \frac{i_E}{\beta+1}$$

$$i_C = \beta i_B \qquad i_E = (\beta+1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

V_T = thermal voltage $= \dfrac{kT}{q} \simeq 25$ mV at room temperature

In a parallel manner, the *pnp* transistor will operate in the active mode *if the EBJ is forward biased and the collector voltage is not allowed to rise above that of the base by more than 0.4 V or so*. Otherwise, the CBJ becomes forward biased, and the *pnp* transistor enters the saturation region of operation.

For easy reference, we present in Table 6.2 a summary of the BJT current–voltage relationships in the active mode of operation.

The Collector–Base Reverse Current (I_{CBO}) In our discussion of current flow in transistors we ignored the small reverse currents carried by thermally generated minority carriers. Although such currents can be safely neglected in modern transistors, the reverse current across the collector–base junction deserves some mention. This current, denoted I_{CBO}, is the reverse current flowing from collector to base with the emitter open-circuited (hence the subscript *O*). This current is usually in the nanoampere range, a value that is many times higher than its theoretically predicted value. As with the diode reverse current, I_{CBO} contains a substantial leakage component, and its value is dependent on v_{CB}. I_{CBO} depends strongly on temperature, approximately doubling for every 10°C rise.[7]

[6] It is interesting to contrast the active-mode operation of the BJT with the corresponding mode of operation of the MOSFET: The BJT needs a minimum v_{CE} of about 0.3 V, and the MOSFET needs a minimum v_{DS} equal to V_{OV}, which for modern technologies is in the range 0.2 V to 0.3 V. Thus we see a great deal of similarity! Also note that reverse biasing the CBJ of the BJT corresponds to pinching off the channel of the MOSFET. This condition results in the collector current (drain current in the MOSFET) being independent of the collector voltage (the drain voltage in the MOSFET).

[7] The temperature coefficient of I_{CBO} is different from that of I_S because I_{CBO} contains a substantial leakage component.

Example 6.2

The transistor in the circuit of Fig. 6.14(a) has $\beta = 100$ and exhibits a v_{BE} of 0.7 V at $i_C = 1$ mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.

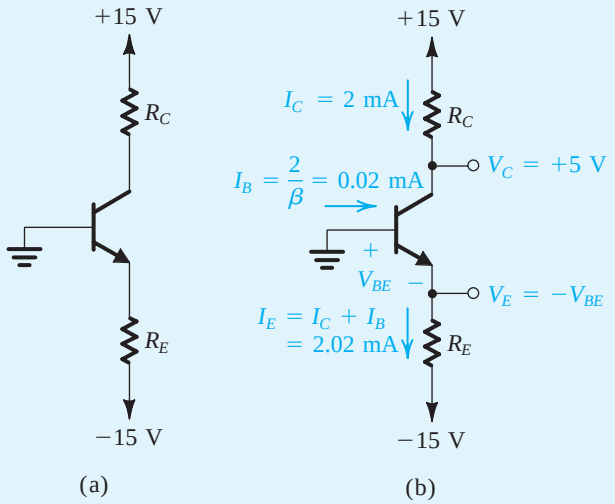


Figure 6.14 Circuit for Example 6.2.

Solution

Refer to Fig. 6.14(b). We note at the outset that since we are required to design for $V_C = +5$ V, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage $V_C = +5$ V, the voltage drop across R_C must be 15 – 5 = 10 V. Now, since $I_C = 2$ mA, the value of R_C should be selected according to

$$R_C = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since $v_{BE} = 0.7$ V at $i_C = 1$ mA, the value of v_{BE} at $i_C = 2$ mA is

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.717 \text{ V}$$

Since the base is at 0 V, the emitter voltage should be

$$V_E = -0.717 \text{ V}$$

For $\beta = 100$, $\alpha = 100/101 = 0.99$. Thus the emitter current should be

$$I_E = \frac{I_C}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

Now the value required for R_E can be determined from

$$R_E = \frac{V_E - (-15)}{I_E}$$

$$= \frac{-0.717 + 15}{2.02} = 7.07 \text{ k}\Omega$$

This completes the design. We should note, however, that the calculations above were made with a degree of precision that is usually neither necessary nor justified in practice in view, for instance, of the expected tolerances of component values. Nevertheless, we chose to do the design precisely in order to illustrate the various steps involved.

EXERCISES

D6.12 Repeat Example 6.2 for a transistor fabricated in a modern integrated-circuit process. Such a process yields devices that exhibit larger v_{BE} at the same i_C because they have much smaller junction areas. The dc power supplies utilized in modern IC technologies fall in the range of 1 V to 3 V. Design a circuit similar to that shown in Fig. 6.14 except that now the power supplies are ±1.5 V and the BJT has $\beta = 100$ and exhibits v_{BE} of 0.8 V at $i_C = 1$ mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +0.5 V appears at the collector.
Ans. $R_C = 500\ \Omega$; $R_E = 338\ \Omega$

6.13 In the circuit shown in Fig. E6.13, the voltage at the emitter was measured and found to be –0.7 V. If $\beta = 50$, find I_E, I_B, I_C, and V_C.

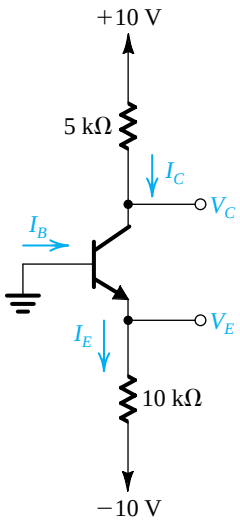


Figure E6.13

Ans. 0.93 mA; 18.2 μA; 0.91 mA; +5.45 V

6.14 In the circuit shown in Fig. E6.14, measurement indicates V_B to be +1.0 V and V_E to be +1.7 V. What are α and β for this transistor? What voltage V_C do you expect at the collector?

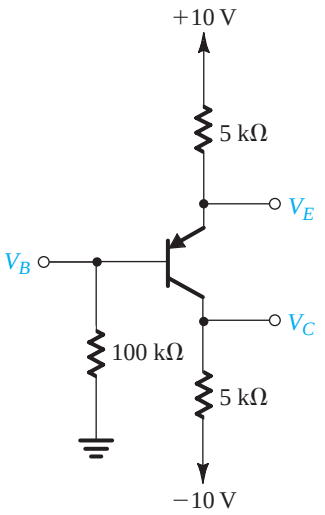


Figure E6.14

Ans. 0.994; 165; –1.75 V

6.2.2 Graphical Representation of Transistor Characteristics

It is sometimes useful to describe the transistor i–v characteristics graphically. Figure 6.15 shows the i_C–v_{BE} characteristic, which is the exponential relationship

$$i_C = I_S e^{v_{BE}/V_T}$$

which is identical to the diode i–v relationship. The i_E–v_{BE} and i_B–v_{BE} characteristics are also exponential but with different scale currents: I_S/α for i_E, and I_S/β for i_B. Since the constant of the exponential characteristic, $1/V_T$, is quite high ($\simeq 40$), the curve rises very sharply. For v_{BE} smaller than about 0.5 V, the current is negligibly small.[8] Also, over most of the normal current range v_{BE} lies in the range of 0.6 V to 0.8 V. In performing rapid first-order dc calculations, we normally will assume that $V_{BE} \simeq 0.7$ V, which is similar to the approach used in the analysis of diode circuits (Chapter 4). For a *pnp* transistor, the i_C–v_{EB} characteristic will look identical to that of Fig. 6.15 with v_{BE} replaced with v_{EB}.

As in silicon diodes, the voltage across the emitter–base junction decreases by about 2 mV for each rise of 1°C in temperature, provided the junction is operating at a constant current. Figure 6.16 illustrates this temperature dependence by depicting i_C–v_{BE} curves for an *npn* transistor at three different temperatures.

[8]The i_C–v_{BE} characteristic is the BJT's counterpart of the i_D–v_{GS} characteristic of the MOSFET. They share an important attribute: In both cases the voltage has to exceed a "threshold" for the device to conduct appreciably. In the case of the MOSFET, there is a formal threshold voltage, V_t, which lies typically in the range of 0.4 V to 0.8 V. For the BJT, there is an "apparent threshold" of approximately 0.5 V. The i_D–v_{GS} characteristic of the MOSFET is parabolic, and thus is less steep than the i_C–v_{BE} characteristic of the BJT. This difference has a direct and significant implication for the value of transconductance g_m realized with each device.

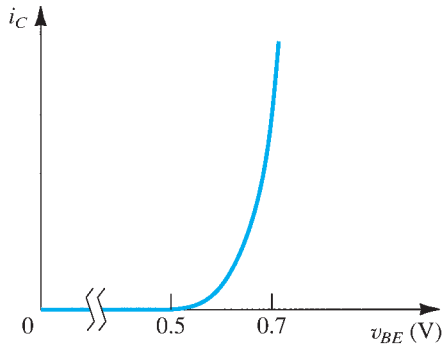


Figure 6.15 The i_C–v_{BE} characteristic for an *npn* transistor.

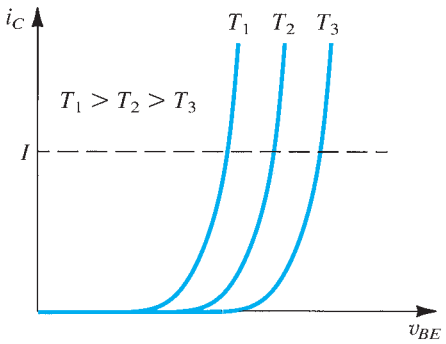


Figure 6.16 Effect of temperature on the i_C–v_{BE} characteristic. At a constant emitter current (broken line), v_{BE} changes by –2 mV/°C.

EXERCISE

6.15 Consider a *pnp* transistor with $v_{EB} = 0.7$ V at $i_E = 1$ mA. Let the base be grounded, the emitter be fed by a 2-mA constant-current source, and the collector be connected to a –5-V supply through a 1-kΩ resistance. If the temperature increases by 30°C, find the changes in emitter and collector voltages. Neglect the effect of I_{CBO}.
Ans. –60 mV; 0 V.

6.2.3 Dependence of i_C on the Collector Voltage—The Early Effect

When operated in the active region, practical BJTs show some dependence of the collector current on the collector voltage, with the result that, unlike the graph shown in Fig. 6.8, their i_C–v_{CB} characteristics are not perfectly horizontal straight lines. To see this dependence more clearly, consider the conceptual circuit shown in Fig. 6.17(a). The transistor is connected in

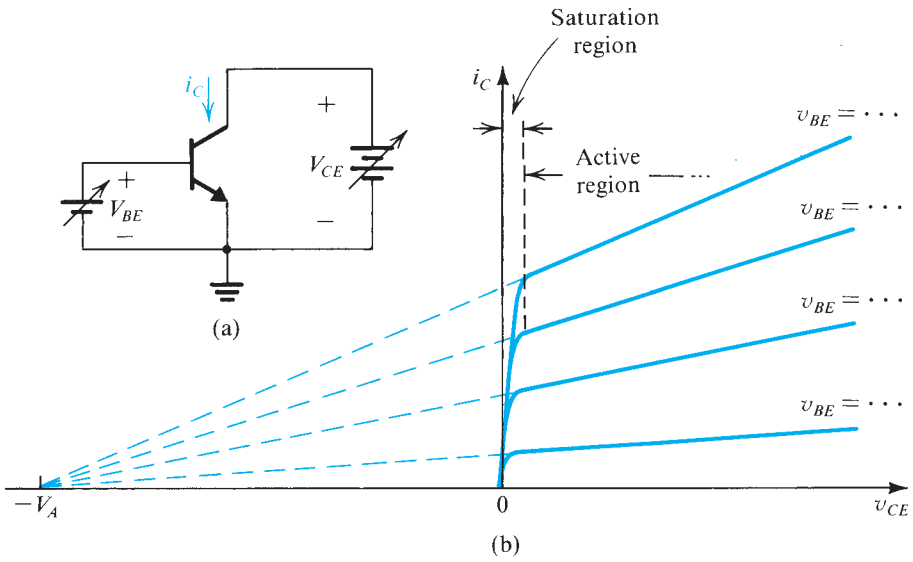


Figure 6.17 **(a)** Conceptual circuit for measuring the i_C–v_{CE} characteristics of the BJT. **(b)** The i_C–v_{CE} characteristics of a practical BJT.

the **common-emitter configuration**; that is, here the emitter serves as a common terminal between the input and output ports. The voltage V_{BE} can be set to any desired value by adjusting the dc source connected between base and emitter. At each value of V_{BE}, the corresponding i_C–v_{CE} characteristic curve can be measured point by point by varying the dc source connected between collector and emitter and measuring the corresponding collector current. The result is the family of i_C–v_{CE} characteristic curves shown in Fig. 6.17(b) and known as **common-emitter characteristics**.

At low values of v_{CE} (lower than about 0.3 V), as the collector voltage goes below that of the base by more than 0.4 V, the collector–base junction becomes forward biased and the transistor leaves the active mode and enters the saturation mode. Shortly, we shall look at the details of the i_C–v_{CE} curves in the saturation region. At this time, however, we wish to examine the characteristic curves in the active region in detail. We observe that the characteristic curves, though still straight lines, have finite slope. In fact, when extrapolated, the characteristic lines meet at a point on the negative v_{CE} axis, at $v_{CE} = -V_A$. The voltage V_A, a positive number, is a parameter for the particular BJT, with typical values in the range of 10 V to 100 V. It is called the **Early voltage**, after J. M. Early, the engineering scientist who first studied this phenomenon.

At a given value of v_{BE}, increasing v_{CE} increases the reverse-bias voltage on the collector–base junction, and thus increases the width of the depletion region of this junction (refer to Fig. 6.3). This in turn results in a decrease in the **effective base width** W. Recalling that I_S is inversely proportional to W (Eq. 6.4), we see that I_S will increase and that i_C increases proportionally. This is the Early effect. For obvious reasons, it is also known as the **base-width moduation effect**.[9]

[9] Recall that the MOSFET's counterpart is the channel-length modulation effect. These two effects are remarkably similar and have been assigned the same name, Early effect.

The linear dependence of i_C on v_{CE} can be explicitly accounted for by assuming that I_S remains constant and including the factor $(1 + v_{CE}/V_A)$ in the equation for i_C as follows:

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right) \tag{6.18}$$

The nonzero slope of the i_C–v_{CE} straight lines indicates that the **output resistance** looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o \equiv \left[\left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}\ =\ \text{constant}}\right]^{-1} \tag{6.19}$$

Using Eq. (6.18) we can show that

$$r_o = \frac{V_A + V_{CE}}{I_C} \tag{6.20}$$

where I_C and V_{CE} are the coordinates of the point at which the BJT is operating on the particular i_C–v_{CE} curve (i.e., the curve obtained for v_{BE} equal to constant value V_{BE} at which Eq. (6.19) is evaluated). Alternatively, we can write

$$r_o = \frac{V_A}{I'_C} \tag{6.21}$$

where I'_C is the value of the collector current with the Early effect neglected; that is,

$$I'_C = I_S e^{V_{BE}/V_T} \tag{6.22}$$

It is rarely necessary to include the dependence of i_C on v_{CE} in dc bias design and analysis that is performed by hand. Such an effect, however, can be easily included in the SPICE simulation of circuit operation, which is frequently used to "fine-tune" pencil-and-paper analysis or design.

The finite output resistance r_o can have a significant effect on the gain of transistor amplifiers. This is particularly the case in integrated–circuit amplifiers, as will be shown in chapter 7. Fortunately, there are many situations in which r_o can be included relatively easily in pencil-and-paper analysis.

The output resistance r_o can be included in the circuit model of the transistor. This is illustrated in Fig. 6.18, where we show the two large-signal circuit models of a common-emitter *npn* transistor operating in the active mode, those in Fig 6.5(c) and (d), with the resistance r_o connected between the collector and the emitter terminals.

EXERCISES

6.16 Use the circuit model in Fig. 6.18(a) to express I_C in terms of e^{v_{BE}/V_T} and v_{CE} and thus show that this circuit is a direct representation of Eq. (6.18).

6.17 Find the output resistance of a BJT for which $V_A = 100$ V at $I_C = 0.1$, 1, and 10 mA.
Ans. 1 MΩ; 100 kΩ; 10 kΩ

6.18 Consider the circuit in Fig. 6.17(a). At $V_{CE} = 1$ V, V_{BE} is adjusted to yield a collector current of 1 mA. Then, while V_{BE} is kept constant, V_{CE} is raised to 11 V. Find the new value of I_C. For this transistor, $V_A = 100$ V.
Ans. 1.1 mA

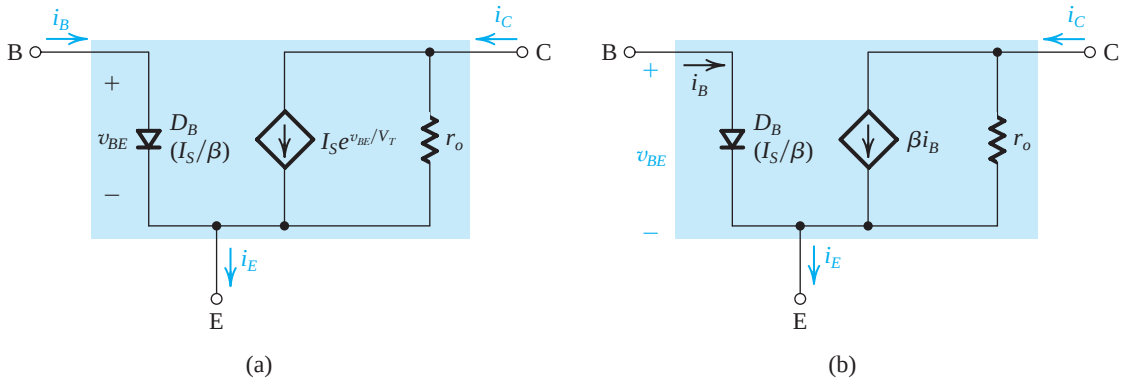


Figure 6.18 Large-signal equivalent-circuit models of an *npn* BJT operating in the active mode in the common-emitter configuration with the output resistance r_o included.

6.2.4 An Alternative Form of the Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in Fig. 6.19. Here the base current i_B rather than the base–emitter voltage v_{BE} is used as a parameter. That is, each i_C–v_{CE} curve is measured with the base fed with a constant current I_B. The resulting characteristics, shown in Fig. 6.19(b), look similar to those in Fig. 6.17. Figure 6.19(c) shows an expanded view of the characteristics in the saturation region.

The Common-Emitter Current Gain β In the active region of the characteristics shown in Fig. 6.19(b) we have identified a particular point Q. Note that this operating point for the transistor is characterized by a base current I_B, a collector current I_C, and a collector–emitter voltage V_{CE}. The ratio I_C/I_B is the transistor β. However, there is another way to measure β: change the base current by an increment Δi_B and measure the resulting increment Δi_C, while keeping V_{CE} constant. This is illustrated in Fig. 6.19(b). The ratio $\Delta i_C/\Delta i_B$ should, according to our study thus far, yield an identical value for β. It turns out, however, that the latter value of β (called *incremental*, or ac, β) is a little different from the dc β (i.e., I_C/I_B). Such a distinction, however, is too subtle for our needs in this book. We shall use β to denote both dc and incremental values.[10]

The Saturation Voltage $V_{CE\text{sat}}$ and Saturation Resistance $R_{CE\text{sat}}$ Refer next to the expanded view of the common-emitter characteristics in the saturation region shown in Fig. 6.19(c). The "bunching together" of the curves in the saturation region implies that the incremental β is lower there than in the active region. A possible operating point in the saturation region is that labeled X. It is characterized by a base current I_B, a collector current $I_{C\text{sat}}$, and a collector–emitter voltage $V_{CE\text{sat}}$. From our previous discussion of saturation, recall that $I_{C\text{sat}} = \beta_{\text{forced}} I_B$, where $\beta_{\text{forced}} < \beta$.

The i_C–v_{CE} curves in saturation are rather steep, indicating that the saturated transistor exhibits a low collector-to-emitter resistance $R_{CE\text{sat}}$,

$$R_{CE\text{sat}} \equiv \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{\substack{i_B = I_B \\ i_C = I_{C\text{sat}}}} \tag{6.23}$$

Typically, $R_{CE\text{sat}}$ ranges from a few ohms to a few tens of ohms.

[10] Manufacturers of bipolar transistors use h_{FE} to denote the dc value of β and h_{fe} to denote the incremental β. These symbols come from the *h*-parameter description of two-port networks (see Appendix C), with the subscript *F*(*f*) denoting forward and *E*(*e*) denoting common emitter.

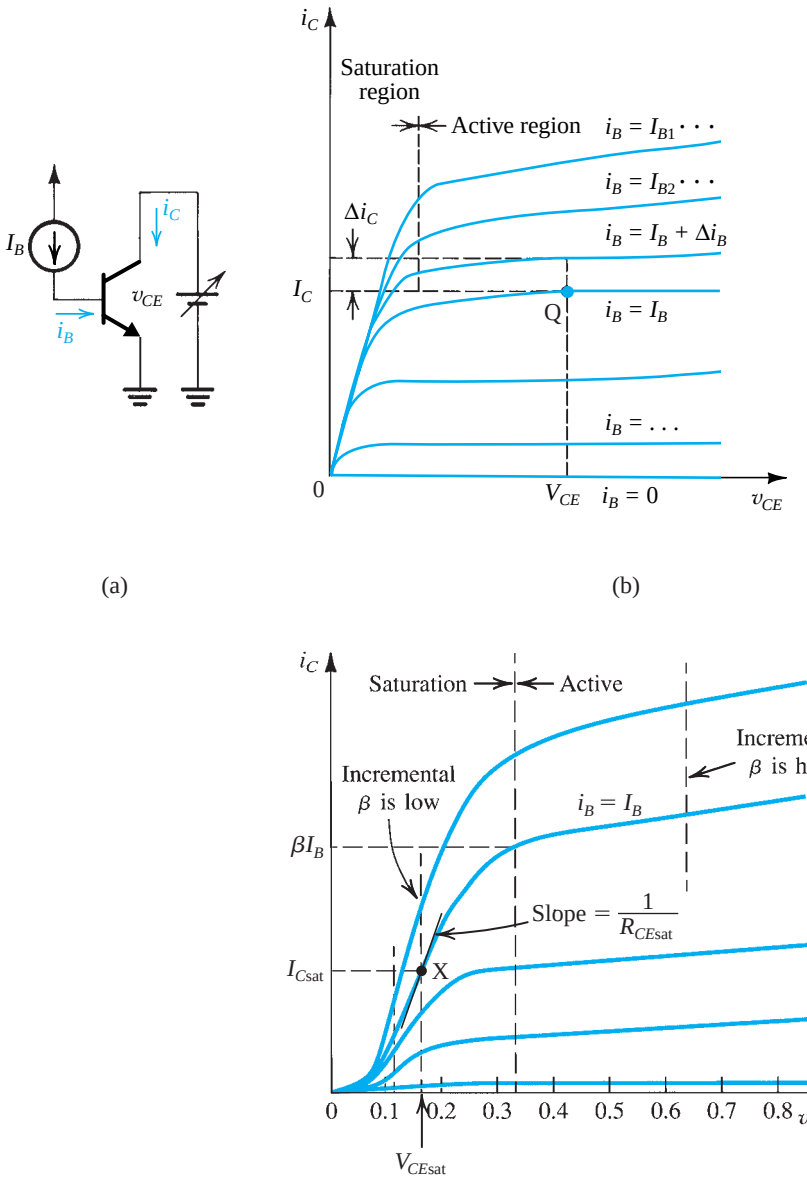


Figure 6.19 Common-emitter characteristics. (**a**) Basic CE circuit; note that in (**b**) the horizontal scale is expanded around the origin to show the saturation region in some detail. A much greater expansion of the saturation region is shown in (**c**).

That the collector-to-emitter resistance of a saturated BJT is small should have been anticipated from the fact that between C and E we now have two forward-conducting diodes in series[11] (see also Fig. 6.9).

[11]In the corresponding mode of operation for the MOSFET, the triode region, the resistance between drain and source is small because it is the resistance of the continuous (non-pinched-off) channel.

A simple model for the saturated BJT is shown in Fig. 6.20. Here V_{BE} is assumed constant (approximately 0.7 V) and V_{CE} also is assumed constant, $V_{CE\text{sat}} \simeq 0.2$ V. That is, we have neglected the small saturation resistance $R_{CE\text{sat}}$ for the sake of making the model simple for hand calculations.

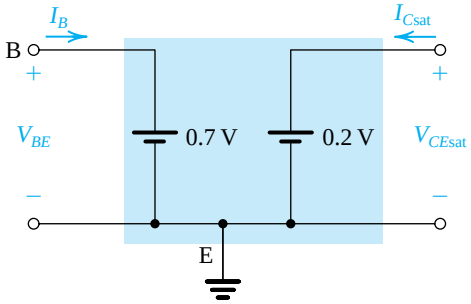


Figure 6.20 A simplified equivalent-circuit model of the saturated transistor.

Example 6.3

For the circuit in Fig. 6.21, it is required to determine the value of the voltage V_{BB} that results in the transistor operating

(a) in the active mode with $V_{CE} = 5$ V
(b) at the edge of saturation
(c) deep in saturation with $\beta_{\text{forced}} = 10$

For simplicity, assume that V_{BE} remains constant at 0.7 V. The transistor β is specified to be 50.

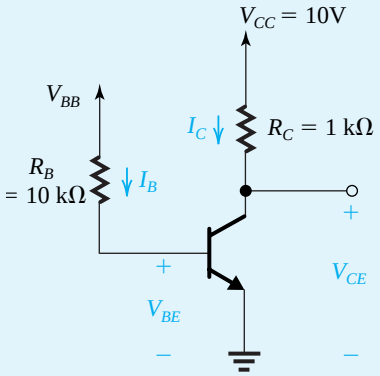


Figure 6.21 Circuit for Example 6.3.

Solution

(a) To operate in the active mode with $V_{CE} = 5$ V,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$= \frac{10 - 5}{1\ \text{k}\Omega} = 5\ \text{mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{5}{50} = 0.1 \text{ mA}$$

Now the required value of V_{BB} can be found as follows:

$$V_{BB} = I_B R_B + V_{BE}$$
$$= 0.1 \times 10 + 0.7 = 1.7 \text{ V}$$

(b) Operation at the edge of saturation is obtained with $V_{CE} = 0.3$ V. Thus

$$I_C = \frac{10 - 0.3}{1} = 9.7 \text{ mA}$$

Since, at the edge of saturation, I_C and I_B are still related by β,

$$I_B = \frac{9.7}{50} = 0.194 \text{ mA}$$

The required value of V_{BB} can be determined as

$$V_{BB} = 0.194 \times 10 + 0.7 = 2.64 \text{ V}$$

(c) To operate deep in saturation,

$$V_{CE} = V_{CE\text{sat}} \simeq 0.2 \text{ V}$$

Thus,

$$I_C = \frac{10 - 0.2}{1} = 9.8 \text{ mA}$$

We then use the value of forced β to determine the required value of I_B as

$$I_B = \frac{I_C}{\beta_{\text{forced}}} = \frac{9.8}{10} = 0.98 \text{ mA}$$

and the required V_{BB} can now be found as

$$V_{BB} = 0.98 \times 10 + 0.7 = 10.5 \text{ V}$$

Observe that once the transistor is in saturation, increasing V_{BB} and thus I_B results in negligible change in I_C since $V_{CE\text{sat}}$ will change only slightly. Thus I_C is said to *saturate*, which is the origin of the name "saturation mode of operation."

EXERCISES

6.19 Repeat Example 6.3 for $R_C = 10\ \text{k}\Omega$.
Ans. 0.8 V; 0.894 V; 1.68 V

6.20 For the circuit in Fig. 6.21, find V_{CE} for $V_{BB} = 0$ V.
Ans. + 10 V

6.21 For the circuit in Fig. 6.21, let V_{BB} be set to the value obtained in Example 6.3, part (a), namely, $V_{BB} = 1.7$ V. Verify that the transistor is indeed operating in the active mode. Now, while keeping V_{BB} constant, find that value to which R_C should be increased in order to obtain (a) operation at the edge of saturation, and (b) operation deep in saturation with $\beta_{\text{forced}} = 10$.
Ans. (a) 1.94 kΩ; (b) 9.8 kΩ

6.3 BJT Circuits at DC

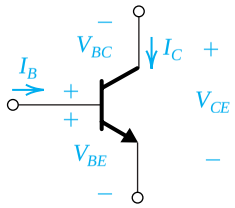
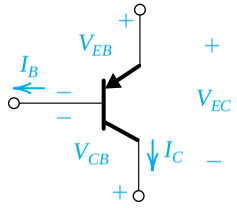
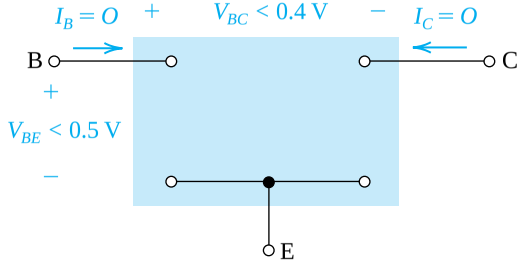
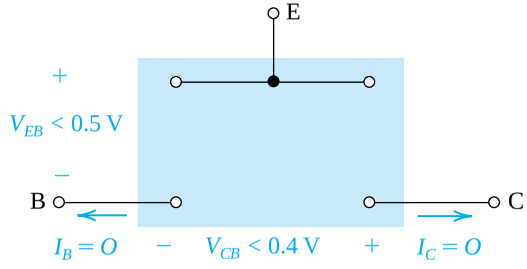
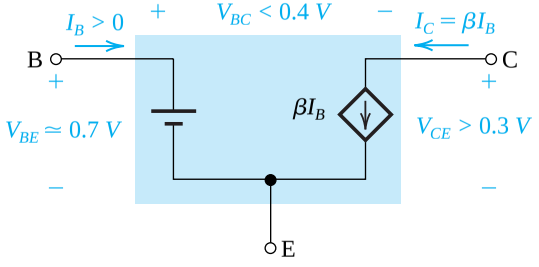
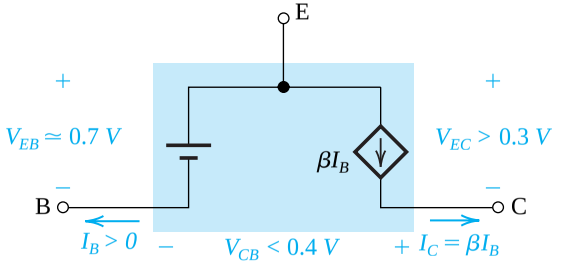
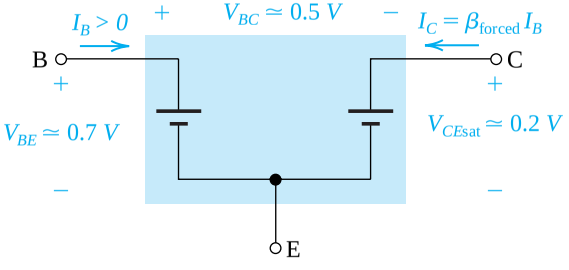
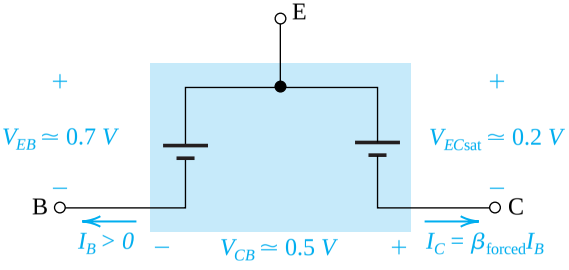
We are now ready to consider the analysis of BJT circuits to which only dc voltages are applied. In the following examples we will use the simple model in which $|V_{BE}|$ of a conducting transistor is 0.7 V and $|V_{CE}|$ of a saturated transistor is 0.2 V, and we will neglect the Early effect. Better models can, of course, be used to obtain more accurate results. This, however, is usually achieved at the expense of speed of analysis, and more importantly, it could impede the circuit designer's ability to gain insight regarding circuit behavior. Accurate results using elaborate models can be obtained using circuit simulation with SPICE. This is almost always done in the final stages of a design and certainly before circuit fabrication. Computer simulation, however, is not a substitute for quick pencil-and-paper circuit analysis, an essential ability that aspiring circuit designers must muster. The following series of examples is a step in that direction.

As will be seen, in analyzing a circuit the first question that one must answer is: *In which mode is the transistor operating*? In some cases, the answer will be obvious. For instance, a quick check of the terminal voltages will indicate whether the transistor is cut off or conducting. If it is conducting, we have to determine whether it is operating in the active mode or in saturation. In some cases, however, this may not be obvious. Needless to say, as the reader gains practice and experience in transistor circuit analysis and design, the answer will be apparent in a much larger proportion of problems. The answer, however, can always be determined by utilizing the following procedure:

Assume that the transistor is operating in the active mode, and proceed to determine the various voltages and currents that correspond. Then check for consistency of the results with the assumption of active-mode operation; that is, is v_{CB} of an *npn* transistor greater than –0.4 V (or v_{CB} of a *pnp* transistor lower than 0.4 V)? If the answer is yes, then our task is complete. If the answer is no, assume saturation-mode operation, and proceed to determine currents and voltages and then to check for consistency of the results with the assumption of saturation-mode operation. Here the test is usually to compute the ratio I_C/I_B and to verify that it is lower than the transistor β (i.e., $\beta_{\text{forced}} < \beta$). Since β for a given transistor type varies over a wide range,[12] one must use the lowest specified β for this test. Finally, note that the order of these two assumptions can be reversed. As a further aid to the reader, we provide in Table 6.3 a summary of the conditions and models for the operation of the BJT in its three possible modes.

[12]That is, if one buys BJTs of a certain part number, the manufacturer guarantees only that their values of β fall within a certain range, say 50 to 150.

Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes

	npn	*pnp*
		
Cutoff EJB: Reverse Biased CBJ: Reverse Biased		
Active EBJ: Forward Biased CBJ: Reverse Biased		
Saturation EBJ: Forward Biased CBJ: Forward Biased		

Example 6.4

Consider the circuit shown in Fig. 6.22(a), which is redrawn in Fig. 6.22(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100.

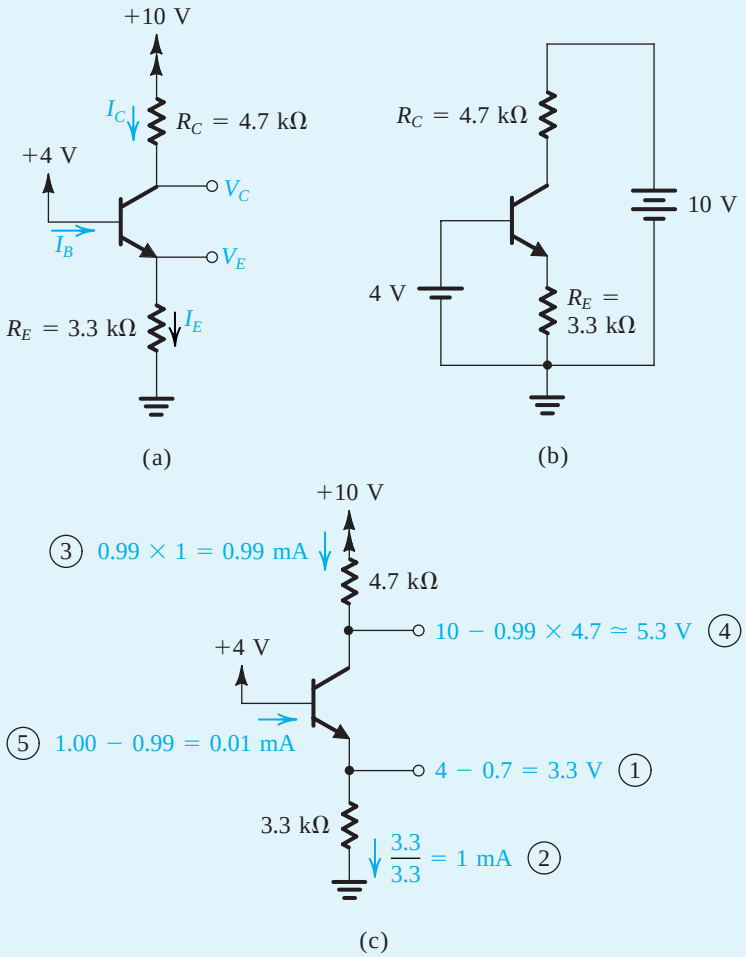


Figure 6.22 Analysis of the circuit for Example 6.4: **(a)** circuit; **(b)** circuit redrawn to remind the reader of the convention used in this book to show connections to the power supply; **(c)** analysis with the steps numbered.

Solution

Glancing at the circuit in Fig. 6.22(a), we note that the base is connected to +4 V and the emitter is connected to ground through a resistance R_E. Therefore, it is safe to conclude that the base–emitter junction

will be forward biased. Assuming that this is the case and assuming that V_{BE} is approximately 0.7 V, it follows that the emitter voltage will be

$$V_E = 4 - V_{BE} \simeq 4 - 0.7 = 3.3 \text{ V}$$

We are now in an opportune position; we know the voltages at the two ends of R_E and thus can determine the current I_E through it,

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

Since the collector is connected through R_C to the +10-V power supply, it appears possible that the collector voltage will be higher than the base voltage, which implies active-mode operation. Assuming that this is the case, we can evaluate the collector current from

$$I_C = \alpha I_E$$

The value of α is obtained from

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \simeq 0.99$$

Thus I_C will be given by

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

We are now in a position to use Ohm's law to determine the collector voltage V_C,

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \simeq +5.3 \text{ V}$$

Since the base is at +4 V, the collector–base junction is reverse biased by 1.3 V, and the transistor is indeed in the active mode as assumed.

It remains only to determine the base current I_B, as follows:

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \simeq 0.01 \text{ mA}$$

Before leaving this example we wish to emphasize strongly the value of carrying out the analysis directly on the circuit diagram. Only in this way will one be able to analyze complex circuits in a reasonable length of time. Figure 6.22(c) illustrates the above analysis on the circuit diagram, with the order of the analysis steps indicated by the circled numbers.

Example 6.5

We wish to analyze the circuit of Fig. 6.23(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 6.22 except that the voltage at the base is now +6 V. Assume that the transistor β is specified to be *at least* 50.

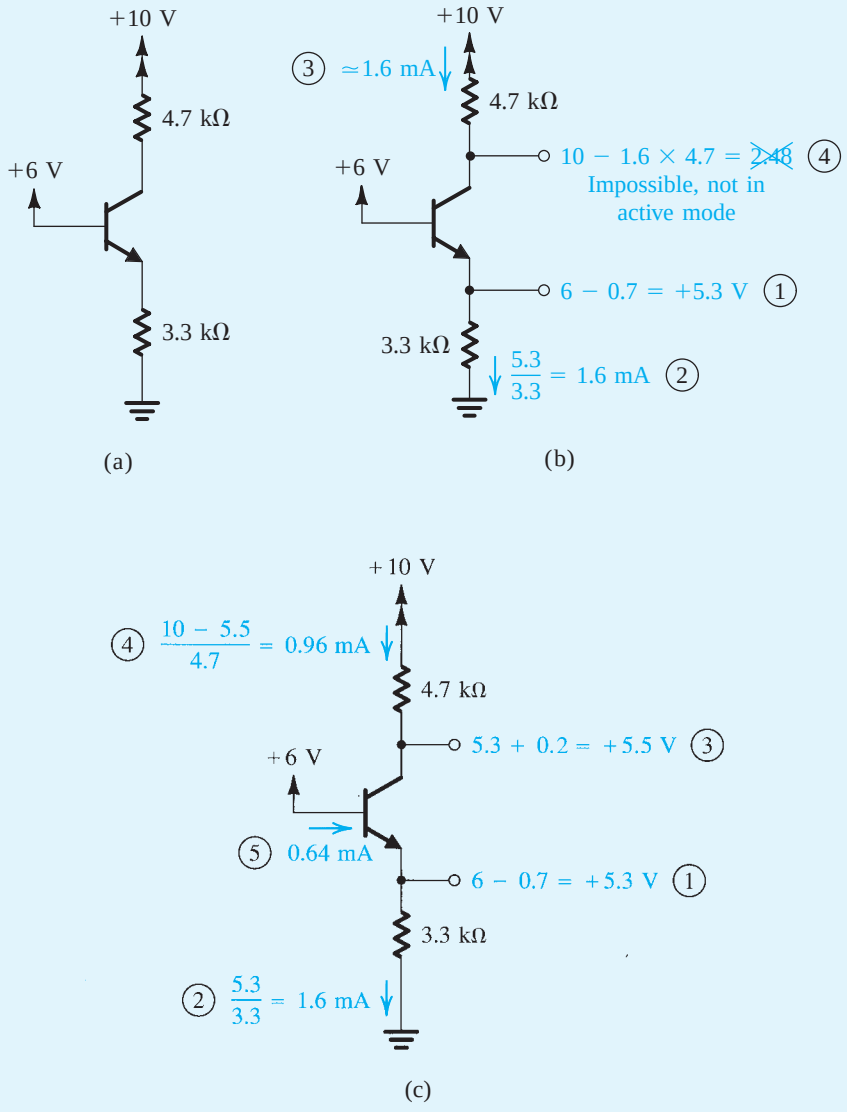


Figure 6.23 Analysis of the circuit for Example 6.5. Note that the circled numbers indicate the order of the analysis steps.

Solution

With +6 V at the base, the base–emitter junction will be forward biased; thus,

$$V_E = +6 - V_{BE} \simeq 6 - 0.7 = 5.3 \text{ V}$$

and

$$I_E = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

Now, assuming active-mode operation, $I_C = \alpha I_E \simeq I_E$; thus,

$$V_C = +10 - 4.7 \times I_C \simeq 10 - 7.52 = 2.48 \text{ V}$$

The details of the analysis performed above are illustrated in Fig. 6.23(b).

Since the collector voltage calculated appears to be less than the base voltage by 3.52 V, it follows that our original assumption of active-mode operation is incorrect. In fact, the transistor has to be in the *saturation* mode. Assuming this to be the case, the values of V_E and I_E will remain unchanged. The collector voltage, however, becomes

$$V_C = V_E + V_{CE\text{sat}} \simeq +5.3 + 0.2 = +5.5 \text{ V}$$

from which we can determine I_C as

$$I_C = \frac{+10 - 5.5}{4.7} = 0.96 \text{ mA}$$

and I_B can now be found as

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA}$$

Thus the transistor is operating at a forced β of

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

Since β_{forced} is less than the *minimum* specified value of β, the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of β should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified β. Obviously, if a transistor with this minimum β is saturated, then transistors with higher values of β will also be saturated. The details of the analysis are shown in Fig. 6.23(c), where the order of the steps used is indicated by the circled numbers.

Example 6.6

We wish to analyze the circuit in Fig. 6.24(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that considered in Examples 6.4 and 6.5 except that now the base voltage is zero.

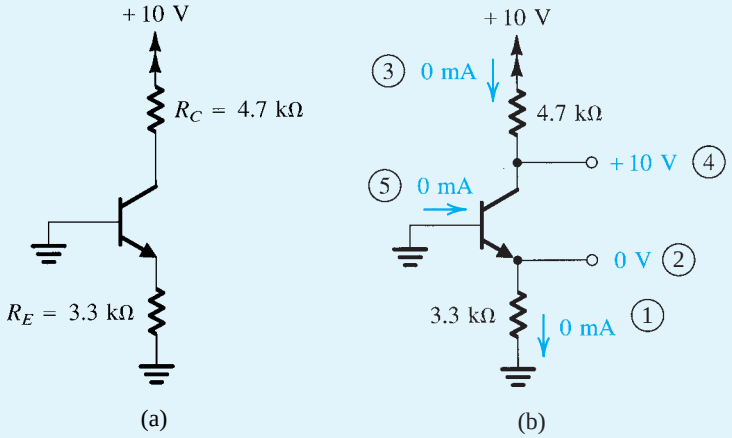


Figure 6.24 Example 6.6: **(a)** circuit; **(b)** analysis, with the order of the analysis steps indicated by circled numbers.

Solution

Since the base is at zero volts and the emitter is connected to ground through R_E, the base–emitter junction cannot conduct and the emitter current is zero. Note that this situation will obtain as long as the voltage at the base is less than 0.5 V or so. Also, the collector–base junction cannot conduct, since the *n*-type collector is connected through R_C to the positive power supply while the *p*-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the *cutoff* mode of operation.

The emitter voltage will be zero, while the collector voltage will be equal to +10 V, since the voltage drops across R_E and R_C are zero. Figure 6.24(b) shows the analysis details.

EXERCISES

D6.22 For the circuit in Fig. 6.22(a), find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume $\alpha \simeq 1$.
Ans. +4.7 V

D6.23 Redesign the circuit of Fig. 6.22(a) (i.e., find new values for R_E and R_C) to establish a collector current of 0.5 mA and a reverse-bias voltage on the collector–base junction of 2 V. Assume $\alpha \simeq 1$.
Ans. $R_E = 6.6$ kΩ; $R_C = 8$ kΩ

6.24 For the circuit in Fig. 6.23(a), find the value to which the base voltage should be changed so that the transistor operates in saturation with a forced β of 5.
Ans. +5.18 V

Example 6.7

We want to analyze the circuit of Fig. 6.25(a) to determine the voltages at all nodes and the currents through all branches.

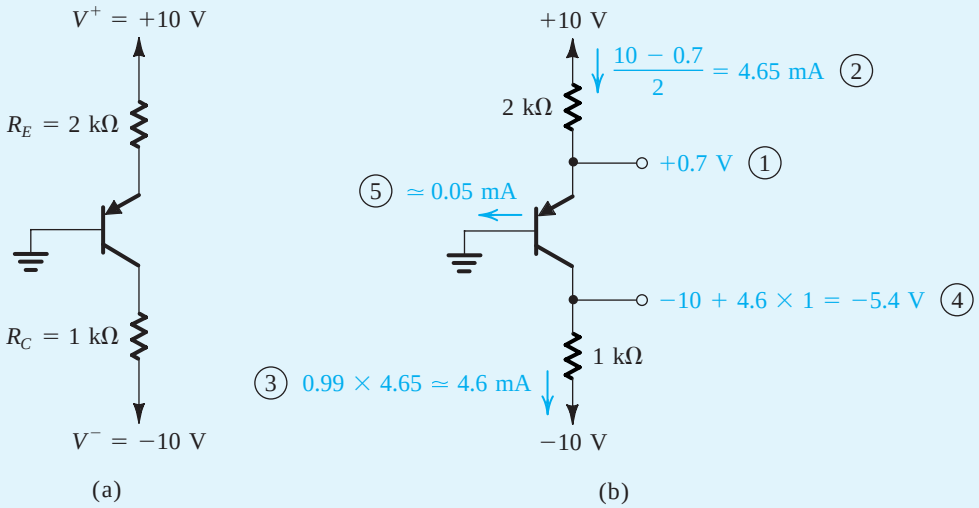


Figure 6.25 Example 6.7: **(a)** circuit; **(b)** analysis, with the steps indicated by circled numbers.

Solution

The base of this *pnp* transistor is grounded, while the emitter is connected to a positive supply ($V^+ = +10$ V) through R_E. It follows that the emitter–base junction will be forward biased with

$$V_E = V_{EB} \simeq 0.7 \text{ V}$$

Thus the emitter current will be given by

$$I_E = \frac{V^+ - V_E}{R_E} = \frac{10 - 0.7}{2} = 4.65 \text{ mA}$$

Since the collector is connected to a negative supply (more negative than the base voltage) through R_C, it is *possible* that this transistor is operating in the active mode. Assuming this to be the case, we obtain

$$I_C = \alpha I_E$$

Since no value for β has been given, we shall assume $\beta = 100$, which results in $\alpha = 0.99$. Since large variations in β result in small differences in α, this assumption will not be critical as far as determining the value of I_C is concerned. Thus,

$$I_C = 0.99 \times 4.65 = 4.6 \text{ mA}$$

The collector voltage will be

$$\begin{aligned} V_C &= V^- + I_C R_C \\ &= -10 + 4.6 \times 1 = -5.4 \text{ V} \end{aligned}$$

Thus the collector–base junction is reverse biased by 5.4 V, and the transistor is indeed in the active mode, which supports our original assumption.

It remains only to calculate the base current,

$$I_B = \frac{I_E}{\beta + 1} = \frac{4.65}{101} \simeq 0.05 \text{ mA}$$

Obviously, the value of β critically affects the base current. Note, however, that in this circuit the value of β will have no effect on the mode of operation of the transistor. Since β is generally an ill-specified parameter, this circuit represents a good design. As a rule, one should strive to *design the circuit such that its performance is as insensitive to the value of β as possible.* The analysis details are illustrated in Fig. 6.25(b).

EXERCISES

D6.25 For the circuit in Fig. 6.25(a), find the largest value to which R_C can be raised while the transistor remains in the active mode.

Ans. 2.26 kΩ

D6.26 Redesign the circuit of Fig. 6.25(a) (i.e., find new values for R_E and R_C) to establish a collector current of 1 mA and a reverse bias on the collector–base junction of 4 V. Assume $\alpha \simeq 1$.

Ans. $R_E = 9.3$ kΩ; $R_C = 6$ kΩ

Example 6.8

We want to analyze the circuit in Fig. 6.26(a) to determine the voltages at all nodes and the currents in all branches. Assume $\beta = 100$.

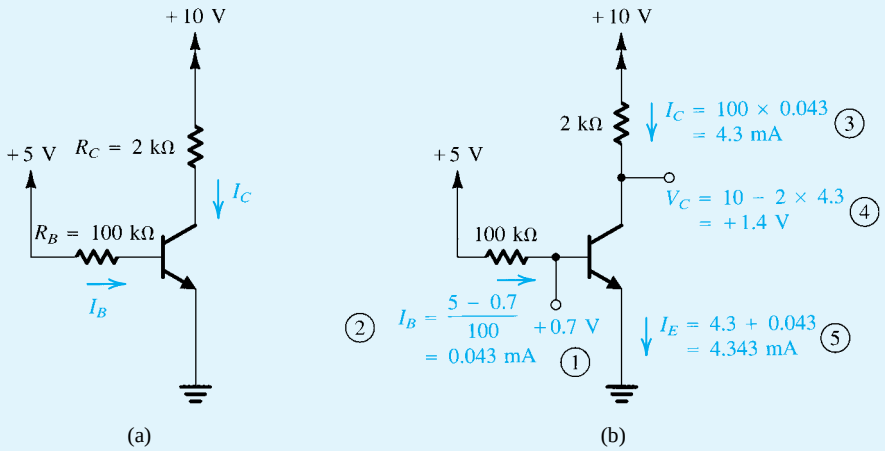


Figure 6.26 Example 6.8: **(a)** circuit; **(b)** analysis, with the steps indicated by the circled numbers.

Solution

The base–emitter junction is clearly forward biased. Thus,

$$I_B = \frac{+5 - V_{BE}}{R_B} \simeq \frac{5 - 0.7}{100} = 0.043 \text{ mA}$$

Assume that the transistor is operating in the active mode. We now can write

$$I_C = \beta I_B = 100 \times 0.043 = 4.3 \text{ mA}$$

The collector voltage can now be determined as

$$V_C = +10 - I_C R_C = 10 - 4.3 \times 2 = +1.4 \text{ V}$$

Since the base voltage V_B is

$$V_B = V_{BE} \simeq +0.7 \text{ V}$$

it follows that the collector–base junction is reverse-biased by 0.7 V and the transistor is indeed in the active mode. The emitter current will be given by

$$I_E = (\beta + 1) I_B = 101 \times 0.043 \simeq 4.3 \text{ mA}$$

We note from this example that the collector and emitter currents depend critically on the value of β. In fact, if β were 10% higher, the transistor would leave the active mode and enter saturation. Therefore this clearly is a *bad* design. The analysis details are illustrated in Fig. 6.26(b).

EXERCISE

D6.27 The circuit of Fig. 6.26(a) is to be fabricated using a transistor type whose β is specified to be in the range of 50 to 150. That is, individual units of this same transistor type can have β values anywhere in this range. Redesign the circuit by selecting a new value for R_C so that all fabricated circuits are guaranteed to be in the active mode. What is the range of collector voltages that the fabricated circuits may exhibit?

Ans. $R_C = 1.5$ kΩ; $V_C = 0.3$ V to 6.8 V

Example 6.9

We want to analyze the circuit of Fig. 6.27 to determine the voltages at all nodes and the currents through all branches. The minimum value of β is specified to be 30.

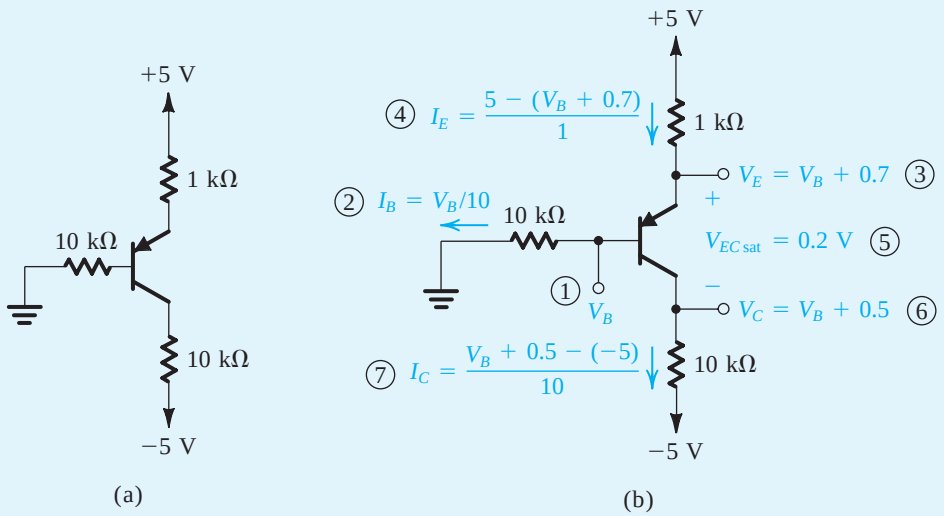


Figure 6.27 Example 6.9: **(a)** circuit; **(b)** analysis with steps numbered.

Solution

A quick glance at this circuit reveals that the transistor will be either active or saturated. Assuming active-mode operation and neglecting the base current, we see that the base voltage will be approximately zero volts, the emitter voltage will be approximately +0.7 V, and the emitter current will be approximately 4.3 mA. Since the maximum current that the collector can support while the transistor remains in the active mode is approximately 0.5 mA, it follows that the transistor is definitely saturated.

Assuming that the transistor is saturated and denoting the voltage at the base by V_B (refer to Fig. 6.27b), it follows that

$$V_E = V_B + V_{EB} \simeq V_B + 0.7$$

$$V_C = V_E - V_{EC\,sat} \simeq V_B + 0.7 - 0.2 = V_B + 0.5$$

$$I_E = \frac{+5 - V_E}{1} = \frac{5 - V_B - 0.7}{1} = 4.3 - V_B \quad \text{mA}$$

$$I_B = \frac{V_B}{10} = 0.1 V_B \quad \text{mA}$$

$$I_C = \frac{V_C - (-5)}{10} = \frac{V_B + 0.5 + 5}{10} = 0.1 V_B + 0.55 \quad \text{mA}$$

Using the relationship $I_E = I_B + I_C$, we obtain

$$4.3 - V_B = 0.1V_B + 0.1V_B + 0.55$$

which results in

$$V_B = \frac{3.75}{1.2} \simeq 3.13 \text{ V}$$

Substituting in the equations above, we obtain

$$V_E = 3.83 \text{ V}$$

$$V_C = 3.63 \text{ V}$$

$$I_E = 1.17 \text{ mA}$$

$$I_C = 0.86 \text{ mA}$$

$$I_B = 0.31 \text{ mA}$$

from which we see that the transistor is saturated, since the value of forced β is

$$\beta_{\text{forced}} = \frac{0.86}{0.31} \simeq 2.8$$

which is much smaller than the specified minimum β.

Example 6.10

We want to analyze the circuit of Fig. 6.28(a) to determine the voltages at all nodes and the currents through all branches. Assume $\beta = 100$.

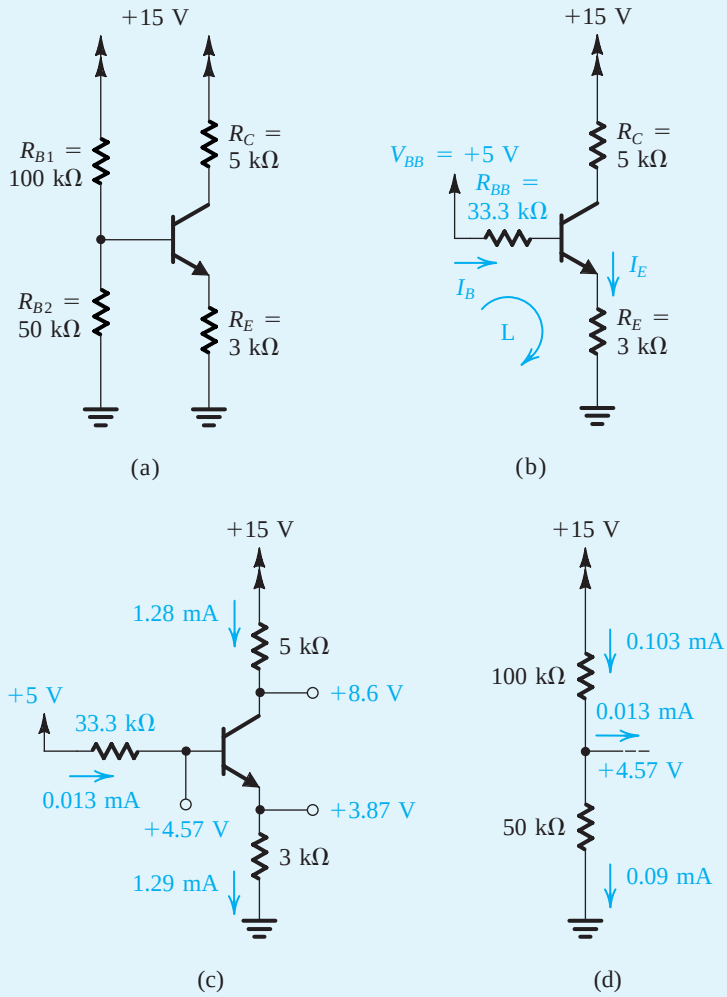


Figure 6.28 Circuits for Example 6.10.

Solution

The first step in the analysis consists of simplifying the base circuit using Thévenin's theorem. The result is shown in Fig. 6.28(b), where

$$V_{BB} = +15\frac{R_{B2}}{R_{B1} + R_{B2}} = 15\frac{50}{100 + 50} = +5 \text{ V}$$

$$R_{BB} = R_{B1} \parallel R_{B2} = 100 \parallel 50 = 33.3\ \text{k}\Omega$$

To evaluate the base or the emitter current, we have to write a loop equation around the loop labeled L in Fig. 6.28(b). Note, however, that the current through R_{BB} is different from the current through R_E. The loop equation will be

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

Now, assuming active-mode operation, we replace I_B with

$$I_B = \frac{I_E}{\beta + 1}$$

and rearrange the equation to obtain

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + [R_{BB}/(\beta + 1)]}$$

For the numerical values given we have

$$I_E = \frac{5 - 0.7}{3 + (33.3/101)} = 1.29\ \text{mA}$$

The base current will be

$$I_B = \frac{1.29}{101} = 0.0128\ \text{mA}$$

The base voltage is given by

$$\begin{aligned} V_B &= V_{BE} + I_E R_E \\ &= 0.7 + 1.29 \times 3 = 4.57\ \text{V} \end{aligned}$$

We can evaluate the collector current as

$$I_C = \alpha I_E = 0.99 \times 1.29 = 1.28\ \text{mA}$$

The collector voltage can now be evaluated as

$$V_C = +15 - I_C R_C = 15 - 1.28 \times 5 = 8.6\ \text{V}$$

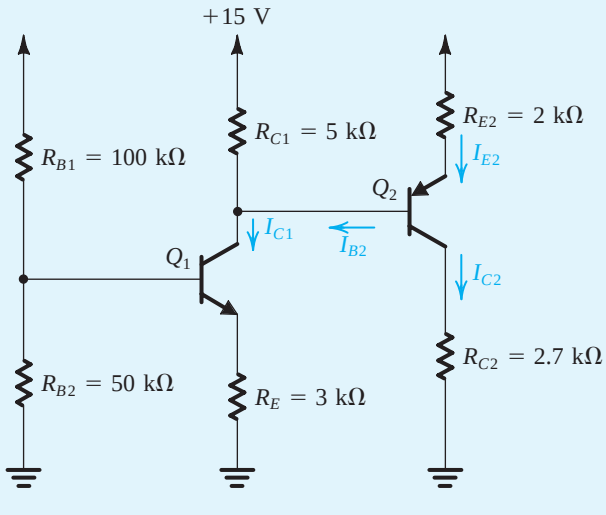
It follows that the collector is higher in potential than the base by 4.03 V, which means that the transistor is in the active mode, as had been assumed. The results of the analysis are given in Fig. 6.28(c, d).

EXERCISE

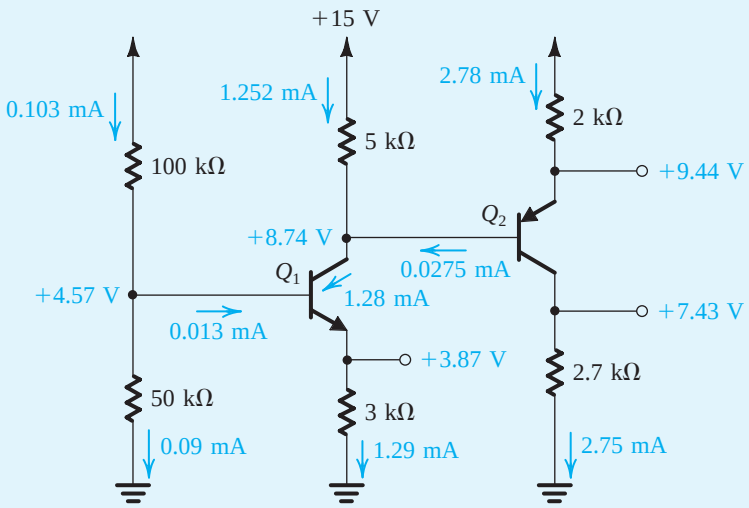
6.28 If the transistor in the circuit of Fig. 6.28(a) is replaced with another having half the value of β (i.e., $\beta = 50$), find the new value of I_C, and express the change in I_C as a percentage.
Ans. $I_C = 1.15$ mA; -10%

Example 6.11

We want to analyze the circuit in Fig. 6.29(a) to determine the voltages at all nodes and the currents through all branches.



(a)



(b)

Figure 6.29 Circuits for Example 6.11.

Solution

We first recognize that part of this circuit is identical to the circuit we analyzed in Example 6.10—namely, the circuit of Fig. 6.28(a). The difference, of course, is that in the new circuit we have an additional

transistor Q_2 together with its associated resistors R_{E2} and R_{C2}. Assume that Q_1 is still in the active mode. The following values will be identical to those obtained in the previous example:

$$V_{B1} = +4.57 \text{ V} \qquad I_{E1} = 1.29 \text{ mA}$$

$$I_{B1} = 0.0128 \text{ mA} \qquad I_{C1} = 1.28 \text{ mA}$$

However, the collector voltage will be different than previously calculated, since part of the collector current I_{C1} will flow in the base lead of Q_2 (I_{B2}). As a first approximation we may assume that I_{B2} is much smaller than I_{C1}; that is, we may assume that the current through R_{C1} is almost equal to I_{C1}. This will enable us to calculate V_{C1}:

$$V_{C1} \simeq +15 - I_{C1}R_{C1}$$

$$= 15 - 1.28 \times 5 = +8.6 \text{ V}$$

Thus Q_1 is in the active mode, as had been assumed.

As far as Q_2 is concerned, we note that its emitter is connected to +15 V through R_{E2}. It is therefore safe to assume that the emitter–base junction of Q_2 will be forward biased. Thus the emitter of Q_2 will be at a voltage V_{E2} given by

$$V_{E2} = V_{C1} + V_{EB}\big|_{Q_2} \simeq 8.6 + 0.7 = +9.3 \text{ V}$$

The emitter current of Q_2 may now be calculated as

$$I_{E2} = \frac{+15 - V_{E2}}{R_{E2}} = \frac{15 - 9.3}{2} = 2.85 \text{ mA}$$

Since the collector of Q_2 is returned to ground via R_{C2}, it is possible that Q_2 is operating in the active mode. Assume this to be the case. We now find I_{C2} as

$$I_{C2} = \alpha_2 I_{E2}$$

$$= 0.99 \times 2.85 = 2.82 \text{ mA} \quad (\text{assuming } \beta_2 = 100)$$

The collector voltage of Q_2 will be

$$V_{C2} = I_{C2}R_{C2} = 2.82 \times 2.7 = 7.62 \text{ V}$$

which is lower than V_{B2} by 0.98 V. Thus Q_2 is in the active mode, as assumed.

It is important at this stage to find the magnitude of the error incurred in our calculations by the assumption that I_{B2} is negligible. The value of I_{B2} is given by

$$I_{B2} = \frac{I_{E2}}{\beta_2 + 1} = \frac{2.85}{101} = 0.028 \text{ mA}$$

which is indeed much smaller than I_{C1} (1.28 mA). If desired, we can obtain more accurate results by iterating one more time, assuming I_{B2} to be 0.028 mA. The new values will be

$$\text{Current in } R_{C1} = I_{C1} - I_{B2} = 1.28 - 0.028 = 1.252 \text{ mA}$$

$$V_{C1} = 15 - 5 \times 1.252 = 8.74 \text{ V}$$

$$V_{E2} = 8.74 + 0.7 = 9.44 \text{ V}$$

$$I_{E2} = \frac{15 - 9.44}{2} = 2.78 \text{ mA}$$

Example 6.11 *continued*

$$I_{C2} = 0.99 \times 2.78 = 2.75 \text{ mA}$$

$$V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V}$$

$$I_{B2} = \frac{2.78}{101} = 0.0275 \text{ mA}$$

Note that the new value of I_{B2} is very close to the value used in our iteration, and no further iterations are warranted. The final results are indicated in Fig. 6.29(b).

The reader justifiably might be wondering about the necessity for using an iterative scheme in solving a linear (or linearized) problem. Indeed, we can obtain the exact solution (if we can call anything we are doing with a first-order model exact!) by writing appropriate equations. The reader is encouraged to find this solution and then compare the results with those obtained above. It is important to emphasize, however, that in most such problems it is quite sufficient to obtain an approximate solution, provided we can obtain it quickly and, of course, correctly.

In the above examples, we frequently used a precise value of α to calculate the collector current. Since $\alpha \simeq 1$, the error in such calculations will be very small if one assumes $\alpha = 1$ and $I_C = I_E$. Therefore, except in calculations that depend critically on the value of α (e.g., the calculation of base current), one usually assumes $\alpha \simeq 1$.

EXERCISES

6.29 For the circuit in Fig. 6.29, find the total current drawn from the power supply. Hence find the power dissipated in the circuit.

Ans. 4.135 mA; 62 mW

6.30 The circuit in Fig. E6.30 is to be connected to the circuit in Fig. 6.29(a) as indicated; specifically, the base of Q_3 is to be connected to the collector of Q_2. If Q_3 has $\beta = 100$, find the new value of V_{C2} and the values of V_{E3} and I_{C3}.

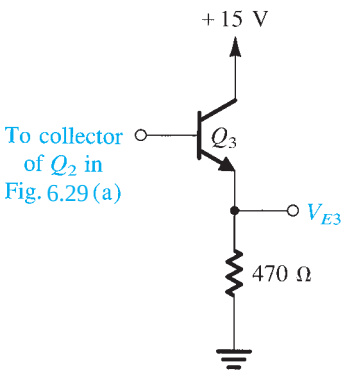


Figure E6.30

Ans. +7.06 V; +6.36 V; 13.4 mA

Example 6.12

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 6.30(a). Assume $\beta = 100$.

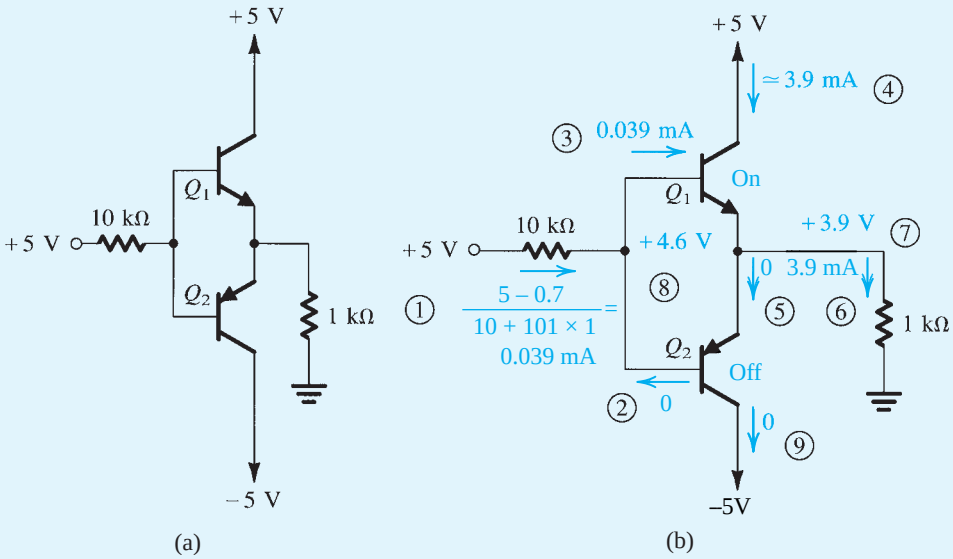


Figure 6.30 Example 6.12: **(a)** circuit; **(b)** analysis with the steps numbered.

Solution

By examining the circuit, we conclude that the two transistors Q_1 and Q_2 cannot be simultaneously conducting. Thus if Q_1 is on, Q_2 will be off, and vice versa. Assume that Q_2 is on. It follows that current will flow from ground through the 1-kΩ resistor into the emitter of Q_2. Thus the base of Q_2 will be at a negative voltage, and base current will be flowing out of the base through the 10-kΩ resistor and into the +5-V supply. This is impossible, since if the base is negative, current in the 10-kΩ resistor will have to flow into the base. Thus we conclude that our original assumption—that Q_2 is on—is incorrect. It follows that Q_2 will be off and Q_1 will be on.

The question now is whether Q_1 is active or saturated. The answer in this case is obvious: Since the base is fed with a +5-V supply and since base current flows into the base of Q_1, it follows that the base of Q_1 will be at a voltage lower than +5 V. Thus the collector–base junction of Q_1 is reverse biased and Q_1 is in the active mode. It remains only to determine the currents and voltages using techniques already described in detail. The results are given in Fig. 6.30(b).

EXERCISES

6.31 Solve the problem in Example 6.12 for the case of a voltage of –5 V feeding the bases. What voltage appears at the emitters?

Ans. –3.9 V

6.32 Solve the problem in Example 6.12 with the voltage feeding the bases changed to +10 V. Assume that $\beta_{min} = 30$, and find V_E, V_B, I_{C1}, and I_{C2}.

Ans. +4.8 V; +5.5 V; 4.35 mA; 0

6.4 Applying the BJT in Amplifier Design

We now begin our study of the utilization of the BJT in the design of amplifiers.[13] The basis for this important application is that when operated in the active mode, the BJT functions as a voltage-controlled current source: the base–emitter voltage v_{BE} controls the collector current i_C. Although the control relationship is nonlinear (exponential), we will shortly devise a method for obtaining almost-linear amplification from this fundamentally nonlinear device.

6.4.1 Obtaining a Voltage Amplifier

In the introduction to amplifiers in Section 1.5, we learned that a voltage-controlled current source can serve as a transconductance amplifier, that is, an amplifier whose input signal is a voltage and whose output signal is a current. More commonly, however, one is interested in voltage amplifiers. A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output. Doing this for a BJT results in the simple amplifier circuit shown in Fig. 6.31(a). Here v_{BE} is the input voltage, R_C (known as a **load resistance**) converts the collector current i_C to a voltage ($i_C R_C$), and V_{CC} is the supply voltage that powers up the amplifier and, together with R_C, establishes operation in the active mode, as will be shown shortly.

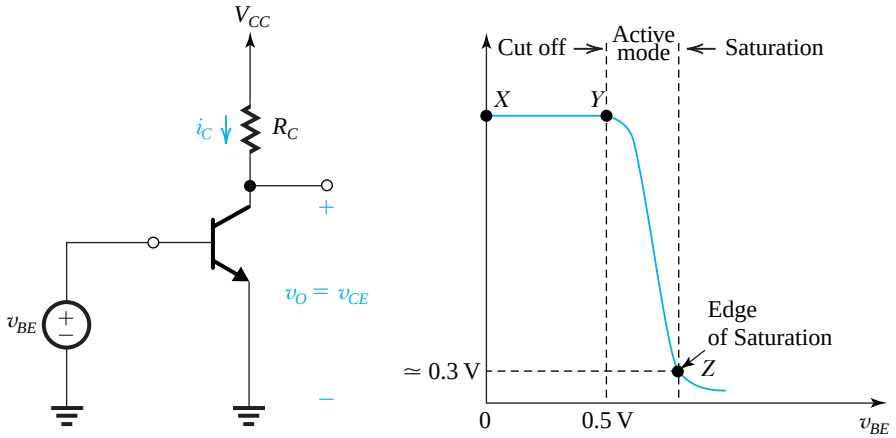


Figure 6.31 **(a)** Simple BJT amplifier with input v_{BE} and output v_{CE}. **(b)** The voltage transfer characteristic (VTC) of the amplifier in **(a)**. The three segments of the VTC correspond to the three modes of operation of the BJT.

In the amplifier circuit of Fig. 6.31(a), the output voltage is taken between the collector and ground, rather than simply across R_C. This is done because of the need to maintain a ground reference throughout the circuit. The output voltage v_{CE} is given by

$$v_{CE} = V_{CC} - i_C R_C \tag{6.24}$$

Thus it is an inverted version (note the minus sign) of $i_C R_C$ that is shifted by the constant value of the supply voltage V_{CC}.

[13] An introduction to amplifiers from an external terminals perspective is presented in Sections 1.4 and 1.5. It would be helpful for readers unfamiliar with basic amplifier concepts to review this material before proceeding with the study of BJT amplifiers.

6.4.2 The Voltage Transfer Characteristic (VTC)

A very useful tool that yields great insight into the operation of an amplifier circuit is its voltage transfer characteristic (VTC). This is simply a plot (or a clearly labeled sketch) of the output voltage versus the input voltage. For the BJT amplifier in Fig. 6.31(a), this is the plot of v_{CE} versus v_{BE} shown in Fig. 6.31(b).

Observe that for v_{BE} lower than about 0.5 V, the transistor is cut off, $i_C = 0$, and, from Eq. (6.24), $v_{CE} = V_{CC}$. As v_{BE} rises, the transistor turns on and v_{CE} decreases. However, since initially v_{CE} will still be high, the BJT will be operating in the active mode. This continues as v_{BE} is increased until it reaches a value that results in v_{CE} becoming lower than v_{BE} by 0.4 volt or so (point Z on the VTC in Fig. 6.31b). For v_{BE} greater than that at point Z, the transistor operates in the saturation region and v_{CE} decreases very slowly.

The VTC in Fig. 6.31(b) indicates that the segment of greatest slope (and hence potentially the largest amplifier gain) is that labeled YZ, which corresponds to operation in the active mode. An expression for the segment YZ can be obtained by substituting for i_C in Eq. (6.24) by its active-mode value

$$i_C = I_S\, e^{v_{BE}/V_T} \tag{6.25}$$

where we have for simplicity neglected base-width modulation (the Early effect). The result is

$$v_{CE} = V_{CC} - R_C I_S\, e^{v_{BE}/V_T} \tag{6.26}$$

This is obviously a nonlinear relationship. Nevertheless, linear (or almost-linear) amplification can be obtained by using the technique of biasing the BJT.

6.4.3 Biasing the BJT to Obtain Linear Amplification

Biasing enables us to obtain almost-linear amplification from the BJT. The technique is illustrated in Fig. 6.32(a). A dc voltage V_{BE} is selected to obtain operation at a point Q on the segment YZ of the VTC. How to select an appropriate location for the bias point Q will be discussed shortly. For the time being, observe that the coordinates of Q are the dc

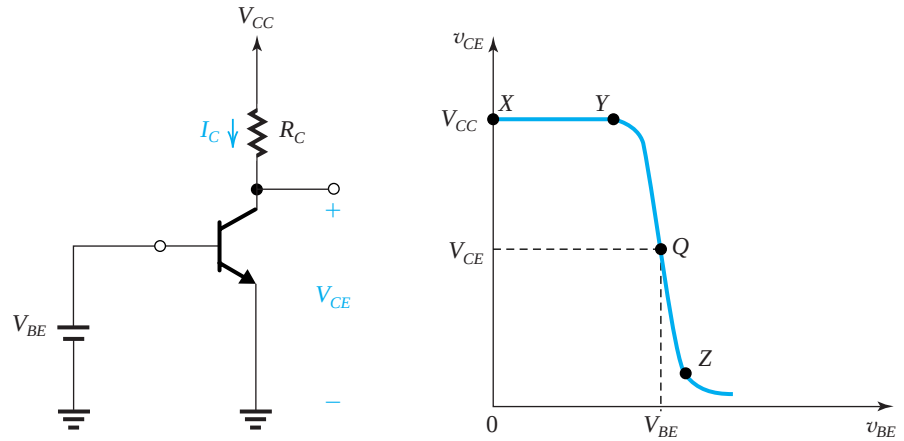


Figure 6.32 Biasing the BJT amplifier at a point Q located on the active-mode segment of the VTC.

voltages V_{BE} and V_{CE}, which are related by

$$V_{CE} = V_{CC} - R_C I_S e^{V_{BE}/V_T} \tag{6.27}$$

Point Q is known as the **bias point** or the **dc operating point**. Also, since at Q no signal component is present, it is also known as the **quiescent point** (which is the origin of the symbol Q). Note that a transistor operating at Q will have a collector current I_C given by

$$I_C = I_S e^{V_{BE}/V_T} \tag{6.28}$$

Next, the signal to be amplified v_{be}. a function of time t, is superimposed on the bias voltage V_{BE}, as shown in Fig. 6.33(a). Thus the total instantaneous value of v_{BE} becomes

$$v_{BE}(t) = V_{BE} + v_{be}(t)$$

The resulting $v_{CE}(t)$ can be obtained by substituting this expression for $v_{BE}(t)$ into Eq. (6.25). Graphically, we can use the VTC to obtain $v_{CE}(t)$, point by point, as illustrated in Fig. 6.33(b).

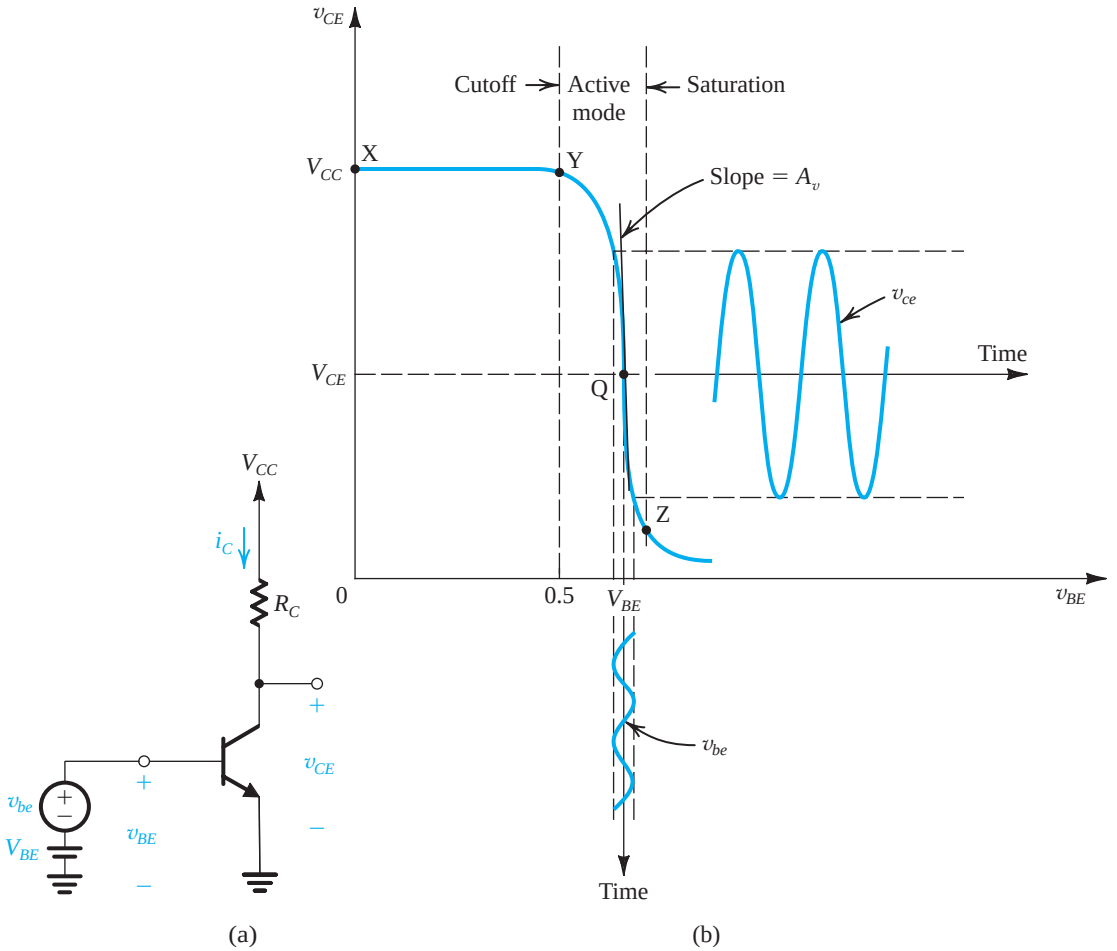


Figure 6.33 BJT amplifier biased at a point Q, with a small voltage signal v_{be} superimposed on the dc bias voltage V_{BE}. The resulting output signal v_{ce} appears superimposed on the dc collector voltage V_{CE}. The amplitude of v_{ce} is larger than that of v_{be} by the voltage gain A_v.

Here we show the case when v_{be} is a sine wave of "small" amplitude. Specifically, the amplitude of v_{be} is small enough to restrict the excursion of the instantaneous operating point to a short almost-linear segment of the VTC around the bias point Q. The shorter the segment, the greater the linearity achieved, and the closer to an ideal sine wave the signal component at the output, v_{ce}, will be. This is the essence of obtaining linear amplification from the nonlinear BJT.

6.4.4 The Small-Signal Voltage Gain

If the input signal v_{be} is kept small, the corresponding signal at the output v_{ce} will be nearly proportional to v_{be} with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q. This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q,

$$A_v \equiv \left.\frac{dv_{CE}}{dv_{BE}}\right|_{v_{BE}=V_{BE}} \tag{6.29}$$

Utilizing Eq. (6.26) together with Eq. (6.28), we obtain

$$A_v = -\left(\frac{I_C}{V_T}\right)R_C \tag{6.30}$$

We make the following observations on this expression for the voltage gain:

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a 180° phase shift between the input and the output. This inversion is obvious in Fig. 6.33(b) and should have been anticipated from Eq. (6.26).
2. The gain is proportional to the collector bias current I_C and to the load resistance R_C.

Additional insight into the voltage gain A_v can be obtained by expressing Eq. (6.30) as

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T} \tag{6.31}$$

where V_{RC} is the dc voltage drop across R_C,

$$V_{RC} = V_{CC} - V_{CE} \tag{6.32}$$

The simple expression in Eq. (6.31) indicates that the voltage gain of the amplifier is the ratio of the dc voltage drop across R_C to the thermal voltage V_T (≃ 25 mV at room temperature). It follows that to maximize the voltage gain we should use as large a voltage drop across R_C as possible. For a given value of V_{CC}, Eq. (6.32) indicates that to increase V_{RC} we have to operate at a lower V_{CE}. However, reference to Fig. 6.33(b) shows that a lower V_{CE} means a bias point Q close to the end of the active-region segment, which might not leave sufficient room for the negative-output signal swing without the amplifier entering the saturation region. If this happens, the negative peaks of the waveform of v_{ce} will be flattened. Indeed, it is the need to allow sufficient room for output signal swing that determines the most effective placement of the bias point Q on the active-region segment, YZ, of the transfer curve. Placing Q too high on this segment not only results in reduced gain (because V_{RC} is lower) but could possibly limit the available range of positive signal swing. At the positive end, the limitation is imposed by the BJT cutting off, in which event the positive-output peaks would be clipped off at a level equal to V_{CC}. Finally, it is useful to note that the theoretical

maximum gain A_v is obtained by biasing the BJT at the edge of saturation, which of course would not leave any room for negative signal swing. The resulting gain is given by

$$A_v = -\frac{V_{CC} - V_{CE\text{sat}}}{V_T} \tag{6.33}$$

Thus,

$$|A_{v\max}| \simeq \frac{V_{CC}}{V_T} \tag{6.34}$$

Although the gain can be increased by using a larger supply voltage, other considerations come into play when one is determining an appropriate value for V_{CC}. In fact, the trend has been toward using lower and lower supply voltages, currently approaching 1 V or so. At such low supply voltages, large gain values can be obtained by replacing the resistance R_C with a constant-current source, as will be seen in Chapter 7.

Example 6.13

Consider an amplifier circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8$ kΩ, and a power supply $V_{CC} = 10$ V.

(a) Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of I_C?
(b) Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE}, find the amplitude of the output sine-wave signal (assume linear operation).
(c) Find the positive increment in v_{BE} (above V_{BE}) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3$ V.
(d) Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff (i.e., to $v_{CE} = 0.99V_{CC}$).

Solution

(a)
$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$
$$= \frac{10 - 3.2}{6.8} = 1 \text{ mA}$$

The value of V_{BE} can be determined from

$$1 \times 10^{-3} = 10^{-15} e^{V_{BE}/V_T}$$

which results in

$$V_{BE} = 690.8 \text{ mV}$$

(b)
$$A_v = -\frac{V_{CC} - V_{CE}}{V_T}$$
$$= -\frac{10 - 3.2}{0.025} = -272 \text{ V/V}$$
$$\hat{V}_{ce} = 272 \times 0.005 = 1.36 \text{ V}$$

(c) For $v_{CE} = 0.3$ V,
$$i_C = \frac{10 - 0.3}{6.8} = 1.617 \text{ mA}$$

To increase i_C from 1 mA to 1.617 mA, v_{BE} must be increased by
$$\Delta v_{BE} = V_T \ln\left(\frac{1.617}{1}\right)$$
$$= 12 \text{ mV}$$

(d) For $v_{CE} = 0.99V_{CC} = 9.9$ V,
$$i_C = \frac{10 - 9.9}{6.8} = 0.0147 \text{ mA}$$

To decrease i_C from 1 mA to 0.0147 mA, v_{BE} must change by
$$\Delta v_{BE} = V_T \ln\left(\frac{0.0147}{1}\right)$$
$$= -105.5 \text{ mV}$$

EXERCISE

6.33 For the situation described in Example 6.13, while keeping I_C unchanged at 1 mA, find the value of R_C that will result in a voltage gain of –320 V/V. What is the largest negative signal swing allowed at the output (assume that v_{CE} is not to decrease below 0.3 V)? What (approximately) is the corresponding input signal amplitude? (Assume linear operation.)
Ans. 8 kΩ; 1.7 V; 5.3 mV

6.4.5 Determining the VTC by Graphical Analysis

Figure 6.34 shows a graphical method for determining the VTC of the amplifier of Figure 6.33(a). Although graphical analysis of transistor circuits is rarely employed in practice, it is useful for us at this stage in gaining greater insight into circuit operation, especially in answering the question of where to locate the bias point Q.

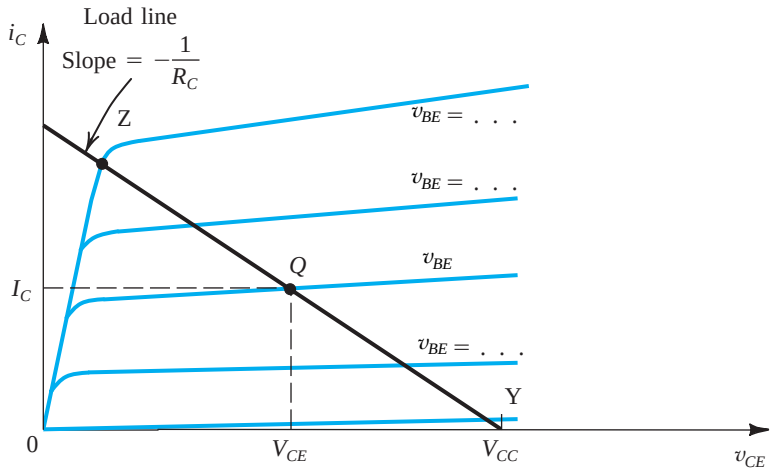


Figure 6.34 Graphical construction for determining the VTC of the amplifier circuit of Fig. 6.33(a).

The graphical analysis is based on the observation that for each value of v_{BE}, the circuit will be operating at the point of intersection of the corresponding $i_C - v_{CE}$ graph and the straight line representing Eq. (6.24), which can be rewritten in the form

$$i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE} \tag{6.35}$$

The straight line representing this relationship is superimposed on the $i_C - v_{CE}$ characteristics in Fig. 6.34. It intersects the horizontal axis at $v_{CE} = V_{CC}$ and has a slope of $-1/R_C$. Since this straight line represents in effect the load resistance R_C, it is called the **load line**. The VTC is then determined point by point. Note that we have labeled three important points: point Y at which $v_{BE} = 0.5$ V, point Q at which the BJT can be biased for amplifier operation ($v_{BE} = V_{BE}$ and $v_{CE} = V_{CE}$), and point Z at which the BJT leaves the active mode and enters the saturation region. If the BJT is to be used as a switch, then operating points Y and Z are applicable: At Y the transistor is off (open switch), and at Z the transistor operates as a low valued resistance $R_{CE\text{sat}}$ and has a small voltage drop (closed switch). It should be noted, however, that because of the long delay time needed to turn off a saturated BJT, modern digital integrated circuits no longer utilize the saturated mode of operation. Nonsaturated BJT digital circuits will be studied in Chapter 14.

6.4.6 Locating the Bias Point Q

The bias point Q is determined by the value of V_{BE} and that of the load resistance R_C. Two important considerations in deciding on the location of Q are the gain and the allowable signal swing at the output. To illustrate, consider the VTC shown in Fig. 6.33(b). Here the value of R_C is fixed, and the only variable remaining is the value of V_{BE}. Since the slope increases as we move closer to point Z, we obtain higher gain by locating Q as close to Z as possible. However, the closer Q is to the boundary point Z, the smaller the allowable magnitude of negative signal swing. Thus, as usual in engineering design, we encounter a situation requiring a trade-off.

In deciding on a value for R_C it is useful to refer to the $i_C - v_{CE}$ plane. Figure 6.35 shows two load lines resulting in two extreme bias points: Point Q_A, is too close to V_{CC}, resulting in a severe constraint on the positive signal swing of v_{ce}. Exceeding the allowable positive

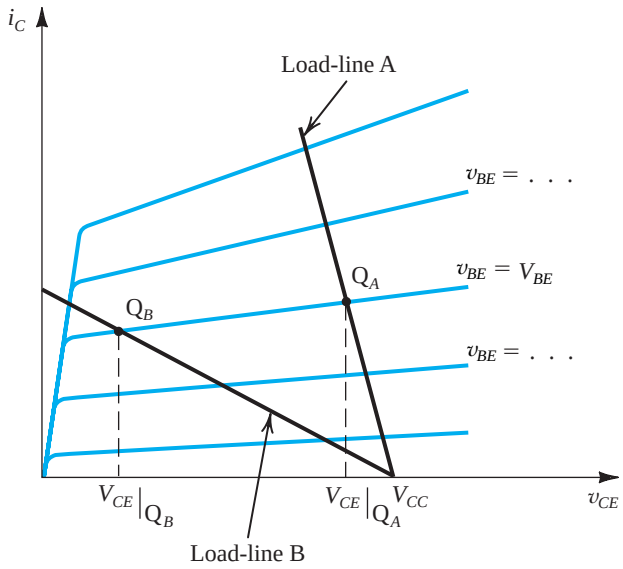


Figure 6.35 Effect of bias-point location on allowable signal swing: Load line A results in bias point Q_A with a corresponding V_{CE} that is too close to V_{CC} and thus limits the positive swing of v_{CE}. At the other extreme, load line B results in an operating point, Q_B, too close to the saturation region, thus limiting the negative swing of v_{CE}.

maximum results in the positive peaks of the signal being clipped off, since the BJT will turn off for the part of each cycle near the positive peak. We speak of this situation as the circuit not having sufficient "headroom." Similarly, point Q_B is too close to the boundary of the saturation region, thus severely limiting the allowable negative signal swing of v_{ce}. Exceeding this limit would result in the transistor entering the saturation region for part of each cycle near the negative peaks, resulting in a distorted output signal. We speak of this situation as the circuit not having sufficient "legroom." We will have more to say on bias design in Section 6.7.

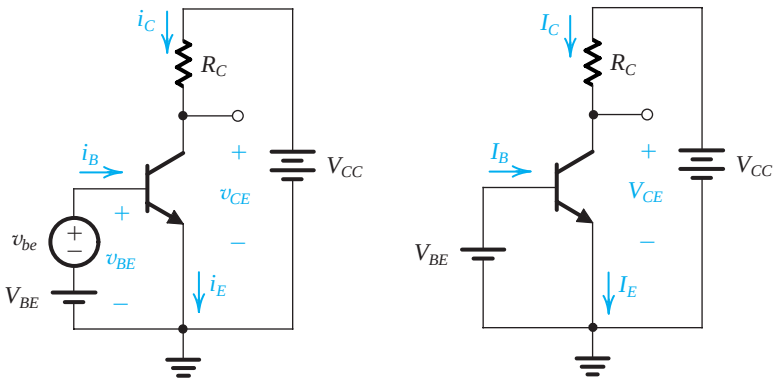
6.5 Small-Signal Operation and Models

Having learned the basis for the operation of the BJT as an amplifier, we now take a closer look at the small-signal operation of the transistor. Toward that end, consider once more the *conceptual* amplifier circuit shown in Fig. 6.36(a). Here the base–emitter junction is forward biased by a dc voltage V_{BE} (battery). The reverse bias of the collector–base junction is established by connecting the collector to another power supply of voltage V_{CC} through a resistor R_C. The input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE}.

We consider first the dc bias conditions by setting the signal v_{be} to zero. The circuit reduces to that in Fig. 6.36(b), and we can write the following relationships for the dc currents and voltages:

$$I_C = I_S e^{V_{BE}/V_T} \tag{6.36}$$

$$I_E = I_C/\alpha \tag{6.37}$$



(a) (b)

Figure 6.36 **(a)** Conceptual circuit to illustrate the operation of the transistor as an amplifier. **(b)** The circuit of **(a)** with the signal source v_{be} eliminated for dc (bias) analysis.

$$I_B = I_C/\beta \tag{6.38}$$

$$V_{CE} = V_{CC} - I_C R_C \tag{6.39}$$

Obviously, for active-mode operation, V_C should be greater than $(V_B - 0.4)$ by an amount that allows for the required signal swing at the collector.

6.5.1 The Collector Current and the Transconductance

If a signal v_{be} is applied as shown in Fig. 6.36(a), the total instantaneous base–emitter voltage v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly, the collector current becomes

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$
$$= I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$$

Use of Eq. (6.36) yields

$$i_C = I_C e^{v_{be}/V_T} \tag{6.40}$$

Now, if $v_{be} \ll V_T$, we may approximate Eq. (6.40) as

$$i_C \simeq I_C\left(1 + \frac{v_{be}}{V_T}\right) \tag{6.41}$$

Here we have expanded the exponential in Eq. (6.40) in a series and retained only the first two terms. This approximation, which is valid only for v_{be} less than approximately 10 mV, is referred to as the **small-signal approximation**. Under this approximation, the total collector current is given by Eq. (6.41) and can be rewritten

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \tag{6.42}$$

Thus the collector current is composed of the dc bias value I_C and a signal component i_c,

$$i_c = \frac{I_C}{V_T} v_{be} \tag{6.43}$$

This equation relates the signal current in the collector to the corresponding base–emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be} \tag{6.44}$$

where g_m is called the **transconductance**, and from Eq. (6.43), it is given by

$$g_m = \frac{I_C}{V_T} \tag{6.45}$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current I_C. Thus to obtain a constant predictable value for g_m, we need a constant predictable I_C. Finally, we note that BJTs have relatively high transconductance (as compared to MOSFETs, which we studied in Chapter 5); for instance, at $I_C = 1$ mA, $g_m \simeq 40$ mA/V.

A graphical interpretation for g_m is given in Fig. 6.37, where it is shown that g_m is equal to the slope of the i_C–v_{BE} characteristic curve at $i_C = I_C$ (i.e., at the bias point Q). Thus,

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C} \tag{6.46}$$

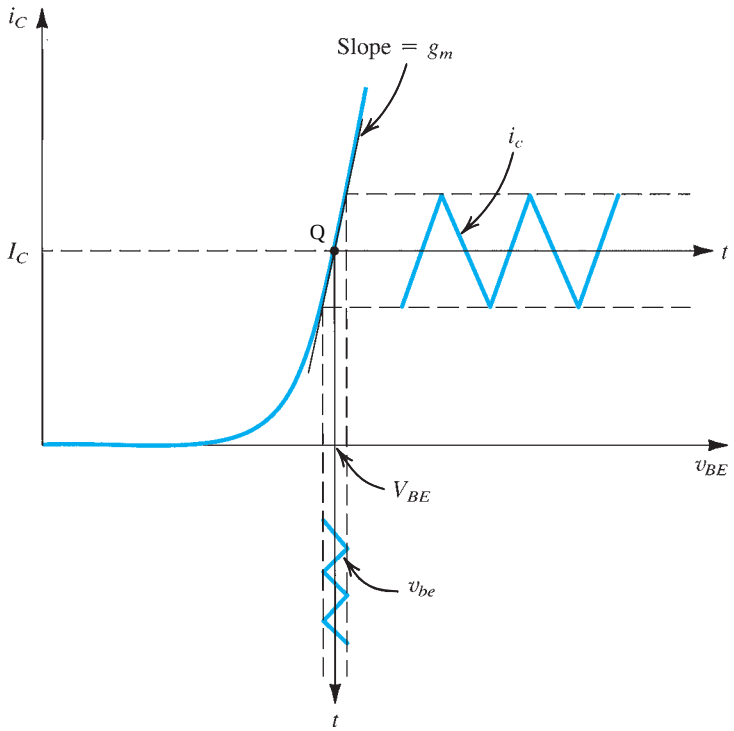


Figure 6.37 Linear operation of the transistor under the small-signal condition: A small signal v_{be} with a triangular waveform is superimposed on the dc voltage V_{BE}. It gives rise to a collector signal current i_c, also of triangular waveform, superimposed on the dc current I_C. Here, $i_c = g_m v_{be}$, where g_m is the slope of the i_C–v_{BE} curve at the bias point Q.

The small-signal approximation implies keeping the signal amplitude sufficiently small that *operation is restricted to an almost-linear segment of the i_C–v_{BE} exponential curve.* Increasing the signal amplitude will result in the collector current having components nonlinearly related to v_{be}. This, of course, is the same approximation that we discussed in the context of the amplifier transfer curve in Section 6.4.

The analysis above suggests that for small signals ($v_{be} \ll V_T$), the transistor behaves as a voltage-controlled current source. The input port of this controlled source is between base and emitter, and the output port is between collector and emitter. The transconductance of the controlled source is g_m, and the output resistance is infinite. The latter ideal property is a result of our first-order model of transistor operation in which the collector voltage has no effect on the collector current in the active mode. As we have seen in Section 6.2, practical BJTs have finite output resistance because of the Early effect. The effect of the output resistance on amplifier performance will be considered later.

EXERCISES

6.34 Use Eq. (6.46) to derive the expression for g_m in Eq. (6.45).

6.35 Calculate the value of g_m for a BJT biased at $I_C = 0.5$ mA.
Ans. 20 mA/V

6.5.2 The Base Current and the Input Resistance at the Base

To determine the resistance seen by v_{be}, we first evaluate the total base current i_B using Eq. (6.42), as follows:

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Thus,

$$i_B = I_B + i_b \tag{6.47}$$

where I_B is equal to I_C/β and the signal component i_b is given by

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be} \tag{6.48}$$

Substituting for I_C/V_T by g_m gives

$$i_b = \frac{g_m}{\beta}v_{be} \tag{6.49}$$

The small-signal input resistance between base and emitter, *looking into the base,* is denoted by r_π and is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b} \tag{6.50}$$

Using Eq. (6.49) gives

$$r_\pi = \frac{\beta}{g_m} \tag{6.51}$$

Thus r_π is directly dependent on β and is inversely proportional to the bias current I_C. Substituting for g_m in Eq. (6.51) from Eq. (6.45) and replacing I_C/β by I_B gives an alternative expression for r_π,

$$r_\pi = \frac{V_T}{I_B} \tag{6.52}$$

EXERCISE

6.36 A BJT amplifier is biased to operate at a constant collector current $I_C = 0.5$ mA irrespective of the value β. If the transistor manufacturer specifies β to range from 50 to 200, give the expected range of g_m, I_B, and r_π.
Ans. g_m is constant at 20 mA/V; $I_B = 10$ μA to 2.5 μA; $r_\pi = 2.5\,\text{k}\Omega$ to $10\,\text{k}\Omega$

6.5.3 The Emitter Current and the Input Resistance at the Emitter

The total emitter current i_E can be determined from

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

Thus,

$$i_E = I_E + i_e \tag{6.53}$$

where I_E is equal to I_C/α and the signal current i_e is given by

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be} \tag{6.54}$$

If we denote the small-signal resistance between base and emitter *looking into the emitter* by r_e, it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e} \tag{6.55}$$

Using Eq. (6.54) we find that r_e, called the **emitter resistance**, is given by

$$r_e = \frac{V_T}{I_E} \tag{6.56}$$

Comparison with Eq. (6.45) reveals that

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m} \tag{6.57}$$

The relationship between r_π and r_e can be found by combining their respective definitions in Eqs. (6.50) and (6.55) as

$$v_{be} = i_b r_\pi = i_e r_e$$

Thus,

$$r_\pi = (i_e / i_b) r_e$$

which yields

$$r_\pi = (\beta + 1) r_e \tag{6.58}$$

Figure 6.38 illustrates the definition of r_π and r_e.

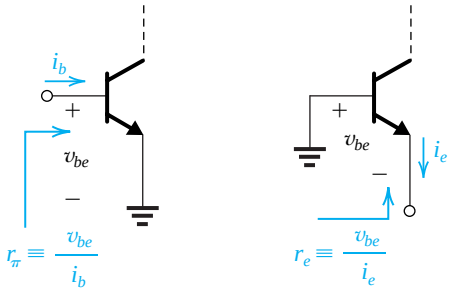


Figure 6.38 Illustrating the definition of r_π and r_e.

EXERCISE

6.37 A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find the value of g_m, r_e, and r_π at the bias point.
Ans. 40 mA/V; 25 Ω; 2.5 kΩ

6.5.4 Voltage Gain

We have established above that the transistor senses the base–emitter signal v_{be} and causes a proportional current $g_m v_{be}$ to flow in the collector lead at a high (ideally infinite) impedance level. In this way the transistor is acting as a voltage-controlled current source. To obtain an output voltage signal, we may force this current to flow through a resistor, as is done in Fig. 6.36(a). Then the total collector voltage v_{CE} will be

$$\begin{aligned} v_{CE} &= V_{CC} - i_C R_C \\ &= V_{CC} - (I_C + i_c) R_C \\ &= (V_{CC} - I_C R_C) - i_c R_C \\ &= V_{CE} - i_c R_C \end{aligned} \tag{6.59}$$

Here the quantity V_{CE} is the dc bias voltage at the collector, and the signal voltage is given by

$$v_{ce} = -i_c R_C = -g_m v_{be} R_C \tag{6.60}$$

$$= (-g_m R_C) v_{be}$$

Thus the voltage gain of this amplifier A_v is

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C \tag{6.61}$$

Here again we note that because g_m is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made. Substituting for g_m from Eq. (6.45) enables us to express the gain in the form

$$A_v = -\frac{I_C R_C}{V_T} \tag{6.62}$$

which is identical to the expression we derived in Section 6.4 (Eq. 6.31).

EXERCISE

6.38 In the circuit of Fig. 6.36(a), V_{BE} is adjusted to yield a dc collector current of 1 mA. Let $V_{CC} = 15$ V, $R_C = 10$ kΩ, and $\beta = 100$. Find the voltage gain v_{ce}/v_{be}. If $v_{be} = 0.005 \sin \omega t$ volt, find $v_C(t)$ and $i_B(t)$.
Ans. –400 V/V; $5 - 2 \sin \omega t$ volts; $10 + 2 \sin \omega t$ μA

6.5.5 Separating the Signal and the DC Quantities

The analysis above indicates that every current and voltage in the amplifier circuit of Fig. 6.36(a) is composed of two components: a dc component and a signal component. For instance, $v_{BE} = V_{BE} + v_{be}$, $I_C = I_C + i_c$, and so on. The dc components are determined from the dc circuit given in Fig. 6.36(b) and from the relationships imposed by the transistor (Eqs. 6.36 through 6.38). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. 6.39. Observe that since the voltage of an ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced V_{CC} and V_{BE} with short circuits. Had the circuit contained ideal dc

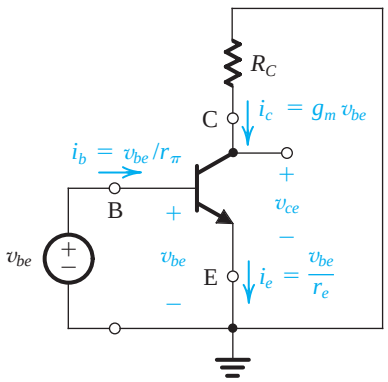


Figure 6.39 The amplifier circuit of Fig. 6.36(a) with the dc sources (V_{BE} and V_{CC}) eliminated (short-circuited). Thus only the signal components are present. Note that this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. 6.39 is useful only in so far as it shows the various signal currents and voltages; it is *not* an actual amplifier circuit, since the dc bias circuit is not shown.

Figure 6.39 also shows the expressions for the current increments (i_c, i_b, and i_e) obtained when a small signal v_{be} is applied. These relationships can be represented by a circuit. Such a circuit should have three terminals—C, B, and E—and should yield the same terminal currents indicated in Fig. 6.39. The resulting circuit is then *equivalent to the transistor as far as small-signal operation is concerned,* and thus it can be considered an equivalent small-signal circuit model.

6.5.6 The Hybrid-π Model

An equivalent circuit model for the BJT is shown in Fig. 6.40(a). This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base, r_π. The model obviously yields $i_c = g_m v_{be}$ and $i_b = v_{be}/r_\pi$. Not so obvious, however, is the fact that the model also yields the correct expression for i_e. This can be shown as follows: At the emitter node we have

$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi) \\ &= \frac{v_{be}}{r_\pi}(1+\beta) = v_{be} \Big/ \left(\frac{r_\pi}{1+\beta}\right) \\ &= v_{be}/r_e \end{aligned}$$

A slightly different equivalent-circuit model can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b as follows:

$$\begin{aligned} g_m v_{be} &= g_m(i_b r_\pi) \\ &= (g_m r_\pi) i_b = \beta i_b \end{aligned}$$

This results in the alternative equivalent-circuit model shown in Fig. 6.40(b). Here the transistor is represented as a current-controlled current source, with the control current being i_b.

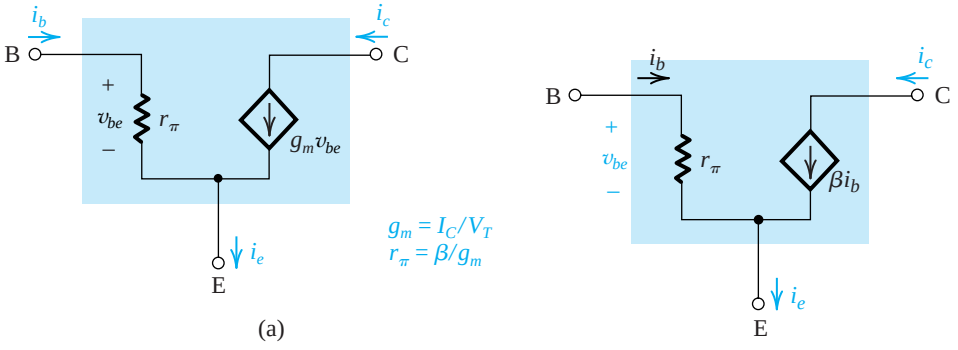


Figure 6.40 Two slightly different versions of the hybrid-π model for the small-signal operation of the BJT. The equivalent circuit in **(a)** represents the BJT as a voltage-controlled current source (a transconductance amplifier), and that in **(b)** represents the BJT as a current-controlled current source (a current amplifier).

The two models of Fig. 6.40 are simplified versions of what is known as the hybrid-π model. This is the most widely used model for the BJT.

It is important to note that the small-signal equivalent circuits of Fig. 6.40 model the operation of the BJT *at a given bias point*. This should be obvious from the fact that the model parameters g_m and r_π depend on the value of the dc bias current I_C, as indicated in Fig. 6.40. It is interesting and useful to note that the models of Fig. 6.40 (a) and (b) are the small-signal versions of the models of Fig. 6.5(c) and (d), respectively. Specifically, observe that r_π is the incremental resistance of D_B.

EXERCISE

6.39 For the model in Fig. 6.40(b) show that $i_c = g_m v_{be}$ and $i_e = v_{be}/r_e$.

6.5.7 The T Model

Although the hybrid-π model (in one of its two variants shown in Fig. 6.40) can be used to carry out small-signal analysis of any transistor circuit, there are situations in which an alternative model, shown in Fig. 6.41, is much more convenient. This model, called the **T model**, is shown in two versions in Fig. 6.41. The model of Fig. 6.41(a) represents the BJT as a voltage-controlled current source with the control voltage being v_{be}. Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown. From Fig. 6.41(a) we see clearly that the model yields the correct expressions for i_c and i_e. For i_b we note that at the base node we have

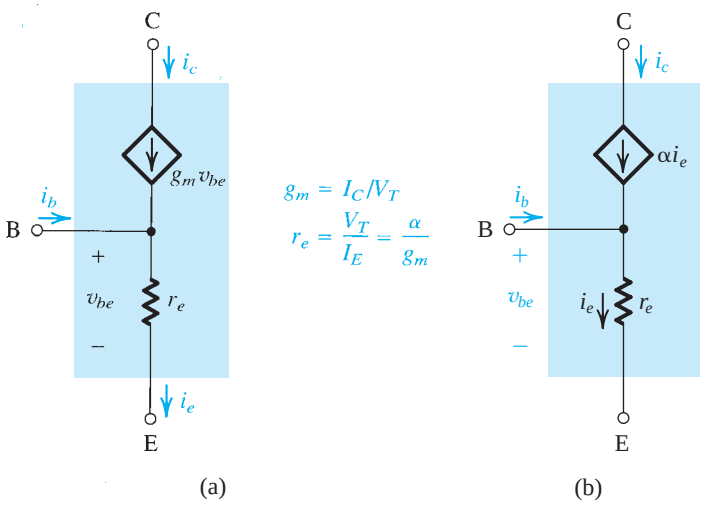


Figure 6.41 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in **(a)** is a voltage-controlled current source representation and that in **(b)** is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid-π model.

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e)$$

$$= \frac{v_{be}}{r_e}(1 - \alpha) = \frac{v_{be}}{r_e}\left(1 - \frac{\beta}{\beta + 1}\right)$$

$$= \frac{v_{be}}{(\beta + 1) r_e} = \frac{v_{be}}{r_\pi}$$

as should be the case.

If in the model of Fig. 6.41(a) the current of the controlled source is expressed in terms of the emitter current as

$$g_m v_{be} = g_m(i_e r_e)$$

$$= (g_m r_e) i_e = \alpha i_e$$

we obtain the alternative T model shown in Fig. 6.41(b). Here the BJT is represented as a current-controlled current source but with the control signal being i_e.

It is interesting and useful to note that the models of Fig. 6.41(a) and (b) are the small-signal versions of the models in Fig. 6.5(a) and (b), respectively. Specifically observe that r_e is the incremental resistance of D_E.

6.5.8 Small-Signal Models of the *pnp* Transistor

Although the small-signal models in Figs. 6.40 and 6.41 were developed for the case of the *npn* transistor, they apply equally well to the *pnp* transistor *with no change in polarities*.

6.5.9 Application of the Small-Signal Equivalent Circuits

The availability of the small-signal BJT circuit models makes the analysis of transistor amplifier circuits a systematic process. The process consists of the following steps:

1. Eliminate the signal source and determine the dc operating point of the BJT and in particular the dc collector current I_C.
2. Calculate the values of the small-signal model parameters: $g_m = I_C/V_T$, $r_\pi = \beta/g_m$, and $r_e = V_T/I_E = \alpha/g_m$.
3. Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
4. Replace the BJT with one of its small-signal equivalent circuit models. Although any one of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer later in this chapter.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance). The process will be illustrated by the following examples.

Example 6.14

We wish to analyze the transistor amplifier shown in Fig. 6.42(a) to determine its voltage gain v_o/v_i. Assume $\beta = 100$.

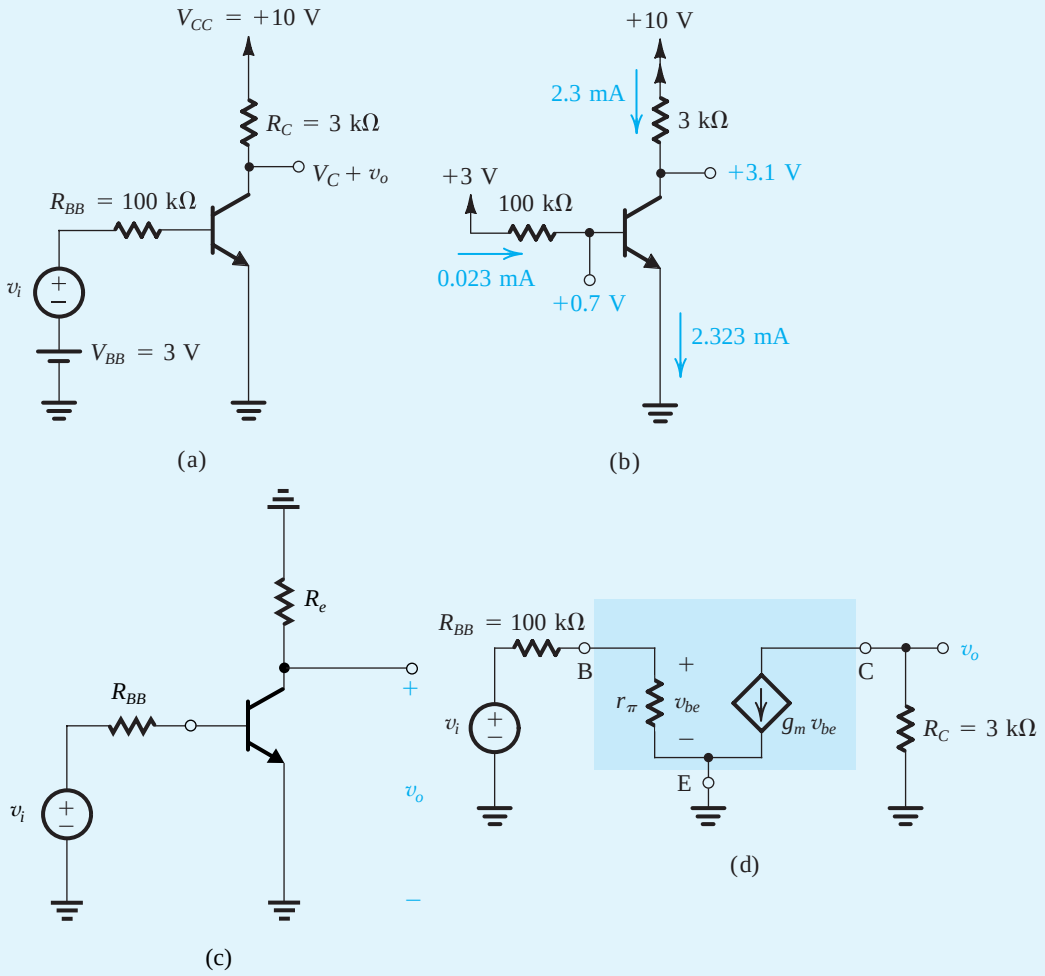


Figure 6.42 Example 6.14: **(a)** amplifier circuit; **(b)** circuit for dc analysis; **(c)** amplifier circuit with dc sources replaced by short circuits; **(d)** amplifier circuit with transistor replaced by its hybrid-π, small-signal models.

Solution

We shall follow the five-step process outlined above:

1. The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $v_i = 0$ and thus obtain the dc circuit shown in Fig. 6.42(b). The dc base current will be

Example 6.14 *continued*

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}}$$
$$\simeq \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$V_C = V_{CC} - I_C R_C$$
$$= +10 - 2.3 \times 3 = +3.1 \text{ V}$$

Since V_B at +0.7 V is less than V_C, it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 6.42(b).

2. Having determined the operating point, we can now proceed to determine the small-signal model parameters:

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3/0.99) \text{ mA}} = 10.8 \ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

3. Replacing V_{BB} and V_{CC} with short circuits results in the circuit in Fig. 6.42(c).
4. To carry out the small-signal analysis, it is equally convenient to employ either of the two hybrid-π, equivalent-circuit models of Fig. 6.40 to replace the transistor in the circuit of Fig. 6.42(c). Using the first results in the amplifier equivalent circuit given in Fig. 6.42(d).
5. Analysis of the equivalent circuit in Fig. 6.42(d) proceeds as follows:

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}}$$
$$= v_i \frac{1.09}{101.09} = 0.011 v_i \tag{6.63}$$

The output voltage v_o is given by

$$v_o = -g_m v_{be} R_C$$
$$= -92 \times 0.011 v_i \times 3 = -3.04 v_i$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V} \tag{6.64}$$

Example 6.15

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that v_i has a triangular waveform. First determine the maximum amplitude that v_i is allowed to have. Then, with the amplitude of v_i set to this value, give the waveforms of the total quantities $i_B(t)$, $v_{BE}(t)$, $i_C(t)$, and $v_C(t)$.

Solution

One constraint on signal amplitude is the small-signal approximation, which stipulates that v_{be} should not exceed about 10 mV. If we take the triangular waveform v_{be} to be 20 mV peak-to-peak and work backward, Eq. (6.63) can be used to determine the maximum possible peak of v_i,

$$\hat{v}_o = \frac{v_{be}}{0.011} = \frac{10}{0.011} = 0.91 \text{ V}$$

To check whether the transistor remains in the active mode with v_i having a peak value $\hat{v}_i = 0.91$ V, we have to evaluate the collector voltage. The voltage at the collector will consist of a triangular wave v_o superimposed on the dc value $V_C = 3.1$ V. The peak voltage of the triangular waveform will be

$$\hat{v}_o = \hat{v}_i \times \text{gain} = 0.91 \times 3.04 = 2.77 \text{ V}$$

It follows that when the output swings negative, the collector voltage reaches a minimum of 3.1 – 2.77 = 0.33 V, which is lower than the base voltage by less than 0.4 V. Thus the transistor will remain in the active mode with v_i having a peak value of 0.91 V. Nevertheless, to be on the safe side, we will use a somewhat lower value for $\hat{v}_i$ of approximately 0.8 V, as shown in Fig. 6.43(a), and complete the analysis of this problem utilizing the equivalent circuit in Fig. 6.42(d). The signal current in the base will be triangular, with a peak value $\hat{i}_b$ of

$$\hat{i}_b = \frac{\hat{v}_i}{R_{BB} + r_\pi} = \frac{0.8}{100 + 1.09} = 0.008 \text{ mA}$$

This triangular-wave current will be superimposed on the quiescent base current I_B, as shown in Fig. 6.43(b). The base–emitter voltage will consist of a triangular-wave component superimposed on the dc V_{BE} that is approximately 0.7 V. The peak value of the triangular waveform will be

$$\hat{v}_{be} = \hat{v}_i \frac{r_\pi}{r_\pi + R_{BB}} = 0.8 \frac{1.09}{100 + 1.09} = 8.6 \text{ mV}$$

The total v_{BE} is sketched in Fig. 6.43(c).

The signal current in the collector will be triangular in waveform, with a peak value $\hat{i}_c$ given by

$$\hat{i}_c = \beta \hat{i}_b = 100 \times 0.008 = 0.8 \text{ mA}$$

This current will be superimposed on the quiescent collector current I_C (=2.3 mA), as shown in Fig. 6.43(d).

The signal voltage at the collector can be obtained by multiplying v_i by the voltage gain; that is,

$$\hat{v}_o = 3.04 \times 0.8 = 2.43 \text{ V}$$

Figure 6.43(e) shows a sketch of the total collector voltage v_C versus time. Note the phase reversal between the input signal v_i and the output signal v_o.

Finally, we observe that each of the total quantities is the sum of a dc quantity (found from the dc circuit in Fig. 6.42b), and a signal quantity (found from the circuit in Fig. 6.42d).

Example 6.15 *continued*

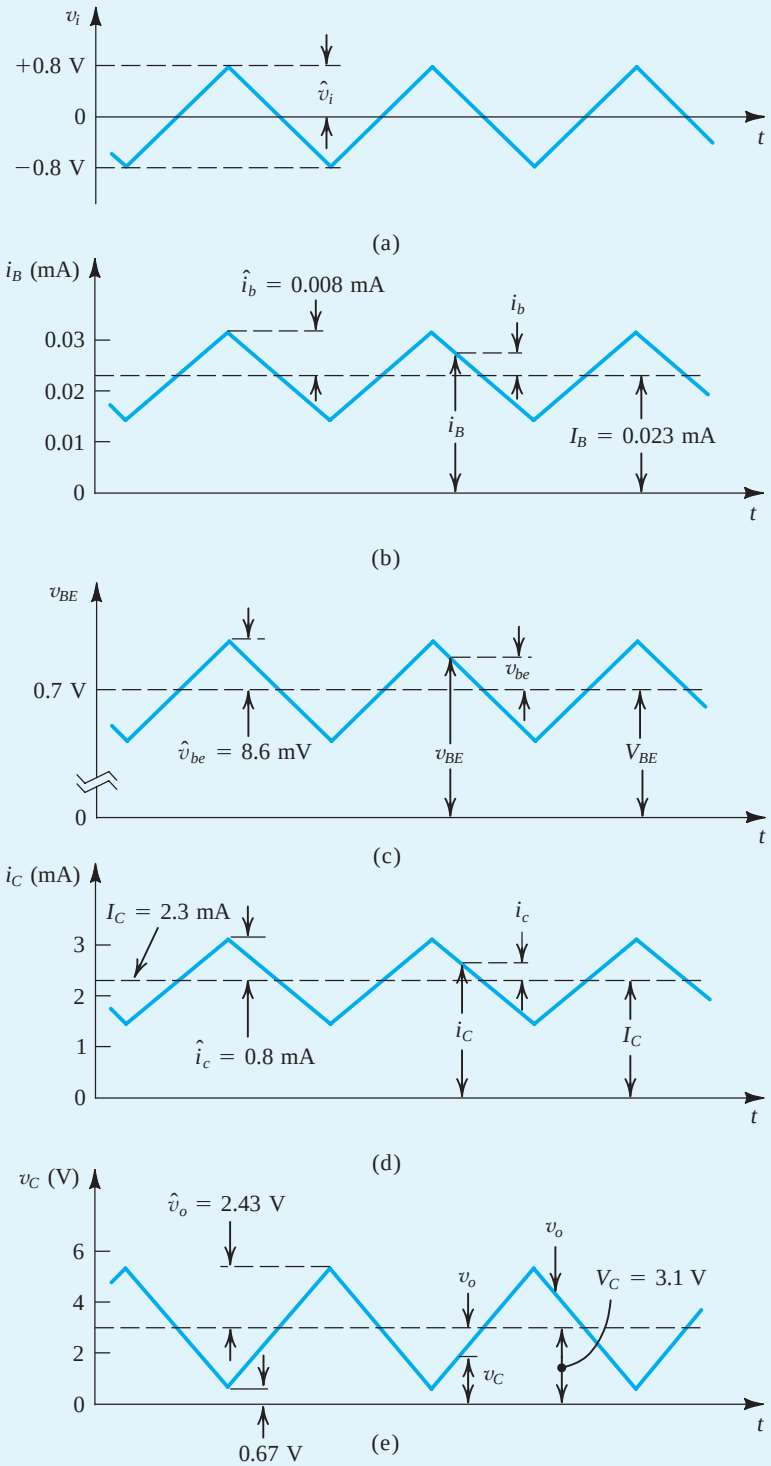


Figure 6.43 Signal waveforms in the circuit of Fig. 6.42.

Example 6.16

We need to analyze the circuit of Fig. 6.44(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by $V^+$and V^-together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system.

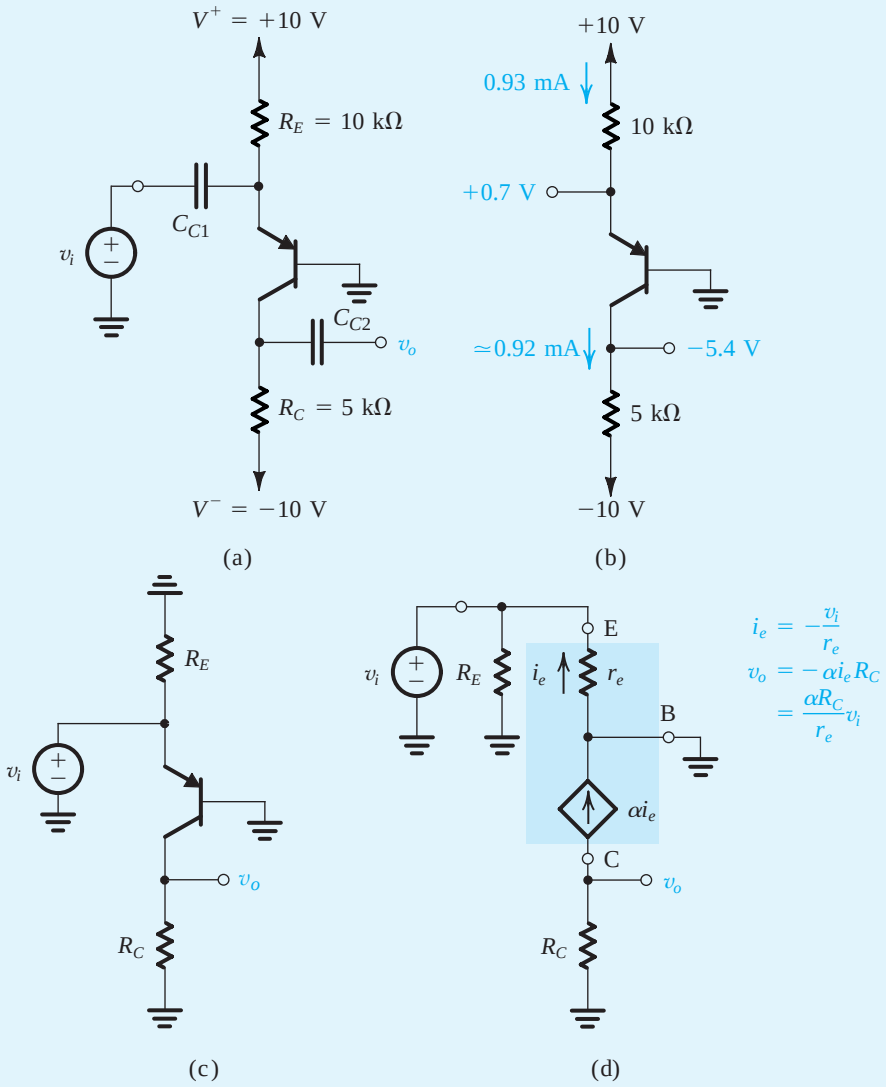


Figure 6.44 **(a)** circuit; **(b)** dc analysis; **(c)** circuit with the dc sources eliminated; **(d)** small-signal analysis using the T model for the BJT.

Example 6.16 *continued*

Solution

Here again we shall follow the five-step process outlined at the beginning of Section 6.5.9:

1. Figure 6.44(b) shows the circuit with the signal source and the coupling capacitors eliminated. The dc operating point can be determined as follows:

$$I_E = \frac{+10 - V_E}{R_E} \simeq \frac{+10 - 0.7}{10} = 0.93 \text{ mA}$$

Assuming $\beta = 100$, then $\alpha = 0.99$, and

$$I_C = 0.99 I_E = 0.92 \text{ mA}$$
$$V_C = -10 + I_C R_C$$
$$= -10 + 0.92 \times 5 = -5.4 \text{ V}$$

Thus the transistor is in the active mode.

2. We now determine the small-signal parameters as follows:

$$g_m = \frac{I_C}{V_T} = \frac{0.92}{0.025} = 36.8 \text{ mA/V}$$
$$r_e = \frac{V_T}{I_E} = \frac{0.025}{0.92} = 27.2 \ \Omega$$
$$\beta = 100 \qquad \alpha = 0.99$$
$$r_\pi = \frac{\beta}{g_m} = \frac{100}{36.8} = 2.72 \text{ k}\Omega$$

3. To prepare the circuit for small-signal analysis, we replace the dc sources with short circuits. The resulting circuit is shown in Fig. 6.44(c). Observe that we have also eliminated the two coupling capacitors, since they are assumed to be acting as perfect short circuits.
4. We are now ready to replace the BJT with one of the four equivalent circuit models of Figs. 6.40 and 6.41. Although any of the four will work, the T models of Fig. 6.41 will be more convenient because the base is grounded. Selecting the version in Fig. 6.41(b) results in the amplifier equivalent circuit shown in Fig. 6.44(d).
5. Analysis of the circuit in Fig. 6.44(d) to determine the output voltage v_o and hence the voltage gain v_o/v_i is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = 183.3 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 6.14. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the *pnp* type.

Returning to the question of allowable signal magnitude, we observe from Fig. 6.44(d) that $v_{eb} = v_i$. Thus, if small-signal operation is desired (for linearity), then the peak of v_i should be limited to approximately 10 mV. With $\hat{V}_i$ set to this value, as shown for a sine-wave input in Fig. 6.45, the peak amplitude at the collector, $\hat{V}_o$, will be

$$\hat{V}_o = 183.3 \times 0.01 = 1.833 \text{ V}$$

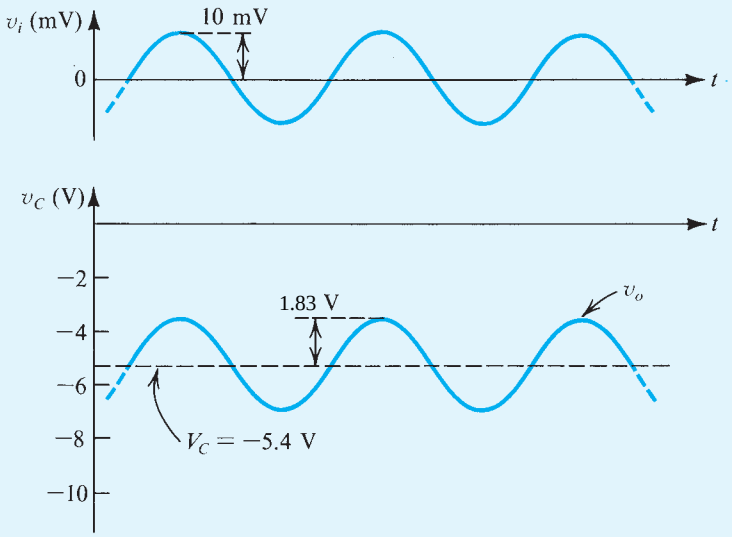


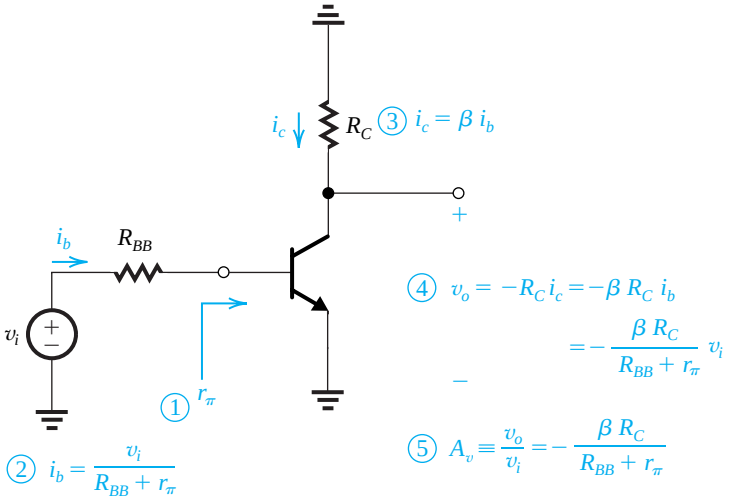
Figure 6.45 Input and output waveforms for the circuit of Fig. 6.44. Observe that this amplifier is noninverting, a property of the grounded base configuration.

EXERCISE

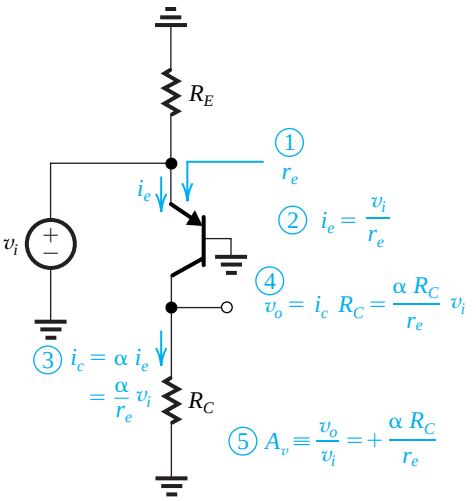
6.40 To increase the voltage gain of the amplifier analyzed in Example 6.16, the collector resistance R_C is increased to 7.5 kΩ. Find the new values of V_C, A_v, and the peak amplitude of the output sine wave corresponding to an input sine wave v_i of 10-mV peak.
Ans. –3.1 V; 275 V/V; 2.75 V

6.5.10 Performing Small-Signal Analysis Directly on the Circuit Diagram

In most cases one should explicitly replace each BJT with its small-signal model and analyze the resulting circuit, as we have done in the examples above. This systematic procedure is particularly recommended for beginning students. Experienced circuit designers, however, often perform a first-order analysis directly on the circuit. Figure 6.46 illustrates this process for the two circuits we analyzed in Examples 6.14 and 6.16. The reader is urged to follow this direct analysis procedure (the steps are numbered). Observe that the equivalent-circuit model is *implicitly* utilized; we are only saving the step of drawing the circuit with the BJT replaced by its model. Direct analysis, however, has an additional very important benefit: It



(a)



(b)

Figure 6.46 Performing signal analysis directly on the circuit diagram with the BJT small-signal model implicitly employed: (**a**) Circuit for Example 6.14; (**b**) Circuit for Example 6.16.

provides insight regarding the signal transmission through the circuit. Such insight can prove invaluable in design, particularly at the stage of selecting a circuit configuration appropriate for a given application.

6.5.11 Augmenting the Small-Signal Models to Account for the Early Effect

The Early effect, discussed in Section 6.2, causes the collector current to depend not only on v_{BE} but also on v_{CE}. The dependence on v_{CE} can be modeled by assigning a finite output resistance to the controlled current source in the hybrid-π model, as shown in Fig. 6.47. The output resistance r_o was defined in Eq. (6.19); its value is given by $r_o = V_A / I_C'$, where V_A is the Early voltage and I_C' is the dc bias current without taking the Early effect into account. We will normally drop the prime and just use $r_o = V_A / I_C$. Note that in the models of Fig. 6.47 we have renamed v_{be} as v_π, in order to conform with the literature.

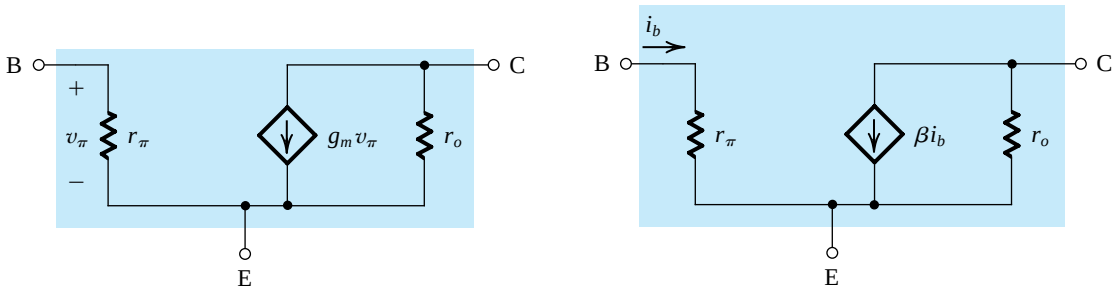


Figure 6.47 The hybrid-π small-signal model, in its two versions, with the resistance r_o included.

The question arises as to the effect of r_o on the operation of the transistor as an amplifier. In amplifier circuits in which the emitter is grounded (as in the circuit of Fig. 6.42), r_o simply appears in parallel with R_C. Thus, if we include r_o in the equivalent circuit of Fig. 6.42(d), for example, the output voltage v_o becomes

$$v_o = -g_m v_{be}(R_C \parallel r_o)$$

Thus the gain will be somewhat reduced. Obviously if $r_o \gg R_C$, the reduction in gain will be negligible, and one can ignore the effect of r_o. In general, in such a configuration r_o can be neglected if it is greater than $10R_C$.

When the emitter of the transistor is not grounded, including r_o in the model can complicate the analysis. We will make comments regarding r_o and its inclusion or exclusion on frequent occasions throughout the book. We should also note that in integrated-circuit BJT amplifiers, r_o plays a dominant role and *cannot* be neglected, as will be seen in Chapter 7. Of course, if one is performing an accurate analysis of an almost-final design using computer-aided analysis, then r_o can be easily included.

Finally, it should be noted that either of the T models in Fig. 6.41 can be augmented to account for the Early effect by including r_o between collector and emitter.

EXERCISE

6.41 The transistor in Fig. E6.41 is biased with a constant current source $I = 1$ mA and has $\beta = 100$ and $V_A = 100$ V.
(a) Find the dc voltages at the base, emitter, and collector.
(b) Find g_m, r_π, and r_o.
(c) If terminal Z is connected to ground, X to a signal source v_{sig} with a source resistance $R_{sig} = 2$ kΩ, and Y to an 8-kΩ load resistance, use the hybrid-π model of Fig. 6.47(a), to draw the small-signal equivalent circuit of the amplifier. (Note that the current source I should be replaced with an open circuit.) Calculate the overall voltage gain v_y/v_{sig}. If r_o is neglected, what is the error in estimating the gain magnitude? (*Note:* An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

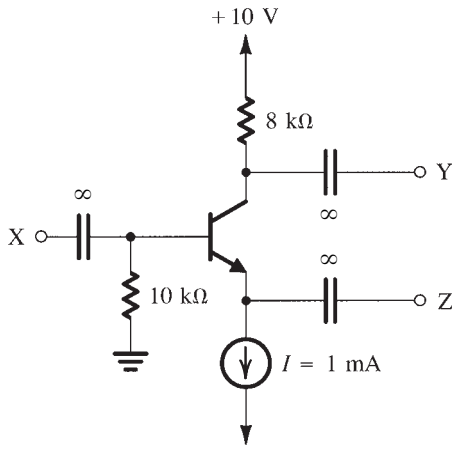


Figure E6.41

Ans. (a) –0.1 V, –0.8 V, +2 V; (b) 40 mA/V, 2.5 kΩ, 100 kΩ; (c) –77 V/V, +3.9%

6.5.12 Summary

The analysis and design of BJT amplifier circuits is greatly facilitated if the relationships between the various small-signal model parameters are at your fingertips. For easy reference, these are summarized in Table 6.4. Over time, however, we expect the reader to be able to recall these from memory. Finally, note that the material in Table 6.4 applies equally well to both the *npn* and the *pnp* transistors with no change in polarities.

6.6 Basic BJT Amplifier Configurations

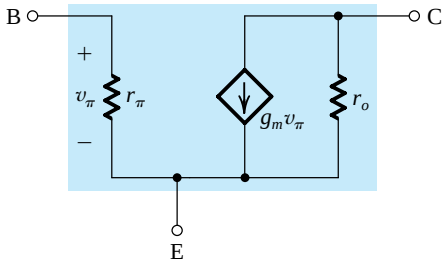
It is useful at this point to take stock of where we are and where we are going in our study of BJT amplifiers. In Section 6.4 we examined the essence of the use of the BJT as an amplifier. There we found that almost-linear amplification can be obtained by biasing the BJT at an appropriate point in its active region of operation and by keeping the signal v_{be} (or v_{π}) small. Then in Section 6.5 we took a closer look at the small-signal operation of the BJT and developed circuit models to represent the transistor, thus facilitating the determination of amplifier parameters such as voltage gain and input and output resistances.

We are now ready to consider the various possible configurations of BJT amplifiers, and we will do that in the present section. To focus our attention on the salient features of the various configurations, we shall present them in their most simple, or "stripped-down," version. Thus, we will not show the dc biasing arrangements, leaving the study of bias design to the next section. Finally, in Section 6.8 we will bring everything together and present practical circuits for discrete-circuit BJT amplifiers, namely, those amplifier circuits that can be constructed using discrete components. The study of integrated-circuit amplifiers begins in Chapter 7.

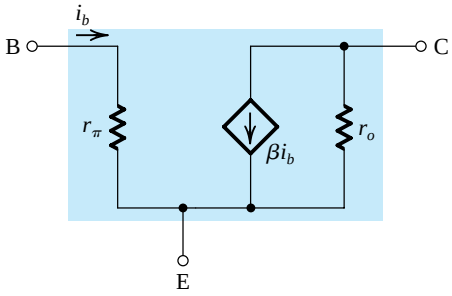
Table 6.4 Small-Signal Models of the BJT

Hybrid-π Model

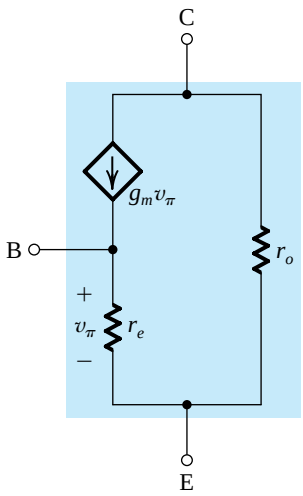
■ $(g_m v_\pi)$ Version



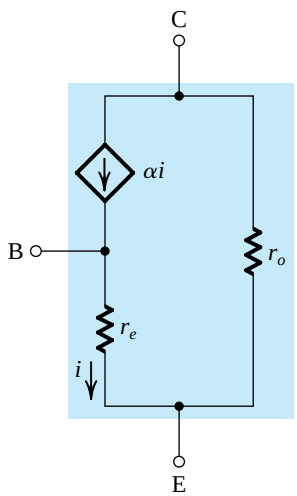
■ (βi_b) Version



■ $(g_m v_\pi)$ Version



■ (αi) Version



Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\frac{V_T}{I_C} \qquad r_\pi = \frac{V_T}{I_B} = \beta\frac{V_T}{I_C} \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

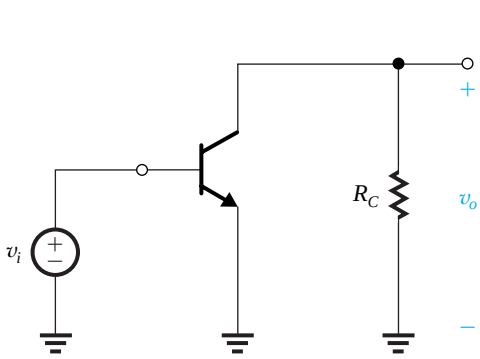
Relationships between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta+1 = \frac{1}{1-\alpha}$$

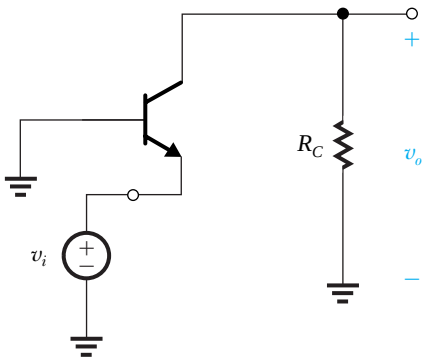
6.6.1 The Three Basic Configurations

There are three basic configurations for connecting the BJT as an amplifier. Each of these configurations is obtained by connecting one of the three BJT terminals to ground, thus creating a two-port network with the grounded terminal being *common* to the input and output ports. Figure 6.48 shows the resulting three configurations with the biasing arrangements omitted.

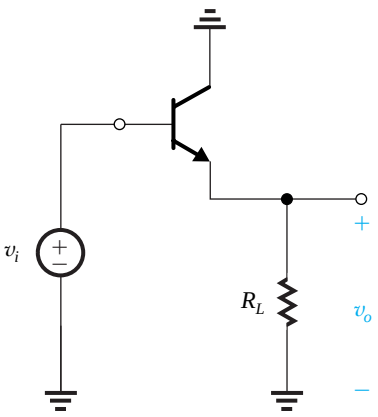
In the circuit of Fig. 6.48(a) the emitter terminal is connected to ground, the input voltage signal v_i is applied between the base and ground, and the output voltage signal v_o is taken between the collector and ground, across the resistance R_C. This configuration, therefore, is called the grounded-emitter or **common-emitter (CE)** amplifier. It is by far the most popular BJT amplifier configuration and is the one we have utilized in Sections 6.4 and 6.5 to study BJT amplifier operation.



(a) Common-Emitter (CE)



(b) Common-Base (CB)



(c) Common-Collector (CC)
or Emitter Follower

Figure 6.48 The three basic configurations of BJT amplifier. The biasing arrangements are not shown.

The **common-base (CB)** or grounded-base amplifier is shown in Fig. 6.48(b). It is obtained by connecting the base to ground, applying the input v_i between the emitter and ground, and taking the output v_o across the resistance R_C connected between the collector and ground. We have encountered a CB amplifier in Example 6.14.

Finally, Fig. 6.48(c) shows the **common-collector (CC)** or grounded-collector amplifier. It is obtained by connecting the collector terminal to ground, applying the input voltage signal v_i between base and ground, and taking the output voltage signal v_o between the emitter and ground, across a load resistance R_L. For reasons that will become apparent shortly, this configuration is more commonly called the **emitter follower**.

Our study of the three basic BJT amplifier configurations will reveal that each has distinctly different attributes and hence areas of application.[14]

6.6.2 Characterizing Amplifiers[15]

Before we begin our study of the different BJT amplifier configurations, we consider how to characterize the performance of an amplifier as a circuit building block. An introduction to this topic was presented in Section 1.5.

Figure 6.49(a) shows an amplifier fed with a signal source having an open-circuit voltage v_{sig} and an internal resistance R_{sig}. These can be the parameters of an actual signal source or, in a cascade amplifier, the Thévenin equivalent of the output circuit of another stage preceding the one under study. The amplifier is shown with a load resistance R_L connected to the output terminal. Here, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

Figure 6.49(b) shows the amplifier circuit with the amplifier block replaced by its equivalent-circuit model. The input resistance R_{in} represents the loading effect of the amplifier input on the signal source. It is found from

$$R_{in} \equiv \frac{v_i}{i_i}$$

and together with the resistance R_{sig} forms a voltage divider that reduces v_{sig} to the value v_i that appears at the input of the amplifier proper,

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} \tag{6.65}$$

It is important to note that in general R_{in} may depend on the load resistance R_L. One of the three configurations we are studying in this section, the emitter follower, exhibits such dependence.

The second parameter for characterizing amplifier performance is the **open-circuit voltage gain** A_{vo}, defined as

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

The third and final parameter is the output resistance R_o. Observe from Fig. 6.49(b) that R_o is the resistance seen looking back into the amplifier output terminal with v_i set to zero. Thus R_o can be determined, at least conceptually, as indicated in Fig. 6.49(c) with

$$R_o = \frac{v_x}{i_x}$$

[14]The CE, CB, and CC configurations are the BJT counterparts of the MOSFET CS, CG, and CD configurations, respectively.

[15]This section can be skipped if the reader has already studied Section 5.6.2; it presents substantially the same material.

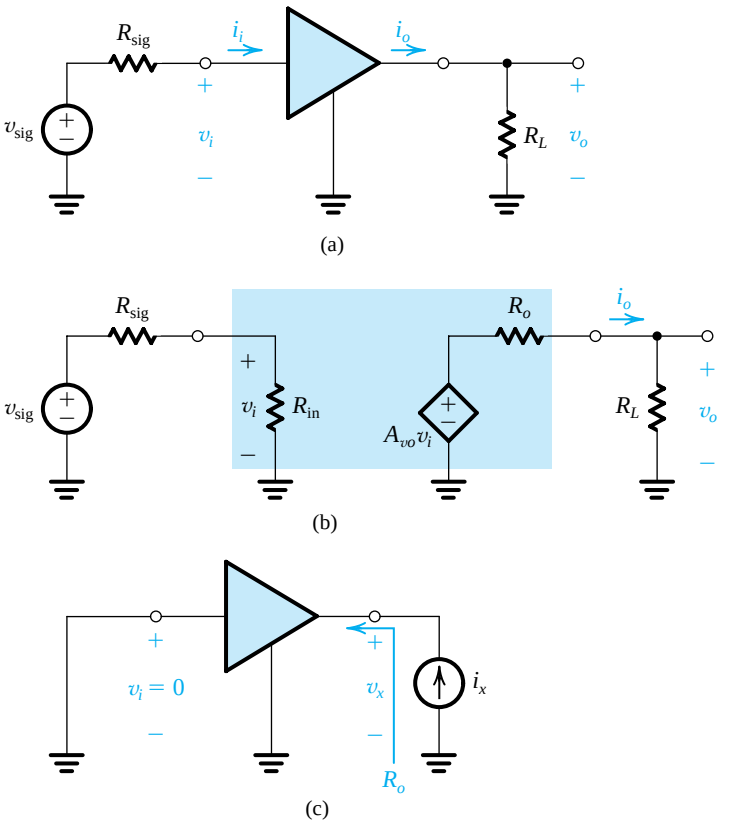


Figure 6.49 **(a)** An amplifier fed with a signal source (v_{sig}, R_{sig}) and providing its output across a load resistance R_L. **(b)** The circuit in **(a)** with the amplifier represented by its equivalent circuit model. **(c)** Determining the output resistance R_o of the amplifier.

Because R_o is determined with $v_i = 0$, its value does not depend on R_{sig}.

The controlled source $A_{vo}v_i$ and the output resistance R_o represent the Thévenin equivalent of the amplifier output circuit, and the output voltage v_o can be found from

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i \tag{6.66}$$

Thus the voltage gain of the amplifier proper, A_v, can be found as

$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \tag{6.67}$$

and the overall voltage gain G_v,

$$G_v \equiv \frac{v_o}{v_{sig}}$$

can be determined by combining Eqs. (6.65) and (6.66),

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v \tag{6.68}$$

6.6.3 The Common-Emitter (CE) Amplifier

Of the three basic BJT amplifier configurations, the common emitter is the most widely used. Typically, in an amplifier formed by cascading a number of stages, the bulk of the voltage gain is obtained by using one or more common-emitter stages in the cascade.

Figure 6.50(a) shows a common-emitter amplifier (with the biasing arrangement omitted) fed with a signal source v_{sig} having a source resistance R_{sig}. We wish to analyze the circuit to determine R_{in}, A_{vo}, R_o, and G_v. For this purpose we shall assume that R_C is part of the amplifier; thus if a load resistance R_L is connected to the amplifier output, it appears in parallel with R_C.

Characteristic Parameters of the CE Amplifier Replacing the BJT with its hybrid-π model, we obtain the CE amplifier equivalent circuit shown in Fig. 6.50(b). We shall use this equivalent circuit to determine the characteristic parameters of the amplifier R_{in}, A_{vo}, and R_o as follows.

The input resistance R_{in} is found by inspection to be

$$R_{in} = r_\pi \tag{6.69}$$

Observe that R_{in} does not depend on the output side of the amplifier; hence, this amplifier is said to be **unilateral**.

The output voltage v_o can be found by multiplying the current $(g_m v_\pi)$ by the total resistance between the output node and ground,

$$v_o = -(g_m v_\pi)(R_C \| r_o)$$

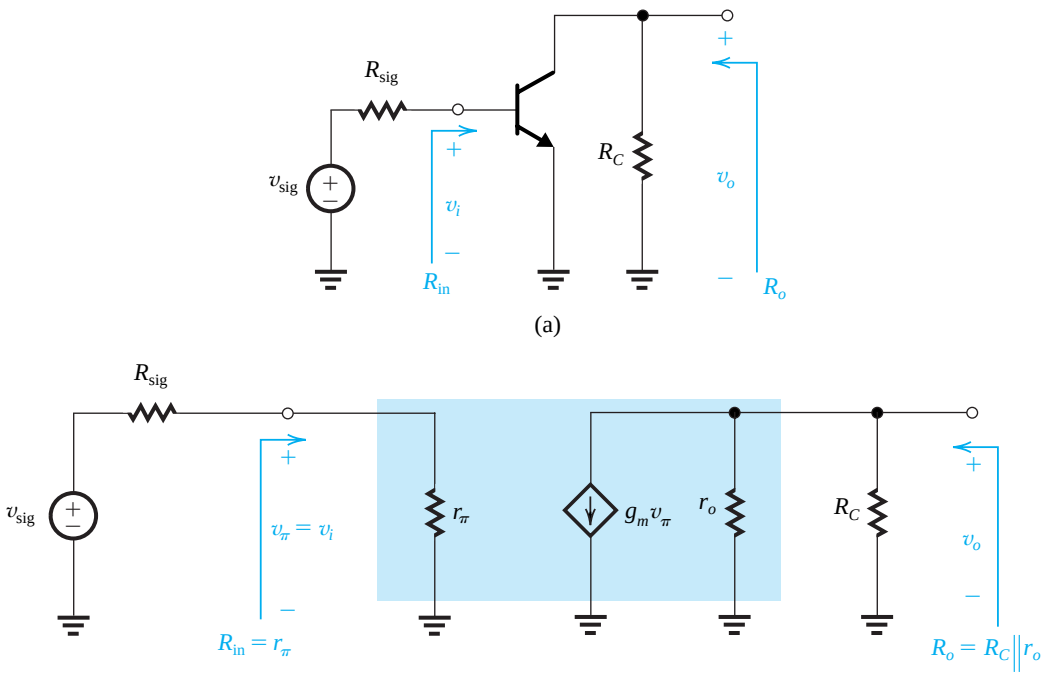


Figure 6.50 **(a)** Common-emitter amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig}. **(b)** The common-emitter amplifier circuit with the BJT relaced with its hybrid-π model.

Since $v_\pi = v_i$, the open-circuit voltage gain $A_{vo} \equiv v_o/v_i$ can be obtained as

$$A_{vo} = -g_m(R_C \| r_o) \tag{6.70}$$

Observe that the transistor output resistance r_o reduces the magnitude of the voltage gain. In discrete-circuit amplifiers, which are of interest to us in this chapter, R_C is usually much lower than r_o and the effect of r_o on reducing $|A_{vo}|$ is slight (less than 10% or so). Thus in many cases we can neglect r_o and express A_{vo} simply as

$$A_{vo} \simeq (-g_m R_C) \tag{6.71}$$

The reader is cautioned, however, that neglecting r_o is allowed only in discrete-circuit design. As will be seen in Chapter 7, r_o plays a central role in IC amplifiers.

The output resistance R_o is the resistance seen looking back into the output terminal with v_i set to zero. From Fig. 6.50(b) we see that with v_i set to zero, v_π will be zero and $g_m v_\pi$ will be zero, resulting in

$$R_o = R_C \| r_o \tag{6.72}$$

Here r_o has the beneficial effect of reducing the value of R_o. In discrete circuits, however, this effect is slight and we can make the approximation

$$R_o \simeq R_C \tag{6.73}$$

This concludes the analysis of the amplifier proper. Now, we can make the following observations:

1. The input resistance $R_{\text{in}} = r_\pi = \beta/g_m$ is moderate to low in value (typically, in the kilohm range). Obviously R_{in} is directly dependent on β and is inversely proportional to the collector bias current I_C. To obtain a higher input resistance, the bias current can be lowered, but this also lowers the gain. This is a significant design trade-off. If a much higher input resistance is desired, then a modification of the CE configuration (to be discussed shortly) or an emitter-follower stage can be employed.
2. The output resistance $R_o \simeq R_C$ is moderate to high in value (typically, in the kilohm range). Reducing R_C to lower R_o is usually not a viable proposition because the voltage gain is also reduced. Alternatively, if a very low output resistance (in the ohms to tens of ohms range) is needed, an emitter-follower stage is called for, as will be discussed in Section 6.6.6.
3. The open-circuit voltage gain A_{vo} can be high, making the CE configuration the workhorse in BJT amplifier design. Unfortunately, however, the bandwidth of the CE amplifier is severely limited. We shall study amplifier frequency response in Chapter 9.

Overall Voltage Gain To determine the overall voltage gain G_v we first determine the fraction of v_{sig} that appears at the amplifier input proper, that is, v_i;

$$v_i = v_{\text{sig}} \frac{r_\pi}{r_\pi + R_{\text{sig}}} \tag{6.74}$$

Depending on the relative values of r_π and R_{sig}, significant loss of signal strength can occur at the input, which is obviously undesirable and can be avoided by raising the input

resistance, as discussed above. At this point, we should remind the reader that to maintain a reasonably linear operation, v_i should not exceed about 5 mV to 10 mV, which poses a constraint on the value of v_{sig}.

If a load resistance R_L is connected to the output terminal of the amplifier, this resistance will appear in parallel with R_C. It follows that the voltage gain A_v can be obtained by simply replacing R_C in the expression of A_{vo} in Eq. (6.70) by $R_C \parallel R_L$,

$$A_v = -g_m(R_C \parallel R_L \parallel r_o) \tag{6.75}$$

We can now use this expression for A_v together with (v_i/v_{sig}) from Eq. (6.74) to obtain the overall voltage gain G_v as

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = -\frac{r_\pi}{r_\pi + R_{\text{sig}}}\, g_m(R_C \parallel R_L \parallel r_o) \tag{6.76}$$

EXERCISE

6.41 Use A_{vo} in Eq. (6.70) together with R_o in Eq. (6.72) to obtain A_v. Show that the result is identical to that in Eq. (6.75).

Alternative Gain Expressions There are alternative forms for A_v and G_v that can yield considerable insight besides being intuitive and easy to remember. The expression for A_v can be obtained by replacing g_m in Eq. (6.75) with α/r_e;

$$A_v = -\alpha \frac{(R_C \parallel R_L \parallel r_o)}{r_e} \tag{6.77}$$

Observing that $(R_C \parallel R_L \parallel r_o)$ is the total resistance in the collector and r_e is the total resistance in the emitter, this expression simply states that the voltage gain from base to collector is given by

$$A_v = -\alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}} \tag{6.78}$$

The reason for the factor α is that the collector current is α times the emitter current. Of course $\alpha \simeq 1$ and can usually be neglected, and the expression in Eq. (6.78) is simply stated as a resistance ratio. This expression is a general one and applies to any BJT amplifier circuit for finding the voltage gain from base to collector.

A corresponding expression for G_v can be obtained by replacing $(g_m r_\pi)$ in the numerator of Eq. (6.76) with β,

$$G_v = -\beta \frac{(R_C \parallel R_L \parallel r_o)}{R_{\text{sig}} + r_\pi} \tag{6.79}$$

which can be expressed in words as

$$G_v = -\beta \frac{\text{Total resistance in collector}}{\text{Total resistance in base}} \tag{6.80}$$

Observe that here the multiplicative factor is β, which is the ratio of i_c to i_b; this makes sense because we are using the ratio of resistances in the collector and the base. The reader is urged to reflect on these expressions while referring to Fig. 6.50.

Performing the Analysis Directly on the Circuit As mentioned in Section 6.5, with practice one can dispense with the *explicit* use of the BJT equivalent circuit and perform the analysis directly on the circuit schematic. Because in this way one remains closer to the actual circuit, this direct analysis can yield greater insight into circuit operation. Although at this stage in learning electronic circuits it is perhaps a little early to follow this direct analysis route, we show in Fig. 6.51 the CE amplifier circuit prepared for direct analysis. Observe that we have "pulled out" the resistance r_o from the transistor, thus making the transistor collector conduct $g_m v_\pi$ while still accounting for the effect of r_o.

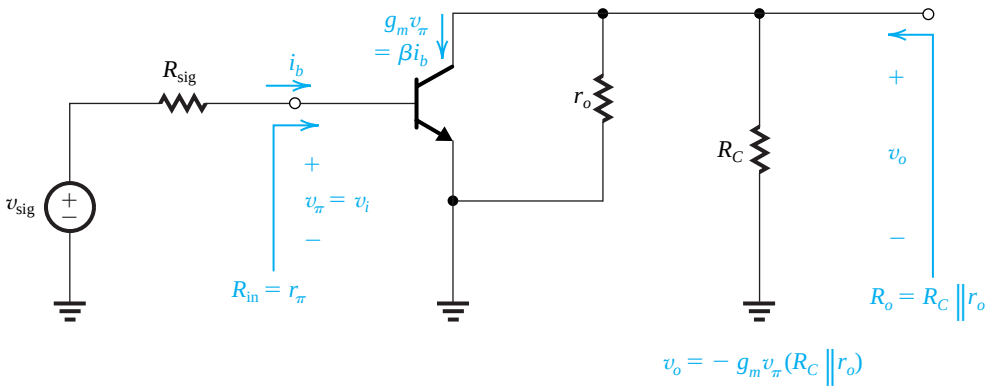


Figure 6.51 Performing the analysis directly on the circuit with the BJT model used implicitly.

Example 6.17

A CE amplifier utilizes a BJT with $\beta = 100$ and $V_A = 100$ V, is biased at $I_C = 1$ mA and has a collector resistance $R_C = 5$ kΩ. Find R_{in}, R_o, and A_{vo}. If the amplifier is fed with a signal source having a resistance of 5 kΩ, and a load resistance $R_L = 5$ kΩ is connected to the output terminal, find the resulting A_v and G_v. If $\hat{v}_\pi$ is to be limited to 5 mV, what are the corresponding $\hat{v}_{sig}$ and $\hat{v}_o$ with the load connected?

Solution

At $I_C = 1$ mA,

$$g_m = \frac{I_C}{V_T} = \frac{1 \text{ mA}}{0.025 \text{ V}} = 40 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40 \text{ mA/V}} = 2.5 \text{ kΩ}$$

$$r_o = \frac{V_A}{I_C} = \frac{100 \text{ V}}{1 \text{ mA}} = 100 \text{ kΩ}$$

The amplifier characteristic parameters can now be found as

$$R_{\text{in}} = r_\pi = 2.5 \text{ k}\Omega$$

$$A_{vo} = -g_m(R_C \| r_o)$$

$$= -40 \text{ mA/V} \qquad (5 \text{ k}\Omega \| 100 \text{ k}\Omega)$$

$$= -190.5 \text{ V/V}$$

$$R_o = R_C \| r_o$$

$$= 5 \| 100 = 4.76 \text{ k}\Omega$$

With a load resistance $R_L = 5 \text{ k}\Omega$ connected at the output, we can find A_v by either of the following two approaches:

$$A_v = A_{vo} \frac{R_L}{R_L + R_o}$$

$$= -190.5 \times \frac{5}{5 + 4.76} = -97.6 \text{ V/V}$$

or

$$A_v = -g_m(R_C \| R_L \| r_o)$$

$$= -40(5 \| 5 \| 100) = -97.6 \text{ V/V}$$

The overall voltage gain G_v can now be determined as

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_v$$

$$= \frac{2.5}{2.5 + 5} \times -97.6 = -32.5 \text{ V/V}$$

If the maximum amplitude of v_π is to be 5 mV, the corresponding value of $\hat{v}_{\text{sig}}$ will be

$$\hat{v}_{\text{sig}} = \left(\frac{R_{\text{in}} + R_{\text{sig}}}{R_{\text{in}}}\right)\hat{v}_\pi = \frac{2.5 + 5}{2.5} \times 5 = 15 \text{ mV}$$

and the amplitude of the signal at the output will be

$$\hat{v}_o = G_v \hat{v}_{\text{sig}} = 32.5 \times 0.015 = 0.49 \text{ V}$$

EXERCISE

6.42. The designer of the amplifier in Example 6.17 decides to lower the bias current to half its original value in order to raise the input resistance and hence increase the fraction of v_{sig} that appears at the input of the amplifier proper. In an attempt to maintain the voltage gain, the designer decides to double the value of R_C. For the new design, determine R_{in}, A_{vo}, R_o, A_v, and G_v. If the peak amplitude of v_π is to be limited to 5 mV, what are the corresponding values of $\hat{v}_{\text{sig}}$ and $\hat{v}_o$ (with the load connected)?

Ans. 5 kΩ; –190.5 V/V; 9.5 kΩ; –65.6 V/V; –32.8 V/V; 10 mV; 0.33 V

6.6.4 The Common-Emitter Amplifier with an Emitter Resistance

Including a resistance in the emitter as shown in Fig. 6.52(a) can lead to significant changes in the amplifier characteristics. Thus, such a resistor can be an effective design tool for tailoring the amplifier characteristics to fit the design requirements.

Analysis of the circuit in Fig. 6.52(a) can be performed by replacing the BJT with one of its small-signal models. Although any one of the models of Figs. 6.40 and 6.41 can be used, the most convenient for this application is one of the two T models. This is because the resistance R_e in the emitter will appear in series with the emitter resistance r_e of the T model and can thus be added to it, simplifying the analysis considerably. In fact, whenever there is a resistance in the emitter lead, the T model should prove more convenient to use than the hybrid-π model.

Replacing the BJT with the T model of Fig. 6.41(b) results in the amplifier small-signal, equivalent-circuit model shown in Fig. 6.52(b). Note that we have not included the BJT output resistance r_o; because this would complicate the analysis considerably. Since for the discrete amplifier at hand it turns out that the effect of r_o on circuit performance is small, we shall not include it in the analysis here. This is not the case, however, for the IC version of this circuit, and we shall indeed take r_o into account in the analysis in Chapter 7.

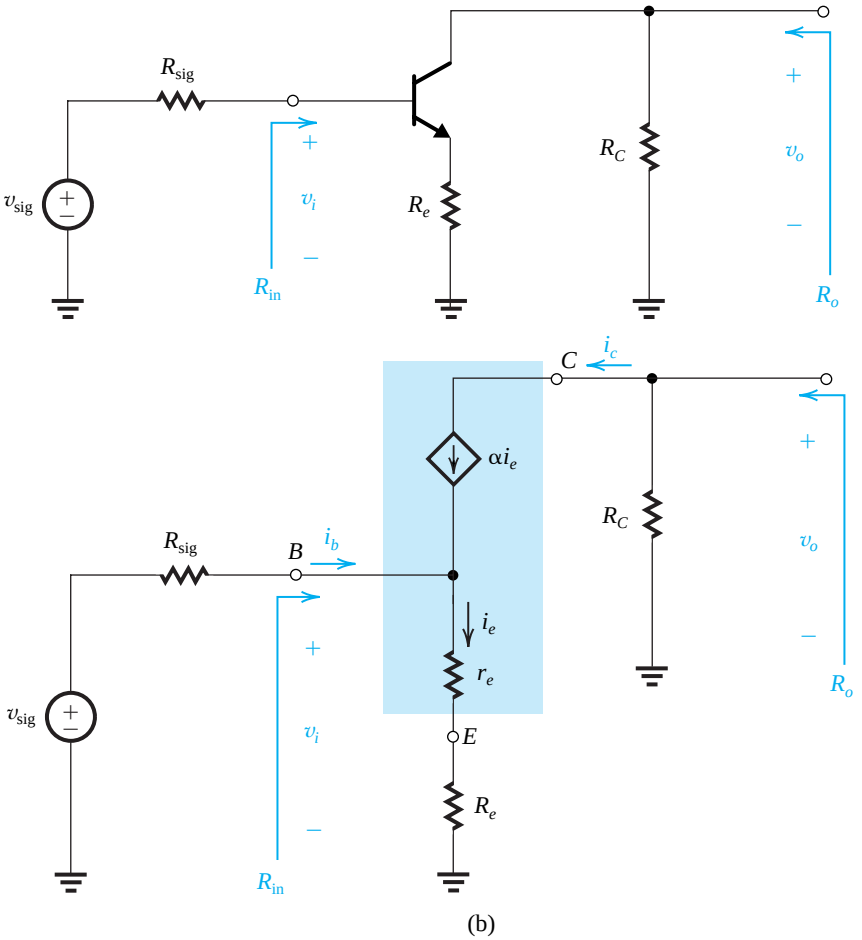


Figure 6.52 The CE amplifier with an emitter resistance R_e; **(a)** Circuit without bias details; **(b)** Equivalent circuit with the BJT replaed with its T model.

To determine the amplifier input resistance R_{in}, we note from Fig. 6.52(b) that

$$R_{\text{in}} \equiv \frac{v_i}{i_b}$$

where

$$i_b = (1-\alpha)i_e = \frac{i_e}{\beta+1} \tag{6.81}$$

and

$$i_e = \frac{v_i}{r_e + R_e} \tag{6.82}$$

Thus,

$$R_{\text{in}} = (\beta+1)(r_e + R_e) \tag{6.83}$$

This is a very important result. It states that *the input resistance looking into the base is* $(\beta+1)$ *times the total resistance in the emitter*, and is known as the **resistance-reflection rule**. The factor $(\beta+1)$ arises because the base current is $1/(\beta+1)$ times the emitter current. The expression for R_{in} in Eq. (6.83) shows clearly that including a resistance R_e in the emitter can substantially increase R_{in}. Indeed, the value of R_{in} is increased by the ratio

$$\frac{R_{\text{in}}(\text{with } R_e \text{ included})}{R_{\text{in}}(\text{without } R_e)} = \frac{(\beta+1)(r_e+R_e)}{(\beta+1)r_e}$$

$$= 1 + \frac{R_e}{r_e} \simeq 1 + g_m R_e \tag{6.84}$$

Thus the circuit designer can use the value of R_e to control the value of R_{in}.

To determine the voltage gain A_{vo}, we see from Fig. 6.52(b) that

$$v_o = -i_c R_C$$

$$= -\alpha i_e R_C$$

Substituting for i_e from Eq. (6.82) gives

$$A_{vo} = -\alpha \frac{R_C}{r_e + R_e} \tag{6.85}$$

which is a simple application of the general expression in Eq. (6.78). Here, of course, the total resistance in the emitter is $r_e + R_e$.

The open-circuit voltage gain in Eq. (6.85) can be expressed alternatively as

$$A_{vo} = -\frac{\alpha}{r_e} \frac{R_C}{1 + R_e/r_e}$$

$$A_{vo} = -\frac{g_m R_C}{1 + R_e/r_e} \simeq -\frac{g_m R_C}{1 + g_m R_e} \tag{6.86}$$

Thus, including R_e reduces the voltage gain by the factor $(1 + g_m R_e)$, which is the same factor by which R_{in} is increased. This points out an interesting trade-off between gain and input resistance, a trade-off that the designer can exercise through the choice of an appropriate value for R_e.

The output resistance R_o can be found from the circuit in Fig. 6.52(b) by inspection:

$$R_o = R_C$$

If a load resistance R_L is connected at the amplifier output, A_v can be found as

$$\begin{aligned} A_v &= A_{vo}\frac{R_L}{R_L + R_o} \\ &= -\alpha\frac{R_C}{r_e + R_e}\frac{R_L}{R_L + R_C} \\ &= -\alpha\frac{R_C \parallel R_L}{r_e + R_e} \end{aligned} \tag{6.87}$$

which could have been written directly using Eq. (6.78). The overall voltage gain G_v can now be found:

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \times -\alpha\frac{R_C \parallel R_L}{r_e + R_e}$$

Substituting for R_{in} from Eq. (6.83) and replacing α with $\beta/(\beta+1)$ results in

$$G_v = -\beta\frac{R_C \parallel R_L}{R_{\text{sig}} + (\beta+1)(r_e + R_e)} \tag{6.88}$$

which is a direct application of the general expression presented in Eq. (6.80). We observe that the overall voltage gain G_v is lower than the value without R_e because of the additional term $(\beta+1)R_e$ in the denominator. The gain, however, is less sensitive to the value of β, a desirable result.

Another important consequence of including the resistance R_e in the emitter is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion. This is because only a fraction of the input signal at the base, v_i, appears between the base and the emitter. Specifically, from the circuit in Fig. 6.52(b), we see that

$$\frac{v_\pi}{v_i} = \frac{r_e}{r_e + R_e} \simeq \frac{1}{1 + g_m R_e} \tag{6.89}$$

Thus, for the same v_π, the signal at the input terminal of the amplifier, v_i, can be greater than for the CE amplifier by the factor $(1 + g_m R_e)$.

To summarize, including a resistance R_e in the emitter of the CE amplifier results in the following characteristics:

1. The input resistance R_{in} is increased by the factor $(1 + g_m R_e)$.
2. The voltage gain from base to collector, A_v, is reduced by the factor $(1 + g_m R_e)$.
3. For the same nonlinear distortion, the input signal v_i can be increased by the factor $(1 + g_m R_e)$.
4. The overall voltage gain is less dependent on the value of β.
5. The high-frequency response is significantly improved (as we shall see in Chapter 9).

With the exception of gain reduction, these characteristics represent performance improvements. Indeed, the reduction in gain is the price paid for obtaining the other performance improvements. In many cases this is a good bargain; it is the underlying philosophy for the use of negative feedback. That the resistance R_e introduces negative feedback in the amplifier circuit can be seen by reference to Fig. 6.52(a): While keeping v_i constant, assume that for some reason the collector current increases; the emitter current also will increase, resulting in an increased voltage drop across R_e. Thus the emitter voltage rises, and the base–emitter voltage decreases. The latter effect causes the collector current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 10, where we shall study negative

feedback formally, we will find that the factor $(1 + g_m R_e)$, which appears repeatedly, is the "amount of negative-feedback" introduced by R_e. Finally, we note that the negative-feedback action of R_e gives it the name **emitter degeneration resistance**.

Example 6.18

For the CE amplifier specified in Example 6.17, what value of R_e is needed to raise R_{in} to a value four times that of R_{sig}? With R_e included, find A_{vo}, R_o, A_v, and G_v. Also, if $\hat{v}_\pi$ is limited to 5 mV, what are the corresponding values of $\hat{v}_{\text{sig}}$ and $\hat{v}_o$?

Solution

To obtain $R_{\text{in}} = 4\,R_{\text{sig}} = 4 \times 5 = 20\ \text{k}\Omega$, the required R_e is found from

$$20 = (\beta + 1)\ (r_e + R_e)$$

With $\beta = 100$,

$$r_e + R_e \simeq 200\ \Omega$$

Thus,

$$R_e = 200 - 25 = 175\ \Omega$$

$$A_{vo} = -\alpha\ \frac{R_C}{r_e + R_e}$$

$$\simeq \left(-\frac{5000}{25 + 175}\right) = -25\ \text{V/V}$$

$$R_o = R_C = 5\ \text{k}\Omega\ \text{(unchanged)}$$

$$A_v = A_{vo}\ \frac{R_L}{R_L + R_o} = -25 \times \frac{5}{5 + 5} = -12.5\ \text{V/V}$$

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}\ A_v = -\frac{20}{20 + 5} \times 12.5 = -10\ \text{V/V}$$

For $\hat{v}_\pi = 5$ mV,

$$\hat{v}_i = \hat{v}_\pi \left(\frac{r_e + R_e}{r_e}\right)$$

$$= 5\left(1 + \frac{175}{25}\right) = 40\ \text{mV}$$

$$\hat{v}_{\text{sig}} = \hat{v}_i\ \frac{R_{\text{in}} + R_{\text{sig}}}{R_{\text{in}}}$$

$$= 40\left(1 + \frac{5}{20}\right) = 50\ \text{mV}$$

$$\hat{v}_o = \hat{v}_{\text{sig}} \times |G_v|$$

$$= 50 \times 10 = 500\ \text{mV} = 0.5\ \text{V}$$

Thus, while $|G_v|$ has decreased to about a third of its original value, the amplifier is able to produce as large an output signal as before for the same nonlinear distortion.

EXERCISE

6.43 Show that with R_e included, and v_π limited to a maximum value $\hat{v}_\pi$, the maximum allowable input signal, $\hat{v}_{sig}$, is given by

$$\hat{v}_{sig} = \hat{v}_\pi\left(1 + \frac{R_e}{r_e} + \frac{R_{sig}}{r_\pi}\right)$$

If the transistor is biased at $I_C = 0.5$ mA and has a β of 100, what value of R_e is needed to permit an input signal $\hat{v}_{sig}$ of 100 mV from a source with a resistance $R_{sig} = 10$ kΩ while limiting $\hat{v}_\pi$ to 10 mV? What is R_{in} for this amplifier? If the total resistance in the collector is 10 kΩ, what G_v value results?

Ans. 350 Ω ; 40.4 kΩ ; –19.8 V/V

6.6.5 The Common-Base (CB) Amplifier

Figure 6.53(a) shows a common-base amplifier with the biasing circuit omitted. The amplifier is fed with a signal source characterized by v_{sig} and R_{sig}. Since R_{sig} appears in series with the emitter, it is more convenient to represent the transistor with the T model than with the hybrid-π model. Doing this, we obtain the amplifier equivalent circuit shown in Fig. 6.53(b). Note that we have not included r_o. This is because including r_o would complicate the analysis considerably, for it would appear between the output and input of the amplifier. Fortunately, it turns out that the effect of r_o on the performance of a discrete CB amplifier is very small. We will consider the effect of r_o when we study the IC form of the CB amplifier in Chapter 7.

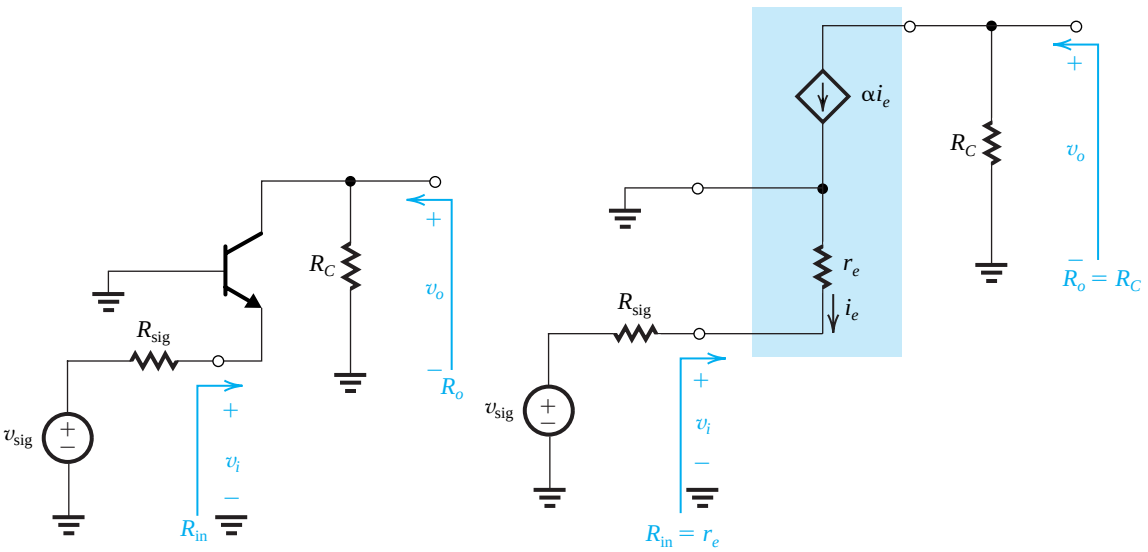


Figure 6.53 (**a**) CB amplifier with bias details omitted; (**b**) Amplifier equivalent circuit with the BJT represented by its T Model.

From inspection of the equivalent circuit in Fig. 6.53(b), we see that the input resistance is

$$R_{\text{in}} = r_e \tag{6.90}$$

This should have been expected, since we are looking into the emitter and the base is grounded. Typically r_e is a few ohms to a few tens of ohms; thus the CB amplifier has a low input resistance.

To determine the voltage gain, we write at the collector node

$$v_o = -\alpha i_e R_C$$

and substitute for the emitter current from

$$i_e = -\frac{v_i}{r_e}$$

to obtain

$$A_{vo} \equiv \frac{v_o}{v_i} = \frac{\alpha}{r_e} R_C = g_m R_C \tag{6.91}$$

which except for its positive sign is identical to the expression for A_{vo} for the CE amplifier.

The output resistance of the CB circuit can be found by inspection of the circuit in Fig. 6.53(b) as

$$R_o = R_C \tag{6.92}$$

which is the same as in the case of the CE amplifier (with r_o neglected).

Although the gain of the CB amplifier proper has the same magnitude as that of the CE amplifier, this is usually not the case for the overall voltage gain. The low input resistance of the CB amplifier can cause the input signal to be severely attenuated, specifically,

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{sig}} + R_{\text{in}}} = \frac{r_e}{R_{\text{sig}} + r_e} \tag{6.93}$$

from which we see that except for situations in which R_{sig} is on the order of r_e, the signal transmission factor v_i/v_{sig} can be very small. It is useful at this point to mention that one of the applications of the CB circuit is to amplify high-frequency signals that appear on a coaxial cable. To prevent signal reflection on the cable, the CB amplifier is required to have an input resistance equal to the characteristic resistance of the cable, which is usually in the range of 50 Ω to 75 Ω.

If a load resistance R_L is connected to the amplifier output terminal, it will appear in parallel with R_C and thus A_v can be determined as

$$A_v = g_m(R_C \parallel R_L)$$

The overall voltage gain G_v can now be obtained by multiplying A_v with the expression for v_i/v_{sig} in Eq. (6.93),

$$\begin{aligned} G_v &= \frac{r_e}{R_{\text{sig}} + r_e}\, g_m(R_C \parallel R_L) \\ &= \alpha\, \frac{R_C \parallel R_L}{R_{\text{sig}} + r_e} \end{aligned} \tag{6.94}$$

Since $\alpha \simeq 1$, we see that the overall voltage gain is simply the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit. We also note that the overall

voltage gain is almost independent of the value of β (except through the small dependence of α on β), a desirable property. Observe that for R_{sig} of the same order as R_C and R_L, the gain will be very small.

In summary, the CB amplifier exhibits a very low input resistance (r_e), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE amplifier $(g_m R_C)$, and, like the CE amplifier, a relatively high output resistance (R_C). Because of its very low input resistance, the CB circuit *alone* is not attractive as a voltage amplifier except in specialized applications, such as the cable amplifier mentioned above. The CB amplifier has excellent high-frequency performance, which as we shall see in Chapters 7 and 9, makes it useful in combination with other circuits in the implementation of high-frequency amplifiers.

EXERCISES

6.44 Consider a CB amplifier utilizing a BJT biased at $I_C = 1$ mA and with $R_C = 5$ kΩ. Determine R_{in}, A_{vo}, and R_o, If the amplifier is loaded in $R_L = 5$ kΩ, what value of A_v results? What G_v is obtained if $R_{sig} = 5$ kΩ?

Ans. 25 Ω; 200 V/V; 5 kΩ; 100 V/V; 0.5 V/V

6.45 A CB amplifier is required to amplify a signal delivered by a coaxial cable having a characteristic resistance of 50 Ω. What bias current I_C should be utilized to obtain R_{in} that is matched to the cable resistance? To obtain an overall voltage gain of G_v of 40 V/V, what should the total resistance in the collector (i.e., $R_C \parallel R_L$) be?

Ans. 0.5 mA; 4 kΩ

6.6.6 The Common-Collector Amplifier or Emitter Follower

The last of the basic BJT amplifier configurations is the common-collector amplifier, a very important circuit that finds frequent application in the design of both small-signal amplifiers and amplifiers that are required to handle large signals and deliver substantial amounts of signal power to a load. This latter variety will be studied in Chapter 11. As well, the common-collector amplifier is utilized in a significant family of digital logic circuits (Chapter 14). The circuit is more commonly known by the alternative name *emitter follower*; the reason for this will become apparent shortly.

The Need for Voltage Buffers Before delving into the analysis of the emitter follower, it is useful to look at one of its most common applications. Consider the situation depicted in Fig. 6.54(a). A signal source delivering a signal of reasonable strength (200 mV) with an internal resistance of 100 kΩ, is to be connected to a 1-kΩ load resistance. Connecting the source to the load directly as in Fig. 6.54(b) would result in severe attenuation of the signal; the signal appearing across the load will be only $1/(100 + 1)$ of the input signal, or about 2 mV.

An alternative course of action is suggested in Fig. 6.54(c). Here we have interposed an amplifier between the source and the load. Our amplifier, however, is unlike the amplifiers we have been studying in this chapter thus far; it has a voltage gain of unity. This is because our signal is already of sufficient strength and we do not need to increase its amplitude. Note, however, that our amplifier has an input resistance of 100 kΩ; thus half the input signal (100 mV) will appear at the input of the amplifier proper. Since the amplifier has a low

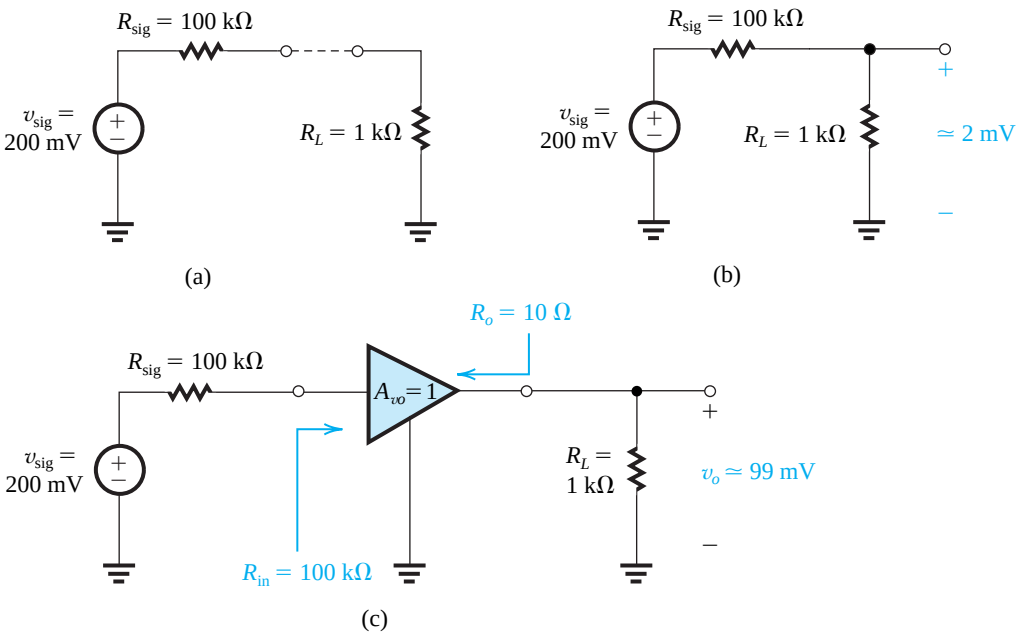


Figure 6.54 Illustrating the need for a unity-gain buffer amplifer.

output resistance (10 Ω), 99% of this signal (99 mV) will appear at the output. This is a significant improvement over the situation with the source connected directly to the load. As will be seen shortly, the emitter follower can easily implement the unity-gain **buffer amplifier** shown in Fig. 6.54(c).

Characteristic Parameters of the Emitter Follower Figure 6.55(a) shows a common-collector amplifier or emitter follower, as we will refer to it henceforth. Note that the biasing circuit is not shown. The emitter follower is fed with a signal source (v_{sig}, R_{sig}) and has a load resistance R_L connected between emitter and ground. To keep things simple, we are assuming that R_L includes both the actual load and any other resistance that may be present between emitter and ground. Normally the actual R_L would be much lower in value than such other resistances and thus would dominate.

Since the BJT has a resistance R_L connected in its emitter, it is most convenient to use the T model to represent the BJT. Doing this results in the emitter-follower equivalent circuit shown in Fig. 6.55(b). We have included r_o simply because it is very easy to do so. However, note that r_o appears in parallel with R_L, and in discrete circuits is much larger than R_L and can thus be neglected. The resulting simplified circuit shown in Fig. 6.55(c), can now be used to determine the characteristic parameters of the amplifier.

The input resistance R_{in} is found from

$$R_{in} = \frac{v_i}{i_b}$$

Substituting for $i_b = i_e/(\beta + 1)$ where i_e is given by

$$i_e = \frac{v_i}{r_e + R_L}$$

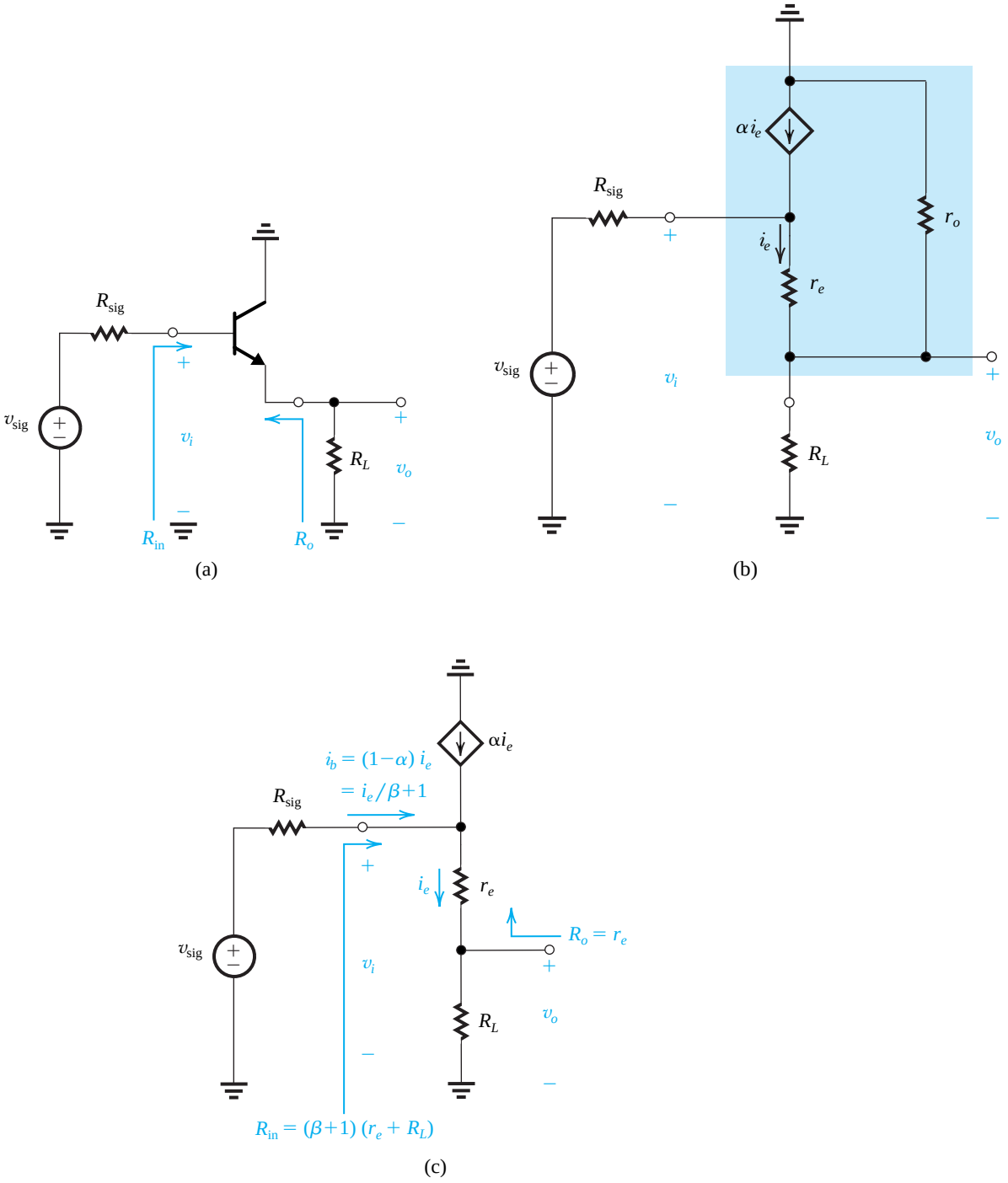


Figure 6.55 **(a)** Common-collector amplifier or emitter-follower. **(b)** Equivalent circuit obtained by replacing the BJT with its T model. Note that r_o appears in parallel with R_L. Since in discrete circuits $r_0 \gg R_L$, we shall neglect it, thus obtaining the simplified circuit in **(c)**.

we obtain

$$R_{\text{in}} = (\beta+1)(r_e + R_L) \tag{6.95}$$

a result that we could have written directly, utilizing the resistance-reflection rule. Note that as expected the emitter follower takes the low load resistance and reflects it to the base side, where the signal source is, after increasing its value by a factor $(\beta+1)$. It is this impedance transformation property of the emitter follower that makes it useful in connecting a low-resistance load to a high-resistance source, that is, to implement a buffer amplifier.

The voltage gain A_v is given by

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + r_e} \tag{6.96}$$

Setting $R_L = \infty$ yields A_{vo},

$$A_{vo} = 1 \tag{6.97}$$

Thus, as expected, the open-circuit voltage gain of the emitter follower proper is unity[16] which means that the signal voltage at the emitter *follows* that at the base; which is the origin of the name "emitter follower."

To determine R_o, refer to Fig. 6.55(c) and look back into the emitter (i.e., behind or excluding R_L) while setting $v_i = 0$ (i.e., grounding the base). You will see r_e of the BJT, thus

$$R_o = r_e \tag{6.98}$$

This result together with $A_{vo} = 1$ yields A_v in Eq. (6.96), thus confirming our earlier analysis.

Overall Voltage Gain We now proceed to determine the overall voltage gain G_v, as follows:

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}$$

$$= \frac{(\beta+1)(r_e + R_L)}{(\beta+1)(r_e + R_L) + R_{\text{sig}}}$$

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times A_v$$

Substituting for A_v from Eq. (6.96), results in

$$G_v = \frac{(\beta+1)R_L}{(\beta+1)R_L + (\beta+1)r_e + R_{\text{sig}}} \tag{6.99}$$

This equation indicates that the overall gain, though lower than one, can be close to one if $(\beta+1)R_L$ is larger or comparable in value to R_{sig}. This again confirms the action of the emitter follower in delivering a large proportion of v_{sig} to a low-valued load resistance R_L even though R_{sig} can be much larger than R_L. The key point is that R_L is multiplied by $(\beta+1)$

[16] In practice, the value of A_{vo} will be lower than, but close to unity. For one thing, r_o, which we have neglected, would make $A_{vo} = r_o/(r_o + r_e)$. Also, as already mentioned, there may be other resistances (e.g., for biasing purposes) attached to the emitter.

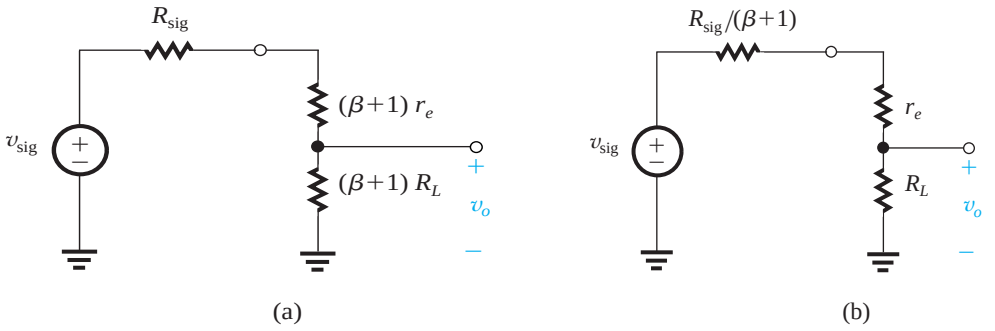


Figure 6.56 Simple equivalent circuits for the emitter follower obtained by **(a)** reflecting r_e and R_L to the base side, and **(b)** reflecting v_{sig} and R_{sig} to the emitter side. Note that the circuit in **(b)** can be obtained from that in **(a)** by simply dividing all resistances by $(\beta+1)$.

before it is "presented to the source." Figure 6.56(a) shows an equivalent circuit of the emitter follower obtained by simply reflecting r_e and R_L to the base side. The overall voltage gain $G_v \equiv v_o/v_{sig}$ can be determined directly and very simply from this circuit by using the voltage divider rule. The result is the expression for G_v already given in Eq. (6.99).

Dividing all resistances in the circuit of Fig. 6.56(a) by $\beta+1$ does not change the voltage ratio v_o/v_{sig}. Thus we obtain another equivalent circuit, shown in Fig. 6.56(b), that can be used to determine $G_v \equiv v_o/v_{sig}$ of the emitter follower. A glance at this circuit reveals that it is simply the equivalent circuit obtained by reflecting v_{sig} and R_{sig} from the base side to the emitter side. In this reflection, v_{sig} does not change, but R_{sig} is divided by $\beta+1$. Thus, we either reflect to the base side and obtain the circuit in Fig. 6.56(a) or reflect to the emitter side and obtain the circuit in Fig. 6.56(b). From the latter, G_v can be found as

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + r_e + R_{sig}/(\beta+1)} \tag{6.100}$$

Observe that this expression is the same as that in Eq. (6.99) except for dividing both the numerator and denominator by $\beta+1$.

The expression for G_v in Eq. (6.100) has an interesting interpretation: The emitter follower reduces R_{sig} by the factor $(\beta+1)$ before "presenting it to the load resistance R_L": an impedance transformation that has the same buffering effect.

At this point it is important to note that although the emitter follower does not provide voltage gain it has a current gain of $\beta+1$.

Thévenin Representation of the Emitter-Follower Output A more general representation of the emitter-follower output is shown in Fig. 6.57(a). Here G_{vo} is the overall open-circuit voltage gain that can be obtained by setting $R_L = \infty$ in the circuit of Fig. 6.56(b), as illustrated in Fig. 6.57(b). The result is $G_{vo} = 1$. The output resistance R_{out} is *different* from R_o. To determine R_{out} we set v_{sig} to zero (rather than setting v_i to zero). Again we can use the equivalent circuit in Fig. 6.56(b) to do this, as illustrated in Fig. 6.57(c). We see that

$$R_{out} = r_e + \frac{R_{sig}}{\beta+1} \tag{6.101}$$

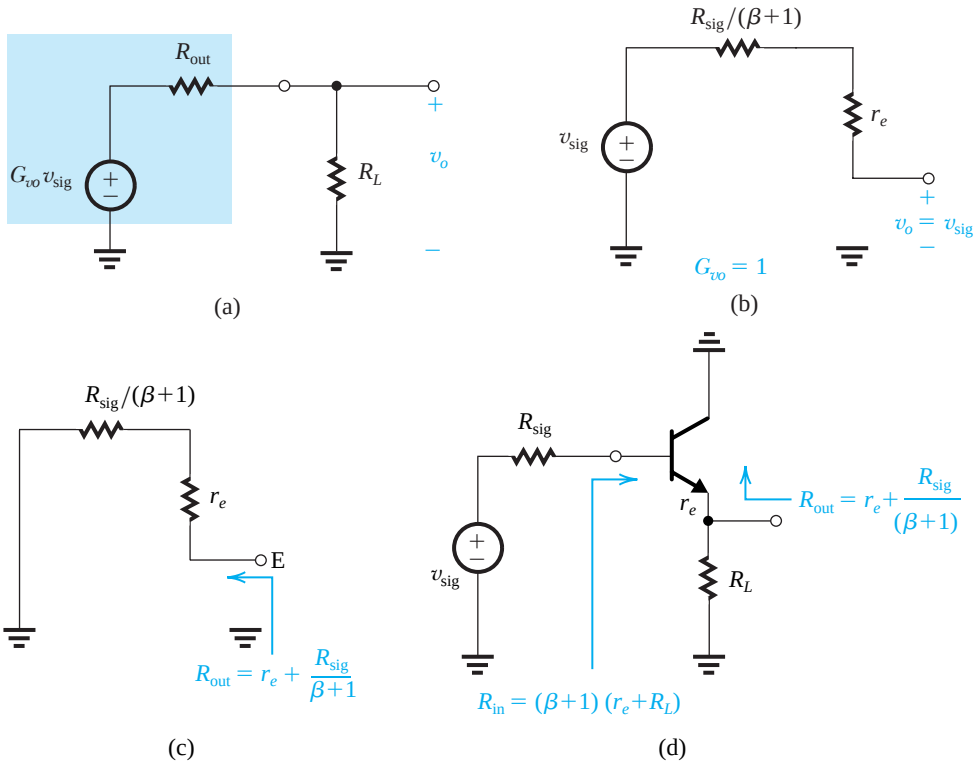


Figure 6.57 **(a)** Thévenin representation of the output of the emitter follower. (**b**) Obtaining G_{vo} from the equivalent circuit in Fig. 6.56(b). **(c)** Obtaining R_{out} from the equivalent circuit in Fig. 6.56(b) with v_{sig} set to zero. **(d)** The emitter follower with R_{in} and R_{out} determined simply by looking into the input and output terminals, respectively.

Finally, we show in Fig. 6.57(d) the emitter-follower circuit together with its R_{in} and R_{out}. Observe that R_{in} is determined by reflecting r_e and R_L to the base side (by multiplying their values by $\beta+1$). To determine R_{out}, grab hold of the emitter and walk (or just look!) backward while $v_{sig} = 0$. You will see r_e in series with R_{sig}, which because it is in the base must be divided by $(\beta+1)$.

We note that unlike the CE and CB amplifiers we studied earlier, the emitter follower is *not* unilateral. This is manifested by the fact that R_{in} depends on R_L and R_{out} depends on R_{sig}.

Example 6.19

It is required to design an emitter follower to implement the buffer amplifier of Fig. 6.54(c). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{sig} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 kΩ, and to 0.5 kΩ.

Example 6.19 *continued*

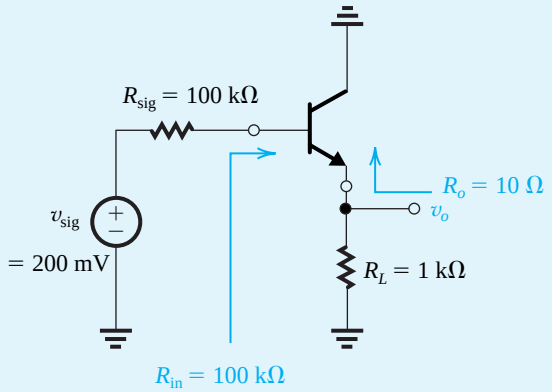


Figure 6.58 Circuit for Example 6.19.

Solution

The emitter-follower circuit is shown in Fig. 6.58. To obtain $R_o = 10\ \Omega$, we bias the transistor to obtain $r_e = 10\ \Omega$. Thus,

$$10\ \Omega = \frac{V_T}{I_E}$$
$$I_E = 2.5\ \text{mA}$$

The input resistance R_{in} will be

$$R_{in} = (\beta + 1)(r_e + R_L)$$
$$100 = (\beta + 1)(0.01 + 1)$$

Thus, the BJT should have a β with a minimum value of 98. A higher β would obviously be beneficial.

The overall voltage gain can be determined from

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + r_e + \dfrac{R_{sig}}{(\beta + 1)}}$$

Assuming $\beta = 100$, the value of G_v obtained is

$$G_v = 0.5$$

Thus when $v_{sig} = 200$ mV, the signal at the output will be 100 mV. Since the 100 mV appears across the 1-kΩ load, the signal across the base–emitter junction can be found from

$$v_\pi = \frac{v_o}{R_L} \times r_e$$
$$= \frac{100}{1000} \times 10 = 1\ \text{mV}$$

If $\hat{v}_\pi = 5$ mV then v_{sig} can be increased by a factor of 5, resulting in $\hat{v}_{sig} = 1$ V.

To obtain v_o as the load is varied, we use the Thévenin equivalent of the emitter follower, shown in Fig. 6.57(a) with $G_{vo} = 1$ and

$$R_{out} = \frac{R_{sig}}{\beta + 1} + r_e = \frac{100}{101} + 0.01 = 1\ \text{k}\Omega$$

to obtain

$$v_o = v_{\text{sig}} \frac{R_L}{R_L + R_{\text{out}}}$$

For $R_L = 2\ \text{k}\Omega$,

$$v_o = 200\ \text{mV} \times \frac{2}{2+1} = 133.3\ \text{mV}$$

and for $R_L = 0.5\ \text{k}\Omega$,

$$v_o = 200\ \text{mV} \times \frac{0.5}{0.5+1} = 66.7\ \text{mV}$$

EXERCISE

6.46 An emitter follower utilizes a transistor with $\beta = 100$ and is biased at $I_C = 5$ mA. It operates between a source having a resistance of 10 kΩ and a load of 1 kΩ. Find R_{in}, G_{vo}, R_{out}, and G_v. What is the peak amplitude of v_{sig} that results in v_π having a peak amplitude of 5 mV? Find the resulting peak amplitude at the output.

Ans. 101.5 kΩ; 1 V/V; 104 Ω; 0.91 V/V; 1.1 V; 1 V

6.6.7 Summary and Comparisons

For easy reference and to enable comparisons, we present in Table 6.5 the formulas for determining the characteristic parameters of discrete BJT amplifiers. Note that r_o has been neglected throughout. As has already been mentioned, this is possible in discrete-circuit amplifiers. In addition to the remarks made throughout this section about the characteristics and applicability of the various configurations, we make the following concluding points.

1. The CE configuration is the one best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
2. Including a resistor R_e in the emitter lead of the CE stage provides a number of performance improvements at the expense of gain reduction.
3. The low input resistance of the CB amplifier makes it useful only in specific applications. As we shall see in Chapter 9, it has a much better high-frequency response than the CE amplifier. This superiority will make it useful as a high-frequency amplifier, especially when combined with the CE circuit. We shall see one such combination in Chapter 7.
4. The emitter follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multistage amplifier, where its purpose is to equip the amplifier with a low output-resistance.

TABLE 6.5 Characteristics of BJT Amplifiers[a, b, c]

	R_{in}	A_{vo}	R_o	A_v	G_v
Common emitter (Fig. 6.50)	$(\beta+1)r_e$	$-g_m R_C$	R_C	$-g_m(R_C \parallel R_L)$ $-\alpha\dfrac{R_C \parallel R_L}{r_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{sig}+(\beta+1)r_e}$
Common emitter with R_e (Fig. 6.52)	$(\beta+1)(r_e+R_e)$	$-\dfrac{g_m R_C}{1+g_m R_e}$	R_C	$\dfrac{-g_m(R_C \parallel R_L)}{1+g_m R_e}$ $-\alpha\dfrac{R_C \parallel R_L}{r_e+R_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{sig}+(\beta+1)(r_e+R_e)}$
Common base (Fig. 6.53)	r_e	$g_m R_C$	R_C	$g_m(R_C \parallel R_L)$ $\alpha\dfrac{R_C \parallel R_L}{r_e}$	$\alpha\dfrac{R_C \parallel R_L}{R_{sig}+r_e}$
Emitter follower (Fig. 6.55)	$(\beta+1)(r_e+R_L)$	1	r_e	$\dfrac{R_L}{R_L+r_e}$	$\dfrac{R_L}{R_L+r_e+R_{sig}/(\beta+1)}$ $G_{vo}=1$ $R_{out}=r_e+\dfrac{R_{sig}}{\beta+1}$

[a] For the interpretation of R_{in}, A_{vo}, and R_o refer to Fig. 6.49.
[b] The BJT output resistance r_o has been neglected, which is permitted in the discrete-circuit amplifiers studied in this chapter. For integrated-circuit amplifiers (Chapter 7), r_o must always be taken into account.
[c] Setting $\beta=\infty$ ($\alpha=1$) and replacing r_e with $1/g_m$, R_C with R_D, and R_e with R_s results in the corresponding formulas for MOSFET amplifiers (Table 5.4).

6.7 Biasing in BJT Amplifier Circuits

Having studied the various configurations of BJT amplifiers, we now address the important question of biasing and its relationship to small-signal behavior. The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculable, predictable, and insensitive to variations in temperature and to the large variations in the value of β encountered among transistors of the same type. Another important consideration in bias design is locating the dc bias point in the i_C–v_{CE} plane to allow for maximum output signal swing (see the discussion in Section 6.4.6). In this section, we shall deal with various approaches to solving the bias problem in transistor circuits designed with discrete devices. Bias methods for integrated-circuit design are presented in Chapter 7.

Before presenting the "good" biasing schemes, we should point out why two obvious arrangements are *not* good. First, attempting to bias the BJT by fixing the voltage V_{BE} by, for instance, using a voltage divider across the power supply V_{CC}, as shown in Fig. 6.59(a), is not a viable approach: The very sharp exponential relationship i_C–v_{BE} means that any small and inevitable differences in V_{BE} from the desired value will result in large differences in I_C and in V_{CE}. Second, biasing the BJT by establishing a constant current in the base, as shown in Fig. 6.59(b), where $I_B \simeq ((V_{CC}-0.7)/R_B$, is also not a recommended approach. Here the typically large variations in the value of β among units of the same device type will result in correspondingly large variations in I_C and hence in V_{CE}.

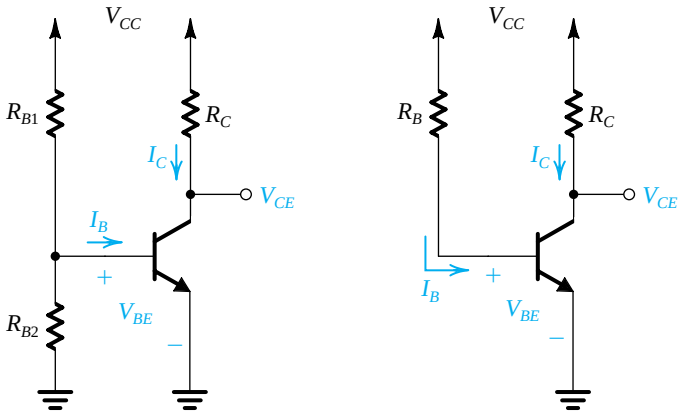


Figure 6.59 Two obvious schemes for biasing the BJT: **(a)** by fixing V_{BE}; **(b)** by fixing I_B. Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be "bad." Neither scheme is recommended.

6.7.1 The Classical Discrete-Circuit Bias Arrangement

Figure 6.60(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1, R_2. In addition, a resistor R_E is connected to the emitter.

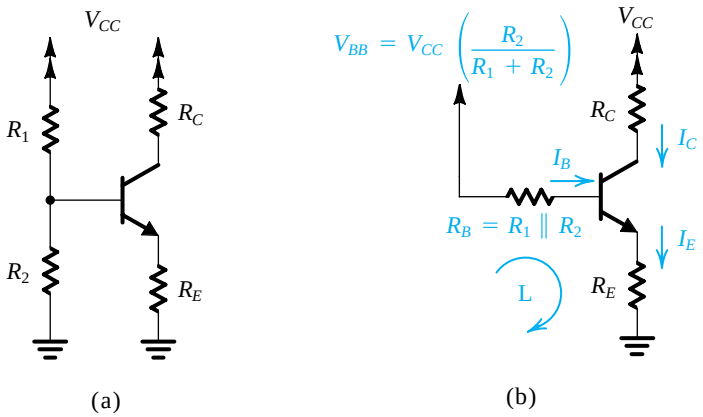


Figure 6.60 Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

Figure 6.60(b) shows the same circuit with the voltage divider network replaced by its Thévenin equivalent,

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{6.102}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{6.103}$$

The current I_E can be determined by writing a Kirchhoff loop equation for the base–emitter–ground loop, labeled L, and substituting $I_B = I_E/(\beta+1)$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta+1)} \tag{6.104}$$

To make I_E insensitive to temperature and β variation,[17] we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE} \tag{6.105}$$

$$R_E \gg \frac{R_B}{\beta+1} \tag{6.106}$$

Condition (6.105) ensures that small variations in V_{BE} ($\simeq 0.7$ V) will be swamped by the much larger V_{BB}. There is a limit, however, on how large V_{BB} can be: For a given value of the supply voltage V_{CC}, the higher the value we use for V_{BB}, the lower will be the sum of voltages across R_C and the collector–base junction (V_{CB}). On the other hand, we want the voltage across R_C to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want V_{CB} (or V_{CE}) to be large to provide a large signal swing (before transistor saturation). Thus, as is the case in any design, we have a set of conflicting requirements, and the solution must be a trade-off. As a rule of thumb, one designs for V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC}$, and $I_C R_C$ about $\frac{1}{3}V_{CC}$.

Condition (6.106) makes I_E insensitive to variations in β and could be satisfied by selecting R_B small. This in turn is achieved by using low values for R_1 and R_2. Lower values for R_1 and R_2, however, will mean a higher current drain from the power supply, and will result in a lowering of the input resistance of the amplifier (if the input signal is coupled to the base),[18] which is the trade-off involved in this part of the design. It should be noted that condition (6.106) means that we want to make the base voltage independent of the value of β and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$.

Further insight regarding the mechanism by which the bias arrangement of Fig. 6.60(a) stabilizes the dc emitter (and hence collector) current is obtained by considering the feedback action provided by R_E. Consider that for some reason the emitter current increases. The voltage drop across R_E, and hence V_E will increase correspondingly. Now, if the base voltage is determined primarily by the voltage divider R_1, R_2, which is the case if R_B is small, it will remain constant, and the increase in V_E will result in a corresponding decrease in V_{BE}. This in turn reduces the collector (and emitter) current, a change opposite to that originally assumed. Thus R_E provides a *negative feedback* action that stabilizes the bias current. This should remind the reader of the resistance R_e that we included in the emitter lead of the CE amplifier in Section 6.6.4. We shall study negative feedback formally in Chapter 10.

[17] Bias design seeks to stabilize either I_E or I_C since $I_C = \alpha I_E$ and α varies very little. That is, a stable I_E will result in an equally stable I_C, and vice versa.

[18] If the input signal is coupled to the transistor base, the two bias resistances R_1 and R_2 effectively appear in parallel between the base and ground. Thus, low values for R_1 and R_2 will result in lowering R_{in}.

Example 6.20

We wish to design the bias network of the amplifier in Fig. 6.60 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.

Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across R_2 and another one-third to the voltage drop across R_C, leaving one-third for possible negative signal swing at the collector. Thus,

$$V_B = +4 \text{ V}$$

$$V_E = 4 - V_{BE} \simeq 3.3 \text{ V}$$

and R_E is determined from

$$R_E = \frac{V_E}{I_E} = \frac{3.3}{1} = 3.3 \text{ k}\Omega$$

From the discussion above we select a voltage divider current of $0.1I_E = 0.1 \times 1 = 0.1$ mA. Neglecting the base current, we find

$$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

and

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

Thus $R_2 = 40$ kΩ and $R_1 = 80$ kΩ.

At this point, it is desirable to find a more accurate estimate for I_E, taking into account the nonzero base current. Using Eq. (6.104),

$$I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \dfrac{(80 \,\|\, 40)(\text{k}\Omega)}{101}} = 0.93 \text{ mA}$$

This is quite a bit lower than 1 mA, the value we are aiming for. It is easy to see from the above equation that a simple way to restore I_E to its nominal value would be to reduce R_E from 3.3 kΩ by the magnitude of the second term in the denominator (0.267 kΩ). Thus a more suitable value for R_E in this case would be $R_E = 3$ kΩ, which results in $I_E = 1.01$ mA $\simeq 1$ mA.[19]

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to I_E (i.e., 1 mA), resulting in $R_1 = 8$ kΩ and $R_2 = 4$ kΩ. We shall refer to the circuit using these latter values as design 2, for which the actual value of I_E using the initial value of R_E of 3.3 kΩ will be

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1 \text{ mA}$$

[19]Although reducing R_E restores I_E to the design value of 1 mA, it does not solve the problem of the dependence of the value of I_E on β. See Exercise 6.47.

Example 6.20 *continued*

In this case, design 2, we need not change the value of R_E.

Finally, the value of R_C can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99\ \text{mA} \simeq 1\ \text{mA}$ results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4\ \text{k}\Omega$$

EXERCISE

6.47 For design 1 in Example 6.20, calculate the expected range of I_E if the transistor used has β in the range of 50 to 150. Express the range of I_E as a percentage of the nominal value ($I_E \simeq 1$ mA) obtained for $\beta = 100$. Repeat for design 2.

Ans. For design 1: 0.94 mA to 1.04 mA, a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.

6.7.2 A Two-Power-Supply Version of the Classical Bias Arrangement

A somewhat simpler bias arrangement is possible if two power supplies are available, as shown in Fig. 6.61. Writing a loop equation for the loop labeled L gives

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{6.107}$$

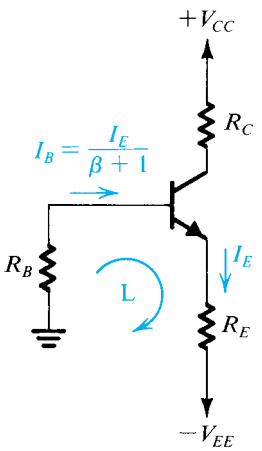


Figure 6.61 Biasing the BJT using two power supplies. Resistor R_B is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β-independence of the bias current.

This equation is identical to Eq. (6.104) except for V_{EE} replacing V_{BB}. Thus the two constraints of Eqs. (6.105) and (6.106) apply here as well. Note that if the transistor is to be used with the base grounded (i.e., in the common-base configuration), then R_B can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then R_B is needed. We shall study complete circuits of the various BJT amplifier configurations in Section 6.8.

EXERCISE

D6.48 The bias arrangement of Fig. 6.61 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a maximum signal swing at the collector of ±2 V. Use +10-V and −5-V power supplies.
Ans. $R_B = 0$; $R_E = 4.3\ \text{k}\Omega$; $R_C = 8.4\ \text{k}\Omega$

6.7.3 Biasing Using a Collector-to-Base Feedback Resistor

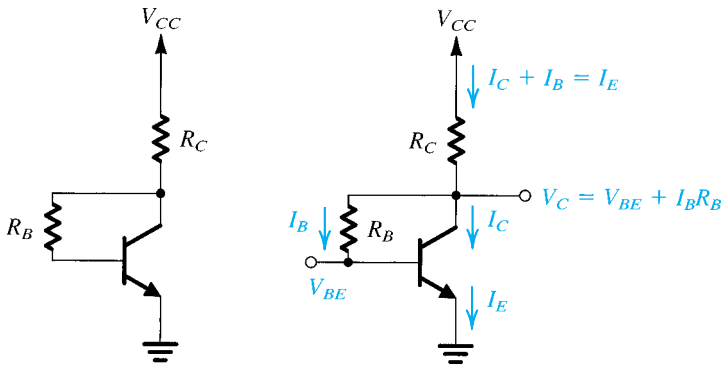
Figure 6.62(a) shows a simple but effective alternative biasing arrangement suitable for common-emitter amplifiers. The circuit employs a resistor R_B connected between the collector and the base. Resistor R_B provides negative feedback, which helps to stabilize the bias point of the BJT. We shall study feedback formally in Chapter 10.

Analysis of the circuit is shown in Fig. 6.62(b), from which we can write

$$\begin{aligned} V_{CC} &= I_E R_C + I_B R_B + V_{BE} \\ &= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE} \end{aligned}$$

Thus the emitter bias current is given by

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)} \tag{6.108}$$



(a) (b)

Figure 6.62 **(a)** A common-emitter transistor amplifier biased by a feedback resistor R_B. **(b)** Analysis of the circuit in **(a)**.

It is interesting to note that this equation is identical to Eq. (6.109), which governs the operation of the traditional bias circuit, except that V_{CC} replaces V_{BB} and R_C replaces R_E. It follows that to obtain a value of I_E that is insensitive to variation of β, we select $R_B/(\beta+1) \ll R_C$. Note, however, that the value of R_B determines the allowable negative signal swing at the collector since

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta+1} \tag{6.109}$$

EXERCISE

D6.49 Design the circuit of Fig. 6.62 to obtain a dc emitter current of 1 mA, maximum gain, and a ±2-V signal swing at the collector; that is, design for $V_{CE} = +2.3$ V. Let $V_{CC} = 10$ V and $\beta = 100$.
Ans. $R_B = 162$ kΩ; $R_C = 7.7$ kΩ. Note that if standard 5% resistor values are used (Appendix G) we select $R_B = 160$ kΩ and $R_C = 7.5$ kΩ. This results in $I_E = 1.02$ mA and $V_C = +2.3$ V.

6.7.4 Biasing Using a Constant-Current Source

The BJT can be biased using a constant-current source I as indicated in the circuit of Fig. 6.63(a). This circuit has the advantage that the emitter current is independent of the values of β and R_B. Thus R_B can be made large, enabling an increase in the input resistance at the base without adversely affecting bias stability. Further, current-source biasing leads to significant design simplification, as will become obvious in later sections and chapters.

A simple implementation of the constant-current source I is shown in Fig. 6.63(b). The circuit utilizes a pair of matched transistors Q_1 and Q_2, with Q_1 connected as a diode by shorting its collector to its base. If we assume that Q_1 and Q_2 have high β values, we can neglect their base currents. Thus the current through Q_1 will be approximately equal to I_{REF},

$$I_{REF} = \frac{V_{CC} - (-V_{EE}) - V_{BE}}{R} \tag{6.110}$$

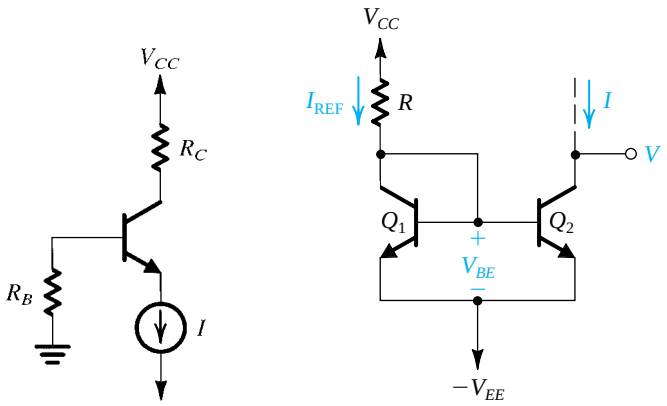


Figure 6.63 **(a)** A BJT biased using a constant-current source I. **(b)** Circuit for implementing the current source I.

Now, since Q_1 and Q_2 have the same V_{BE}, their collector currents will be equal, resulting in

$$I = I_{\text{REF}} = \frac{V_{CC} + V_{EE} - V_{BE}}{R} \tag{6.111}$$

Neglecting the Early effect in Q_2, the collector current will remain constant at the value given by this equation as long as Q_2 remains in the active region. This can be guaranteed by keeping the voltage at the collector, V, greater than that at the emitter ($-V_{EE}$) by at least 0.3V. The connection of Q_1 and Q_2 in Fig. 6.63(b) is known as a **current mirror**. We will study current mirrors in detail in Chapter 7.

EXERCISE

6.50 For the circuit in Fig. 6.63(a) with $V_{CC} = 10$ V, $I = 1$ mA, $\beta = 100$, $R_B = 100$ kΩ, and $R_C = 7.5$ kΩ, find the dc voltage at the base, the emitter, and the collector. For $V_{EE} = 10$ V, and neglecting base currents, find the required value of R in order for the circuit of Fig. 6.63(b) to implement the current source I.
Ans. −1 V; −1.7 V; +2.6 V; 19.3 kΩ

6.8 Discrete-Circuit BJT Amplifiers

With our study of BJT amplifier basics complete, we now put everything together by presenting practical circuits for discrete-circuit amplifiers. These circuits, which utilize the amplifier configurations studied in Section 6.6 and one of the biasing methods of Section 6.7, can be assembled using off-the-shelf discrete transistors, resistors, and capacitors. Though practical and carefully selected to illustrate some important points, the circuits presented in this section should be regarded as examples of discrete-circuit, bipolar-transistor amplifiers. Indeed, there is a great variety of such circuits, a number of which are explored in the end-of-chapter problems.

In this section we present a series of exercise problems, Exercises 6.51 to 6.55, which are carefully designed to illustrate important aspects of the amplifier circuits studied. These exercises are also intended to enable the reader to see more clearly the differences between the various circuit configurations. We strongly urge the reader to solve these exercises. As usual, the answers are provided.

6.8.1 The Basic Structure

Figure 6.64 shows the basic circuit that we shall utilize to implement the various configurations of discrete BJT amplifiers. Among the various biasing schemes possible for discrete BJT amplifiers (Section 6.7), we have selected, for simplicity and effectiveness, the one employing constant-current biasing. Figure 6.64 indicates the dc currents in all branches and the dc voltages at all nodes. We should note that one would want to select a large value for R_B in order to keep the input resistance at the base large. However, we also want to limit the dc voltage drop across R_B and even more importantly the variability of this dc voltage resulting from the variation in β values among transistors of the same type. The dc voltage V_B determines the allowable negative signal swing at the collector.

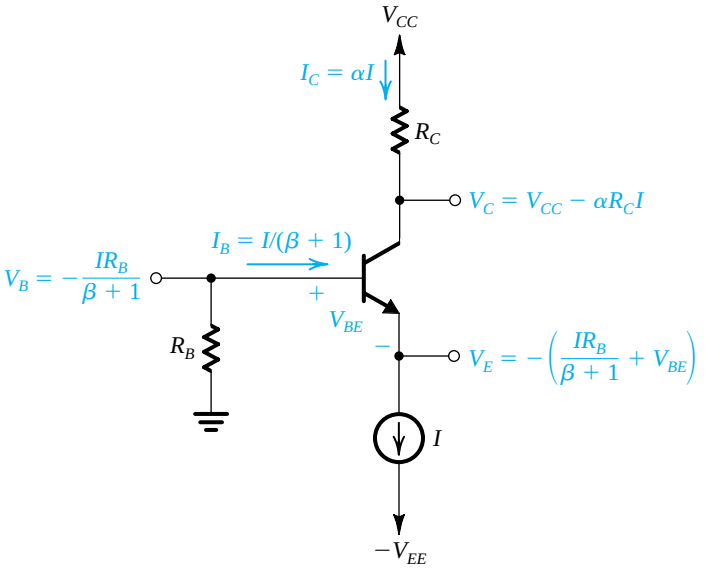


Figure 6.64 Basic structure of the circuit used to realize single-stage, discrete-circuit BJT amplifier configurations.

EXERCISE

6.51 Consider the circuit of Fig. 6.64 for the case $V_{CC} = V_{EE} = 10$ V, $I = 1$ mA, $R_B = 100$ kΩ, $R_C = 8$ kΩ, and $\beta = 100$. Find all dc currents and voltages. What are the allowable signal swings at the collector in both directions? How do these values change as β is changed to 50? To 200? Find the values of the BJT small-signal parameters at the bias point (with $\beta = 100$). The Early voltage $V_A = 100$ V.
Ans. See Fig. E6.51. Signal swing: for $\beta = 100$, +8 V, −3.4 V; for $\beta = 50$, +8 V, −4.4 V; for $\beta = 200$, +8 V, −2.9 V.

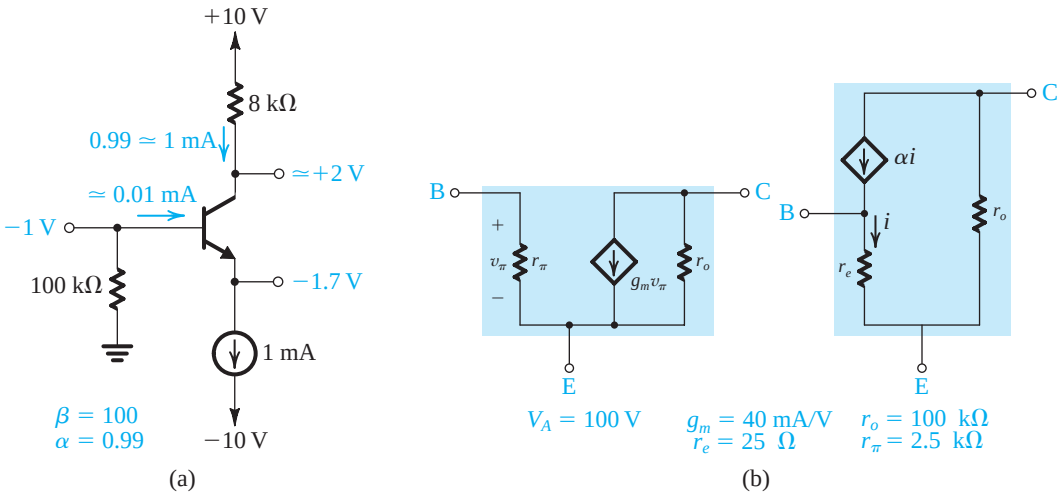
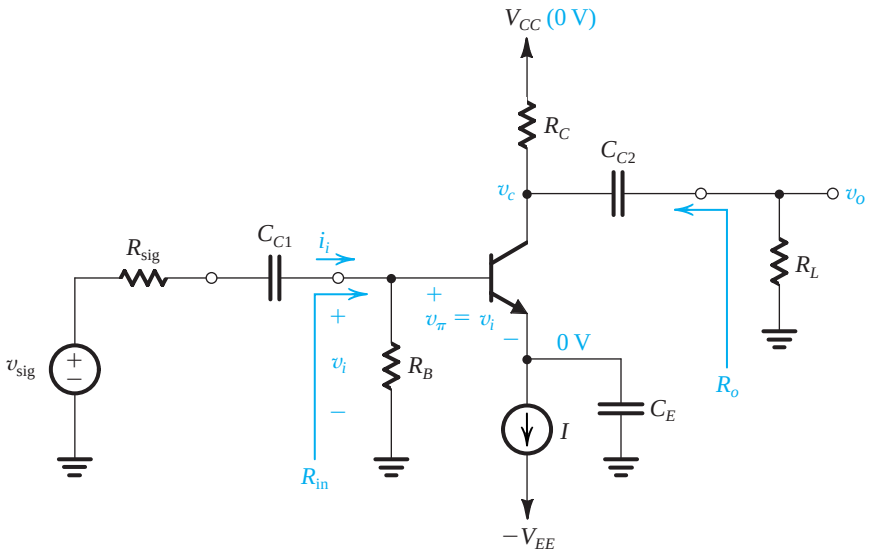


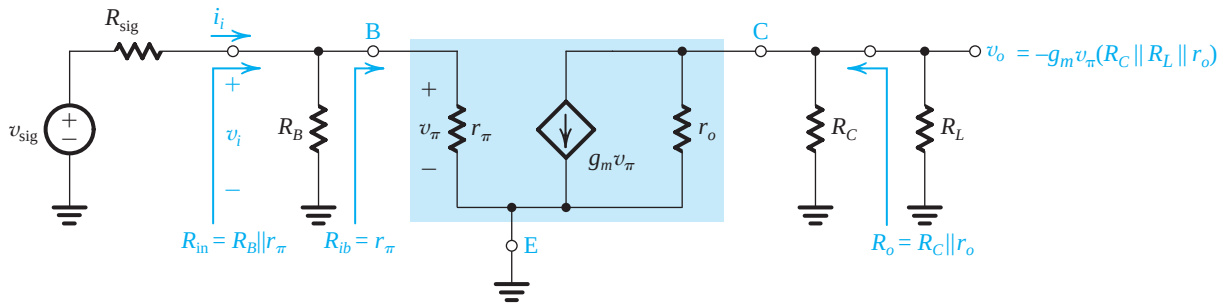
Figure E6.51

6.8.2 The Common-Emitter (CE) Amplifier

As mentioned in Section 6.6, the CE configuration is the most widely used of all BJT amplifier circuits. Figure 6.65(a) shows a CE amplifier implemented using the circuit of Fig. 6.64. To establish a **signal ground** (or an **ac ground**, as it is sometimes called) at the emitter, a large capacitor C_E, usually in the range of microfarads or tens of microfarads is connected between emitter and ground. This capacitor is required to provide a very low impedance to ground (ideally, zero impedance; i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the emitter signal current passes through C_E to ground and thus *bypasses* the output resistance of the current source I (and any other circuit component that might be connected to the emitter); hence C_E is called a **bypass capacitor**. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 9.1.2. For our purposes here we shall assume that C_E



(a)



(b)

Figure 6.65 **(a)** A common-emitter amplifier using the structure of Fig. 6.64. **(b)** Equivalent circuit obtained by replacing the transistor with its hybrid-π model.

is acting as a perfect short circuit and thus is establishing a zero signal voltage at the emitter.

In order not to disturb the dc bias currents and voltages, the signal to be amplified, shown as a voltage source v_{sig} with an internal resistance R_{sig}, is connected to the base through a large capacitor C_{C1}. Capacitor C_{C1}, known as a **coupling capacitor**, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again we shall assume this to be the case and defer discussion of imperfect signal coupling, arising as a result of the rise of the impedance of C_{C1} at low frequencies, to Section 9.1.2. At this juncture, we should point out that in situations where the signal source can provide a dc path for the dc base current I_B without significantly changing the bias point, we may connect the source directly to the base, thus dispensing with C_{C1} as well as R_B. Eliminating R_B has the added beneficial effect of raising the input resistance of the amplifier.

The voltage signal resulting at the collector, v_c, is coupled to the load resistance R_L via another coupling capacitor C_{C2}. We shall assume that C_{C2} also acts as a perfect short circuit at all signal frequencies of interest; thus the output voltage $v_o = v_c$. Note that R_L can be an actual load resistor to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of a subsequent amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 8.)

To determine the characteristic parameters of the CE amplifier, that is, its input resistance, voltage gain, and output resistance, we replace the BJT with its hybrid-π, small-signal model. The resulting small-signal equivalent circuit of the CE amplifier is shown in Fig. 6.65(b).

The equivalent circuit of Fig. 6.65(b) can be used to determine the amplifier characteristic parameters R_{in}, A_v, R_o, and G_v in exactly the same way we used for the "stripped-down" version of the CE amplifier in Section 6.6.3. We also show some of the analysis done directly on the circuit itself in Fig. 6.65(a).

Observe that the only difference between the circuit in Fig. 6.65(b) and the simplified version in Fig. 6.50(b) is the bias resistance R_B that appears across the amplifier input and thus changes R_{in} to

$$R_{in} = R_B \parallel r_\pi \tag{6.112}$$

If $R_B \gg r_\pi$ we can neglect its effect, and we are back to the simpler circuit of Fig. 6.50(b) and the formulas derived in Section 6.6.3. Those formulas, with r_o neglected, were presented in the CE entry in Table 6.4.

If R_B is not much greater than r_π, then it must be taken into account in the analysis. This is a simple task, and we urge the readers to just work their way through the circuit rather than relying on memorized formulas. As a check, however, there is a simple approach to adapt the CE formulas of Table 6.4 to the case at hand: Apply the Thévenin theorem to the network composed of v_{sig}, R_{sig}, and R_B, thus reducing it to a generator $v'_{sig} = (R_B/(R_B + R_{sig}))v_{sig}$ and a resistance $R'_{sig} = R_{sig} \parallel R_B$. Now the formulas in the CE entry in Table 6.4 can be changed as follows: Replace the expression for R_{in} by that in Eq. (6.112); multiply the expression for G_v by the factor $R_B/(R_B + R_{sig})$; and replace R_{sig} in that expression by $(R_{sig} \parallel R_B)$.

EXERCISE

6.52 Consider the CE amplifier of Fig. 6.65(a) when biased as in Exercise 6.51. In particular, refer to Fig. E6.51 for the bias currents and the values of the elements of the BJT model at the bias point. Evaluate R_{in} (without and with R_B taken into account), A_{vo} (without and with r_o taken into account), and R_o (without and with r_o taken into account). For $R_L = 5$ kΩ, find A_v. If $R_{sig} = 5$ kΩ, find the overall voltage gain G_v. If the sine-wave v_π is to be limited to 5 mV peak, what is the maximum allowed peak amplitude of v_{sig} and the corresponding peak amplitude of v_o?
Ans. 2.5 kΩ, 2.4 kΩ; –320 V/V, –296 V/V; 8 kΩ, 7.4 kΩ; –119 V/V; –39 V/V; 15 mV; 0.6 V

6.8.3 The Common-Emitter Amplifier with an Emitter Resistance

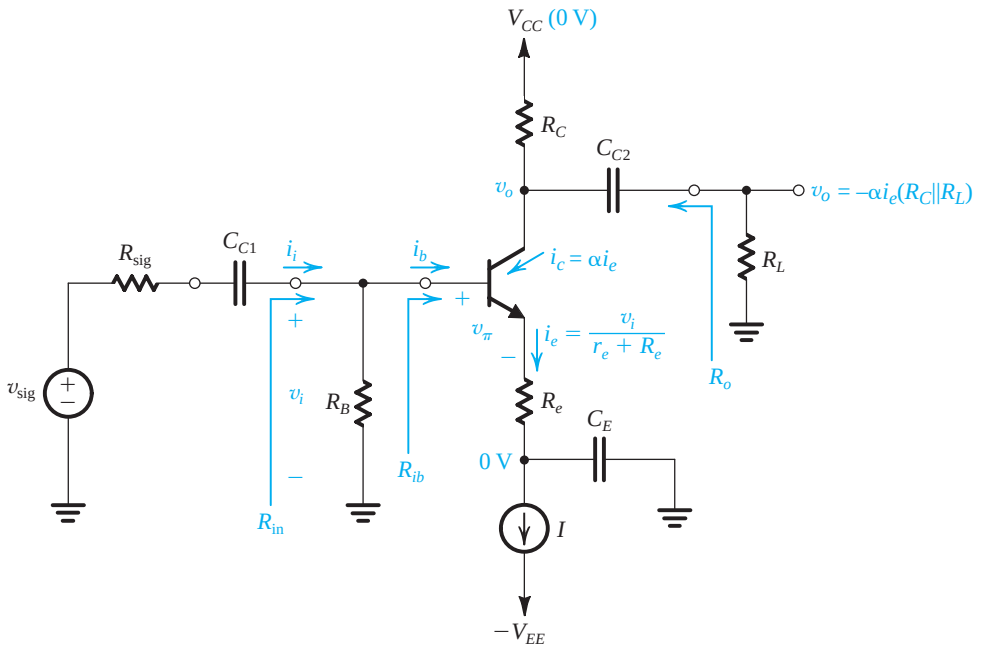
As demonstrated in Section 6.6.4, a number of beneficial results can be obtained by connecting a resistance R_e in the emitter of the transistor. This is shown in Fig. 6.66(a) where R_e is, of course, unbypassed. Figure 6.66(b) shows the small-signal, equivalent-circuit model. Observe that the only difference between this circuit and the simplified version studied in Section 6.6.4 is the inclusion of the bias resistance R_B, which unfortunately can limit the increase in R_{in} due to R_e, since

$$R_{in} = R_B \| [(\beta + 1)(r_e + R_e)] \tag{6.113}$$

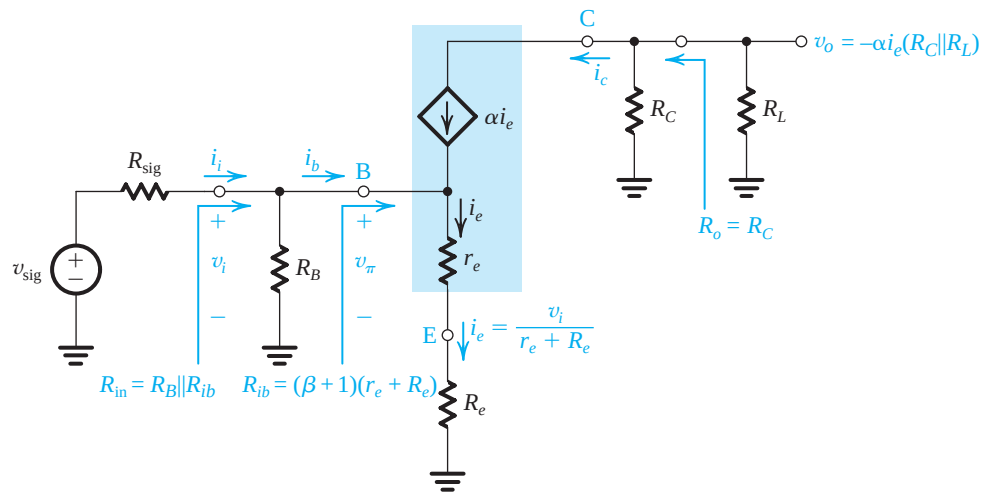
The analysis of the circuits in Fig. 6.66 is straightforward and is illustrated in the figure. The formulas given in Table 6.4 can be adapted to apply to the circuit here by replacing the formula for R_{in} with that in Eq. (6.113), replacing R_{sig} by $R'_{sig} = R_{sig} \| R_B$, and multiplying the expression for G_v by the factor $R_B/(R_B + R_{sig})$. Once again, we do not recommend this approach of plugging into formulas; rather, since each circuit the reader will encounter will be different, it is much more useful to work one's way through the circuit using the analysis methods studied as a guide.

EXERCISE

6.53 Consider the emitter-degenerated CE circuit of Fig. 6.66 when biased as in Exercise 6.51. In particular, refer to Fig. E6.51 for the bias currents and for the values of the elements of the BJT model at the bias point. Let the amplifier be fed from a source having $R_{sig} = 5$ kΩ, and let $R_L = 5$ kΩ. Find the value of R_e that results in R_{in} equal to four times the source resistance R_{sig}. For this value of R_e, find A_{vo}, R_o, A_v, and G_v. If v_π is to be limited to 5 mV, what is the maximum value v_{sig} can have with and without R_e included? Find the corresponding v_o.
Ans. 225 Ω; –32 V/V; 8 kΩ; –12.3 V/V; –9.8 V/V; 62.5 mV; 15 mV; 0.6 V



(a)



(b)

Figure 6.66 **(a)** A common-emitter amplifier with an emitter resistance R_e. **(b)** Equivalent circuit obtained by replacing the transistor with its T model.

6.8.4 The Common-Base (CB) Amplifier

Figure 6.67(a) shows a CB amplifier based on the circuit of Fig. 6.64. Observe that since both the dc and ac voltages at the base are zero, we have connected the base directly to ground, thus eliminating resistor R_B altogether. Coupling capacitors C_{C1} and C_{C2} perform similar functions to those in the CE circuit.

The small-signal, equivalent-circuit model of the amplifier is shown in Fig. 6.67(b). This circuit is identical to that in Fig. 6.53(b), which we analyzed in detail in Section 6.6.5. Thus the analysis of Section 6.6.5, and indeed the results summarized in the CB entry in Table 6.4, apply directly here.

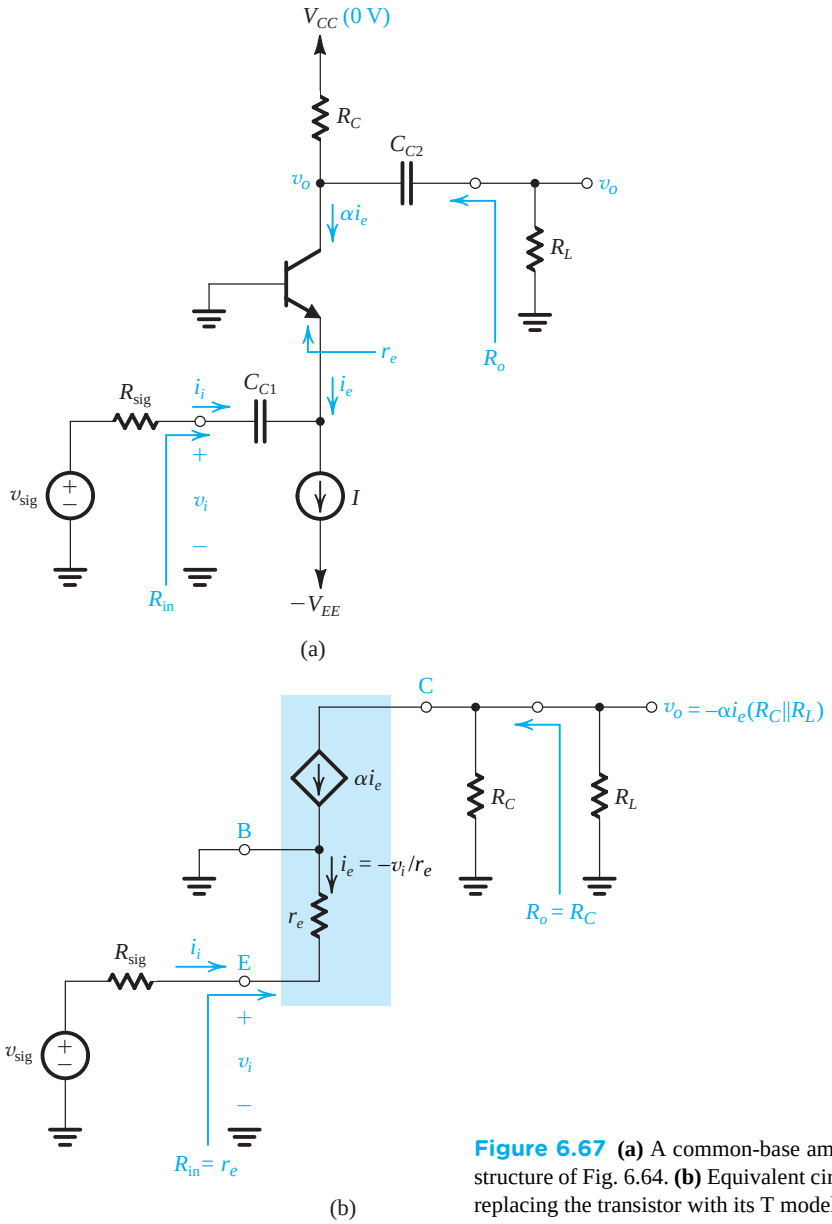


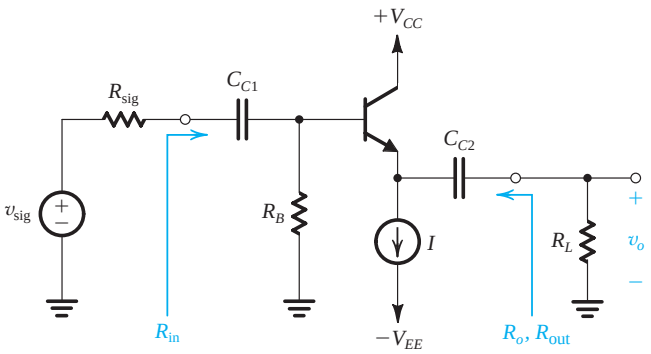
Figure 6.67 **(a)** A common-base amplifier using the structure of Fig. 6.64. **(b)** Equivalent circuit obtained by replacing the transistor with its T model.

EXERCISE

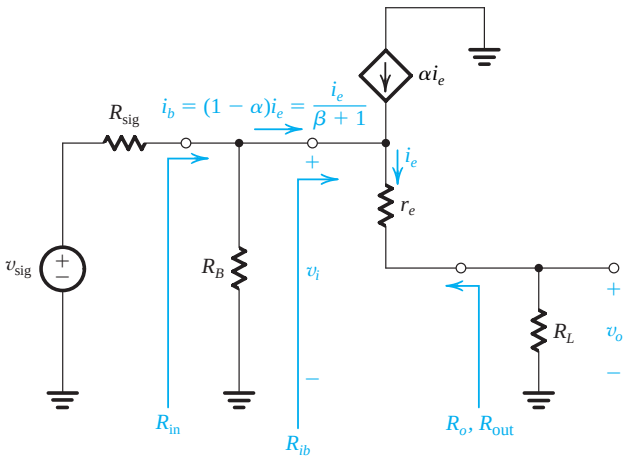
6.54 Consider the CB amplifier of Fig. 6.66(a) when designed using the BJT and component values specified in Exercise 6.51. Specifically, refer to Fig. E6.51 for the bias quantities and the values of the components of the BJT small-signal model. Let $R_{sig} = R_L = 5$ kΩ. Find the values of R_{in}, A_{vo}, R_o, A_v, v_i/v_{sig}, and G_v. To what value should R_{sig} be reduced (usually not possible to do!) to obtain an overall voltage gain equal to that found for the CE amplifier in Exercise 6.52, that is, –39 V/V?
Ans. 25 Ω; +320 V/V; 8 kΩ; +123 V/V; 0.005 V/V; 0.6 V/V; 54 Ω

6.8.5 The Emitter Follower

An emitter-follower circuit based on the structure of Fig. 6.64 is shown in Fig. 6.68(a). Observe that since the collector is to be at signal ground, we have eliminated the collector resistance R_C. The input signal is capacitively coupled to the base, and the output signal is capacitively coupled from the emitter to a load resistance R_L.



(a)



(b)

Figure 6.68 **(a)** An emitter-follower circuit based on the structure of Fig. 6.64. **(b)** Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model.

Replacing the BJT with its T model and neglecting r_o, we obtain the equivalent circuit shown in Fig. 6.68(b). This circuit is identical to that in the stripped-down case analyzed in Section 6.6.6 except here we have the bias resistance R_B. Note that it is very important to select as large a value for R_B as permitted by dc bias considerations, since a low R_B could defeat the purpose of the emitter follower. To appreciate this point recall that the most important feature of the emitter follower is that it multiplies R_L by $(\beta+1)$, thus presenting a high input resistance to the signal source. Here, however, R_B appears in parallel with this increased resistance, resulting in

$$R_{\text{in}} = R_B \| (\beta+1)(r_e + R_L) \tag{6.114}$$

Thus ideally, R_B should be much larger than $(\beta+1)\ (r_e + R_L)$.

Again we urge the reader to analyze the circuit being studied (here, Fig. 6.68) directly, without the need to refer back to memorized formulas. As a check, however, we note that the results presented in Table 6.4 in the emitter-follower entry apply to the circuit in Fig. 6.68(b) with the following adaptations: Replace the expression for R_{in} with that in Eq. (6.114); multiply the expression for G_v by the factor $R_B/(R_B + R_{\text{sig}})$; and replace R_{sig} in the expression for G_v by $(R_{\text{sig}} \| R_B)$. Also, the equivalent circuits in Fig. 6.56 can be adapted to the circuit in Fig. 6.68 by replacing v_{sig} by $(R_B/(R_B + R_{\text{sig}}))v_{\text{sig}}$ and R_{sig} by $(R_{\text{sig}} \| R_B)$. Finally, the Thévenin equivalent in Fig 6.57(a) can be made to apply to the circuit in Fig. 6.67 by using $G_{vo} = R_B/(R_B + R_{\text{sig}})$ and $R_{\text{out}} = r_e + (R_{\text{sig}} \| R_B)/(\beta+1)$.

EXERCISE

6.55 The emitter follower in Fig. 6.68(a) is used to connect a source with $R_{\text{sig}} = 10$ kΩ to a load $R_L = 1$ kΩ. The transistor is biased at $I = 5$ mA, utilizes a resistance $R_B = 40$ kΩ, and has $\beta = 100$. Find R_{ib}, R_{in}, G_v, G_{vo}, and R_{out}. If in order to limit nonlinear distortion, the base–emitter signal voltage is limited to 10 mV peak, what is the corresponding amplitude at the output? What will the overall voltage gain become if R_L is changed to 2 kΩ? To 500 Ω?

Ans. 101.5 kΩ; 28.7 kΩ; 0.738 V/V; 0.8 V/V; 84 Ω; 2 V; 0.768 V/V; 0.685 V/V.

6.8.6 The Amplifier Frequency Response

Thus far, we have assumed that the gain of BJT amplifiers is constant independent of the frequency of the input signal. This would imply that BJT amplifiers have infinite bandwidth, which of course is not true. To illustrate, we show in Fig. 6.69 a sketch of the magnitude of the gain of a common-emitter amplifier versus frequency. Observe that there is indeed a wide frequency range over which the gain remains almost constant. This obviously is the useful frequency range of operation for the particular amplifier. Thus far, we have been assuming that our amplifiers are operating in this frequency band, called **the midband**.

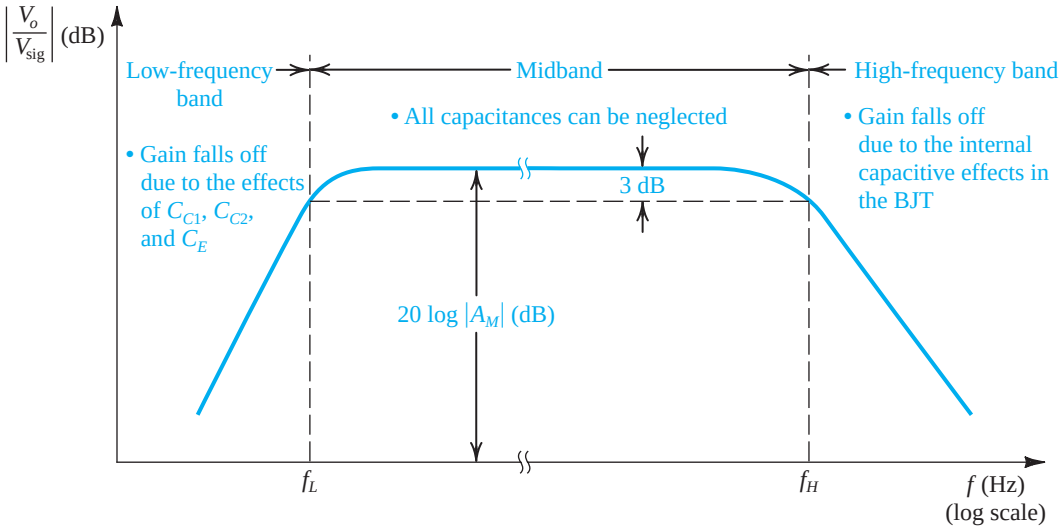


Figure 6.69 Sketch of the magnitude of the gain of a CE amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency-response determination.

Figure 6.69 indicates that at lower frequencies, the magnitude of amplifier gain falls off. This is because the coupling and bypass capacitors no longer have low impedances. Recall that we assumed that their impedances were small enough to act as short circuits. Although this can be true at midband frequencies, as the frequency of the input signal is lowered, the reactance $1/j\omega C$ of each of these capacitors becomes significant, and it can be shown that this results in the overall voltage gain of the amplifier decreasing.

Figure 6.69 indicates also that the gain of the amplifier falls off at the high-frequency end. This is due to the internal capacitive effects in the BJT. In Chapter 3 we briefly introduced such capacitive effects in our study of the *pn* junction. In Chapter 9 we shall study the internal capacitive effects of the BJT and will augment the hybrid-π model with capacitances that model these effects.

We will undertake a detailed study of the frequency response of BJT amplifiers in Chapter 9. For the time being, however, it is important for the reader to realize that for every BJT amplifier, there is a finite band over which the gain is almost constant. The boundaries of this useful frequency band or midband, are the two frequencies f_L and f_H at which the gain drops by a certain number of decibels (usually 3 dB) below its value at midband. As indicated in Fig. 6.69, the amplifier **bandwidth**, or 3-dB bandwidth, is defined as the difference between the lower (f_L) and upper or higher (f_H) 3-dB frequencies:

$$BW = f_H - f_L \tag{6.115}$$

and since usually $f_L \ll f_H$,

$$BW \simeq f_H \tag{6.116}$$

A figure-of-merit for the amplifier is its **gain–bandwidth product**, defined as

$$GB = |A_M| BW \tag{6.117}$$

where $|A_M|$ is the magnitude of the amplifier gain in the midband. It will be seen in Chapter 9 that in amplifier design it is usually possible to trade off gain for bandwidth. One way to accomplish this, for instance, is by including resistance R_e in the emitter of the CE amplifier.

6.9 Transistor Breakdown and Temperature Effects

We conclude this chapter with a brief discussion of two important nonideal effects in the BJT: voltage breakdown, and the dependence of β on I_C and temperature.

6.9.1 Transistor Breakdown

The maximum voltages that can be applied to a BJT are limited by the EBJ and CBJ breakdown effects that follow the avalanche multiplication mechanism described in Section 3.5.3. Consider first the common-base configuration. The i_C–v_{CB} characteristics in Fig. 6.70(b) indicate that for $i_E = 0$ (i.e., with the emitter open-circuited) the collector–base junction breaks down at a voltage denoted by BV_{CBO}. For $i_E > 0$, breakdown occurs at voltages smaller than BV_{CBO}. Typically, for discrete BJTs, BV_{CBO} is greater than 50 V.

Next consider the common-emitter characteristics of Fig. 6.71, which show breakdown occurring at a voltage BV_{CEO}. Here, although breakdown is still of the avalanche type, the effects on the characteristics are more complex than in the common-base configuration. We will not explain these in detail; it is sufficient to point out that typically BV_{CEO} is about half BV_{CBO}. On transistor data sheets, BV_{CEO} is sometimes referred to as the **sustaining voltage** LV_{CEO}.

Breakdown of the CBJ in either the common-base or common-emitter configuration is not destructive as long as the power dissipation in the device is kept within safe limits. This, however, is not the case with the breakdown of the emitter–base junction. The EBJ breaks down in an avalanche manner at a voltage BV_{EBO} much smaller than BV_{CBO}. Typically, BV_{EBO} is in the range of 6 V to 8 V, and the breakdown is destructive in the sense that the β of the transistor is permanently reduced. This does not prevent use of the EBJ as a zener diode to generate reference voltages in IC design. In such applications one is not concerned with the β-degradation effect. A circuit arrangement to prevent EBJ breakdown in IC amplifiers will be discussed in Chapter 12. Transistor breakdown and the maximum allowable power dissipation are important parameters in the design of power amplifiers (Chapter 11) .

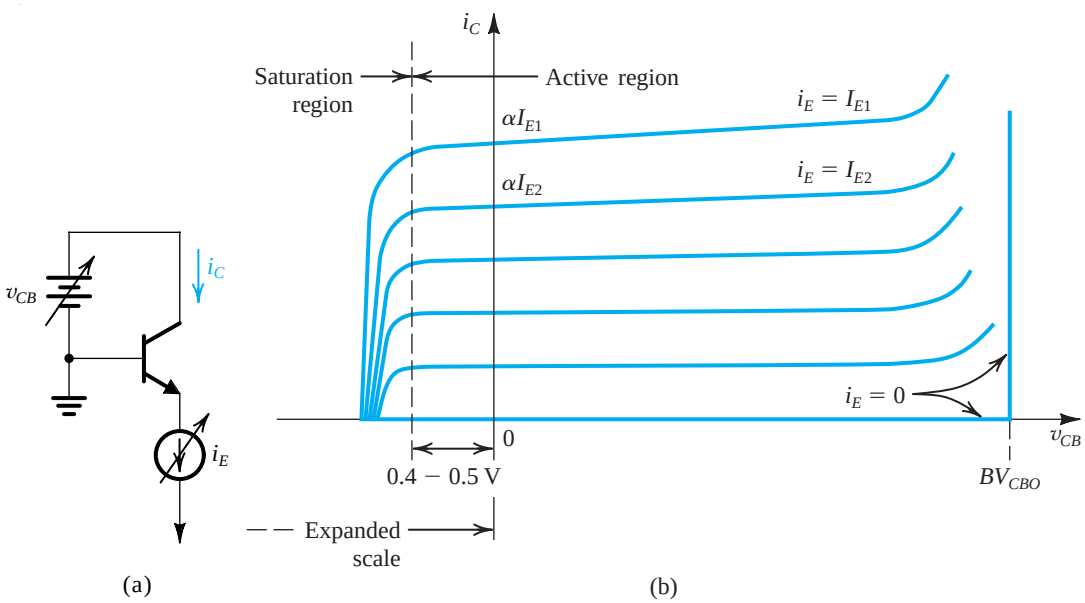


Figure 6.70 The BJT common-base characteristics including the transistor breakdown region.

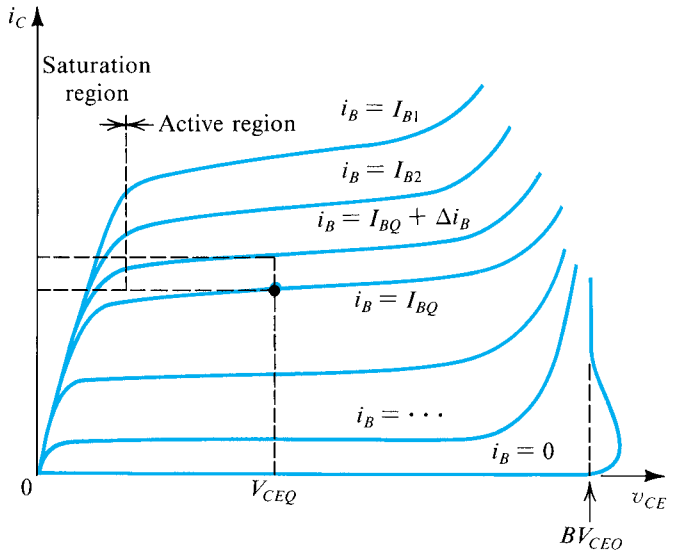


Figure 6.71 The BJT common-emitter characteristics including the breakdown region.

EXERCISE

6.56 What is the output voltage of the circuit in Fig. E6.56 if the transistor BV_{BCO} = 70 V?

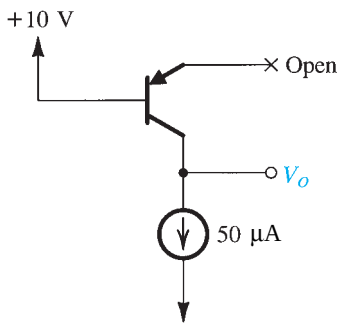


Figure E6.56

Ans. –60 V

6.9.2 Dependence of β on I_C and Temperature

Throughout this chapter we have assumed that the transistor common-emitter dc current gain, β or h_{FE}, is constant for a given transistor. In fact, β depends on the dc current at which the transistor is biased, as shown in Fig. 6.72. The physical processes that give rise to this dependence are beyond the scope of this book. Note, however, that there is a current range over which β is highest. Normally, one biases the transistor to operate at a current within this range.

Figure 6.72 also shows the dependence of β on temperature. The fact that β increases with temperature can lead to serious problems in transistors that operate at large power levels (see Chapter 11).

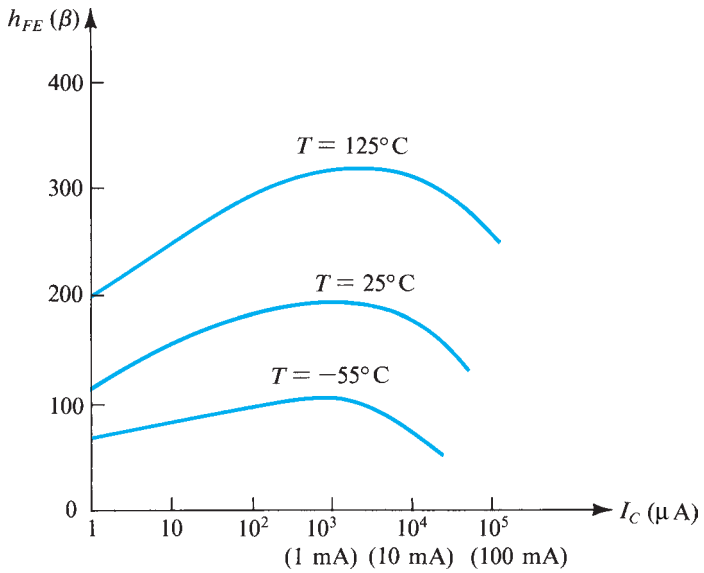


Figure 6.72 Typical dependence of β on I_C and on temperature in an integrated-circuit npn silicon transistor intended for operation around 1 mA.

Summary

- Depending on the bias conditions on its two junctions, the BJT can operate in one of three possible modes: cutoff (both junctions reverse biased), active (the EBJ forward biased and the CBJ reverse biased), and saturation (both junctions forward biased). Refer to Table 6.1.
- For amplifier applications, the BJT is operated in the active mode. Switching applications make use of the cutoff and saturation modes.
- A BJT operating in the active mode provides a collector current $i_C = I_S e^{|v_{BE}|/V_T}$. The base current $i_B = i_C/\beta$, and the emitter current $i_E = i_C + i_B$. Also, $i_C = \alpha i_E$, and thus $\beta = \alpha/(1-\alpha)$ and $\alpha = \beta/(\beta+1)$. See Table 6.2.
- To ensure operation in the active mode, the collector voltage of an *npn* transistor must be kept higher than approximately 0.4 V below the base voltage. For a *pnp* transistor the collector voltage must be lower than approximately 0.4 V above the base voltage. Otherwise, the CBJ becomes forward biased, and the transistor enters the saturation region.
- At a constant collector current, the magnitude of the base–emitter voltage decreases by about 2 mV for every 1°C rise in temperature.
- The BJT will be at the edge of saturation when $|v_{CE}|$ is reduced to about 0.3 V. In saturation, $|v_{CE}| \simeq 0.2$ V, and the ratio of i_C to i_B is lower than β (i.e., $\beta_{\text{forced}} < \beta$)
- In the active mode, i_C shows a slight dependence on v_{CE}. This phenomenon, known as the Early effect, is modeled by ascribing a finite (i.e., noninfinite) output resistance to the BJT: $r_o = |V_A|/I'_C$, where V_A is the Early voltage and I'_C is the dc collector current without the Early effect taken into account. In discrete circuits, r_o plays a minor role and can usually be neglected. This is *not* the case, however, in integrated-circuit design (Chapter 7).
- The dc analysis of transistor circuits is greatly simplified by assuming that $|V_{BE}| \simeq 0.7$ V. Refer to Table 6.3.
- To operate as a linear amplifier, the BJT is biased in the active region and the signal v_{be} is kept small ($v_{be} \ll V_T$).
- For small signals, the BJT functions as a linear voltage-controlled current source with a transconductance $g_m = I_C/V_T$. The input resistance between base and emitter, looking into the base, is $r_\pi = \beta/g_m$. The input resistence between base and emitter, looking into the emitter is $r_e \simeq 1/g_m$. Table 6.4 provides a summary of the small-signal models and the equations for determining their parameters.
- Bias design seeks to establish a dc collector current that is as independent of the value of β as possible.
- The three basic BJT amplifier configurations are shown in Fig. 6.48. A summary of their characteristic parameters is provided in Table 6.5.

- The CE amplifier is used to obtain the bulk of the required voltage gain in a cascade amplifier. It has a large voltage gain and a moderate input resistance but a relatively high output resistance and limited high-frequency response (Chapter 9).
- The input resistance of the common-emitter amplifier can be increased by including an unbypassed resistance in the emitter lead. This emitter-degeneration resistance provides other performance improvements at the expense of reduced voltage gain.
- The CB amplifier has a very low input resistance and is useful in a limited number of special applications. It does, however, have an excellent high-frequency response (Chapter 9) and thus can be combined with the CE amplifier to obtain an excellent amplifier circuit (Chapter 7).
- The emitter follower has a high input resistance and a low output resistance. Thus, it is useful as a buffer amplifier to connect a high-resistance signal source to a low-resistance load. Another important application of the emitter follower is as the last stage (called the output stage) of a cascade amplifier.
- A systematic procedure to analyze an amplifier circuit consists of replacing each BJT with one of its small-signal, equivalent circuit models. DC voltage sources are replaced by short circuits and dc current sources by open circuits. The analysis can then be performed on the resulting equivalent circuit. If a resistance is connected in series with the emitter lead of the BJT, the T model is the most convenient to use. Otherwise, the hybrid-π model is employed.
- The resistance reflection rule is a powerful tool in the analysis of BJT amplifier circuits: All resistances in the emitter circuit including the emitter resistance r_e can be reflected to the base side by multiplying them by $(\beta+1)$. Conversely, we can reflect all resistances in the base circuit to the emitter side by dividing them by $(\beta+1)$.
- Discrete-circuit BJT amplifiers utilize large coupling and bypass capacitors. Example circuits are given in Section 6.8. As will be seen in Chapter 7, this is not the case in IC amplifiers.

PROBLEMS

Computer Simulation Problems

SIM Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the disc. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption. * difficult problem; ** more difficult; *** very challenging and/or time-consuming; D: design problem.

Section 6.1: Device Structure and Physical operation

6.1 The terminal voltages of various *npn* transistors are measured during operation in their respective circuits with the following results:

Case	E	B	C	Mode
1	0	0.7	0.7	
2	0	0.8	0.1	
3	–0.7	0	0.7	
4	–0.7	0	–0.6	
5	–2.7	–2.0	0	
6	0	0	5.0	

In this table, where the entries are in volts, 0 indicates the reference terminal to which the black (negative) probe of the voltmeter is connected. For each case, identify the mode of operation of the transistor.

6.2 Two transistors, fabricated with the same technology but having different junction areas, when operated at a base-emitter voltage of 0.75 V, have collector currents of 0.2 mA and 5 mA. Find I_S for each device. What are the relative junction areas?

6.3 In a particular technology, a small BJT operating at $v_{BE} = 28V_T$ conducts a collector current of 100 μA. What is the corresponding saturation current? For a transistor in the same technology but with an emitter junction that is 32 times larger, what is the saturation current? What current will this transistor conduct at $v_{BE} = 28V_T$? What is the base–emitter voltage of the latter transistor at $i_C = 1$ mA? Assume active-mode operation in all cases.

6.4 Two transistors have EBJ areas as follows: $A_{E1} = A_{E1} = 400\ \mu m \times 400\ \mu m$ and $A_{E2} = 0.4\ \mu m \times 0.2\ \mu m$. If the two transistors are operated in the active mode and conduct equal collector currents, what do you expect the difference in their v_{BE} values to be?

6.5 Find the collector currents that you would expect for operation at $v_{BE} = 700$ mV for transistors for which

$I_S = 10^{-12}$ A and $I_S = 10^{-18}$ A. For the transistor with the larger EBJ, what is the v_{BE} required to provide a collector current equal to that provided by the smaller transistor at $v_{BE} = 700$ mV? Assume active-mode operation in all cases.

6.6 In this problem, we contrast two BJT integrated-circuit fabrication technologies: For the "old" technology, a typical *npn* transistor has $I_S = 5 \times 10^{-15}$ A, and for the "new" technology a typical *npn* transistor has $I_S = 5 \times 10^{-18}$ A. These typical devices have vastly different junction areas and base width. For our purpose here we wish to determine the v_{BE} required to establish a collector current of 1 mA in each of the two typical devices. Assume active-mode operation.

6.7 Consider an *npn* transistor whose base–emitter drop is 0.76 V at a collector current of 10 mA. What current will it conduct at $v_{BE} = 0.70$ V? What is its base–emitter voltage for $i_C = 10$ μA?

6.8 In a particular BJT, the base current is 10 μA, and the collector current is 600 μA. Find β and α for this device.

6.9 Find the values of β that correspond to α values of 0.5, 0.8, 0.9, 0.95, 0.99, 0.995, and 0.999.

6.10 Find the values of α that correspond to β values of 1, 2, 10, 20, 100, 200, 1000, and 2000.

***6.11** Show that for a transistor with α close to unity, if α changes by a small per-unit amount $(\Delta\alpha/\alpha)$, the corresponding per-unit change in β is given approximately by

$$\frac{\Delta\beta}{\beta} \simeq \beta\left(\frac{\Delta\alpha}{\alpha}\right)$$

6.12 An *npn* transistor of a type whose β is specified to range from 60 to 300 is connected in a circuit with emitter grounded, collector at +9 V, and a current of 20 μA injected into the base. Calculate the range of collector and emitter currents that can result. What is the maximum power dissipated in the transistor? (*Note:* Perhaps you can see why this is a bad way to establish the operating current in the collector of a BJT.)

6.13 A BJT is specified to have $I_S = 5 \times 10^{-15}$ A and β that falls in the range of 50 to 200. If the transistor is operated in the active mode with v_{BE} set to 0.650 V, find the expected range of i_C, i_B, and i_E.

6.14 Measurements made on a number of transistors operating in the active mode with $i_E = 1$ mA indicate base currents of 50 μA, 10 μA, and 25 μA. For each device, find i_C, β, and α.

6.15 Measurement of V_{BE} and two terminal currents taken on a number of *npn* transistors operating in the active mode are tabulated below. For each, calculate the missing current value as well as α, β, and I_S as indicated by the table.

Transistor	a	b	c	d	e
V_{BE} (mV)	690	690	580	780	820
I_C (mA)	1.000	1.000		10.10	
I_B (μA)	50		7	120	1050
I_E (mA)		1.070	0.137		75.00
α					
β					
I_S					

6.16 A particular BJT when operated in the active mode conducts a collector current of 10 mA and has $v_{BE} = 0.70$ V and $i_B = 100$ μA. Use these data to create specific transistor models of the form shown in Figs. 6.5(a) to (d).

6.17 Using the *npn* transistor model of Fig. 6.5(b), consider the case of a transistor for which the base is connected to ground, the collector is connected to a 10-V dc source through a 2-kΩ resistor, and a 3-mA current source is connected to the emitter with the polarity so that current is drawn out of the emitter terminal. If $\beta = 100$ and $I_S = 10^{-15}$ A, find the voltages at the emitter and the collector and calculate the base current.

D 6.18 Consider an *npn* transistor operated in the active mode and represented by the model of Fig. 6.5(d). Let the transistor be connected as indicated by the equivalent circuit shown in Fig. 6.6(b). It is required to calculate the values of R_B and R_C that will establish a collector current I_C of 1 mA and a collector-to-emitter voltage V_{CE} of 1 V. The BJT is specified to have $\beta = 125$ and $I_S = 5 \times 10^{-15}$ A.

6.19 An *npn* transistor has a CBJ with an area 150 times that of the EBJ. If $I_S = 5 \times 10^{-15}$ A, find the voltage drop across EBJ and across CBJ when each is forward biased and conducting a current of 1 mA. Also find the forward current each junction would conduct when forward biased with 0.5 V.

6.20 We wish to investigate the operation of the *npn* transistor in saturation using the model of Fig. 6.9. Let $I_S = 10^{-15}$ A, $v_{BE} = 0.7$ V, $\beta = 100$ and $I_{SC}/I_S = 100$. For each of three values of v_{CE} (namely, 0.4 V, 0.3 V, and 0.1 V), find v_{BC}, i_{BC}, i_B, i_C, and i_C/i_B. Also find v_{CE} that results in $i_C = 0$.

***6.21** Use Eqs. (6.14), (6.15), and (6.16) to show that an *npn* transistor operated in saturation exhibits a collector-to-emitter voltage, $V_{CE\text{sat}}$ given by

$$V_{CE\text{sat}} = V_T \ln\left[\left(\frac{I_{SC}}{I_S}\right)\frac{1+\beta_{\text{forced}}}{1-\beta_{\text{forced}}/\beta}\right]$$

Use this relationship to evaluate V_{CEsat} for β_{forced} = 50, 10, 5, and 1 for a transistor with $\beta = 100$ and with a CBJ area 100 times that of the EBJ.

6.22 Consider the *pnp* large-signal model of Fig. 6.11(b) applied to a transistor having $I_S = 10^{-13}$ A and $\beta = 40$. If the emitter is connected to ground, the base is connected to a current source that pulls 20 μA out of the base terminal, and the collector is connected to a negative supply of −10 V via a 10-kΩ resistor, find the collector voltage, the emitter current, and the base voltage.

6.23 A *pnp* transistor has $v_{EB} = 0.8$ V at a collector current of 1 A. What do you expect v_{EB} to become at $i_C = 10$ mA? At $i_C = 5$ A?

6.24 A *pnp* transistor modeled with the circuit in Fig. 6.11 (b) is connected with its base at ground, collector at –1.0 V, and a 10-mA current is injected into its emitter. If the transistor is said to have $\beta = 10$, what are its base and collector currents? In which direction do they flow? If $I_S = 10^{-15}$ A, what voltage results at the emitter? What does the collector current become if a transistor with $\beta = 1000$ is substituted? (*Note:* The fact that the collector current changes by less than 10% for a large change of β illustrates that this is a good way to establish a specific collector current.)

6.25 A *pnp* power transistor operates with an emitter-to-collector voltage of 5 V, an emitter current of 10 A, and V_{EB} = 0.85 V. For β = 15, what base current is required? What is I_S for this transistor? Compare the emitter–base junction area of this transistor with that of a small-signal transistor that conducts i_C = 1 mA with v_{EB} = 0.70 V. How much larger is it?

6.26 While Fig. 6.5 provides four possible large-signal equivalent circuits for the *npn* transistor, only two equivalent circuits for the *pnp* transistor are provided in Fig. 6.11. Supply the missing two.

6.27 By analogy to the *npn* case shown in Fig. 6.9, give the equivalent circuit of a *pnp* transistor in saturation.

Section 6.2: Current–Voltage Characteristics

6.28 For the circuits in Fig. P6.28, assume that the transistors have very large β. Some measurements have been made on these circuits, with the results indicated in the figure. Find the values of the other labeled voltages and currents.

6.29 Measurements on the circuits of Fig. P6.29 produce labeled voltages as indicated. Find the value of β for each transistor.

6.30 A very simple circuit for measuring β of an *npn* transistor is shown in Fig. P6.30. In a particular design, V_{CC} is provided by a 9-V battery; M is a current meter with a 50-μA full scale and relatively low resistance that you can neglect for our purposes here. Assuming that the transistor has V_{BE} = 0.7 V at I_E = 1 mA, what value of R would establish a resistor current of 1 mA? Now, to what value of β does a meter reading of full scale correspond? What is β if the meter reading is 1/5 of full scale? 1/10 of full scale?

6.31 Repeat Exercise 6.13 for the situation in which the power supplies are reduced to ±1.5 V.

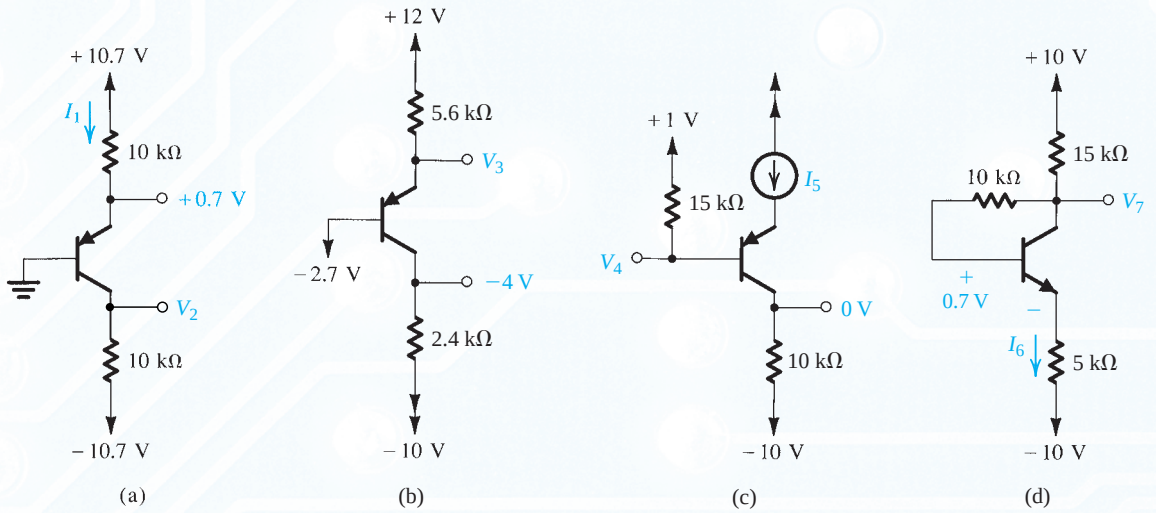


Figure P6.28

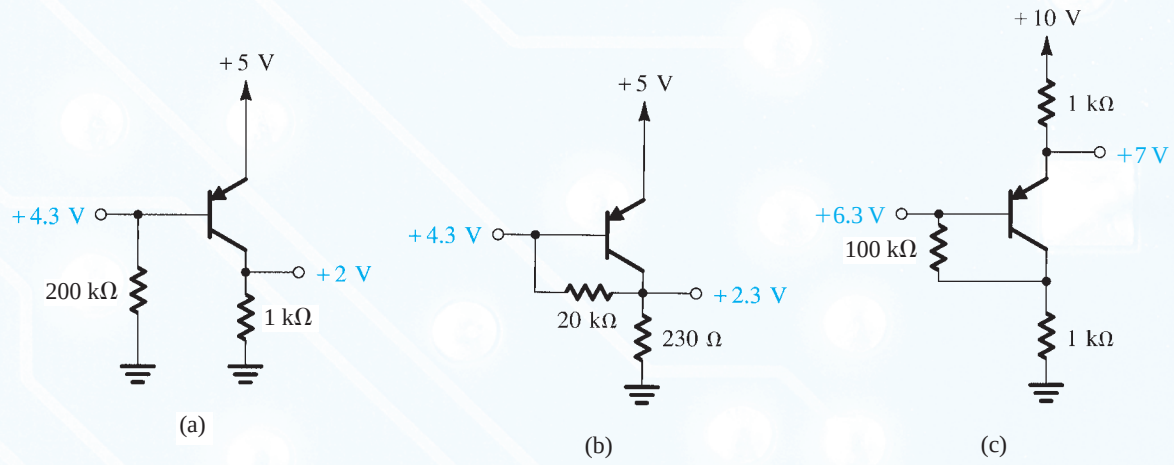


Figure P6.29

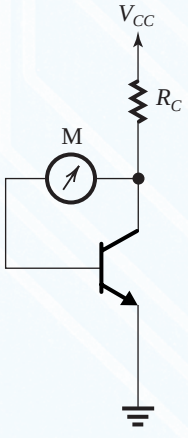


Figure P6.30

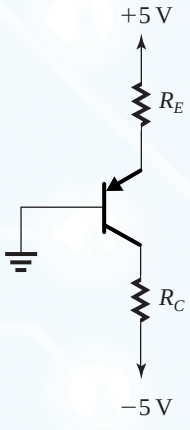


Figure P6.32

D 6.32 Design the circuit in Fig. P6.32 to establish a current of 1 mA in the emitter and a voltage of −1 V at the collector. The transistor $v_{EB} = 0.64$ V at $I_E = 0.1$ mA, and $\beta = 100$. To what value can R_C be increased while the collector current remains unchanged?

D 6.33 Examination of the table of standard values for resistors with 5% tolerance in Appendix G reveals that the closest values to those found in the design of Example 6.20 are 5.1 kΩ and 6.8 kΩ. For these values use approximate calculations (e.g., $V_{BE} \simeq 0.7$ V and $\alpha \simeq 1$) to determine the values of collector current and collector voltage that are likely to result.

D 6.34 Design the circuit in Fig. P6.34 to establish $I_C = 0.1$ mA and $V_C = 0.5$ V. The transistor exhibits v_{BE} of 0.8 V at $i_C = 1$ mA, and $\beta = 100$.

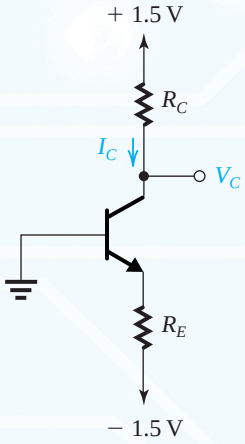


Figure P6.34

6.35 For each of the circuits shown in Fig. P6.35, find the emitter, base, and collector voltages and currents. Use $\beta = 50$, but assume $|V_{BE}| = 0.8$ V independent of current level.

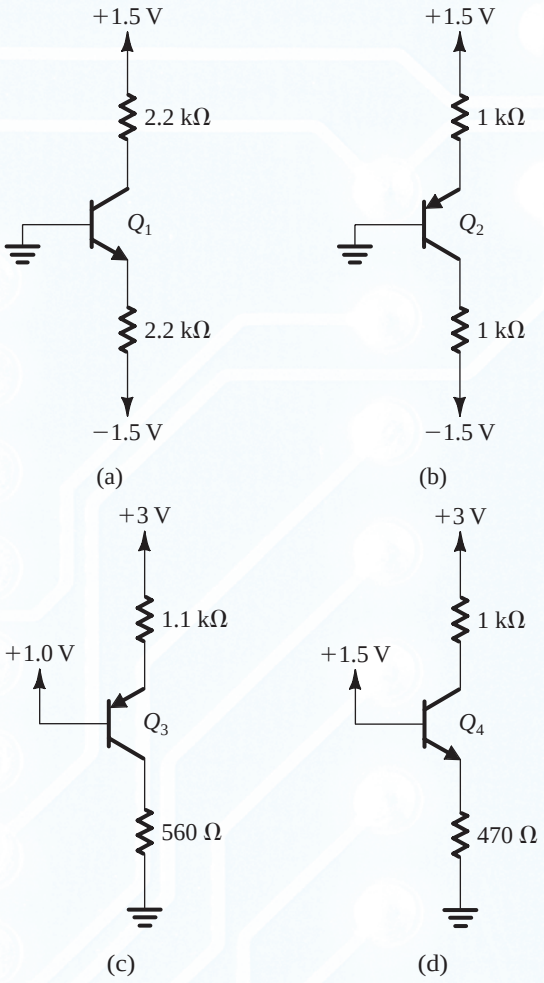


Figure P6.35

6.36 The current I_{CBO} of a small transistor is measured to be 10 nA at 25°C. If the temperature of the device is raised to 125°C, what do you expect I_{CBO} to become?

***6.37** Augment the model of the *npn* BJT shown in Fig. 6.18(a) by a current source representing I_{CBO}. Assume that r_o is very large and thus can be neglected. In terms of this addition, what do the terminal currents i_B, i_C, and i_E become? If the base lead is open-circuited while the emitter is connected to ground, and the collector is connected to a positive supply, find the emitter and collector currents.

6.38 A BJT whose emitter current is fixed at 1 mA has a base–emitter voltage of 0.69 V at 25°C. What base–emitter voltage would you expect at 0°C? At 100°C?

6.39 A particular *pnp* transistor operating at an emitter current of 0.5 mA at 20°C has an emitter–base voltage of 692 mV.

(a) What does v_{EB} become if the junction temperature rises to 50°C?

(b) If the transistor is operated at a fixed emitter–base voltage of 700 mV, what emitter current flows at 20°C? At 50°C?

6.40 Consider a transistor for which the base–emitter voltage drop is 0.7 V at 10 mA. What current flows for $v_{BE} = 0.5$ V? Evaluate the ratio of the slopes of the i_C–v_{BE} curve at $v_{BE} = 700$ mV and at $v_{BE} = 500$ mV. The large ratio confirms the point that the BJT has an "apparent threshold" at $v_{BE} \simeq 0.5$V .

6.41 In Problem 6.40, the stated voltages are measured at 25°C. What values correspond at –25°C? At 125°C?

6.42 Use Eq. (6.18) to plot i_C versus v_{CE} for an *npn* transistor having $I_S = 10^{-15}$ A and $V_A = 100$ V. Provide curves for $v_{BE} = 0.65$, 0.70, 0.72, 0.73, and 0.74 volts. Show the characteristics for v_{CE} up to 15 V.

***6.43** In the circuit shown in Fig. P6.43, current source I is 1.1 mA, and at 25° C $v_{BE} = 680$ mV at $i_C = 1$ mA. At 25° C with $\beta = 100$, what currents flow in R_1 and R_2? What voltage would you expect at node E? Noting that the temperature coefficient of v_{BE} for I_C constant is –2 mV/° C, what is the TC of v_E ? For an ambient temperature of 75° C, what voltage would you expect at node E? Clearly state any simplifying assumptions you make.

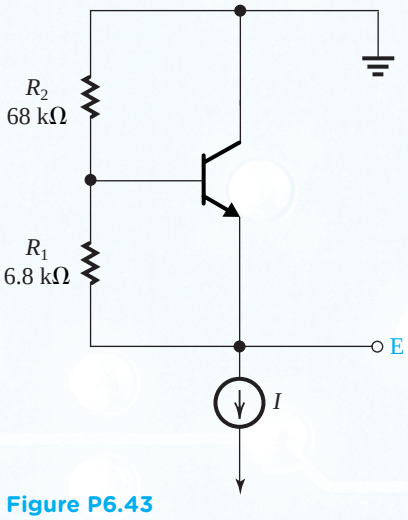


Figure P6.43

6.44 For a particular *npn* transistor operating at a v_{BE} of 670 mV and $I_C = 2$ mA, the i_C–v_{CE} characteristic has a slope of 2×10^{-5} ℧. To what value of output resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at 20 mA, what would the output resistance become?

6.45 For a BJT having an Early voltage of 150 V, what is its output resistance at 1 mA? At 100 μA?

6.46 Measurements of the i_C–v_{CE} characteristic of a small-signal transistor operating at $v_{BE} = 720$ mV show that $i_C = 1.8$ mA at $v_{CE} = 2$ V and that $i_C = 2.4$ mA at $v_{CE} = 14$ V. What is the corresponding value of i_C near saturation? At what value of v_{CE} is $i_C = 2.0$ mA? What is the value of the Early voltage for this transistor? What is the output resistance that corresponds to operation at $v_{BE} = 720$ mV?

6.47 Give the *pnp* equivalent circuit models that correspond to those shown in Fig. 6.18 for the *npn* case.

6.48 A BJT operating at $i_B = 8$ μA and $i_C = 1.2$ mA undergoes a reduction in base current of 0.8 μA. It is found that when v_{CE} is held constant, the corresponding reduction in collector current is 0.1 mA. What are the values of β and the incremental β or β_{ac} that apply? If the base current is increased from 8 μA to 10 μA and v_{CE} is increased from 8 V to 10 V, what collector current results? Assume $V_A = 100$ V.

6.49 For the circuit in Fig. P6.49 let $V_{CC} = 5$ V, $R_C = 1$ kΩ, and $R_B = 20$ kΩ. The BJT has $\beta = 50$. Find the value of V_{BB} that results in the transistor operating

(a) in the active mode with $V_C = 1$ V;
(b) at the edge of saturation;
(c) deep in saturation with $\beta_{\text{forced}} = 10$.

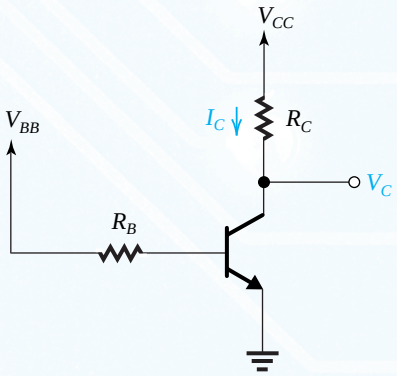


Figure P6.49

SIM **D** ***6.50** Consider the circuit of Fig. P6.49 for the case $V_{BB} = V_{CC}$. If the BJT is saturated, use the equivalent circuit of Fig. 6.20 to derive an expression for β_{forced} in terms of V_{CC} and (R_B/R_C). Also derive an expression for the total power dissipated in the circuit. For $V_{CC} = 5$ V, design the circuit to obtain operation at a forced β as close to 10 as possible while limiting the power dissipation to no larger than 20 mW. Use 1% resistors (see Appendix G).

6.51 The *pnp* transistor in the circuit in Fig. P6.51 has $\beta = 50$. Show that the BJT is operating in the saturation mode and find β_{forced} and V_C. To what value should R_B be increased in order for the transistor to operate at the edge of saturation?

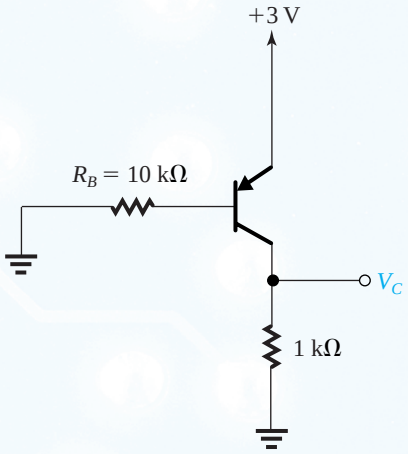


Figure P6.51

Section 6.3: BJT Circuits at DC

6.52 The transistor in the circuit of Fig. P6.52 has a very high β. Find V_E and V_C for V_B (a) +1.5 V, (b) +1 V, and (c) 0 V.

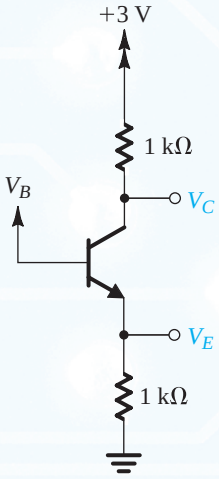


Figure P6.52

6.53 The transistor in the circuit of Fig. P6.52 has a very high β. Find the highest value of V_B for which the transistor still operates in the active mode. Also, find the value of V_B for which the transistor operates in saturation with a forced β of 1.

6.54 Consider the operation of the circuit shown in Fig. P6.54 for V_B at –1 V, 0 V, and +1 V. Assume that β is very high. What values of V_E and V_C result? At what value of V_B does the emitter current reduce to one-tenth of its value for $V_B = 0$ V? For what value of V_B is the transistor just at the edge of conduction? What values of V_E and V_C correspond?

For what value of V_B does the transistor reach the edge of saturation? What values of V_C and V_E correspond? Find the value of V_B for which the transistor operates in saturation with a forced β of 2.

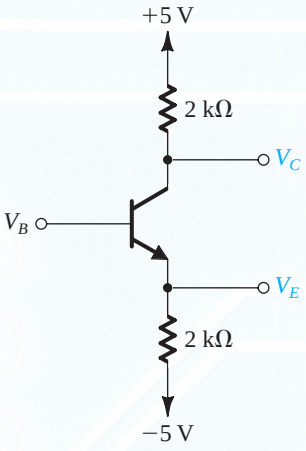


Figure P6.54

6.55 For the transistor shown in Fig. P6.55, assume $\alpha \simeq 1$ and $v_{BE} = 0.5$ V at the edge of conduction. What are the values of V_E and V_C for $V_B = 0$ V? For what value of V_B does the transistor cut off? Saturate? In each case, what values of V_E and V_C result?

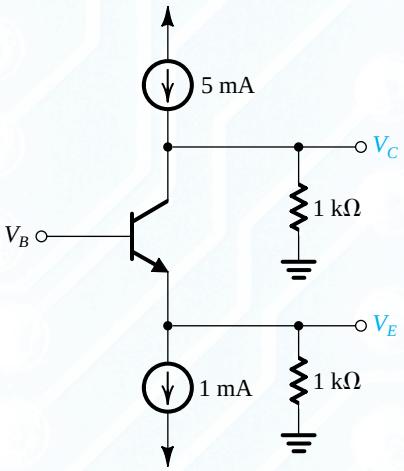


Figure P6.55

D 6.56 Consider the circuit in Fig. P6.52 with the base voltage V_B obtained using a voltage divider across the 3-V supply. Assuming the transistor β to be very large (i.e., ignoring the base current), design the voltage divider to obtain $V_B = 1.5$ V. Design for a 0.1-mA current in the voltage divider. Now, if the BJT $\beta = 100$, analyze the circuit to determine the collector current and the collector voltage.

6.57 A single measurement indicates the emitter voltage of the transistor in the circuit of Fig. P5.57 to be 1.2 V. Under the assumption that $|V_{BE}| = 0.7$ V, what are V_B, I_B, I_E, I_C, V_C, β, and α? (*Note:* Isn't it surprising what a little measurement can lead to?)

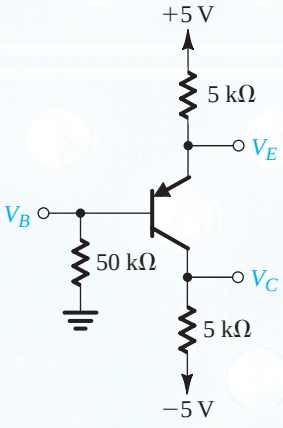


Figure P6.57

D 6.58 Design a circuit using a *pnp* transistor for which $\alpha \simeq 1$ using two resistors connected appropriately to ±5 V so that $I_E = 2$ mA and $V_{BC} = 2.5$ V. What exact values of R_E and R_C would be needed? Now, consult a table of standard 5% resistor values (e.g., that provided in Appendix G) to select suitable practical values. What values of resistors have you chosen? What are the values of I_E and V_{BC} that result?

6.59 In the circuit shown in Fig. P6.59, the transistor has $\beta = 50$. Find the values of V_B, V_E, and V_C. If R_B is raised to 100 kΩ, what voltages result? With R_B = 100 kΩ, what value of β would return the voltages to the values first calculated?

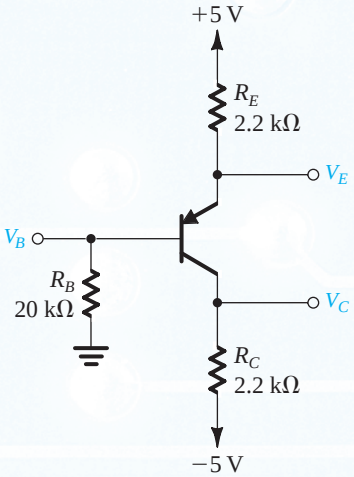


Figure P6.59

6.60 In the circuit shown in Fig. P6.59, the transistor has $\beta = 50$. Find the values of V_B, V_E, and V_C, and verify that the transistor is operating in the active mode. What is the largest value that R_C can have while the transistor remains in the active mode?

SIM 6.61 For the circuit in Fig. P6.61, find V_B, V_E, and V_C for $R_B = 100$ kΩ, 10 kΩ, and 1 kΩ. Let $\beta = 100$.

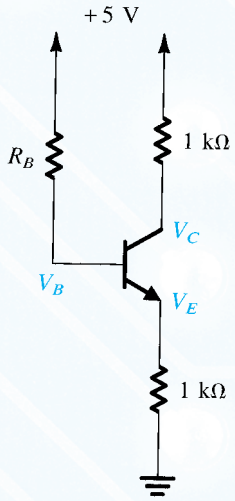


Figure P6.61

6.62 For the circuits in Fig. P6.62, find values for the labeled node voltages and branch currents. Assume β to be very high.

***6.63** Repeat the analysis of the circuits in Problem 6.62 using $\beta = 100$. Find all the labeled node voltages and branch currents.

D **6.64 It is required to design the circuit in Fig. P6.64 so that a current of 1 mA is established in the emitter and a voltage of −5 V appears at the collector. The transistor type used has a nominal β of 100. However, the β value can be as low as 50 and as high as 150. Your design should ensure that the specified emitter current is obtained when $\beta = 100$ and that at the extreme values of β the emitter current does not change by more than 10% of its nominal value. Also, design for as large a value for R_B as possible. Give the values of R_B, R_E, and R_C to the nearest kilohm. What is the expected range of collector current and collector voltage corresponding to the full range of β values?

D 6.65 The *pnp* transistor in the circuit of Fig. P6.65 has $\beta = 50$. Find the value for R_C to obtain $V_C = +3$ V. What happens if the transistor is replaced with another having $\beta = 100$?

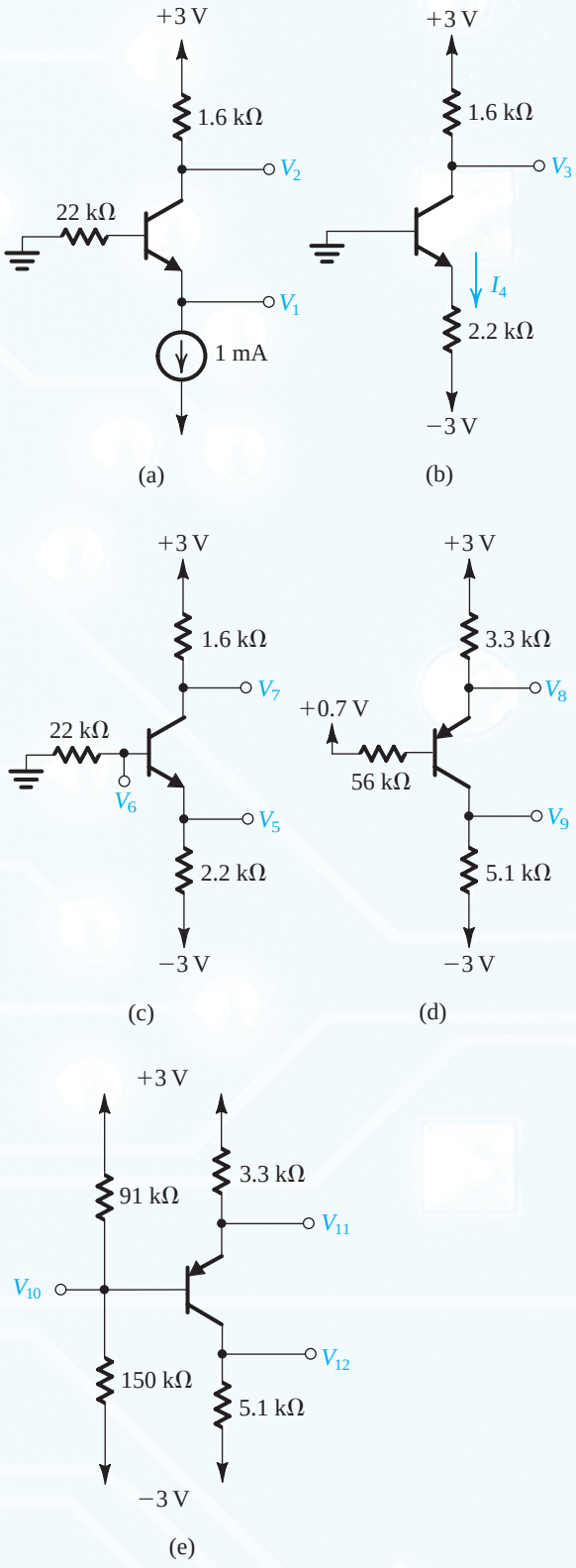


Figure P6.62

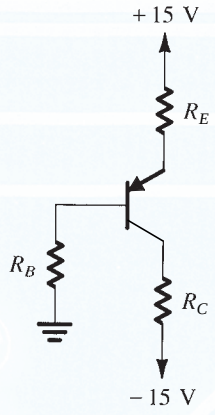


Figure P6.64

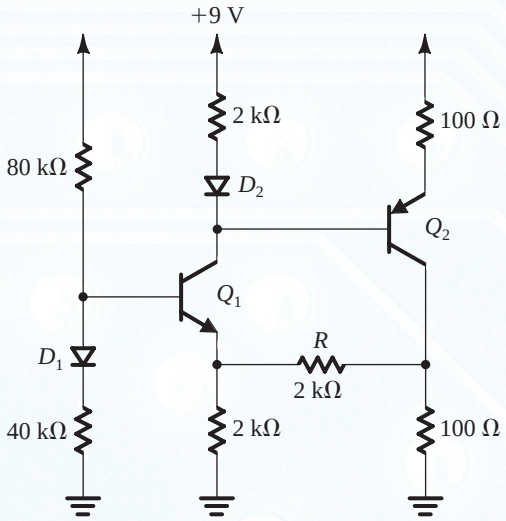


Figure P6.66

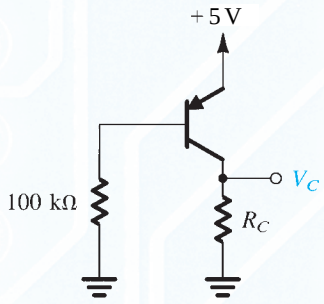


Figure P6.65

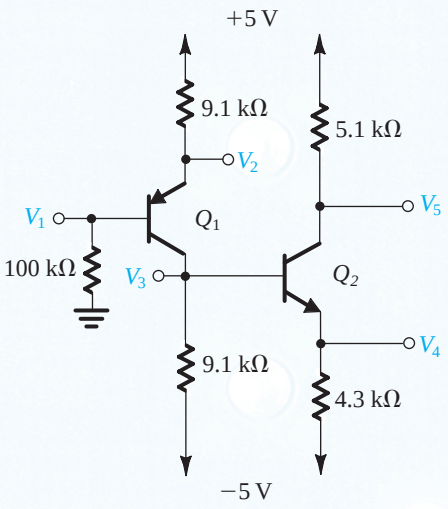


Figure P6.67

**6.66 Consider the circuit shown in Fig. P6.66. It resembles that in Fig. 6.29 but includes other features. First, note diodes D_1 and D_2 are included to make design (and analysis) easier and to provide temperature compensation for the emitter–base voltages of Q_1 and Q_2. Second, note resistor R whose purpose is to provide negative feedback (more on this later in the book!). Using $|V_{BE}|$ and $V_D = 0.7$ V independent of current and $\beta = \infty$, find the voltages V_{B1}, V_{E1}, V_{C1}, V_{B2}, V_{E2}, and V_{C2}, initially with R open-circuited and then with R connected. Repeat for $\beta = 100$, initially with R open-circuited then connected.

*6.67 For the circuit shown in Fig. P6.67, find the labeled node voltages for:

(a) $\beta = \infty$
(b) $\beta = 100$

D *6.68 Using $\beta = \infty$, design the circuit shown in Fig. P6.68 so that the bias currents in Q_1, Q_2, and Q_3 are 1 mA, 1 mA, and 2 mA, respectively, and $V_3 = 0$, $V_5 = -2$ V, and $V_7 = 1$ V. For each resistor, select the nearest standard value utilizing the table of standard values for 5% resistors in Appendix G. Now, for $\beta = 100$, find the values of V_3, V_4, V_5, V_6, and V_7.

*6.69 For the circuit in Fig. P6.69, find V_B and V_E for $v_I = 0$ V, +2 V, −2.5 V, and −5 V. The BJTs have $\beta = 100$.

**6.70 Find approximate values for the collector voltages in the circuits of Fig. P6.70. Also, calculate forced β for each of the transistors. (*Hint:* Initially, assume all transistors are operating in saturation, and verify the assumption.

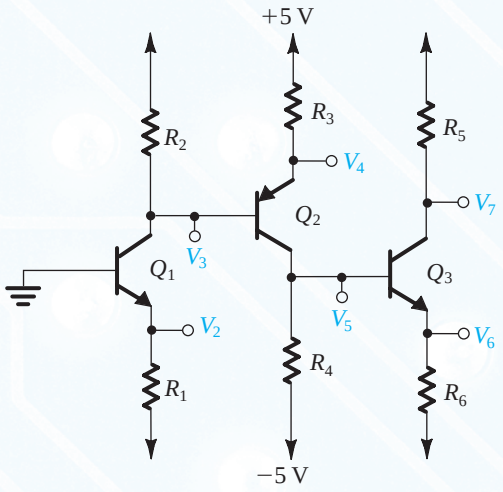


Figure P6.68

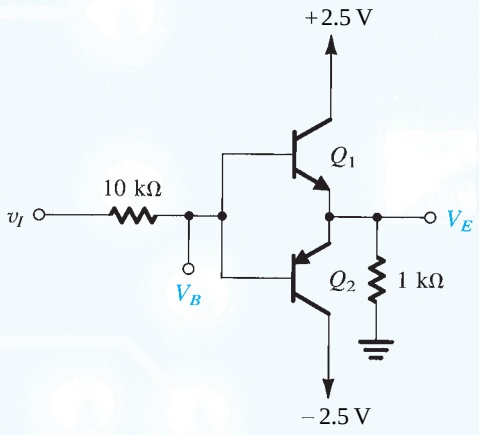


Figure P6.69

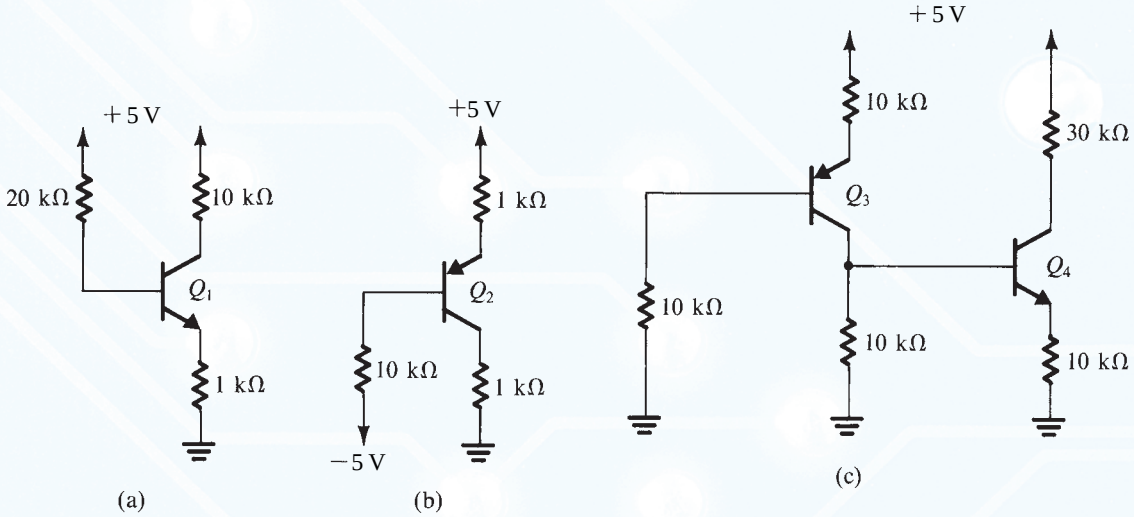


Figure P6.70

Section 6.4: Applying the BJT in Amplifier Design

6.71 A BJT amplifier circuit such as that in Fig. 6.33(a) is operated with V_{CC} = +5 V and is biased at V_{CE} = +1 V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

6.72 For the amplifier circuit in Fig. 6.33(a) with V_{CC} = +5 V and R_C = 1 kΩ, find V_{CE} and the voltage gain at the following dc collector bias currents: 0.5 mA, 1 mA, 2.5 mA, 4 mA, and 4.5 mA. For each, give the maximum possible positive- and negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

D 6.73 Consider the CE amplifier circuit of Fig. 6.33(a) when operated with a dc supply V_{CC} = +5 V. It is required to find the point at which the transistor should be biased; that is, find the value of V_{CE} so that the output sine-wave signal v_{ce} resulting from an input sine-wave signal v_{be} of 5-mV peak amplitude has the maximum possible magnitude. What is the

peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (*Hint:* To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without v_{CE} decreasing below 0.3 V.)

6.74 A designer considers a number of low-voltage BJT amplifier designs utilizing power supplies with voltage V_{CC} of 1.0, 1.5, 2.0, or 3.0 V. For transistors that saturate at $V_{CE} = 0.3$ V, what is the largest possible voltage gain achievable with each of these supply voltages? If in each case biasing is adjusted so that $V_{CE} = V_{CC}/2$, what gains are achieved? If a negative-going output signal swing of 0.4V is required, at what V_{CE} should the transistor be biased to obtain maximum gain? What is the gain achieved with each of the supply voltages? Notice that all of these gains are independent of the value of I_C chosen!)

D ***6.75** A BJT amplifier such as that in Fig. 6.33(a) is to be designed to support relatively undistorted sine-wave output signals of peak amplitudes P volt without the BJT entering saturation or cutoff and to have a voltage gain of A_v V/V. Show that the minimum supply voltage V_{CC} needed is given by

$$V_{CC} = V_{CEsat} + P + |A_v| V_T$$

Also, find V_{CC}, specified to the nearest 0.5 V, for the following situations:

(a) $A_v = -20$ V/V, $P = 0.2$ V

(b) $A_v = -50$ V/V, $P = 0.5$ V

(c) $A_v = -100$ V/V, $P = 0.5$ V

(d) $A_v = -100$ V/V, $P = 1.0$ V

(e) $A_v = -200$ V/V, $P = 1.0$ V

(f) $A_v = -500$ V/V, $P = 1.0$ V

(g) $A_v = -500$ V/V, $P = 2.0$ V

6.76 The transistor in the circuit of Fig. P6.76 is biased at a dc collector current of 0.4 mA. What is the voltage gain? (*Hint:* Use Thévenin's theorem to convert the circuit to the form in Fig. 6.33a).

6.77 Sketch and label the voltage transfer characteristics of the *pnp* common-emitter amplifiers shown in Fig. P6.77.

***6.78** In deriving the expression for small-signal voltage gain A_v in Eq. (6.31) we neglected the Early effect.

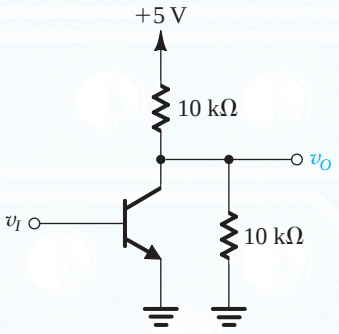


Figure P6.76

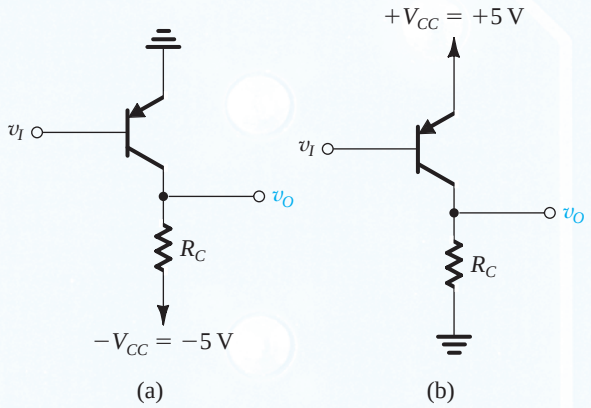


Figure P6.77

Derive this expression including the Early effect, by substituting

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

in Eq. (6.24) and including the factor $(1 + v_{CE}/V_A)$ in Eq. (6.28). Show that the gain expression changes to

$$A_v = \frac{-I_C R_C/V_T}{\left[1 + \dfrac{I_C R_C}{V_A + V_{CE}}\right]} = -\frac{(V_{CC} - V_{CE})/V_T}{\left[1 + \dfrac{V_{CC} - V_{CE}}{V_A + V_{CE}}\right]}$$

For the case $V_{CC} = 5$ V and $V_{CE} = 2.5$ V, what is the gain without and with the Early effect taken into account? Let $V_A = 100$ V.

6.79 When the amplifier circuit of Fig. 6.33(a) is biased with a certain V_{BE}, the dc voltage at the collector is found to be +2 V. For $V_{CC} = +5$ V and $R_C = 1$ kΩ, find I_C and the small-signal voltage gain. For a change $\Delta v_{BE} = +5$ mV, calculate the resulting Δv_O. Calculate it two ways: by finding

Δi_C using the transistor exponential characteristic, and approximately using the small-signal voltage gain. Repeat for $\Delta v_{BE} = -5$ mV. Summarize your results in a table.

***6.80** Consider the amplifier circuit of Fig. 6.33(a) when operated with a supply voltage $V_{CC} = +3$V.

(a) What is the theoretical maximum voltage gain that this amplifier can provide?
(b) What value of V_{CE} must this amplifier be biased at to provide a voltage gain of –80 V/V?
(c) If the dc collector current I_C at the bias point in (b) is to be 0.5 mA, what value of R_C should be used?
(d) What is the value of V_{BE} required to provide the bias point mentioned above? Assume that the BJT has $I_S = 10^{-15}$ A.
(e) If a sine-wave signal v_{be} having a 5-mV peak amplitude is superimposed on V_{BE}, find the corresponding output voltage signal v_{ce} that will be superimposed on V_{CE} assuming linear operation around the bias point.
(f) Characterize the signal current i_c that will be superimposed on the dc bias current I_C.
(g) What is the value of the dc base current I_B at the bias point? Assume $\beta = 100$. Characterize the signal current i_b that will be superimposed on the base current I_B.
(h) Dividing the amplitude of v_{be} by the amplitude of i_b, evaluate the incremental (or small-signal) input resistance of the amplifier.
(i) Sketch and clearly label correlated graphs for v_{BE}, v_{CE}, i_C, and i_B. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

6.81 The essence of transistor operation is that a change in v_{BE}, Δv_{BE}, produces a change in i_C, Δi_C. By keeping Δv_{BE} small, Δi_C is approximately linearly related to Δv_{BE}, $\Delta i_C = g_m \Delta v_{BE}$, where g_m is known as the transistor transconductance. By passing Δi_C through R_C, an output voltage signal Δv_O is obtained. Use the expression for the small-signal voltage gain in Eq. (6.30) to derive an expression for g_m. Find the value of g_m for a transistor biased at $I_C = 1$ mA.

6.82 The purpose of this problem is to illustrate the application of graphical analysis to the circuit shown in Fig. P6.82. Sketch i_C–v_{CE} characteristic curves for the BJT for $i_B = 1$ μA, 10 μA, 20 μA, and 40 μA. Assume the lines to be horizontal (i.e., neglect the Early effect), and let $\beta = 100$. For $V_{CC} = 5$ V and $R_C = 1$ kΩ, sketch the load line. What peak-to-peak collector voltage swing will result for i_B varying over the range 10 μA to 40 μA? If the BJT is biased at $V_{CE} = \frac{1}{2} V_{CC}$, find the value of I_C and I_B. If at this current $V_{BE} = 0.7$ V and if $R_B = 100$ kΩ, find the required value of V_{BB}.

***6.83** Sketch the i_C–v_{CE} characteristics of an *npn* transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves

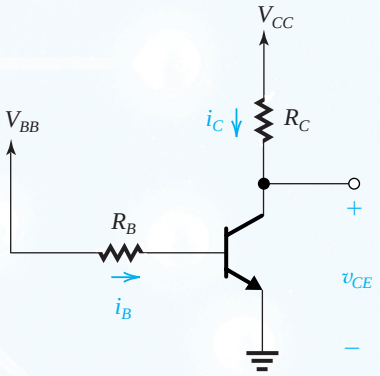


Figure P6.82

for $i_B = 20$ μA, 50 μA, 80 μA, and 100 μA. For the purpose of this sketch, assume that $i_C = \beta i_B$ at $v_{CE} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_C = 1$ kΩ. If the dc bias current into the base is 50 μA, write the equation for the corresponding i_C–v_{CE} curve. Also, write the equation for the load line, and solve the two equations to obtain V_{CE} and I_C. If the input signal causes a sinusoidal signal of 30-μA peak amplitude to be superimposed on I_B, find the corresponding signal components of i_C and v_{CE}.

***6.84** Consider the operation of the circuit shown in Fig. P6.84 as v_B rises slowly from zero. For this transistor, assume $\beta = 50$, v_{BE} at which the transistor conducts is 0.5 V, v_{BE} when fully conducting is 0.7 V, saturation begins at $v_{BC} = 0.4$ V, and the transistor is deeply in saturation at $v_{BC} = 0.6$V. Sketch and label v_E and v_C versus v_B. For what range of v_B is i_C essentially zero? What are the values of v_E, i_E, i_C, and v_C for $v_B = 1$ V and 3 V? For what value of v_B does saturation begin? What is i_B at this point? For $v_B = 4$ V and 6 V, what are the values of v_E, v_C, i_E, i_C, and i_B? Augment your sketch by adding a plot of i_B.

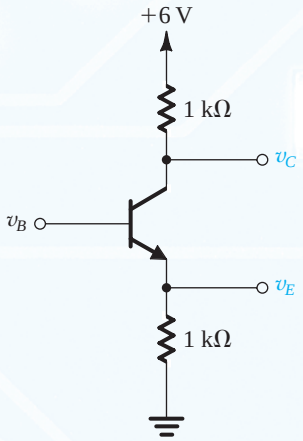


Figure P6.84

Section 6.5: Small-Signal Operation and Models

6.85 Consider a transistor biased to operate in the active mode at a dc collector current I_C. Calculate the collector signal current as a fraction of I_C (i.e., i_c/I_C) for input signals v_{be} of +1 mV, −1 mV, +2 mV, −2 mV, +5 mV, −5 mV, +8 mV, −8 mV, +10 mV, −10 mV, +12 mV, and −12 mV. In each case do the calculation two ways:

(a) using the exponential characteristic, and
(b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

6.86 An *npn* BJT with grounded emitter is operated with $V_{BE} = 0.700$ V, at which the collector current is 0.5 mA. A 10-kΩ resistor connects the collector to a +10-V supply. What is the resulting collector voltage V_C? Now, if a signal applied to the base raises v_{BE} to 705 mV, find the resulting total collector current i_C and total collector voltage v_C using the exponential i_C–v_{BE} relationship. For this situation, what are v_{be} and v_c? Calculate the voltage gain v_c/v_{be}. Compare with the value obtained using the small-signal approximation, that is, $-g_m R_C$.

6.87 A transistor with $\beta = 120$ is biased to operate at a dc collector current of 0.6 mA. Find the values of g_m, r_π, and r_e. Repeat for a bias current of 60 μA.

6.88 A *pnp* BJT is biased to operate at $I_C = 1.0$ mA. What is the associated value of g_m? If $\beta = 100$, what is the value of the small-signal resistance seen looking into the emitter (r_e)? Into the base (r_π)? If the collector is connected to a 5-kΩ load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

D 6.89 A designer wishes to create a BJT amplifier with a g_m of 25 mA/V and a base input resistance of 3000 Ω or more. What emitter-bias current should he choose? What is the minimum β he can tolerate for the transistor used?

6.90 A transistor operating with nominal g_m of 50 mA/V has a β that ranges from 50 to 150. Also, the bias circuit, being less than ideal, allows a ±20% variation in I_C. What are the extreme values found of the resistance looking into the base?

6.91 In the circuit of Fig. 6.36, V_{BE} is adjusted so that $V_C = 1$ V. If $V_{CC} = 3$ V, $R_C = 2$ kΩ, and a signal $v_{be} = 0.005 \sin \omega t$ volts is applied, find expressions for the total instantaneous quantities $i_C(t)$, $v_C(t)$, and $i_B(t)$. The transistor has $\beta = 80$. What is the voltage gain?

D *6.92 We wish to design the amplifier circuit of Fig. 6.36 under the constraint that V_{CC} is fixed. Let the input signal $v_{be} = \hat{V}_{be} \sin \omega t$, where $\hat{V}_{be}$ is the maximum value for acceptable linearity. For the design that results in the largest signal at the collector, without the BJT leaving the active region, show that

$$R_C I_C = (V_{CC} - 0.3 - \hat{V}_{be}) \Big/ \left(1 + \frac{\hat{V}_{be}}{V_T}\right)$$

and find an expression for the voltage gain obtained. For $V_{CC} = 3$ V and $\hat{V}_{be} = 5$ mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

6.93 The table below summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifiers under various conditions. Provide the missing entries. (*Note:* Isn't it remarkable how much two parameters can reveal?)

6.94 A BJT is biased to operate in the active mode at a dc collector current of 0.5 mA. It has a β of 100. Give the four small-signal models (Figs. 6.40 and 6.41) of the BJT complete with the values of their parameters.

6.95 The transistor amplifier in Fig. P6.95 is biased with a current source I and has a very high β. Find the dc voltage at the collector, V_C. Also, find the value of g_m. Replace the transistor with the simplified hybrid-π model of Fig. 6.40(a)

Transistor	a	b	c	d	e	f	g
α	1.000					0.90	
β		100		∞			
I_C (mA)	1.00		1.00				
I_E (mA)		1.00				5	
I_B (mA)			0.020				1.10
g_m (mA/V)							700
r_e (Ω)				25	100		
r_π (Ω)					10.1 kΩ		

(note that the dc current source I should be replaced with an open circuit). Hence find the voltage gain v_c/v_i.

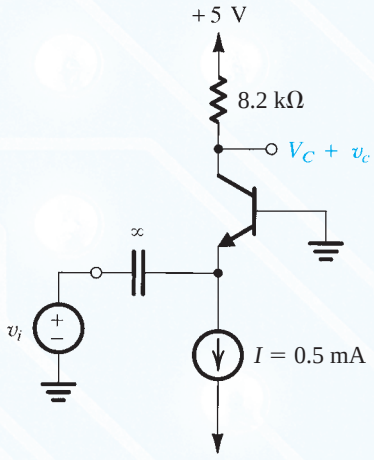


Figure P6.95

6.96 For the conceptual circuit shown in Fig. 6.39, $R_C = 3\ \text{k}\Omega$, $g_m = 50$ mA/V, and $\beta = 100$. If a peak-to-peak output voltage of 1 V is measured at the collector, what are the peak-to-peak values of v_{be} and i_b?

6.97 Figure P6.97 shows the circuit of an amplifier fed with a signal source v_{sig} with a source resistance R_{sig}. The bias circuitry is not shown. Replace the BJT with its hybrid-π equivalent circuit of Fig. 6.40(a). Find the input resistance $R_{\text{in}} \equiv v_\pi/i_b$, the voltage transmission from source to amplifier input, v_π/v_{sig}, and the voltage gain from base to collector, v_o/v_π. Use these to show that the overall voltage gain v_o/v_{sig} is given by

$$\frac{v_o}{v_{\text{sig}}} = -\frac{\beta R_C}{r_\pi + R_{\text{sig}}}$$

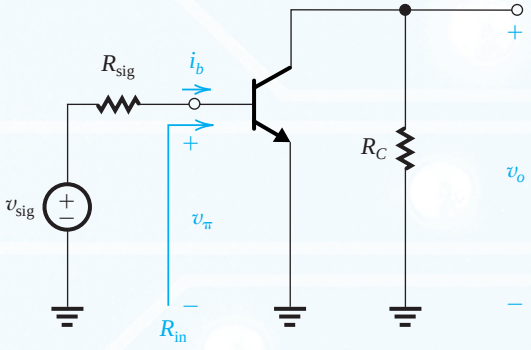


Figure P6.97

6.98 Figure P6.98 shows a transistor with the collector connected to the base. The bias arrangement is not shown. Since a zero v_{BC} implies operation in the active mode, the BJT can be replaced by one of the small-signal models of Figs. 6.40 and 6.41. Use the model of Fig. 6.41(b) and show that the resulting two-terminal device, known as a diode connected transistor, has a small-signal resistance r equal to r_e.

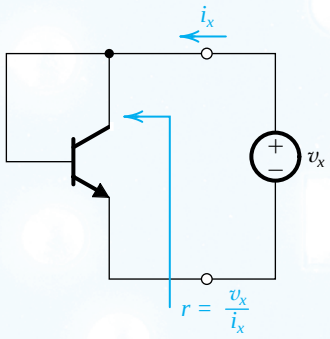


Figure P6.98

6.99 Figure P6.99 shows a particular configuration of BJT amplifiers, known as "emitter follower." The bias arrangement is not shown. Replace the BJT with its T equivalent-circuit model of Fig. 6.41(b). Show that

$$R_{\text{in}} \equiv \frac{v_i}{i_b} = (\beta + 1)(r_e + R_e)$$

$$\frac{v_o}{v_i} = \frac{R_e}{R_e + r_e}$$

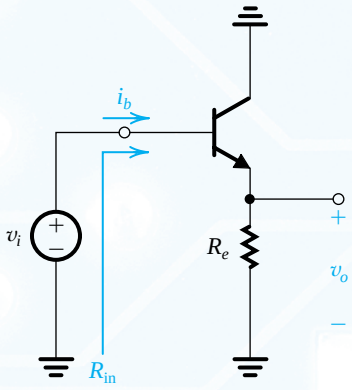


Figure P6.99

6.100 For the circuit shown in Fig. P6.100, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (use $\alpha = 0.99$). Your circuit should show the values of all components, including the model parameters. What is the input resistance R_{in}? Calculate the overall voltage gain (v_o/v_{sig}).

6.101 In the circuit shown in Fig. P6.101, the transistor has a β of 200. What is the dc voltage at the collector? Find the input resistances R_{ib} and R_{in} and the overall voltage gain

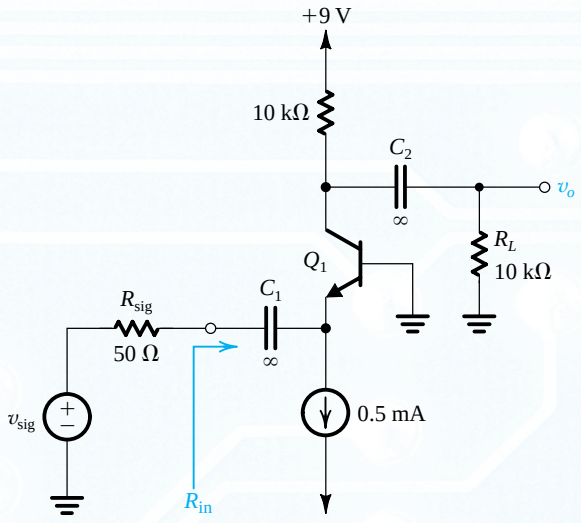


Figure P6.100

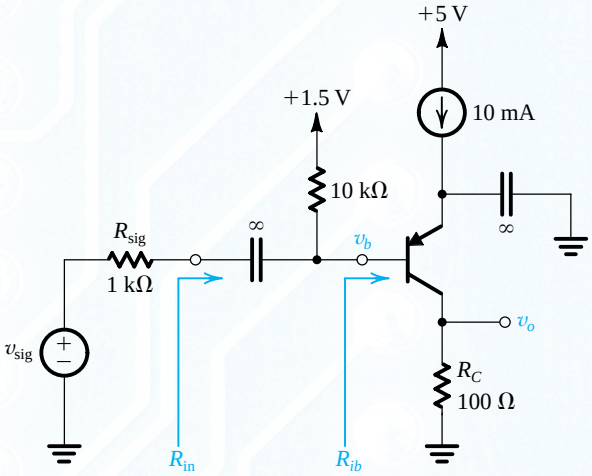


Figure P6.101

(v_o/v_{sig}). For an output signal of ±0.4 V, what values of v_{sig} and v_b are required?

6.102 Consider the augmented hybrid-π model shown in Fig. 6.47(a). Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for $V_A = 25$ V and $V_A = 250$ V.

6.103 Reconsider the amplifier shown in Fig. 6.42 and analyzed in Example 6.14 under the condition that β is not well controlled. For what value of β does the circuit begin to saturate? We can conclude that large β is dangerous in this circuit. Now, consider the effect of reduced β, say, to $\beta = 25$. What values of r_e, g_m, and r_π result? What is the overall voltage gain? (*Note:* You can see that this circuit, using base-current control of bias, is very β-sensitive and usually *not recommended*.)

6.104 Reconsider the circuit shown in Fig. 6.44(a) under the condition that the signal source has an internal resistance of 100 Ω. What does the overall voltage gain become? What is the largest input signal voltage that can be used without output-signal clipping?

D 6.105 Redesign the circuit of Fig. 6.44 by raising the resistor values by a factor n to increase the resistance seen by the input v_i to 75 Ω. What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be "matched" to the equivalent resistances of the interconnecting cables.

D **6.106 Design an amplifier using the configuration of Fig. 6.44(a). The power supplies available are ±5 V. The input signal source has a resistance of 50 Ω, and it is required that the amplifier input resistance match this value. (Note that $R_{in} = r_e \parallel R_E \simeq r_e$.) The amplifier is to have the greatest possible voltage gain and the largest possible output signal but retain small-signal linear operation (i.e., the signal component across the base–emitter junction should be limited to no more than 10 mV). Find appropriate values for R_E and R_C. What is the value of voltage gain realized?

*6.107 The transistor in the circuit shown in Fig. P6.107 is biased to operate in the active mode. Assuming that β is very large, find the collector bias current I_C. Replace the transistor with the small-signal equivalent circuit model of Fig. 6.41(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

$$\frac{v_{o1}}{v_i} = \frac{R_E}{R_E + r_e}$$

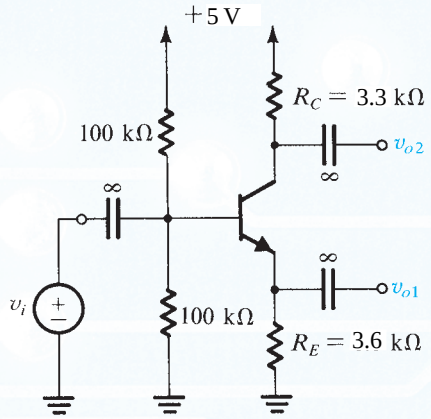


Figure P6.107

$$\frac{v_{o2}}{v_i} = \frac{-\alpha R_C}{R_E + r_e}$$

Find the values of these voltage gains (for $\alpha \simeq 1$). Now, if the terminal labeled v_{o1} is connected to ground, what does the voltage gain v_{o2}/v_i become?

Section 6.6: Basic BJT Amplifier Configurations †

6.108 An amplifier with an input resistance of 100 kΩ, an open-circuit voltage gain of 100 V/V, and an output resistance of 100 Ω, is connected between a 10-kΩ signal source and a 1-kΩ load. Find the overall voltage gain G_v. Also find the current gain, defined as the ratio of the load current to the current drawn from the signal source.

D 6.109 Specify the parameters R_{in}, A_{vo}, and R_o of an amplifier that is to be connected between a 100-kΩ source and a 2-kΩ load. The amplifier is required to meet the following specifications:

(a) No more than 10% of the signal strength is lost in the connection to the amplifier input.
(b) If the load resistance changes from the nominal value of 2 kΩ to a low value of 1 kΩ, the change in output voltage is limited to 10% of nominal value.
(c) The nominal overall voltage gain is 10 V/V.

6.110 Figure P6.110 shows an alternative equivalent circuit representation of an amplifier. If this circuit is to be equivalent to that in Fig. 6.50(b) show that $G_m = A_{vo}/R_o$. Also convince yourself that the transconductance G_m is defined as

$$G_m = \left.\frac{i_o}{v_i}\right|_{R_L = 0}$$

and hence is known as the short-circuit transconductance. Now if the amplifier is fed with a signal source (v_{sig}, R_{sig}) and is connected to a load resistance R_L, show that the gain of the amplifier proper A_v is given by $A_v = G_m(R_o \parallel R_L)$ and the overall voltage gain G_v is given by

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} G_m(R_o \parallel R_L)$$

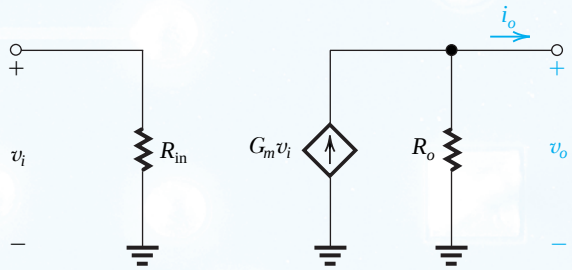


Figure P6.110

6.111 An alternative equivalent circuit of an amplifier fed with a signal source (v_{sig}, R_{sig}) and connected to a load R_L is shown in Fig. P6.111. Here G_{vo} is the open-circuit overall voltage gain,

$$G_{vo} = \left.\frac{v_o}{v_{sig}}\right|_{R_L=\infty}$$

and R_{out} is the output resistance with v_{sig} set to zero. This is different from R_o. Show that

$$G_{vo} = \frac{R_i}{R_i + R_{sig}} A_{vo}$$

where $R_i = \left.R_{in}\right|_{R_L=\infty}$.

Also show that the overall voltage gain

$$G_v = G_{vo} \frac{R_L}{R_L + R_{out}}$$

****6.112** Most practical amplifiers have internal feedback that make them nonunilateral. In such a case, R_{in} depends on R_L. To illustrate this point we show in Fig. P6.112 the equivalent circuit of an amplifier in which a feedback resistance R_f models the internal feedback mechanism that is present in this amplifier. It is R_f that makes the amplifier nonunilateral. Show that

$$R_{in} = R_1 \parallel \left[\frac{R_f + (R_2 \parallel R_L)}{1 + g_m(R_2 \parallel R_L)}\right]$$

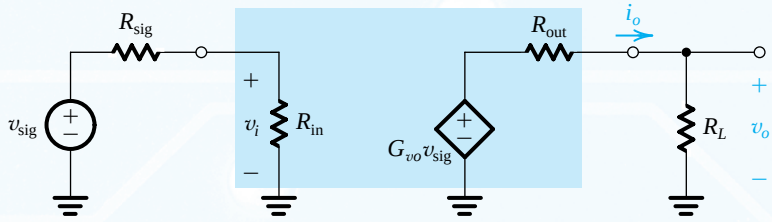


Figure P6.111

†Problems 6.108 to 6.111 are identical to problems 5.80 to 5.84.

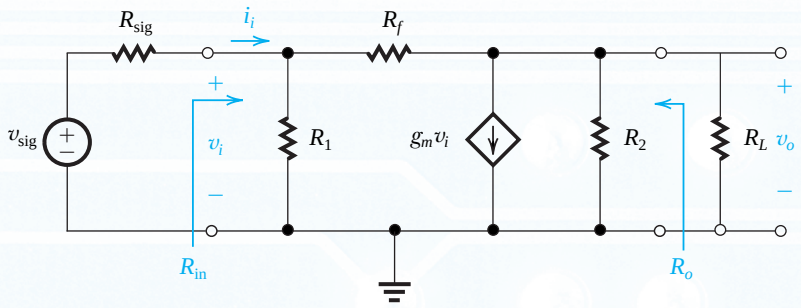


Figure P6.112

$$A_{vo} = -g_m R_2 \frac{1-(1/g_m R_f)}{1+(R_2/R_f)}$$

$$R_o = R_2 \parallel R_f$$

Evaluate R_{in}, A_{vo}, and R_o for the case $R_1 = 100\ \text{k}\Omega$, $R_f = 1\ \text{M}\Omega$, $g_m = 100$ mA/V, $R_2 = 100\ \Omega$, and $R_L = 1\ \text{k}\Omega$. Which of the amplifier characteristic parameters is most affected by R_f (i.e., relative to the case with $R_f = \infty$)? For $R_{sig} = 100\ \text{k}\Omega$, determine the overall voltage gain, G_v, with and without R_f present.

6.113 A CE amplifier utilizes a BJT with $\beta = 100$ and $V_A = 50$ V, biased at $I_C = 0.5$ mA; it has a collector resistance $R_C = 10\ \text{k}\Omega$. Assume $R_B \gg r_\pi$. Find R_{in}, R_o, and A_{vo}. If the amplifier is fed with a signal source having a resistance of $10\ \text{k}\Omega$, and a load resistance $R_L = 10\ \text{k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v. If the peak voltage of the sine wave appearing between base and emitter is to be limited to 5 mV, what $\hat{v}_{sig}$ is allowed, and what output voltage signal appears across the load?

D *6.114 In this problem we investigate the effect of the inevitable variability of β on the realized gain of the CE amplifier. For this purpose, use the overall gain expression in Eq. (6.79). Assume r_o is sufficiently large to be negligible and thus show that

$$|G_v| \simeq \frac{R'_L}{(R_{sig}/\beta)+(1/g_m)}$$

where $R'_L = R_L \parallel R_C$.

Consider the case $R'_L = 10\ \text{k}\Omega$ and $R_{sig} = 10\ \text{k}\Omega$, and let the BJT be biased at $I_C = 1$ mA. The BJT has a nominal β of 100.

(a) What is the nominal value of $|G_v|$?
(b) If β can be anywhere between 50 and 150, what is the corresponding range of $|G_v|$?
(c) If in a particular design, it is required to maintain $|G_v|$ within $\pm 20\ \%$ of its nominal value, what is the maximum allowable range of β?
(d) If it is not possible to restrict β to the range found in (c), and the designer has to contend with β in the range 50 to 150, what value of bias current I_C would result in $|G_v|$ falling in a range of $\pm 20\ \%$ of a new nominal value? What is the nominal value of $|G_v|$ in this case?

D 6.115 In this problem, we investigate the effect of changing the bias current I_C on the overall voltage gain G_v of a CE amplifier. Consider the situation of a CE amplifier operating with a signal source having $R_{sig} = 10\ \text{k}\Omega$ and having $R_C \parallel R_L = 10\ \text{k}\Omega$. The BJT is specified to have $\beta = 100$ and $V_A = 25$ V. Use Eq. (6.79) to find $|G_v|$ at $I_C = 0.1$ mA, 0.2 mA, 0.5 mA, 1.0 mA, and 1.25 mA. Observe the effect of r_o on limiting $|G_v|$ as I_C is increased. Find the value of I_C that results in $|G_v| = 50$ V/V.

6.116 Two identical CE amplifiers are connected in cascade. The first stage is fed with a source v_{sig} having a resistance $R_{sig} = 10\ \text{k}\Omega$. A load resistance $R_L = 10\ \text{k}\Omega$ is connected to the collector of the second stage. Each BJT is biased at $I_C = 0.25$ mA and has $\beta = 100$ and a very large V_A. Each stage utilizes a collector resistance $R_C = 10\ \text{k}\Omega$.

(a) Sketch the equivalent circuit of the two-stage amplifier.
(b) Calculate the voltage transmission from the signal source to the input of the first stage.
(c) Calculate the voltage gain of the first stage, A_{v1}.
(d) Calculate the voltage gain of the second stage, A_{v2}.
(e) Find the overall voltage gain, v_{o2}/v_{sig}.

6.117 A CE amplifier utilizes a BJT with $\beta = 100$ biased at $I_C = 0.5$ mA and has a collector resistance $R_C = 10\ \text{k}\Omega$ and a resistance $R_e = 150\ \Omega$ connected in the emitter. Find R_{in}, A_{vo}, and R_o. If the amplifier is fed with a signal source having a resistance of $10\ \text{k}\Omega$, and a load resistance $R_L = 10\ \text{k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v. If the peak voltage of the sine wave appearing between base and emitter is to be limited to 5 mV, what $\hat{v}_{sig}$ is allowed, and what output voltage signal appears across the load?

D 6.118 Design a CE amplifier with a resistance R_e in the emitter to meet the following specifications:

(i) Input resistance $R_{in} = 20\ k\Omega$.
(ii) When fed from a signal source with a peak amplitude of 0.1 V and a source resistance of 20 $k\Omega$, the peak amplitude of v_π is 5 mV.
Specify R_e and the bias current I_C. The BJT has $\beta = 100$. If the total resistance in the collector is 5 $k\Omega$, find the overall voltage gain G_v and the peak amplitude of the output signal v_o.

SIM **D 6.119** Inclusion of an emitter resistance R_e reduces the variability of the gain G_v due to the inevitable wide variance in the value of β. Consider a CE amplifier operating between a signal source with $R_{sig} = 10\ k\Omega$ and a total collector resistance $R_C \| R_L$ of 10 $k\Omega$. The BJT is biased at $I_C = 1$ mA and its β is specified to be nominally 100 but can lie in the range of 50 to 150. First determine the nominal value and the range of $|G_v|$ without resistance R_e. Then select a value for R_e that will ensure that $|G_v|$ be within ±20 % of its new nominal value. Specify the value of R_e, the new nominal value of $|G_v|$, and the expected range of $|G_v|$.

D 6.120 A CB amplifier is operating with $R_L = 10\ k\Omega$, $R_C = 10\ k\Omega$, and $R_{sig} = 100\ \Omega$. At what current I_C should the transistor be biased for the input resistance R_{in} to equal that of the signal source? What is the resulting overall voltage gain? Assume $\alpha \simeq 1$.

6.121 For the circuit in Fig. P6.121, let $R_{sig} \gg r_e$ and $\alpha \simeq 1$. Find v_o.

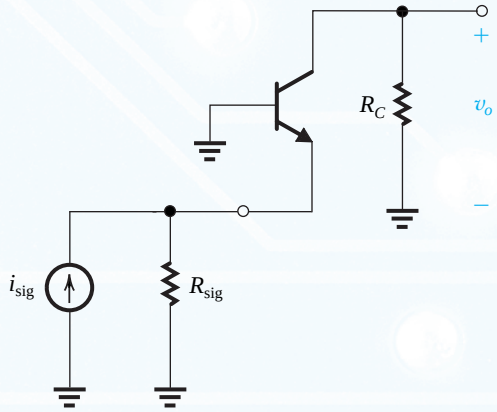


Figure P6.121

6.122 A CB amplifier is biased at $I_E = 0.25$ mA with $R_C = R_L = 10\ k\Omega$ and is driven by a signal source with $R_{sig} = 1\ k\Omega$. Find the overall voltage gain G_v. If the maximum signal amplitude of the voltage between base and emitter is limited to 10 mV, what are the corresponding amplitudes of v_{sig} and v_o? Assume $\alpha \simeq 1$.

D 6.123 An emitter follower is required to deliver a 0.5 -V peak sinusoid to a 2 -kΩ load. If the peak amplitude of v_{be} is to be limited to 5 mV, what is the lowest value of I_E at which the BJT can be biased? At this bias current, what are the maximum and minimum currents that the BJT will be conducting (at the positive and negative peaks of the output sine wave)? If the resistance of the signal source is 200 $k\Omega$, what value of G_v is obtained? Thus determine the required amplitude of v_{sig}.

6.124 An emitter follower with a BJT biased at $I_C = 1$ mA and having $\beta = 100$ is connected between a source with $R_{sig} = 20\ k\Omega$ and a load $R_L = 1\ k\Omega$.

(a) Find R_{in}, v_b/v_{sig}, and v_o/v_{sig}.
(b) If the signal amplitude across the base–emitter junction is to be limited to 10 mV, what is the corresponding amplitude of v_{sig} and v_o?
(c) Find the open-circuit voltage gain G_{vo} and the output resistance R_{out}. Use these values first to verify the value of G_v obtained in (a), then to find the value of G_v obtained with R_L reduced to 500 Ω.

6.125 An emitter follower is operating at a collector bias current of 0.25 mA and is used to connect a 10 -kΩ source to a 1-kΩ load. If the nominal value of β is 100, what output resistance R_{out} and overall voltage gain G_v result? Now if transistor β is specified to lie in the range 50 to 150, find the corresponding range of R_{out} and G_v.

6.126 An emitter follower, when driven from a 10-kΩ source, was found to have an output resistance R_{out} of 200 Ω. The output resistance increased to 300 Ω when the source resistance was increased to 20 $k\Omega$. Find the overall voltage gain when the follower is driven by a 30-kΩ source and loaded by a 1-kΩ resistor.

6.127 For the general amplifier circuit shown in Fig. P6.127 neglect the Early effect.

(a) Find expressions for v_c/v_{sig} and v_e/v_{sig}.
(b) If v_{sig} is disconnected from node X, node X is grounded, and node Y is disconnected from ground and connected to v_{sig}, find the new expression for v_c/v_{sig}.

Section 6.7: Biasing in BJT Amplifier Circuits

D 6.128 For the circuit in Fig. 6.59(a), neglect the base current I_B in comparison with the current in the voltage divider. It is required to bias the transistor at $I_C = 1$ mA, which requires selecting R_{B1} and R_{B2} so that $V_{BE} = 0.690$ V. If $V_{CC} = 3$ V, what must the ratio R_{B1}/R_{B2} be? Now, if R_{B1} and

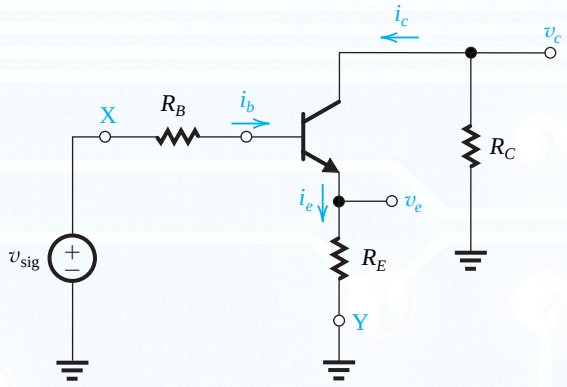


Figure P6.127

R_{B2} are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for V_{BE}? What is the corresponding range of I_C? If $R_C = 2$ kΩ, what is the range obtained for V_{CE}? Comment on the efficacy of this biasing arrangement.

D 6.129 It is required to bias the transistor in the circuit of Fig. 6.59(b) at $I_C = 1$ mA. The transistor β is specified to be nominally 100, but it can fall in the range of 50 to 150. For $V_{CC} = +3$ V and $R_C = 2$ kΩ, find the required value of R_B to achieve $I_C = 1$ mA for the "nominal" transistor. What is the expected range for I_C and V_{CE}? Comment on the efficacy of this bias design.

D 6.130 Consider the single-supply bias network shown in Fig. 6.60(a). Provide a design using a 9-V supply in which the supply voltage is equally split between R_C, V_{CE}, and R_E with a collector current of 0.6 mA. The transistor β is specified to have a minimum value of 90. Use a voltage divider current of $I_E/10$, or slightly higher. Since a reasonable design should operate for the best transistors for which β is very high, do your initial design with $\beta = \infty$. Then choose suitable 5% resistors (see Appendix H), making the choice in a way that will result in a V_{BB} that is slightly higher than the ideal value. Specify the values you have chosen for R_E, R_C, R_1, and R_2. Now, find V_B, V_E, V_C, and I_C for your final design using $\beta = 90$.

D 6.131 Repeat Problem 6.130, but use a voltage divider current that is $I_E/2$. Check your design at $\beta = 90$. If you have the data available, find how low β can be while the value of I_C does not fall below that obtained with the design of Problem 6.130 for $\beta = 90$.

D *6.132 It is required to design the bias circuit of Fig. 6.60 for a BJT whose nominal $\beta = 100$.

(a) Find the largest ratio (R_B/R_E) that will guarantee I_E remain within ±10% of its nominal value for β as low as 50 and as high as 150.

(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BB} \equiv V_{CC} R_2/(R_1 + R_2)$ that will result in a voltage drop of $V_{CC}/3$ across R_E.
(c) For $V_{CC} = 5$ V, find the required values of R_1, R_2, and R_E to obtain $I_E = 0.5$ mA and to satisfy the requirement for stability of I_E in (a).
(d) Find R_C so that $V_{CE} = 1.5$ V for β equal to its nominal value.

Check your design by evaluating the resulting range of I_E.

D *6.133 Consider the two-supply bias arrangement shown in Fig. 6.61 using ±3-V supplies. It is required to design the circuit so that $I_C = 0.6$ mA and V_C is placed midway between V_{CC} and V_E.

(a) For $\beta = \infty$, what values of R_E and R_C are required?
(b) If the BJT is specified to have a minimum β of 90, find the largest value for R_B consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across R_E.
(c) What standard 5% resistor values (see Appendix H) would you use for R_B, R_E, and R_C? In making your selection, use somewhat lower values in order to compensate for the low-β effects.
(d) For the values you selected in (c), find I_C, V_B, V_E, and V_C for $\beta = \infty$ and for $\beta = 90$.

D *6.134 Utilizing ±3-V power supplies, it is required to design a version of the circuit in Fig. 6.61 in which the signal will be coupled to the emitter and thus R_B can be set to zero. Find values for R_E and R_C so that a dc emitter current of 0.5 mA is obtained and so that the gain is maximized while allowing ±1 V of signal swing at the collector. If temperature increases from the nominal value of 25°C to 125°C, estimate the percentage change in collector bias current. In addition to the −2 mV/°C change in V_{BE}, assume that the transistor β changes over this temperature range from 50 to 150.

SIM **D 6.135** Using a 3-V power supply, design a version of the circuit of Fig. 6.62 to provide a dc emitter current of 0.5 mA and to allow a ±1-V signal swing at the collector. The BJT has a nominal $\beta = 100$. Use standard 5% resistor values (see Appendix H). If the actual BJT used has $\beta = 50$, what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for $\beta = 150$.

D *6.136 (a) Using a 3-V power supply, design the feedback bias circuit of Fig. 6.62 to provide $I_C = 3$ mA and $V_C = V_{CC}/2$ for $\beta = 90$.
(b) Select standard 5% resistor values, and reevaluate V_C and I_C for $\beta = 90$.
(c) Find V_C and I_C for $\beta = \infty$.
(d) To improve the situation that obtains when high-β transistors are used, we have to arrange for an additional current to flow through R_B. This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P6.136.

Design this circuit for $\beta = 90$. Use a current through R_{B2} equal to the base current. Now, what values of V_C and I_C result with $\beta = \infty$?

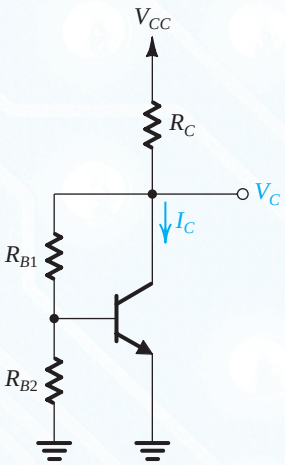


Figure P6.136

D 6.137 A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P6.137. Find the values of I and R_B to bias the BJT at $I_C = 1$ mA and $V_C = 1.5$ V. Let $\beta = 100$.

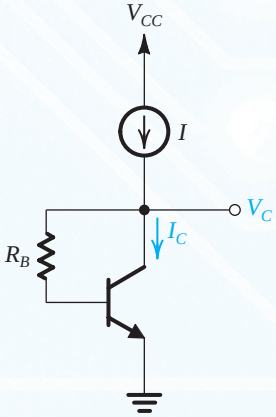


Figure P6.137

6.138 The circuit in Fig. P6.138 provides a constant current I_O as long as the circuit to which the collector is connected maintains the BJT in the active mode. Show that

$$I_O = \alpha \frac{V_{CC}[R_2/(R_1 + R_2)] - V_{BE}}{R_E + (R_1 \| R_2)/(\beta + 1)}$$

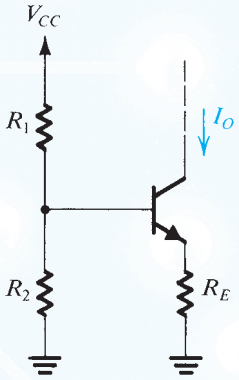


Figure P6.138

D **6.139 The current-source biasing circuit shown in Fig. P6.139 provides a bias current to Q_1 that is determined by the current source formed by Q_2, R_1, R_2, and R_E. The bias current is independent of R_B and nearly independent of β_1 (as long as both Q_1 and Q_2 operate in the active mode). It is required to design the circuit using ± 5-V dc supplies to establish $I_{C1} = 0.1$ mA and $V_{CE1} = 1.5$ V, in the ideal situation of infinite β_1 and β_2. In designing the current source, use 2-V dc voltage drop across R_E and impose the requirement that I_{E2} remain within 5% of its ideal value for β_2 as low as 50. In selecting a value for R_B, ensure that for the lowest value of $\beta_1 = 50$, V_{CE2} is 2.5 V. Use standard 5% resistor values (see Appendix H). What values for R_1, R_2, R_E, R_B, and R_C do you choose? What values of I_{C1} and V_{CE1} result for $\beta_1 = \beta_2 = 50$, 100, and 200?

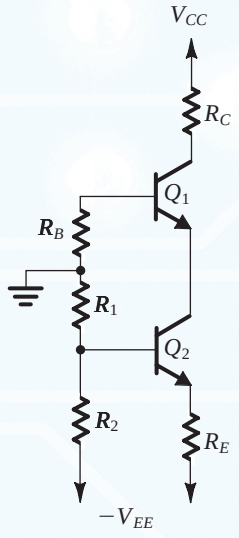


Figure P6.139

SIM **D *6.140** For the circuit in Fig. P6.140, assuming all transistors to be identical with β infinite, derive an expression for the output current I_O, and show that by selecting

$$R_1 = R_2$$

and keeping the current in each junction the same, the current I_O will be

$$I_O = \frac{V_{CC}}{2R_E}$$

which is independent of V_{BE}. What must the relationship of R_E to R_1 and R_2 be? For $V_{CC} = 10$ V and $V_{BE} = 0.7$ V, design the circuit to obtain an output current of 0.5 mA. What is the lowest voltage that can be applied to the collector of Q_3?

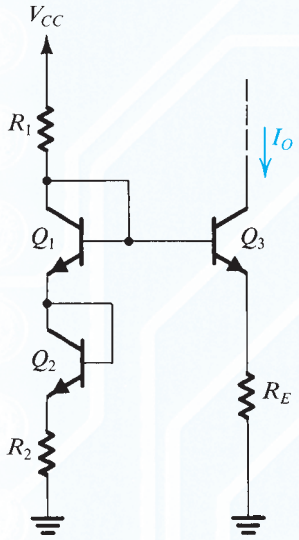


Figure P6.140

D 6.141 For the circuit in Fig. P6.141 find the value of R that will result in $I_O \simeq 1$ mA. What is the largest voltage that can be applied to the collector? Assume $|V_{BE}| = 0.7$ V.

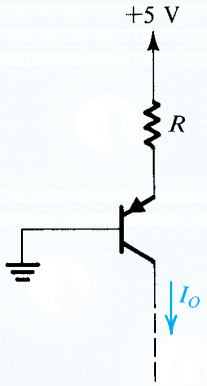


Figure P6.141

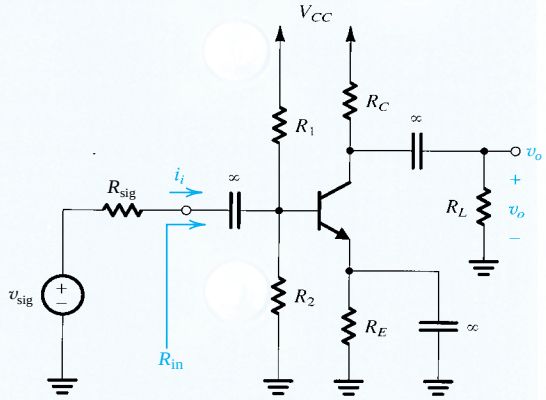


Figure P6.142

Section 6.8: Discrete-Circuit BJT Amplifiers

6.142 For the common-emitter amplifier shown in Fig. P6.142, let $V_{CC} = 15$ V, $R_1 = 27$ kΩ, $R_2 = 15$ kΩ, $R_E = 2.4$ kΩ, and $R_C = 3.9$ kΩ. The transistor has $\beta = 100$. Calculate the dc bias current I_C. If the amplifier operates between a source for which $R_{sig} = 2$ kΩ and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, and the overall voltage gain v_o/v_{sig}.

D 6.143 Using the topology of Fig. P6.142, design an amplifier to operate between a 2-kΩ source and a 2-kΩ load with a gain v_o/v_{sig} of –40 V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has $\beta = 100$. Use standard 5% resistor (see Appendix H).

6.144 A designer, having examined the situation described in Problem 6.142 and estimating the available gain to be approximately –36.6 V/V, wants to explore the possibility of improvement by reducing the loading of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3: R_1 to 82 kΩ, R_2 to 47 kΩ, R_E to 7.2 kΩ, and R_C to 12 kΩ (standard values of 5%-tolerance resistors). With $V_{CC} = 15$ V, $R_{sig} = 2$ kΩ, $R_L = 2$ kΩ, and $\beta = 100$, what does the gain become? Comment.

D 6.145 Consider the CE amplifier circuit of Fig. 6.65(a). It is required to design the circuit (i.e., find values for I, R_B, and R_C) to meet the following specifications:

(a) $R_{in} \simeq 5$ kΩ

(b) The dc voltage drop across R_B is approximately 0.2 V.
(c) The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never falls by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that v_{sig} is a sinusoidal source, the available supply $V_{CC} = 3$ V, and the transistor has $\beta = 100$. Use standard 5% resistance values, and specify the value of I to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If $R_{sig} = R_L = 10$ kΩ, what is the overall voltage gain?

D 6.146 In the circuit of Fig. P6.146, v_{sig} is a small sine-wave signal with zero average. The transistor β is 100.

(a) Find the value of R_E to establish a dc emitter current of about 0.5 mA.
(b) Find R_C to establish a dc collector voltage of about +1 V.
(c) For $R_L = 10$ kΩ, draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

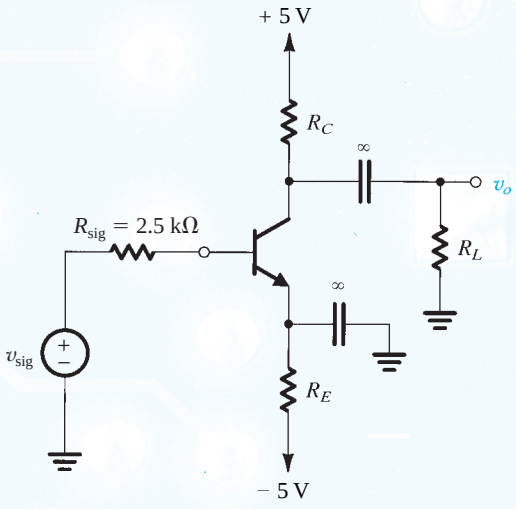


Figure P6.146

***6.147** The amplifier of Fig. P6.147 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage, R_{in2}, constitutes the load resistance of the first stage.

(a) For $V_{CC} = 9$ V, $R_1 = 100$ kΩ, $R_2 = 47$ kΩ, $R_E = 3.9$ kΩ, $R_C = 6.8$ kΩ, and $\beta = 100$, determine the dc collector current and dc collector voltage of each transistor.
(b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components.
(c) Find R_{in1} and v_{b1}/v_{sig} for $R_{sig} = 5$ kΩ.
(d) Find R_{in2} and v_{b2}/v_{b1}.
(e) For $R_L = 2$ kΩ, find v_o/v_{b2}.
(f) Find the overall voltage gain v_o/v_{sig}.

6.148 In the circuit of Fig. P6.148, v_{sig} is a small sine-wave signal. Find R_{in} and the gain v_o/v_{sig}. Assume $\beta = 100$. If the amplitude of the signal v_{be} is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

***6.149** The BJT in the circuit of Fig. P6.149 has $\beta = 100$.

(a) Find the dc collector current and the dc voltage at the collector.

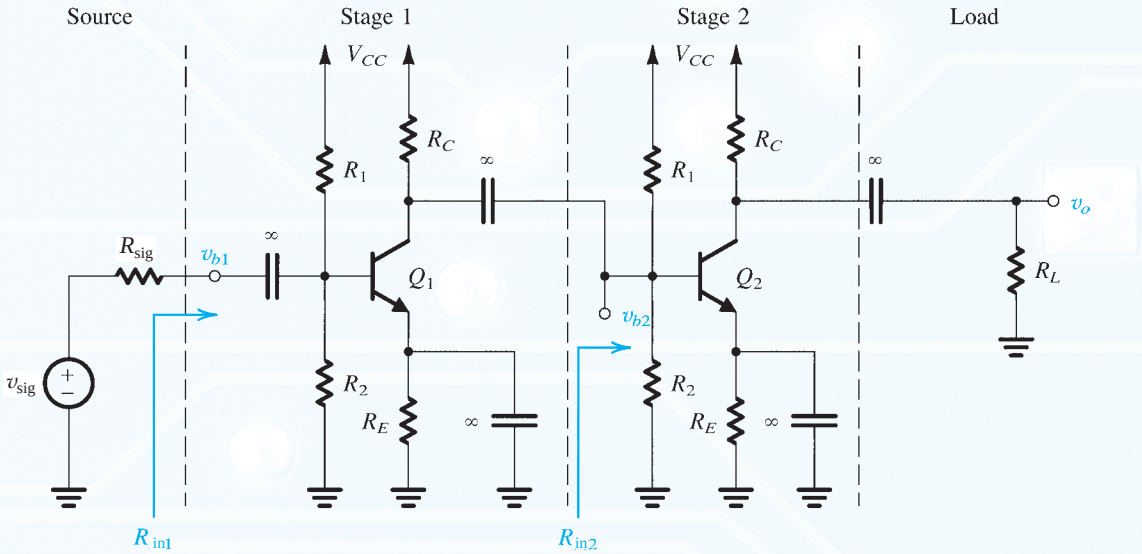


Figure P6.147

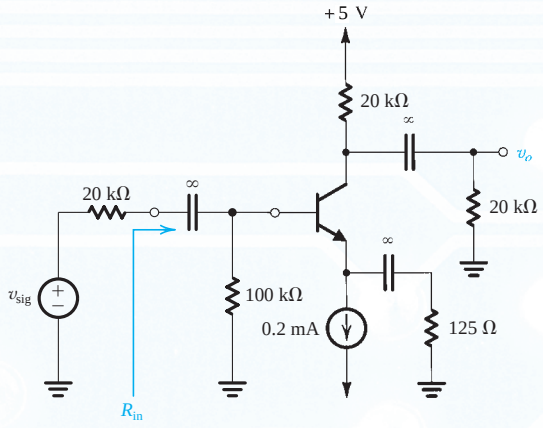


Figure P6.148

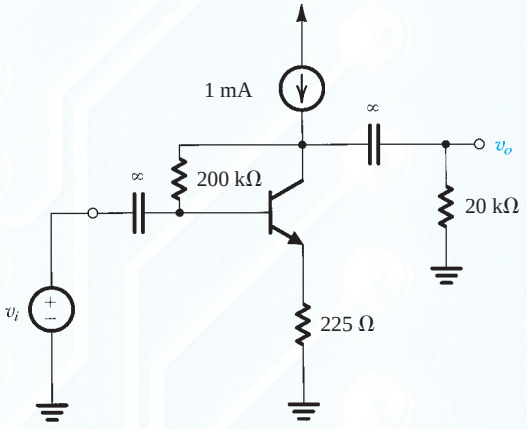


Figure P6.149

(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_o/v_i.

D ***6.150** Consider the CB amplifier of Fig. 6.67(a) with the collector voltage signal coupled to a 1-kΩ load resistance through a large capacitor. Let the power supplies be ±3 V. The source has a resistance of 50 Ω. Design the circuit so that the amplifier input resistance is matched to that of the source and the output signal swing is as large as possible with relatively low distortion (v_{be} limited to 10 mV). Find I and R_C and calculate the overall voltage gain obtained and the output signal swing. Assume $\alpha \simeq 1$.

6.151 For the circuit in Fig. P6.151, find the input resistance R_{in} and the voltage gain v_o/v_{sig}. Assume that the source provides a small signal v_{sig} and that $\beta = 100$.

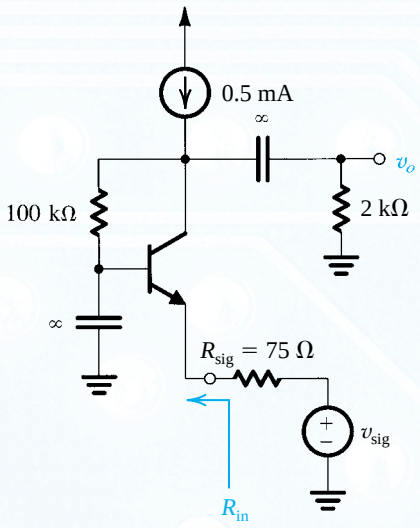


Figure P6.151

6.152 For the emitter-follower circuit shown in Fig. P6.152, the BJT used is specified to have β values in the range of 50 to 200 (a distressing situation for the circuit designer). For the two extreme values of β ($\beta = 50$ and $\beta = 200$), find:

(a) I_E, V_E, and V_B.
(b) the input resistance R_{in}.
(c) the voltage gain v_o/v_{sig}.

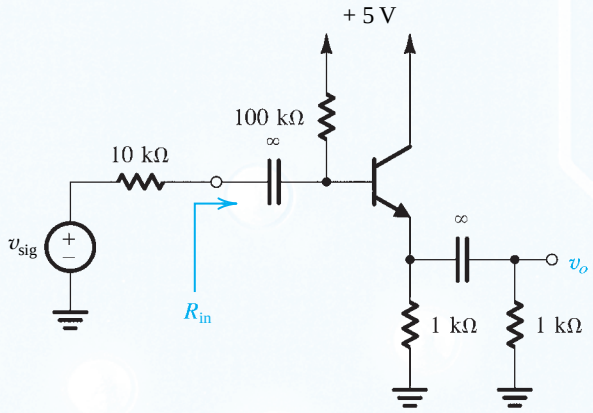


Figure P6.152

6.153 For the emitter follower in Fig. P6.153, the signal source is directly coupled to the transistor base. If the dc component of v_{sig} is zero, find the dc emitter current. Assume $\beta = 100$. Neglecting r_o, find R_{in}, the voltage gain v_o/v_{sig}, the current gain i_o/i_i, and the output resistance R_{out}.

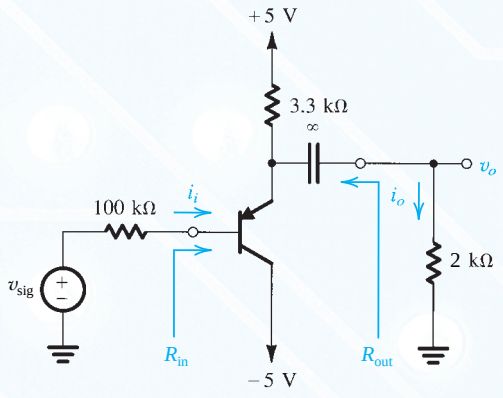


Figure P6.153

6.154 For the circuit in Fig. P6.154, called a **bootstrapped follower:

(a) Find the dc emitter current and g_m, r_e, and r_π. Use $\beta = 100$.

(b) Replace the BJT with its T model (neglecting r_o), and analyze the circuit to determine the input resistance R_{in} and the voltage gain v_o/v_{sig}.

(c) Repeat (b) for the case when capacitor C_B is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

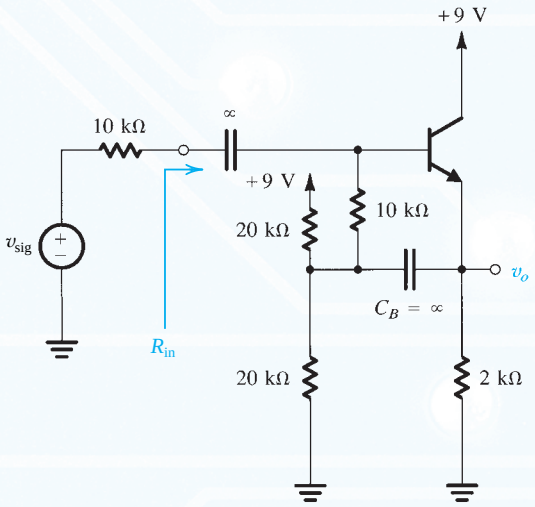


Figure P6.154

**6.155 For the follower circuit in Fig. P6.155, let transistor Q_1 have $\beta = 50$ and transistor Q_2 have $\beta = 100$, and neglect the effect of r_o. Use $V_{BE} = 0.7$ V.

(a) Find the dc emitter currents of Q_1 and Q_2. Also, find the dc voltages V_{B1} and V_{B2}.

(b) If a load resistance $R_L = 1$ kΩ is connected to the output terminal, find the voltage gain from the base to the emitter of Q_2, v_o/v_{b2}, and find the input resistance R_{ib2} looking into the base of Q_2. (*Hint:* Consider Q_2 as an emitter follower fed by a voltage v_{b2} at its base.)

(c) Replacing Q_2 with its input resistance R_{ib2} found in (b), analyze the circuit of emitter follower Q_1 to determine its input resistance R_{in}, and the gain from its base to its emitter, v_{e1}/v_{b1}.

(d) If the circuit is fed with a source having a 100-kΩ resistance, find the transmission to the base of Q_1, v_{b1}/v_{sig}.

(e) Find the overall voltage gain v_o/v_{sig}.

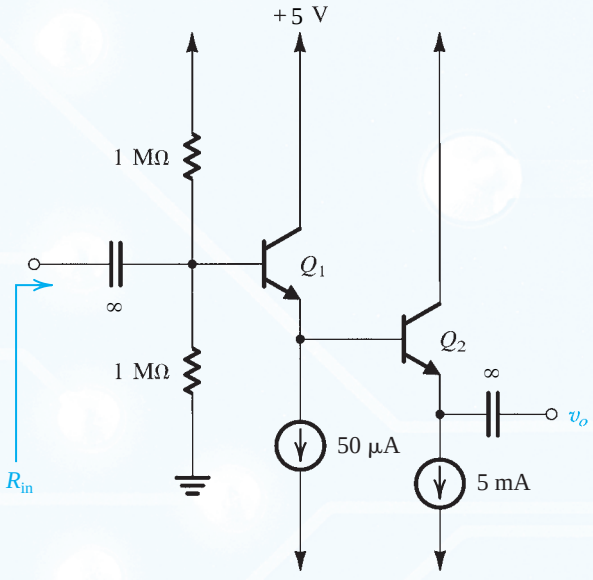


Figure P6.155

D 6.156 A CE amplifier has a midband voltage gain of $|A_M| = 100$ V/V, a lower 3-dB frequency of $f_L = 100$ Hz, and a higher 3-dB frequency $f_L = 100$ MHz. In Chapter 9 we will learn that connecting a resistance R_e in the emitter of the BJT results in lowering f_L and raising f_H by the factor $(1 + g_m R_e)$. If the BJT is biased at $I_C = 1$ mA, find R_e that will result in f_H at least equal to 5 MHz. What will the new values of f_L and A_M be?