

CHAPTER 5

MOS Field-Effect Transistors (MOSFETs)

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IN THIS CHAPTER YOU WILL LEARN

1. The physical structure of the MOS transistor and how it works.
2. How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current-voltage characteristics.
3. How to analyze and design circuits that contain MOS transistors, resistors, and dc sources.
4. How the transistor can be used to make an amplifier, and how it can be used as a switch in digital circuits.
5. How to obtain linear amplification from the fundamentally nonlinear MOS transistor.
6. The three basic ways for connecting a MOSFET to construct amplifiers with different properties.
7. Practical circuits for MOS-transistor amplifiers that can be constructed using discrete components.

Introduction

Having studied the junction diode, which is the most basic two-terminal semiconductor device, we now turn our attention to three-terminal semiconductor devices. Three-terminal devices are far more useful than two-terminal ones because they can be used in a multitude of applications, ranging from signal amplification to digital logic and memory. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way a three-terminal device can be used to realize a controlled source, which as we have learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. As we shall see in Chapter 13, the switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

There are two major types of three-terminal semiconductor devices: the metal-oxide-semiconductor field-effect transistor (MOSFET), which is studied in this chapter, and the

bipolar junction transistor (BJT), which we shall study in Chapter 6. Although each of the two transistor types offers unique features and areas of application, the MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs), which are entire circuits fabricated on a single silicon chip.

Compared to BJTs, MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip), and their manufacturing process is relatively simple (see Appendix A). Also, their operation requires comparatively little power. Furthermore, circuit designers have found ingenious ways to implement digital and analog functions utilizing MOSFETs almost exclusively (i.e., with very few or no resistors). All of these properties have made it possible to pack large numbers of MOSFETs (as many as 2 billion!) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) digital circuits such as those for memory and microprocessors. Analog circuits such as amplifiers and filters can also be implemented in MOS technology, albeit in smaller, less-dense chips. Also, both analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design.

The objective of this chapter is to develop in the reader a high degree of familiarity with the MOSFET: its physical structure and operation, terminal characteristics, circuit models, and basic circuit applications. Although discrete MOS transistors exist, and the material studied in this chapter will enable the reader to design discrete MOS circuits, our study of the MOSFET is strongly influenced by the fact that most of its applications are in integrated-circuit design. The design of IC analog and digital MOS circuits occupies a large proportion of the remainder of this book.

5.1 Device Structure and Physical Operation

The enhancement-type MOSFET is the most widely used field-effect transistor. Except for the last section, this chapter is devoted to the study of the enhancement-type MOSFET. We begin in this section by learning about its structure and physical operation. This will lead to the current–voltage characteristics of the device, studied in the next section.

5.1.1 Device Structure

Figure 5.1, shows the physical structure of the n -channel enhancement-type MOSFET. The meaning of the names “enhancement” and “ n -channel” will become apparent shortly. The transistor is fabricated on a p -type substrate, which is a single-crystal silicon wafer that provides physical support for the device (and for the entire circuit in the case of an integrated circuit). Two heavily doped n -type regions, indicated in the figure as the n^+ **source**¹ and the n^+ **drain** regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2) of thickness t_{ox} (typically 1 to 10 nm),² which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the **gate electrode** of the device. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the

¹The notation n^+ indicates heavily doped n -type silicon. Conversely, n^- is used to denote lightly doped n -type silicon. Similar notation applies for p -type silicon.

²A nanometer (nm) is 10^{-9} m or 0.001 μm . A micrometer (μm), or micron, is 10^{-6} m. Sometimes the oxide thickness is expressed in angstroms. An angstrom (\AA) is 10^{-1} nm, or 10^{-10} m.

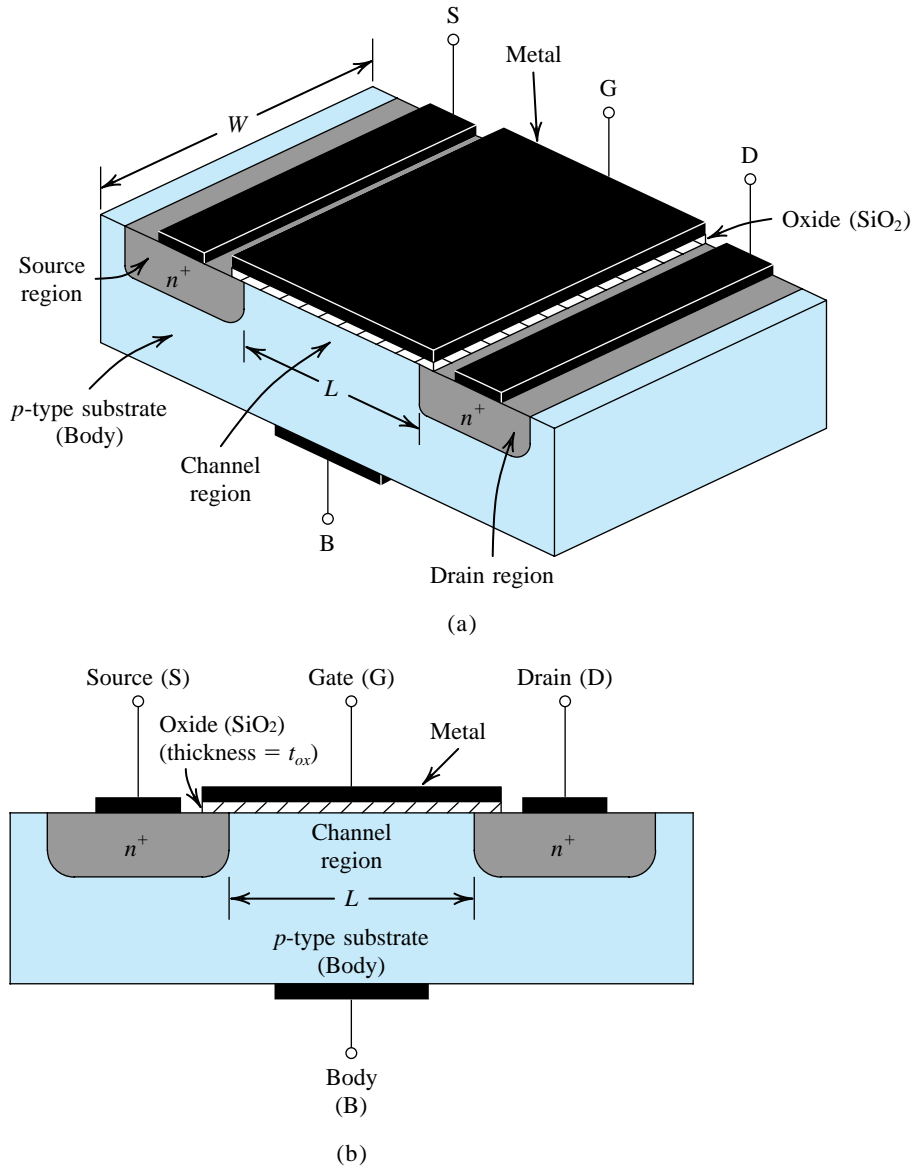


Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically $L = 0.03\ \mu\text{m}$ to $1\ \mu\text{m}$, $W = 0.1\ \mu\text{m}$ to $100\ \mu\text{m}$, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.

body.³ Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

At this point it should be clear that the name of the device (metal-oxide-semiconductor FET) is derived from its physical structure. The name, however, has become a general one and

³In Fig. 5.1, the contact to the body is shown on the bottom of the device. This will prove helpful in Section 5.9 in explaining a phenomenon known as the “body effect.” It is important to note, however, that in actual ICs, contact to the body is made at a location on the top of the device.

is used also for FETs that do not use metal for the gate electrode. In fact, most modern MOSFETs are fabricated using a process known as silicon-gate technology, in which a certain type of silicon, called polysilicon, is used to form the gate electrode (see Appendix A). Our description of MOSFET operation and characteristics applies irrespective of the type of gate electrode.

Another name for the MOSFET is the **insulated-gate FET** or **IGFET**. This name also arises from the physical structure of the device, emphasizing the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation that causes the current in the gate terminal to be extremely small (of the order of 10^{-15} A).

Observe that the substrate forms *pn* junctions with the source and drain regions. In normal operation these *pn* junctions are kept reverse-biased at all times. Since, as we shall see shortly, the drain will always be at a positive voltage relative to the source, the two *pn* junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal. We shall assume this to be the case in the following description of MOSFET operation. Thus, here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a three-terminal device, with the terminals being the gate (G), the source (S), and the drain (D). It will be shown that a voltage applied to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled “channel region.” Note that this region has a length L and a width W , two important parameters of the MOSFET. Typically, L is in the range of $0.03\text{ }\mu\text{m}$ to $1\text{ }\mu\text{m}$, and W is in the range of $0.1\text{ }\mu\text{m}$ to $100\text{ }\mu\text{m}$. Finally, note that the MOSFET is a symmetrical device; thus its source and drain can be interchanged with no change in device characteristics.

5.1.2 Operation with Zero Gate Voltage

With zero voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the *pn* junction between the n^+ drain region and the *p*-type substrate, and the other diode is formed by the *pn* junction between the *p*-type substrate and the n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12}\text{ }\Omega$).

5.1.3 Creating a Channel for Current Flow

Consider next the situation depicted in Fig. 5.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS} . The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are “uncovered” because the neutralizing holes have been pushed downward into the substrate.

As well, the positive gate voltage attracts electrons from the n^+ source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an *n* region is in effect created, connecting the source and drain regions, as indicated in Fig. 5.2. Now if a voltage is applied between drain and source, current flows through this induced *n* region, carried by the mobile electrons. The *induced n* region thus forms a **channel** for current flow from drain to source and is aptly called so. Correspondingly, the MOSFET of Fig. 5.2 is called an ***n*-channel MOSFET** or, alternatively, an **NMOS transistor**. Note that an *n*-channel MOSFET is

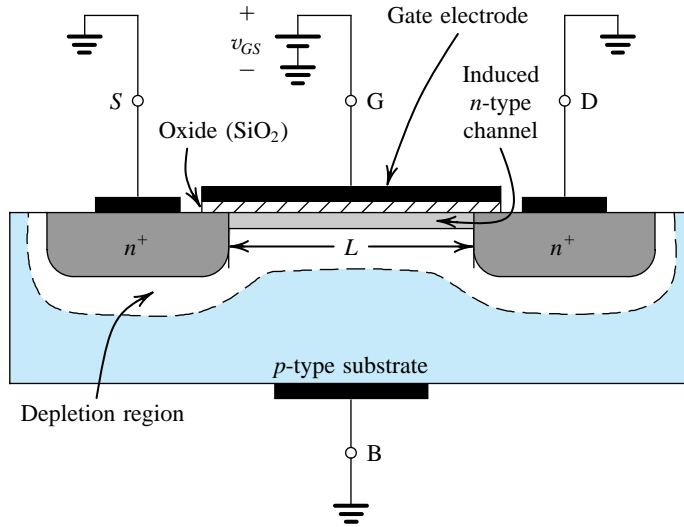


Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

formed in a p -type substrate: The channel is created by *inverting* the substrate surface from p type to n type. Hence the induced channel is also called an **inversion layer**.

The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t .⁴ Obviously, V_t for an n -channel FET is positive. The value of V_t is controlled during device fabrication and typically lies in the range of 0.3 V to 1.0 V.

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is applied. This is the origin of the name “field-effect transistor” (FET).

The voltage across this parallel-plate capacitor, that is, the voltage across the oxide, must exceed V_t for a channel to form. When $v_{DS} = 0$, as in Fig. 5.2, the voltage at every point along the channel is zero, and the voltage across the oxide (i.e., between the gate and the points along the channel) is uniform and equal to v_{GS} . The excess of v_{GS} over V_t is termed the **effective voltage** or the **overdrive voltage** and is the quantity that determines the charge in the channel. In this book, we shall denote $(v_{GS} - V_t)$ by v_{OV} ,

$$v_{GS} - V_t \equiv v_{OV} \quad (5.1)$$



We can express the magnitude of the electron charge in the channel by

$$|Q| = C_{ox}(WL)v_{OV} \quad (5.2)$$



⁴Some texts use V_t to denote the threshold voltage. We use V_t to avoid confusion with the thermal voltage V_T .

where C_{ox} , called the **oxide capacitance**, is the capacitance of the parallel-plate capacitor per unit gate area (in units of F/m²), W is the width of the channel, and L is the length of the channel. The oxide capacitance C_{ox} is given by

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (5.3)$$

where ϵ_{ox} is the permittivity of the silicon dioxide,

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

The oxide thickness t_{ox} is determined by the process technology used to fabricate the MOSFET. As an example, for a process with $t_{ox} = 4 \text{ nm}$,

$$C_{ox} = \frac{3.45 \times 10^{-11}}{4 \times 10^{-9}} = 8.6 \times 10^{-3} \text{ F/m}^2$$

It is much more convenient to express C_{ox} per micron squared. For our example, this yields $8.6 \text{ fF}/\mu\text{m}^2$, where fF denotes femtofarad (10^{-15} F). For a MOSFET fabricated in this technology with a channel length $L = 0.18 \mu\text{m}$ and a channel width $W = 0.72 \mu\text{m}$, the total capacitance between gate and channel is

$$C = C_{ox}WL = 8.6 \times 0.18 \times 0.72 = 1.1 \text{ fF}$$

Finally, note from Eq. (5.2) that as v_{OV} is increased, the magnitude of the channel charge increases proportionately. Sometimes this is depicted as an increase in the depth of the channel; that is, the larger the overdrive voltage, the deeper the channel.

5.1.4 Applying a Small v_{DS}

Having induced a channel, we now apply a positive voltage v_{DS} between drain and source, as shown in Fig. 5.3. We first consider the case where v_{DS} is small (i.e., 50 mV or so). The voltage v_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_D , will be from drain to source, as indicated in Fig. 5.3.

We now wish to calculate the value of i_D . Toward that end, we first note that because v_{DS} is small, we can continue to assume that the voltage between the gate and various points along the channel remains approximately constant and equal to the value at the source end, v_{GS} . Thus, the effective voltage between the gate and the various points along the channel remains equal to v_{OV} , and the channel charge Q is still given by Eq. (5.2). Of particular interest in calculating the current i_D is the charge per unit channel length, which can be found from Eq. (5.2) as

$$\frac{|Q|}{\text{unit channel length}} = C_{ox}Wv_{OV} \quad (5.4)$$

The voltage v_{DS} establishes an electric field E across the length of the channel,

$$|E| = \frac{v_{DS}}{L} \quad (5.5)$$

This electric field in turn causes the channel electrons to drift toward the drain with a velocity given by

$$\text{Electron drift velocity} = \mu_n |E| = \mu_n \frac{v_{DS}}{L} \quad (5.6)$$

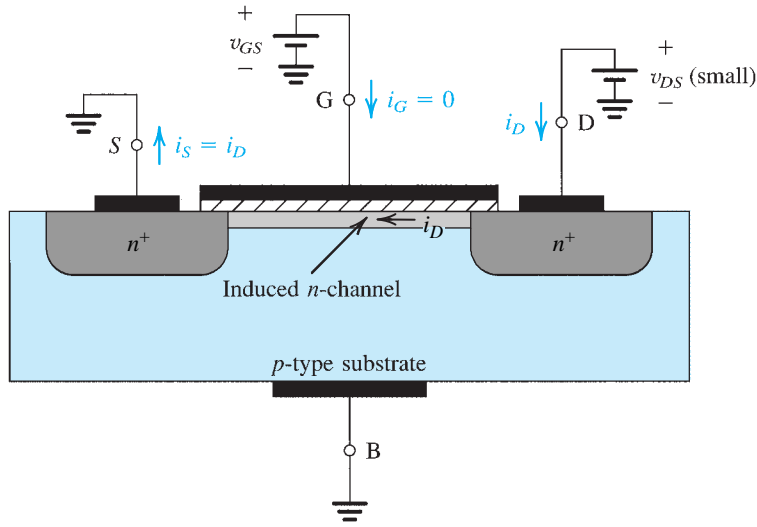


Figure 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS} . Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

where μ_n is the mobility of the electrons at the surface of the channel. It is a physical parameter whose value depends on the fabrication process technology. The value of i_D can now be found by multiplying the charge per unit channel length (Eq. 5.4) by the electron drift velocity (Eq. 5.6),

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) v_{OV} \right] v_{DS} \quad (5.7)$$

Thus, for small v_{DS} , the channel behaves as a linear resistance whose value is controlled by the overdrive voltage v_{OV} , which in turn is determined by v_{GS} :

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t) \right] v_{DS} \quad (5.8)$$

The conductance g_{DS} of the channel can be found from Eq. (5.7) or (5.8) as

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) v_{OV} \quad (5.9)$$

or

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t) \quad (5.10)$$

Observe that the conductance is determined by the product of three factors: $(\mu_n C_{ox})$, (W/L) , and v_{OV} (or equivalently, $v_{GS} - V_t$). To gain insight into MOSFET operation, we consider each of the three factors in turn.

The first factor, $(\mu_n C_{ox})$, is determined by the process technology used to fabricate the MOSFET. It is the product of the electron mobility, μ_n , and the oxide capacitance, C_{ox} . It makes physical sense for the channel conductance to be proportional to each of μ_n and C_{ox}

(why?) and hence to their product, which is termed the **process transconductance parameter**⁵ and given the symbol k'_n where the subscript n denotes n channel,

$$k'_n = \mu_n C_{ox} \quad (5.11)$$

It can be shown that with μ_n having the dimensions of meters squared per volt-second ($\text{m}^2/\text{V}\cdot\text{s}$) and C_{ox} having the dimensions of farads per meter squared (F/m^2), the dimensions of k'_n are amperes per volt squared (A/V^2).

The second factor in the expression for the conductance g_{DS} in Eqs. (5.9) and (5.10) is the transistor **aspect ratio** (W/L). That the channel conductance is proportional to the channel width W and inversely proportional to the channel length L should make perfect physical sense. The (W/L) ratio is obviously a dimensionless quantity that is determined by the device designer. Indeed, the values of W and L can be selected by the device designer to give the device the $i-v$ characteristics desired. For a given fabrication process, however, there is a minimum channel length, L_{\min} . In fact, the minimum channel length that is possible with a given fabrication process is used to characterize the process and is being continually reduced as technology advances. For instance, in 2009 the state-of-the-art in commercially available MOS technology was a 45-nm process, meaning that for this process the minimum channel length possible was 45 nm. Finally, we should note that the oxide thickness t_{ox} scales down with L_{\min} . Thus, for a 0.13- μm technology, t_{ox} is 2.7 nm, but for the modern 45-nm technology t_{ox} is about 1.4 nm.

The product of the process transconductance parameter k'_n and the transistor aspect ratio (W/L) is the **MOSFET transconductance parameter** k_n ,

$$k_n = k'_n (W/L) \quad (5.12a)$$

or

$$k_n = (\mu_n C_{ox}) (W/L) \quad (5.12b)$$

The MOSFET parameter k_n has the dimensions of A/V^2 .

The third term in the expression of the channel conductance g_{DS} is the overdrive voltage v_{OV} . This is hardly surprising since v_{OV} directly determines the magnitude of electron charge in the channel. As will be seen, v_{OV} is a very important circuit-design parameter. In this book, we will use v_{OV} and $v_{GS} - V_t$ interchangeably.

We conclude this subsection by noting that with v_{DS} kept small, the MOSFET behaves as a linear resistance r_{DS} whose value is controlled by the gate voltage v_{GS} ,

$$r_{DS} = \frac{1}{g_{DS}} \quad (5.13a)$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}} \quad (5.13b)$$

The operation of the MOSFET as a voltage-controlled resistance is further illustrated in Fig. 5.4, which is a sketch of i_D versus v_{DS} for various values of v_{GS} . Observe that the

⁵This name arises from the fact that $(\mu_n C_{ox})$ determines the transconductance of the MOSFET, as will be seen shortly.

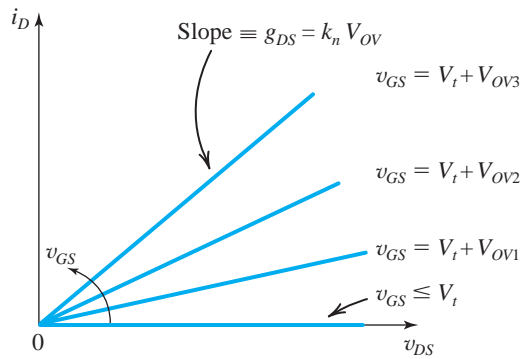


Figure 5.4 The i_D - v_{DS} characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source, v_{DS} , is kept small. The device operates as a linear resistance whose value is controlled by v_{GS} .

resistance is infinite for $v_{GS} \leq V_t$ and decreases as v_{GS} is increased above V_t . It is interesting to note that although v_{GS} is used as the parameter for the set of graphs in Fig. 5.4, the graphs in fact depend only on v_{OV} (and, of course, k_n).

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**. Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

EXERCISE

- 5.1** A 0.18- μm fabrication process is specified to have $t_{ox} = 4 \text{ nm}$, $\mu_n = 450 \text{ cm}^2/\text{V}\cdot\text{s}$, and $V_t = 0.5 \text{ V}$. Find the value of the process transconductance parameter k'_n . For a MOSFET with minimum length fabricated in this process, find the required value of W so that the device exhibits a channel resistance r_{DS} of $1 \text{ k}\Omega$ at $v_{GS} = 1 \text{ V}$.

Ans. $388 \mu\text{A}/\text{V}^2$; $0.93 \mu\text{m}$

5.1.5 Operation as v_{DS} Is Increased

We next consider the situation as v_{DS} is increased. For this purpose, let v_{GS} be held constant at a value greater than V_t ; that is, let the MOSFET be operated at a constant overdrive voltage V_{OV} . Refer to Fig. 5.5, and note that v_{DS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from zero to v_{DS} . Thus the voltage between the gate and points along the channel decreases from $v_{GS} = V_t + V_{OV}$ at the source end to $v_{GD} = v_{GS} - v_{DS} = V_t + V_{OV} - v_{DS}$ at the drain end. Since the channel depth depends on this voltage, and specifically on the amount by which this voltage exceeds V_t , we find that the channel is no longer of uniform depth; rather, the channel will take the tapered shape shown in Fig. 5.5, being deepest at the source end (where the depth is proportional to V_{OV}) and shallowest at the drain end⁶ (where the depth is proportional to $V_{OV} - v_{DS}$). This point is further illustrated in Fig. 5.6.

⁶For simplicity, we do not show in Fig. 5.5 the depletion region. Physically speaking, it is the widening of the depletion region as a result of the increased v_{DS} that makes the channel shallower near the drain.

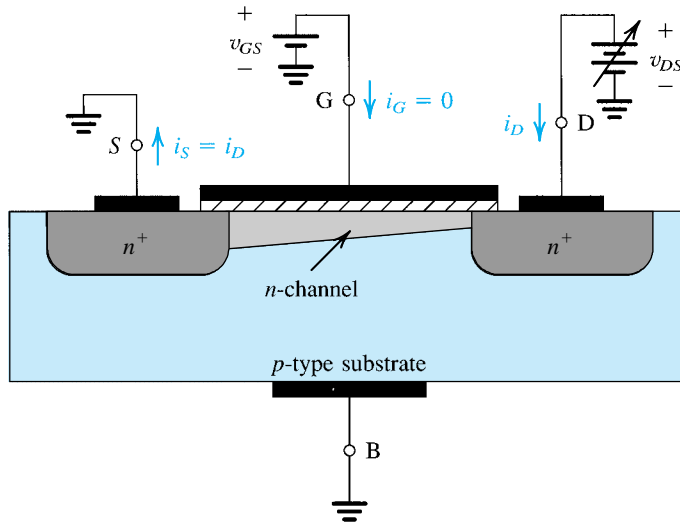


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$; $v_{GS} = V_t + V_{OV}$.

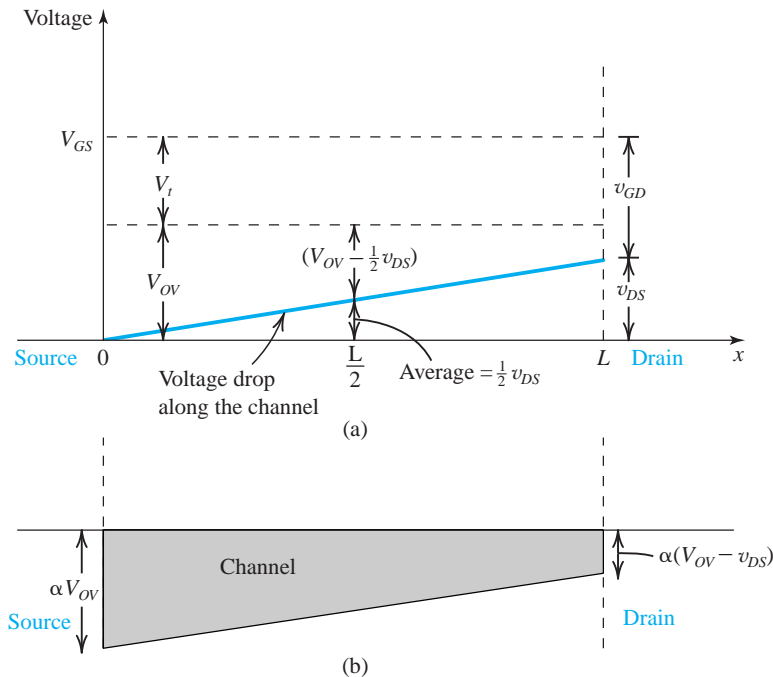


Figure 5.6 (a) For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. (b) The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV} , that at the drain end is proportional to $(V_{OV} - v_{DS})$.

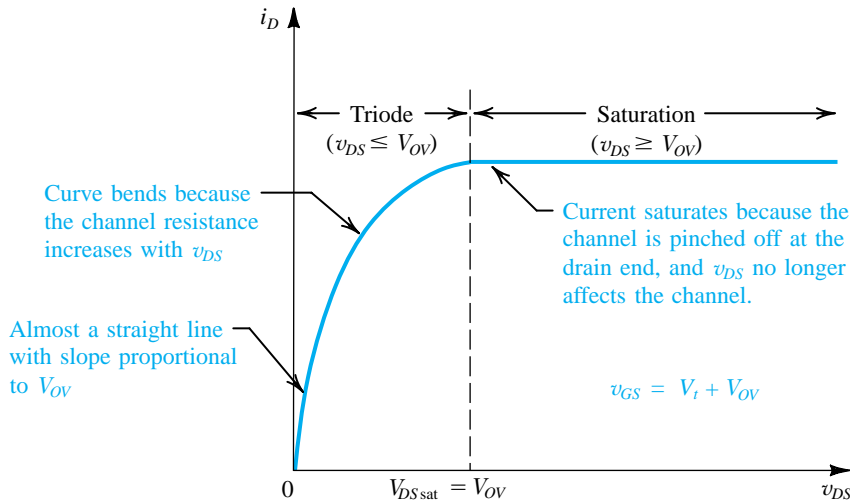


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.

As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus, the i_D - v_{DS} curve does not continue as a straight line but bends as shown in Fig. 5.7. The equation describing this portion of the i_D - v_{DS} curve can be easily derived by utilizing the information in Fig. 5.6. Specifically, note that the charge in the tapered channel is proportional to the channel cross-sectional area shown in Fig. 5.6(b). This area in turn can be easily seen as proportional to $\frac{1}{2}[V_{OV} + (V_{OV} - v_{DS})]$ or $(V_{OV} - \frac{1}{2}v_{DS})$. Thus, the relationship between i_D and v_{DS} can be found by replacing V_{OV} in Eq. (5.7) by $(V_{OV} - \frac{1}{2}v_{DS})$,

$$i_D = k'_n \left(\frac{W}{L} \right) \left(V_{OV} - \frac{1}{2}v_{DS} \right) v_{DS} \quad (5.14)$$

This relationship describes the semiparabolic portion of the i_D - v_{DS} curve in Fig. 5.7. It applies to the entire segment down to $v_{DS} = 0$. Specifically, note that as v_{DS} is reduced, we can neglect $\frac{1}{2}v_{DS}$ relative to V_{OV} in the factor in parentheses, and the expression reduces to that in Eq. (5.7). The latter of course is an approximation and applies only for small v_{DS} (i.e., near the origin).

There is another useful interpretation of the expression in Eq. (5.14). From Fig. 5.6(a) we see that the average voltage along the channel is $\frac{1}{2}v_{DS}$. Thus, the average voltage that gives rise to channel charge and hence to i_D is no longer V_{OV} but $(V_{OV} - \frac{1}{2}v_{DS})$, which is indeed the factor that appears in Eq. (5.14). Finally, we note that Eq. (5.14) is frequently written in the alternate form

$$i_D = k'_n \left(\frac{W}{L} \right) \left(V_{OV} v_{DS} - \frac{1}{2}v_{DS}^2 \right) \quad (5.15)$$

Furthermore, for an arbitrary value of V_{OV} , we can replace V_{OV} by $(v_{GS} - V_t)$ and rewrite Eq. (5.15) as

$$i_D = k'_n \left(\frac{W}{L} \right) \left[(v_{GS} - V_t) v_{DS} - \frac{1}{2}v_{DS}^2 \right] \quad (5.16)$$

5.1.6 Operation for $v_{DS} \geq V_{OV}$

The above description of operation assumed that even though the channel became tapered, it still had a finite (nonzero) depth at the drain end. This in turn is achieved by keeping v_{DS} sufficiently small that the voltage between the gate and the drain, v_{GD} , exceeds V_t . This is indeed the situation shown in Fig. 5.6(a). Note that for this situation to obtain, v_{DS} must not exceed V_{OV} , for as $v_{DS} = V_{OV}$, $v_{GD} = V_t$, and the channel depth at the drain end reduces to zero.

Figure 5.8 shows v_{DS} reaching V_{OV} and v_{GD} correspondingly reaching V_t . The zero depth of the channel at the drain end gives rise to the term **channel pinch-off**. Increasing v_{DS} beyond this value (i.e., $v_{DS} > V_{OV}$) has no effect on the channel shape and charge, and the current through the channel remains constant at the value reached for $v_{DS} = V_{OV}$. The drain current thus **saturates** at the value found by substituting $v_{DS} = V_{OV}$ in Eq. (5.14),

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) V_{OV}^2 \quad (5.17)$$

The MOSFET is then said to have entered the **saturation region** (or, equivalently, the saturation mode of operation). The voltage v_{DS} at which saturation occurs is denoted V_{DSsat} ,

$$V_{DSsat} = V_{OV} = V_{GS} - V_t \quad (5.18)$$

It should be noted that channel pinch-off does *not* mean channel blockage: Current continues to flow through the pinched-off channel, and the electrons that reach the drain end of the

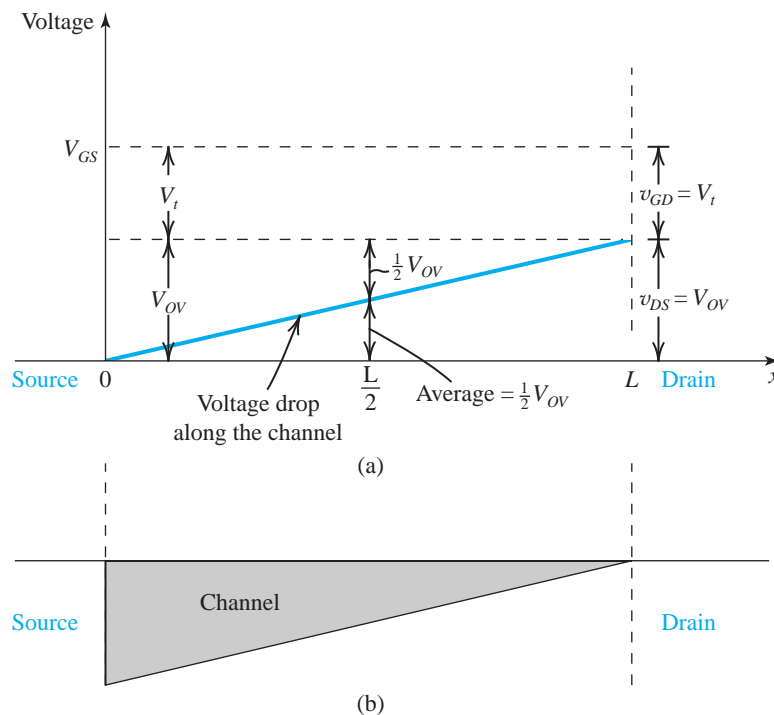


Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV} . At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{DSat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

channel are accelerated through the depletion region that exists there (not shown in Fig. 5.5) and into the drain terminal. Any increase in v_{DS} above V_{DSsat} appears as a voltage drop across the depletion region. Thus, both the current through the channel and the voltage drop across it remain constant in saturation.

The saturation portion of the $i_D - v_{DS}$ curve is, as expected, a horizontal straight line, as indicated in Fig. 5.7. Also indicated in Fig. 5.7 is the name of the region of operation obtained with a continuous (non-pinched-off) channel, the **triode region**. This name is a carryover from the days of vacuum-tube devices, whose operation a FET resembles.

Finally, we note that the $i_D - v_{DS}$ relationship in saturation can be generalized by replacing the constant overdrive voltage V_{OV} by a variable one, v_{OV} :

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2 \quad (5.19) \quad \text{!}$$

Also, v_{OV} can be replaced by $(v_{GS} - V_t)$ to obtain the alternate expression for saturation-mode i_D ,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2 \quad (5.20) \quad \text{!}$$

Example 5.1

Consider a process technology for which $L_{\min} = 0.4 \mu\text{m}$, $t_{ox} = 8 \text{ nm}$, $\mu_n = 450 \text{ cm}^2/\text{V} \cdot \text{s}$, and $V_t = 0.7 \text{ V}$.

- Find C_{ox} and k'_n .
- For a MOSFET with $W/L = 8 \mu\text{m}/0.8 \mu\text{m}$, calculate the values of V_{OV} , V_{GS} , and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100 \mu\text{A}$.
- For the device in (b), find the values of V_{OV} and V_{GS} required to cause the device to operate as a $1000\text{-}\Omega$ resistor for very small v_{DS} .

Solution

$$\begin{aligned} \text{(a)} \quad C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3} \text{ F/m}^2 \\ &= 4.32 \text{ fF}/\mu\text{m}^2 \\ k'_n &= \mu_n C_{ox} = 450 (\text{cm}^2/\text{V} \cdot \text{s}) \times 4.32 (\text{fF}/\mu\text{m}^2) \\ &= 450 \times 10^8 (\mu\text{m}^2/\text{V} \cdot \text{s}) \times 4.32 \times 10^{-15} (\text{F}/\mu\text{m}^2) \\ &= 194 \times 10^{-6} (\text{F}/\text{V} \cdot \text{s}) \\ &= 194 \mu\text{A}/\text{V}^2 \end{aligned}$$

- For operation in the saturation region,

$$i_D = \frac{1}{2} k'_n \frac{W}{L} v_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} V_{OV}^2$$

which results in

$$V_{OV} = 0.32 \text{ V}$$

Example 5.1 *continued*

Thus,

$$V_{GS} = V_t + V_{OV} = 1.02 \text{ V}$$

and

$$V_{DSmin} = V_{OV} = 0.32 \text{ V}$$

(c) For the MOSFET in the triode region with v_{DS} very small,

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} V_{OV}}$$

Thus

$$1000 = \frac{1}{194 \times 10^{-6} \times 10 \times V_{OV}}$$

which yields

$$V_{OV} = 0.52 \text{ V}$$

Thus,

$$V_{GS} = 1.22 \text{ V}$$

EXERCISES

- 5.2** For a 0.8- μm process technology for which $t_{ox} = 15 \text{ nm}$ and $\mu_n = 550 \text{ cm}^2/\text{V} \cdot \text{s}$, find C_{ox} , k'_n , and the overdrive voltage V_{OV} required to operate a transistor having $W/L = 20$ in saturation with $I_D = 0.2 \text{ mA}$. What is the minimum value of V_{DS} needed?

Ans. 2.3 fF/ μm^2 ; 127 $\mu\text{A}/\text{V}^2$; 0.40 V; 0.40 V

- D5.3** A circuit designer intending to operate a MOSFET in saturation is considering the effect of changing the device dimensions and operating voltages on the drain current I_D . Specifically, by what factor does I_D change in each of the following cases?

- (a) The channel length is doubled.
- (b) The channel width is doubled.
- (c) The overdrive voltage is doubled.
- (d) The drain-to-source voltage is doubled.
- (e) Changes (a), (b), (c), and (d) are made simultaneously.

Which of these cases might cause the MOSFET to leave the saturation region?

Ans. 0.5; 2; 4; no change; 4; case (c) if v_{DS} is smaller than $2 V_{OV}$

5.1.7 The p-Channel MOSFET

Figure 5.9(a) shows a cross-sectional view of a *p*-channel enhancement-type MOSFET. The structure is similar to that of the NMOS device except that here the substrate is *n* type and the source and the drain regions are *p*⁺ type; that is, all semiconductor regions are reversed in polarity relative to their counterparts in the NMOS case. The PMOS and NMOS transistor are said to be *complementary* devices.

To induce a channel for current flow between source and drain, a negative voltage is applied to the gate, that is, between gate and source, as indicated in Fig. 5.9(b). By increasing the magni-

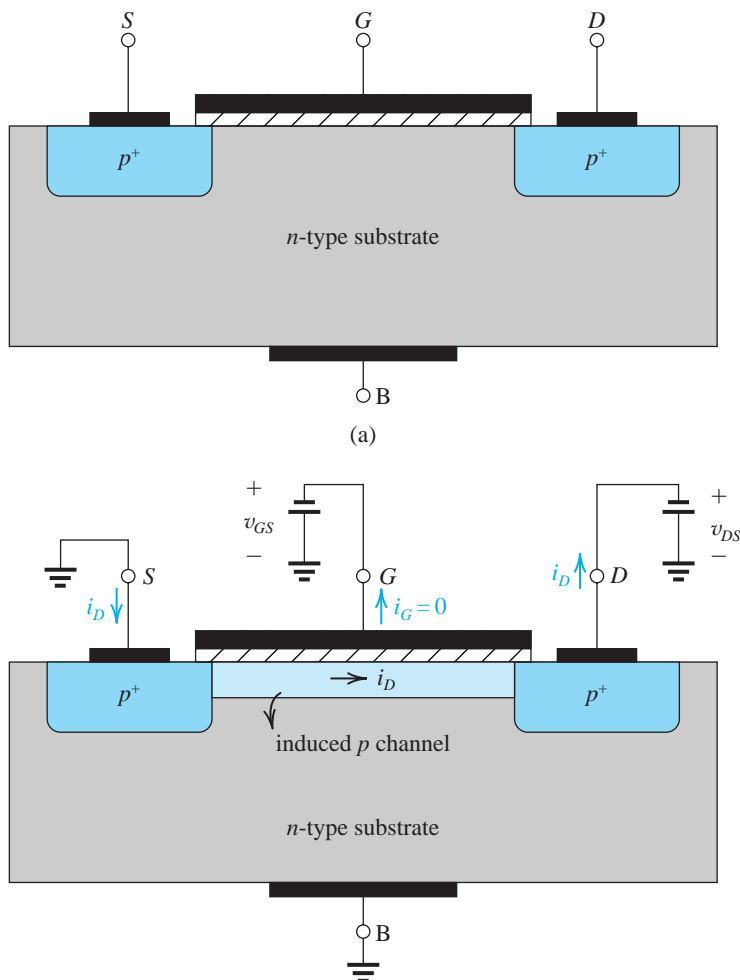


Figure 5.9 (a) Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. (b) A negative voltage v_{GS} of magnitude greater than $|V_{tp}|$ induces a p channel, and a negative v_{DS} causes a current i_D to flow from source to drain.

tude of the negative v_{GS} beyond the magnitude of the threshold voltage V_{tp} , which by convention is negative, a p channel is established as shown in Fig. 5.9(b). This condition can be described as

$$v_{GS} \leq V_{tp}$$

or, to avoid dealing with negative signs,

$$|v_{GS}| \geq |V_{tp}|$$

Now, to cause a current i_D to flow in the p channel, a negative voltage v_{DS} is applied to the drain. The current i_D is carried by holes and flows through the channel from source to drain. As we have done for the NMOS transistor, we define the process transconductance parameter for the PMOS device as

$$k'_p = \mu_p C_{ox}$$

where μ_p is the mobility of the holes in the induced p channel. Typically, $\mu_p = 0.25 \mu_n$ to $0.5 \mu_n$ and is process technology dependent. The transistor transconductance parameter k_p is obtained by multiplying k'_p by the aspect ratio W/L ,

$$k_p = k'_p(W/L)$$

The remainder of the description of the physical operation of the p -channel MOSFET follows that for the NMOS device, except of course for the sign reversals of all voltages. We will present the complete current–voltage characteristics of both NMOS and PMOS transistors in the next section.

PMOS technology originally dominated MOS integrated-circuit manufacturing, and the original microprocessors utilized PMOS transistors. As the technological difficulties of fabricating NMOS transistors were solved, NMOS completely supplanted PMOS. The main reason for this change is that electron mobility μ_n is higher by a factor of 2 to 4 than the hole mobility μ_p , resulting in NMOS transistors having greater gains and speeds of operation than PMOS devices. Subsequently, a technology was developed that permits the fabrication of both NMOS and PMOS transistors on the same chip. Appropriately called **complementary MOS**, or **CMOS**, this technology is currently the dominant electronics technology.

5.1.8 Complementary MOS or CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit configurations. Indeed, at the present time CMOS is the most widely used of all the IC technologies. This statement applies to both analog and digital circuits. CMOS technology has virtually replaced designs based on NMOS transistors alone. Furthermore, by 2009 CMOS technology had taken over many applications that just a few years earlier were possible only with bipolar devices. Throughout this book, we will study many CMOS circuit techniques.

Figure 5.10 shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the p -type substrate, the PMOS transistor is fabricated in a specially created n region, known as an **n well**. The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connections made to the p -type body and to the n well. The latter connection serves as the body terminal for the PMOS transistor.

5.1.9 Operating the MOS Transistor in the Subthreshold Region

The above description of the n -channel MOSFET operation implies that for $v_{GS} < V_t$, no current flows and the device is cut off. This is not entirely true, for it has been found that for values of v_{GS} smaller than but close to V_t , a small drain current flows. In this **subthreshold region** of operation, the drain current is exponentially related to v_{GS} , much like the i_C – v_{BE} relationship of a BJT, as will be shown in the next chapter.

Although in most applications the MOS transistor is operated with $v_{GS} > V_t$, there are special, but a growing number of, applications that make use of subthreshold operation. In Chapter 13, we will briefly consider subthreshold operation.

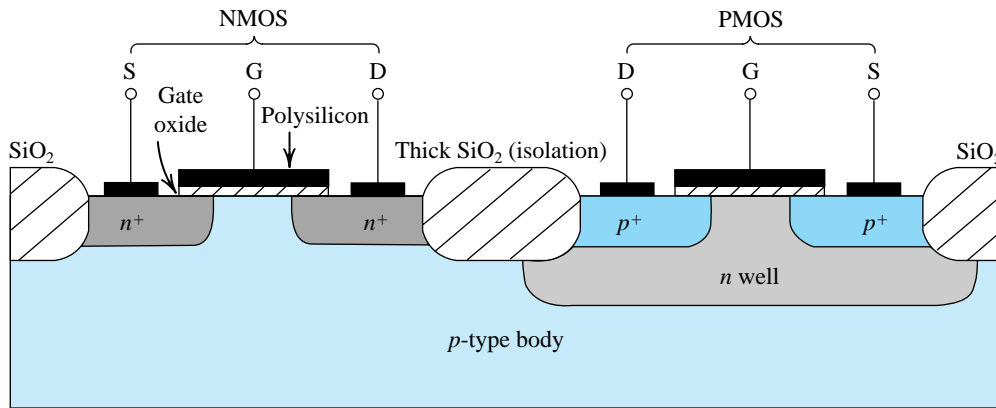


Figure 5.10 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate n -type region, known as an n well. Another arrangement is also possible in which an n -type body is used and the n device is formed in a p well. Not shown are the connections made to the p -type body and to the n well; the latter functions as the body terminal for the p -channel device.

5.2 Current–Voltage Characteristics

Building on the physical foundation established in the previous section for the operation of the enhancement MOS transistor, in this section we present its complete current–voltage characteristics. These characteristics can be measured at dc or at low frequencies and thus are called static characteristics. The dynamic effects that limit the operation of the MOSFET at high frequencies and high switching speeds will be discussed in Chapter 9.

5.2.1 Circuit Symbol

Figure 5.11(a) shows the circuit symbol for the n -channel enhancement-type MOSFET. Observe that the spacing between the two vertical lines that represent the gate and the channel indicates the fact that the gate electrode is insulated from the body of the device. The polarity of the p -type substrate (body) and the n channel is indicated by the arrowhead on the

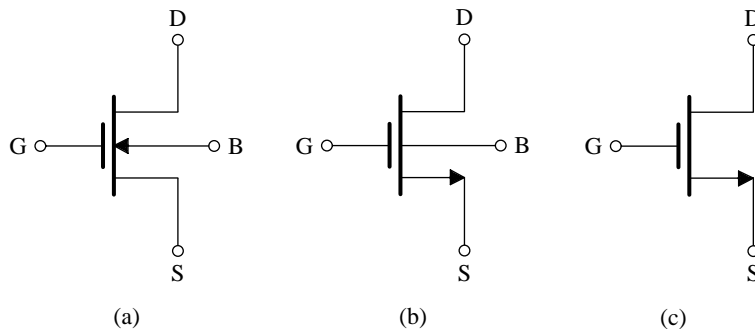


Figure 5.11 (a) Circuit symbol for the n -channel enhancement-type MOSFET. (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., n channel). (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

line representing the body (B). This arrowhead also indicates the polarity of the transistor, namely, that it is an n -channel device.

Although the MOSFET is a symmetrical device, it is often useful in circuit design to designate one terminal as the source and the other as the drain (without having to write S and D beside the terminals). This objective is achieved in the modified circuit symbol shown in Fig. 5.11(b). Here an arrowhead is placed on the source terminal, thus distinguishing it from the drain terminal. The arrowhead points in the normal direction of current flow and thus indicates the polarity of the device (i.e., n channel). Observe that in the modified symbol, there is no need to show the arrowhead on the body line. Although the circuit symbol of Fig. 5.11(b) clearly distinguishes the source from the drain, in practice it is the polarity of the voltage impressed across the device that determines source and drain; *the drain is always positive relative to the source in an n -channel FET.*

In applications where the source is connected to the body of the device, a further simplification of the circuit symbol is possible, as indicated in Fig. 5.11(c). This symbol is also used in applications when the effect of the body on circuit operation is not important, as will be seen later.

5.2.2 The i_D - v_{DS} Characteristics

Table 5.1 provides a compilation of the conditions and the formulas for the operation of the NMOS transistor in each of the three possible regions: the cutoff region, the triode region, and the saturation region. The first two are useful if the MOSFET is to be utilized as a switch. On the other hand, if the MOSFET is to be used to design an amplifier, it must be operated in the saturation region. The rationale for these choices will be addressed in Section 5.4.

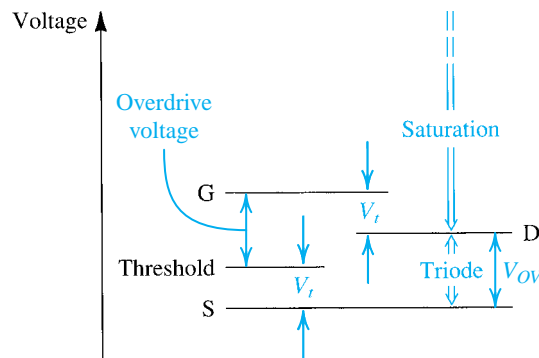
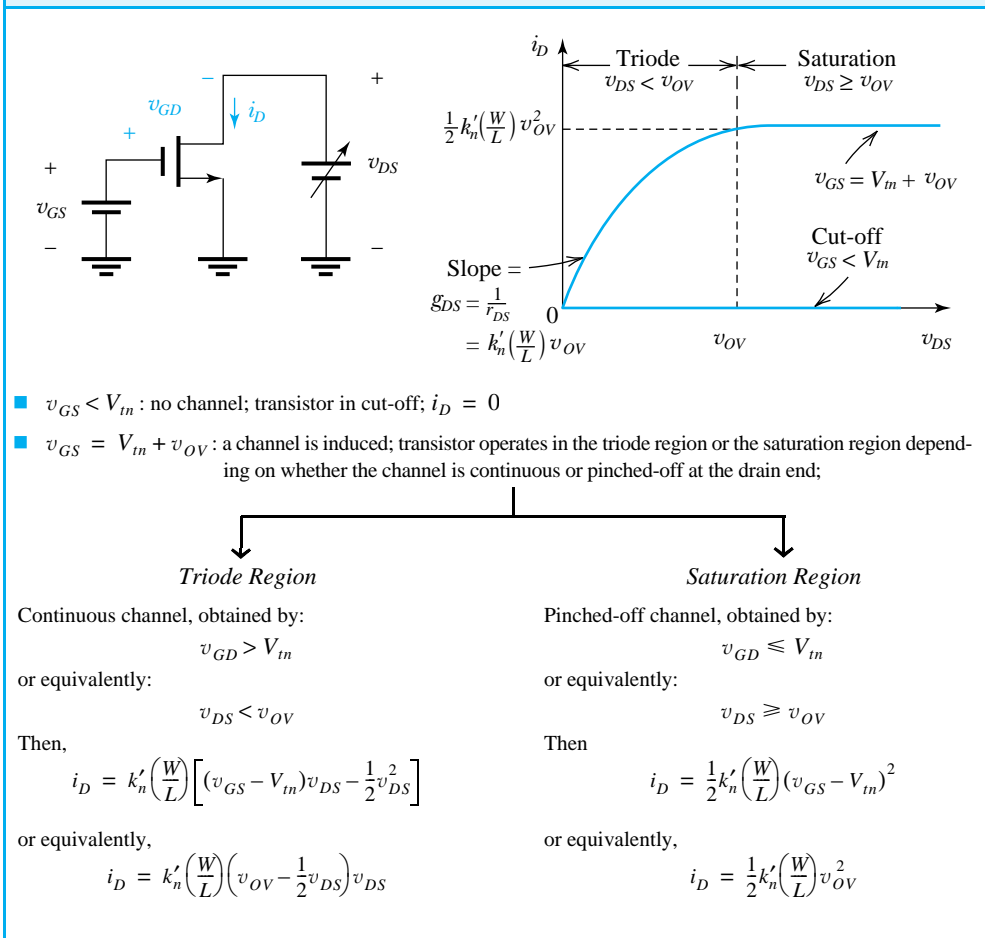
At the top of Table 5.1 we show a circuit consisting of an NMOS transistor and two dc supplies providing v_{GS} and v_{DS} . This conceptual circuit can be used to measure the i_D - v_{DS} characteristic curves of the NMOS transistor. Each curve is measured by setting v_{GS} to a desired constant value, varying v_{DS} , and measuring the corresponding i_D . Two of these characteristic curves are shown in the accompanying diagram: one for $v_{GS} < V_{in}$ and the other for $v_{GS} = V_{in} + v_{OV}$. (Note that we now use V_{in} to denote the threshold voltage of the NMOS transistor, to distinguish it from that of the PMOS transistor, denoted V_{ip} .)

As Table 5.1 shows, the boundary between the triode region and the saturation region is determined by whether v_{DS} is less or greater than the overdrive voltage v_{OV} at which the transistor is operating. An equivalent way to check for the region of operation is to examine the relative values of the drain and gate voltages. To operate in the triode region, the gate voltage must exceed the drain voltage by at least V_{in} volts, which ensures that the channel remains continuous (not pinched off). On the other hand, to operate in saturation, the channel must be pinched off at the drain end; pinch-off is achieved here by keeping v_D higher than $v_G - V_{in}$, that is, not allowing v_D to fall below v_G by more than V_{in} volts. The graphical construction of Fig. 5.12 should serve to remind the reader of these conditions.

A set of i_D - v_{DS} characteristics for the NMOS transistor is shown in Fig. 5.13. Observe that each graph is obtained by setting v_{GS} above V_{in} by a specific value of overdrive voltage, denoted V_{OV1} , V_{OV2} , V_{OV3} , and V_{OV4} . This in turn is the value of v_{DS} at which the corresponding graph saturates, and the value of the resulting saturation current is directly determined by the value of v_{OV} , namely, $\frac{1}{2}k'_n V_{OV1}^2$, $\frac{1}{2}k'_n V_{OV2}^2$, \dots . The reader is advised to commit to memory both the structure of these graphs and the coordinates of the saturation points.

Finally, observe that the boundary between the triode and the saturation regions, that is, the locus of the saturation points, is a parabolic curve described by

$$i_D = \frac{1}{2}k'_n \left(\frac{W}{L}\right)v_{DS}^2$$

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor**Figure 5.12** The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

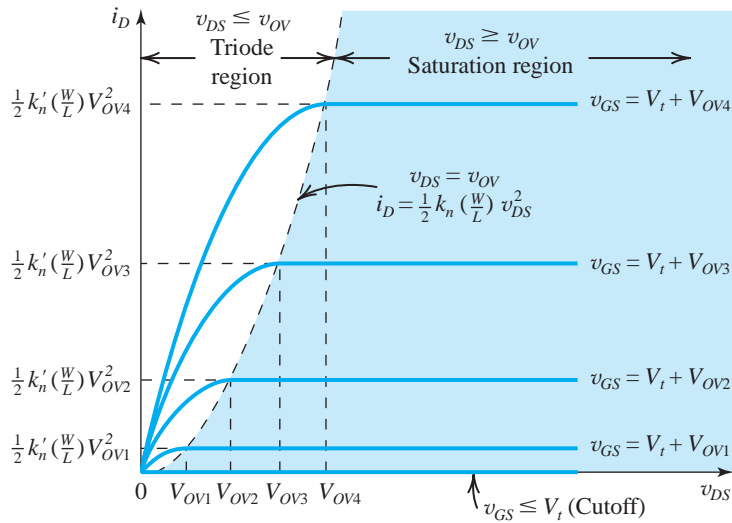


Figure 5.13 The i_D - v_{DS} characteristics for an enhancement-type NMOS transistor.

5.2.3 The i_D - v_{GS} Characteristic

When the MOSFET is used to design an amplifier, it is operated in the saturation region. As Fig. 5.13 indicates, in saturation the drain current is constant determined by v_{GS} (or v_{OV}) and is independent of v_{DS} . That is, the MOSFET operates as a constant-current source where the value of the current is determined by v_{GS} . In effect, then, the MOSFET operates as a voltage-controlled current source with the control relationship described by

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 \quad (5.21)$$

or in terms of v_{OV} ,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2 \quad (5.22)$$

This is the relationship that underlies the application of the MOSFET as an amplifier. That it is nonlinear should be of concern to those interested in designing linear amplifiers. Nevertheless, later in this chapter, we will see how one can obtain linear amplification from this nonlinear control or transfer characteristic.

Figure 5.14 shows the i_D - v_{GS} characteristic of an NMOS transistor operating in saturation. Note that if we are interested in a plot of i_D versus v_{OV} , we simply shift the origin to the point $v_{GS} = V_{tn}$.

The view of the MOSFET in the saturation region as a voltage-controlled current source is illustrated by the equivalent-circuit representation shown in Fig. 5.15. For reasons that will become apparent shortly, the circuit in Fig. 5.15 is known as a **large-signal equivalent circuit**. Note that the current source is ideal, with an infinite output resistance representing the independence, in saturation, of i_D from v_{DS} . This, of course, has been assumed in the idealized model of device operation utilized thus far. We are about to rectify an important shortcoming of this model. First, however, we present an example.

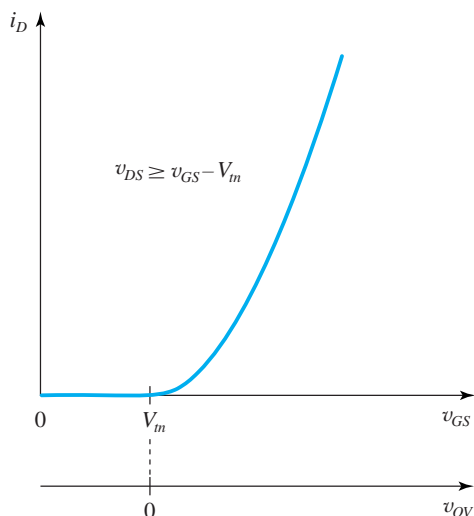


Figure 5.14 The i_D - v_{GS} characteristic of an NMOS transistor operating in the saturation region. The i_D - v_{OV} characteristic can be obtained by simply re-labelling the horizontal axis; that is, shifting the origin to the point $v_{GS} = V_m$.

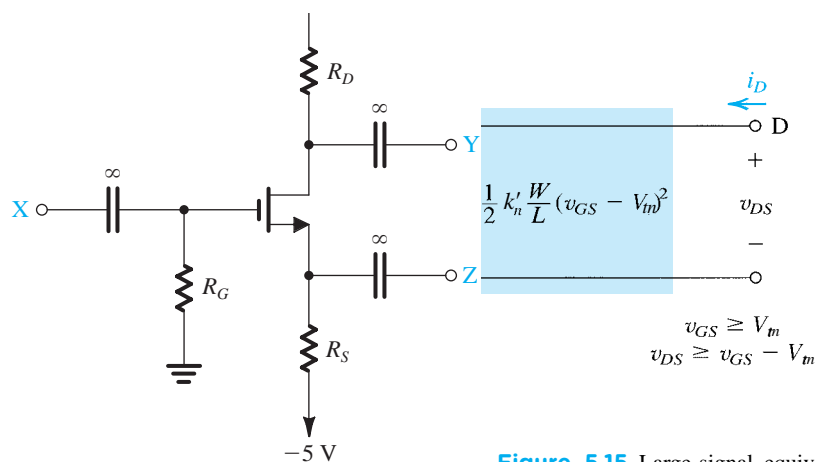


Figure 5.15 Large-signal equivalent-circuit model of an n -channel MOSFET operating in the saturation

Example 5.2

Consider an NMOS transistor fabricated in a $0.18\text{-}\mu\text{m}$ process with $L = 0.18\text{ }\mu\text{m}$ and $W = 2\text{ }\mu\text{m}$. The process technology is specified to have $C_{ox} = 8.6\text{ fF}/\mu\text{m}^2$, $\mu_n = 450\text{ cm}^2/\text{V}\cdot\text{s}$, and $V_m = 0.5\text{ V}$.

- Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100\text{ }\mu\text{A}$.
- If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50\text{ }\mu\text{A}$.
- To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3\text{ V}$. Find the change in i_D resulting from v_{GS} changing from 0.7 V by $+0.01\text{ V}$ and by -0.01 V .

Solution

First we determine the process transconductance parameter k'_n

$$\begin{aligned} k'_n &= \mu_n C_{ox} \\ &= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12} \text{ A/V}^2 \\ &= 387 \text{ } \mu\text{A/V}^2 \end{aligned}$$

and the transistor transconductance parameter k_n ,

$$\begin{aligned} k_n &= k'_n \left(\frac{W}{L} \right) \\ &= 387 \left(\frac{2}{0.18} \right) = 4.3 \text{ mA/V}^2 \end{aligned}$$

(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22 \text{ V}$$

Thus,

$$V_{GS} = V_{in} + V_{OV} = 0.5 + 0.22 = 0.72 \text{ V}$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22 \text{ V}$$

(b) With V_{GS} kept constant at 0.72 V and I_D reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

$$\begin{aligned} I_D &= k_n \left[V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ 50 &= 4.3 \times 10^3 \left[0.22 V_{DS} - \frac{1}{2} V_{DS}^2 \right] \end{aligned}$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44 V_{DS} + 0.023 = 0$$

This quadratic equation has two solutions

$$V_{DS} = 0.06 \text{ V} \quad \text{and} \quad V_{DS} = 0.39 \text{ V}$$

The second answer is greater than V_{OV} and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06 \text{ V}$$

Example 5.2 *continued*

(c) For $v_{GS} = 0.7$ V, $V_{OV} = 0.2$ V, and since $V_{DS} = 0.3$ V, the transistor is operating in saturation and

$$\begin{aligned} I_D &= \frac{1}{2} k_n V_{OV}^2 \\ &= \frac{1}{2} \times 4300 \times 0.04 \\ &= 86 \mu\text{A} \end{aligned}$$

Now for $v_{GS} = 0.710$ V, $v_{OV} = 0.21$ V and

$$i_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8 \mu\text{A}$$

and for $v_{GS} = 0.690$ V, $v_{OV} = 0.19$ V, and

$$i_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6 \mu\text{A}$$

Thus, with $\Delta V_{GS} = +0.01$ V, $\Delta i_D = 8.8 \mu\text{A}$; and for $\Delta V_{GS} = -0.01$ V, $\Delta i_D = -8.4 \mu\text{A}$.

We conclude that the two changes are almost equal, an indication of almost-linear operation when the changes in v_{GS} are kept small. This is just a preview of the “small-signal operation” of the MOSFET studied in Sections 5.4 and 5.5.

EXERCISES

- 5.4** An NMOS transistor is operating at the edge of saturation with an overdrive voltage V_{OV} and a drain current I_D . If V_{OV} is doubled, and we must maintain operation at the edge of saturation, what should V_{DS} be changed to? What value of drain current results?

Ans. $2 V_{OV}$; $4 I_D$

- 5.5** An n -channel MOSFET operating with $V_{OV} = 0.5$ V exhibits a linear resistance $r_{DS} = 1$ k Ω when v_{DS} is very small. What is the value of the device transconductance parameter k_n ? What is the value of the current I_D obtained when v_{DS} is increased to 0.5 V? and to 1 V?

Ans. 2 mA/V²; 0.25 mA; 0.25 mA

5.2.4 Finite Output Resistance in Saturation

Equation (5.21) and the corresponding large-signal equivalent circuit in Fig. 5.15, as well as the graphs in Fig. 5.13, indicate that in saturation, i_D is independent of v_{DS} . Thus, a change Δv_{DS} in the drain-to-source voltage causes a zero change in i_D , which implies that the incremental resistance looking into the drain of a saturated MOSFET is infinite. This, however, is an idealization based on the premise that once the channel is pinched off at the drain end, further increases in v_{DS} have no effect on the channel's shape. But, in practice, increasing v_{DS} beyond v_{OV} does affect the channel somewhat. Specifically, as v_{DS} is increased, the channel pinch-off point is moved slightly away from the drain, toward the source. This is illustrated in Fig. 5.16, from which we note that the voltage across the channel remains constant at v_{OV} , and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain. Note, however, that (with depletion-layer widening) the channel

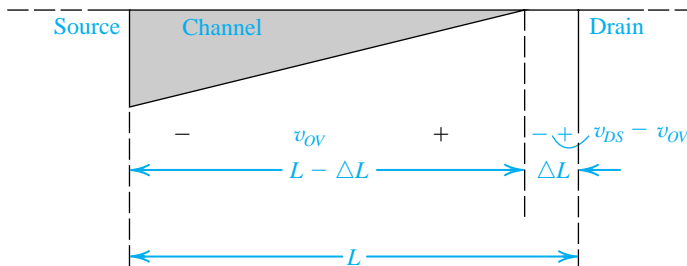


Figure 5.16 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

length is in effect reduced, from L to $L - \Delta L$, a phenomenon known as **channel-length modulation**. Now, since i_D is inversely proportional to the channel length (Eq. 5.21), i_D increases with v_{DS} .

This effect can be accounted for in the expression for i_D by including a factor $1 + \lambda(v_{DS} - v_{OV})$ or, for simplicity, $(1 + \lambda v_{DS})$,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{in})^2 (1 + \lambda v_{DS}) \quad (5.23)$$

Here λ is a device parameter having the units of reciprocal volts (V^{-1}). The value of λ depends both on the process technology used to fabricate the device and on the channel length L that the circuit designer selects. Specifically, the value of λ is much larger for newer submicron technologies than for older technologies. This makes intuitive sense: Newer technologies have very short channels, and are thus much greatly impacted by the channel-length modulation effect. Also, for a given process technology, λ is inversely proportional to L .

A typical set of i_D - v_{DS} characteristics showing the effect of channel-length modulation is displayed in Fig. 5.17. The observed linear dependence of i_D on v_{DS} in the saturation region is represented in Eq. (5.23) by the factor $(1 + \lambda v_{DS})$. From Fig. 5.17 we observe that when the straight-line i_D - v_{DS} characteristics are extrapolated, they intercept the v_{DS} axis at the point, $v_{DS} = -V_A$, where V_A is a positive voltage. Equation (5.23), however, indicates that $i_D = 0$ at $v_{DS} = -1/\lambda$. It follows that

$$V_A = \frac{1}{\lambda}$$

and thus V_A is a device parameter with the dimensions of V. For a given process, V_A is proportional to the channel length L that the designer selects for a MOSFET. We can isolate the dependence of V_A on L by expressing it as

$$V_A = V'_A L$$

where V'_A is entirely process-technology dependent with the dimensions of volts per micron. Typically, V'_A falls in the range of 5 V/ μm to 50 V/ μm . The voltage V_A is usually referred to as the Early voltage, after J. M. Early, who discovered a similar phenomenon for the BJT (Chapter 6).

Equation (5.23) indicates that when channel-length modulation is taken into account, the saturation values of i_D depend on v_{DS} . Thus, for a given v_{GS} , a change Δv_{DS} yields a corresponding change Δi_D in the drain current i_D . It follows that the output resistance of the current source representing i_D in saturation is no longer infinite. Defining the output resistance r_o as⁷

⁷In this book we use r_o to denote the output resistance in saturation, and r_{DS} to denote the drain-to-source resistance in the triode region, for small v_{DS} .

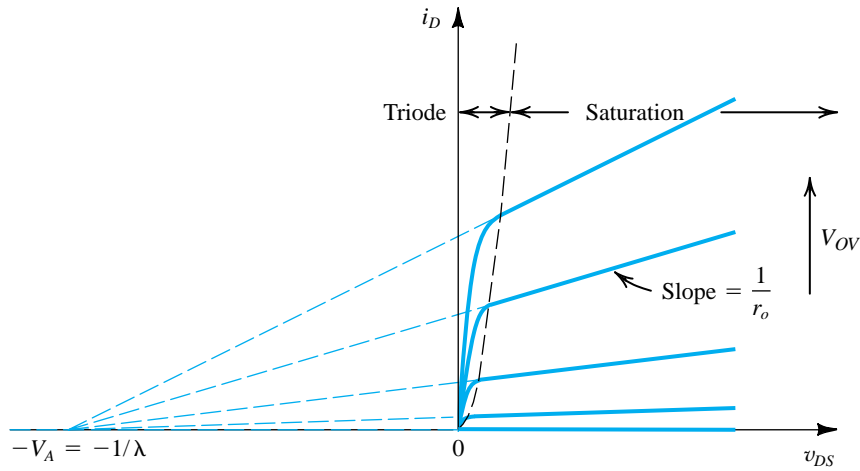


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L .

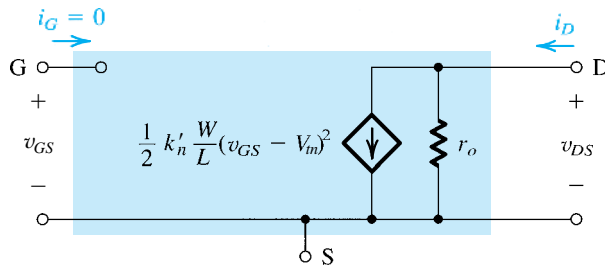


Figure 5.18 Large-signal equivalent circuit model of the n -channel MOSFET in saturation, incorporating the output resistance r_o . The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.23).

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}} \right]_{v_{GS} \text{ constant}}^{-1} \quad (5.24)$$

and using Eq. (5.23) results in

$$r_o = \left[\lambda \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_{tn})^2 \right]^{-1} \quad (5.25)$$

which can be written as

$$r_o = \frac{1}{\lambda I_D} \quad (5.26)$$

or, equivalently,

$$r_o = \frac{V_A}{I_D} \quad (5.27) \quad \text{!}$$

where I_D is the drain current *without* channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{tn})^2 \quad (5.27')$$

Thus the output resistance is inversely proportional to the drain current. Finally, we show in Fig. 5.18 the large-signal, equivalent-circuit model incorporating r_o .

EXERCISE

- 5.6** An NMOS transistor is fabricated in a $0.4\text{-}\mu\text{m}$ process having $\mu_n C_{ox} = 200\text{ }\mu\text{A/V}^2$ and $V_A' = 50\text{ V}/\mu\text{m}$ of channel length. If $L = 0.8\text{ }\mu\text{m}$ and $W = 16\text{ }\mu\text{m}$, find V_A and λ . Find the value of I_D that results when the device is operated with an overdrive voltage $V_{OV} = 0.5\text{ V}$ and $V_{DS} = 1\text{ V}$. Also, find the value of r_o at this operating point. If V_{DS} is increased by 2 V , what is the corresponding change in I_D ?

Ans. 40 V ; 0.025 V^{-1} ; 0.51 mA ; $80\text{ k}\Omega$; 0.025 mA

5.2.5 Characteristics of the p -Channel MOSFET

The circuit symbol for the p -channel enhancement-type MOSFET is shown in Fig. 5.19(a). Figure 5.19(b) shows a modified circuit symbol in which an arrowhead pointing in the normal direction of current flow is included on the source terminal. For the case where the source is connected to the substrate, the simplified symbol of Fig. 5.19(c) is usually used.

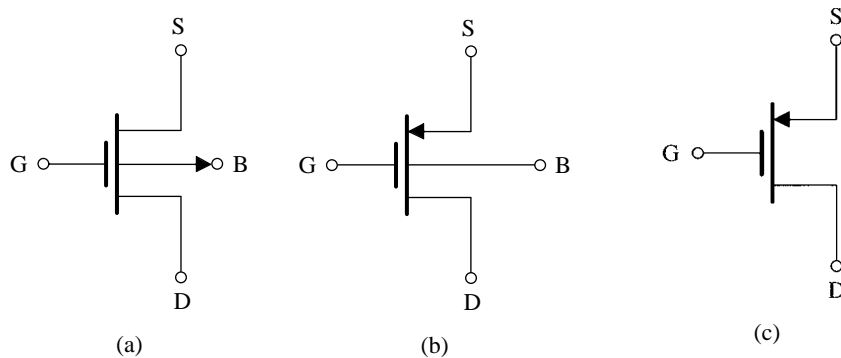


Figure 5.19 (a) Circuit symbol for the p -channel enhancement-type MOSFET. (b) Modified symbol with an arrowhead on the source lead. (c) Simplified circuit symbol for the case where the source is connected to the body.

The regions of operation of the PMOS transistor and the corresponding conditions and expression for i_D are shown in Table 5.2. Observe that the equations are written in a way that emphasizes physical intuition and avoids the confusion of negative signs. Thus while V_{tp} is by convention negative, we use $|V_{tp}|$, and the voltages v_{SG} and v_{SD} are positive. Also, in all of our circuit diagrams we will always draw p -channel devices with their sources on top so that current flows from top to bottom. Finally, we note that PMOS devices also suffer from the channel-length modulation effect. This can be taken into account by including a factor $(1 + |\lambda|v_{SD})$ in the saturation-region expression for i_D as follows

$$i_D = \frac{1}{2}k_p' \left(\frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2 (1 + |\lambda|v_{SD}) \quad (5.28)$$

or equivalently

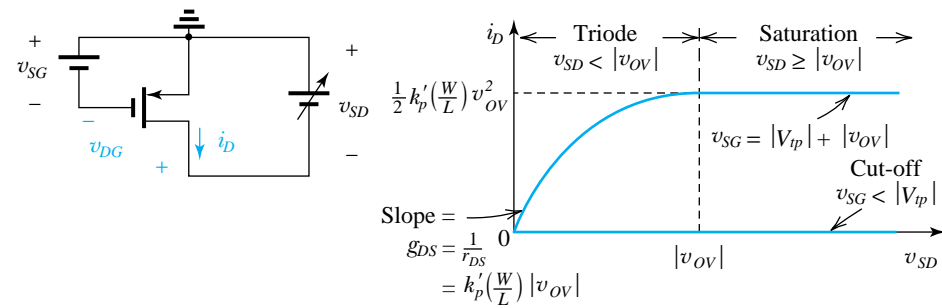
$$i_D = \frac{1}{2} k_p' \left(\frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2 \left(1 + \frac{v_{SD}}{|V_A|} \right) \quad (5.29)$$

where λ and V_A (the Early voltage for the PMOS transistor) are by convention negative quantities, hence we use $|\lambda|$ and $|V_A|$.

Finally, we should note that for a given CMOS fabrication process λ_n and $|\lambda_p|$ are generally not equal, and similarly for V_{An} and $|V_{Ap}|$.

To recap, to turn a PMOS transistor on, the gate voltage has to be made lower than that of the source by at least $|V_{tp}|$. To operate in the triode region, the drain voltage has to exceed that of the gate by at least $|V_{tp}|$; otherwise, the PMOS operates in saturation. Finally, Fig. 5.20 provides a pictorial representation of these operating conditions.

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor



- $v_{SG} < |V_{tp}|$: no channel; transistor in cut-off; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region	Saturation Region
Continuous channel, obtained by: $v_{DG} > V_{tp} $	Pinched-off channel, obtained by: $v_{DG} \leq V_{tp} $
or equivalently: $v_{SD} < v_{OV} $	or equivalently $v_{SD} \geq v_{OV} $
Then, $i_D = k_p' \left(\frac{W}{L} \right) \left[(v_{SG} - V_{tp}) v_{SD} - \frac{1}{2} v_{SD}^2 \right]$	Then $i_D = \frac{1}{2} k_p' \left(\frac{W}{L} \right) (v_{SG} - V_{tp})^2$
or equivalently $i_D = k_p' \left(\frac{W}{L} \right) \left(v_{OV} - \frac{1}{2} v_{SD} \right) v_{SD}$	or equivalently $i_D = \frac{1}{2} k_p' \left(\frac{W}{L} \right) v_{OV}^2$

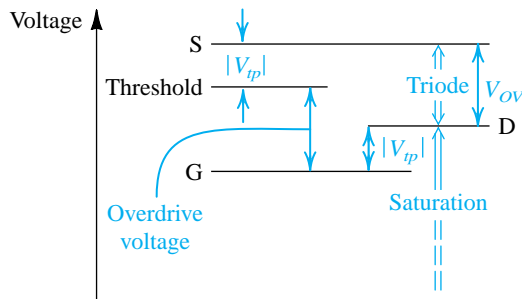


Figure 5.20 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

EXERCISE

- 5.7** The PMOS transistor shown in Fig. E5.7 has $V_{tp} = -1$ V, $k_p' = 60 \mu\text{A}/\text{V}^2$, and $W/L = 10$.
- Find the range of V_G for which the transistor conducts.
 - In terms of V_G , find the range of V_D for which the transistor operates in the triode region.
 - In terms of V_G , find the range of V_D for which the transistor operates in saturation.
 - Neglecting channel-length modulation (i.e., assuming $\lambda = 0$), find the values of $|V_{OV}|$ and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with $I_D = 75 \mu\text{A}$.
 - If $\lambda = -0.02 \text{ V}^{-1}$, find the value of r_o corresponding to the overdrive voltage determined in (d).
 - For $\lambda = -0.02 \text{ V}^{-1}$ and for the value of V_{OV} determined in (d), find I_D at $V_D = +3$ V and at $V_D = 0$ V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).

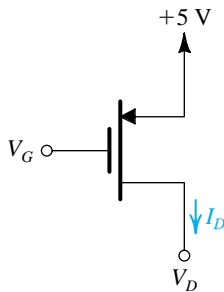


Figure E5.7

Ans. (a) $V_G \leq +4$ V; (b) $V_D \geq V_G + 1$; (c) $V_D \leq V_G + 1$; (d) 0.5 V, 3.5 V, ≤ 4.5 V; (e) $0.67 \text{ M}\Omega$; (f) $78 \mu\text{A}$, $82.5 \mu\text{A}$, $0.67 \text{ M}\Omega$ (same)

5.3 MOSFET Circuits at DC

Having studied the current–voltage characteristics of MOSFETs, we now consider circuits in which only dc voltages and currents are of concern. Specifically, we shall present a series of design and analysis examples of MOSFET circuits at dc. The objective is to instill in the reader a familiarity with the device and the ability to perform MOSFET circuit analysis both rapidly and effectively.

In the following examples, to keep matters simple and thus focus attention on the essence of MOSFET circuit operation, we will generally neglect channel-length modulation; that is, we will assume $\lambda = 0$. We will find it convenient to work in terms of the overdrive voltage; $V_{OV} = V_{GS} - V_{tn}$ for NMOS and $|V_{OV}| = V_{SG} - |V_{tp}|$ for PMOS.

Example 5.3

Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S , so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100$ $\mu\text{A}/\text{V}^2$, $L = 1$ μm , and $W = 32$ μm . Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

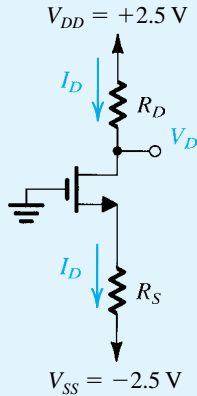


Figure 5.21 Circuit for Example 5.3.

Solution

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega \end{aligned}$$

To determine the value required for R_S , we need to know the voltage at the source, which can be easily found if we know V_{GS} . This in turn can be determined from V_{OV} . Toward that end, we note that since $V_D = 0.5$ V is greater than V_G , the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of i_D to determine the required value of V_{OV} ,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

Then substituting $I_D = 0.4$ mA = 400 μA , $\mu_n C_{ox} = 100$ $\mu\text{A}/\text{V}^2$, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 5.21, we note that the gate is at ground potential. Thus, the source must be at -1.2 V, and the required value of R_S can be determined from

$$\begin{aligned} R_S &= \frac{V_S - V_{SS}}{I_D} \\ &= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega \end{aligned}$$

EXERCISE

D5.8 Redesign the circuit of Fig. 5.21 for the following case: $V_{DD} = -V_{SS} = 2.5$ V, $V_t = 1$ V, $\mu_n C_{ox} = 60$ $\mu\text{A}/\text{V}^2$, $W/L = 120$ $\mu\text{m}/3$ μm , $I_D = 0.3$ mA, and $V_D = +0.4$ V.

Ans. $R_D = 7$ k Ω ; $R_S = 3.3$ k Ω

Example 5.4

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the $i-v$ relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k'_n(W/L)$ and V_{tn} . Neglect channel-length modulation (i.e., $\lambda = 0$). Note that this two-terminal device is known as a **diode-connected transistor**.

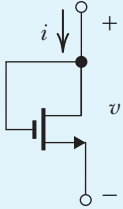


Figure 5.22

Solution

Since $v_D = v_G$ implies operation in the saturation mode,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

Now, $i = i_D$ and $v = v_{GS}$, thus

$$i = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v - V_{tn})^2$$

Replacing $k'_n \left(\frac{W}{L} \right)$ by k_n results in

$$i = \frac{1}{2} k_n (v - V_{tn})^2$$

EXERCISES

D5.9 For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.8$ V. The MOSFET has $V_{in} = 0.5$ V, $\mu_n C_{ox} = 0.4$ mA/V², $W/L = \frac{0.72 \mu\text{m}}{0.18 \mu\text{m}}$, and $\lambda = 0$.

Ans. 13.9 k Ω

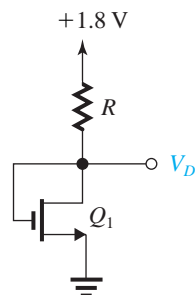


Figure E5.9

D5.10 Figure E5.10, shows a circuit obtained by augmenting the circuit of Fig. E5.9 considered in Exercise 5.9 with a transistor Q_2 identical to Q_1 and a resistance R_2 . Find the value of R_2 that results in Q_2 operating at the edge of the saturation region. Use your solution to Exercise 5.9.

Ans. 20.8 k Ω

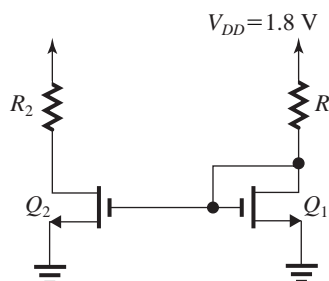


Figure E5.10

Example 5.5

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{in} = 1$ V and $k'_n(W/L) = 1$ mA/V².

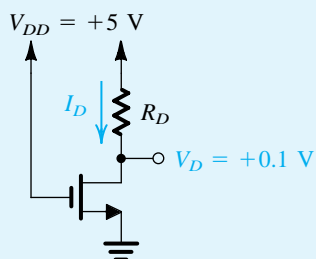


Figure 5.23 Circuit for Example 5.5.

Example 5.5 *continued***Solution**

Since the drain voltage is lower than the gate voltage by 4.9 V and $V_{tn} = 1$ V, the MOSFET is operating in the triode region. Thus the current I_D is given by

$$\begin{aligned} I_D &= k'_n \frac{W}{L} \left[(V_{GS} - V_{tn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ I_D &= 1 \times \left[(5 - 1) \times 0.1 - \frac{1}{2} \times 0.01 \right] \\ &= 0.395 \text{ mA} \end{aligned}$$

The required value for R_D can be found as follows:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega \end{aligned}$$

In a practical discrete-circuit design problem, one selects the closest standard value available for, say, 5% resistors—in this case, 12 k Ω ; see Appendix G. Since the transistor is operating in the triode region with a small V_{DS} , the effective drain-to-source resistance can be determined as follows:

$$\begin{aligned} r_{DS} &= \frac{V_{DS}}{I_D} \\ &= \frac{0.1}{0.395} = 253 \text{ }\Omega \end{aligned}$$

EXERCISE

5.11 If in the circuit of Example 5.5 the value of R_D is doubled, find approximate values for I_D and V_D .

Ans. 0.2 mA; 0.05 V

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k'_n(W/L) = 1$ mA/V². Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

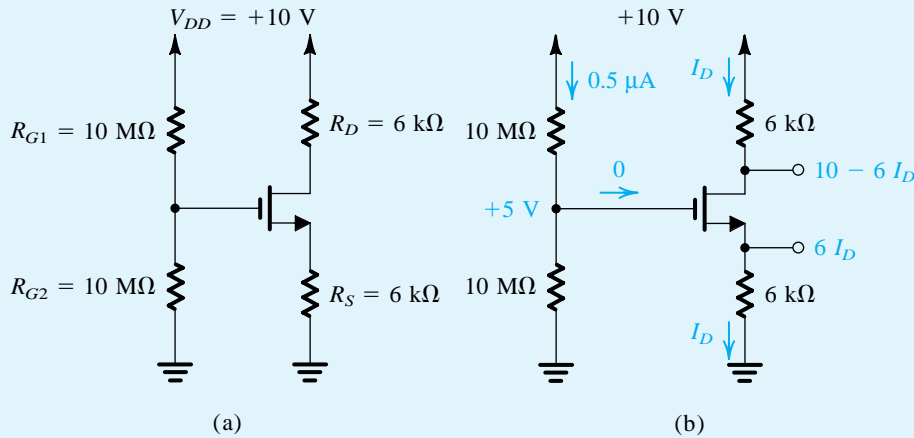


Figure 5.24 (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown.

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two $10\text{-M}\Omega$ resistors,

$$V_G = V_{DD} \frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5\text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is $I_D (\text{mA}) \times 6 (\text{k}\Omega) = 6I_D$, we have

$$V_{GS} = 5 - 6I_D$$

Thus, I_D is given by

$$\begin{aligned} I_D &= \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{tn})^2 \\ &= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2 \end{aligned}$$

which results in the following quadratic equation in I_D :

$$18I_D^2 - 25I_D + 8 = 0$$

Example 5.6 *continued*

This equation yields two values for I_D : 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$ V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_{in}$, the transistor is operating in saturation, as initially assumed.

EXERCISES

- 5.12** For the circuit of Fig. 5.24, what is the largest value that R_D can have while the transistor remains in the saturation mode?

Ans. 12 k Ω

- D5.13** Redesign the circuit of Fig. 5.24 for the following requirements: $V_{DD} = +5$ V, $I_D = 0.32$ mA, $V_S = 1.6$ V, $V_D = 3.4$ V, with a 1- μ A current through the voltage divider R_{G1} , R_{G2} . Assume the same MOSFET as in Example 5.6.

Ans. $R_{G1} = 1.6$ M Ω ; $R_{G2} = 3.4$ M Ω , $R_S = R_D = 5$ k Ω

Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the enhancement-type PMOS transistor have $V_{tp} = -1$ V and $k'_p(W/L) = 1$ mA/V². Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

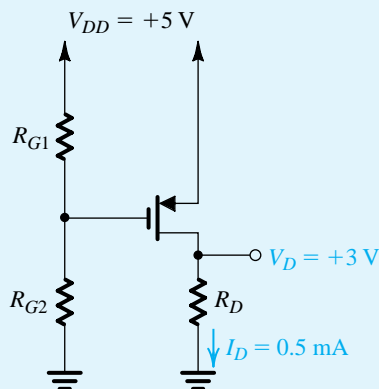


Figure 5.25 Circuit for Example 5.7.

Solution

Since the MOSFET is to be in saturation, we can write

$$I_D = \frac{1}{2} k_p' \frac{W}{L} |V_{OV}|^2$$

Substituting $I_D = 0.5 \text{ mA}$ and $k_p' W/L = 1 \text{ mA/V}^2$, we obtain

$$|V_{OV}| = 1 \text{ V}$$

and

$$V_{SG} = |V_{tp}| + |V_{OV}| = 1 + 1 = 2 \text{ V}$$

Since the source is at +5 V, the gate voltage must be set to +3 V. This can be achieved by the appropriate selection of the values of R_{G1} and R_{G2} . A possible selection is $R_{G1} = 2 \text{ M}\Omega$ and $R_{G2} = 3 \text{ M}\Omega$.

The value of R_D can be found from

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6 \text{ k}\Omega$$

Saturation-mode operation will be maintained up to the point that V_D exceeds V_G by $|V_{tp}|$; that is, until

$$V_{D_{\max}} = 3 + 1 = 4 \text{ V}$$

This value of drain voltage is obtained with R_D given by

$$R_D = \frac{4}{0.5} = 8 \text{ k}\Omega$$

EXERCISE

D5.14 For the circuit in Fig. E5.14, find the value of R that results in the PMOS transistor operating with an overdrive voltage $|V_{OV}| = 0.6 \text{ V}$. The threshold voltage is $V_{tp} = -0.4 \text{ V}$, the process transconductance parameter $k_p' = 0.1 \text{ mA/V}^2$, and $W/L = 10 \text{ }\mu\text{m}/0.18 \text{ }\mu\text{m}$.

Ans. $800 \text{ }\Omega$

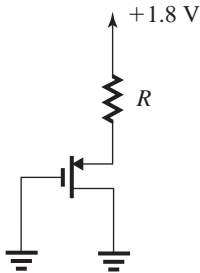


Figure E5.14

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_O , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .

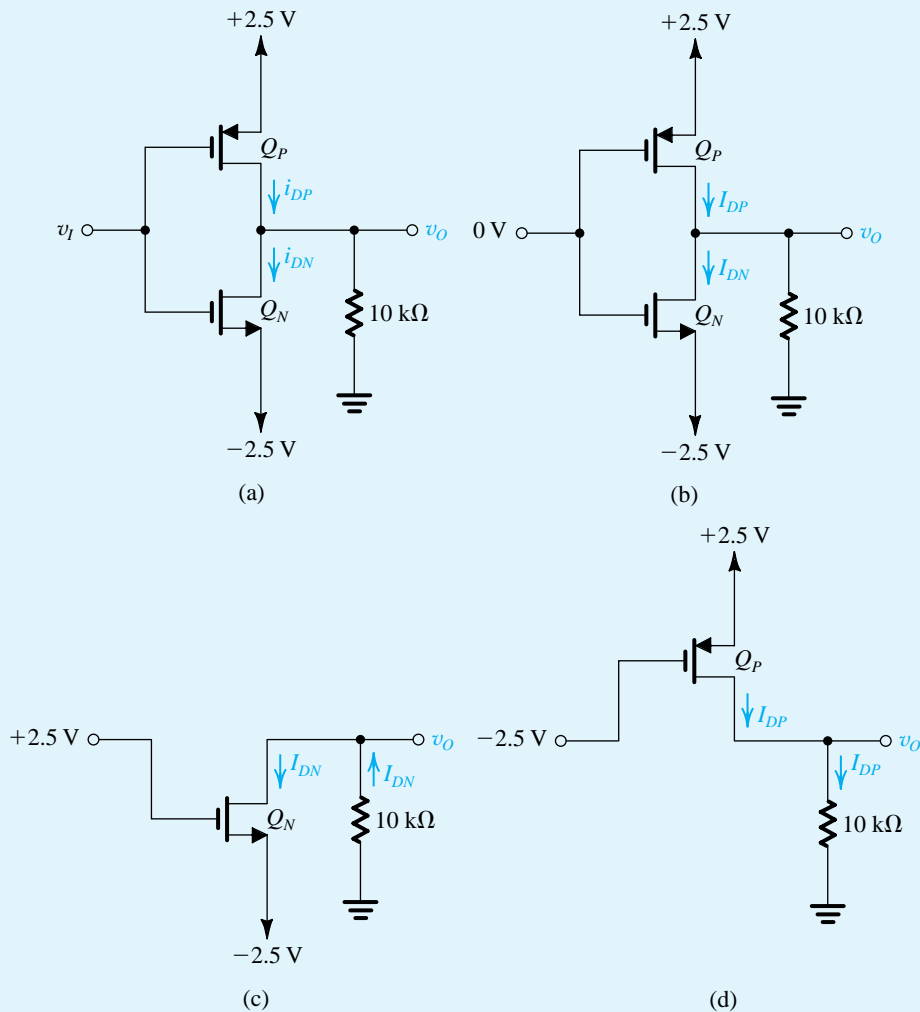


Figure 5.26 Circuits for Example 5.8.

Solution

Figure 5.26(b) shows the circuit for the case $v_I = 0 \text{ V}$. We note that since Q_N and Q_P are perfectly matched and are operating at equal values of $|V_{GS}|$ (2.5 V), the circuit is symmetrical, which dictates that $v_O = 0 \text{ V}$. Thus both Q_N and Q_P are operating with $|V_{DS}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \frac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{ mA}$$

Next, we consider the circuit with $v_I = +2.5$ V. Transistor Q_P will have a V_{SG} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 5.26(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_{tn} , causing Q_N to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$\begin{aligned} I_{DN} &\cong k'_n(W_n/L_n)(V_{GS} - V_{tn})V_{DS} \\ &= 1[2.5 - (-2.5) - 1][v_O - (-2.5)] \end{aligned}$$

From the circuit diagram shown in Fig. 5.26(c), we can also write

$$I_{DN}(\text{mA}) = \frac{0 - v_O}{10(\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \quad v_O = -2.44 \text{ V}$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06$ V, which is small as assumed.

Finally, the situation for the case $v_I = -2.5$ V [Fig. 5.26(d)] will be the exact complement of the case $v_I = +2.5$ V: Transistor Q_N will be off. Thus $I_{DN} = 0$, Q_P will be operating in the triode region with $I_{DP} = 2.44$ mA and $v_O = +2.44$ V.

EXERCISE

5.15 The NMOS and PMOS transistors in the circuit of Fig. E5.15 are matched with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage v_O for $v_I = 0$ V, $+2.5$ V, and -2.5 V.

Ans. $v_I = 0$ V: 0 mA, 0 mA, 0 V; $v_I = +2.5$ V: 0.104 mA, 0 mA, 1.04 V; $v_I = -2.5$ V: 0 mA, 0.104 mA, -1.04 V

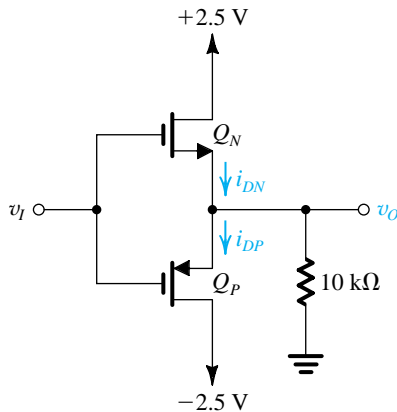


Figure E5.15

5.4 Applying the MOSFET in Amplifier Design

We now begin our study of the utilization of the MOSFET in the design of amplifiers. The basis for this important application is that when operated in saturation, the MOSFET functions as voltage-controlled current source: The gate-to-source voltage v_{GS} controls the drain current i_D . Although the control relationship is nonlinear (square law), we will shortly devise a method for obtaining almost-linear amplification from this fundamentally nonlinear device.

5.4.1 Obtaining a Voltage Amplifier

In the introduction to amplifier circuits in Section 1.5, we learned that a voltage-controlled current source can serve as a transconductance amplifier; that is, an amplifier whose input signal is a voltage and whose output signal is a current. More commonly, however, one is interested in voltage amplifiers. A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output. Doing this for a MOSFET results in the simple amplifier circuit shown in Fig. 5.27(a). Here v_{GS} is the input voltage, R_D (known as a **load resistance**) converts the drain current i_D to a voltage ($i_D R_D$), and V_{DD} is the supply voltage that powers up the amplifier and, together with R_D , establishes operation in the saturation region, as will be shown shortly.

In the amplifier circuit of Fig. 5.27(a) the output voltage is taken between the drain and ground, rather than simply across R_D . This is done because of the need to maintain a ground reference throughout the circuit. The output voltage v_{DS} is given by

$$v_{DS} = V_{DD} - i_D R_D \quad (5.30)$$

Thus it is an inverted version (note the minus sign) of $i_D R_D$ that is shifted by the constant value of the supply voltage V_{DD} .

5.4.2 The Voltage Transfer Characteristic (VTC)

A very useful tool that yields great insight into the operation of an amplifier circuit is its voltage transfer characteristic (VTC). This is simply a plot (or a clearly labeled sketch) of the output voltage versus the input voltage. For the MOS amplifier in Fig. 5.27(a), this is the plot of v_{DS} versus v_{GS} shown in Fig. 5.27(b).

Observe that for $v_{GS} < V_t$, the transistor is cut off, $i_D = 0$ and, from Eq. (5.30), $v_{DS} = V_{DD}$. As v_{GS} exceeds V_t , the transistor turns on and v_{DS} decreases. However, since initially v_{DS} is still high, the MOSFET will be operating in saturation. This continues as v_{GS} is increased until the value of v_{GS} is reached that results in v_{DS} becoming lower than v_{GS} by V_t volts (point B on the VTC in Fig. 5.27b). For v_{GS} greater than that at point B, the transistor operates in the triode region and v_{DS} decreases more slowly.

The VTC in Fig. 5.27(b) indicates that the segment of greatest slope (and hence potentially the largest amplifier gain) is that labeled AB, which corresponds to operation in the saturation region. An expression for the segment AB can be obtained by substituting for i_D in Eq. (5.30) by its saturation-region value

$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2 \quad (5.31)$$

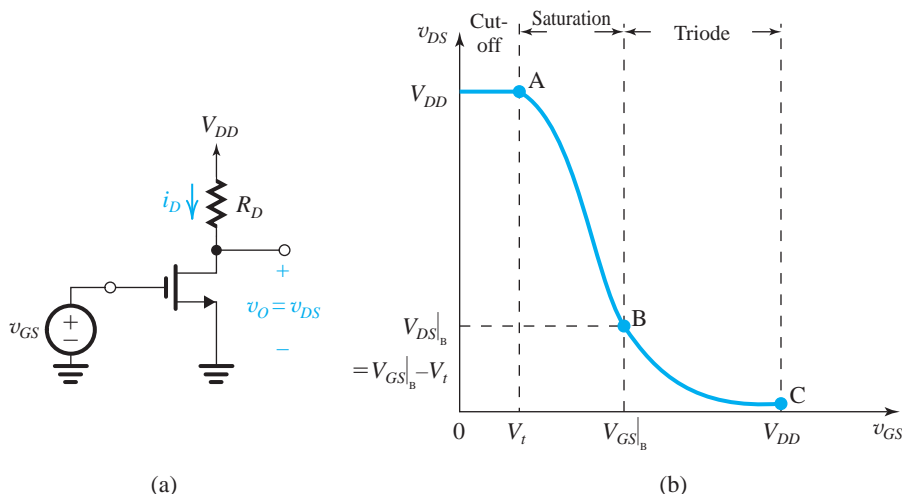


Figure 5.27 (a) Simple MOSFET amplifier with input v_{GS} and output v_{DS} . (b) The voltage transfer characteristic (VTC) of the amplifier in (a). The three segments of the VTC correspond to the three regions of operation of the MOSFET.

where we have for simplicity neglected channel-length modulation. The result is

$$v_{DS} = V_{DD} - \frac{1}{2}k_n R_D (v_{GS} - V_t)^2 \quad (5.32)$$

This is obviously a nonlinear relationship. Nevertheless, linear (or almost-linear) amplification can be obtained by using the technique of biasing the MOSFET. Before considering biasing, however, it is useful to determine the coordinates of point B, which is at the boundary between the saturation and the triode regions of operation. These can be obtained by substituting in Eq. (5.32), $v_{GS} = V_{GS}|_B$ and $v_{DS} = V_{DS}|_B = V_{GS}|_B - V_t$. The result is

$$V_{GS}|_B = V_t + \frac{\sqrt{2k_n R_D V_{DD} + 1} - 1}{k_n R_D} \quad (5.33)$$

EXERCISE

5.16 Consider the amplifier of Fig. 5.27(a) with $V_{DD} = 1.8$ V, $R_D = 17.5$ k Ω , and with a MOSFET specified to have $V_t = 0.4$ V, $k_n = 4$ mA/V², and $\lambda = 0$. Determine the coordinates of the end points of the saturation-region segment of the VTC. Also, determine $V_{DS}|_C$ assuming $V_{GS}|_C = V_{DD}$.

Ans. A: 0.4 V, 1.8 V; B: 0.613 V, 0.213 V; $V_{DS}|_C = 18$ mV

5.4.3 Biasing the MOSFET to Obtain Linear Amplification

Biasing enables us to obtain almost-linear amplification from the MOSFET. The technique is illustrated in Fig. 5.28(a). A dc voltage V_{GS} is selected to obtain operation at a point Q on the segment AB of the VTC. How to select an appropriate location for the bias point Q will be discussed shortly. For the time being, observe that the coordinates of Q are the dc

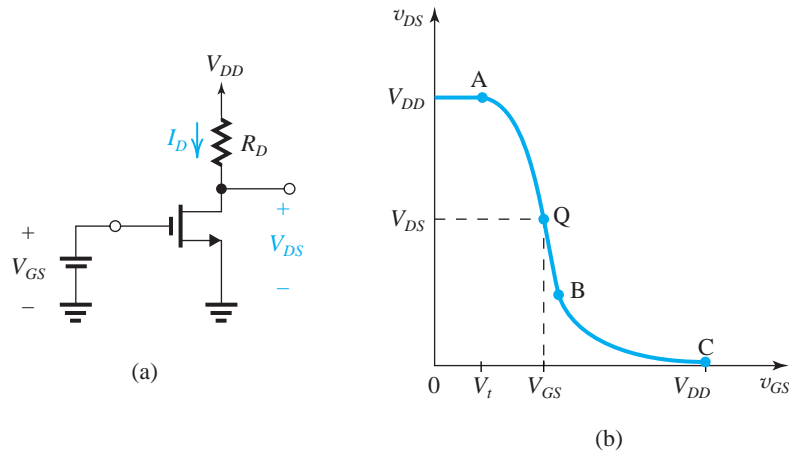


Figure 5.28 Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.

voltages V_{GS} and V_{DS} , which are related by

$$V_{DS} = V_{DD} - \frac{1}{2}k_n R_D (V_{GS} - V_t)^2 \quad (5.34)$$

Point Q is known as the **bias point** or the **dc operating point**. Also, since at Q no signal component is present, it is also known as the **quiescent point** (which is the origin of the symbol Q).

Next, the signal to be amplified, v_{gs} , a function of time t , is superimposed on the bias voltage V_{GS} , as shown in Fig. 5.29(a). Thus the total instantaneous value of v_{GS} becomes

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

The resulting $v_{DS}(t)$ can be obtained by substituting for $v_{GS}(t)$ into Eq. (5.32). Graphically, we can use the VTC to obtain $v_{DS}(t)$ point-by-point, as illustrated in Fig. 5.29(b). Here we show the case of v_{gs} being a triangular wave of “small” amplitude. Specifically, the amplitude of v_{gs} is small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. The shorter the segment, the greater the linearity achieved, and the closer to an ideal triangular wave the signal component at the output, v_{ds} , will be. This is the essence of obtaining linear amplification from the nonlinear MOSFET.

5.4.4 The Small-Signal Voltage Gain

If the input signal v_{gs} is kept small, the corresponding signal at the output v_{ds} will be nearly proportional to v_{gs} with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q. This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q,

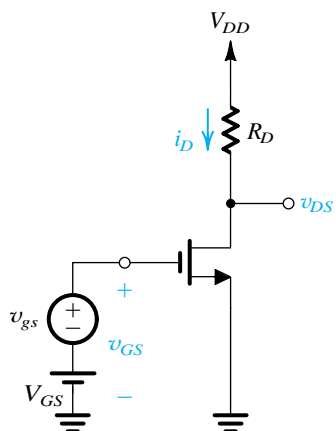
$$A_v \equiv \left. \frac{dv_{DS}}{dv_{GS}} \right|_{v_{GS}=V_{GS}} \quad (5.35)$$

Utilizing Eq. (5.32) we obtain

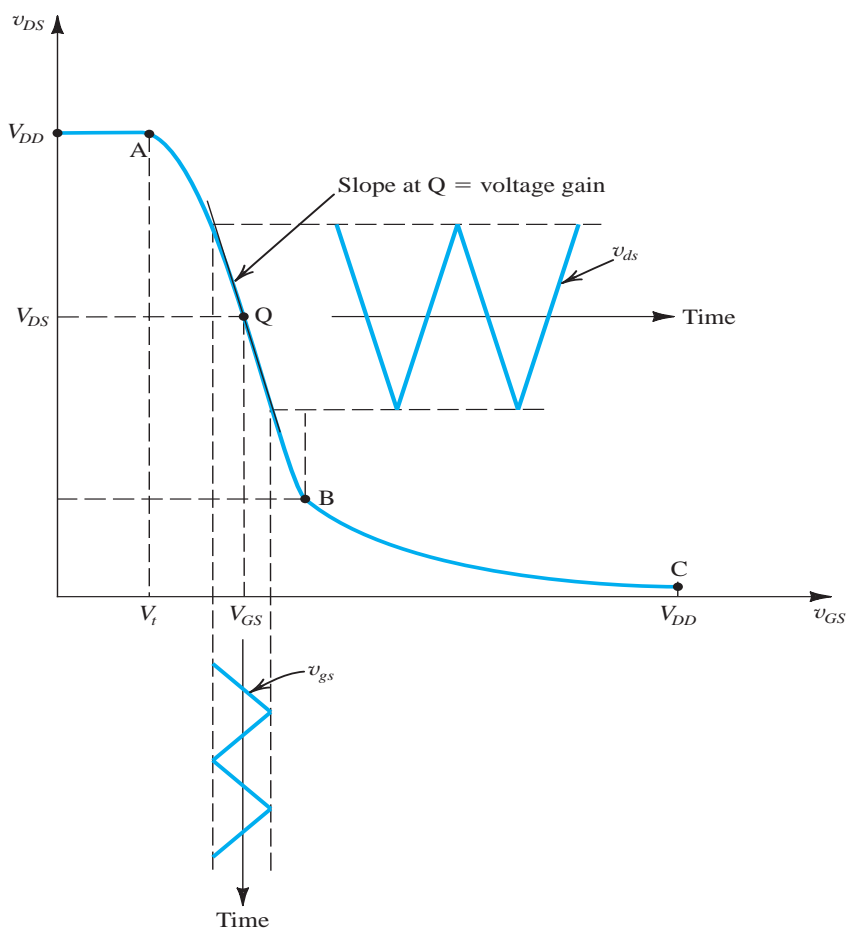
$$A_v = -k_n (V_{GS} - V_t) R_D \quad (5.36)$$

which can be expressed in terms of the overdrive voltage at the bias point V_{OV} as

$$A_v = -k_n V_{OV} R_D \quad (5.37)$$



(a)



(b)

Figure 5.29 The MOSFET amplifier with a small time-varying signal $v_{gs}(t)$ superimposed on the dc bias voltage V_{GS} . The MOSFET operates on a short almost-linear segment of the VTC around the bias point Q and provides an output voltage $v_{ds} = A_v v_{gs}$.

We make the following observations on this expression for the voltage gain.

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a 180° phase shift between the input and the output. This inversion is obvious in Fig. 5.29(b) and should have been anticipated from Eq. (5.32).
2. The gain is proportional to the load resistance R_D , to the transistor transconductance parameter k_n , and to the overdrive voltage V_{OV} . This all makes intuitive sense.

Another simple and insightful expression for the voltage gain A_v can be derived by recalling that the dc current in the drain at the bias point is related to V_{OV} by

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

This equation can be combined with Eq. (5.37) to yield

$$A_v = -\frac{I_D R_D}{V_{OV}/2} \quad (5.38)$$

That is, the gain is simply the ratio of the dc voltage drop across the load resistance R_D to $V_{OV}/2$. This relationship allows one to find an absolute upper limit on the magnitude of voltage gain achievable from this amplifier circuit. Simply note that $I_D R_D$ can approach but never exceed the power-supply voltage V_{DD} ; thus,

$$|A_{v\max}| = \frac{V_{DD}}{V_{OV}/2}$$

For modern CMOS technologies V_{OV} is usually no lower than about 0.2 V, with the result that the maximum achievable gain is about $10 V_{DD}$. Thus for a 0.13- μm CMOS technology that utilizes $V_{DD} = 1.3$ V, the approximate value of $|A_{\max}|$ is 13 V/V. In actual circuits, however, the maximum gain achievable is lower than this absolute maximum.

Example 5.9

Consider the amplifier circuit shown in Fig. 5.29(a). The transistor is specified to have $V_t = 0.4$ V, $k'_n = 0.4$ mA/V², $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8$ V, $R_D = 17.5$ k Ω , and $V_{GS} = 0.6$ V.

(a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV} , I_D , V_{DS} , and A_v .

(b) What is the maximum symmetrical signal swing allowed at the drain? Hence find the maximum allowable amplitude of a sinusoidal v_{gs} .

Solution

(a) With $V_{GS} = 0.6$ V, $V_{OV} = 0.6 - 0.4 = 0.2$ V.

Thus,

$$I_D = \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08 \text{ mA}$$

$$\begin{aligned} V_{DS} &= V_{DD} - R_D I_D \\ &= 1.8 - 17.5 \times 0.08 = 0.4 \text{ V} \end{aligned}$$

Since V_{DS} is greater than V_{OV} , the transistor is indeed operating in saturation. The voltage gain can be found from Eq. (5.37),

$$\begin{aligned} A_v &= -k_n V_{OV} R_D \\ &= -0.4 \times 10 \times 0.2 \times 17.5 \\ &= -14 \text{ V/V} \end{aligned}$$

An identical result can be found using Eq. (5.38).

(b) Since $V_{OV} = 0.2 \text{ V}$ and $V_{DS} = 0.4 \text{ V}$, we see that the maximum allowable negative signal swing at the drain is 0.2 V . In the positive direction, a swing of $+0.2 \text{ V}$ would not cause the transistor to cut off and thus is allowed. Thus the maximum symmetrical signal swing allowable at the drain is $\pm 0.2 \text{ V}$. The corresponding amplitude of v_{gs} can be found from

$$\hat{v}_{gs} = \frac{\hat{v}_{ds}}{|A_v|} = \frac{0.2 \text{ V}}{14} = 14.2 \text{ mV}$$

Since $\hat{v}_{gs} \ll V_{OV}$, the operation will be reasonably linear (more on this in later sections).

Greater insight into the issue of allowable signal swing can be obtained by examining the signal waveforms shown in Fig. 5.30. Note that for the MOSFET to remain in saturation at the negative peak of v_{ds} , we must ensure that

$$v_{DS\min} \geq v_{GS\max} - V_t$$

that is,

$$0.4 - |A_v| \hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

which results in

$$\hat{v}_{gs} \leq \frac{0.2}{|A_v| + 1} = 13.3 \text{ mV}$$

This is a more precise result than the one obtained earlier.

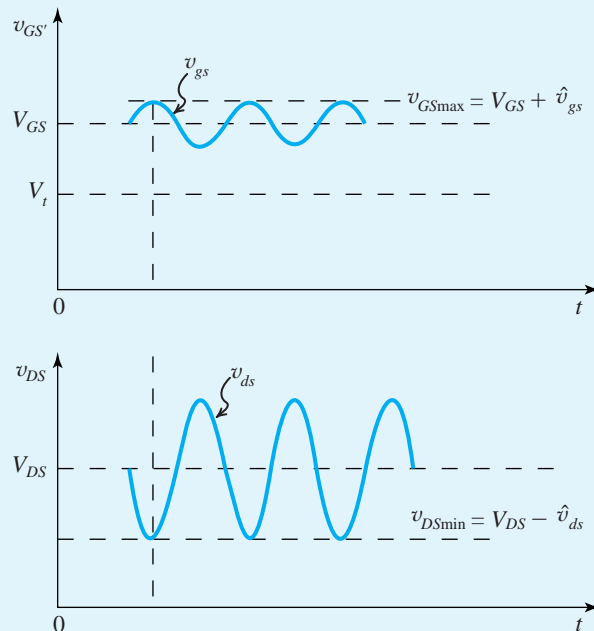


Figure 5.30 Signal waveforms at gate and drain for the amplifier in Example 5.9. Note that to ensure operation in the saturation region at all times, $v_{DS\min} \geq v_{GS\max} - V_t$.

EXERCISE

5.17 For the amplifier circuit studied in Example 5.9, provide two alternative designs, each providing a voltage gain of 10 by (a) changing R_D while keeping V_{OV} constant, and (b) changing V_{OV} while keeping R_D constant. For each design, specify V_{GS} , I_D , R_D , and V_{DS} .

Ans. (a) 0.6 V, 0.08 mA, 12.5 k Ω , 0.8 V; (b) 0.54 V, 0.04 mA, 17.5 k Ω , 1.1 V

5.4.5 Determining the VTC by Graphical Analysis

Figure 5.31 shows a graphical method for determining the VTC of the amplifier of Fig. 5.29(a). Although graphical analysis of transistor circuits is rarely employed in practice, it is useful for us at this stage for gaining greater insight into circuit operation, especially in answering the question of where to locate the bias point Q.

The graphical analysis is based on the observation that for each value of v_{GS} , the circuit will be operating at the point of intersection of the i_D - v_{DS} graph corresponding to the particular value of v_{GS} and the straight line representing Eq. (5.30), which can be rewritten in the form

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \quad (5.39)$$

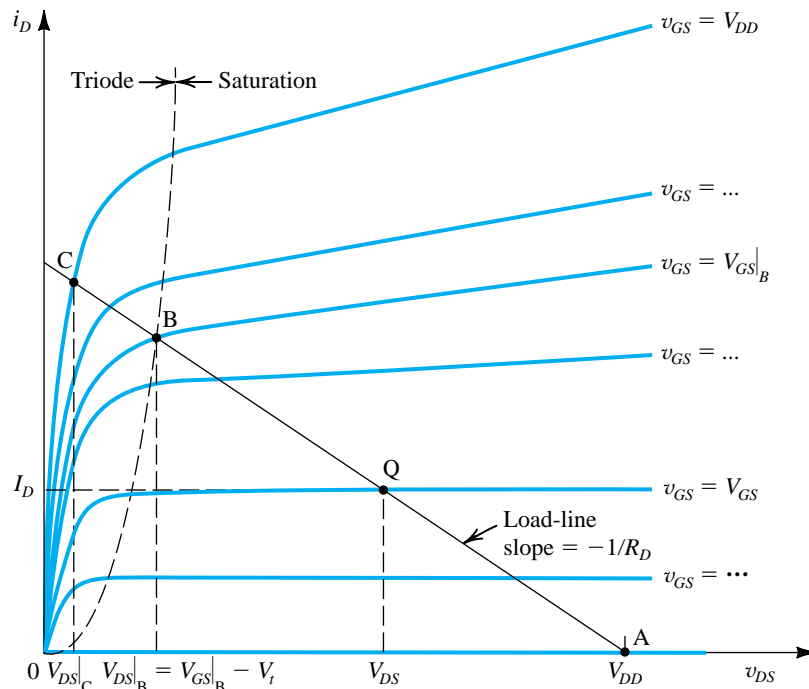


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

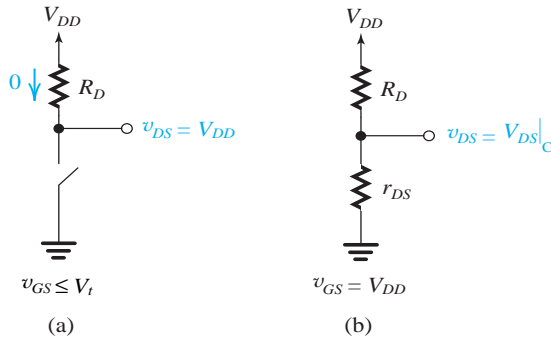


Figure 5.32 Operation of the MOSFET in Figure 5.29(a) as a switch: (a) Open, corresponding to point A in Figure 5.31; (b) Closed, corresponding to point C in Figure 5.31. The closure resistance is approximately equal to r_{DS} because V_{DS} is usually very small.

The straight line representing this relationship is superimposed on the i_D - v_{DS} characteristics in Fig. 5.31. It intersects the horizontal axis at $v_{DS} = V_{DD}$ and has a slope of $-1/R_D$. Since this straight line represents in effect the load resistance R_D , it is called the **load line**. The VTC is then determined point by point. Note that we have labeled four important points: point A at which $v_{GS} = V_t$, point Q at which the MOSFET can be biased for amplifier operation ($v_{GS} = V_{GS}$ and $v_{DS} = V_{DS}$), point B at which the MOSFET leaves saturation and enters the triode region, and point C, which is deep into the triode region and for which $v_{GS} = V_{DD}$. If the MOSFET is to be used as a switch, then operating points A and C are applicable: At A the transistor is off (open switch), and at C the transistor operates as a low-valued resistance r_{DS} and has a small voltage drop (closed switch). The incremental resistance at point C is also known as the **closure resistance**. The operation of the MOSFET as a switch is illustrated in Fig. 5.32. A detailed study of the application of the MOSFET as a switch is undertaken in Chapter 13 dealing with CMOS digital logic circuits.

5.4.6 Locating the Bias Point Q

The bias point Q is determined by the value of V_{GS} and that of the load resistance R_D . Two important considerations in deciding on the location of Q are the required gain and the allowable signal swing at the output. To illustrate, consider the VTC shown in Fig. 5.29(b). Here the value of R_D is fixed and the only variable remaining is the value of V_{GS} . Since the slope increases as we move closer to point B, we obtain higher gain by locating Q as close to B as possible. However, the closer Q is to the boundary point B, the smaller the allowable magnitude of negative signal swing. Thus, as often happens in engineering design, we encounter a situation requiring a trade-off.

In deciding on a value for R_D , it is useful to refer to the i_D - v_{DS} plane. Figure 5.33 shows two load lines resulting in two extreme bias points: Point Q_1 is too close to V_{DD} , resulting in a severe constraint on the positive signal swing of v_{ds} . Exceeding the allowable positive maximum results in the positive peaks of the signal being clipped off, since the MOSFET will turn off for the part of each cycle near the positive peak. We speak of this situation by saying that the circuit does not have sufficient “headroom.” Similarly, point Q_2 is too close to the boundary of the triode region, thus severely limiting the allowable negative signal swing of v_{ds} . Exceeding this limit would result in the transistor entering the triode region for part of each cycle near the negative peaks, resulting in a distorted output signal. In this situation we say that the circuit does not have sufficient “legroom.” We will have more to say on bias design in the Section 5.7.

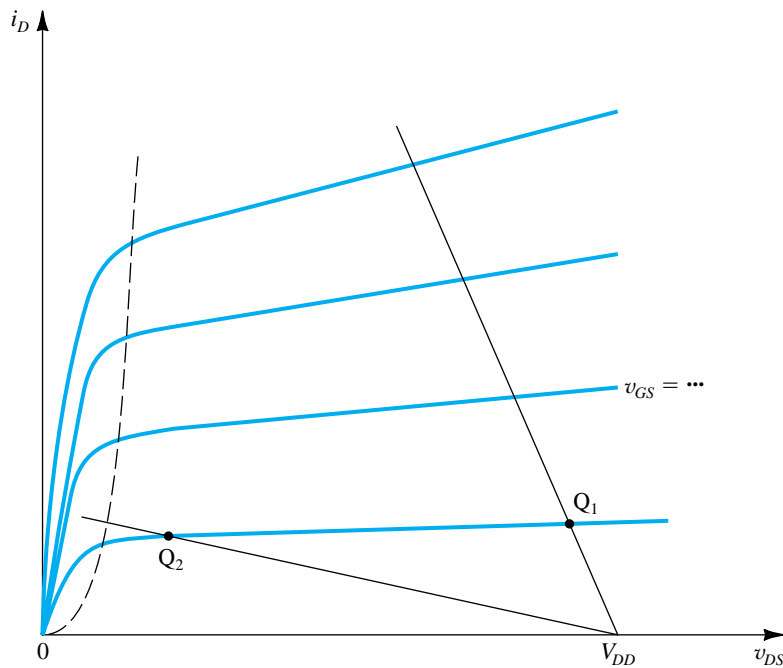


Figure 5.33 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

5.5 Small-Signal Operation and Models

In our study of the operation of the MOSFET amplifier in Section 5.4 we learned that linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small. In this section, we explore the small-signal operation in some detail. For this purpose we utilize the conceptual amplifier circuit shown in Fig. 5.34. Here the MOS transistor is biased by applying a dc voltage⁸ V_{GS} , and the input signal to be amplified, v_{gs} , is superimposed on the dc bias voltage V_{GS} . The output voltage is taken at the drain.

5.5.1 The DC Bias Point

The dc bias current I_D can be found by setting the signal v_{gs} to zero; thus,

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_nV_{OV}^2 \quad (5.40)$$

where we have neglected channel-length modulation (i.e., we have assumed $\lambda = 0$). Here $V_{OV} = V_{GS} - V_t$ is the overdrive voltage at which the MOSFET is biased to operate. The dc

⁸Practical biasing arrangements will be studied in Section 5.7.

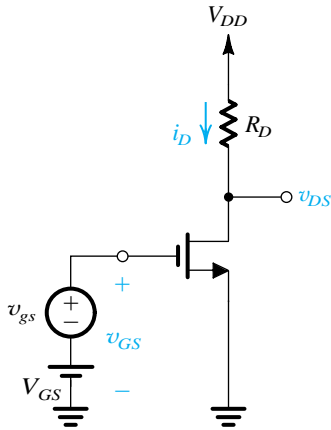


Figure 5.34 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

voltage at the drain, V_{DS} , will be

$$V_{DS} = V_{DD} - R_D I_D \quad (5.41)$$

To ensure saturation-region operation, we must have

$$V_{DS} > V_{OV}$$

Furthermore, since the total voltage at the drain will have a signal component superimposed on V_{DS} , V_{DS} has to be sufficiently greater than (V_{OV}) to allow for the required signal swing.

5.5.2 The Signal Current in the Drain Terminal

Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \quad (5.42)$$

resulting in a total instantaneous drain current i_D ,

$$\begin{aligned} i_D &= \frac{1}{2} k_n (V_{GS} + v_{gs} - V_t)^2 \\ &= \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n v_{gs}^2 \end{aligned} \quad (5.43)$$

The first term on the right-hand side of Eq. (5.43) can be recognized as the dc bias current I_D (Eq. 5.40). The second term represents a current component that is directly proportional to the input signal v_{gs} . The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents *nonlinear distortion*. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2} k_n v_{gs}^2 \ll k_n (V_{GS} - V_t) v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS} - V_t) \quad (5.44)$$

or, equivalently,

$$v_{gs} \ll 2V_{OV} \quad (5.45)$$

If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (5.43) and express i_D as

$$i_D \cong I_D + i_d \quad (5.46)$$

where

$$i_d = k_n(V_{GS} - V_t)v_{gs}$$

The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m ,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_t) \quad (5.47)$$

or in terms of the overdrive voltage V_{OV} ,

$$g_m = k_n V_{OV} \quad (5.48)$$

Figure 5.35 presents a graphical interpretation of the small-signal operation of the MOSFET amplifier. Note that g_m is equal to the slope of the $i_D - v_{GS}$ characteristic at the bias point,

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS} = V_{GS}} \quad (5.49)$$

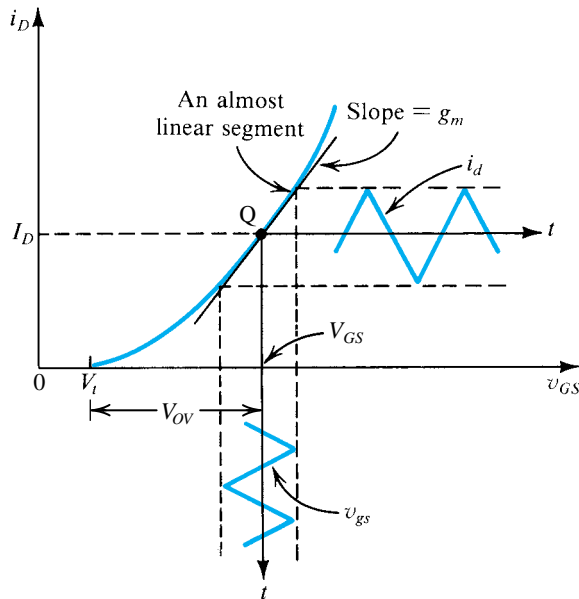


Figure 5.35 Small-signal operation of the MOSFET amplifier.

This is the formal definition of g_m , which can be shown to yield the expressions given in Eqs. (5.47) and (5.48).

5.5.3 The Voltage Gain

Returning to the circuit of Fig. 5.34, we can express the total instantaneous drain voltage v_{DS} as follows:

$$v_{DS} = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_{DS} = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as

$$v_{DS} = V_{DD} - R_D i_d$$

Thus the signal component of the drain voltage is

$$v_{ds} = -i_d R_D = -g_m v_{gs} R_D \quad (5.50)$$

which indicates that the voltage gain is given by

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D \quad (5.51)$$



The minus sign in Eq. (5.51) indicates that the output signal v_{ds} is 180° out of phase with respect to the input signal v_{gs} . This is illustrated in Fig. 5.36, which shows v_{GS} and v_{DS} . The input signal is assumed to have a triangular waveform with an amplitude much smaller than $2(V_{GS} - V_t)$, the small-signal condition in Eq. (5.44), to ensure linear operation. For operation in the saturation region at all times, the minimum value of v_{DS} should not fall below the corresponding value of v_{GS} by more than V_t . Also, the maximum value of v_{DS} should be smaller than V_{DD} ; otherwise the FET will enter the cutoff region and the peaks of the output signal waveform will be clipped off.

Finally, we note that by substituting for g_m from Eq. (5.48) the voltage gain expression in Eq. (5.51) becomes identical to that derived in Section 5.4—namely, Eq. (5.37).

5.5.4 Separating the DC Analysis and the Signal Analysis

From the preceding analysis, we see that under the small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d , the total drain voltage $v_{DS} = V_{DS} + v_{ds}$, and so on. It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations. That is, once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.

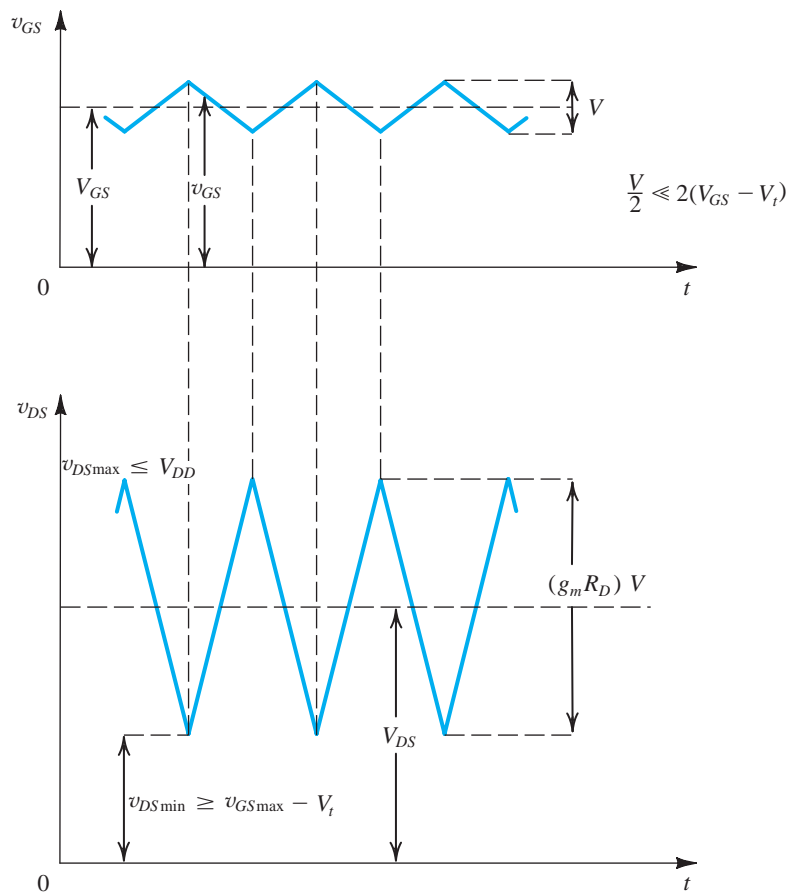


Figure 5.36 Total instantaneous voltages v_{GS} and v_{DS} for the circuit in Fig. 5.34.

5.5.5 Small-Signal Equivalent-Circuit Models

From a signal point of view, the FET behaves as a voltage-controlled current source. It accepts a signal v_{gs} between gate and source and provides a current $g_m v_{gs}$ at the drain terminal. The input resistance of this controlled source is very high—ideally, infinite. The output resistance—that is, the resistance looking into the drain—also is high, and we have assumed it to be infinite thus far. Putting all of this together, we arrive at the circuit in Fig. 5.37(a), which represents the small-signal operation of the MOSFET and is thus a **small-signal model** or a **small-signal equivalent circuit**.

In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent circuit model shown in Fig. 5.37(a). The rest of the circuit remains unchanged except that *ideal constant dc voltage sources are replaced by short circuits*. This is a result of the fact that the voltage across an ideal constant dc voltage source does not change, and thus there will always be a zero voltage signal across a constant dc voltage source. A dual statement applies for constant dc current sources; namely, the signal current of an ideal constant dc current source will always be zero, and thus *an ideal constant dc current source can be replaced by an open circuit* in the small-signal equivalent circuit of the amplifier. The

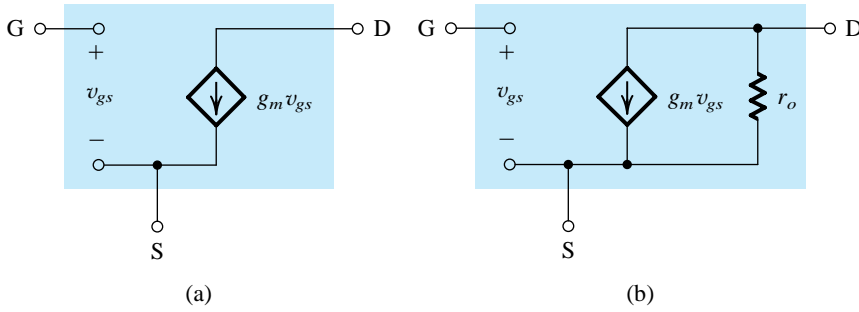


Figure 5.37 Small-signal models for the MOSFET: (a) neglecting the dependence of i_D on v_{DS} in saturation (the channel-length modulation effect); and (b) including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$.

circuit resulting can then be used to perform any required signal analysis, such as calculating voltage gain.

The most serious shortcoming of the small-signal model of Fig. 5.37(a) is that it assumes the drain current in saturation to be independent of the drain voltage. From our study of the MOSFET characteristics in saturation, we know that the drain current does in fact depend on v_{DS} in a linear manner. Such dependence was modeled by a finite resistance r_o between drain and source, whose value was given by Eq. (5.27) in Section 5.2.4, which we repeat here as

$$r_o = \frac{|V_A|}{I_D} \quad (5.52)$$

where $V_A = 1/\lambda$ is a MOSFET parameter that either is specified or can be measured. It should be recalled that for a given process technology, V_A is proportional to the MOSFET channel length. The current I_D is the value of the dc drain current without the channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_n V_{OV}^2 \quad (5.53)$$

Typically, r_o is in the range of 10 k Ω to 1000 k Ω . It follows that the accuracy of the small-signal model can be improved by including r_o in parallel with the controlled source, as shown in Fig. 5.37(b).

It is important to note that the small-signal model parameters g_m and r_o depend on the dc bias point of the MOSFET.

Returning to the amplifier of Fig. 5.34, we find that replacing the MOSFET with the small-signal model of Fig. 5.37(b) results in the voltage-gain expression

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m (R_D \parallel r_o) \quad (5.54)$$



Thus, the finite output resistance r_o results in a reduction in the magnitude of the voltage gain.

Although the analysis above is performed on an NMOS transistor, the results, and the equivalent circuit models of Fig. 5.37, apply equally well to PMOS devices, except for using $|V_{GS}|$, $|V_t|$, $|V_{OV}|$, and $|V_A|$ and replacing k_n with k_p .

5.5.6 The Transconductance g_m

We shall now take a closer look at the MOSFET transconductance given by Eq. (5.47), which we rewrite with $k_n = k'_n (W/L)$ as follows:

$$\text{I} \quad g_m = k'_n (W/L) (V_{GS} - V_t) = k'_n (W/L) V_{OV} \quad (5.55)$$

This relationship indicates that g_m is proportional to the process transconductance parameter $k'_n = \mu_n C_{ox}$ and to the W/L ratio of the MOS transistor; hence to obtain relatively large transconductance the device must be short and wide. We also observe that for a given device the transconductance is proportional to the overdrive voltage, $V_{OV} = V_{GS} - V_t$, the amount by which the bias voltage V_{GS} exceeds the threshold voltage V_t . Note, however, that increasing g_m by biasing the device at a larger V_{GS} has the disadvantage of reducing the allowable voltage signal swing at the drain.

Another useful expression for g_m can be obtained by substituting for V_{OV} in Eq. (5.55) by $\sqrt{2I_D / (k'_n (W/L))}$ [from Eq. (5.40)]:

$$\text{I} \quad g_m = \sqrt{2k'_n} \sqrt{W/L} \sqrt{I_D} \quad (5.56)$$

This expression shows two things:

1. For a given MOSFET, g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{W/L}$.

In contrast, the transconductance of the bipolar junction transistor (BJT) studied in Chapter 6 is proportional to the bias current and is independent of the physical size and geometry of the device.

To gain some insight into the values of g_m obtained in MOSFETs consider an integrated-circuit device operating at $I_D = 0.5$ mA and having $k'_n = 120 \mu\text{A}/\text{V}^2$. Equation (5.56) shows that for $W/L = 1$, $g_m = 0.35$ mA/V, whereas a device for which $W/L = 100$ has $g_m = 3.5$ mA/V. In contrast, a BJT operating at a collector current of 0.5 mA has $g_m = 20$ mA/V.

Yet another useful expression for g_m of the MOSFET can be obtained by substituting for $k'_n (W/L)$ in Eq. (5.55) by $2I_D / (V_{GS} - V_t)^2$:

$$\text{I} \quad g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}} \quad (5.57)$$

A convenient graphical construction that clearly illustrates this relationship is shown in Fig. 5.38.

In summary, there are three different relationships for determining g_m —Eqs. (5.55), (5.56), and (5.57)—and there are three design parameters— (W/L) , V_{OV} , and I_D , any two of which can be chosen independently. That is, the designer may choose to operate the MOSFET with a certain overdrive voltage V_{OV} and at a particular current I_D ; the required W/L ratio can then be found and the resulting g_m determined.

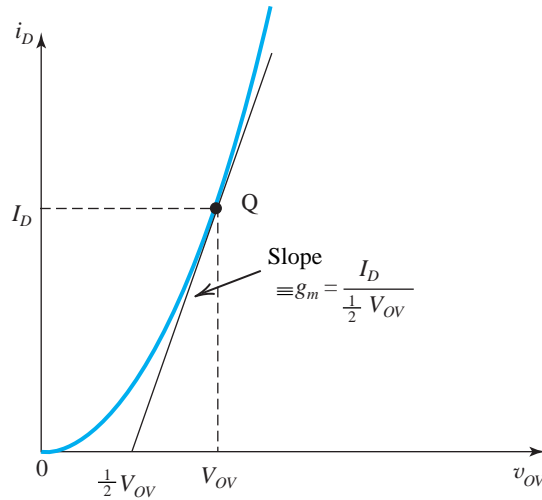
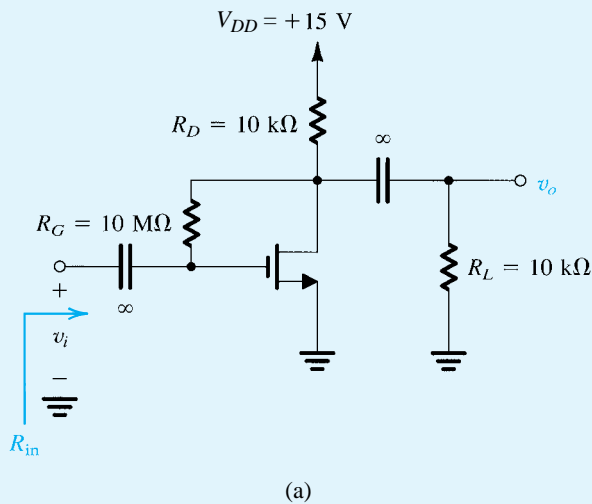


Figure 5.38 The slope of the tangent at the bias point Q intersects the v_{OV} axis at $\frac{1}{2} V_{OV}$. Thus, $g_m = I_D / (\frac{1}{2} V_{OV})$.

Example 5.10

Figure 5.39(a) shows a discrete common-source MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 5.7. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k'_n(W/L) = 0.25$ mA/V², and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.



Example 5.10 continued

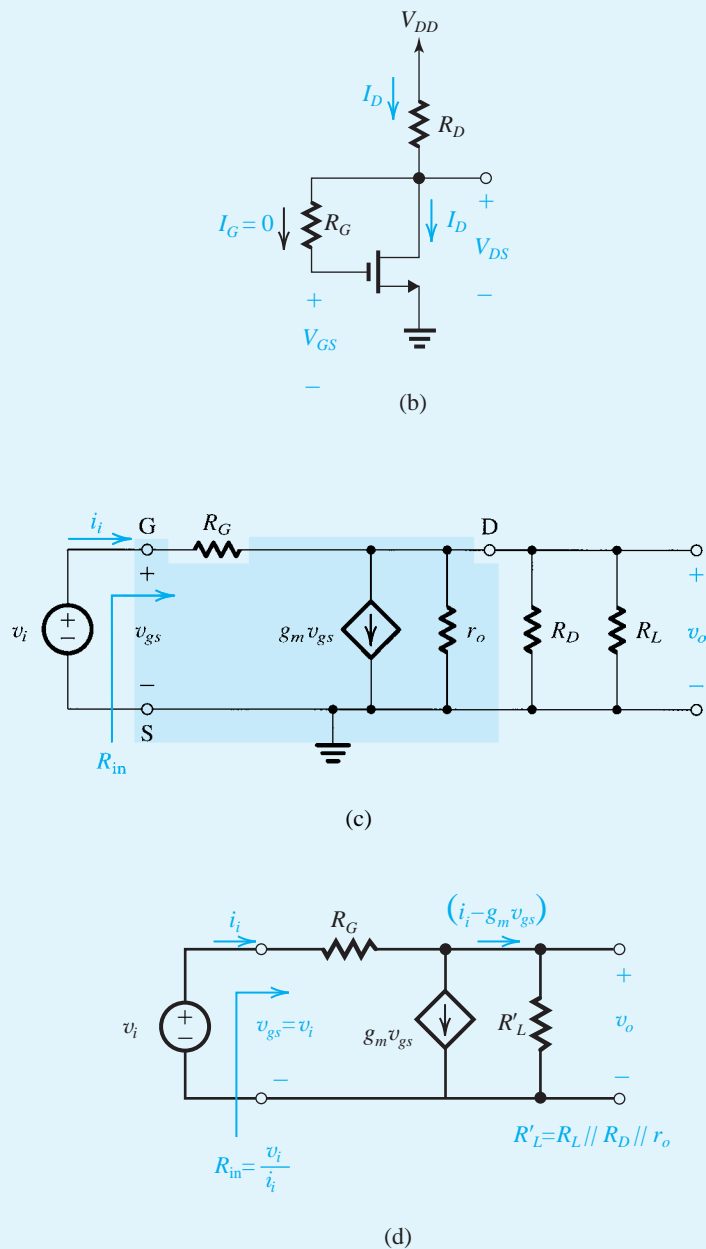


Figure 5.39 Example 5.10: (a) amplifier circuit; (b) circuit for determining the dc operating point; (c) the amplifier small-signal equivalent circuit; (d) a simplified version of the circuit in (c).

Solution

We first determine the dc operating point. For this purpose, we eliminate the input signal v_i , and open-circuit the two coupling capacitors (since they block dc currents). The result is the circuit shown in Fig. 5.39(b). We note that since $I_G = 0$, the dc voltage drop across R_G will be zero, and

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \quad (5.58)$$

With $V_{DS} = V_{GS}$, the NMOS transistor will be operating in saturation. Thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad (5.59)$$

where, for simplicity, we have neglected the effect of channel-length modulation on the dc operating point. Substituting $V_{DD} = 15$ V, $R_D = 10$ k Ω , $k_n = 0.25$ mA/V², and $V_t = 1.5$ V in Eqs. (5.58) and (5.59), and substituting for V_{GS} from Eq. (5.58) into Eq. (5.59) results in a quadratic equation in I_D . Solving the latter and discarding the root that is not physically meaningful yields the solution

$$I_D = 1.06 \text{ mA}$$

which corresponds to

$$V_{GS} = V_{DS} = 4.4 \text{ V}$$

and

$$V_{OV} = 4.4 - 1.5 = 2.9 \text{ V}$$

Next we proceed with the small-signal analysis of the amplifier. Toward that end we replace the MOSFET with its small-signal model to obtain the small-signal equivalent circuit of the amplifier, shown in Fig. 5.39(c). Observe that we have replaced the coupling capacitors with short circuits. The dc voltage supply V_{DD} has also been replaced with a short circuit to ground.

The values of the transistor small-signal parameters g_m and r_o can be determined by using the dc bias quantities found above, as follows:

$$\begin{aligned} g_m &= k_n V_{OV} \\ &= 0.25 \times 2.9 = 0.725 \text{ mA/V} \\ r_o &= \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega \end{aligned}$$

Next we use the equivalent circuit of Fig. 5.39(c) to determine the input resistance $R_{in} \equiv v_i/i_i$ and the voltage gain $A_v = v_o/v_i$. Toward that end we simplify the circuit by combining the three parallel resistances r_o , R_D , and R_L in a single resistance R'_L ,

$$\begin{aligned} R'_L &= R_L \parallel R_D \parallel r_o \\ &= 10 \parallel 10 \parallel 47 = 4.52 \text{ k}\Omega \end{aligned}$$

as shown in Fig. 5.39(d). For the latter circuit we can write the two equations

$$v_o = (i_i - g_m v_{gs}) R'_L \quad (5.60)$$

Example 5.10 *continued*

and

$$i_i = \frac{v_{gs} - v_o}{R_G} \quad (5.61)$$

Substituting for i_i from Eq. (5.61) into Eq. (5.60) results in the following expression for the voltage gain $A_v \equiv v_o/v_i = v_o/v_{gs}$:

$$A_v = -g_m R'_L \frac{1 - (1/g_m R_G)}{1 + (R'_L/R_G)}$$

Since R_G is very large, $g_m R_G \gg 1$ and $R'_L/R_G \ll 1$ (the reader can easily verify this), and the gain expression can be approximated as

$$A_v \simeq -g_m R'_L \quad (5.62)$$

Substituting, $g_m = 0.725 \text{ mA/V}$ and $R'_L = 4.52 \text{ k}\Omega$ yields

$$A_v = -3.3 \text{ V/V}$$

To obtain the input resistance, we substitute in Eq. (5.61) for $v_o = A_v v_{gs} = -g_m R'_L v_{gs}$, then use $R_{in} \equiv v_i/i_i = v_{gs}/i_i$ to obtain

$$R_{in} = \frac{R_G}{1 + g_m R'_L} \quad (5.63)$$

This is an interesting relationship: The input resistance decreases as the gain ($g_m R'_L$) is increased. The value of R_{in} can now be determined; it is

$$R_{in} = \frac{10 \text{ M}\Omega}{1 + 3.3} = 2.33 \text{ M}\Omega$$

which is still very large.

The largest allowable input signal \hat{v}_i is constrained by the need to keep the transistor in saturation at all times; that is,

$$v_{DS} \geq v_{GS} - V_t$$

Enforcing this condition with equality at the point v_{GS} is maximum and v_{DS} is minimum, we write

$$\begin{aligned} v_{DS\min} &= v_{GS\max} - V_t \\ V_{DS} - |A_v| \hat{v}_i &= V_{GS} + \hat{v}_i - V_t \end{aligned}$$

Since $V_{DS} = V_{GS}$, we obtain

$$\hat{v}_i = \frac{V_t}{|A_v| + 1}$$

This is a general relationship that applies to this circuit irrespective of the component values. Observe that it simply states that the maximum signal swing is determined by the fact that the bias arrangement makes $V_D = V_G$ and thus, to keep the MOSFET out of the triode region, the signal between D and G is constrained to be equal to V_t . For our particular design,

$$\hat{v}_i = \frac{1.5}{3.3 + 1} = 0.35 \text{ V}$$

A modification of this circuit that increases the allowable signal swing is investigated in Problem 5.80.

EXERCISE

D5.18 Consider the amplifier circuit of Fig. 5.39(a) without the load resistance R_L and with channel length modulation neglected. Let $V_{DD} = 5$ V, $V_t = 0.7$ V, and $k_n = 1$ mA/V². Find V_{OV} , I_D , R_D , and R_G to obtain a voltage gain of 25 V/V and an input resistance of 0.5 M Ω . What is the maximum allowable input signal, \hat{v}_i ?

Ans. 0.319 V; 50.7 μ A; 78.5 k Ω ; 13 M Ω ; 27 mV

5.5.7 The T Equivalent-Circuit Model

Through a simple circuit transformation it is possible to develop an alternative equivalent-circuit model for the MOSFET. The development of such a model, known as the T model, is illustrated in Fig. 5.40. Figure 5.40(a) shows the equivalent circuit studied

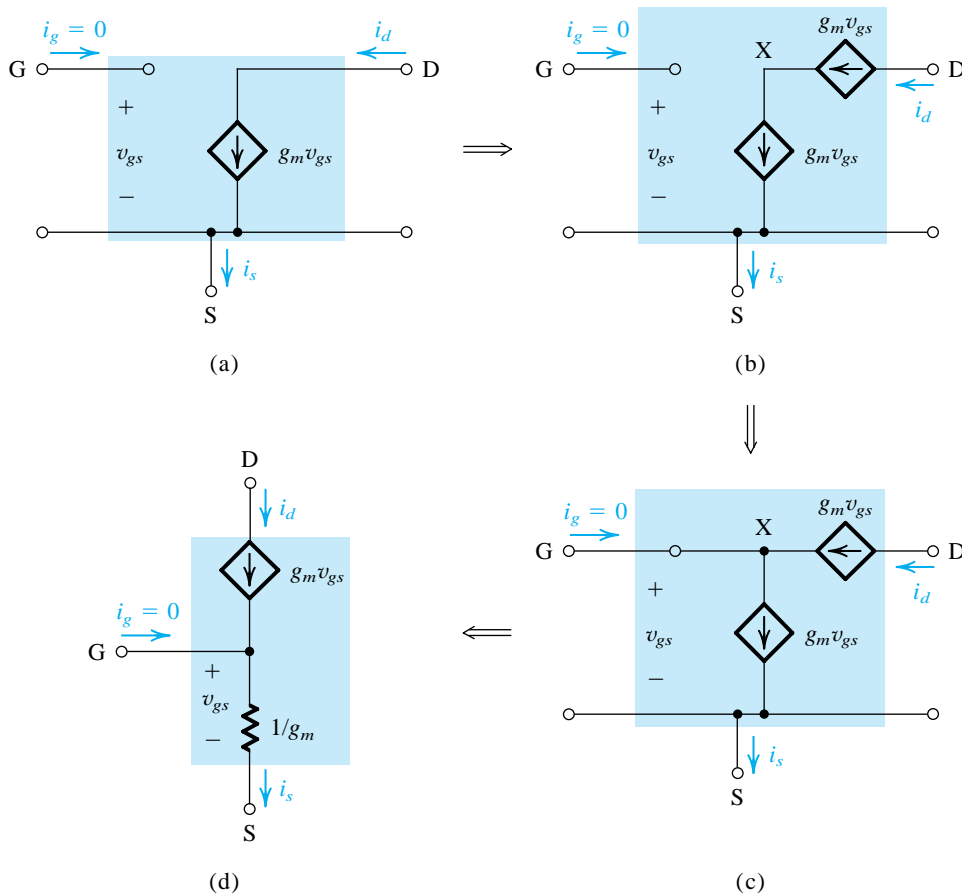


Figure 5.40 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted; however, it may be added between D and S in the T model of (d).

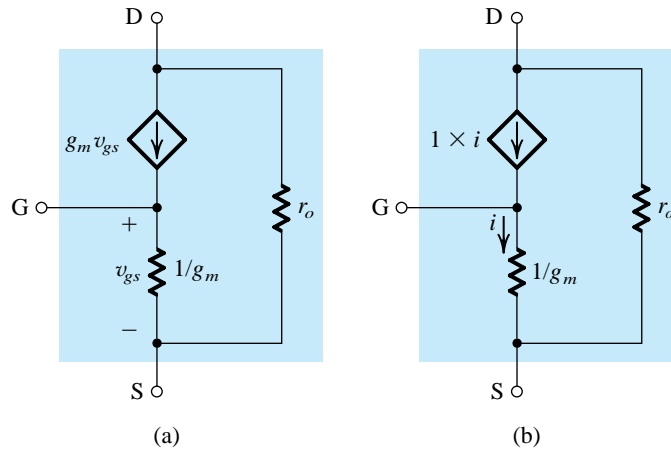


Figure 5.41 (a) The T model of the MOSFET augmented with the drain-to-source resistance r_o . (b) An alternative representation of the T model.

above without r_o . In Fig. 5.40(b) we have added a second $g_m v_{gs}$ current source in series with the original controlled source. This addition obviously does not change the terminal currents and is thus allowed. The newly created circuit node, labeled X, is joined to the gate terminal G in Fig. 5.40(c). Observe that the gate current does not change—that is, it remains equal to zero—and thus this connection does not alter the terminal characteristics. We now note that we have a controlled current source $g_m v_{gs}$ connected across its control voltage v_{gs} . We can replace this controlled source by a resistance as long as this resistance draws an equal current as the source. (See the source-absorption theorem in Appendix D.) Thus the value of the resistance is $v_{gs}/g_m v_{gs} = 1/g_m$. This replacement is shown in Fig. 5.40(d), which depicts the alternative model. Observe that i_g is still zero, $i_d = g_m v_{gs}$, and $i_s = v_{gs}/(1/g_m) = g_m v_{gs}$, all the same as in the original model in Fig. 5.40(a).

The model of Fig. 5.40(d) shows that the resistance between gate and source looking into the source is $1/g_m$. This observation and the T model prove useful in many applications. Note that the resistance between gate and source, looking into the gate, is infinite.

In developing the T model we did not include r_o . If desired, this can be done by incorporating in the circuit of Fig. 5.40(d) a resistance r_o between drain and source, as shown in Fig. 5.41(a). An alternative representation of the T model, in which the voltage-controlled current source is replaced with a current-controlled current source, is shown in Fig. 5.41(b).

Finally, we should note that in order to distinguish the model of Fig. 5.37(b) from the equivalent T model, the former is sometimes referred to as the **hybrid- π model**, a carryover from the bipolar transistor literature. The origin of this name will be explained in the next chapter.

Example 5.11

Figure 5.42(a) shows a MOSFET amplifier biased by a constant-current source I . Assume that the values of I and R_D are such that the MOSFET operates in the saturation region. The input signal v_i is coupled to

the source terminal by utilizing a large capacitor C_{C1} . Similarly, the output signal at the drain is taken through a large coupling capacitor C_{C2} . Find the input resistance R_{in} and the voltage gain v_o/v_i . Neglect channel-length modulation.

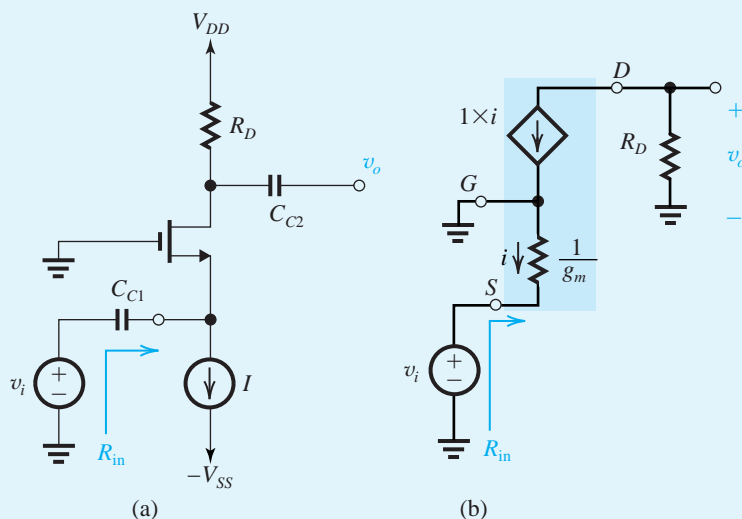


Figure 5.42 (a) Amplifier circuit for Example 5.11; (b) Small-signal equivalent circuit of the amplifier in (a).

Solution

Replacing the MOSFET with its T equivalent-circuit model results in the amplifier equivalent circuit shown in Fig. 5.42(b). Observe that the dc current source I is replaced with an open circuit and the dc voltage source V_{DD} is replaced by a short circuit. The large coupling capacitors have been replaced by short circuits. From the equivalent circuit-model we determine

$$R_{in} = \frac{v_i}{-i} = 1/g_m$$

and

$$v_o = -iR_D = \left(\frac{v_i}{1/g_m} \right) R_D = g_m R_D v_i$$

Thus,

$$A_v \equiv \frac{v_o}{v_i} = g_m R_D$$

We note that this amplifier, known as the common-gate amplifier because the gate at ground potential is common to both the input and output ports, has a low input resistance ($1/g_m$) and a noninverting gain. We shall study this amplifier type in Section 5.6.5.

EXERCISE

5.19 Use the T model of Fig. 5.41(b) to show that a MOSFET whose drain is connected to its gate exhibits an incremental resistance equal to $[(1/g_m) \parallel r_o]$.

Ans. See Fig. E5.19.

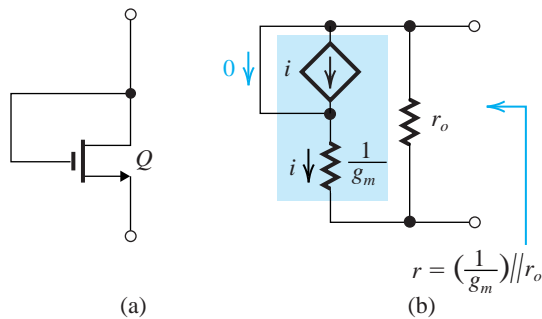


Figure E5.19 Circuits for Exercise 5.19. Note that the bias arrangement of Q is not shown.

5.5.8 Summary

We conclude this section by presenting in Table 5.3 a summary of the formulas for calculating the values of the small-signal MOSFET parameters. Observe that for g_m we have three different formulas, each providing the circuit designer with insight regarding design choices. We shall make frequent comments on these in later sections and chapters.

Table 5.3 Small-Signal Equivalent-Circuit Models for the MOSFET

Small-Signal Parameters

NMOS transistors

■ Transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

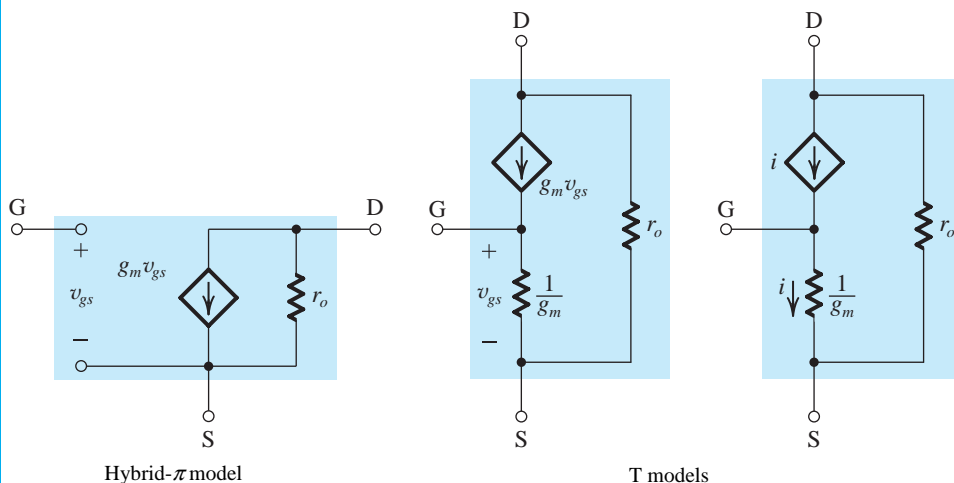
■ Output resistance:

$$r_o = V_A/I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS *except* using $|V_{OV}|$, $|V_A|$, and replacing μ_n with μ_p .

Small-Signal Equivalent Circuit Models



EXERCISES

- 5.20** For the amplifier in Fig. 5.34, let $V_{DD} = 5$ V, $R_D = 10$ k Ω , $V_t = 1$ V, $k'_n = 20$ $\mu\text{A}/\text{V}^2$, $W/L = 20$, $V_{GS} = 2$ V, and $\lambda = 0$.
 (a) Find the dc current I_D and the dc voltage V_{DS} .
 (b) Find g_m .
 (c) Find the voltage gain.
 (d) If $v_{gs} = 0.2 \sin \omega t$ volts, find v_{ds} assuming that the small-signal approximation holds. What are the minimum and maximum values of v_{DS} ?
 (e) Use Eq. (5.43) to determine the various components of i_D . Using the identity ($\sin^2 \omega t = \frac{1}{2} - \frac{1}{2} \cos 2\omega t$), show that there is a slight shift in I_D (by how much?) and that there is a second-harmonic component (i.e., a component with frequency 2ω). Express the amplitude of the second-harmonic component as a percentage of the amplitude of the fundamental. (This value is known as the second-harmonic distortion.)
Ans. (a) 200 μA , 3 V; (b) 0.4 mA/V; (c) -4 V/V; (d) $v_{ds} = -0.8 \sin \omega t$ volts, 2.2 V, 3.8 V; (e) $i_D = (204 + 80 \sin \omega t - 4 \cos 2\omega t)$ μA , 5%
- 5.21** An NMOS transistor has $\mu_n C_{ox} = 60$ $\mu\text{A}/\text{V}^2$, $W/L = 40$, $V_t = 1$ V, and $V_A = 15$ V. Find g_m and r_o when (a) the bias voltage $V_{GS} = 1.5$ V, (b) the bias current $I_D = 0.5$ mA.
Ans. (a) 1.2 mA/V, 50 k Ω ; (b) 1.55 mA/V, 30 k Ω
- 5.22** A MOSFET is to operate at $I_D = 0.1$ mA and is to have $g_m = 1$ mA/V. If $k'_n = 50$ $\mu\text{A}/\text{V}^2$, find the required W/L ratio and the overdrive voltage.
Ans. 100; 0.2 V
- 5.23** For a fabrication process for which $\mu_p \approx 0.4\mu_n$, find the ratio of the width of a PMOS transistor to the width of an NMOS transistor so that the two devices have equal g_m for the same bias conditions. The two devices have equal channel lengths.
Ans. 2.5
- 5.24** A PMOS transistor has $V_t = -1$ V, $k'_p = 60$ $\mu\text{A}/\text{V}^2$, and $W/L = 16$ $\mu\text{m}/0.8$ μm . Find I_D and g_m when the device is biased at $V_{GS} = -1.6$ V. Also, find the value of r_o if λ (at $L = 1$ μm) = -0.04 V^{-1} .
Ans. 216 μA ; 0.72 mA/V; 92.6 k Ω
- 5.25** Use the formulas in Table 5.3 to derive an expression for $(g_m r_o)$ in terms of V_A and V_{OV} . As we shall see in Chapter 7, this is an important transistor parameter and is known as the intrinsic gain. Evaluate the value of $g_m r_o$ for an NMOS transistor fabricated in a 0.8- μm CMOS process for which $V'_A = 12.5$ V/ μm of channel length. Let the device have minimum channel length and be operated at an overdrive voltage of 0.2 V.
Ans. $g_m r_o = 2V_A/V_{OV}$; 100 V/V

5.6 Basic MOSFET Amplifier Configurations

It is useful at this point to take stock of where we are and where we are going in our study of MOSFET amplifiers. In Section 5.4 we examined the essence of the use of the MOSFET as an amplifier. There we found that almost-linear amplification can be obtained by biasing the MOSFET at an appropriate point in its saturation region of operation and by keeping the signal v_{gs} small. We then took a closer look at the small-signal operation of the MOSFET in Section 5.5 and developed circuit models to represent the transistor, thus facilitating the determination of amplifier parameters such as voltage gain and input and output resistances.

We are now ready to consider the various possible configurations of MOSFET amplifiers, and we will do that in the present section. To focus our attention on the salient features of the various configurations, we shall present them in their most simple, or “stripped down” version. Thus, we will not show the dc biasing arrangements, leaving the study of bias design to the next section. Finally, in Section 5.8 we will bring everything together and present practical circuits for discrete-circuit MOSFET amplifiers; namely, those amplifier circuits that can be constructed using discrete components. The study of integrated-circuit amplifiers begins in Chapter 7.

5.6.1 The Three Basic Configurations

There are three basic configurations for connecting the MOSFET as an amplifier. Each of these configurations is obtained by connecting one of the three MOSFET terminals to ground, thus creating a two-port network with the grounded terminal being *common* to the input and output ports. Figure 5.43 shows the resulting three configurations with the biasing arrangements omitted.

In the circuit of Fig. 5.43(a) the source terminal is connected to ground, the input voltage signal v_i is applied between the gate and ground, and the output voltage signal v_o is taken between the drain and ground, across the resistance R_D . This configuration, therefore, is called the grounded-source or **common-source (CS)** amplifier. It is by far the most popular MOS amplifier configuration and is the one we utilized in Sections 5.4 and 5.5 to study MOS amplifier operation.

The **common-gate (CG)** or grounded-gate amplifier is shown in Fig. 5.43(b). It is obtained by connecting the gate to ground, applying the input v_i between the source and

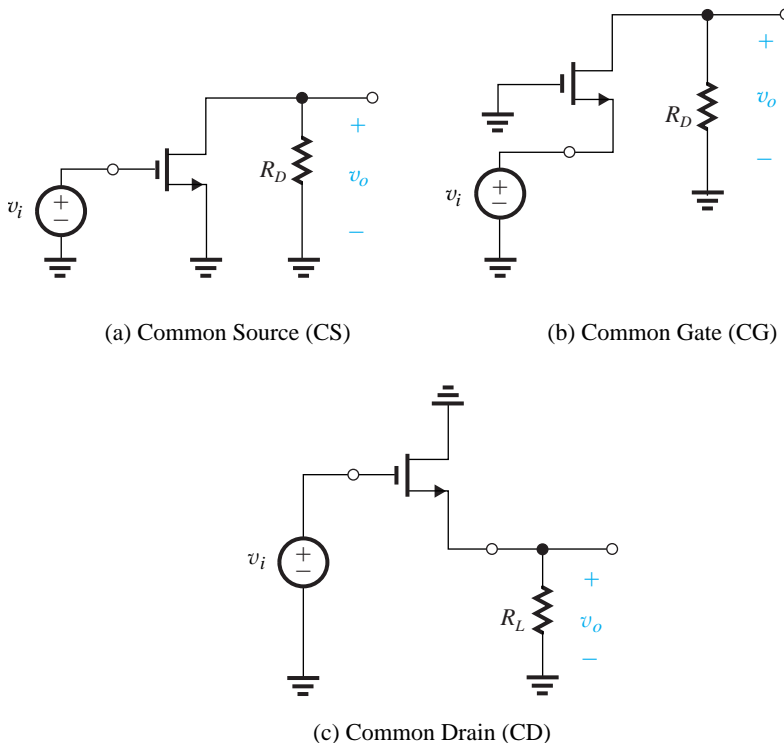


Figure 5.43 The three basic MOSFET amplifier configurations.

ground, and taking the output v_o across the resistance R_D connected between the drain and ground. We encountered a CG amplifier in Example 5.11.

Finally, Fig. 5.43(c) shows the **common-drain (CD)** or grounded-drain amplifier. It is obtained by connecting the drain terminal to ground, applying the input voltage signal v_i between gate and ground, and taking the output voltage signal between the source and ground, across a load resistance R_L . For reasons that will become apparent shortly, this configuration is more commonly called the **source follower**.

Our study of the three basic MOS amplifier configurations will reveal that each has distinctly different attributes and hence areas of application.

5.6.2 Characterizing Amplifiers

Before we begin our study of the different MOSFET amplifier configurations, we consider how to characterize the performance of an amplifier as a circuit building block. An introduction to this topic was presented in Section 1.5.

Figure 5.44(a) shows an amplifier fed with a signal source having an open-circuit voltage v_{sig} and an internal resistance R_{sig} . These can be the parameters of an actual signal source or, in a cascade amplifier, the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study. The amplifier is shown with a load resistance R_L

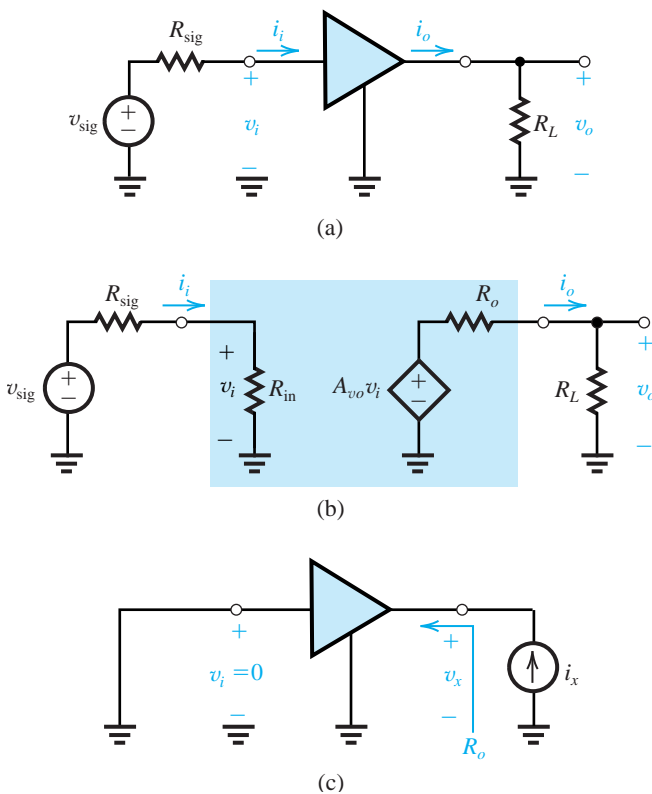


Figure 5.44 Characterization of the amplifier as a functional block: (a) An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig} , and feeding a load resistance R_L ; (b) Equivalent-circuit representation of the circuit in (a); (c) Determining the amplifier output resistance R_o .

connected to the output terminal. Here, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

Figure 5.44(b) shows the amplifier circuit with the amplifier block replaced by its equivalent-circuit model. The input resistance R_{in} represents the loading effect of the amplifier input on the signal source. It is found from

$$R_{in} \equiv \frac{v_i}{i_i}$$

and together with the resistance R_{sig} forms a voltage divider that reduces v_{sig} to the value v_i that appears at the amplifier input,

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} \quad (5.65)$$

All the amplifier circuits studied in this section are **unilateral**. That is, they do not contain internal feedback, and thus R_{in} will be independent of R_L . However, as will be seen in subsequent chapters, this is not always the case.

The second parameter in characterizing amplifier performance is the **open-circuit voltage gain** A_{vo} , defined as

$$A_{vo} \equiv \left. \frac{v_o}{v_i} \right|_{R_L = \infty}$$

The third and final parameter is the output resistance R_o . Observe from Fig. 5.44(b) that R_o is the resistance seen looking back into the amplifier output terminal with v_i set to zero. Thus R_o can be determined, at least conceptually, as indicated in Fig. 5.44(c) with

$$R_o = \frac{v_x}{i_x}$$

The controlled source $A_{vo}v_i$ and the output resistance R_o represent the Thévenin equivalent of the amplifier output circuit, and the output voltage v_o can be found from

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i \quad (5.66)$$

Thus the voltage gain of the amplifier proper, A_v , can be found as

$$\text{I} \quad A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \quad (5.67)$$

and the overall voltage gain G_v ,

$$G_v \equiv \frac{v_o}{v_{sig}}$$

can be determined by combining Eqs. (5.65) and (5.67):

$$\text{I} \quad G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_{vo} \frac{R_L}{R_L + R_o} \quad (5.68)$$

5.6.3 The Common-Source (CS) Amplifier

Of the three basic MOS amplifier configurations, the common source is the most widely used. Typically, in an amplifier formed by cascading a number of stages, the bulk of the voltage gain is obtained by using one or more common-source stages in the cascade.

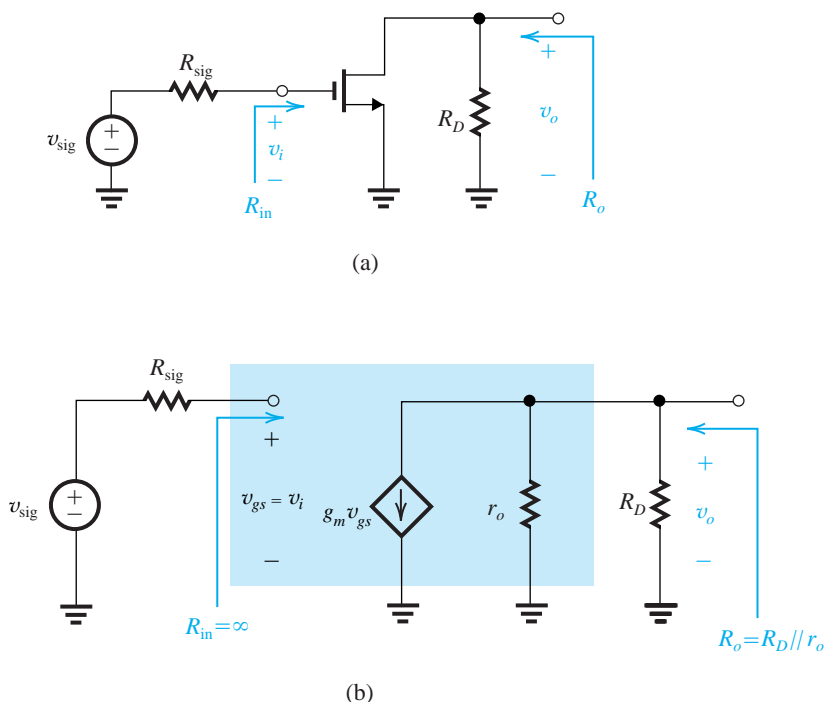


Figure 5.45 (a) Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-source amplifier with the MOSFET replaced with its hybrid- π model.

Figure 5.45(a) shows a common-source amplifier (with the biasing arrangement omitted) fed with a signal source v_{sig} having a source resistance R_{sig} . We wish to analyze this circuit to determine R_{in} , A_{v_o} , R_o , and G_v . For this purpose we shall assume that R_D is part of the amplifier; thus if a load resistance R_L is connected to the amplifier output, it appears in parallel with R_D .

Characteristic Parameters of the CS Amplifier Replacing the MOSFET with its hybrid- π model, we obtain the CS amplifier equivalent circuit shown in Fig 5.45(b). We shall use this equivalent circuit to determine the characteristic parameters R_{in} , A_{v_o} , and R_o as follows.

The input resistance R_{in} is obviously infinite,

$$R_{\text{in}} = \infty \quad (5.69)$$

The output voltage v_o is found by multiplying the current $(g_m v_{gs})$ by the total resistance between the output node and ground,

$$v_o = -(g_m v_{gs})(R_D \parallel r_o)$$

Since $v_{gs} = v_i$, the open-circuit voltage gain $A_{v_o} \equiv v_o/v_i$ can be obtained as

$$A_{v_o} = -g_m(R_D \parallel r_o) \quad (5.70)$$

Observe that the transistor output resistance r_o reduces the magnitude of the voltage gain. In discrete-circuit amplifiers, which are of interest to us in this chapter, R_D is usually much

lower than r_o and the effect of r_o on reducing $|A_{vo}|$ is slight (less than 10% or so). Thus in many cases we can neglect r_o and express A_{vo} simply as

$$A_{vo} \approx (-g_m R_D) \quad (5.71)$$

The reader is cautioned, however, that neglecting r_o is allowed only in discrete-circuit design. As will be seen in Chapter 7, r_o plays a central role in IC amplifiers.

The output resistance R_o is the resistance seen looking back into the output terminal with v_i set to zero. From Fig. 5.45(b) we see that with v_i set to zero, v_{gs} will be zero, and thus $g_m v_{gs}$ will be zero, resulting in

$$\text{I} \quad R_o = R_D \parallel r_o \quad (5.72)$$

Here, r_o has the beneficial effect of reducing the value of R_o . In discrete circuits, however, this effect is slight and we can make the approximation

$$R_o \approx R_D \quad (5.73)$$

This concludes the analysis of the CS amplifier proper. We can now make the following observations.

1. The input resistance is ideally infinite.
2. The output resistance is moderate to high (in the kilohms to tens of kilohms range). Reducing R_D to lower R_o is not a viable proposition, since the voltage gain is also reduced. Alternatively, if a low output resistance (in the ohms to tens of ohms range) is needed, a source follower stage is called for, as will be discussed in Section 5.6.6.
3. The open-circuit voltage gain A_{vo} can be high, making the CS configuration the workhorse in MOS amplifier design. Unfortunately, however, the bandwidth of the CS amplifier is severely limited. We shall study amplifier frequency response in Chapter 9.

Overall Voltage Gain To determine the overall voltage gain G_v , we first note that the infinite input resistance will make the entire signal v_{sig} appear at the amplifier input,

$$v_i = v_{sig} \quad (5.74)$$

an obviously ideal situation. At this point we should remind the reader that to maintain a reasonably linear operation, v_i and hence v_{sig} should be kept much smaller than $2V_{OV}$.

If a load resistance R_L is connected to the output terminal of the amplifier, this resistance will appear in parallel with R_D . It follows that the voltage gain A_v can be obtained by simply replacing R_D in the expression for A_{vo} in Eq. (5.70) by $R_D \parallel R_L$,

$$A_v = -g_m(R_D \parallel R_L \parallel r_o) \quad (5.75)$$

This expression together with the fact that $v_i = v_{sig}$, provides the overall voltage gain,

$$\text{I} \quad G_v = A_v = -g_m(R_D \parallel R_L \parallel r_o) \quad (5.76)$$

EXERCISE

- 5.26** Use A_{vo} in Eq. (5.70) together with R_o in Eq. (5.72) to obtain A_v . Show that the result is identical to that in Eq. (5.75).

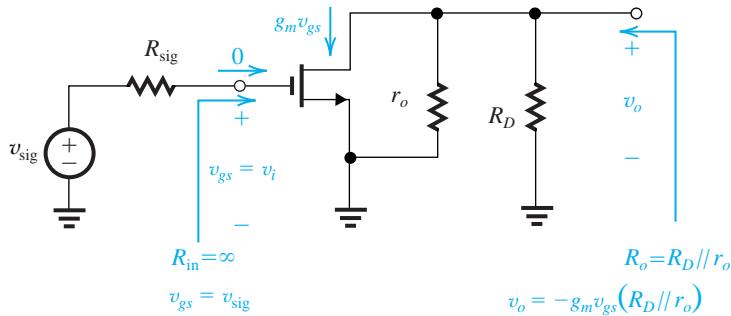


Figure 5.46 Performing the analysis directly on the circuit diagram with the MOSFET model used implicitly.

Performing the Analysis Directly on the Circuit Diagram Although small-signal, equivalent-circuit models provide a systematic process for the analysis of any amplifier circuit, the effort involved in drawing the equivalent circuit is sometimes not justified. That is, in simple situations and after a lot of practice, one can perform the small-signal analysis directly on the circuit schematic. Because in this way one remains closer to the actual circuit, the direct analysis can yield greater insight into circuit operation. Figure 5.46 shows the direct analysis of the CS amplifier. Observe that we have “pulled out” the resistance r_o from the transistor, thus making the transistor drain conduct $g_m v_{gs}$ while still accounting for the effect of r_o .

EXERCISE

5.27 A CS amplifier utilizes a MOSFET biased at $I_D = 0.25$ mA with $V_{OV} = 0.25$ V and $R_D = 20$ k Ω . The device has $V_A = 50$ V. The amplifier is fed with a source having $R_{sig} = 100$ k Ω , and a 20-k Ω load is connected to the output. Find R_{in} , A_{vo} , R_o , A_v , and G_v . If to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of $(2V_{OV})$ what is the peak of the sine-wave voltage at the output?

Ans. ∞ ; -36.4 V/V; 18.2 k Ω ; -19 V/V; -19 V/V; 0.95 V

5.6.4 The Common-Source Amplifier with a Source Resistance

It is often beneficial to insert a resistance R_s in the source lead of the common-source amplifier as shown in Fig. 5.47(a). The corresponding small-signal equivalent circuit is shown in Fig. 5.47(b), where we note that the MOSFET has been replaced with its T equivalent-circuit model. The T model is used in preference to the π model because it makes the analysis in this case somewhat simpler. In general, *whenever a resistance is connected in the source lead, the T model is preferred*. The source resistance then simply appears in series with the resistance $1/g_m$ and can be added to it.

It should be noted that we have not included r_o in the equivalent-circuit model. Including r_o would complicate the analysis considerably; r_o would connect the output node of the amplifier to the input side and thus would make the amplifier *nonunilateral*.

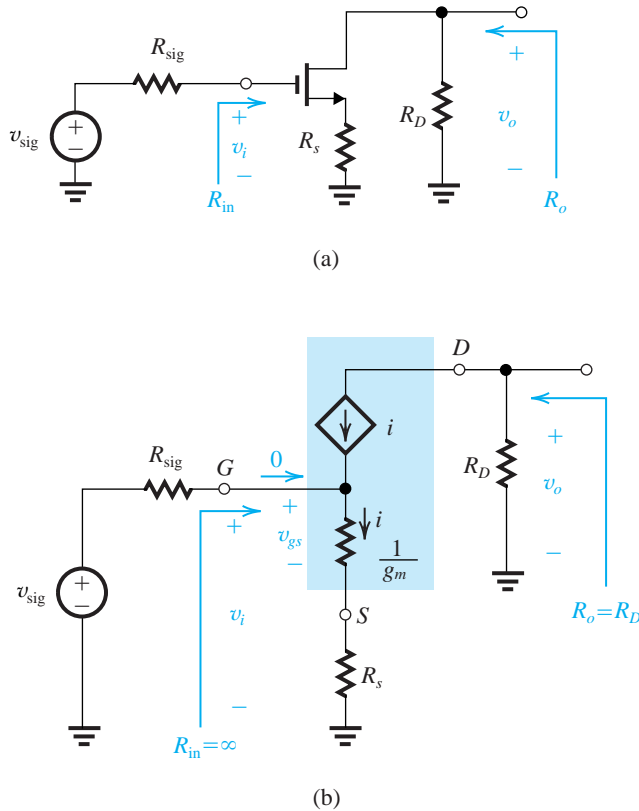


Figure 5.47 The CS amplifier with a source resistance R_s : (a) Circuit without bias details; (b) Equivalent circuit with the MOSFET represented by its T model.

Fortunately, it turns out that the effect of r_o on the operation of the discrete-circuit amplifier is not important. This can be verified by computer simulation, using for instance SPICE. This is not the case, however, for the integrated-circuit version of the circuit, where r_o plays a major role and must be taken into account, as we shall do in Chapter 7.

From Fig. 5.47(b) we see that the input resistance R_{in} is infinite and thus $v_i = v_{sig}$. Unlike the CS amplifier, however, here only a fraction of v_i appears between gate and source as v_{gs} . It can be determined from the voltage divider composed of $1/g_m$ and R_s that appears across the amplifier input, as follows:

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s} \quad (5.77)$$

Thus we can use the value of R_s to control the magnitude of the signal v_{gs} and thereby ensure that v_{gs} does not become too large and cause unacceptably high nonlinear distortion. This is the first benefit of including resistor R_s . Other benefits will be encountered in later sections and chapters. For instance, it will be shown in Chapter 9 that R_s causes the useful bandwidth of the amplifier to be extended. The mechanism by which R_s causes such improvements in amplifier performance is negative feedback. To see how R_s introduces

negative feedback, refer to Fig. 5.47(a): If while keeping v_i constant, for some reason the drain current increases, the source current also will increase, resulting in an increased voltage drop across R_s . Thus the source voltage rises, and the gate-to-source voltage decreases. The latter effect causes the drain current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 10 we shall study negative feedback formally. There we will learn that the improvements that negative feedback provides are obtained at the expense of a reduction in gain. We will now show this to be the case in the circuit of Fig. 5.47.

The output voltage v_o is obtained by multiplying the controlled-source current i by R_D ,

$$v_o = -i R_D$$

The current i in the source lead can be found by dividing v_i by the total resistance in the source,

$$i = \frac{v_i}{1/g_m + R_s} = \left(\frac{g_m}{1 + g_m R_s} \right) v_i \quad (5.78)$$

Thus, the voltage gain A_{vo} can be found as

$$A_{vo} = \frac{v_o}{v_i} = -\frac{R_D}{1/g_m + R_s} \quad (5.79) \quad \text{!}$$

which can also be expressed as

$$A_{vo} = -\frac{g_m R_D}{1 + g_m R_s} \quad (5.80) \quad \text{!}$$

Equation (5.80) indicates that including the resistance R_s reduces the voltage gain by the factor $(1 + g_m R_s)$. This is the price paid for the improvements that accrue as a result of R_s . It is interesting to note that in Chapter 10, we will find that the factor $(1 + g_m R_s)$ is the “amount of negative feedback” introduced by R_s . It is also the same factor by which bandwidth and other performance parameters improve. Because of the negative-feedback action of R_s it is known as a **source-degeneration resistance**.

There is another useful interpretation of the expression for the drain current in Eq. (5.78): The quantity between brackets on the right-hand side can be thought of as the “effective transconductance with R_s included.” Thus, including R_s reduces the transconductance by the factor $(1 + g_m R_s)$. This, of course, is simply the result of the fact that only a fraction $1/(1 + g_m R_s)$ of v_i appears as v_{gs} (see Eq. 5.77.).

The alternative gain expression in Eq. (5.79) has a powerful and insightful interpretation: The voltage gain between gate and drain is equal to the ratio of the total resistance in the drain (R_D) to the total resistance in the source ($1/g_m + R_s$),

$$\text{Voltage gain from gate to drain} = -\frac{\text{Total resistance in drain}}{\text{Total resistance in source}} \quad (5.81) \quad \text{!}$$

This is a general expression. For instance, setting $R_s = 0$ in Eq. (5.79) yields A_{vo} of the CS amplifier.

Finally, we consider the situation of a load resistance R_L connected at the output. We can obtain the gain A_v using the open-circuit voltage gain A_{vo} together with the output resistance R_o , which can be found by inspection to be

$$R_o = R_D$$

Alternatively, A_v can be obtained by simply replacing R_D in Eq. (5.79) or (5.80) by $(R_D \parallel R_L)$; thus,

$$\text{①} \quad A_v = -\frac{R_D \parallel R_L}{1/g_m + R_s} \quad (5.82)$$

or

$$\text{①} \quad A_v = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_s} \quad (5.83)$$

Observe that Eq. (5.82) is a direct application of the ratio of total resistance rule of Eq. (5.81). Finally, note that because R_{in} is infinite, $v_i = v_{sig}$ and the overall voltage gain G_v is equal to A_v .

EXERCISE

5.28 In Exercise 5.27 we applied an input signal v_{sig} of 50 mV peak and obtained an output signal of approximately 1 V peak. Assume that for some reason we now have an input signal v_{sig} that is 0.2 V peak and that we wish to modify the circuit to keep v_{gs} unchanged, and thus keep the nonlinear distortion from increasing. What value should we use for R_s ? What value of G_v will result? What will the peak signal at the output become? Assume $r_o = \infty$.

Ans. 1.5 k Ω ; -5 V/V; 1 V

5.6.5 The Common-Gate (CG) Amplifier

Figure 5.48(a) shows a common-gate amplifier with the biasing circuit omitted. The amplifier is fed with a signal source characterized by v_{sig} and R_{sig} . Since R_{sig} appears in series with the source, it is more convenient to represent the transistor with the T model than with the π model. Doing this, we obtain the amplifier equivalent circuit shown in Fig. 5.48(b). Note that we have not included r_o : This would have complicated the analysis considerably, for r_o would have appeared between the output and the input side of the amplifier. Fortunately, it

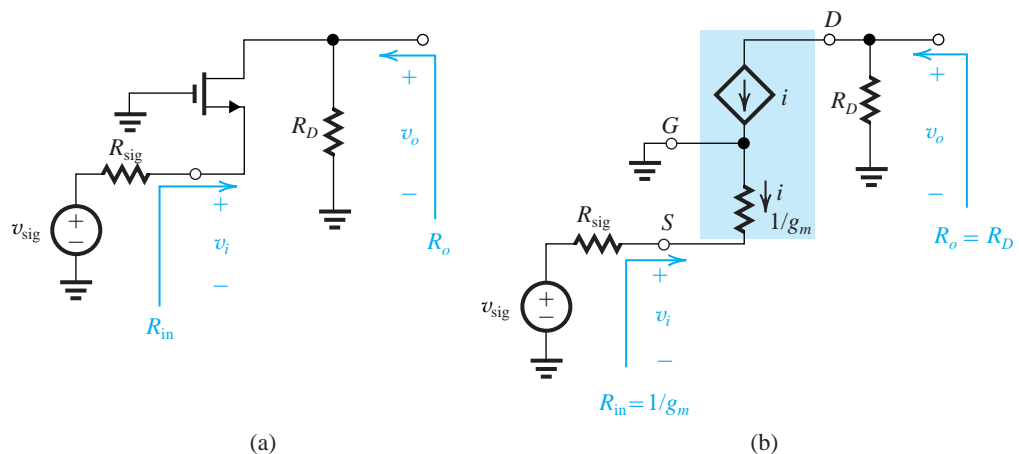


Figure 5.48 (a) Common-gate (CG) amplifier with bias arrangement omitted. (b) Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.

turns out that the effect of r_o on the performance of a discrete CG amplifier is very small. We will consider the effect of r_o when we study the IC form of the CG amplifier in Chapter 7.

From inspection of the equivalent circuit of Fig. 5.48(b), we see that the input resistance

$$R_{in} = \frac{1}{g_m} \quad (5.84)$$

This should have been expected, since we are looking into the source and the gate is grounded. Typically $1/g_m$ is a few hundred ohms; thus the CG amplifier has a low input resistance.

To determine the voltage gain A_{vo} , we write at the drain node

$$v_o = -iR_D$$

and substitute for the source current i from

$$i = -\frac{v_i}{1/g_m}$$

to obtain

$$A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D \quad (5.85)$$

which except for the positive sign is identical to the expression for A_{vo} of the CS amplifier (when r_o is neglected).

The output resistance of the CG circuit can be found by inspection of the circuit in Fig. 5.48(b) as

$$R_o = R_D \quad (5.86)$$

which is the same as in the case of the CS amplifier (with r_o neglected).

Although the gain of the CG amplifier proper has the same magnitude as that of the CS amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CG amplifier can cause the input signal to be severely attenuated. Specifically,

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{1/g_m}{1/g_m + R_{sig}} \quad (5.87)$$

from which we see that except for situations in which R_{sig} is on the order of $1/g_m$, the signal transmission factor v_i/v_{sig} can be very small and the overall voltage gain G_v can be correspondingly small. Specifically, with a resistance R_L connected at the output

$$G_v = \frac{1/g_m}{R_{sig} + 1/g_m} [g_m(R_D \parallel R_L)]$$

Thus,

$$G_v = \frac{(R_D \parallel R_L)}{R_{sig} + 1/g_m} \quad (5.88)$$

Observe that *the overall voltage gain is simply the ratio of the total resistance in the drain circuit to the total resistance in the source circuit*. If R_{sig} is of the same order as R_D and R_L , G_v will be very small.

Because of its low input resistance, the CG amplifier alone has very limited application. One such application is to amplify high-frequency signals that come from sources with relatively low resistances. These include cables, where it is usually necessary for the input

resistance of the amplifier to match the characteristic resistance of the cable. As will be shown in Chapter 9, the CG amplifier has excellent high-frequency response. Thus it can be combined with the CS amplifier in a very beneficial way that takes advantage of the best features of each of the two configurations. A very significant circuit of this kind will be studied in Chapter 7.

EXERCISE

- 5.29** A CG amplifier is required to match a signal source with $R_{\text{sig}} = 100 \Omega$. At what current I_D should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 k Ω , what overall voltage gain is realized?

Ans. 1 mA; 10 V/V

5.6.6 The Common-Drain Amplifier or Source Follower

The last of the basic MOSFET amplifier configurations is the common-drain amplifier, an important circuit that finds application in the design of both small-signal amplifiers as well as amplifiers that are required to handle large signals and deliver substantial amounts of signal power to a load. This latter variety will be studied in Chapter 11. The common drain amplifier is more commonly known as the *source follower*. The reason behind this name will become apparent shortly.

The Need for Voltage Buffers Before embarking on the analysis of the source follower, it is useful to look at one of its more common applications. Consider the situation depicted in Fig. 5.49(a). A signal source delivering a signal of reasonable strength (1 V)

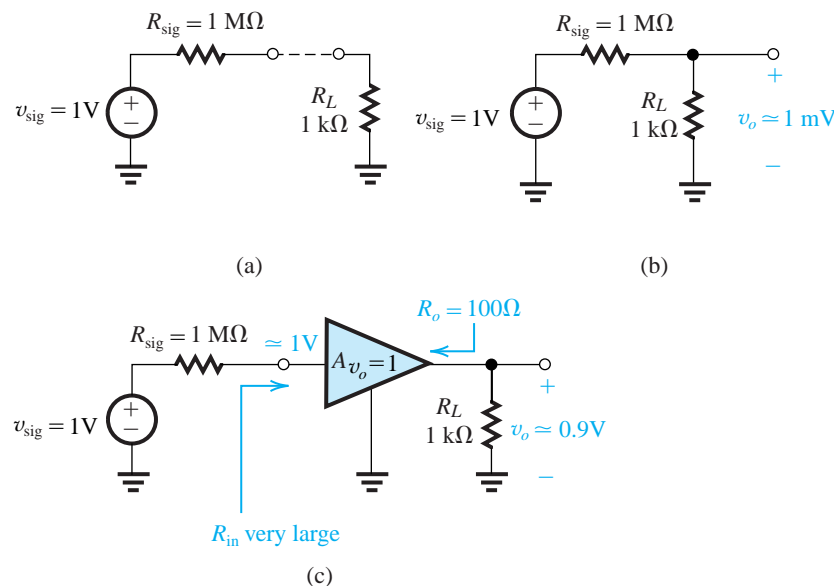


Figure 5.49 Illustrating the need for a unity-gain buffer amplifier.

with an internal resistance of $1\text{ M}\Omega$ is to be connected to a $1\text{-k}\Omega$ load resistance. Connecting the source to the load directly as in Fig. 5.49(b) would result in severe attenuation of the signal; the signal appearing across the load will be only $1/(1000 + 1)$ of the input signal or about 1 mV . An alternative course of action is suggested in Fig. 5.49(c). Here we have interposed an amplifier between the source and the load. Our amplifier, however, is unlike the amplifiers we have been studying in this chapter thus far; it has a voltage gain of only unity. This is because our signal is already of sufficient strength and we do not need to increase its amplitude. Note, however, that our amplifier has a very large input resistance, thus almost all of v_{sig} (i.e., 1 V) will appear at the input of the amplifier proper. Since the amplifier has a low output resistance ($100\ \Omega$), 90% of this signal (0.9 V) will appear at the output, obviously a very significant improvement over the situation without the amplifier. As will be seen shortly, the source follower can easily implement the unity-gain buffer amplifier shown in Fig. 5.49(c).

Characteristic Parameters of the Source Follower Figure 5.50(a) shows a source follower with the bias circuit omitted. The source follower is fed with a signal generator ($v_{\text{sig}}, R_{\text{sig}}$) and has a load resistance R_L connected between the source terminal and ground. We shall assume that R_L includes both the actual load and any other resistance that may be present between the source terminal and ground (e.g., for biasing purposes). Normally, the actual load resistance would be much lower in value than such other resistances and thus would dominate.

Since the MOSFET has a resistance R_L connected in its source terminal, it is most convenient to use the T model, as shown in Fig. 5.50(b). Note that we have included r_o , simply because it is very easy to do so. However, since r_o in effect appears in parallel with R_L , and since in discrete circuits $r_o \gg R_L$, we can neglect r_o and obtain the simplified equivalent circuit shown in Fig. 5.50(c). From the latter circuit we can write by inspection

$$R_{\text{in}} = \infty$$

and obtain A_v from the voltage divider formed by $1/g_m$ and R_L as

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} \quad (5.89) \quad \text{①}$$

Setting $R_L = \infty$ we obtain

$$A_{vo} = 1 \quad (5.90) \quad \text{①}$$

The output resistance R_o is found by setting $v_i = 0$ (i.e., by grounding the gate). Now looking back into the output terminal, excluding R_L , we simply see $1/g_m$, thus

$$R_o = 1/g_m \quad (5.91) \quad \text{①}$$

The unity open-circuit voltage gain together with R_o in Eq. (5.91) can be used to find A_v when a load resistance R_L is connected. The result is simply the expression in Eq. (5.89). Finally, because of the infinite R_{in} , $v_i = v_{\text{sig}}$, and the overall voltage gain is

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m} \quad (5.92) \quad \text{①}$$

Thus G_v will be lower than unity. However, because $1/g_m$ is usually low, the voltage gain can be close to unity. The unity open-circuit voltage gain in Eq. (5.90) indicates that the

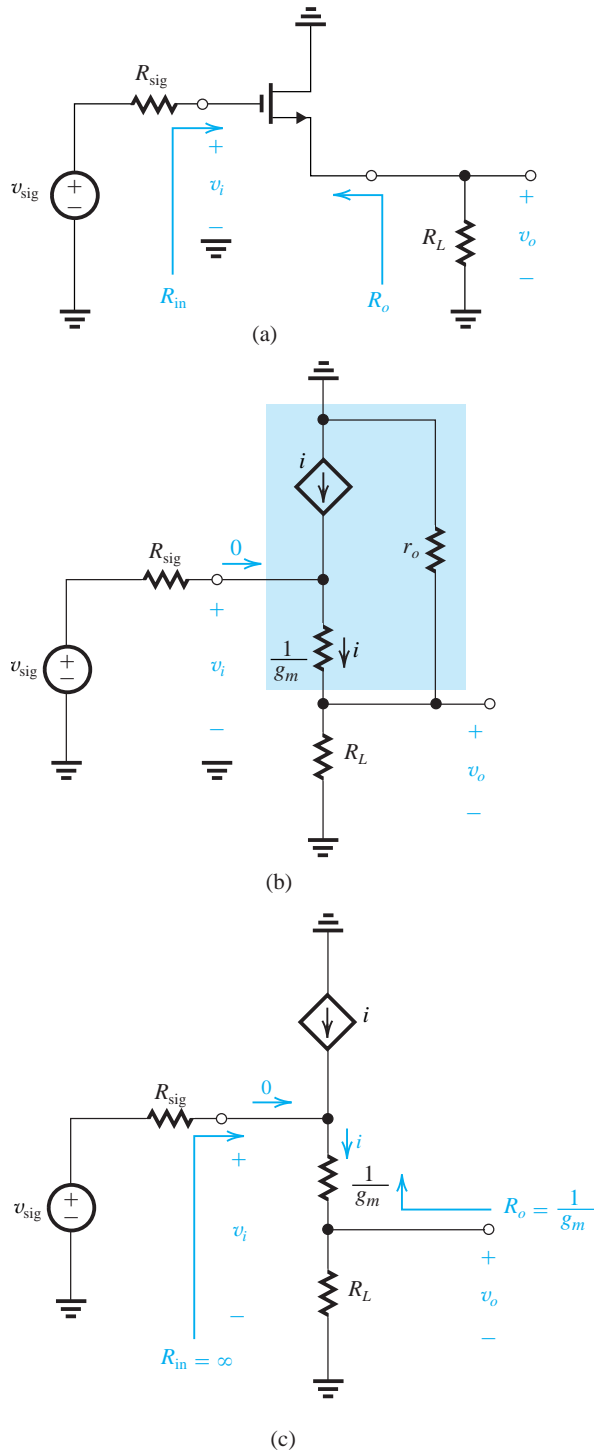


Figure 5.50 (a) Common-drain amplifier or source follower. (b) Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model. Note that r_o appears in parallel with R_L and in discrete circuits, $r_o \gg R_L$. Neglecting r_o , we obtain the simplified equivalent circuit in (c).

voltage at the source terminal will follow that at the input, hence the name *source follower*.

In conclusion, the source follower features a very high input resistance (ideally, infinite), a relatively low output resistance, and an open-circuit voltage gain that is near unity (ideally, unity). Thus the source follower is ideally suited for implementing the unity-gain voltage buffer of Fig. 5.49(c). The source follower is also used as the output (i.e., last) stage in a multistage amplifier, where its function is to equip the overall amplifier with a low output resistance, thus enabling it to supply relatively large load currents without loss of gain (i.e., with little reduction of output signal level). The design of output stages is studied in Chapter 11.

EXERCISES

D5.30 It is required to design a source follower that implements the buffer amplifier shown in Fig. 5.49(c). If the MOSFET is operated with an overdrive voltage $V_{OV} = 0.25$ V, at what drain current should it be biased? Find the output signal amplitude and the signal amplitude between gate and source.

Ans. 1.25 mA; 0.91 V; 91 mV

D5.31 A MOSFET is connected in the source-follower configuration and employed as the output stage of a cascade amplifier. It is required to provide an output resistance of $200\ \Omega$. If the MOSFET has $k'_n = 0.4$ mA/V² and is operated at $V_{OV} = 0.25$ V, find the required W/L ratio. Also specify the dc bias current I_D . If the amplifier load resistance varies over the range $1\text{ k}\Omega$ to $10\text{ k}\Omega$, what is the range of G_v of the source follower?

Ans. 50; 0.625 mA; 0.83 V/V to 0.98 V/V

5.32 Refer to Fig. 5.50(b). Show that taking r_o into account results in

$$A_{vo} = \frac{r_o}{r_o + 1/g_m}$$

Now, recalling that $r_o = V_A/I_D$ and $g_m = 2I_D/V_{OV}$, find A_{vo} in terms of V_A and V_{OV} . For a technology for which $V_A = 20$ V, what is the maximum V_{OV} at which the transistor can be operated while obtaining $A_{vo} \geq 0.99$ V/V?

Ans. $A_{vo} = 1/[1 + V_{OV}/2V_A]$; 0.4 V

5.6.7 Summary and Comparisons

For easy reference and to enable comparisons, we present in Table 5.4 the formulas for determining the characteristic parameters of discrete MOS amplifiers. Note that r_o has been neglected throughout. This is because our interest in this chapter is primarily in discrete-circuit amplifiers. As already mentioned, r_o has a relatively small effect on the performance of discrete-circuit amplifiers and can usually be neglected. In some cases, however, it is very easy to take r_o into account, such as in the case of the CS and CD amplifiers, and one is encouraged to do so. For integrated-circuit amplifiers, r_o *must* always be taken into account.

Table 5.4 Characteristics of MOSFET Amplifiers

Amplifier type	Characteristics ^{a, b}				
	R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 5.45)	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s (Fig. 5.47)	∞	$\frac{g_m R_D}{1 + g_m R_s}$	R_D	$\frac{-g_m(R_D \parallel R_L)}{1 + g_m R_s}$	$-\frac{g_m(R_D \parallel R_L)}{1 + g_m R_s}$
				$\frac{R_D \parallel R_L}{1/g_m + R_s}$	$-\frac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 5.48)	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 5.50)	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$

^a For the interpretation of R_{in} , A_{vo} , and R_o , refer to Fig. 5.44(b).

^b The MOSFET output resistance r_o has been neglected, as is permitted in the discrete-circuit amplifiers studied in this chapter. For IC amplifiers, r_o must always be taken into account.

In addition to the remarks already made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

1. The CS configuration is the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
2. Including a resistor R_s in the source lead of the CS stage provides a number of performance improvements at the expense of gain reduction.
3. The low input resistance of the CG amplifier makes it useful only in specific applications. As we shall see in Chapter 9, it has a much better high-frequency response than the CS amplifier. This superiority makes it useful as a high-frequency amplifier, especially when combined with the CS circuit. We shall see one such combination in Chapter 7.
4. The source follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multistage amplifier where its purpose is to equip the amplifier with a low output resistance.

5.7 Biasing in MOS Amplifier Circuits

As discussed in Section 5.4, an essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor. This is the step known as biasing or bias design. An appropriate dc operating point or bias point is characterized by a stable and predictable dc drain current I_D and by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels.

5.7.1 Biasing by Fixing V_{GS}

The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required⁹ to provide the desired I_D . This voltage value can be derived from the power-supply voltage V_{DD} through the use of an appropriate voltage divider. Alternatively, it can be derived from another suitable reference voltage that might be available in the system. Independent of how the voltage V_{GS} may be generated, this is *not* a good approach to biasing a MOSFET. To understand the reason for this statement, recall that

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

and note that the values of the threshold voltage V_t , the oxide-capacitance C_{ox} , and (to a lesser extent) the transistor aspect ratio W/L vary widely among devices of supposedly the same size and type. This is certainly the case for discrete devices, in which large spreads in the values of these parameters occur among devices of the same manufacturer's part number. The spread is also large in integrated circuits, especially among devices fabricated on different wafers and certainly between different batches of wafers. Furthermore, both V_t and μ_n depend on temperature, with the result that if we fix the value of V_{GS} , the drain current I_D becomes very much temperature dependent.

To emphasize the point that biasing by fixing V_{GS} is not a good technique, we show in Fig. 5.51 two i_D - v_{GS} characteristic curves representing extreme values in a batch of MOSFETs of the same type. Observe that for the fixed value of V_{GS} , the resultant spread in the values of the drain current can be substantial.

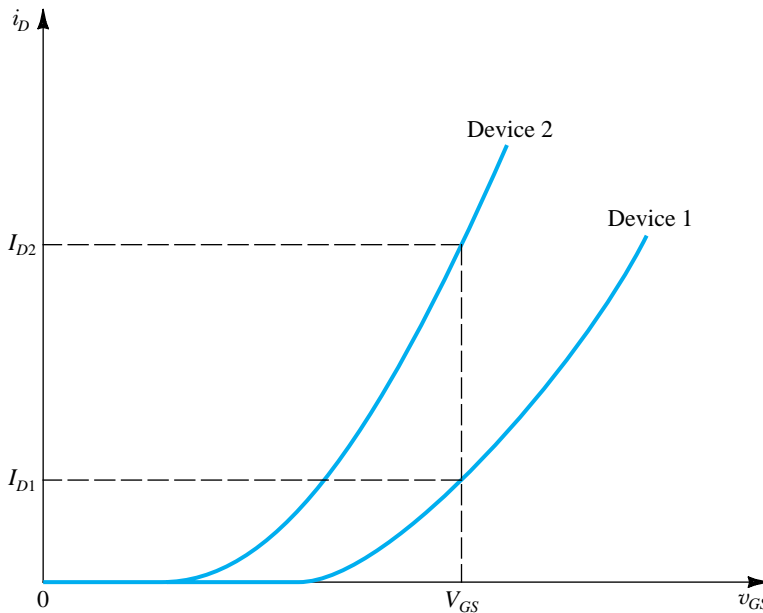


Figure 5.51 The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D . Devices 1 and 2 represent extremes among units of the same type.

⁹That is indeed what we were doing in Section 5.4. However, the amplifier circuits studied there were conceptual ones, not actual practical circuits. Our purpose in this section is to study the latter.

5.7.2 Biasing by Fixing V_G and Connecting a Resistance in the Source

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G , and connecting a resistance in the source lead, as shown in Fig. 5.52(a). For this circuit we can write

$$V_G = V_{GS} + R_S I_D \quad (5.93)$$

Now, if V_G is much greater than V_{GS} , I_D will be mostly determined by the values of V_G and R_S . However, even if V_G is not much larger than V_{GS} , resistor R_S provides *negative feedback*, which acts to stabilize the value of the bias current I_D . To see how this comes about, consider what happens when I_D increases for whatever reason. Equation (5.93) indicates that since V_G is constant, V_{GS} will have to decrease. This in turn results in a decrease in I_D , a change that is

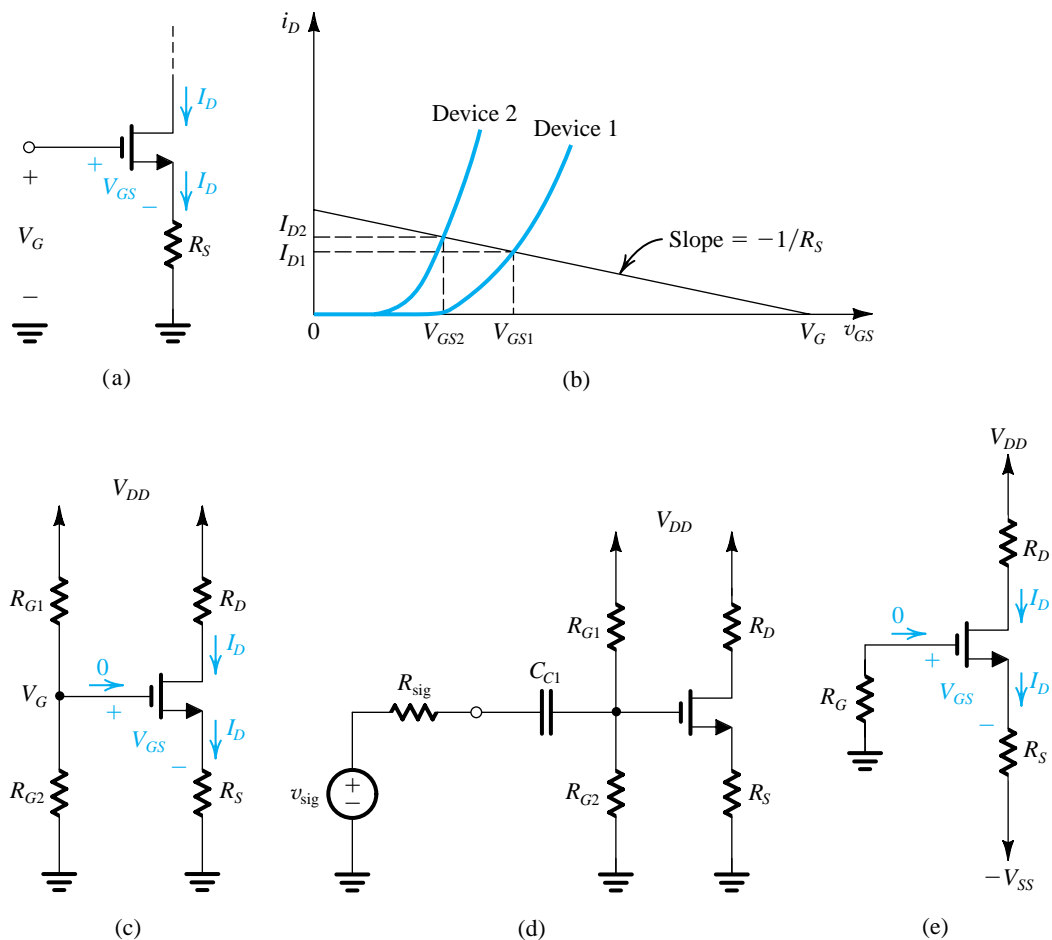


Figure 5.52 Biasing using a fixed voltage at the gate, V_G , and a resistance in the source lead, R_S : (a) basic arrangement; (b) reduced variability in I_D ; (c) practical implementation using a single supply; (d) coupling of a signal source to the gate using a capacitor C_{C1} ; (e) practical implementation using two supplies.

opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name **degeneration resistance**, a name that we will appreciate much better at a later point in this text.¹⁰

Figure 5.52(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here too we show the i_D-v_{GS} characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit—namely, Eq. (5.93). The intersection of this straight line with the i_D-v_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point. Observe that compared to the case of fixed V_{GS} , here the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_S are made larger (thus providing a bias line that is less steep).

Two possible practical discrete implementations of this bias scheme are shown in Fig. 5.52(c) and (e). The circuit in Fig. 5.52(c) utilizes one power-supply V_{DD} and derives V_G through a voltage divider (R_{G1} , R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the megohm range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor, as shown in Fig. 5.52(d). Here capacitor C_{C1} blocks dc and thus allows us to couple the signal v_{sig} to the amplifier input without disturbing the MOSFET dc bias point. The value of C_{C1} should be selected large enough to approximate a short circuit at all signal frequencies of interest. We shall study capacitively coupled MOSFET amplifiers, which are suitable only in discrete circuit design, in Section 5.8. Finally, note that in the circuit of Fig. 5.52(c), resistor R_D is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, as is often the case, the somewhat simpler bias arrangement of Fig. 5.52(e) can be utilized. This circuit is an implementation of Eq. (5.93), with V_G replaced by V_{SS} . Resistor R_G establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

Example 5.12

It is required to design the circuit of Fig. 5.52(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k'_n W/L = 1$ mA/V². For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k'_n W/L$ but $V_t = 1.5$ V.

Solution

As a rule of thumb for designing this classical biasing circuit, we choose R_D and R_S to provide one-third of the power-supply voltage V_{DD} as a drop across each of R_D , the transistor (i.e., V_{DS}) and R_S . For $V_{DD} = 15$ V,

¹⁰The action of R_S in stabilizing the value of the bias current I_D is not unlike that of the resistance R_s , which we included in the source lead of a CS amplifier in Section 5.6.4. In the latter case also, R_s works to reduce the change in i_D with the result that the amplifier gain is reduced.

Example 5.12 *continued*

this choice makes $V_D = +10$ V and $V_S = +5$ V. Now, since I_D is required to be 0.5 mA, we can find the values of R_D and R_S as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10 \text{ k}\Omega$$

$$R_S = \frac{V_S}{I_D} = \frac{5}{0.5} = 10 \text{ k}\Omega$$

The required value of V_{GS} can be determined by first calculating the overdrive voltage V_{OV} from

$$I_D = \frac{1}{2} k_n' (W/L) V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

which yields $V_{OV} = 1$ V, and thus,

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2 \text{ V}$$

Now, since $V_S = +5$ V, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7 \text{ V}$$

To establish this voltage at the gate we may select $R_{G1} = 8 \text{ M}\Omega$ and $R_{G2} = 7 \text{ M}\Omega$. The final circuit is shown in Fig. 5.53. Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to V_{DD}) and a negative signal swing of -4 V [i.e., down to $(V_G - V_t)$].

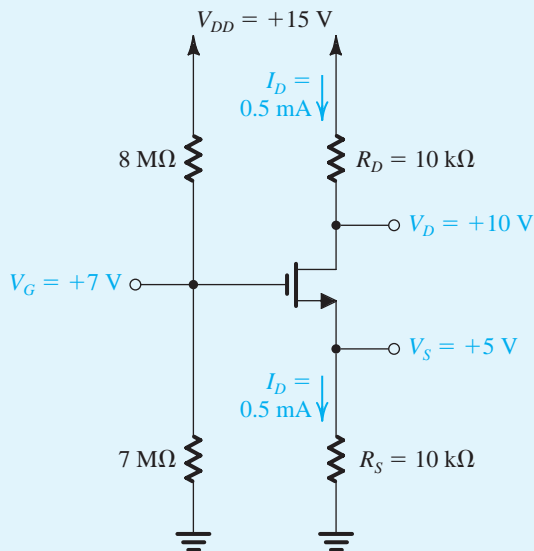


Figure 5.53 Circuit for Example 5.12.

If the NMOS transistor is replaced with another having $V_t = 1.5$ V, the new value of I_D can be found as follows:

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad (5.94)$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10I_D \quad (5.95)$$

Solving Eqs. (5.94) and (5.95) together yields

$$I_D = 0.455 \text{ mA}$$

Thus the change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is $\frac{-0.045}{0.5} \times 100 = -9\%$ change.

EXERCISES

5.33 Consider the MOSFET in Example 5.12 when fixed- V_{GS} bias is used. Find the required value of V_{GS} to establish a dc bias current $I_D = 0.5$ mA. Recall that the device parameters are $V_t = 1$ V, $k'_n W/L = 1$ mA/V², and $\lambda = 0$. What is the percentage change in I_D obtained when the transistor is replaced with another having $V_t = 1.5$ V?

Ans. $V_{GS} = 2$ V; -75%

D5.34 Design the circuit of Fig. 5.52(e) to operate at a dc drain current of 0.5 mA and $V_D = +2$ V. Let $V_t = 1$ V, $k'_n W/L = 1$ mA/V², $\lambda = 0$, $V_{DD} = V_{SS} = 5$ V. Use standard 5% resistor values (see Appendix G), and give the resulting values of I_D , V_D , and V_S .

Ans. $R_D = R_S = 6.2$ k Ω ; $I_D = 0.49$ mA, $V_S = -1.96$ V, and $V_D = +1.96$ V. R_G can be selected in the range of 1 M Ω to 10 M Ω .

5.7.3 Biasing Using a Drain-to-Gate Feedback Resistor

A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 5.54. Here the large feedback resistance R_G (usually in the megohm range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D \quad (5.96)$$

which is identical in form to Eq. (5.93), which describes the operation of the bias scheme discussed above [that in Fig. 5.52(a)]. Thus, here too, if I_D for some reason changes, say increases, then Eq. (5.96) indicates that V_{GS} must decrease. The decrease in V_{GS} in turn causes a decrease in I_D , a change that is opposite in direction to the one originally assumed. Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

The circuit of Fig. 5.54 can be utilized as an amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The amplified output signal at the drain can be coupled to another part of the circuit, again via a capacitor. We have considered such an amplifier circuit in Section 5.5 (Example 5.10).

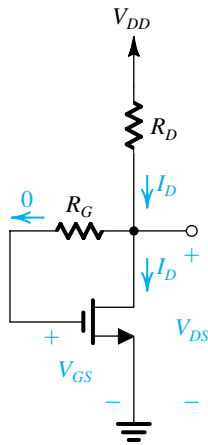


Figure 5.54 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G .

EXERCISE

D5.35 Design the circuit in Fig. 5.54 to operate at a dc drain current of 0.5 mA. Assume $V_{DD} = +5$ V, $k'_n W/L = 1$ mA/V², $V_t = 1$ V, and $\lambda = 0$. Use a standard 5% resistance value for R_D , and give the actual values obtained for I_D and V_D .

Ans. $R_D = 6.2$ k Ω ; $I_D \approx 0.49$ mA; $V_D \approx 1.96$ V

5.7.4 Biasing Using a Constant-Current Source

The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source. Figure 5.55(a) shows such an arrangement applied to a discrete MOSFET. Here R_G (usually in the megohm range) establishes a dc ground at the gate and presents a large resistance to an input signal source that can be capacitively coupled to the gate. Resistor R_D establishes an appropriate dc voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region.

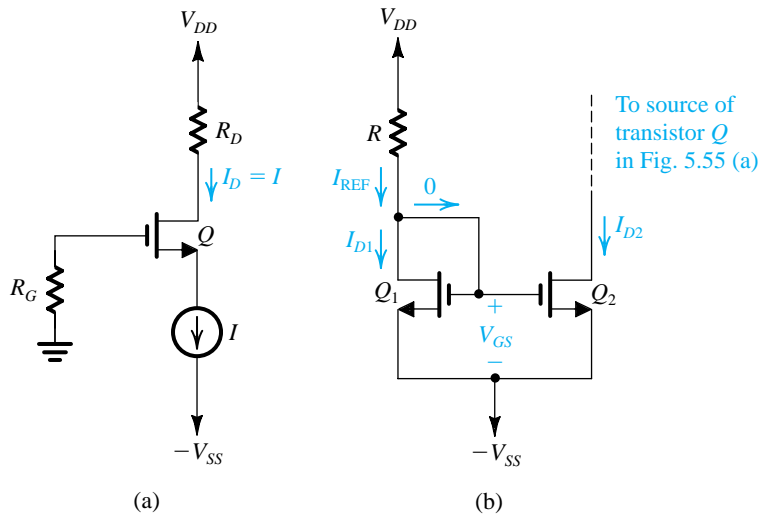


Figure 5.55 (a) Biasing the MOSFET using a constant-current source I . (b) Implementation of the constant-current source I using a current mirror.

A circuit for implementing the constant-current source I is shown in Fig. 5.55(b). The heart of the circuit is transistor Q_1 , whose drain is shorted to its gate, and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2}k'_n \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2 \quad (5.97)$$

where we have neglected channel-length modulation (i.e., assumed $\lambda = 0$). The drain current of Q_1 is supplied by V_{DD} through resistor R . Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} \quad (5.98)$$

where the current through R is considered to be the *reference current* of the current source and is denoted I_{REF} . Given the parameter values of Q_1 and a desired value for I_{REF} , Eqs. (5.97) and (5.98) can be used to determine the value of R . Now consider transistor Q_2 : It has the same V_{GS} as Q_1 ; thus if we assume that it is operating in saturation, its drain current, which is the desired current I of the current source, will be

$$I = I_{D2} = \frac{1}{2}k'_n \left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \quad (5.99)$$

where we have neglected channel-length modulation. Equations (5.98) and (5.99) enable us to relate the current I to the reference current I_{REF} ,

$$I = I_{REF} \frac{(W/L)_2}{(W/L)_1} \quad (5.100) \quad \text{!}$$

Thus I is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2 . This circuit, known as a **current mirror**, is very popular in the design of IC MOS amplifiers and will be studied in great detail in Chapter 7.

EXERCISE

D5.36 Using two transistors Q_1 and Q_2 having equal lengths but widths related by $W_2/W_1 = 5$, design the circuit of Fig. 5.55(b) to obtain $I = 0.5$ mA. Let $V_{DD} = -V_{SS} = 5$ V, $k'_n(W/L)_1 = 0.8$ mA/V², $V_t = 1$ V, and $\lambda = 0$. Find the required value for R . What is the voltage at the gates of Q_1 and Q_2 ? What is the lowest voltage allowed at the drain of Q_2 while Q_2 remains in the saturation region?

Ans. 85 k Ω ; -3.5 V; -4.5 V

5.7.5 A Final Remark

The bias circuits studied in this section are intended for discrete-circuit applications. The only exception is the current mirror circuit of Fig. 5.55(b) which, as mentioned above, is extensively used in IC design. Bias arrangements for IC MOS amplifiers will be studied in Chapter 7.

5.8 Discrete-Circuit MOS Amplifiers

With our study of MOS amplifier basics complete, we now put everything together by presenting practical circuits for discrete-circuit amplifiers. These circuits, which utilize the amplifier configurations studied in Section 5.6 and one of the biasing methods of Section 5.7, can be assembled using off-the-shelf discrete transistors, resistors, and capacitors. Though practical and carefully selected to illustrate some important points, the circuits presented in this section should be regarded only as examples of discrete-circuit MOS amplifiers. Indeed, there is a great variety of such circuits, a number of which are explored in the end-of-chapter problems. We should, however, caution the reader that MOS transistors are primarily used in integrated circuit design, as we shall see in Chapter 7 and beyond.

In this section we present a series of exercise problems, Exercises 5.37 to 5.41, that are carefully designed to illustrate important aspects of the amplifier circuits studied. These exercises are also intended to enable the reader to see more clearly the differences between the various circuit configurations. We strongly urge the reader to solve these exercises. As usual, the answers are provided.

5.8.1 The Basic Structure

Figure 5.56 shows the basic circuit we shall utilize to implement the various configurations of discrete-circuit MOS amplifiers. Among the various schemes for biasing MOS amplifiers (Section 5.7), we have selected, for both its effectiveness and its simplicity, the one employing constant-current biasing. Figure 5.56 indicates the dc current and the dc voltages resulting at various nodes.

EXERCISE

5.37 Consider the circuit of Fig. 5.56 for the case $V_{DD} = V_{SS} = 10$ V, $I = 0.5$ mA, $R_G = 4.7$ M Ω , $R_D = 15$ k Ω , $V_t = 1.5$ V, and $k'_n(W/L) = 1$ mA/V². Find V_{OV} , V_{GS} , V_G , V_S , and V_D . Also, calculate the values of g_m and r_o , assuming that $V_A = 75$ V. What is the maximum possible signal swing at the drain for which the MOSFET remains in saturation?

Ans. See Fig. E5.37; without taking into account the signal swing at the gate, the drain can swing to -1.5 V, a negative signal swing of 4 V

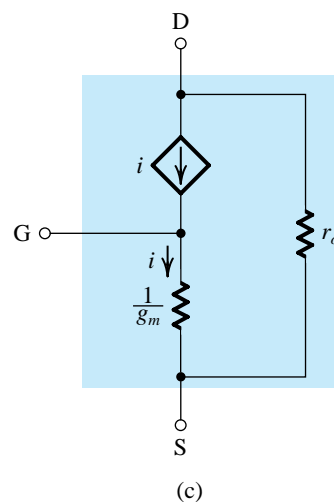
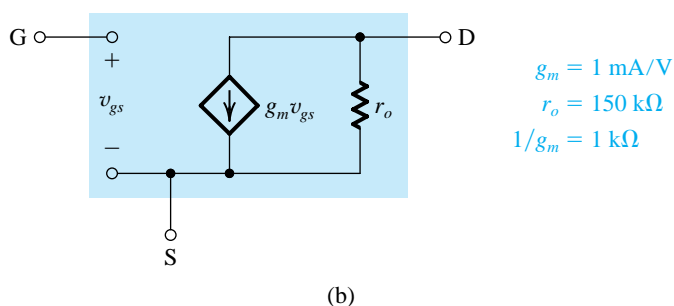
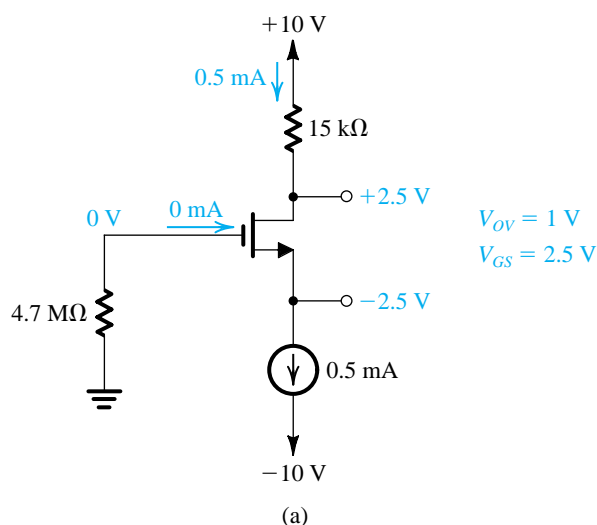


Figure E5.37

5.8.2 The Common-Source (CS) Amplifier

As mentioned in Section 5.6, the common-source (CS) configuration is the most widely used of all MOSFET amplifier circuits. A common-source amplifier realized using the circuit of Fig. 5.56 is shown in Fig. 5.57(a). Observe that to establish a **signal ground**, or an **ac ground** as it is sometimes called, at the source, we have connected a large capacitor, C_S , between the source and ground. This capacitor, usually in the microfarad range, is required to provide a very small impedance (ideally, zero impedance; i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the signal current passes through C_S to ground and thus *bypasses* the output resistance of current source I (and any other circuit component that might be connected to the MOSFET source); hence, C_S is called a **bypass capacitor**. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 9.1. For our purposes here we shall assume that C_S is acting as a perfect short circuit and thus is establishing a zero signal voltage at the MOSFET source.

In order not to disturb the dc bias current and voltages, the signal to be amplified, shown as voltage source v_{sig} with an internal resistance R_{sig} , is connected to the gate through a large capacitor C_{C1} . Capacitor C_{C1} , known as a **coupling capacitor**, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again, we note that as the signal frequency is lowered, the impedance of C_{C1} (i.e., $1/j\omega C_{C1}$) will increase and its effectiveness as a coupling capacitor will be correspondingly reduced. This problem too will be considered in Section 9.1 when the dependence of the amplifier operation on frequency is studied. For our purposes here we shall assume C_{C1} is acting as a perfect short circuit as far as the signal is concerned. Before leaving C_{C1} , we should point out that when the signal source can provide an appropriate dc path to ground, the gate can be connected directly to the signal source and both R_G and C_{C1} can be dispensed with.

The voltage signal resulting at the drain is coupled to the load resistance R_L via another coupling capacitor C_{C2} . We shall assume that C_{C2} acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage $v_o = v_d$. Note that R_L can be either an actual load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of another amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 8.)

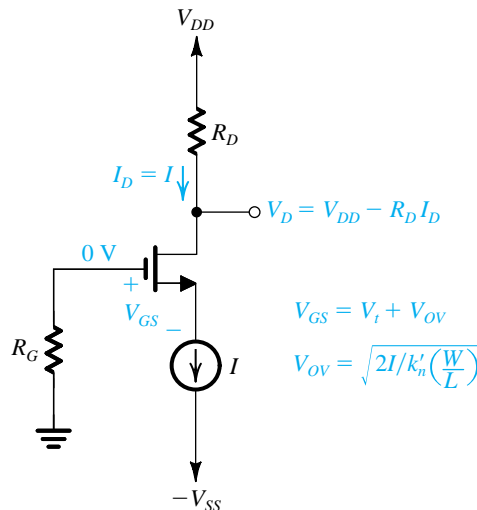


Figure 5.56 Basic structure of the circuit used to realize single-stage, discrete-circuit MOS amplifier configurations.

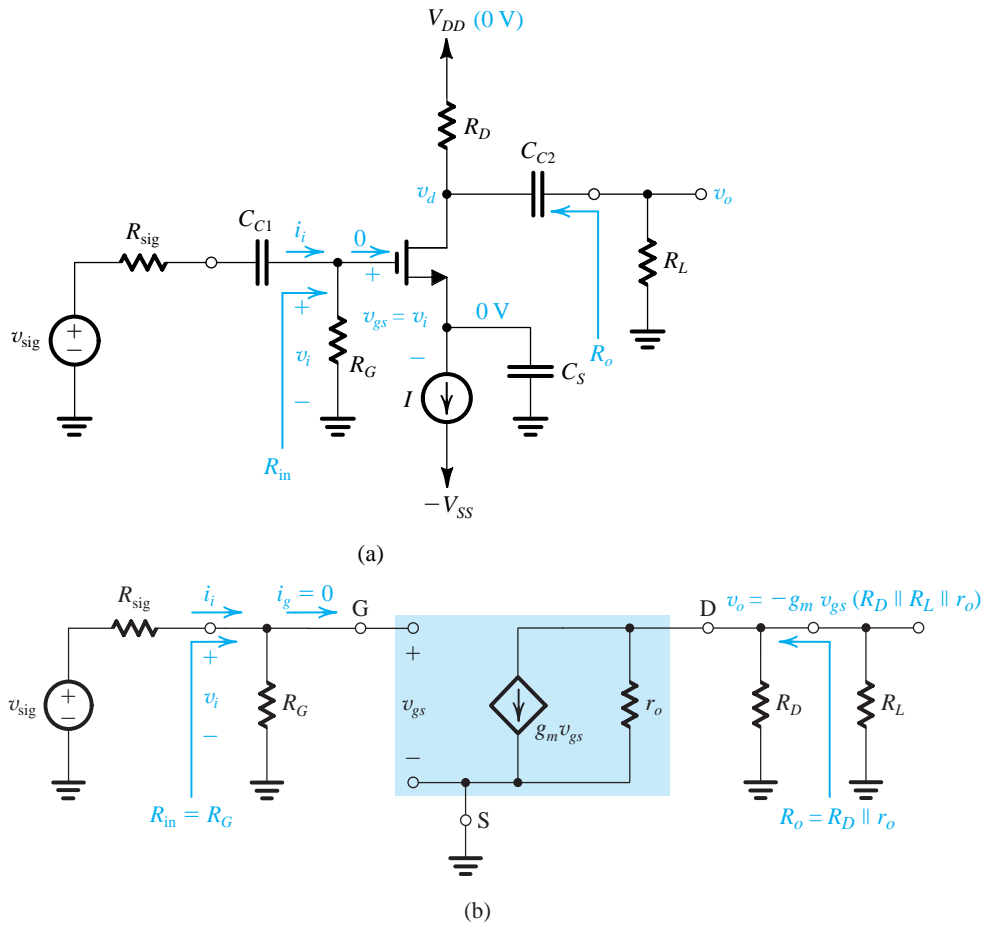


Figure 5.57 (a) Common-source amplifier based on the circuit of Fig. 5.56. (b) Equivalent circuit of the amplifier for small-signal analysis.

To determine the terminal characteristics of the CS amplifier—that is, its input resistance, voltage gain, and output resistance—we replace the MOSFET with its small-signal model. The resulting circuit is shown in Fig. 5.57(b).

We observe that the only difference between this circuit and the stripped-down version studied in Section 5.6.3 (Fig. 5.45) is that here we have the bias resistance R_G . Since R_G appears across the input terminals of the amplifier, the input resistance will no longer be infinite, rather

$$R_{in} = R_G$$

To keep R_{in} high, a large value of R_G (in the megohm range) is usually selected. The finite R_{in} will affect the overall voltage gain G_v which becomes

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L \parallel r_o) \quad (5.101)$$

Finally, to encourage the reader to do the analysis directly on the circuit diagram, with the MOSFET model used implicitly, we show some of the analysis on the circuit in Fig. 5.57(a).

EXERCISE

- 5.38** Consider a CS amplifier based on the circuit analyzed in Exercise 5.37. Specifically, refer to the results of that exercise shown in Fig. E5.37. Find R_{in} , A_{v_o} , and R_o , both without and with r_o taken into account. Then calculate the overall voltage gain G_v , with r_o taken into account, for the case $R_{sig} = 100\text{ k}\Omega$ and $R_L = 15\text{ k}\Omega$. If v_{sig} is a 0.4-V peak-to-peak sinusoid, what output signal v_o results?
- Ans.** Without r_o : $R_{in} = 4.7\text{ M}\Omega$, $A_{v_o} = -15\text{ V/V}$, and $R_o = 15\text{ k}\Omega$; with r_o : $R_{in} = 4.7\text{ M}\Omega$, $A_{v_o} = -13.6\text{ V/V}$, and $R_o = 13.6\text{ k}\Omega$; $G_v = -7\text{ V/V}$; v_o is a 2.8-V peak-to-peak sinusoid superimposed on a dc drain voltage of +2.5 V.

5.8.3 The Common-Source Amplifier with a Source Resistance

As demonstrated in Section 5.6.4, a number of beneficial results can be obtained by connecting a resistance R_s in the source lead of the transistor in the CS amplifier. This is shown in Fig. 5.58(a), where R_s is, of course, unbypassed. Figure 5.58(b) shows the small-signal equivalent-circuit model. Observe that the only difference between this circuit and the simplified version studied in Section 5.6.4 is the bias resistance R_G that appears across the input terminals and makes R_{in} finite. This will in turn affect the overall voltage gain G_v , which becomes

$$G_v = -\frac{R_G}{R_G + R_{sig}} \frac{R_D \parallel R_L}{1/g_m + R_s} \quad (5.102)$$

Finally, note that much of the analysis is shown both on the actual circuit in Fig. 5.58(a) and on the equivalent circuit in Fig. 5.58(b).

EXERCISE

- 5.39** In Exercise 5.38 we applied an input signal of 0.4 V peak-to-peak, which resulted in an output signal of the CS amplifier of 2.8 V peak-to-peak. Assume that for some reason we now have an input signal three times as large as before (i.e., 1.2 V p-p) and that we wish to modify the circuit to keep the output signal level unchanged. What value should we use for R_s ?
- Ans.** 2.15 k Ω

5.8.4 The Common-Gate (CG) Amplifier

Figure 5.59(a) shows a CG amplifier obtained from the circuit of Fig. 5.56. Observe that since both the dc and ac voltages at the gate are to be zero, we have connected the gate directly to ground, thus eliminating resistor R_G altogether. Coupling capacitors C_{c1} and C_{c2} perform similar functions to those in the CS circuit.

The small-signal, equivalent circuit model of the CG amplifier is shown in Fig. 5.59(b). We note that this circuit is identical to the equivalent circuit of the stripped-down version of the CG amplifier, in Fig. 5.48(b). Thus the analysis performed and the results obtained in Section 5.6.5 apply directly here. A substantial portion of the analysis is also shown in Fig. 5.59.

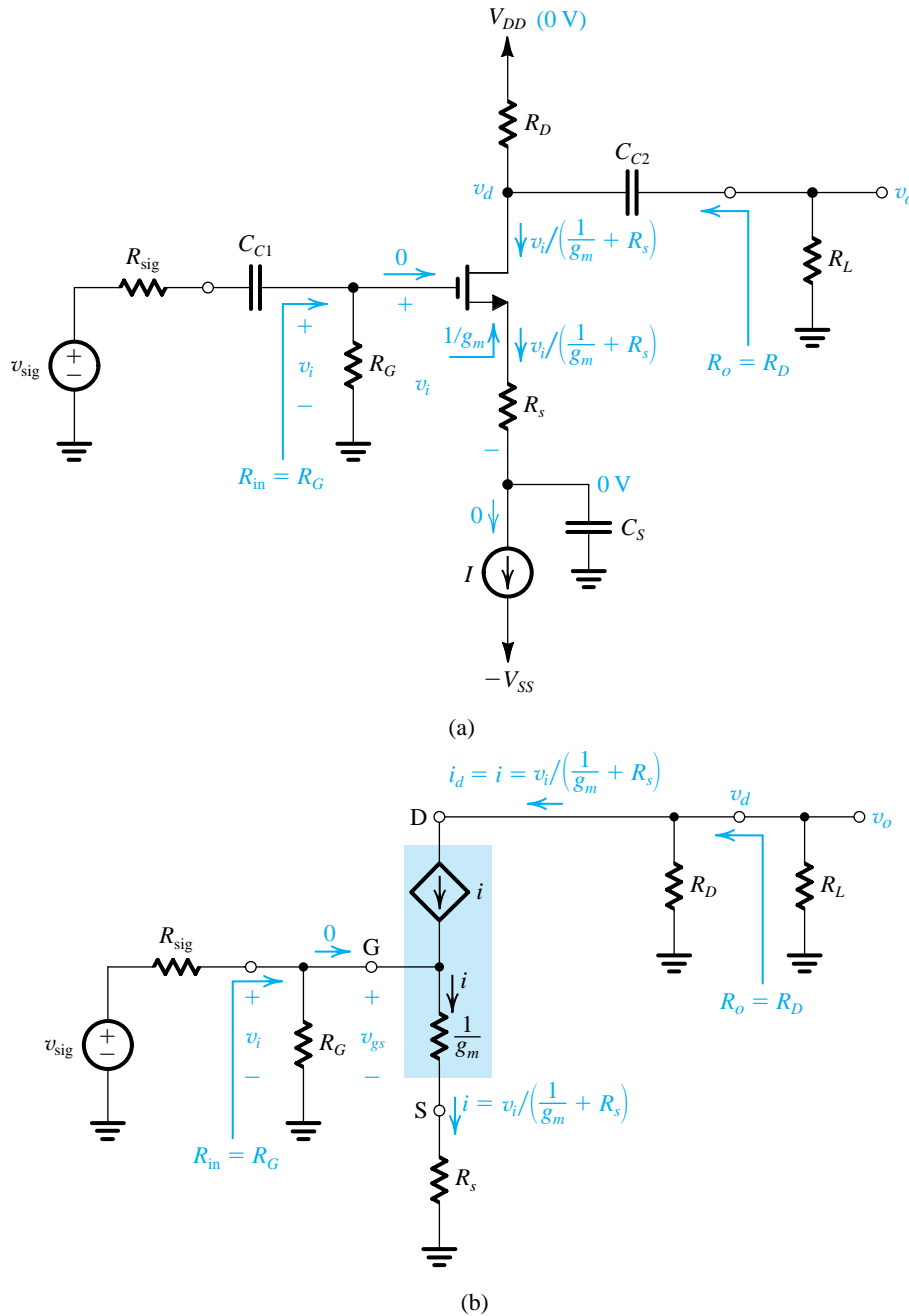
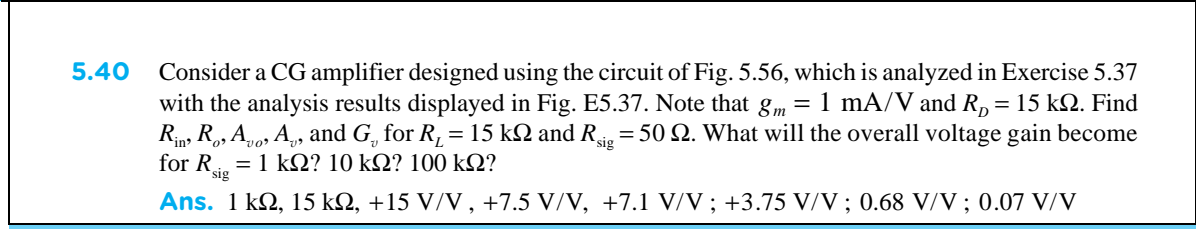


Figure 5.58 (a) Common-source amplifier with a resistance R_s in the source lead. (b) Small-signal equivalent circuit with r_o neglected.



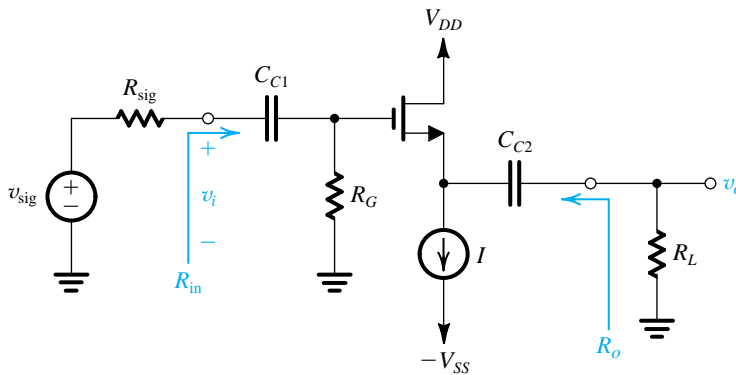
Ans. 1 k Ω , 15 k Ω , +15 V/V, +7.5 V/V, +7.1 V/V; +3.75 V/V; 0.68 V/V; 0.07 V/V

5.8.5 The Source Follower

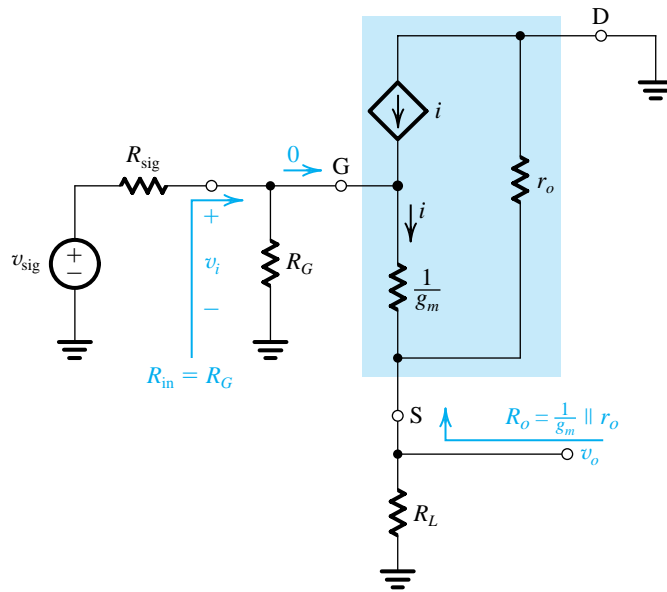
Figure 5.60(a) shows a common-drain amplifier based on the circuit of Fig. 5.56. Since the drain is to function as a signal ground, there is no need for resistor R_D , and it has therefore been eliminated. The input signal is coupled via capacitor C_{C1} to the MOSFET gate, and the output signal at the MOSFET source is coupled via capacitor C_{C2} to a load resistor R_L .

Replacing the MOSFET with its T model results in the equivalent circuit in Fig. 5.60(b). We note that the only difference between this circuit and that in Fig. 5.50(b) is the bias resistance R_G that appears across the input terminals. Thus, here too, the input resistance will no longer be infinite and the overall voltage gain will become

$$G_v = \frac{R_G}{R_G + R_{\text{sig}}} \frac{(R_L \parallel r_o)}{(R_L \parallel r_o) + 1/g_m} \quad (5.103)$$



(a)



(b)

Figure 5.60 (a) A source-follower amplifier. (b) Small-signal, equivalent-circuit model.

EXERCISE

5.41 Consider a source follower such as that in Fig. 5.60(a) designed on the basis of the circuit of Fig. 5.56, the results of whose analysis are displayed in Fig. E5.37. Specifically, note that $g_m = 1 \text{ mA/V}$ and $r_o = 150 \text{ k}\Omega$. Let $R_{\text{sig}} = 1 \text{ M}\Omega$ and $R_L = 15 \text{ k}\Omega$. (a) Find R_{in} , $A_{v_{\text{no}}}$, A_v , and R_o without and with r_o taken into account. (b) Find the overall small-signal voltage gain G_v with r_o taken into account.

Ans. (a) $R_{\text{in}} = 4.7 \text{ M}\Omega$; $A_{v_{\text{no}}} = 1 \text{ V/V}$ (without r_o), 0.993 V/V (with r_o); $A_v = 0.938$ (without r_o), 0.932 V (with r_o); $R_o = 1 \text{ k}\Omega$ (without r_o), $0.993 \text{ k}\Omega$ (with r_o); (b) 0.768 V/V

5.8.6 The Amplifier Frequency Response

Thus far, we have assumed that the gain of MOS amplifiers is constant, independent of the frequency of the input signal. This would imply that MOS amplifiers have infinite bandwidth, which of course is not true. To illustrate, we show in Fig. 5.61 a sketch of the magnitude of the gain of a common-source amplifier versus frequency. Observe that there is indeed a wide frequency range over which the gain remains almost constant. This obviously is the useful frequency range of operation for the particular amplifier. Thus far, we have been assuming that our amplifiers are operating in this frequency band, called **the midband**.

Figure 5.61 indicates that at lower frequencies, the magnitude of amplifier gain falls off. This is because the coupling and bypass capacitors no longer have low impedances. Recall that we assumed that their impedances were small enough to act as short circuits. Although this can be true at midband frequencies, as the frequency of the input signal is lowered, the reactance $1/j\omega C$ of each of these capacitors becomes significant, and it can be shown that this results in the overall voltage gain of the amplifier decreasing.

Figure 5.61 indicates also that the gain of the amplifier falls off at the high-frequency end. This is due to the internal capacitive effects in the MOSFET. We have had a brief introduction to such capacitive effects in our study of the *pn* junction in Chapter 3. In Chapter 9, we shall study the internal capacitive effects of the MOSFET and will augment the hybrid- π model with capacitances that model these effects.

We will undertake a detailed study of the frequency response of MOS amplifiers in Chapter 9. For the time being, however, it is important for the reader to realize that for every MOS amplifier there is a finite band over which the gain is almost constant. The boundaries of this useful frequency band or midband, are the two frequencies f_L and f_H , at which the gain drops by a certain number of decibels (usually 3 dB) below its value at midband. As indicated in Fig. 5.61, the **amplifier bandwidth**, or 3-dB bandwidth, is defined as the difference between the lower (f_L) and the upper or higher (f_H) 3-dB frequencies:

$$BW = f_H - f_L \quad (5.104)$$

and since usually $f_L \ll f_H$,

$$BW \simeq f_H \quad (5.105)$$

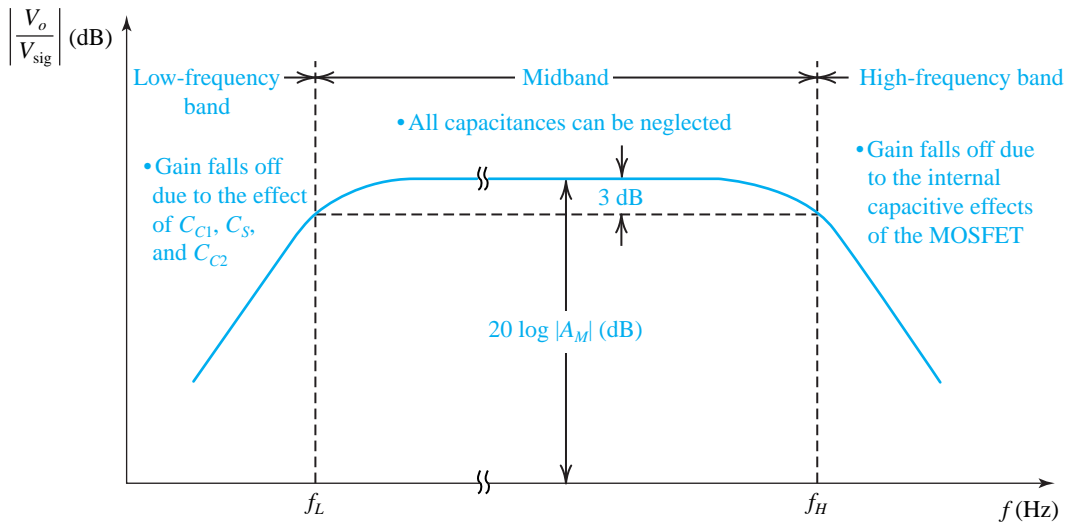


Figure 5.61 A sketch of the frequency response of a CS amplifier delineating the three frequency bands of interest.

A figure of merit for the amplifier is its gain–bandwidth product, defined as

$$GB = |A_M| BW \quad (5.106)$$

where $|A_M|$ is the magnitude of the amplifier gain in the midband. It will be seen in Chapter 9 that in amplifier design it is usually possible to trade off gain for bandwidth. One way to accomplish this, for instance, is by including resistance R_s in the source of the CS amplifier.

5.9 The Body Effect and Other Topics¹¹



In this section we briefly consider a number of important though secondary issues.

5.9.1 The Role of the Substrate—The Body Effect

In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the pn junction between the substrate and the induced channel (review Fig. 5.5) having a constant zero (cutoff) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the cutoff condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in an n -channel device) will have an effect on device operation. To appreciate this fact, consider an NMOS transistor and let its substrate be made negative relative to the

¹¹This section can be omitted in a first reading with little or no loss of continuity. Some of this material, however, will be required for the study of digital circuits in Chapter 13.

source. The reverse-bias voltage will widen the depletion region (refer to Fig. 5.2). This in turn reduces the channel depth. To return the channel to its former state, v_{GS} has to be increased.

The effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_t . Specifically, it has been shown that increasing the reverse substrate bias voltage V_{SB} results in an increase in V_t according to the relationship

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}] \quad (5.107)$$

where V_{t0} is the threshold voltage for $V_{SB} = 0$; ϕ_f is a physical parameter with $(2\phi_f)$ typically 0.6 V; γ is a fabrication-process parameter given by

$$\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \quad (5.108)$$

where q is the electron charge (1.6×10^{-19} C), N_A is the doping concentration of the p -type substrate, and ϵ_s is the permittivity of silicon ($11.7\epsilon_0 = 11.7 \times 8.854 \times 10^{-14} = 1.04 \times 10^{-12}$ F/cm). The parameter γ has the dimension of \sqrt{V} and is typically $0.4 \text{ V}^{1/2}$. Finally, note that Eq. (5.107) applies equally well for p -channel devices with V_{SB} replaced by the reverse bias of the substrate, V_{BS} (or, alternatively, replace V_{SB} by $|V_{SB}|$) and note that γ is negative. Also, in evaluating γ , N_A must be replaced with N_D , the doping concentration of the n well in which the PMOS is formed. For p -channel devices, $2\phi_f$ is typically 0.75 V, and γ is typically $-0.5 \text{ V}^{1/2}$.

EXERCISE

5.42 An NMOS transistor has $V_{t0} = 0.8 \text{ V}$, $2\phi_f = 0.7 \text{ V}$, and $\gamma = 0.4 \text{ V}^{1/2}$. Find V_t when $V_{SB} = 3 \text{ V}$.

Ans. 1.23 V

Equation (5.107) indicates that an incremental change in V_{SB} gives rise to an incremental change in V_t , which in turn results in an incremental change in i_D even though v_{GS} might have been kept constant. It follows that the body voltage controls i_D ; thus the body acts as another gate for the MOSFET, a phenomenon known as the **body effect**. Here we note that the parameter γ is known as the **body-effect parameter**.

5.9.2 Modeling the Body Effect

As mentioned above the body effect occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most negative power supply in the integrated circuit for n -channel devices and to the most positive for p -channel devices). Thus the substrate (body) will be at signal ground, but since the source is not, a signal voltage v_{bs} develops between the body (B) and the source (S). The substrate then acts as a “second gate” or a **backgate** for the MOSFET. Thus the signal v_{bs} gives rise to a drain-current component, which we shall write as $g_{mb}v_{bs}$, where g_{mb} is the **body transconductance**, defined as

$$g_{mb} \equiv \left. \frac{\partial i_D}{\partial v_{BS}} \right|_{v_{GS} = \text{constant}} \quad (5.109)$$

Recalling that i_D depends on v_{BS} through the dependence of V_t on V_{BS} , we can show that

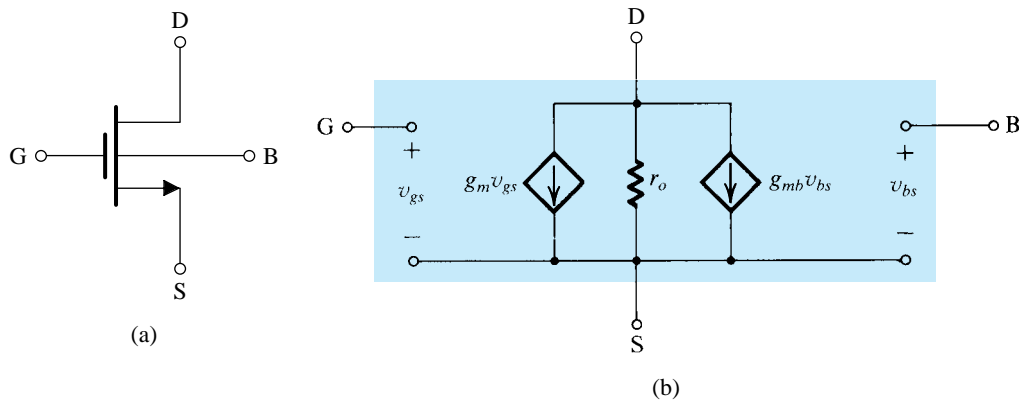


Figure 5.62 Small-signal, equivalent-circuit model of a MOSFET in which the source is not connected to the body.

$$g_{mb} = \chi g_m \quad (5.110)$$

where

$$\chi \equiv \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} \quad (5.111)$$

Typically the value of χ lies in the range 0.1 to 0.3.

Figure 5.62 shows the MOSFET model augmented to include the controlled source $g_{mb}v_{bs}$ that models the body effect. Ideally, this is the model to be used whenever the source is not connected to the substrate. It has been found, however, that except in some very particular situations, the body effect can generally be ignored in the initial, pencil-and-paper design of MOSFET amplifiers.

Finally, although the analysis above was performed on a NMOS transistor, the results and the equivalent circuit of Fig. 5.62 apply equally well to PMOS transistors, except for using $|V_{GS}|$, $|V_t|$, $|V_{OV}|$, $|V_A|$, $|V_{SB}|$, $|\gamma|$, and $|\lambda|$ and replacing k'_n with k'_p in the appropriate formula.

5.9.3 Temperature Effects

Both V_t and k' are temperature sensitive. The magnitude of V_t decreases by about 2 mV for every 1°C rise in temperature. This decrease in $|V_t|$ gives rise to a corresponding increase in drain current as temperature is increased. However, because k' decreases with temperature and its effect is a dominant one, the overall observed effect of a temperature increase is a *decrease* in drain current. This very interesting result is put to use in applying the MOSFET in power circuits (Chapter 11).

5.9.4 Breakdown and Input Protection

As the voltage on the drain is increased, a value is reached at which the *pn* junction between the drain region and substrate suffers avalanche breakdown (see Section 3.5.3). This breakdown usually occurs at voltages of 20 V to 150 V and results in a somewhat rapid increase in current (known as a **weak avalanche**).

Another breakdown effect that occurs at lower voltages (about 20 V) in modern devices is called **punch-through**. It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage to the device.

Yet another kind of breakdown occurs when the gate-to-source voltage exceeds about 30 V. This is the breakdown of the gate oxide and results in permanent damage to the device. Although 30 V may seem high, it must be remembered that the MOSFET has a very high input resistance, and a very small input capacitance, and thus small amounts of static charge accumulating on the gate capacitor can cause its breakdown voltage to be exceeded.

To prevent the accumulation of static charge on the gate capacitor of a MOSFET, gate-protection devices are usually included at the input terminals of MOS integrated circuits. The protection mechanism invariably makes use of clamping diodes.

5.9.5 Velocity Saturation

At high longitudinal electric fields, the drift velocity of charge carriers in the channel reaches an upper limit (approximately 10^7 cm/s for electrons and holes in silicon). This effect, which in modern very-short-channel devices can occur for v_{DS} lower than 1 V, is called velocity saturation. It can be shown that when velocity saturation occurs, the current i_D will no longer be related to v_{GS} by the square-law relationship. Rather, i_D becomes linearly dependent on v_{GS} and the transconductance g_m becomes constant and independent of v_{GS} . In Chapter 13, we shall consider velocity saturation in our study of deep submicron (i.e., $L < 0.25$ μm) CMOS digital circuits.

5.9.6 The Depletion-Type MOSFET

We conclude this section with a brief discussion of another type of MOSFET, the depletion-type MOSFET. Its structure is similar to that of the enhancement-type MOSFET with one important difference: The depletion MOSFET has a physically implanted channel. Thus an n -channel depletion-type MOSFET has an n -type silicon region connecting the n^+ source and the n^+ drain regions at the top of the p -type substrate. Thus if a voltage v_{DS} is applied between drain and source, a current i_D flows for $v_{GS} = 0$. In other words, there is no need to induce a channel, unlike the case of the enhancement MOSFET.

The channel depth and hence its conductivity can be controlled by v_{GS} in exactly the same manner as in the enhancement-type device. Applying a positive v_{GS} enhances the channel by attracting more electrons into it. Here, however, we also can apply a negative v_{GS} , which causes electrons to be repelled from the channel, and thus the channel becomes shallower and its conductivity decreases. The negative v_{GS} is said to **deplete** the channel of its charge carriers, and this mode of operation (negative v_{GS}) is called **depletion mode**. As the magnitude of v_{GS} is increased in the negative direction, a value is reached at which the channel is completely depleted of charge carriers and i_D is reduced to zero even though v_{DS} may be still applied. This negative value of v_{GS} is the threshold voltage of the n -channel depletion-type MOSFET.

The description above suggests (correctly) that a depletion-type MOSFET can be operated in the enhancement mode by applying a positive v_{GS} and in the depletion mode by

applying a negative v_{GS} . This is illustrated in Fig. 5.63, which shows both the circuit symbol for the depletion NMOS transistor (Fig. 5.63a) and its i_D - v_{GS} characteristic. Observe that here the threshold voltage V_t is negative. The i_D - v_{DS} characteristics (not shown) are similar to those for the enhancement-type MOSFET except for the negative V_t . Finally, note that the device symbol denotes the existing channel via the shaded area next to the vertical line.

Depletion-type MOSFETs can be fabricated on the same IC chip as enhancement-type devices, resulting in circuits with improved characteristics, as will be shown in a later chapter.

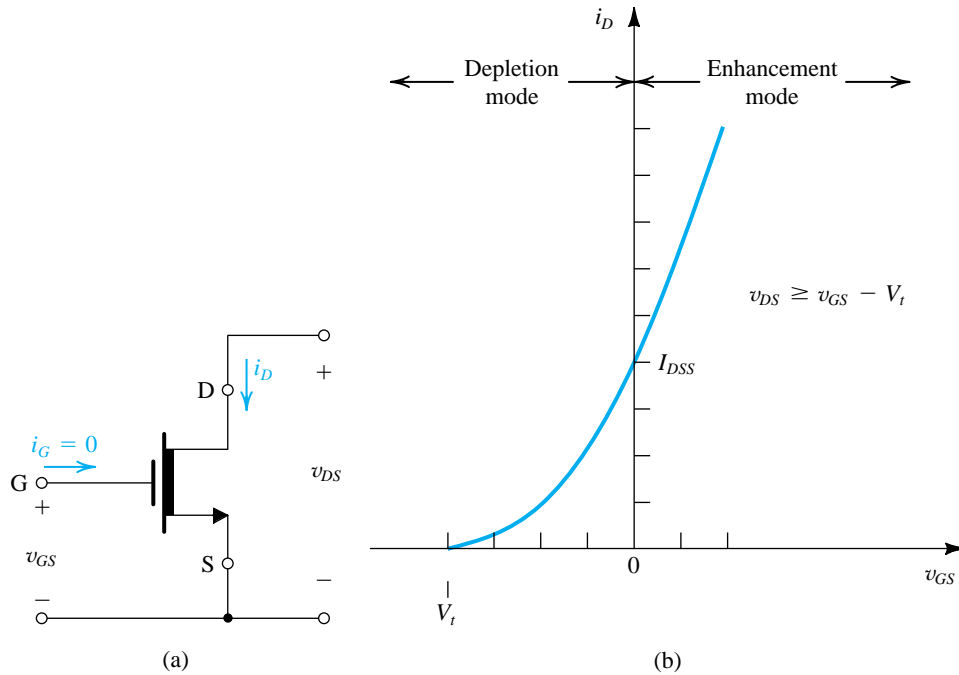


Figure 5.63 The circuit symbol (a) and the i_D - v_{GS} characteristic in saturation; (b) for an n -channel depletion-type MOSFET.

EXERCISE

5.43 For a depletion-type NMOS transistor with $V_t = -2$ V and $k'_n(W/L) = 2$ mA/V², find the minimum v_{DS} required to operate in the saturation region when $v_{GS} = +1$ V. What is the corresponding value of i_D ?

Ans. 3 V; 9 mA

Summary

- The enhancement-type MOSFET is currently the most widely used semiconductor device. It is the basis of CMOS technology, which is the most popular IC fabrication technology at this time. CMOS provides both n -channel (NMOS) and p -channel (PMOS) transistors, which increases design flexibility. The minimum MOSFET channel length achievable with a given CMOS process is used to characterize the process. This figure has been continually reduced and is currently 45 nm.
- The overdrive voltage, $|v_{OV}| \equiv |v_{GS}| - |V_t|$, is the key quantity that governs the operation of the MOSFET. For the MOSFET to operate in the saturation region, which is the region for amplifier application, $|v_{DS}| \geq |v_{OV}|$, and the resulting $i_D = \frac{1}{2}\mu_n C_{ox}(W/L)v_{OV}^2$ (for NMOS; replace μ_n with μ_p for PMOS). If $|v_{DS}| < |v_{OV}|$, the MOSFET operates in the triode region, which together with cutoff is used for operating the MOSFET as a switch.
- Tables 5.1 and 5.2 provide summaries of the conditions and relationships that describe the operation of NMOS and PMOS transistors, respectively.
- In saturation, i_D shows some linear dependence on v_{DS} as a result of the change in channel length. This channel-length modulation phenomenon becomes more pronounced as L decreases. It is modeled by ascribing an output resistance $r_o = |V_A|/I_D$ to the MOSFET model. Although the effect of r_o on the operation of discrete-circuit MOS amplifiers is small, that is not the case in IC amplifiers (Chapter 7).
- The essence of the use of the MOSFET as an amplifier is that in saturation v_{GS} controls i_D in the manner of a voltage-controlled current source. When the device is dc biased in the saturation region and the signal v_{gs} is kept small, the operation of the MOSFET becomes almost linear.
- A systematic procedure to analyze a MOS amplifier circuit consists of replacing the MOSFET with one of its small-signal, equivalent-circuit models (Refer to Table 5.3). DC voltage sources are replaced by short circuits, and dc current sources by open circuits. The analysis is then performed on the resulting equivalent circuit.
- In cases where a resistance is connected in series with the source lead of the MOSFET, the T model is the most convenient to use.
- The three basic configurations of MOS amplifiers are shown in Fig. 5.43 (without the bias arrangements). Their characteristic parameter values are provided in Table 5.4.
- The CS amplifier has (ideally) infinite input resistance and a reasonably high gain but a rather high output resistance and a limited high-frequency response. It is used to obtain most of the gain in a cascade amplifier.
- Adding a resistance R_s in the source lead of the CS amplifier can lead to beneficial results.
- The CG amplifier has a low input resistance and thus it alone has limited and specialized applications. However, its excellent high-frequency response makes it attractive in combination with the CS amplifier (Chapters 7 and 9).
- The source follower has (ideally) infinite input resistance, a voltage gain lower than but close to unity, and a low output resistance. It is employed as a voltage buffer and as the output stage of a multistage amplifier.
- A key step in the design of transistor amplifiers is to bias the transistor to operate at an appropriate point in the saturation region. A good bias design ensures that the parameters of the bias point, I_D , V_{OV} , and V_{DS} , are predictable and stable, and do not vary by a large amount when the transistor is replaced by another of the same type.
- As evidenced by the example circuits given in Section 5.8, discrete-circuit MOS amplifiers utilize large coupling and bypass capacitors. As will be seen in Chapter 7, this is *not* the case in IC amplifiers.
- The depletion-type MOSFET has an implanted channel and thus can be operated in either the depletion or enhancement modes. It is characterized by the same equations used for the enhancement device except for having a negative V_t (positive V_t for depletion PMOS transistors).



Computer Simulation Problems

SIM Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the disc. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

* difficult problem; ** more difficult; *** very challenging and/or time-consuming; D: design problem.

Section 5.1: Device Structure and Physical Operation

5.1 MOS technology is used to fabricate a capacitor, utilizing the gate metallization and the substrate as the capacitor electrodes. Find the area required per 1-pF capacitance for oxide thickness ranging from 2 nm to 10 nm. For a square plate capacitor of 10 pF, what dimensions are needed?

5.2 Calculate the total charge stored in the channel of an NMOS transistor having $C_{ox} = 6 \text{ fF}/\mu\text{m}^2$, $L = 0.25 \mu\text{m}$, and $W = 2.5 \mu\text{m}$, and operated at $V_{OV} = 0.5 \text{ V}$ and $V_{DS} = 0 \text{ V}$.

5.3 Use dimensional analysis to show that the units of the process transconductance parameter k'_n are A/V^2 . What are the dimensions of the MOSFET transconductance parameter k_n ?

5.4 An NMOS transistor that is operated with a small v_{DS} is found to exhibit a resistance r_{DS} . By what factor will r_{DS} change in each of the following situations?

- V_{OV} is doubled.
- The device is replaced with another fabricated in the same technology but with double the width.
- The device is replaced with another fabricated in the same technology but with both the width and length doubled.
- The device is replaced with another fabricated in a more advanced technology for which the oxide thickness is halved and similarly for W and L (assume μ_n remains unchanged).

D 5.5 An NMOS transistor fabricated in a technology for which $k'_n = 400 \mu\text{A}/\text{V}^2$ and $V_t = 0.4 \text{ V}$ is required to operate with a small v_{DS} as a variable resistor ranging in value from 200Ω to $1 \text{ k}\Omega$. Specify the range required for the control voltage V_{GS} and the required transistor width W . It is required to use the smallest possible device, as limited by the minimum channel length of this technology ($L_{\min} = 0.18 \mu\text{m}$) and the maximum allowed voltage of 1.8 V .

5.6 Sketch a set of i_D - v_{DS} characteristic curves for an NMOS transistor operating with a small v_{DS} (in the manner shown in Fig. 5.4). Let the MOSFET have $k_n = 5 \text{ mA}/\text{V}^2$

and $V_t = 0.5 \text{ V}$. Sketch and clearly label the graphs for $V_{GS} = 0.5, 1.0, 1.5, 2.0$, and 2.5 V . Let V_{DS} be in the range 0 to 50 mV . Give the value of r_{DS} obtained for each of the five values of V_{GS} . Although only a sketch, your diagram should be drawn to scale as much as possible.

D 5.7 An n -channel MOS device in a technology for which oxide thickness is 20 nm , minimum channel length is $1 \mu\text{m}$, $k'_n = 100 \mu\text{A}/\text{V}^2$, and $V_t = 0.8 \text{ V}$ operates in the triode region, with small v_{DS} and with the gate-source voltage in the range 0 V to $+5 \text{ V}$. What device width is needed to ensure that the minimum available resistance is $1 \text{ k}\Omega$?

5.8 Consider an NMOS transistor operating in the triode region with an overdrive voltage V_{OV} . Find an expression for the incremental resistance

$$r_{ds} \equiv 1 / \left. \frac{\partial i_D}{\partial v_{DS}} \right|_{v_{DS}=V_{DS}}$$

Give the values of r_{ds} in terms of k_n and V_{OV} for $V_{DS} = 0$, $0.5 V_{OV}$, $0.8 V_{OV}$, and V_{OV} .

5.9 An NMOS transistor with $k_n = 1 \text{ mA}/\text{V}^2$ and $V_t = 1 \text{ V}$ is operated with $V_{GS} = 2.5 \text{ V}$. At what value of V_{DS} does the transistor enter the saturation region? What value of I_D is obtained in saturation?

5.10 Consider a CMOS process for which $L_{\min} = 0.25 \mu\text{m}$, $t_{ox} = 6 \text{ nm}$, $\mu_n = 460 \text{ cm}^2/\text{V}\cdot\text{s}$, and $V_t = 0.5 \text{ V}$.

- Find C_{ox} and k'_n .
- For an NMOS transistor with $W/L = 15 \mu\text{m}/0.25 \mu\text{m}$, calculate the values of V_{OV} , V_{GS} , and $V_{DS\min}$ needed to operate the transistor in the saturation region with a dc current $I_D = 0.8 \text{ mA}$.
- For the device in (b), find the value of V_{OV} and V_{GS} required to cause the device to operate as a $500\text{-}\Omega$ resistor for very small v_{DS} .

5.11 A p -channel MOSFET with a threshold voltage $V_{tp} = -0.7 \text{ V}$ has its source connected to ground.

- What should the gate voltage be for the device to operate with an overdrive voltage of $|V_{OV}| = 0.5 \text{ V}$?
- With the gate voltage as in (b), what is the highest voltage allowed at the drain while the device operates in the saturation region?
- If the drain current obtained in (b) is 1 mA , what would the current be for $V_D = -10 \text{ mV}$ and for $V_D = -2 \text{ V}$?

5.12 With the knowledge that $\mu_p \approx 0.4\mu_n$, what must be the relative width of n -channel and p -channel devices if they are to have equal drain currents when operated in the saturation mode with overdrive voltages of the same magnitude?

5.13 An n -channel device has $k'_n = 50 \mu\text{A}/\text{V}^2$, $V_t = 0.8 \text{ V}$, and $W/L = 20$. The device is to operate as a switch for small v_{DS} , utilizing a control voltage v_{GS} in the range 0 V to 5 V . Find the switch closure resistance, r_{DS} , and closure voltage, V_{DS} , obtained when $v_{GS} = 5 \text{ V}$ and $i_D = 1 \text{ mA}$. Recalling that $\mu_p \approx 0.4\mu_n$, what must W/L be for a p -channel device that provides the same performance as the n -channel device in this application?

5.14 Consider an n -channel MOSFET with $t_{ox} = 9 \text{ nm}$, $\mu_n = 500 \text{ cm}^2/\text{V} \cdot \text{s}$, $V_t = 0.7 \text{ V}$, and $W/L = 10$. Find the drain current in the following cases:

- (a) $v_{GS} = 5 \text{ V}$ and $v_{DS} = 1 \text{ V}$
- (b) $v_{GS} = 2 \text{ V}$ and $v_{DS} = 1.3 \text{ V}$
- (c) $v_{GS} = 5 \text{ V}$ and $v_{DS} = 0.2 \text{ V}$
- (d) $v_{GS} = v_{DS} = 5 \text{ V}$

***5.15** This problem illustrates the central point in the electronics revolution that has been in effect for the past four decades: By continually reducing the MOSFET size, we are able to pack more devices on an IC chip. Gordon Moore,

co-founder of Intel Corporation, predicted this exponential growth of chip-packing density very early in the history of the development of the integrated circuit in the formulation that has become known as **Moore's law**.

The table below shows four technology generations, each characterized by the minimum possible MOSFET channel length (row 1). In going from one generation to another, both L and t_{ox} are scaled by the same factor. The power supply utilized V_{DD} is also scaled by the same factor, to keep the magnitudes of all electrical fields within the device unchanged. Unfortunately, but for good reasons, V_t cannot be scaled similarly.

Complete the table entries, noting that row 5 asks for the transconductance parameter of an NMOS transistor with $W/L = 10$; row 9 asks for the value of I_D obtained with $V_{GS} = V_{DS} = V_{DD}$; row 10 asks for the power $P = V_{DD}I_D$ dissipated in the circuit. An important quantity is the power density, P/A , asked for in row 11. Finally, you are asked to find the number of transistors that can be placed on an IC chip fabricated in each of the technologies in terms of the number obtained with the $0.5\text{-}\mu\text{m}$ technology (n).

1	L (μm)	0.5	0.25	0.18	0.13
2	t_{ox} (nm)	10			
3	C_{ox} (fF/ μm^2)				
4	k'_n ($\mu\text{A}/\text{V}^2$) ($\mu_n = 500 \text{ cm}^2/\text{V} \cdot \text{s}$)				
5	k_n (mA/ V^2) for $W/L = 10$				
6	Device area, A (μm^2)				
7	V_{DD} (V)	5			
8	V_t (V)	0.7	0.5	0.4	0.4
9	I_D (mA) For $V_{GS} = V_{DS} = V_{DD}$				
10	P (mW)				
11	P/A (mW/ μm^2)				
12	Devices per chip	n			

Section 5.2: Current–Voltage Characteristics

In the following problems, when λ is not specified, assume it is zero.

5.16 Show that when channel-length modulation is neglected (i.e., $\lambda = 0$), plotting i_D/k_n versus v_{DS} for various values of v_{OV} , and plotting i_D/k_n versus v_{OV} for $v_{DS} \geq v_{OV}$, results in universal representation of the i_D – v_{DS} and i_D – v_{GS} characteristics of the NMOS transistor. That is, the resulting graphs are both technology and device independent. Furthermore, these graphs apply equally well to the PMOS transistor by a simple relabeling of variables. (How?) What is the slope at $v_{DS} = 0$ of each of the i_D/k_n versus v_{DS} graphs? For the i_D/k_n versus v_{GS} graph, find the slope at a point $v_{OV} = V_{OV}$.

5.17 An NMOS transistor having $V_t = 1$ V is operated in the triode region with v_{DS} small. With $V_{GS} = 1.5$ V, it is found to have a resistance r_{DS} of 1 k Ω . What value of V_{GS} is required to obtain $r_{DS} = 200$ Ω ? Find the corresponding resistance values obtained with a device having twice the value of W .

5.18 A particular enhancement MOSFET for which $V_t = 0.5$ V and $k'_n(W/L) = 0.1$ mA/V² is to be operated in the saturation region. If i_D is to be 12.5 μ A, find the required v_{GS} and the minimum required v_{DS} . Repeat for $i_D = 50$ μ A.

5.19 A particular n -channel enhancement MOSFET is measured to have a drain current of 0.4 mA at $V_{GS} = V_{DS} = 2$ V and of 0.1 mA at $V_{GS} = V_{DS} = 1.5$ V. What are the values of k_n and V_t for this device?

D 5.20 For a particular IC-fabrication process, the transconductance parameter $k'_n = 400$ μ A/V², and $V_t = 0.4$ V. In an application in which $v_{GS} = v_{DS} = V_{\text{supply}} = 1.8$ V, a drain current of 2 mA is required of a device of minimum length of 0.18 μ m. What value of channel width must the design use?

5.21 An NMOS transistor, operating in the linear-resistance region with $v_{DS} = 0.1$ V, is found to conduct 60 μ A for $v_{GS} = 2$ V and 160 μ A for $v_{GS} = 4$ V. What is the apparent value of threshold voltage V_t ? If $k'_n = 50$ μ A/V², what is the device W/L ratio? What current would you expect to flow with $v_{GS} = 3$ V and $v_{DS} = 0.15$ V? If the device is operated at $v_{GS} = 3$ V, at what value of v_{DS} will the drain end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?

5.22 For an NMOS transistor, for which $V_t = 0.5$ V, operating with v_{GS} in the range of 0.8 V to 1.8 V, what is the largest value of v_{DS} for which the channel remains continuous?

5.23 An NMOS transistor, fabricated with $W = 100$ μ m and $L = 5$ μ m in a technology for which $k'_n = 50$ μ A/V² and $V_t = 1$ V, is to be operated at very low values of v_{DS} as a linear resistor. For v_{GS} varying from 1.1 V to 11 V, what range of resistor values can be obtained? What is the available range if

- (a) the device width is halved?
- (b) the device length is halved?
- (c) both the width and length are halved?

5.24 When the drain and gate of a MOSFET are connected together, a two-terminal device known as a “diode-connected transistor” results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

- (a) the i – v relationship is given by

$$i = \frac{1}{2}k' \frac{W}{L} (v - |V_t|)^2$$

- (b) the incremental resistance r for a device biased to operate at $v = |V_t| + V_{OV}$ is given by

$$r \equiv 1 / \left[\frac{\partial i}{\partial v} \right] = 1 / \left(k' \frac{W}{L} V_{OV} \right)$$

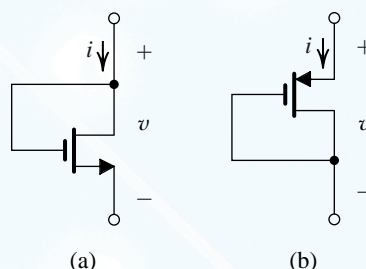


Figure P5.24

5.25 For the circuit in Fig. P5.25, sketch i_D versus v_S for v_S varying from 0 to V_{DD} . Clearly label your sketch.

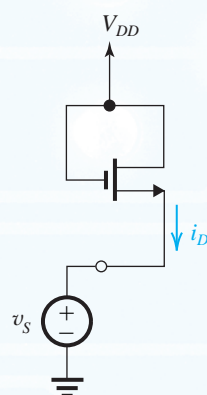


Figure P5.25

5.26 For the circuit in Fig. P5.26, find an expression for v_{DS} in terms of i_D . Sketch and clearly label a graph for v_{DS} versus i_D .

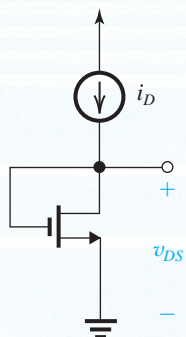


Figure P5.26

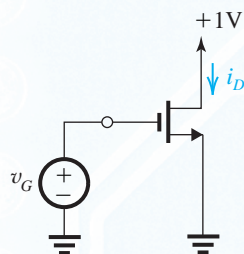


Figure P5.28

***5.27** The table below lists 10 different cases labeled (a) to (j) for operating an NMOS transistor with $V_t = 1$ V. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which v_{DS} is negative, you should exchange the drain and

source before solving the problem. You can do this because the MOSFET is a symmetric device.

5.28 The NMOS transistor in Fig. P5.28 has $V_t = 0.4$ V and $k'_n(W/L) = 1$ mA/V². Sketch and clearly label i_D versus v_G with v_G varying in the range 0 to +1.8 V. Give equations for the various portions of the resulting graph.

5.29 Fig. P5.29 shows two NMOS transistors operating in saturation at equal V_{GS} and V_{DS} .

(a) If the two devices are matched except for a maximum possible mismatch in their W/L ratios of 2%, what is the maximum resulting mismatch in the drain currents?

(b) If the two devices are matched except for a maximum possible mismatch in their V_t values of 10 mV, what is the maximum resulting mismatch in the drain currents? Assume that the nominal value of V_t is 1 V.

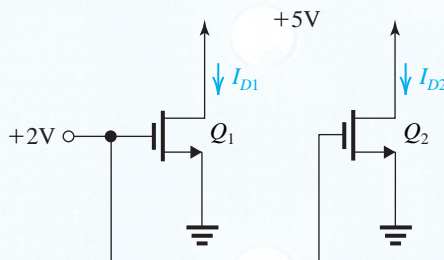


Figure P5.29

5.30 For a particular MOSFET operating in the saturation region at a constant v_{GS} , i_D is found to be 1 mA for

Case	Voltage (V)						Region of operation
	V_s	V_g	V_d	V_{GS}	V_{OV}	V_{DS}	
a	+1.0	+1.0	+2.0				
b	+1.0	+2.5	+2.0				
c	+1.0	+2.5	+1.5				
d	+1.0	+1.5	0				
e	0	+2.5	1.0				
f	+1.0	+1.0	+1.0				
g	-1.0	0	0				
h	-1.5	0	0				
i	-1.0	0	+1.0				
j	+0.5	+2.0	+0.5				

$v_{DS} = 1$ V and 1.05 mA for $v_{DS} = 2$ V. What values of r_o , V_A , and λ correspond?

5.31 A particular MOSFET has $V_A = 50$ V. For operation at 0.1 mA and 1 mA, what are the expected output resistances? In each case, for a change in v_{DS} of 1 V, what percentage change in drain current would you expect?

D 5.32 In a particular IC design in which the standard channel length is 2 μm , an NMOS device with W/L of 5 operating at 100 μA is found to have an output resistance of 0.5 $\text{M}\Omega$, about $\frac{1}{4}$ of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new W/L ratio? What is V_A for the standard device in this IC? The new device?

D 5.33 For a particular n -channel MOS technology, in which the minimum channel length is 1 μm , the associated value of λ is 0.02 V^{-1} . If a particular device for which L is 3 μm operates at $v_{DS} = 1$ V with a drain current of 80 μA , what does the drain current become if v_{DS} is raised to 5 V? What percentage change does this represent? What can be done to reduce the percentage by a factor of 2?

5.34 An NMOS transistor is fabricated in a 0.8- μm process having $k'_n = 130 \mu\text{A/V}^2$ and $V'_A = 20 \text{ V}/\mu\text{m}$ of channel length. If $L = 1.6 \mu\text{m}$ and $W = 16 \mu\text{m}$, find V_A and λ . Find the value of I_D that results when the device is operated with an overdrive voltage of 0.5 V and $V_{DS} = 2$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 1 V, what is the corresponding change in I_D ?

5.35 If in an NMOS transistor, both W and L are quadrupled and V_{OV} is halved, by what factor does r_o change?

D 5.36 Consider the circuit in Fig. P5.29 with both transistors perfectly matched but with the dc voltage at the drain of Q_1 lowered to +2 V. If the two drain currents are to be matched within 1% (i.e., the maximum difference allowed between the two currents is 1%), what is the minimum required value of V_A ? If the technology is specified to have $V'_A = 100 \text{ V}/\mu\text{m}$, what is the minimum channel length the designer must use?

5.37 Complete the missing entries in the following table, which describes characteristics of suitably biased NMOS transistors:

MOS	1	2	3	4
$\lambda(\text{V}^{-1})$		0.01		
V_A (V)	10			200
I_D (mA)	1		0.1	
r_o (k Ω)		30	100	1000

5.38 An enhancement PMOS transistor has $k'_p(W/L) = 80 \mu\text{A/V}^2$, $V_t = -1.5$ V, and $\lambda = -0.02 \text{ V}^{-1}$. The gate is connected to ground and the source to +5 V. Find the drain current for $v_D = +4$ V, +1.5 V, 0 V, and -5 V.

5.39 A p -channel transistor for which $|V_t| = 1$ V and $|V_A| = 50$ V operates in saturation with $|v_{GS}| = 3$ V, $|v_{DS}| = 4$ V, and $i_D = 3$ mA. Find corresponding signed values for v_{GS} , v_{SG} , v_{DS} , v_{SD} , V_t , V_A , λ , and $k'_p(W/L)$.

5.40 The table below lists the terminal voltages of a PMOS transistor in six cases, labeled a, b, c, d, e, and f. The transistor has $V_{tp} = -1$ V. Complete the table entries.

	V_S	V_G	V_D	V_{SG}	$ V_{OV} $	V_{SD}	Region of operation
a	+2	+2	0				
b	+2	+1	0				
c	+2	0	0				
d	+2	0	+1				
e	+2	0	+1.5				
f	+2	0	+2				

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5.41 The PMOS transistor in Fig. P5.41 has $V_{tp} = -0.5$ V. As the gate voltage v_G is varied from +2.5 V to 0 V, the transistor moves through all of its three possible modes of operation. Specify the value of v_G at which the device changes modes of operation.

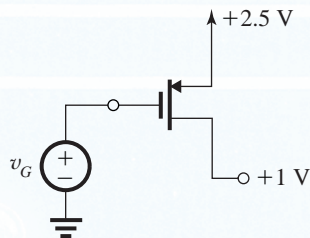


Figure P5.41

***5.42** (a) Using the expression for i_D in saturation and neglecting the channel-length modulation effect (i.e., let $\lambda = 0$), derive an expression for the per unit change in i_D per $^{\circ}\text{C}$ $[(\partial i_D / i_D) / \partial T]$ in terms of the per unit change in k'_n per $^{\circ}\text{C}$ $[(\partial k'_n / k'_n) / \partial T]$, the temperature coefficient of V_t in $\text{V}/^{\circ}\text{C}$ $(\partial V_t / \partial T)$, and V_{GS} and V_t .

(b) If V_t decreases by 2 mV for every $^{\circ}\text{C}$ rise in temperature, find the temperature coefficient of k'_n that results in i_D decreasing by $0.2\%/^{\circ}\text{C}$ when the NMOS transistor with $V_t = 1$ V is operated at $V_{GS} = 5$ V.

***5.43** Various NMOS and PMOS transistors, numbered 1 to 4, are measured in operation, as shown in the table at the bottom of the page. For each transistor, find the value of $\mu C_{ox} W/L$ and V_t that apply and complete the table, with V in volts, I in μA , and $\mu C_{ox} W/L$ in $\mu\text{A}/\text{V}^2$.

***5.44** All the transistors in the circuits shown in Fig. P5.44 have the same values of $|V_t|$, k' , W/L , and λ . Moreover, λ is negligibly small. All operate in saturation at $I_D = I$ and $|V_{GS}| = |V_{DS}| = 1$ V. Find the voltages V_1 , V_2 , V_3 , and V_4 . If $|V_t| = 0.5$ V and $I = 0.1$ mA, how large a resistor can be inserted in series with each drain connection while maintaining saturation? What is the largest resistor that can be placed in series with each gate? If the current source I requires at least 0.5 V between its terminals to operate

properly, what is the largest resistor that can be placed in series with each MOSFET source while ensuring saturated-mode operation of each transistor at $I_D = I$? In the latter limiting situation, what do V_1 , V_2 , V_3 , and V_4 become?

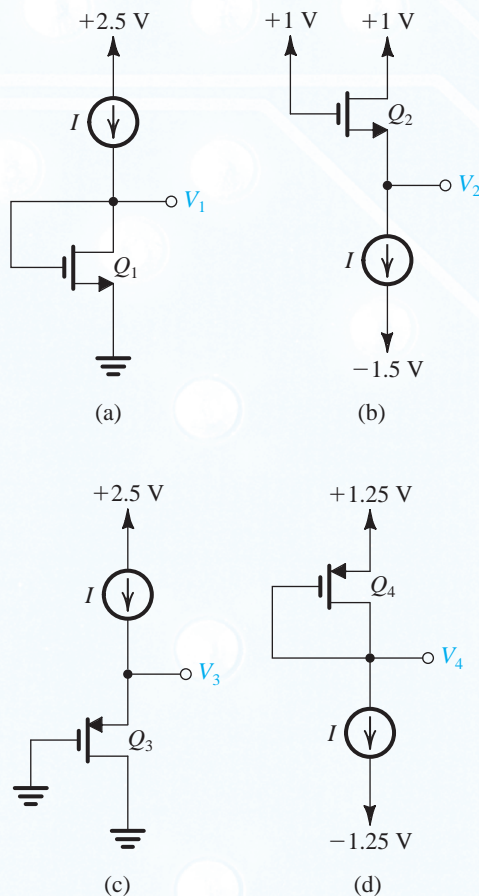


Figure P5.44

Case	Transistor	V_s	V_g	V_d	I_D	Type	Mode	$\mu C_{ox} W/L$	V_t
a	1	0	2	5	100				
	1	0	3	5	400				
b	2	5	3	-4.5	50				
	2	5	2	-0.5	450				
c	3	5	3	4	200				
	3	5	2	0	800				
d	4	-2	0	0	72				
	4	-4	0	-3	270				

Section 5.3: MOSFET Circuits at DC

Note: If λ is not specified, assume it is zero.

D 5.45 Design the circuit of Fig. 5.21 to establish a drain current of 0.25 mA and a drain voltage of 0 V. The MOSFET has $V_t = 1$ V, $\mu_n C_{ox} = 60 \mu\text{A}/\text{V}^2$, $L = 3 \mu\text{m}$, and $W = 100 \mu\text{m}$.

D 5.46 For the circuit in Fig. E5.10, assume that Q_1 and Q_2 are matched except for having different widths, W_1 and W_2 . Let $V_t = 0.5$ V, $k'_n = 0.4 \text{ mA}/\text{V}^2$, $L_1 = L_2 = 0.36 \mu\text{m}$, $W_1 = 1.8 \mu\text{m}$, and $\lambda = 0$.

(a) Find the value of R required to establish a current of $90 \mu\text{A}$ in Q_1 .

(b) Find W_2 and R_2 so that Q_2 operates at the edge of saturation with a current of 0.9 mA.

5.47 The transistor in the circuit of Fig. P5.47 has $k'_n = 0.4 \text{ mA}/\text{V}^2$, $V_t = 0.5$ V, and $\lambda = 0$. Show that operation at the edge of saturation is obtained when the following condition is satisfied:

$$\left(\frac{W}{L}\right)R_D = 1.5 \text{ k}\Omega$$

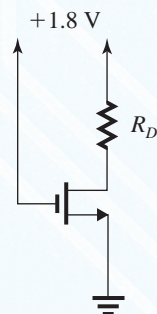


Figure P5.47

5.48 It is required to operate the transistor in the circuit of Fig. P5.47 at the edge of saturation with $I_D = 1$ mA. If $V_t = 0.5$ V, find the required value of R_D .

D 5.49 The PMOS transistor in the circuit of Fig. P5.49 has $V_t = -0.6$ V, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $L = 0.25 \mu\text{m}$, and $\lambda = 0$. Find the values required for W and R in order to establish a drain current of 0.8 mA and a voltage V_D of 1.5 V.

D 5.50 The NMOS transistors in the circuit of Fig. P5.50 have $V_t = 0.5$ V, $\mu_n C_{ox} = 250 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $L_1 = L_2 = 0.25 \mu\text{m}$. Find the required values of gate width for each of Q_1 and Q_2 , and the value of R , to obtain the voltage and current values indicated.

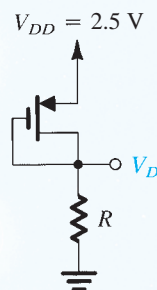


Figure P5.49

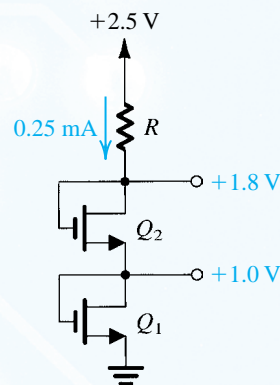


Figure P5.50

D 5.51 The NMOS transistors in the circuit of Fig. P5.51 have $V_t = 1$ V, $\mu_n C_{ox} = 120 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $L_1 = L_2 = L_3 = 1 \mu\text{m}$. Find the required values of gate width for each of Q_1 , Q_2 , and Q_3 to obtain the voltage and current values indicated.

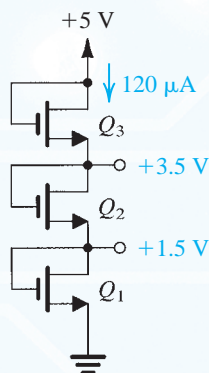


Figure P5.51

5.52 Consider the circuit of Fig. 5.24(a). In Example 5.5 it was found that when $V_t = 1$ V and $k'_n(W/L) = 1$ mA/V², the drain current is 0.5 mA and the drain voltage is +7 V. If the transistor is replaced with another having $V_t = 2$ V and $k'_n(W/L) = 2$ mA/V², find the new values of I_D and V_D . Comment on how tolerant (or intolerant) the circuit is to changes in device parameters.

D 5.53 Using an enhancement-type PMOS transistor with $V_t = -1.5$ V, $k'_p(W/L) = 1$ mA/V², and $\lambda = 0$, design a circuit that resembles that in Fig. 5.24(a). Using a 10-V supply, design for a gate voltage of +6 V, a drain current of 0.5 mA, and a drain voltage of +5 V. Find the values of R_S and R_D .

5.54 The MOSFET in Fig. P5.54 has $V_t = 0.5$ V, $k'_n = 400$ μ A/V², and $\lambda = 0$. Find the required values of W/L and of R so that when $v_i = V_{DD} = +1.8$ V, $r_{DS} = 50$ Ω , and $v_o = 50$ mV.

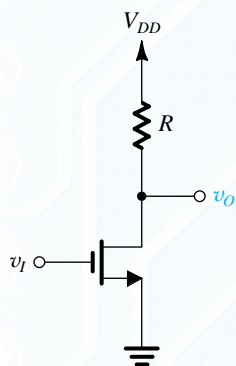


Figure P5.54

5.55 In the circuits shown in Fig. P5.55, transistors are characterized by $|V_t| = 2$ V, $k'W/L = 1$ mA/V², and $\lambda = 0$.

- Find the labeled voltages V_1 through V_7 .
- In each of the circuits, replace the current source with a resistor. Select the resistor value to yield a current as close to that of the current source as possible, while using resistors specified in the 1% table provided in Appendix G. Find the new values of V_1 to V_7 .

5.56 For each of the circuits in Fig. P5.56, find the labeled node voltages. For all transistors, $k'_n(W/L) = 0.5$ mA/V², $V_t = 0.8$ V, and $\lambda = 0$.

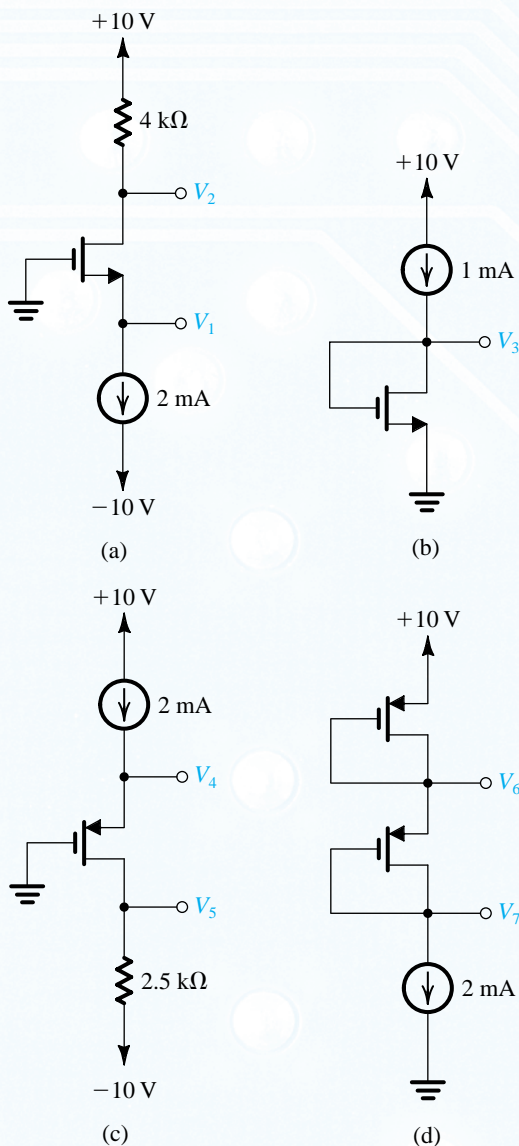


Figure P5.55

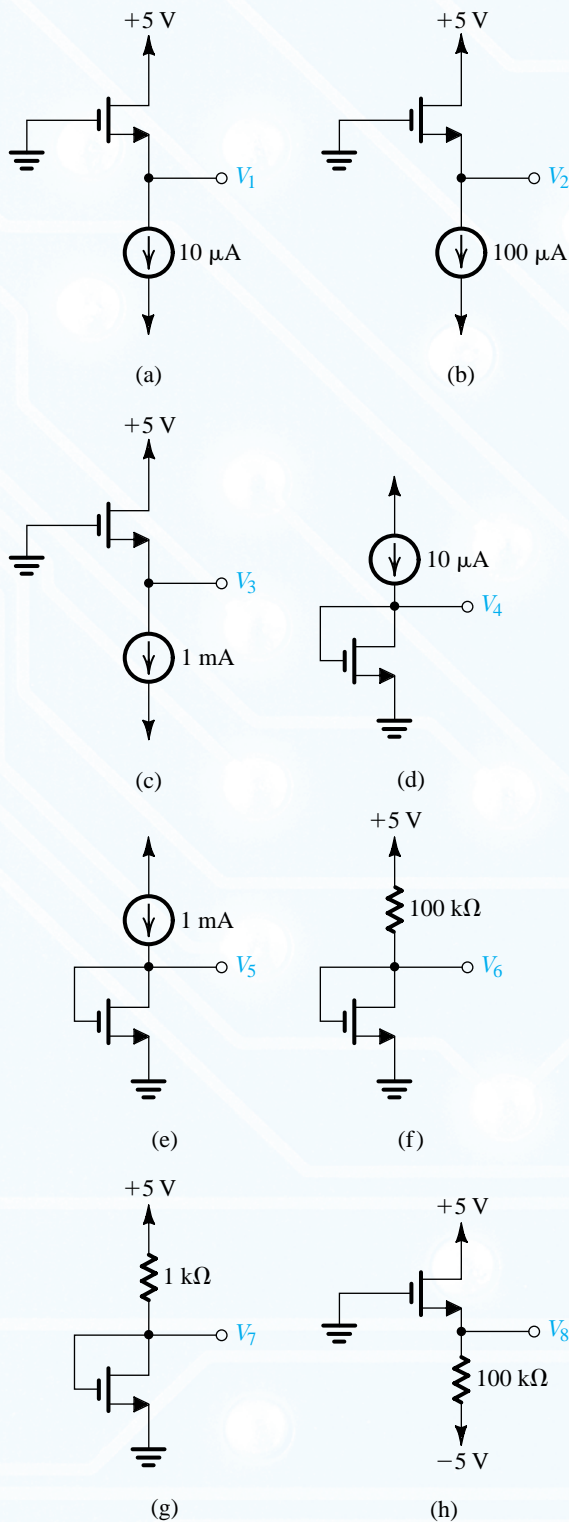


Figure P5.56

5.57 For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have $V_t = 1\ \text{V}$ and $k'_n W/L = 5\ \text{mA/V}^2$.

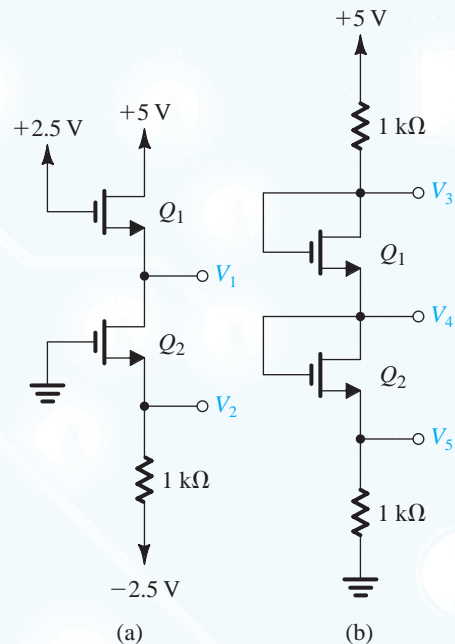


Figure P5.57

***5.58** For the PMOS transistor in the circuit shown in Fig. P5.58, $k'_p = 8\ \mu\text{A/V}^2$, $W/L = 25$, and $|V_{tp}| = 1\ \text{V}$. For $I = 100\ \mu\text{A}$, find the voltages V_{SD} and V_{SG} for $R = 0$, $10\ \text{k}\Omega$, $30\ \text{k}\Omega$, and $100\ \text{k}\Omega$. For what value of R is $V_{SD} = V_{SG}$? $V_{SD} = V_{SG}/2$? $V_{SD} = V_{SG}/10$?

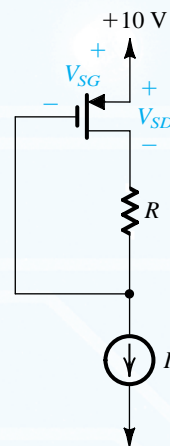


Figure P5.58

5.59 For the circuits in Fig. P5.59, $\mu_n C_{ox} = 2.5 \mu_p C_{ox} = 20 \mu\text{A}/\text{V}^2$, $|V_t| = 1 \text{ V}$, $\lambda = 0$, $L = 10 \mu\text{m}$, and $W = 30 \mu\text{m}$, unless otherwise specified. Find the labeled currents and voltages.

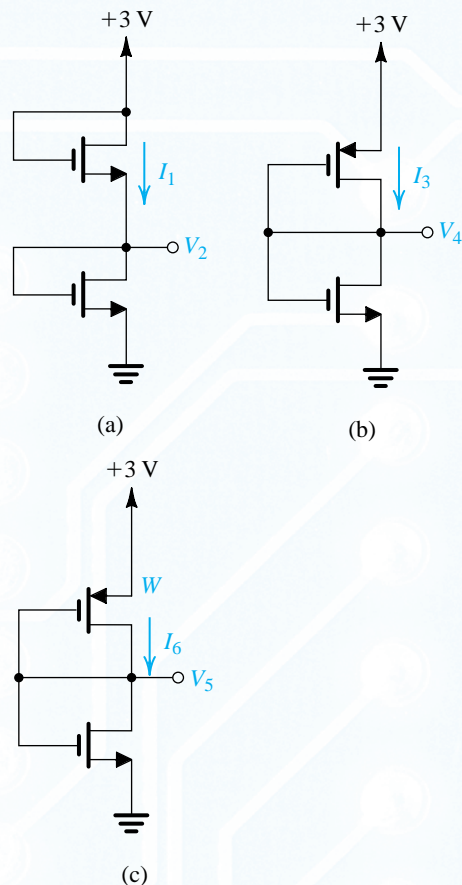


Figure P5.59

SIM *5.60 For the devices in the circuits of Fig. P5.60, $|V_t| = 1 \text{ V}$, $\lambda = 0$, $\mu_n C_{ox} = 50 \mu\text{A}/\text{V}^2$, $L = 1 \mu\text{m}$, and $W = 10 \mu\text{m}$. Find V_2 and I_2 . How do these values change if Q_3 and Q_4 are made to have $W = 100 \mu\text{m}$?

5.61 In the circuit of Fig. P5.61, transistors Q_1 and Q_2 have $V_t = 1 \text{ V}$, and the process transconductance parameter $k'_n = 100 \mu\text{A}/\text{V}^2$. Find V_1 , V_2 , and V_3 for each of the following cases:

- $(W/L)_1 = (W/L)_2 = 20$
- $(W/L)_1 = 1.5(W/L)_2 = 20$

Section 5.4: Applying the MOSFET in Amplifier Design

5.62 Consider the amplifier of Fig. 5.27(a) with $V_{DD} = 2.5 \text{ V}$ and with the MOSFET having $V_t = 0.5 \text{ V}$, $k'_n = 0.25 \text{ mA}/\text{V}^2$ and $W/L = 40$.

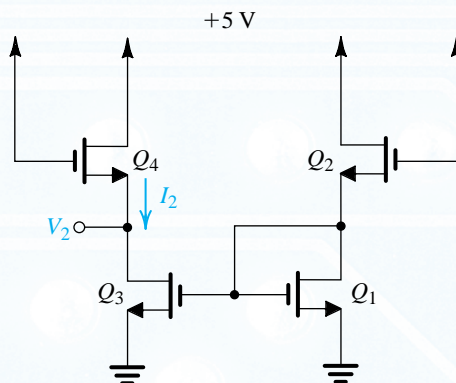


Figure P5.60

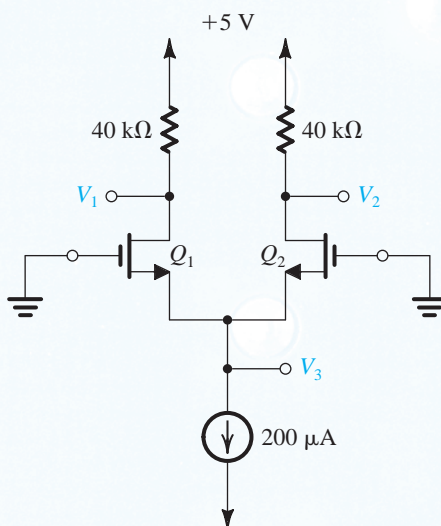


Figure P5.61

- Find the value of R_D that will result in the segment AB of the VTC extending over the range $v_{DS} = 0.5$ to 2.5 V .
- What are the corresponding values of v_{GS} ?
- Find $v_{DS}|_C$ which corresponds to $v_{GS} = V_{DD}$. What is the MOSFET's resistance r_{DS} at operating point C?
- If the amplifier is biased to operate at $V_{GS} = 0.8 \text{ V}$, find V_{DS} and the voltage gain.

5.63 For the amplifier of Fig. 5.29(a) find an expression for the bias voltage V_{GS} at which the magnitude of voltage gain is at its largest value. What is the value of the gain? What is the maximum allowable signal swing at this bias point? Comment on the practical suitability of this bias point.

5.64 Consider the amplifier of Fig. 5.29(a) for the case $V_{DD} = 5 \text{ V}$, $R_D = 24 \text{ k}\Omega$, $k'_n(W/L) = 1 \text{ mA}/\text{V}^2$, and $V_t = 1 \text{ V}$.

- Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig. 5.29(b).

(b) If the amplifier is biased to operate with an overdrive voltage V_{ov} of 0.5 V, find the coordinates of the bias point Q on the transfer characteristic. Also, find the value of I_D and of the incremental gain A_v at the bias point.

(c) For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

5.65 Various measurements are made on an NMOS amplifier for which the drain resistor R_D is 20 k Ω . First, dc measurements show the voltage across the drain resistor, V_{RD} , to be 1.5 V and the gate-to-source bias voltage to be 0.7 V. Then, ac measurements with small signals show the voltage gain to be -10 V/V. What is the value of V_t for this transistor? If the process transconductance parameter k'_n is 200 $\mu\text{A}/\text{V}^2$, what is the MOSFET's W/L ?

***D 5.66** Refer to the expression for the incremental voltage gain in Eq. (5.38). Various design considerations place a lower limit on the value of the overdrive voltage V_{ov} . For our purposes here, let this lower limit be 0.2 V. Also, assume that $V_{DD} = 5$ V.

- Without allowing any room for output voltage swing, what is the maximum voltage gain achievable?
- If we are required to allow for an output voltage swing of ± 0.5 V, what dc bias voltage should be established at the drain to obtain maximum gain? What gain value is achievable? What input signal results in a ± 0.5 -V output swing?
- For the situation in (b), find W/L of the transistor to establish a dc drain current of 100 μA . For the given process technology, $k'_n = 100 \mu\text{A}/\text{V}^2$.
- Find the required value of R_D .

5.67 The expression for the incremental voltage gain A_v given in Eq. (5.38) can be written in as

$$A_v = -\frac{2(V_{DD} - V_{DS})}{V_{ov}}$$

where V_{DS} is the bias voltage at the drain. This expression indicates that for given values of V_{DD} and V_{ov} , the gain magnitude can be increased by biasing the transistor at a lower V_{DS} . This, however, reduces the allowable output signal

swing in the negative direction. Assuming linear operation around the bias point, show that the largest possible negative output signal peak \hat{v}_o that is achievable while the transistor remains saturated is

$$\hat{v}_o = (V_{DS} - V_{ov}) / \left(1 + \frac{1}{|A_v|}\right)$$

For $V_{DD} = 5$ V and $V_{ov} = 0.5$ V, provide a table of values for A_v , \hat{v}_o , and the corresponding \hat{v}_i for $V_{DS} = 1$ V, 1.5 V, 2 V, and 2.5 V. If $k'_n W/L = 1$ mA/V², find I_D and R_D for the design for which $V_{DS} = 1$ V.

***5.68** Figure P5.68 shows an amplifier in which the load resistor R_D has been replaced with another NMOS transistor Q_2 connected as a two-terminal device. Note that because v_{DG} of Q_2 is zero, it will be operating in saturation at all times, even when $v_i = 0$ and $i_{D2} = i_{D1} = 0$. Note also that the two transistors conduct equal drain currents. Using $i_{D1} = i_{D2}$, show that for the range of v_i over which Q_1 is operating in saturation, that is, for

$$V_{t1} \leq v_i \leq v_o + V_{t1}$$

the output voltage will be given by

$$v_o = V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}} V_t - \sqrt{\frac{(W/L)_1}{(W/L)_2}} v_i$$

where we have assumed $V_{t1} = V_{t2} = V_t$. Thus the circuit functions as a linear amplifier, even for large input signals. For $(W/L)_1 = (50 \mu\text{m}/0.5 \mu\text{m})$ and $(W/L)_2 = (5 \mu\text{m}/0.5 \mu\text{m})$, find the voltage gain.

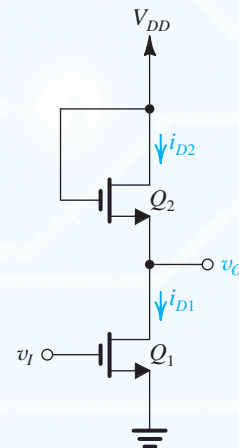


Figure P5.68

Section 5.5: Small-Signal Operation and Models

***5.69** This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal v_{gs} be a sine wave with amplitude V_{gs} , and substitute $v_{gs} = V_{gs} \sin \omega t$ in Eq. (5.43). Using the trigonometric identity $\sin^2 \theta = \frac{1}{2} - \frac{1}{2} \cos 2\theta$, show that the ratio of the signal at frequency 2ω to that at frequency ω , expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4} \frac{V_{gs}}{V_{OV}} \times 100$$

If in a particular application V_{gs} is 10 mV, find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

5.70 Consider an NMOS transistor having $k_n = 10 \text{ mA/V}^2$. Let the transistor be biased at $V_{OV} = 0.5 \text{ V}$. For operation in saturation, what dc bias current I_D results? If a 0.05-V signal is superimposed on V_{GS} , find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias current I_D . Repeat for a -0.05-V signal. Use these results to estimate g_m of the FET at this bias point. Compare with the value of g_m obtained using Eq. (5.48).

5.71 Consider the FET amplifier of Fig. 5.34 for the case $V_t = 0.4 \text{ V}$, $k_n = 4 \text{ mA/V}^2$, $V_{GS} = 0.65 \text{ V}$, $V_{DD} = 1.8 \text{ V}$, and $R_D = 8 \text{ k}\Omega$.

- Find the dc quantities I_D and V_D .
- Calculate the value of g_m at the bias point.
- Calculate the value of the voltage gain.
- If the MOSFET has $\lambda = 0.1 \text{ V}^{-1}$, find r_o at the bias point and calculate the voltage gain.

D *5.72 An NMOS amplifier is to be designed to provide a 0.50-V peak output signal across a 50-k Ω load that can be used as a drain resistor. If a gain of at least 5 V/V is needed,

what g_m is required? Using a dc supply of 1.8 V, what values of I_D and V_{OV} would you choose? What W/L ratio is required if $\mu_n C_{ox} = 200 \text{ }\mu\text{A/V}^2$? If $V_t = 0.4 \text{ V}$, find V_{GS} .

D *5.73 In this problem we investigate an optimum design of the CS amplifier circuit of Fig. 5.34. First, use the voltage gain expression $A_v = -g_m R_D$ together with Eq. (5.57) for g_m to show that

$$A_v = -\frac{2I_D R_D}{V_{OV}} = -\frac{2(V_{DD} - V_D)}{V_{OV}}$$

Next, let the maximum positive input signal be \hat{v}_i . To keep the second-harmonic distortion to an acceptable level, we bias the MOSFET to operate at an overdrive voltage $V_{OV} \gg \hat{v}_i$. Let $V_{OV} = m\hat{v}_i$. Now, to maximize the voltage gain $|A_v|$, we design for the lowest possible V_D . Show that the minimum V_D that is consistent with allowing a negative signal voltage swing at the drain of $|A_v|\hat{v}_i$ while maintaining saturation-mode operation is given by

$$V_D = \frac{V_{OV} + \hat{v}_i + 2V_{DD}(\hat{v}_i/V_{OV})}{1 + 2(\hat{v}_i/V_{OV})}$$

Now, find V_{OV} , V_D , A_v , and \hat{v}_o for the case $V_{DD} = 2.5 \text{ V}$, $\hat{v}_i = 20 \text{ mV}$, and $m = 15$. If it is desired to operate this transistor at $I_D = 100 \text{ }\mu\text{A}$, find the values of R_D and W/L , assuming that for this process technology $k'_n = 100 \text{ }\mu\text{A/V}^2$.

5.74 In the table below, for enhancement MOS transistors operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate g_m using one of Eqs. (5.55), (5.56) or (5.57). Assume $\mu_n = 500 \text{ cm}^2/\text{V}\cdot\text{s}$, $\mu_p = 250 \text{ cm}^2/\text{V}\cdot\text{s}$, and $C_{ox} = 0.4 \text{ fF}/\mu\text{m}^2$.

5.75 An NMOS technology has $\mu_n C_{ox} = 250 \text{ }\mu\text{A/V}^2$ and $V_t = 0.5 \text{ V}$. For a transistor with $L = 0.5 \text{ }\mu\text{m}$, find the value of W that results in $g_m = 1 \text{ mA/V}$ at $I_D = 0.25 \text{ mA}$. Also, find the required V_{GS} .

Case	Type	Voltages (V)				Dimensions (μm)				
		I_D (mA)	$ V_{GS} $	$ V_t $	V_{OV}	W	L	W/L	$k'(W/L)$	g_m (mA/V)
a	N	1	3	2			1			
b	N	1		0.7	0.5	50				
c	N	10			2		1			
d	N	0.5			0.5					
e	N	0.1				10	2			
f	N		1.8	0.8		40	4			
g	P	0.5			2			25		
h	P		3	1					0.5	
i	P	10				4000	2			
j	P	10			4					
k	P				1	30	3			
l	P	0.1			5				0.008	

5.76 For the NMOS amplifier in Fig. P5.76, replace the transistor with its T equivalent circuit, assuming $\lambda = 0$. Derive expressions for the voltage gains v_s/v_i and v_d/v_i .

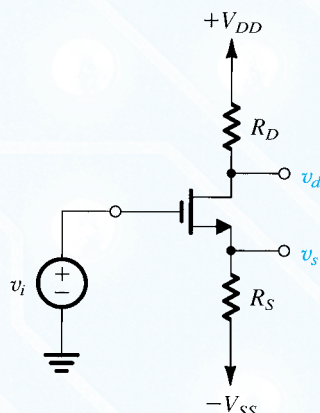


Figure P5.76

SIM 5.77 In the circuit of Fig. P5.77, the NMOS transistor has $|V_t| = 0.5$ V and $V_A = 50$ V and operates with $V_D = 1$ V. What is the voltage gain v_o/v_i ? What do V_D and the gain become for I increased to 1 mA?

5.78 For a 0.8- μm CMOS fabrication process: $V_{tn} = 0.8$ V, $V_{tp} = -0.9$ V, $\mu_n C_{ox} = 90 \mu\text{A/V}^2$, $\mu_p C_{ox} = 30 \mu\text{A/V}^2$, $C_{ox} = 1.9 \text{ fF}/\mu\text{m}^2$, V_A (n -channel devices) $= 8L$ (μm), and $|V_A|$ (p -channel devices) $= 12L$ (μm). Find the small-signal model parameters (g_m and r_o) for both an NMOS and a PMOS transistor having $W/L = 20 \mu\text{m}/2 \mu\text{m}$ and operating at $I_D = 100 \mu\text{A}$. Also, find the overdrive voltage at which each device must be operating.

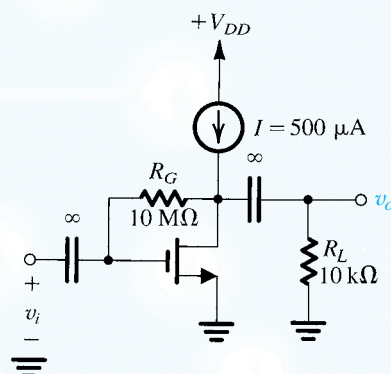


Figure P5.77

***5.79** Figure P5.79 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).

- If the transistor has $V_t = 1$ V, and $k_n = 2 \text{ mA/V}^2$, verify that the bias circuit establishes $V_{GS} = 2$ V, $I_D = 1$ mA, and $V_D = +7.5$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
- Find g_m and r_o if $V_A = 100$ V.
- Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.
- Find R_{in} , v_{gs}/v_{sig} , v_o/v_{gs} , and v_o/v_{sig} .

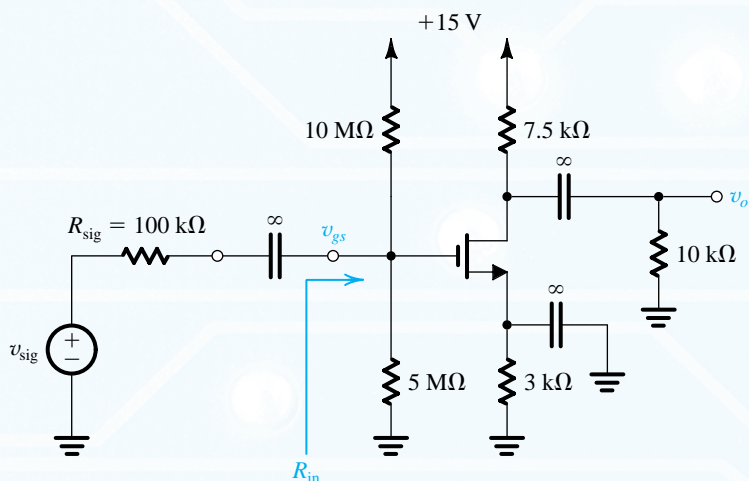


Figure P5.79

Section 5.6: Basic MOSFET Amplifier Configurations*

5.80 An amplifier with an input resistance of 100 k Ω , an open-circuit voltage gain of 100 V/V and an output resistance of 100 Ω is connected between a 10-k Ω signal source and a 1-k Ω load. Find the overall voltage gain G_v . Also find the current gain, defined as the ratio of the load current to the current drawn from the signal source.

D 5.81 Specify the parameters R_{in} , A_{vo} and R_o of an amplifier that is to be connected between a 100-k Ω source and a 2-k Ω load and is required to meet the following specifications:

- (a) No more than 10% of the signal strength is lost in the connection to the amplifier input;
- (b) If the load resistance changes from the nominal value of 2 k Ω to a low value of 1 k Ω , the change in output voltage is limited to 10% of nominal value; and
- (c) The nominal overall voltage gain is 10 V/V.

5.82 Figure P5.82 shows an alternative equivalent circuit representation of an amplifier. If this circuit is to be equivalent to that in Fig. 5.44(b) show that $G_m = A_{vo}/R_o$. Also convince yourself that the transconductance G_m is defined as

$$G_m = \left. \frac{i_o}{v_i} \right|_{R_L = 0}$$

and hence is known as the short-circuit transconductance. Now, if the amplifier is fed with a signal source (v_{sig} , R_{sig}) and is connected to a load resistance R_L show that the gain

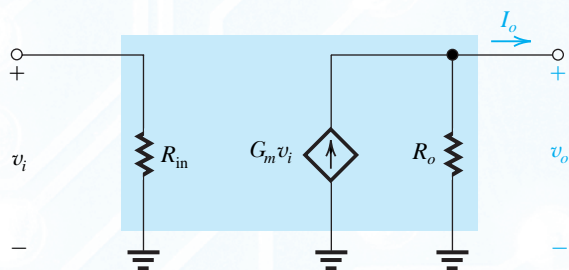


Figure P5.82

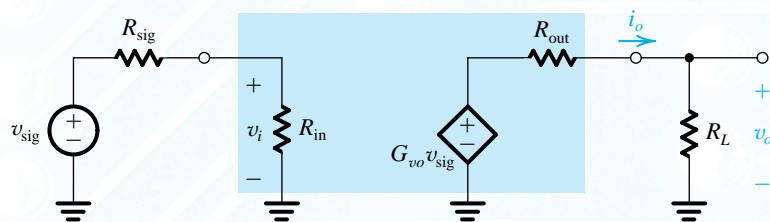


Figure P5.83

of the amplifier proper A_v is given by $A_v = G_m(R_o \parallel R_L)$ and the overall voltage gain G_v is given by

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} G_m(R_o \parallel R_L)$$

5.83 An alternative equivalent circuit of an amplifier fed with a signal source (v_{sig} , R_{sig}) and connected to a load R_L is shown in Fig. P5.83. Here G_{vo} is the open-circuit overall voltage gain,

$$G_{vo} = \left. \frac{v_o}{v_{sig}} \right|_{R_L = \infty}$$

and R_{out} is the output resistance with v_{sig} set to zero. This is different than R_o . Show that

$$G_{vo} = \frac{R_i}{R_i + R_{sig}} A_{vo}$$

where $R_i = R_{in}|_{R_L = \infty}$.

Also show that the overall voltage gain is

$$G_v = G_{vo} \frac{R_L}{R_L + R_{out}}$$

****5.84** Most practical amplifiers have internal feedback that make them non-unilateral. In such a case, R_{in} depends on R_L . To illustrate this point we show in Fig. P5.84 the equivalent circuit of an amplifier where a feedback resistance R_f models the internal feedback mechanism that is present in this amplifier. It is R_f that makes the amplifier non-unilateral. Show that

$$R_{in} = R_1 \parallel \left[\frac{R_f + (R_2 \parallel R_L)}{1 + g_m(R_2 \parallel R_L)} \right]$$

$$A_{vo} = -g_m R_2 \frac{1 - 1/(g_m R_f)}{1 + (R_2/R_f)}$$

$$R_o = R_2 \parallel R_f$$

Evaluate R_{in} , A_{vo} and R_o for the case $R_1 = 100$ k Ω , $R_f = 1$ M Ω , $g_m = 100$ mA/V, $R_2 = 100$ Ω and $R_L = 1$ k Ω . Which of the amplifier characteristic parameters is most affected by R_f (that is, relative to the case with $R_f = \infty$)?

* Problems 5.80 to 5.84 are identical to Problems 6.107 to 6.111.

For $R_{\text{sig}} = 100 \text{ k}\Omega$ determine the overall voltage gain, G_v , with and without R_f present.

5.85 Calculate the overall voltage gain of a CS amplifier fed with a $1\text{-M}\Omega$ source and connected to a $20\text{-k}\Omega$ load. The MOSFET has $g_m = 2 \text{ mA/V}$ and $r_o = 50 \text{ k}\Omega$, and a drain resistance $R_D = 10 \text{ k}\Omega$ is utilized.

5.86 A CS amplifier utilizes a MOSFET with $\mu_n C_{ox} = 400 \text{ }\mu\text{A/V}^2$, $W/L = 10$, and $V_A = 10 \text{ V}$. It is biased at $I_D = 0.2 \text{ mA}$ and uses $R_D = 6 \text{ k}\Omega$. Find R_{in} , A_{v_o} , and R_o . Also, if a load resistance of $10 \text{ k}\Omega$ is connected to the output, what overall voltage gain G_v is realized? Now, if a 0.2-V peak sine-wave signal is required at the output, what must the peak amplitude of v_{sig} be?

5.87 A common-source amplifier utilizes a MOSFET for which $V_A = 12.5 \text{ V}$ and is operated at $V_{OV} = 0.25 \text{ V}$. What is the value of its $(g_m r_o)$? The amplifier feeds a load resistance $R_L = 15 \text{ k}\Omega$. The designer selects $R_D = 2R_L$. If it is required to realize an overall voltage gain G_v of -10 V/V what g_m is needed? Also specify the bias current I_D . If, to increase the output signal swing, R_D is reduced to $R_D = R_L$, what does G_v become?

5.88 Two identical CS amplifiers are connected in cascade. The first stage is fed with a source v_{sig} having a resistance $R_{\text{sig}} = 100 \text{ k}\Omega$. A load resistance $R_L = 10 \text{ k}\Omega$ is connected to the drain of the second stage. Each MOSFET is biased at $I_D = 0.25 \text{ mA}$ and operates with $V_{OV} = 0.25 \text{ V}$. Assume V_A is very large. Each stage utilizes a drain resistance $R_D = 10 \text{ k}\Omega$.

- Sketch the equivalent circuit of the two-stage amplifier.
- Calculate the overall voltage gain G_v .

5.89 In discrete-circuit amplifiers, $(R_D \parallel R_L)$ is usually much smaller than r_o , and thus r_o can be neglected in determining the voltage gain of the CS amplifier. Nevertheless, it is useful to note that r_o poses an absolute upper limit on the voltage gain of a CS amplifier. Find this upper limit by let-

ting $R_D \parallel R_L = \infty$. Express the maximum achievable gain in terms of V_A and V_{OV} .

5.90 A MOSFET connected in the CS configuration has a transconductance $g_m = 5 \text{ mA/V}$. When a resistance R_s is connected in the source lead, the effective transconductance is reduced to 1 mA/V . What do you estimate the value of R_s to be?

5.91 A CS amplifier using an NMOS transistor with $g_m = 4 \text{ mA/V}$ is found to have an overall voltage gain of -16 V/V . What value should a resistance R_s inserted in the source lead have to reduce the overall voltage gain to -8 V/V ?

5.92 The overall voltage gain of a CS amplifier with a resistance $R_s = 1 \text{ k}\Omega$ in the source lead was measured and found to be -15 V/V . When R_s is shorted, but the circuit operation remained linear, the gain doubled. What must g_m be? What value of R_s is needed to obtain an overall voltage gain of -10 V/V ?

5.93 A CG amplifier using an NMOS transistor for which $g_m = 4 \text{ mA/V}$ has a $5\text{-k}\Omega$ drain resistance R_D and a $5\text{-k}\Omega$ load resistance R_L . The amplifier is driven by a voltage source having a $500 \text{ }\Omega$ resistance. What is the input resistance of the amplifier? What is the overall voltage gain G_v ? By what factor must the bias current I_D of the MOSFET be changed so that R_{in} matches R_{sig} ?

5.94 A CG amplifier when fed with a signal source having $R_{\text{sig}} = 200 \text{ }\Omega$ is found to have an overall voltage gain of 10 V/V . When a $200\text{-}\Omega$ resistance is added in series with the signal generator the overall voltage gain decreased to 8 V/V . What must g_m of the MOSFET be? If the MOSFET is biased at $I_D = 0.2 \text{ mA}$, at what overdrive voltage it must be operating?

D 5.95 A source follower is required to connect a high-resistance source to a load whose resistance is nominally $2 \text{ k}\Omega$ but can be as low as $1 \text{ k}\Omega$ and as high as $3 \text{ k}\Omega$. What is the maximum output resistance that the source follower must have if the output voltage is to remain within $\pm 20\%$ of nominal value? If the MOSFET has $k_n = 16 \text{ mA/V}^2$, at

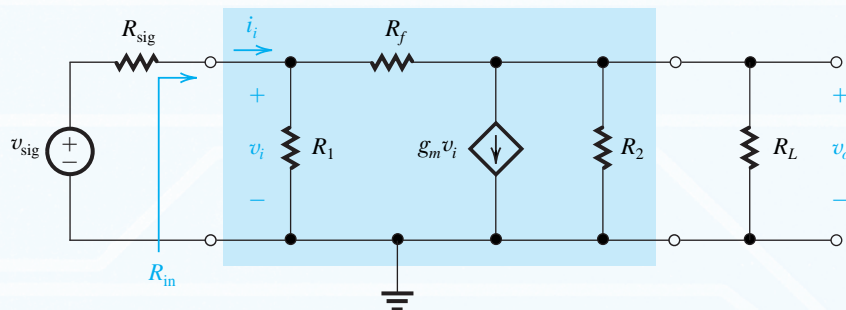


Figure P5.84

what current I_D must it be biased? At what overdrive voltage is the MOSFET operating?

***5.96** Refer to the source-follower equivalent circuit shown in Fig. 5.50(b). Show that

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \frac{R_L \parallel r_o}{(R_L \parallel r_o) + \frac{1}{g_m}}$$

Now, with R_L removed, the voltage gain is carefully measured and found to be 0.98. Then, when R_L is connected and its value is varied, it is found that the gain is halved at $R_L = 500 \Omega$. If the amplifier remained linear throughout this measurement, what must the values of g_m and r_o be?

D 5.97 A source follower is required to deliver a 0.5-V peak sinusoid to 2-k Ω load. If the peak amplitude of v_{gs} is to be limited to 50 mV, what is the lowest value of I_D at which the MOSFET can be biased? At this bias current, what are the maximum and minimum currents that the MOSFET will be conducting (at the positive and negative peaks of the output sine wave)? What must the peak amplitude of v_{sig} be?

Section 5.7: Biasing in MOS Amplifier Circuits

D 5.98 Consider the classical biasing scheme shown in Fig. 5.52(c), using a 9-V supply. For the MOSFET, $V_t = 1$ V, $\lambda = 0$, and $k_n = 2$ mA/V². Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of R_S and R_D . Use 22 M Ω for the larger of R_{G1} and R_{G2} . What are the values of R_{G1} , R_{G2} , R_S , and R_D that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

D 5.99 Using the circuit topology displayed in Fig. 5.52(e), arrange to bias the NMOS transistor at $I_D = 1$ mA with V_D midway between cutoff and the beginning of triode operation. The available supplies are ± 5 V. For the NMOS transistor, $V_t = 1.0$ V, $\lambda = 0$, and $k_n = 2$ mA/V². Use a gate-bias resistor of 10 M Ω . Specify R_S and R_D to two significant digits.

D *5.100 In an electronic instrument using the biasing scheme shown in Fig. 5.52(c), a manufacturing error reduces R_S to zero. Let $V_{DD} = 12$ V, $R_{G1} = 5.6$ M Ω , and $R_{G2} = 2.2$ M Ω . What is the value of V_G created? If supplier specifications allow k_n to vary from 0.2 to 0.3 mA/V² and V_t to vary from 1.0 V to 1.5 V, what are the extreme values of I_D that may result? What value of R_S should have been installed to limit the maximum value of I_D to 0.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix G). What extreme values of current now result?

5.101 An enhancement NMOS transistor is connected in the bias circuit of Fig. 5.52(c), with $V_G = 4$ V and $R_S = 2$ k Ω . The transistor has $V_t = 1$ V and $k_n = 2$ mA/V². What bias

current results? If a transistor for which k_n is 50% higher is used, what is the resulting percentage increase in I_D ?

SIM 5.102 The bias circuit of Fig. 5.52(c) is used in a design with $V_G = 5$ V and $R_S = 2$ k Ω . For an enhancement MOSFET with $k_n = 2$ mA/V², the source voltage was measured and found to be 2 V. What must V_t be for this device? If a device for which V_t is 0.5 V less is used, what does V_S become? What bias current results?

D 5.103 Design the circuit of Fig. 5.52(e) for an enhancement MOSFET having $V_t = 1$ V and $k_n = 2$ mA/V². Let $V_{DD} = V_{SS} = 5$ V. Design for a dc bias current of 1 mA and for the largest possible voltage gain (and thus the largest possible R_D) consistent with allowing a 2-V peak-to-peak voltage swing at the drain. Assume that the signal voltage on the source terminal of the FET is zero.

SIM D 5.104 Design the circuit in Fig. P5.104 so that the transistor operates in saturation with V_D biased 1 V from the edge of the triode region, with $I_D = 1$ mA and $V_D = 3$ V, for each of the following two devices (use a 10- μ A current in the voltage divider):

- (a) $|V_t| = 1$ V and $k'_p W/L = 0.5$ mA/V²
- (b) $|V_t| = 2$ V and $k'_p W/L = 1.25$ mA/V²

For each case, specify the values of V_G , V_D , V_S , R_1 , R_2 , R_S , and R_D .

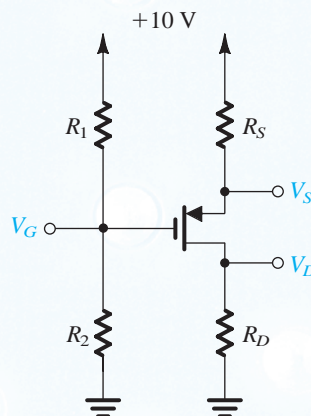


Figure P5.104

****D 5.105** A very useful way to characterize the stability of the bias current I_D is to evaluate the sensitivity of I_D relative to a particular transistor parameter whose variability might be large. The sensitivity of I_D relative to the MOSFET parameter $K \equiv \frac{1}{2}k'(W/L)$ is defined as

$$S_K^{I_D} \equiv \frac{\partial I_D / I_D}{\partial K / K} = \frac{\partial I_D}{\partial K} \frac{K}{I_D}$$

and its value, when multiplied by the variability (or tolerance) of K , provides the corresponding expected variability of I_D . The purpose of this problem is to investigate the use of the sensitivity function in the design of the bias circuit of Fig. 5.52(e).

(a) Show that for V_t constant,

$$S_{K}^{I_D} = 1 / (1 + 2\sqrt{KI_D R_S})$$

(b) For a MOSFET having $K = 100 \mu\text{A}/\text{V}^2$ with a variability of $\pm 10\%$ and $V_t = 1 \text{ V}$, find the value of R_S that would result in $I_D = 100 \mu\text{A}$ with a variability of $\pm 1\%$. Also, find V_{GS} and the required value of V_{SS} .

(c) If the available supply $V_{SS} = 5 \text{ V}$, find the value of R_S for $I_D = 100 \mu\text{A}$. Evaluate the sensitivity function, and give the expected variability of I_D in this case.

5.106 For the circuit in Fig. 5.55(a) with $I = 0.2 \text{ mA}$, $R_G = 0$, $R_D = 10 \text{ k}\Omega$, and $V_{DD} = 2.5 \text{ V}$, consider the behavior in each of the following two cases. In each case, find the voltages V_S , V_D , and V_{DS} that result.

(a) $V_t = 1 \text{ V}$ and $k_n = 1.6 \text{ mA}/\text{V}^2$

(b) $V_t = 0.8 \text{ V}$ and $k_n = 1.25 \text{ mA}/\text{V}^2$

SIM 5.107 In the circuit of Fig. 5.54, let $R_G = 10 \text{ M}\Omega$, $R_D = 10 \text{ k}\Omega$, and $V_{DD} = 10 \text{ V}$. For each of the following two transistors, find the voltages V_D and V_G .

(a) $V_t = 1 \text{ V}$ and $k_n = 0.5 \text{ mA}/\text{V}^2$

(b) $V_t = 2 \text{ V}$ and $k_n = 1.25 \text{ mA}/\text{V}^2$

D 5.108 Using the feedback bias arrangement shown in Fig. 5.54 with a 5-V supply and an NMOS device for which $V_t = 1 \text{ V}$ and $k_n = 0.6 \text{ mA}/\text{V}^2$, find R_D to establish a drain current of 0.2 mA . If resistor values are limited to those on the 5% resistor scale (see Appendix G), what value would you choose? What values of current and V_D result?

D 5.109 Figure P5.109 shows a variation of the feedback-bias circuit of Fig. 5.54. Using a 5-V supply with an NMOS transistor for which $V_t = 1 \text{ V}$, $k_n = 6.25 \text{ mA}/\text{V}^2$ and $\lambda = 0$, provide a design that biases the transistor at $I_D = 2 \text{ mA}$, with V_{DS} large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use $22 \text{ M}\Omega$ as the largest resistor in the feedback-bias network. What values of R_D , R_{G1} , and R_{G2} have you chosen? Specify all resistors to two significant digits.

Section 5.8: Discrete-Circuit MOS Amplifiers

5.110 Calculate the overall voltage gain G_v of a common-source amplifier for which $g_m = 2 \text{ mA}/\text{V}$, $r_o = 50 \text{ k}\Omega$, $R_D = 10 \text{ k}\Omega$, and $R_G = 10 \text{ M}\Omega$. The amplifier is fed from a signal source with a Thévenin resistance of $0.5 \text{ M}\Omega$, and the amplifier output is coupled to a load resistance of $20 \text{ k}\Omega$.

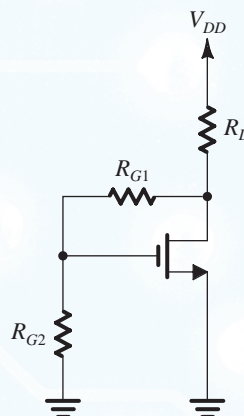


Figure P5.109

D 5.111 This problem investigates a redesign of the common-source amplifier of Exercise 5.38 whose bias design was done in Exercise 5.37 and shown in Fig. E5.37. Please refer to these two exercises.

(a) The open-circuit voltage gain of the CS amplifier can be written as

$$A_{vo} = -\frac{2(V_{DD} - V_D)}{V_{OV}}$$

Verify that this expression yields the results in Exercise 5.38 (i.e., $A_{vo} = -15 \text{ V}/\text{V}$).

(b) A_{vo} can be doubled by reducing V_{OV} by a factor of 2, (i.e., from 1 V to 0.5 V) while V_D is kept unchanged. What corresponding values for I_D , R_D , g_m , and r_o apply?

(c) Find A_{vo} and R_o with r_o taken into account.

(d) For the same value of signal-generator resistance $R_{sig} = 100 \text{ k}\Omega$, the same value of gate-bias resistance $R_G = 4.8 \text{ M}\Omega$, and the same value of load resistance $R_L = 15 \text{ k}\Omega$, evaluate the new value of overall voltage gain G_v with r_o taken into account.

(e) Compare your results to those obtained in Exercises 5.37 and 5.38, and comment.

SIM 5.112 The NMOS transistor in the CS amplifier shown in Fig. P5.112 has $V_t = 0.7 \text{ V}$ and $V_A = 50 \text{ V}$.

(a) Neglecting the Early effect, verify that the MOSFET is operating in saturation with $I_D = 0.5 \text{ mA}$ and $V_{OV} = 0.3 \text{ V}$. What must the MOSFET's k_n be? What is the dc voltage at the drain?

(b) Find R_{in} and G_v .

(c) If v_{sig} is a sinusoid with a peak amplitude \hat{v}_{sig} , find the maximum allowable value of \hat{v}_{sig} for which the transistor remains in saturation. What is the corresponding amplitude of the output voltage?

(d) What is the value of resistance R_s that needs to be inserted in series with capacitor C_s in order to allow us to

double the input signal \hat{v}_{sig} ? What output voltage now results?

SIM D *5.113 The PMOS transistor in the CS amplifier of Fig. P5.113 has $V_{tp} = -0.7$ V and a very large $|V_A|$.

- Select a value for R_S to bias the transistor at $I_D = 0.3$ mA and $|V_{OV}| = 0.3$ V. Assume v_{sig} to have a zero dc component.
- Select a value for R_D that results in $G_v = -10$ V/V.
- Find the largest sinusoid \hat{v}_{sig} that the amplifier can handle while remaining in the saturation region. What is the corresponding signal at the output?
- If to obtain reasonably linear operation, \hat{v}_{sig} is limited to 50 mV, what value can R_D be increased to while maintaining saturation-region operation? What is the new value of G_v ?

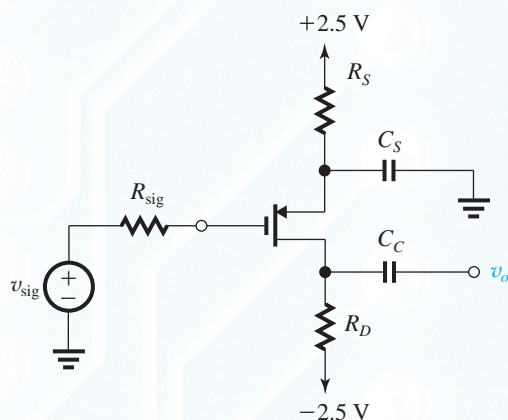


Figure P5.113

5.114 Figure P5.114 shows a scheme for coupling and amplifying a high-frequency pulse signal. The circuit utilizes two MOSFETs whose bias details are not shown and a 50- Ω coaxial cable. Transistor Q_1 operates as a CS amplifier and Q_2 as a CG amplifier. For proper operation, transistor Q_2 is required to present a 50- Ω resistance to the cable. This situation is known as “proper termination” of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is 50 Ω . What must g_{m2} be? If Q_1 is biased at the same point as Q_2 , what is the amplitude of the current pulses in the drain of Q_1 ? What is the amplitude of the voltage pulses at the drain of Q_1 ? What value of R_D is required to provide 1-V pulses at the drain of Q_2 ?

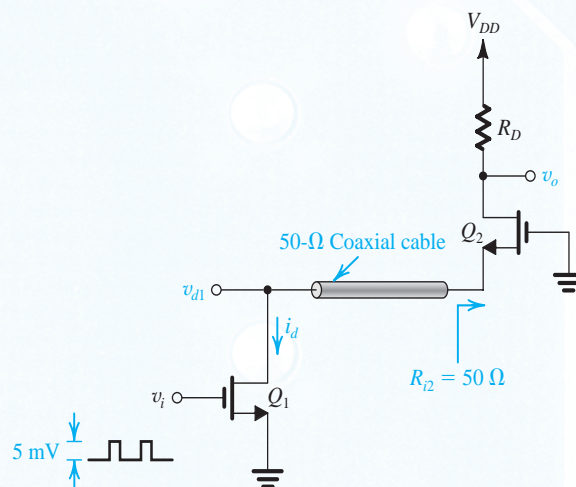


Figure P5.114

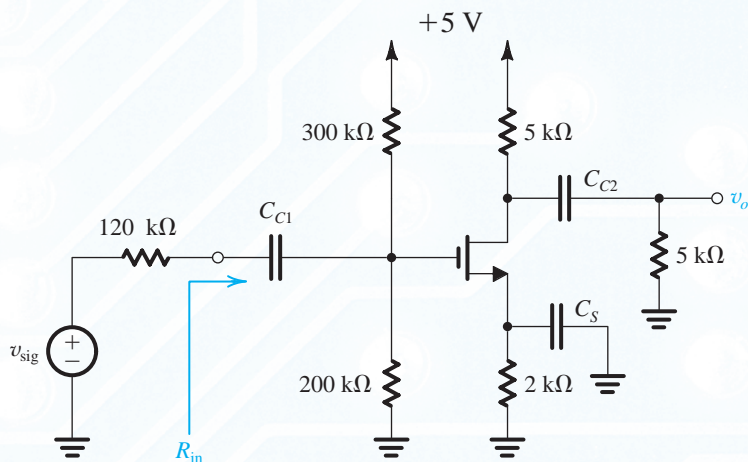


Figure P5.112

D *5.115 The MOSFET in the circuit of Fig. P5.115 has $V_t = 1$ V, $k_n = 0.8$ mA/V², and $V_A = 40$ V.

- Find the values of R_S , R_D , and R_G so that $I_D = 0.1$ mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ± 1 V is possible, and the input resistance at the gate is 10 M Ω . Neglect the Early effect.
- Find the values of g_m and r_o at the bias point.
- If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 M Ω , and terminal Y is connected to a load resistance of 40 k Ω , find the voltage gain from signal source to load.
- If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?
- If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 10 μ A and having a resistance of 100 k Ω , find the voltage signal that can be measured at Y. For simplicity, neglect the effect of r_o .

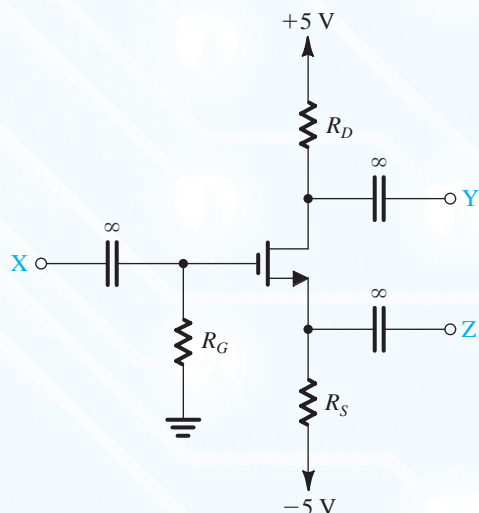


Figure P5.115

- *5.116** (a) The NMOS transistor in the source-follower circuit of Fig. P5.116(a) has $g_m = 5$ mA/V and a large r_o . Find the open-circuit voltage gain and the output resistance.
- (b) The NMOS transistor in the common-gate amplifier of Fig. P5.116(b) has $g_m = 5$ mA/V and a large r_o . Find the input resistance and the voltage gain.
- (c) If the output of the source follower in (a) is connected to the input of the common-gate amplifier in (b), use the results of (a) and (b) to obtain the overall voltage gain v_o/v_i .

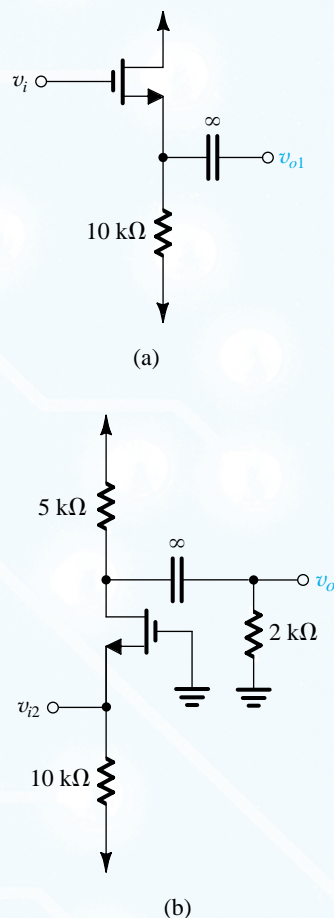


Figure P5.116

***5.117** In this problem we investigate the large-signal operation of the source follower of Fig. 5.60(a). Specifically, consider the situation when negative input signals are applied. Let the negative signal voltage at the output be $-V$. The current in R_L will flow away from ground and will have a value of V/R_L . This current will subtract from the bias current I , resulting in a transistor current of $(I - V/R_L)$. One can use this current value to determine v_{GS} . Now, the signal at the transistor source terminal will be $-V$, superimposed on the dc voltage, which is $-V_{GS}$ (corresponding to a drain current of I). We can thus find the signal voltage at the gate v_i . For the circuit analyzed in Exercise 5.41, find v_i for $v_o = -1$ V, -5 V, -6 V, and -7 V. At each point, find the voltage gain v_o/v_i and compare to the small-signal value found in Exercise 5.41. What is the largest possible negative-output signal?

Section 5.9: The Body Effect and Other Topics

5.118 In a particular application, an n -channel MOSFET operates with V_{SB} in the range 0 V to 4 V. If V_{t0} is nominally 1.0 V, find the range of V_t that results if $\gamma = 0.5 \text{ V}^{1/2}$ and $2\phi_f = 0.6 \text{ V}$. If the gate oxide thickness is increased by a factor of 4, what does the threshold voltage become?

5.119 A p -channel transistor operates in saturation with its source voltage 3 V lower than its substrate. For $\gamma = 0.5 \text{ V}^{1/2}$, $2\phi_f = 0.75 \text{ V}$, and $V_{t0} = -0.7 \text{ V}$, find V_t .

5.120 For an NMOS transistor with $2\phi_f = 0.6 \text{ V}$, $\gamma = 0.5 \text{ V}^{1/2}$, and $V_{SB} = 4 \text{ V}$, find $\chi = g_{mb}/g_m$. If the transistor is biased at $I_D = 0.5 \text{ mA}$ with $V_{OV} = 0.25 \text{ V}$, find g_m and g_{mb} .

5.121 A depletion-type n -channel MOSFET with $k'_n W/L = 2 \text{ mA/V}^2$ and $V_t = -3 \text{ V}$ has its source and gate grounded. Find the region of operation and the drain current for $v_D = 0.1 \text{ V}$, 1 V, 3 V, and 5 V. Neglect the channel-length-modulation effect.

5.122 For a particular depletion-mode NMOS device, $V_t = -2 \text{ V}$, $k'_n W/L = 200 \mu\text{A/V}^2$, and $\lambda = 0.02 \text{ V}^{-1}$. When operated at $v_{GS} = 0$, what is the drain current that flows for $v_{DS} = 1 \text{ V}$, 2 V, 3 V, and 10 V? What does each of these currents become if the device width is doubled with L the same? With L also doubled?

5.123 Neglecting the channel-length-modulation effect show that for the depletion-type NMOS transistor of Fig. P5.123, the $i-v$ relationship is given by

$$i = \frac{1}{2} k'_n (W/L) (v^2 - 2V_t v), \quad \text{for } v \geq V_t$$

$$i = -\frac{1}{2} k'_n (W/L) V_t^2 \quad \text{for } v \leq V_t$$

(Recall that V_t is negative). Sketch the $i-v$ relationship for the case: $V_t = -2 \text{ V}$ and $k'_n(W/L) = 2 \text{ mA/V}^2$.

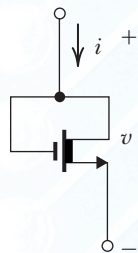


Figure P5.123

General Problems

****5.124** The circuits shown in Fig. P5.124 employ negative feedback, a subject we shall study in detail in Chapter 10. Assume that each transistor is sized and biased so that $g_m = 1 \text{ mA/V}$ and $r_o = 100 \text{ k}\Omega$. Otherwise, ignore all dc biasing detail and concentrate on small-signal operation resulting in response to the input signal v_{sig} . For $R_L = 10 \text{ k}\Omega$, $R_1 = 500 \text{ k}\Omega$, and $R_2 = 1 \text{ M}\Omega$, find the overall voltage gain v_o/v_{sig} and the input resistance R_{in} for each circuit. Neglect the body effect. Do these circuits remind you of op-amp circuits? Comment.

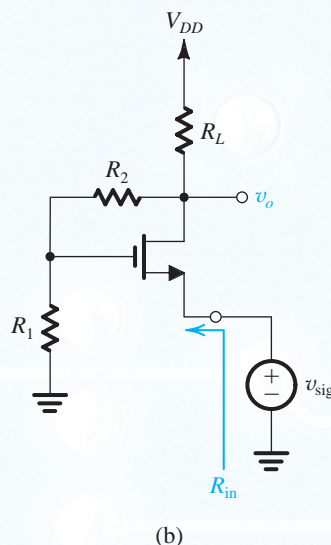
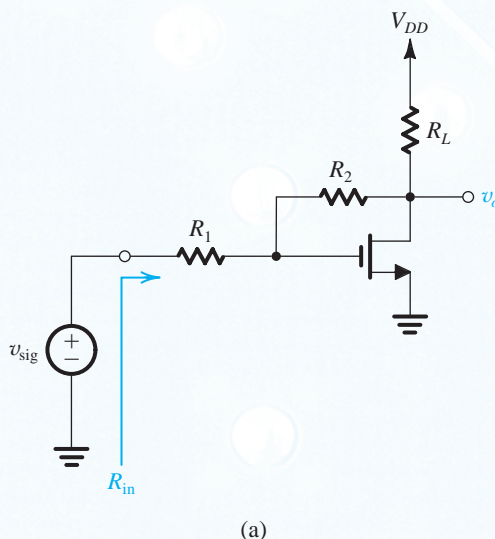


Figure P5.124

5.125 For the two circuits in Problem 5.124 (shown in Fig. P5.124), we wish to consider their dc bias design. Since v_{sig} has a zero dc component, we short-circuit its generator. For NMOS transistors with $V_t = 0.6$ V, find V_{OV} , $k'_n(W/L)$, and V_A to bias each device at $I_D = 0.1$ mA and to obtain the values of g_m and r_o specified in Problem 5.124: namely, $g_m = 1$ mA/V and $r_o = 100$ k Ω . For $R_1 = 0.5$ M Ω , $R_2 = 1$ M Ω , and $R_L = 10$ k Ω , find the required value of V_{DD} .

****5.126** In the amplifier shown in Fig. P5.126, transistors having $V_t = 0.6$ V and $V_A = 20$ V are operated at $V_{GS} = 0.8$ V using the appropriate choice of W/L ratio. In a particular application, Q_1 is to be sized to operate at 10 μ A, while Q_2 is intended to operate at 1 mA. For $R_L = 2$ k Ω , the (R_1, R_2) network sized to consume only 1% of the current in R_L , v_{sig} , having zero dc component, and $I_1 = 10$ μ A, find the values of R_1 and R_2 that satisfy all the requirements. (Hint: V_o must be $+2$ V.) What is the voltage gain v_o/v_i ? Using a result from a theorem known as Miller's theorem (Chapter 9), find the input resistance R_{in} as $R_2/(1 - v_o/v_i)$. Now, calculate the value of the overall voltage gain v_o/v_{sig} . Does this result remind you of the inverting configuration of the op amp? Comment. How would you modify the circuit at the input by using an additional resistor and a very large capacitor to raise the gain v_o/v_{sig} to -5 V/V? Neglect the body effect.

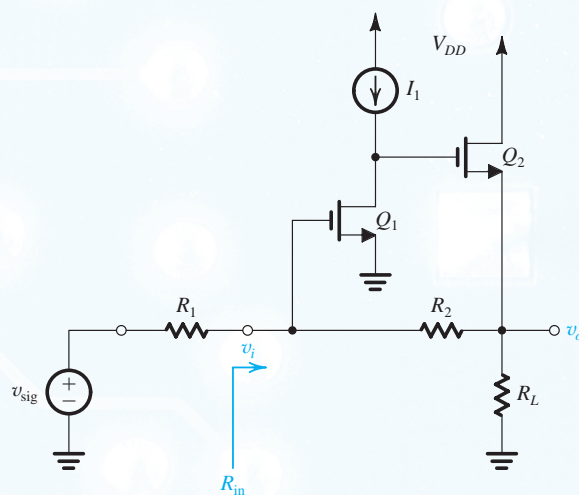


Figure P5.126

5.127 Consider the bias design of the circuit of Problem 5.126 (shown in Fig. P5.126). For $k'_n = 200$ μ A/V² and $V_{DD} = 3.3$ V, find $(W/L)_1$ and $(W/L)_2$ to obtain the operating conditions specified in Problem 5.126.