CHAPTER 12

Operational-Amplifier Circuits

IN THIS CHAPTER YOU WILL LEARN

1. The design and analysis of the two basic CMOS op-amp architectures: the two-stage circuit and the single-stage, folded-cascode circuit.
2. The complete circuit of an analog IC classic: the 741 op amp. Though 40 years old, the 741 circuit includes so many interesting and useful design techniques that its study is still a must.
3. Interesting and useful applications of negative feedback within op-amp circuits to achieve bias stability and increased CMRR.
4. How to break a large analog circuit into its recognizable blocks, to be able to make the analysis amenable to a pencil-and-paper approach, which is the best way to learn design.
5. Some of the modern techniques employed in the design of low-voltage, single-supply BJT op amps.
6. Most importantly, how the different topics we learned about in the preceding chapters come together in the design of the most important analog IC, the op amp.

Introduction

In this chapter, we shall study the internal circuitry of the most important analog IC, namely, the operational amplifier. The terminal characteristics and some circuit applications of op amps were covered in Chapter 2. Here, our objective is to expose the reader to some of the ingenious techniques that have evolved over the years for combining elementary analog circuit building blocks to realize a complete op amp. We shall study both CMOS and bipolar op amps. The CMOS op-amp circuits considered find application primarily in the design of analog and mixed-signal VLSI circuits. Because these op amps are usually designed with a specific application in mind, they can be optimized to meet a subset of the list of desired specifications, such as high dc gain, wide bandwidth, or large output-signal swing. For instance, many CMOS op amps are utilized within an IC and do not connect to the outside terminals of the chip. As a result, the loads on their outputs are usually limited to small capacitances of at most few picofarads. Internal CMOS op amps therefore do not need to have low output resistances, and their design rarely incorporates an output stage. Also, if the op-amp input terminals are not connected to the chip terminals, there will be no danger of static charge damaging the gate oxide of the input MOSFETs. Hence, internal CMOS op amps do not need input clamping diodes for gate protection and thus do not suffer from the

leakage effects of such diodes. In other words, the advantage of near-infinite input resistance of the MOSFET is fully realized.

While CMOS op amps are extensively used in the design of VLSI systems, the BJT remains the device of choice in the design of general-purpose op amps. These are op amps that are utilized in a wide variety of applications and are designed to fit a wide range of specifications. As a result, the circuit of a general-purpose op amp represents a compromise among many performance parameters. We shall study in detail one such circuit, the 741-type op amp. Although the 741 has been available for nearly 40 years, its internal circuit remains as relevant and interesting today as it ever was. Nevertheless, changes in technology have introduced new requirements, such as the need for general-purpose op amps that operate from a single power supply of only 2 V to 3 V. These new requirements have given rise to exciting challenges to op-amp designers. The result has been a wealth of new ideas and design techniques. We shall present a sample of these modern design techniques in the last section.

In addition to exposing the reader to some of the ideas that make analog IC design such an exciting topic, this chapter should serve to tie together many of the concepts and methods studied thus far.

12.1 The Two-Stage CMOS Op Amp

The first op-amp circuit we shall study is the two-stage CMOS topology shown in Fig. 12.1. This simple but elegant circuit has become a classic and is used in a variety of forms in the design of VLSI systems. We have already studied this circuit in Section 8.6.1 as an example of a multistage CMOS amplifier. We urge the reader to review Section 8.6.1 before proceeding further. Here, our discussion will emphasize the performance characteristics of the circuit and the trade-offs involved in its design.

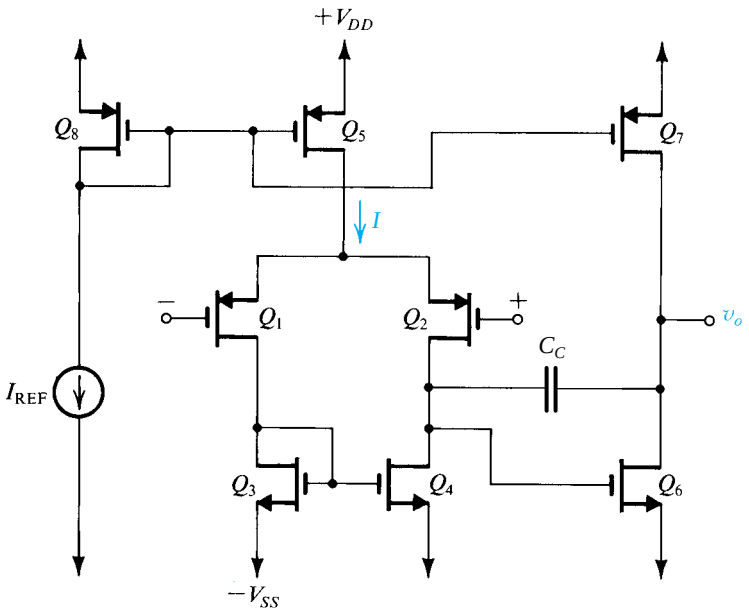


Figure 12.1 The basic two-stage CMOS op-amp configuration.

12.1.1 The Circuit

The circuit consists of two gain stages: The first stage is formed by the differential pair Q_1–Q_2 together with its current mirror load Q_3–Q_4. This differential-amplifier circuit, studied in detail in Section 8.5, provides a voltage gain that is typically in the range of 20 V/V to 60 V/V, as well as performing conversion from differential to single-ended form while providing a reasonable common-mode rejection ratio (CMRR).

The differential pair is biased by current source Q_5, which is one of the two output transistors of the current mirror formed by Q_8, Q_5, and Q_7. The current mirror is fed by a reference current I_{REF}, which can be generated by simply connecting a precision resistor (external to the chip) to the negative supply voltage $-V_{SS}$ or to a more precise negative voltage reference if one is available in the same integrated circuit. Alternatively, for applications with more stringent requirements, I_{REF} can be generated using a circuit such as that studied in Section 8.6.1 (Fig. 8.41).

The second gain stage consists of the common-source transistor Q_6 and its current-source load Q_7. The second stage typically provides a gain of 50 V/V to 80 V/V. In addition, it takes part in the process of frequency compensating the op amp. From Section 10.13 the reader will recall that to guarantee that the op amp will operate in a stable fashion (as opposed to oscillating) when negative feedback of various amounts is applied, the open-loop gain is made to roll off with frequency at the uniform rate of –20 dB/decade. This in turn is achieved by introducing a pole at a relatively low frequency and arranging for it to dominate the frequency-response determination. In the circuit we are studying, this is implemented using a compensation capacitance C_C connected in the negative-feedback path of the second-stage amplifying transistor Q_6. As will be seen, C_C (together with the much smaller capacitance C_{gd6} across it) is Miller-multiplied by the gain of the second stage, and the resulting capacitance at the input of the second stage interacts with the total resistance there to provide the required dominant pole (more on this later).

Unless properly designed, the CMOS op-amp circuit of Fig. 12.1 can exhibit a **systematic output dc offset** voltage. This point was discussed in Section 8.6.1, where it was found that the dc offset can be eliminated by sizing the transistors so as to satisfy the following constraint:

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5} \tag{12.1}$$

Finally, we observe that the CMOS op-amp circuit of Fig. 12.1 does not have an output stage. This is because it is usually required to drive only small on-chip capacitive loads.

12.1.2 Input Common-Mode Range and Output Swing

Refer to Fig. 12.1 and consider the situation when the two input terminals are tied together and connected to a voltage V_{ICM}. The lowest value of V_{ICM} has to be sufficiently large to keep Q_1 and Q_2 in saturation. Thus, the lowest value of V_{ICM} should not be lower than the voltage at the drain of Q_1 ($-V_{SS} + V_{GS3} = -V_{SS} + V_{tn} + V_{OV3}$) by more than $|V_{tp}|$, thus

$$V_{ICM} \geq -V_{SS} + V_{tn} + V_{OV3} - |V_{tp}| \tag{12.2}$$

The highest value of V_{ICM} should ensure that Q_5 remains in saturation; that is, the voltage across Q_5, V_{SD5}, should not decrease below $|V_{OV5}|$. Equivalently, the voltage at the drain of Q_5 should not go higher than $V_{DD} - |V_{OV5}|$. Thus the upper limit of V_{ICM} is

$$V_{ICM} \leq V_{DD} - |V_{OV5}| - V_{SG1}$$

or equivalently

$$V_{ICM} \leq V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}| \tag{12.3}$$

The expressions in Eqs. (12.2) and (12.3) can be combined to express the input common-mode range as

$$-V_{SS} + V_{OV3} + V_{tn} - |V_{tp}| \le V_{ICM} \le V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}| \tag{12.4}$$

As expected, the overdrive voltages, which are important design parameters, subtract from the dc supply voltages, thereby reducing the input common-mode range. It follows that from a V_{ICM} range point of view it is desirable to select the values of V_{OV} as low as possible. We observe from Eq. (12.4) that the lower limit of V_{ICM} is approximately within an overdrive voltage of $-V_{SS}$.The upper limit, however, is not as good; it is lower than V_{DD} by two overdrive voltages and a threshold voltage.

The extent of the signal swing allowed at the output of the op amp is limited at the lower end by the need to keep Q_6 saturated and at the upper end by the need to keep Q_7 saturated, thus

$$-V_{SS} + V_{OV6} \le v_O \le V_{DD} - |V_{OV7}| \tag{12.5}$$

Thus the ouput voltage can swing to within an overdrive voltage of each of the supply rails. This is a reasonably wide output swing and can be maximized by selecting values for $|V_{OV}|$ of Q_6 and Q_7 as low as possible.

An important requirement of an op-amp circuit is that it be possible for its output terminal to be connected back to its negative input terminal so that a unity-gain amplifier is obtained. For such a connection to be possible, there must be a substantial overlap between the allowable range of v_O and the allowable range of V_{ICM}. This is usually the case in the CMOS amplifier circuit under study.

EXERCISE

12.1 For a particular design of the two-stage CMOS op amp of Fig. 12.1, ±1.65-V supplies are utilized and all transistors except for Q_6 and Q_7 are operated with overdrive voltages of 0.3-V magnitude; Q_6 and Q_7 use overdrive voltages of 0.5-V magnitude. The fabrication process employed provides $V_{tn} = |V_{tp}| = 0.5$ V. Find the input common-mode range and the range allowed for v_O.
Ans. −1.35 V to 0.55 V; −1.15 V to +1.15 V

12.1.3 Voltage Gain

To determine the voltage gain and the frequency response, consider a simplified equivalent circuit model for the small-signal operation of the CMOS amplifier (Fig. 12.2), where each of the two stages is modeled as a transconductance amplifier. As expected, the input resistance is practically infinite,

$$R_{\text{in}} = \infty$$

The first-stage transconductance G_{m1} is equal to the transconductance of each of Q_1 and Q_2 (see Section 8.5),

$$G_{m1} = g_{m1} = g_{m2} \tag{12.6}$$

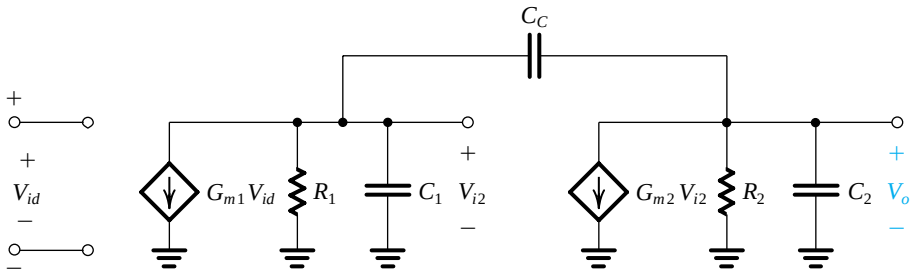


Figure 12.2 Small-signal equivalent circuit for the op amp in Fig. 12.1.

Since Q_1 and Q_2 are operated at equal bias currents ($I/2$) and equal overdrive voltages, $V_{OV1} = V_{OV2}$,

$$G_{m1} = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}} \tag{12.7}$$

Resistance R_1 represents the output resistance of the first stage, thus

$$R_1 = r_{o2} \parallel r_{o4} \tag{12.8}$$

where

$$r_{o2} = \frac{|V_{A2}|}{I/2} \tag{12.9}$$

and

$$r_{o4} = \frac{V_{A4}}{I/2} \tag{12.10}$$

The dc gain of the first stage is thus

$$A_1 = -G_{m1}R_1 \tag{12.11}$$

$$= -g_{m1}(r_{o2} \parallel r_{o4}) \tag{12.12}$$

$$= -\frac{2}{V_{OV1}} \Big/ \left[\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}}\right] \tag{12.13}$$

Observe that the magnitude of A_1 is increased by operating the differential-pair transistors, Q_1 and Q_2, at a low overdrive voltage, and by choosing a longer channel length to obtain larger Early voltages, $|V_A|$.

Returning to the equivalent circuit in Fig. 12.2 and leaving the discussion of the various model capacitances until Section 12.1.5, we note that the second-stage transconductance G_{m2} is given by

$$G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV6}} \tag{12.14}$$

Resistance R_2 represents the output resistance of the second stage, thus

$$R_2 = r_{o6} \| r_{o7} \tag{12.15}$$

where

$$r_{o6} = \frac{V_{A6}}{I_{D6}} \tag{12.16}$$

and

$$r_{o7} = \frac{|V_{A7}|}{I_{D7}} = \frac{|V_{A7}|}{I_{D6}} \tag{12.17}$$

The voltage gain of the second stage can now be found as

$$A_2 = -G_{m2}R_2 \tag{12.18}$$

$$= -g_{m6}(r_{o6} \| r_{o7}) \tag{12.19}$$

$$= -\frac{2}{V_{OV6}} \Big/ \left[\frac{1}{V_{A6}} + \frac{1}{|V_{A7}|}\right] \tag{12.20}$$

Here again we observe that to increase the magnitude of A_2, Q_6 has to be operated at a low overdrive voltage, and the channel lengths of Q_6 and Q_7 should be made longer.

The overall dc voltage gain can be found as the product A_1A_2,

$$A_v = A_1A_2$$

$$= G_{m1}R_1G_{m2}R_2 \tag{12.21}$$

$$= g_{m1}(r_{o2} \| r_{o4})g_{m6}(r_{o6} \| r_{o7}) \tag{12.22}$$

Note that A_v is of the order of $(g_m r_o)^2$. Thus the value of A_v will be in the range of 500 V/V to 5000 V/V.

Finally, we note that the output resistance of the op amp is equal to the output resistance of the second stage,

$$R_o = r_{o6} \| r_{o7} \tag{12.23}$$

Hence R_o can be large (i.e., in the tens-of-kilohms range). Nevertheless, as we learned from the study of negative feedback in Chapter 10, application of negative feedback that samples the op-amp output voltage results in reducing the ouput resistance by a factor equal to the amount of feedback $(1 + A\beta)$. Also, as mentioned before, CMOS op amps are rarely required to drive heavy resistive loads.

EXERCISES

12.2 The CMOS op amp of Fig. 12.1 is fabricated in a process for which $V'_{An} = |V'_{Ap}| = 20$ V/μm. Find A_1, A_2, and A_v if all devices are 1 μm long, $V_{OV1} = 0.2$ V, and $V_{OV6} = 0.5$ V. Also, find the op-amp output resistance obtained when the second stage is biased at 0.5 mA.
Ans. −100 V/V; −40 V/V; 4000 V/V; 20 kΩ

12.3 If the CMOS op amp in Fig. 12.1 is connected as a unity-gain buffer, show that the closed-loop output resistance is given by
$R_{\text{out}} \simeq 1/g_{m6}[g_{m1}(r_{o2} \| r_{o4})]$

12.1.4 Common-Mode Rejection Ratio (CMRR)

The CMRR of the two-stage op amp of Fig. 12.1 is determined by the first stage. This was analyzed in Section 8.5.4 and the result is given in Eq. (8.147), namely,

$$\text{CMRR} = [g_{m1}(r_{o2} \| r_{o4})][2g_{m3}R_{SS}] \tag{12.24}$$

where R_{SS} is the output resistance of the bias current source Q_5. Observe that CMRR is of the order of $(g_m r_o)^2$ and thus can be reasonably high. Also, since $g_m r_o$ is proportional to $V_A/V_{OV} = V'_A L/V_{OV}$, the CMRR is increased if long channels are used, especially for Q_5, and the transistors are operated at low overdrive voltages.

12.1.5 Frequency Response

Refer to the equivalent circuit in Fig. 12.2. Capacitance C_1 is the total capacitance between the output node of the first stage and ground, thus

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6} \tag{12.25}$$

Capacitance C_2 represents the total capacitance between the output node of the op amp and ground and includes whatever load capacitance C_L that the amplifier is required to drive, thus

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L \tag{12.26}$$

Usually, C_L is larger than the transistor capacitances, with the result that C_2 becomes much larger than C_1. Finally, note that C_{gd6} should be shown in parallel with C_C but has been ignored because C_C is usually much larger.

The equivalent circuit of Fig. 12.2 was analyzed in detail in Section 9.8.2, where it was found that it has two poles and a positive real-axis zero with the following approximate frequencies:

$$f_{P1} \simeq \frac{1}{2\pi R_1 G_{m2} R_2 C_C} \tag{12.27}$$

$$f_{P2} \simeq \frac{G_{m2}}{2\pi C_2} \tag{12.28}$$

$$f_Z \simeq \frac{G_{m2}}{2\pi C_C} \tag{12.29}$$

Here, f_{P1} is the dominant pole formed by the interaction of Miller-multiplied C_C [i.e., $(1 + G_{m2}R_2)C_C \simeq G_{m2}R_2C_C$] and R_1. To achieve the goal of a uniform –20-dB/decade gain rolloff down to 0 dB, the unity-gain frequency f_t,

$$f_t = |A_v| f_{P1} \tag{12.30}$$

$$= \frac{G_{m1}}{2\pi C_C} \tag{12.31}$$

must be lower than f_{P2} and f_Z, thus the design must satisfy the following two conditions

$$\frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2} \tag{12.32}$$

and

$$G_{m1} < G_{m2} \tag{12.33}$$

Simplified Equivalent Circuit The uniform –20-dB/decade gain rolloff obtained at frequencies $f \gg f_{P1}$ suggests that at these frequencies, the op amp can be represented by the simplified equivalent circuit shown in Fig. 12.3. Observe that this attractive simplification is based on the assumption that the gain of the second stage, $|A_2|$, is large, and hence a virtual ground appears at the input terminal of the second stage. The second stage then effectively acts as an integrator that is fed with the output current signal of the first stage; $G_{m1}V_{id}$. Although derived for the CMOS amplifier, this simplified equivalent circuit is general and applies to a variety of two-stage op amps, including the first two stages of the 741-type bipolar op amp studied later in this chapter.

Phase Margin The frequency compensation scheme utilized in the two-stage CMOS amplifier is of the pole-splitting type, studied in Section 10.13.3: It provides a dominant low-frequency pole with frequency f_{P1} and shifts the second pole beyond f_t. Figure 12.4 shows a

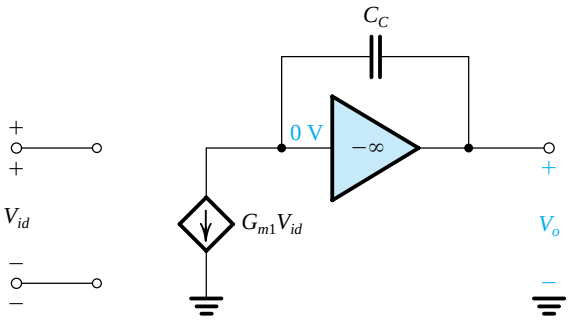


Figure 12.3 An approximate high-frequency equivalent circuit of the two-stage op amp. This circuit applies for frequencies $f \gg f_{P1}$.

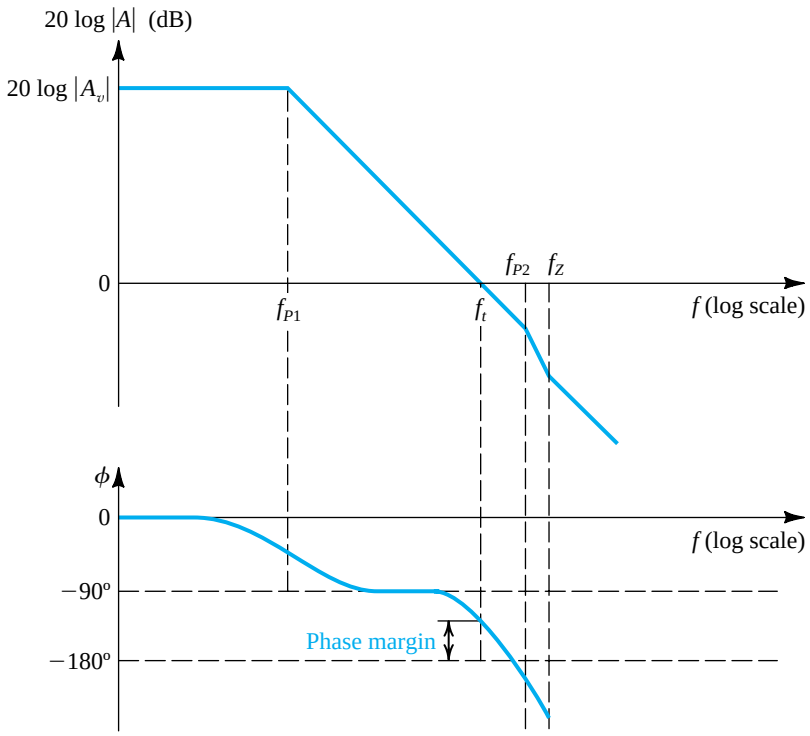


Figure 12.4 Typical frequency response of the two-stage op amp.

representative Bode plot for the gain magnitude and phase. Note that at the unity-gain frequency f_t, the phase lag exceeds the 90° caused by the dominant pole at f_{P1}. This so-called excess phase shift is due to the second pole,

$$\phi_{P2} = -\tan^{-1}\left(\frac{f_t}{f_{P2}}\right) \tag{12.34}$$

and the right-half-plane zero,

$$\phi_Z = -\tan^{-1}\left(\frac{f_t}{f_Z}\right) \tag{12.36}$$

Thus the phase lag at $f = f_t$ will be

$$\phi_{\text{total}} = 90° + \tan^{-1}(f_t/f_{P2}) + \tan^{-1}(f_t/f_Z) \tag{12.37}$$

and thus the phase margin will be

$$\begin{aligned}\text{Phase margin} &= 180° - \phi_{\text{total}} \\ &= 90° - \tan^{-1}(f_t/f_{P2}) - \tan^{-1}(f_t/f_Z)\end{aligned} \tag{12.38}$$

From our study of the stability of feedback amplifiers in Section 10.12.2, we know that the magnitude of the phase margin significantly affects the closed-loop gain. Therefore, obtaining a desired minimum value of phase margin is usually a design requirement.

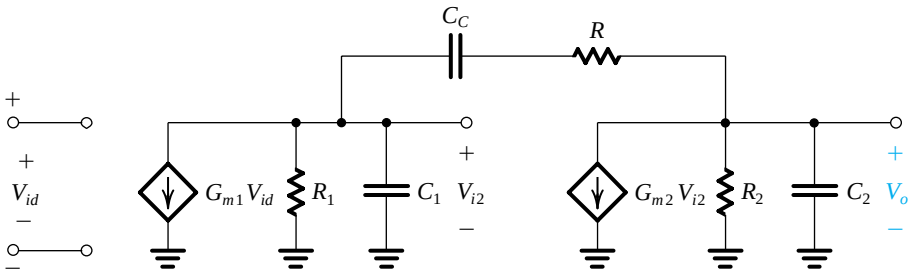


Figure 12.5 Small-signal equivalent circuit of the op amp in Fig. 12.1 with a resistance R included in series with C_C.

The problem of the additional phase lag provided by the right-half-plane zero has a rather simple and elegant solution: By including a resistance R in series with C_C, as shown in Fig. 12.5, the transmission zero can be moved to other less-harmful locations. To find the new location of the transmission zero, set $V_o = 0$. Then, the current through C_C and R will be $V_{i2}/(R + 1/sC_C)$, and a node equation at the output yields

$$\frac{V_{i2}}{R + \dfrac{1}{sC_C}} = G_{m2}V_{i2}$$

Thus the zero is now at

$$s = 1/C_C\left(\frac{1}{G_{m2}} - R\right) \tag{12.39}$$

We observe that by selecting $R = 1/G_{m2}$, we can place the zero at infinite frequency. An even better choice would be to select R greater than $1/G_{m2}$, thus placing the zero at a negative real-axis location where the phase it introduces *adds* to the phase margin.

EXERCISE

12.4 A particular implementation of the CMOS amplifier of Figs. 12.1 and 12.2 provides $G_{m1} = 1$ mA/V, $G_{m2} = 2$ mA/V, $r_{o2} = r_{o4} = 100$ kΩ, $r_{o6} = r_{o7} = 40$ kΩ, and $C_2 = 1$ pF.
(a) Find the value of C_C that results in $f_t = 100$ MHz. What is the 3-dB frequency of the open-loop gain?
(b) Find the value of the resistance R that when placed in series with C_C causes the transmission zero to be located at infinite frequency.
(c) Find the frequency of the second pole and hence find the excess phase lag at $f = f_t$, introduced by the second pole, and the resulting phase margin assuming that the situation in (b) pertains.
Ans. 1.6 pF; 50 kHz; 500 Ω; 318 MHz; 17.4°; 72.6°

12.1.6 Slew Rate

The slew-rate limitation of op amps is discussed in Chapter 2. Here, we shall illustrate the origin of the slewing phenomenon in the context of the two-stage CMOS amplifier under study.

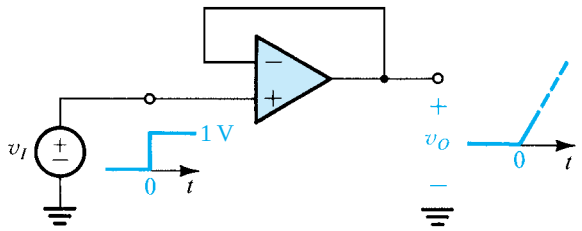


Figure 12.6 A unity-gain follower with a large step input. Since the output voltage cannot change immediately, a large differential voltage appears between the op-amp input terminals.

Consider the unity-gain follower of Fig. 12.6 with a step of, say, 1 V applied at the input. Because of the amplifier dynamics, its output will not change in zero time. Thus, immediately after the input is applied, the entire value of the step will appear as a differential signal between the two input terminals. In all likelihood, such a large signal will exceed the voltage required to turn off one side of the input differential pair ($\sqrt{2}V_{OV1}$: see earlier illustration, Fig. 8.6) and switch the entire bias current I to the other side. Reference to Fig. 12.1 shows that for our example, Q_2 will turn off, and Q_1 will conduct the entire current I. Thus Q_4 will sink a current I that will be pulled from C_C, as shown in Fig. 12.7. Here, as we did in Fig. 12.3, we are modeling the second stage as an ideal integrator. We see that the output voltage will be a ramp with a slope of I/C_C:

$$v_o(t) = \frac{I}{C_C}t$$

Thus the slew rate, SR, is given by

$$SR = \frac{I}{C_C} \tag{12.40}$$

It should be pointed out, however, that this is a rather simplified model of the slewing process.

Relationship Between SR and f_t A simple relationship exists between the unity-gain bandwidth f_t and the slew rate SR. This relationship can be found by combining Eqs. (12.31)

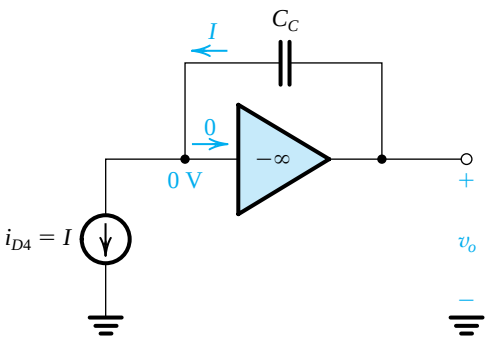


Figure 12.7 Model of the two-stage CMOS op-amp of Fig. 12.1 when a large differential voltage is applied.

and (12.40) and noting that $G_{m1} = g_{m1} = I/V_{OV1}$, to obtain

$$SR = 2\pi f_t V_{OV} \tag{12.41}$$

or equivalently,

$$SR = V_{OV}\omega_t \tag{12.42}$$

Thus, for a given ω_t, the slew rate is determined by the overdrive voltage at which the first-stage transistors are operated. A higher slew rate is obtained by operating Q_1 and Q_2 at a larger V_{OV}. Now, for a given bias current I, a larger V_{OV} is obtained if Q_1 and Q_2 are p-channel devices. This is an important reason for using p-channel rather than n-channel devices in the first stage of the CMOS op amp. Another reason is that it allows the second stage to employ an n-channel device. Now, since n-channel devices have greater transconductances than corresponding p-channel devices, G_{m2} will be high, resulting in a higher second-pole frequency and a correspondingly higher ω_t. However, the price paid for these improvements is a lower G_{m1} and hence a lower dc gain.

EXERCISE

12.5 Find SR for the CMOS op amp of Fig. 12.1 for the case $f_t = 100$ MHz and $V_{OV1} = 0.2$ V. If $C_C = 1.6$ pF, what must the bias current I be?
Ans. 126 V/μs; 200 μA

12.1.7 Power-Supply Rejection Ratio (PSRR)

CMOS op amps are usually utilized in what are known as **mixed-signal circuits**: IC chips that combine analog and digital circuits. In such circuits, the switching activity in the digital portion usually results in increased ripple on the power supplies. A portion of the supply ripple can make its way to the op-amp output and thus corrupt the output signal. The traditional approach for reducing supply ripple by connecting large capacitances between the supply rails and ground is not viable in IC design, as such capacitances would consume most of the chip area. Instead, the analog IC designer has to pay attention to another op-amp specification that so far we have ignored, namely, the power-supply rejection ratio (PSRR).

The PSRR is defined as the ratio of the amplifier differential gain to the gain experienced by a change in the power-supply voltage (v_{dd} and v_{ss}). For circuits utilizing two power supplies, we define

$$\text{PSRR}^+ \equiv \frac{A_d}{A^+} \tag{12.42}$$

and

$$\text{PSRR}^- = \frac{A_d}{A^-} \tag{12.43}$$

where

$$A^+ \equiv \frac{v_o}{v_{dd}} \tag{12.44}$$

$$A^- = \frac{v_o}{v_{ss}} \tag{12.45}$$

Obviously, to minimize the effect of the power-supply ripple, we require the op amp to have a large PSRR.

A detailed analysis of the PSRR of the two-stage CMOS op amp is beyond the scope of this book (see Gray et al., 2009). Nevertheless, we make the following brief remarks. It can be shown that the circuit is remarkably insensitive to variations in V_{DD}, and thus PSRR^+ is very high. This is not the case, however, for the negative-supply ripple v_{ss}, which is coupled to the output primarily through the second-stage transistors Q_6 and Q_7. In particular, the portion of v_{ss} that appears at the op-amp output is determined by the voltage divider formed by the output resistances of Q_6 and Q_7,

$$v_o = v_{ss} \frac{r_{o7}}{r_{o6} + r_{o7}} \tag{12.46}$$

Thus,

$$A^- \equiv \frac{v_o}{v_{ss}} = \frac{r_{o7}}{r_{o6} + r_{o7}} \tag{12.47}$$

Now utilizing A_d from Eq. (12.22) gives

$$\text{PSRR}^- \equiv \frac{A_d}{A^-} = g_{m1}(r_{o2} \| r_{o4}) g_{m6} r_{o6} \tag{12.48}$$

Thus, PSRR^- is of the form $(g_m r_o)^2$ and therefore is maximized by selecting long channels L (to increase $|V_A|$), and operating at low $|V_{OV}|$.

12.1.8 Design Trade-offs

The performance parameters of the two-stage CMOS amplifier are primarily determined by two design parameters:

1. The length L used for the channel of each MOSFET.
2. The overdrive voltage $|V_{OV}|$ at which each transistor is operated.

Throughout this section, we have found that a larger L and correspondingly larger $|V_A|$ increases the amplifier gain, CMRR and PSRR. We also found that operating at a lower $|V_{OV}|$ increases these three parameters as well as increasing the input common-mode range and the allowable range of output swing. Also, although we have not analyzed the offset voltage of the op amp here, we know from our study of the subject in Section 8.4.1 that a number of the components of the input offset voltage that arises from random device mismatches are proportional to $|V_{OV}|$ at which the MOSFETs of the input differential pair are operated. Thus the offset is minimized by operating at a lower $|V_{OV}|$.

There is, however, an important MOSFET performance parameter that requires the selection of a larger $|V_{OV}|$, namely, the **transition frequency** f_T, which determines the high-frequency performance of the MOSFET,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{12.49}$$

For an *n*-channel MOSFET, we can show that (see Appendix 7.A)

$$f_T \simeq \frac{1.5\mu_n V_{OV}}{2\pi L^2} \tag{12.50}$$

A similar relationship applies for the PMOS transistor, with μ_p and $|V_{OV}|$ replacing μ_n and V_{OV}, respectively. Thus to increase f_T and improve the high-frequency response of the op amp, we need to use a larger overdrive value and, not surprisingly, shorter channels. A larger $|V_{OV}|$ also results in a higher op-amp slew rate *SR* (Eq. 12.41). Finally, note that the selection of a larger $|V_{OV}|$ results, for the same bias current, in a smaller *W*/*L*, which combined with a short *L* leads to smaller devices and hence lower values of MOSFET capacitances and higher frequencies of operation.

In conclusion, the selection of $|V_{OV}|$ presents the designer with a trade-off between improving the low-frequency performance parameters on the one hand and the high-frequency performance on the other. For modern submicron technologies, which require operation from power supplies of 1 V to 1.5 V, overdrive voltages between 0.1 V and 0.3 V are typically utilized. For these process technologies, analog designers typically use channel lengths that are at least 1.5 to 2 times the specified value of $L_{\min}$, and even longer channels are used for current-source bias transistors.

Example 12.1

We conclude our study of the two-stage CMOS op amp with a design example. Let it be required to design the circuit to obtain a dc gain of 4000 V/V. Assume that the available fabrication technology is of the 0.5-μm type for which $V_{tn} = |V_{tp}| = 0.5$ V, $k'_n = 200$ μA/V^2, $k'_p = 80$ μA/V^2, $V'_{An} = |V'_{Ap}| = 20$ V/μm, and $V_{DD} = V_{SS} = 1.65$ V. To achieve a reasonable dc gain per stage, use $L = 1$ μm for all devices. Also, for simplicity, operate all devices at the same $|V_{OV}|$, in the range of 0.2 V to 0.4 V. Use $I = 200$ μA, and to obtain a higher G_{m2}, and hence a higher f_{P2}, use $I_{D6} = 0.5$ mA. Specify the *W*/*L* ratios for all transistors. Also give the values realized for the input common-mode range, the maximum possible output swing, R_{in} and R_o. Also determine the CMRR and PSRR realized. If $C_1 = 0.2$ pF and $C_2 = 0.8$ pF, find the required values of C_C and the series resistance *R* to place the transmission zero at $s = \infty$ and to obtain the highest possible f_t consistent with a phase margin of 75°. Evaluate the values obtained for f_t and *SR*.

Solution

Using the voltage-gain expression in Eq. (12.22),

$$\begin{aligned} A_v &= g_{m1}(r_{o2} \parallel r_{o4}) g_{m6}(r_{o6} \parallel r_{o7}) \\ &= \frac{2(I/2)}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times \frac{2I_{D6}}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{I_{D6}} \\ &= \left(\frac{V_A}{V_{OV}}\right)^2 \end{aligned}$$

To obtain $A_v = 4000$, given $V_A = 20$ V,

$$4000 = \frac{400}{V_{OV}^2}$$

$$V_{OV} = 0.316 \text{ V}$$

To obtain the required (W/L) ratios of Q_1 and Q_2,

$$I_{D1} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_1 V_{OV}^2$$

$$100 = \frac{1}{2}\times 80\left(\frac{W}{L}\right)_1 \times 0.316^2$$

Thus,

$$\left(\frac{W}{L}\right)_1 = \frac{25\ \mu\text{m}}{1\ \mu\text{m}}$$

and

$$\left(\frac{W}{L}\right)_2 = \frac{25\ \mu\text{m}}{1\ \mu\text{m}}$$

For Q_3 and Q_4 we write

$$100 = \frac{1}{2}\times 200\left(\frac{W}{L}\right)_3 \times 0.316^2$$

to obtain

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{10\ \mu\text{m}}{1\ \mu\text{m}}$$

For Q_5,

$$200 = \frac{1}{2}\times 80\left(\frac{W}{L}\right)_5 \times 0.316^2$$

Thus,

$$\left(\frac{W}{L}\right)_5 = \frac{50\ \mu\text{m}}{1\ \mu\text{m}}$$

Since Q_7 is required to conduct 500 μA, its (W/L) ratio should be 2.5 times that of Q_5,

$$\left(\frac{W}{L}\right)_7 = 2.5\left(\frac{W}{L}\right)_5 = \frac{125\ \mu\text{m}}{1\ \mu\text{m}}$$

For Q_6 we write

$$500 = \frac{1}{2}\times 200\times\left(\frac{W}{L}\right)_6 \times 0.316^2$$

Thus,

$$\left(\frac{W}{L}\right)_6 = \frac{50\ \mu\text{m}}{1\ \mu\text{m}}$$

Example 12.1 *continued*

Finally, let's select $I_{\text{REF}} = 20\ \mu\text{A}$, thus

$$\left(\frac{W}{L}\right)_8 = 0.1\left(\frac{W}{L}\right)_5 = \frac{5\ \mu\text{m}}{1\ \mu\text{m}}$$

The input common-mode range can be found using the expression in Eq. (12.4) as

$$-1.33\ \text{V} \le V_{ICM} \le 0.52\ \text{V}$$

The maximum signal swing allowable at the output is found using the expression in Eq. (12.5) as

$$-1.33\ \text{V} \le v_O \le 1.33\ \text{V}$$

The input resistance is practically infinite, and the output resistance is

$$R_o = r_{o6} \parallel r_{o7} = \frac{1}{2} \times \frac{20}{0.5} = 20\ \text{k}\Omega$$

The CMRR is determined using Eq. (12.24),

$$\text{CMRR} = g_{m1}(r_{o2} \parallel r_{o4})(2g_{m3}R_{SS})$$

where $R_{SS} = r_{o5} = V_A/I$. Thus,

$$\text{CMRR} = \frac{2(I/2)}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times 2 \times \frac{2(I/2)}{V_{OV}} \times \frac{V_A}{I}$$

$$= 2\left(\frac{V_A}{V_{OV}}\right)^2 = 2\left(\frac{20}{0.316}\right)^2 = 8000$$

Expressed in decibels, we have

$$\text{CMRR} = 20 \log 8000 = 78\ \text{dB}$$

The PSRR is determined using Eq. (12.48):

$$\text{PSRR} = g_{m1}(r_{o2} \parallel r_{o4})g_{m6}r_{o6}$$

$$= \frac{2(I/2)}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times \frac{2I_{D6}}{V_{OV}} \times \frac{V_A}{I_{D6}}$$

$$= 2\left(\frac{V_A}{V_{OV}}\right)^2 = 2\left(\frac{20}{0.316}\right)^2 = 8000$$

or, expressed in decibels,

$$\text{PSRR} = 20 \log 8000 = 78\ \text{dB}$$

To determine f_{P2} we use Eq. (12.28) and substitute for G_{m2},

$$G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV}} = \frac{2 \times 0.5}{0.316} = 3.2\ \text{mA/V}$$

Thus,

$$f_{P2} = \frac{3.2 \times 10^{-3}}{2\pi \times 0.8 \times 10^{-12}} = 637\ \text{MHz}$$

To move the transmission zero to $s = \infty$, we select the value of R as

$$R = \frac{1}{G_{m2}} = \frac{1}{3.2 \times 10^{-3}} = 316\ \Omega$$

For a phase margin of 75°, the phase shift due to the second pole at $f = f_t$ must be 15°, that is,

$$\tan^{-1}\frac{f_t}{f_{P2}} = 15°$$

Thus,

$$f_t = 637 \times \tan 15° = 171\ \text{MHz}$$

The value of C_C can be found using Eq. (12.31),

$$C_C = \frac{G_{m1}}{2\pi f_t}$$

where

$$G_{m1} = g_{m1} = \frac{2 \times 100\ \mu\text{A}}{0.316\ \text{V}} = 0.63\ \text{mA/V}$$

Thus,

$$C_{C1} = \frac{0.63 \times 10^{-3}}{2\pi \times 171 \times 10^{6}} = 0.6\ \text{pF}$$

The value of SR can now be found using Eq. (12.41) as

$$SR = 2\pi \times 171 \times 10^{6} \times 0.316$$
$$= 340\ \text{V}/\mu\text{s}$$

12.2 The Folded-Cascode CMOS Op Amp

In this section we study another type of CMOS op-amp circuit: the folded cascode. The circuit is based on the folded-cascode amplifier studied in Section 7.3.6. There, it was mentioned that although composed of a CS transistor and a CG transistor of opposite polarity, the folded-cascode configuration is generally considered to be a single-stage amplifier. Similarly, the op-amp circuit that is based on the cascode configuration is considered to be a single-stage op amp. Nevertheless, it can be designed to provide performance parameters that equal and in some respects exceed those of the two-stage topology studied in the preceding section. Indeed, the folded-cascode op-amp topology is currently as popular as the two-stage structure. Furthermore, the folded-cascode configuration can be used in conjunction with the two-stage structure to provide performance levels higher than those available from either circuit alone.

12.2.1 The Circuit

Figure 12.8 shows the structure of the CMOS folded-cascode op amp. Here, Q_1 and Q_2 form the input differential pair, and Q_3 and Q_4 are the cascode transistors. Recall that for

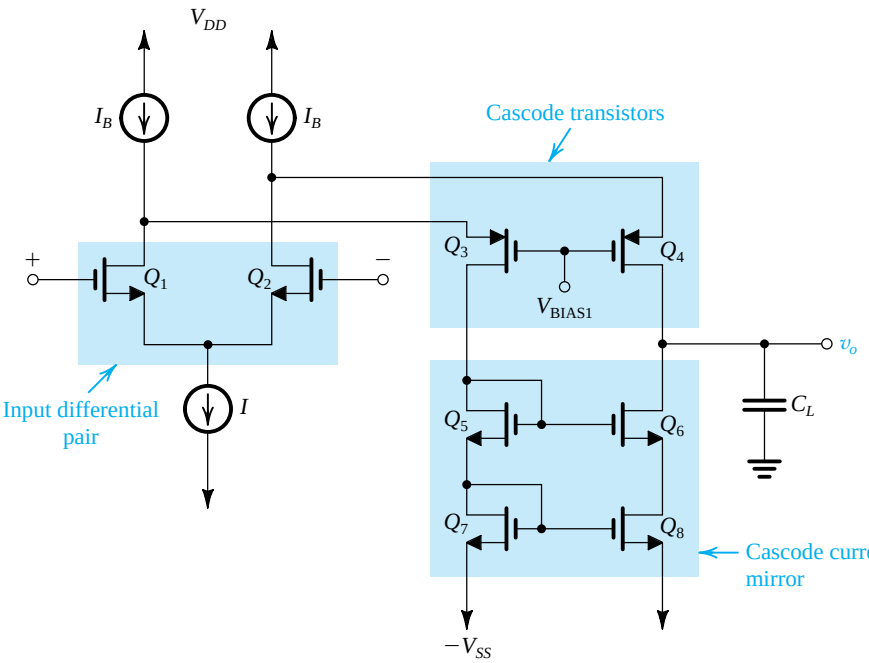


Figure 12.8 Structure of the folded-cascode CMOS op amp.

differential input signals, each of Q_1 and Q_2 acts as a common-source amplifier. Also note that the gate terminals of Q_3 and Q_4 are connected to a constant dc voltage (V_{BIAS1}) and hence are at signal ground. Thus, for differential input signals, each of the transistor pairs Q_1–Q_3 and Q_2–Q_4 acts as a folded-cascode amplifier, such as the one in Fig. 7.16. Note that the input differential pair is biased by a constant-current source I. Thus each of Q_1 and Q_2 is operating at a bias current $I/2$. A node equation at each of their drains shows that the bias current of each of Q_3 and Q_4 is $(I_B - I/2)$. Selecting $I_B = I$ forces all transistors to operate at the same bias current of $I/2$. For reasons that will be explained shortly, however, the value of I_B is usually made somewhat greater than I.

As we learned in Chapter 7, if the full advantage of the high output-resistance achieved through cascoding is to be realized, the output resistance of the current-source load must be equally high. This is the reason for using the cascode current mirror Q_5 to Q_8, in the circuit of Fig. 12.8. (This current-mirror circuit was studied in Section 7.5.1.) Finally, note that capacitance C_L denotes the total capacitance at the output node. It includes the internal transistor capacitances, an actual load capacitance (if any), and possibly an additional capacitance deliberately introduced for the purpose of frequency compensation. In many cases, however, the load capacitance will be sufficiently large, obviating the need to provide additional capacitance to achieve the desired frequency compensation. This topic will be discussed shortly. For the time being, we note that unlike the two-stage circuit, that requires the introduction of a separate compensation capacitor C_C, here the load capacitance contributes to frequency compensation.

A more complete circuit for the CMOS folded-cascode op amp is shown in Fig. 12.9. Here we show the two transistors Q_9 and Q_{10}, which provide the constant bias currents I_B, and transistor Q_{11}, which provides the constant current I utilized for biasing the differential pair. Observe that the details for generating the bias voltages V_{BIAS1}, V_{BIAS2}, and V_{BIAS3} are not

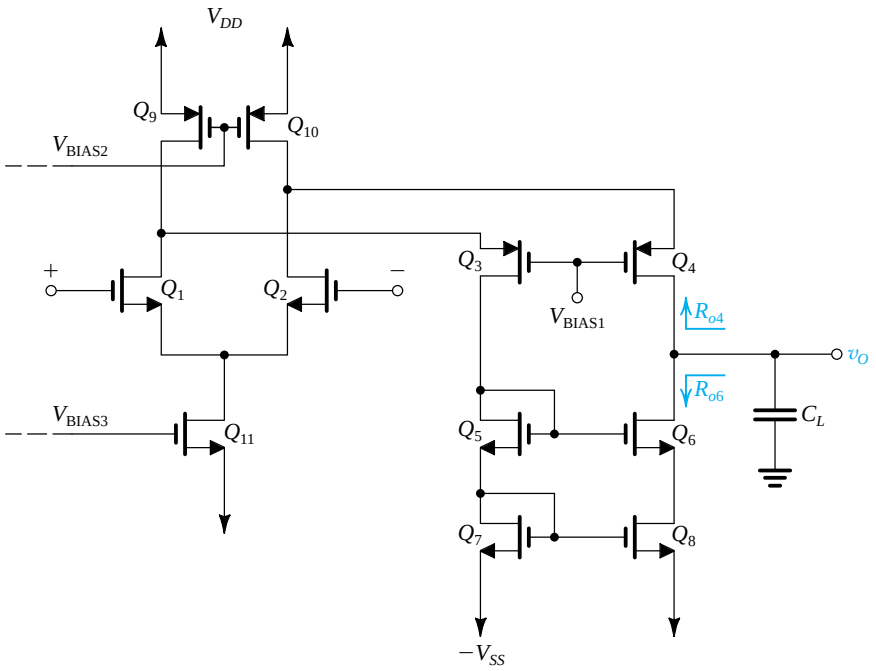


Figure 12.9 A more complete circuit for the folded-cascode CMOS amplifier of Fig. 12.8.

shown. Nevertheless, we are interested in how the values of these voltages are to be selected. Toward that end, we evaluate the input common-mode range and the allowable output swing.

12.2.2 Input Common-Mode Range and Output Swing

To find the input common-mode range, let the two input terminals be tied together and connected to a voltage V_{ICM}. The maximum value of V_{ICM} is limited by the requirement that Q_1 and Q_2 operate in saturation at all times. Thus $V_{ICM\max}$ should be at most V_{tn} volts above the voltage at the drains of Q_1 and Q_2. The latter voltage is determined by V_{BIAS1} and must allow for a voltage drop across Q_9 and Q_{10} at least equal to their overdrive voltage, $|V_{OV9}| = |V_{OV10}|$. Assuming that Q_9 and Q_{10} are indeed operated at the edge of saturation, $V_{ICM\max}$ will be

$$V_{ICM\max} = V_{DD} - |V_{OV9}| + V_{tn} \tag{12.51}$$

which can be larger than V_{DD}, a significant improvement over the case of the two-stage circuit. The value of V_{BIAS2} should be selected to yield the required value of I_B while operating Q_9 and Q_{10} at a small value of $|V_{OV}|$ (e.g., 0.2 V or so). The minimum value of V_{ICM} can be obtained as

$$V_{ICM\min} = -V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \tag{12.52}$$

The presence of the threshold voltage V_{tn} in this expression indicates that $V_{ICM\min}$ is not sufficiently low. Later in this section we shall describe an ingenious technique for solving this problem. For the time being, note that the value of V_{BIAS3} should be selected to provide the

required value of I while operating Q_{11} at a low overdrive voltage. Combining Eqs. (12.51) and (12.52) provides

$$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \le V_{ICM} \le V_{DD} - |V_{OV9}| + V_{tn} \tag{12.53}$$

The upper end of the allowable range of v_O is determined by the need to maintain Q_{10} and Q_4 in saturation. Note that Q_{10} will operate in saturation as long as an overdrive voltage, $|V_{OV10}|$, appears across it. It follows that to maximize the allowable positive swing of v_O (and V_{ICMmax}), we should select the value of V_{BIAS1} so that Q_{10} operates at the edge of saturation, that is,

$$V_{BIAS1} = V_{DD} - |V_{OV10}| - V_{SG4} \tag{12.54}$$

The upper limit of v_O will then be

$$v_{Omax} = V_{DD} - |V_{OV10}| - |V_{OV4}| \tag{12.55}$$

which is two overdrive voltages below V_{DD}. The situation is not as good, however, at the other end: Since the voltage at the gate of Q_6 is $-V_{SS} + V_{GS7} + V_{GS5}$ or equivalently $-V_{SS} + V_{OV7} + V_{OV5} + 2V_{tn}$, the lowest possible v_O is obtained when Q_6 reaches the edge of saturation, namely, when v_O decreases below the voltage at the gate of Q_6 by V_{tn}, that is,

$$v_{Omin} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn} \tag{12.56}$$

Note that this value is two overdrive voltages *plus* a threshold voltage above $-V_{SS}$. This is a drawback of utilizing the cascode mirror. The problem can be alleviated by using a modified mirror circuit, as we shall shortly see.

EXERCISE

12.6 For a particular design of the folded-cascode op amp of Fig. 12.9, ±1.65-V supplies are utilized and all transistors are operated at overdrive voltages of 0.3-V magnitude. The fabrication process employed provides $V_{tn} = |V_{tp}| = 0.5$ V. Find the input common-mode range and the range allowed for v_O.

Ans. –0.55 V to +1.85 V; –0.55 V to +1.05 V.

12.2.3 Voltage Gain

The folded-cascode op amp is simply a transconductance amplifier with an infinite input resistance, a transconductance G_m and an output resistance R_o. G_m is equal to g_m of each of the two transistors of the differential pair,

$$G_m = g_{m1} = g_{m2} \tag{12.57}$$

Thus,

$$G_m = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}} \tag{12.58}$$

The output resistance R_o is the parallel equivalent of the output resistance of the cascode amplifier and the output resistance of the cascode mirror, thus

$$R_o = R_{o4} \parallel R_{o6} \tag{12.59}$$

Reference to Fig. 12.9 shows that the resistance R_{o4} is the output resistance of the CG transistor Q_4. The latter has a resistance $(r_{o2} \parallel r_{o10})$ in its source lead, thus

$$R_{o4} \simeq (g_{m4}r_{o4})(r_{o2} \parallel r_{o10}) \tag{12.60}$$

The resistance R_{o6} is the output resistance of the cascode mirror and is thus given by Eq. (7.25), thus

$$R_{o6} \simeq g_{m6}r_{o6}r_{o8} \tag{12.61}$$

Combining Eqs. (12.59) to (12.61) gives

$$R_o = [g_{m4}r_{o4}(r_{o2} \parallel r_{o10})] \parallel (g_{m6}r_{o6}r_{o8}) \tag{12.62}$$

The dc open-loop gain can now be found using G_m and R_o, as

$$A_v = G_m R_o \tag{12.63}$$

Thus,

$$A_v = g_{m1}\{[g_{m4}r_{o4}(r_{o2} \parallel r_{o10})] \parallel (g_{m6}r_{o6}r_{o8})\} \tag{12.64}$$

Figure 12.10 shows the equivalent-circuit model including the load capacitance C_L, which we shall take into account shortly.

Because the folded-cascode op amp is a transconductance amplifier, it has been given the name **operational transconductance amplifier** (**OTA**). Its very high output resistance, which is of the order of $g_m r_o^2$ (see Eq. 12.62) is what makes it possible to realize a relatively high voltage gain in a single amplifier stage. However, such a high output resistance may be a cause of concern to the reader; after all, in Chapter 2, we stated that an ideal op amp has a zero output resistance! To alleviate this concern somewhat, let us find the closed-loop output resistance of a unity-gain follower formed by connecting the output terminal of the circuit of Fig. 12.9 back to the negative input terminal. Since this feedback is of the voltage sampling type, it reduces the output resistance by the factor $(1 + A\beta)$, where $A = A_v$ and $\beta = 1$, that is,

$$R_{of} = \frac{R_o}{1 + A_v} \simeq \frac{R_o}{A_v} \tag{12.65}$$

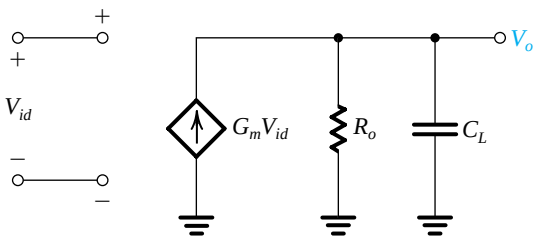


Figure 12.10 Small-signal equivalent circuit of the folded-cascode CMOS amplifier. Note that this circuit is in effect an operational transconductance amplifier (OTA).

Substituting for A_v from Eq. (12.63) gives

$$R_{of} \simeq \frac{1}{G_m} \tag{12.66}$$

which is a general result that applies to any OTA to which 100% voltage feedback is applied. For our particular circuit, $G_m = g_{m1}$, thus

$$R_{of} = 1/g_{m1} \tag{12.67}$$

Since g_{m1} is of the order of 1 mA/V, R_{of} will be of the order of 1 kΩ. Although this is not very small, it is reasonable in view of the simplicity of the op-amp circuit as well as the fact that this type of op amp is not usually intended to drive low-valued resistive loads.

EXERCISE

12.7 The CMOS op amp of Figs. 12.8 and 12.9 is fabricated in a process for which $V'_{An} = |V'_{Ap}| = 20$ V/μm. If all devices have 1-μm channel length and are operated at equal overdrive voltages of 0.2-V magnitude, find the voltage gain obtained. If each of Q_1 to Q_8 is biased at 100 μA, what value of R_o is obtained?

Ans. 13,333 V/V; 13.3 MΩ

12.2.4 Frequency Response

From Section 9.6, we know that one of the advantages of the cascode configuration is its excellent high-frequency response. It has poles at the input, at the connection between the CS and CG transistors (i.e., at the source terminals of Q_3 and Q_4), and at the output terminal. Normally, the first two poles are at very high frequencies, especially when the resistance of the signal generator that feeds the differential pair is small. Since the primary purpose of CMOS op amps is to feed capacitive loads, C_L is usually large, and the pole at the output becomes dominant. Even if C_L is not large, we can increase it deliberately to give the op amp a dominant pole. From Fig. 12.10 we can write

$$\frac{V_o}{V_{id}} = \frac{G_m R_o}{1 + sC_L R_o} \tag{12.68}$$

Thus, the dominant pole has a frequency f_P,

$$f_P = \frac{1}{2\pi C_L R_o} \tag{12.69}$$

and the unity-gain frequency f_t will be

$$f_t = G_m R_o f_P = \frac{G_m}{2\pi C_L} \tag{12.70}$$

From a design point of view, the value of C_L should be such that at $f = f_t$ the excess phase resulting from the nondominant poles is small enough to permit the required phase margin to be achieved. If C_L is not large enough to achieve this purpose, it can be augmented.

It is important to note the different effects of increasing the load capacitance on the operation of the two op-amp circuits we have studied. In the two-stage circuit, if C_L is increased, the frequency of the second pole decreases, the excess phase shift at $f = f_t$ increases, and the phase margin is reduced. Here, on the other hand, when C_L is increased, f_t decreases, but the phase margin increases. In other words, a heavier capacitive load decreases the bandwidth of the folded-cascode amplifier but does not impair its response (which happens when the phase margin decreases). Of course, if an increase in C_L is anticipated in the two-stage op-amp case, the designer can increase C_C, thus decreasing f_t and restoring the phase margin to its required value.

12.2.5 Slew Rate

As discussed in Section 12.1.6, slewing occurs when a large differential input signal is applied. Refer to Fig. 12.8 and consider the case of a large signal V_{id} applied so that Q_2 cuts off and Q_1 conducts the entire bias current I. We see that Q_3 will now carry a current $(I_B - I)$, and Q_4 will conduct a current I_B. The current mirror will see an input current of $(I_B - I)$ through Q_5 and Q_7 and thus its output current in the drain of Q_6 will be $(I_B - I)$. It follows that at the output node the current that will flow into C_L will be $I_4 - I_6 = I_B - (I_B - I) = I$. Thus the output v_O will be a ramp with a slope of I/C_L which is the slew rate,

$$SR = \frac{I}{C_L} \tag{12.71}$$

Note that the reason for selecting $I_B > I$ is to avoid turning off the current mirror completely; if the current mirror turns off, the output distortion increases. Typically, I_B is set 10% to 20% larger than I. Finally, Eqs. (12.70), (12.71), and (12.58) can be combined to obtain the following relationship between SR and f_t

$$SR = 2\pi f_t V_{OV1} \tag{12.72}$$

which is identical to the corresponding relationship in the case of the two-stage design. Note, however, that this relationship applies only when $I_B > I$.

Example 12.2

Consider a design of the folded-cascode op amp of Fig. 12.9 for which $I = 200$ μA, $I_B = 250$ μA, and $|V_{OV}|$ for all transistors is 0.25 V. Assume that the fabrication process provides $k_n' = 100$ μA/V^2, $k_p' = 40$ μA/V^2, $|V_A'| = 20$ V/μm. $V_{DD} = V_{SS} = 2.5$ V, and $|V_t| = 0.75$ V. Let all transistors have $L = 1$ μm and assume that $C_L = 5$ pF. Find I_D, g_m, r_o, and W/L for all transistors. Find the allowable range of V_{ICM} and of the output voltage swing. Determine the values of A_v, f_t, f_P, and SR. What is the power dissipation of the op amp?

Solution

From the given values of I and I_B we can determine the drain current I_D for each transistor. The transconductance of each device is found using

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2I_D}{0.25}$$

Example 12.2 *continued*

and the output resistance r_o from

$$r_o = \frac{|V_A|}{I_D} = \frac{20}{I_D}$$

The W/L ratio for each transistor is determined from

$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{k'V_{OV}^2}$$

The results are as follows:

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
I_D (μA)	100	100	150	150	150	150	150	150	250	250	200
g_m (mA/V)	0.8	0.8	1.2	1.2	1.2	1.2	1.2	1.2	2.0	2.0	1.6
r_o (kΩ)	200	200	133	133	133	133	133	133	80	80	100
W/L	32	32	120	120	48	48	48	48	200	200	64

Note that for all transistors,

$$g_m r_o = 160 \text{ V/V}$$

$$V_{GS} = 1.0 \text{ V}$$

Using the expression in Eq. (12.53), the input common-mode range is found to be

$$-1.25 \text{ V} \le V_{ICM} \le 3 \text{ V}$$

The output voltage swing is found using Eqs. (12.55) and (12.56) to be

$$-1.25 \text{ V} \le v_O \le 2 \text{ V}$$

To obtain the voltage gain, we first determine R_{o4} using Eq. (12.60) as

$$R_{o4} = 160(200 \,\|\, 80) = 9.14 \text{ MΩ}$$

and R_{o6} using Eq. (12.61) as

$$R_{o6} = 21.28 \text{ MΩ}$$

The output resistance R_o can then be found as

$$R_o = R_{o4} \,\|\, R_{o6} = 6.4 \text{ MΩ}$$

and the voltage gain

$$A_v = G_m R_o = 0.8 \times 10^{-3} \times 6.4 \times 10^6$$

$$= 5120 \text{ V/V}$$

The unity-gain bandwidth is found using Eq. (12.70),

$$f_t = \frac{0.8 \times 10^{-3}}{2\pi \times 5 \times 10^{-12}} = 25.5 \text{ MHz}$$

Thus, the dominant-pole frequency must be

$$f_P = \frac{f_t}{A_v} = \frac{25.5 \text{ MHz}}{5120} = 5 \text{ kHz}$$

The slew rate can be determined using Eq. (12.71),

$$SR = \frac{I}{C_L} = \frac{200 \times 10^{-6}}{5 \times 10^{-12}} = 40 \text{ V/}\mu\text{s}$$

Finally, to determine the power dissipation we note that the total current is 500 μA = 0.5 mA, and the total supply voltage is 5 V, thus

$$P_D = 5 \times 0.5 = 2.5 \text{ mW}$$

12.2.6 Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation

In Section 12.2.2 we found that while the upper limit on the input common-mode range exceeds the supply voltage V_{DD}, the magnitude of lower limit is significantly lower than V_{SS}. The opposite situation occurs if the input differential amplifier is made up of PMOS transistors. It follows that an NMOS and a PMOS differential pair placed in parallel would provide an input stage with a common-mode range that exceeds the power supply voltage in both directions. This is known as rail-to-rail input operation. Figure 12.11 shows such an arrangement. To keep the diagram simple, we have not shown the parallel connection of the two differential pairs: The two positive-input terminals are to be connected together and the two negative-input terminals are to be tied together. Transistors Q_5 and Q_6 are the cascode transistors for the Q_1–Q_2 pair, and transistors Q_7 and Q_8 are the cascode devices for the Q_3–Q_4 pair. The output voltage V_o is shown taken differentially between the drains of the cascode devices. To obtain a single-ended output, a differential-to-single-ended conversion circuit should be connected in cascade.

Figure 12.11 indicates by arrows the direction of the current increments that result from the application of a positive differential input signal V_{id}. Each of the current increments indicated is equal to $G_m(V_{id}/2)$ where $G_m = g_{m1} = g_{m2} = g_{m3} = g_{m4}$. Thus the total current feeding each of the two output nodes will be $G_m V_{id}$. Now, if the output resistance between each of the two nodes and ground is denoted R_o, the output voltage will be

$$V_o = 2G_m R_o V_{id} \tag{12.73}$$

Thus the voltage gain will be

$$A_v = 2G_m R_o \tag{12.74}$$

This, however, assumes that both differential pairs will be operating simultaneously. This in turn occurs only over a limited range of V_{ICM}. Over the remainder of the input common-mode range, only one of the two differential pairs will be operational, and the gain drops to half of the value in Eq. (12.74). This rail-to-rail, folded-cascode structure is utilized in a commercially available op amp.[1]

[1]The Texas Instruments OPA357.

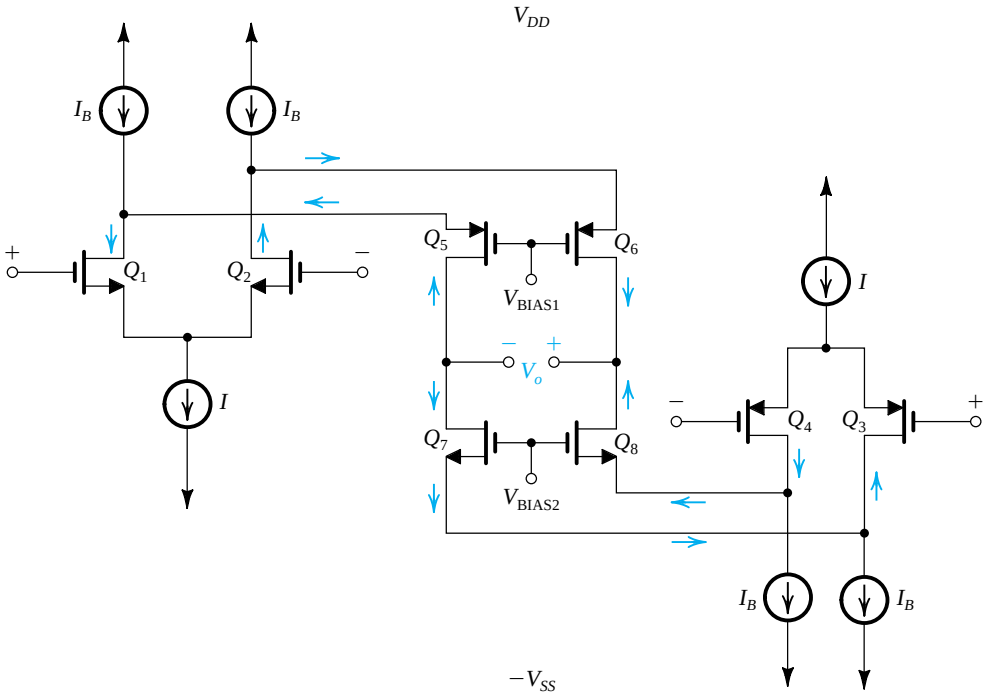


Figure 12.11 A folded-cascode op amp that employs two parallel complementary input stages to achieve rail-to-rail input common-mode operation. Note that the two "+" terminals are connected together and the two "–" terminals are connected together.

EXERCISE

12.8 For the circuit in Fig. 12.11, assume that all transistors, including those that implement the current sources, are operating at equal overdrive voltages of 0.3-V magnitude and have $|V_t| = 0.7$ V and that $V_{DD} = V_{SS} = 2.5$ V.

(a) Find the range over which the NMOS input stage operates.
(b) Find the range over which the PMOS input stage operates.
(c) Find the range over which both operate (the overlap range).
(d) Find the input common-mode range.

(Note that to operate properly, each of the current sources requires a minimum voltage of $|V_{OV}|$ across its terminals.)

Ans. –1.2 V to +2.9 V; –2.9 V to +1.2 V, –1.2 V to +1.2 V; –2.9 V to +2.9 V

12.2.7 Increasing the Output Voltage Range: The Wide-Swing Current Mirror

In Section 12.2.2 it was found that while the output voltage of the circuit of Fig. 12.9 can swing to within $2|V_{OV}|$ of V_{DD}, the cascode current mirror limits the negative swing to $[2|V_{OV}| + V_t]$ above $-V_{SS}$. In other words, the cascode mirror reduces the voltage swing by V_t volts. This point is further illustrated in Fig. 12.12(a), which shows a cascode mirror (with $V_{SS} = 0$, for simplicity) and indicates the voltages that result at the various nodes. Observe

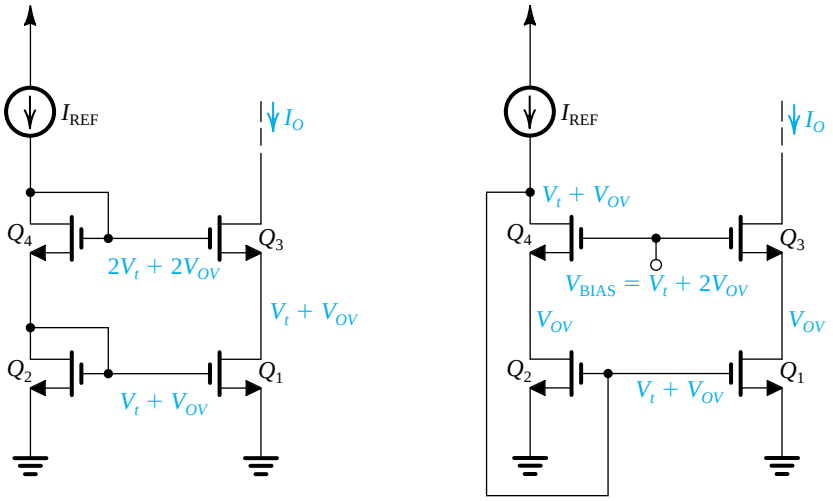


Figure 12.12 **(a)** Cascode current mirror with the voltages at all nodes indicated. Note that the minimum voltage allowed at the output is $V_t + 2V_{OV}$. **(b)** A modification of the cascode mirror that results in the reduction of the minimum output voltage to V_{OV}. This is the wide-swing current mirror. The circuit requires a bias voltage V_{BIAS}.

that because the voltage at the gate of Q_3 is $2V_t + 2V_{OV}$, the minimum voltage permitted at the output (while Q_3 remains saturated) is $V_t + 2V_{OV}$, hence the extra V_t. Also, observe that Q_1 is operating with a drain-to-source voltage $V_t + V_{OV}$, which is V_t volts greater than it needs to operate in saturation.

The observations above lead us to the conclusion that to permit the output voltage at the drain of Q_3 to swing as low as $2V_{OV}$, we must lower the voltage at the gate of Q_3 from $2V_t + 2V_{OV}$ to $V_t + 2V_{OV}$. This is exactly what is done in the modified mirror circuit in Fig. 12.12(b): The gate of Q_3 is now connected to a bias voltage $V_{BIAS} = V_t + 2V_{OV}$. Thus the output voltage can go down to $2V_{OV}$ with Q_3 still in saturation. Also, the voltage at the drain of Q_1 is now V_{OV} and thus Q_1 is operating at the edge of saturation. The same is true of Q_2 and thus the current tracking between Q_1 and Q_2 will be assured. Note, however, that we can no longer connect the gate of Q_2 to its drain. Rather, it is connected to the drain of Q_4. This establishes a voltage of $V_t + V_{OV}$ at the drain of Q_4 which is sufficient to operate Q_4 in saturation (as long as V_t is greater than V_{OV}, which is usually the case). This circuit is known as the **wide-swing current mirror**. Finally, note that Fig. 12.12(b) does not show the circuit for generating V_{BIAS}. There are a number of possible circuits to accomplish this task, one of which is explored in Exercise 12.9.

EXERCISE

12.9 Show that if transistor Q_5 in the circuit of Fig. E12.9 has a W/L ratio equal to one-quarter that of the transistors in the wide-swing current mirror of Fig. 12.12(b), and provided the same value of I_{REF} is utilized in both circuits, then the voltage generated, V_5 is $V_t + 2V_{OV}$, which is the value of V_{BIAS} needed for the gates of Q_3 and Q_4.

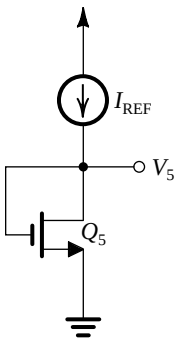


Figure E12.9

12.3 The 741 Op-Amp Circuit

Our study of BJT op amps is in two parts: The first part (Sections 12.3–12.6) is focused on the 741 op-amp circuit, which is shown in Fig. 12.13; the second part (Section 12.7) presents some of the more recent design techniques. Note that in keeping with the IC design philosophy, the circuit in Fig. 12.13 uses a large number of transistors, but relatively few resistors, and only one capacitor. This philosophy is dictated by the economics (silicon area, ease of fabrication, quality of realizable components) of the fabrication of active and passive components in IC form (see Section 7.1 and Appendix A).

As is the case with most general-purpose IC op amps, the 741 requires two power supplies, $+V_{CC}$ and $-V_{EE}$. Normally, $V_{CC} = V_{EE} = 15$ V, but the circuit also operates satisfactorily with the power supplies reduced to much lower values (such as ±5 V). It is important to observe that no circuit node is connected to ground, the common terminal of the two supplies.

With a relatively large circuit such as that shown in Fig. 12.13, the first step in the analysis is the identification of its recognizable parts and their functions. This can be done as follows.

12.3.1 Bias Circuit

The reference bias current of the 741 circuit, I_{REF}, is generated in the branch at the extreme left of Fig. 12.13, consisting of the two diode-connected transistors Q_{11} and Q_{12} and the resistance R_5. Using a Widlar current source formed by Q_{11}, Q_{10}, and R_4, bias current for the first stage is generated in the collector of Q_{10}. Another current mirror formed by Q_8 and Q_9 takes part in biasing the first stage.

The reference bias current I_{REF} is used to provide two proportional currents in the collectors of Q_{13}. This double-collector lateral[2] *pnp* transistor can be thought of as two transistors whose base–emitter junctions are connected in parallel. Thus Q_{12} and Q_{13} form a two-output current mirror: One output, the collector of Q_{13B}, provides bias current and acts as a current-source load for Q_{17}, and the other output, the collector of Q_{13A}, provides bias current for the output stage of the op amp.

[2]See Appendix A for a description of lateral *pnp* transistors. Also, their characteristics were discussed in the Appendix to Chapter 7, Section 7.A.2.

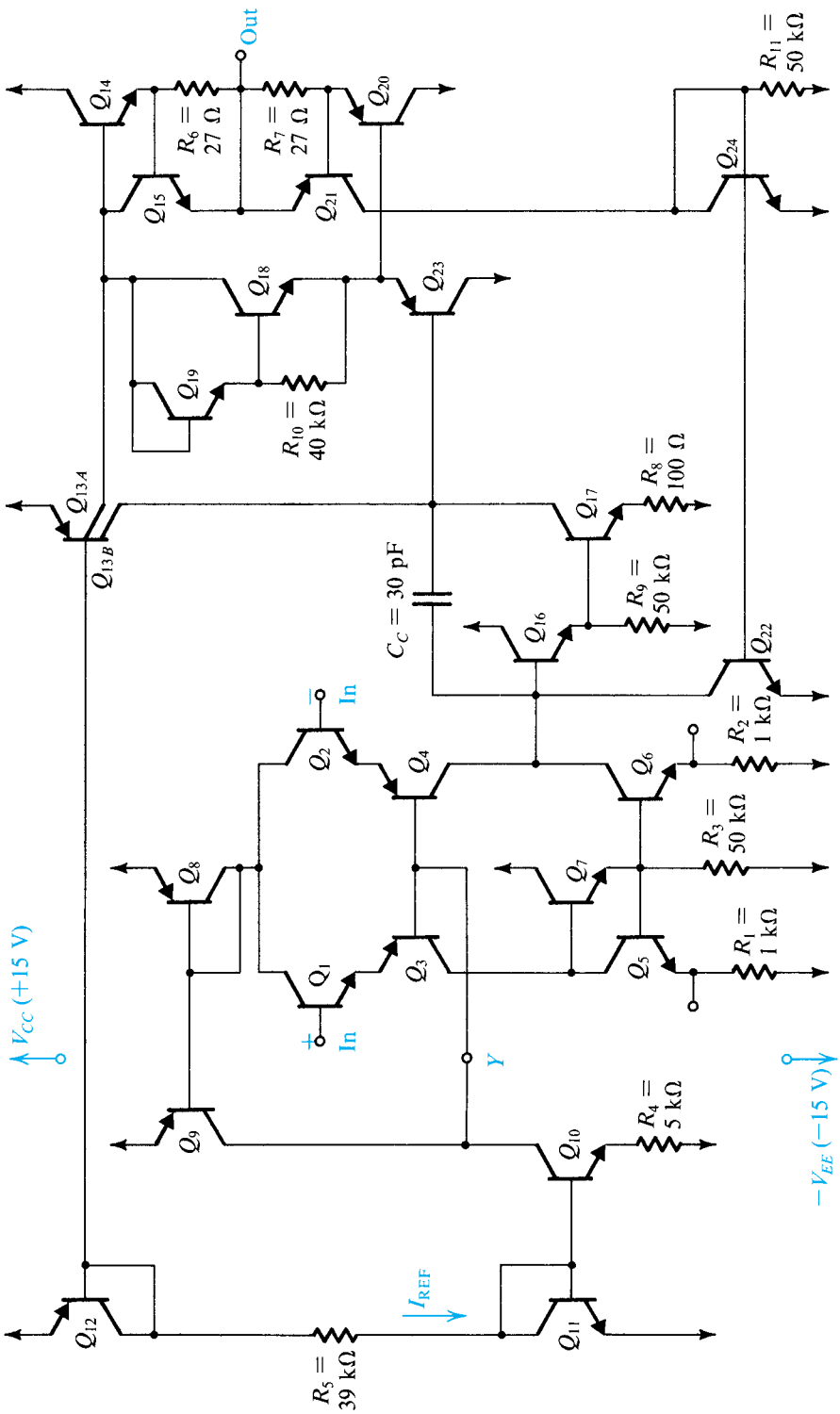


Figure 12.13 The 741 op-amp circuit: Q_{11}, Q_{12}, and R_5 generate a reference bias current; I_{REF}. Q_{10}, Q_9, and Q_8 bias the input stage, which is composed of Q_1 to Q_7. The second gain stage is composed of Q_{16} and Q_{17} with Q_{13B} acting as active load. The class AB output stage is formed by Q_{14} and Q_{20} with biasing devices Q_{13A}, Q_{18}, and Q_{19}, and an input buffer Q_{23}. Transistors Q_{15}, Q_{21}, Q_{24}, and Q_{22} serve to protect the amplifier against output short circuits and are normally cut off.

Two more transistors, Q_{18} and Q_{19}, take part in the dc bias process. The purpose of Q_{18} and Q_{19} is to establish two V_{BE} drops between the bases of the output transistors Q_{14} and Q_{20}.

12.3.2 Short-Circuit Protection Circuitry

The 741 circuit includes a number of transistors that are normally off and conduct only in the event of on attempt to draw a large current from the op-amp output terminal. This happens, for example, if the output terminal is short-circuited to one of the two supplies. The short-circuit protection network consists of R_6, R_7, Q_{15}, Q_{21}, Q_{24}, R_{11}, and Q_{22}. In the following we shall assume that these transistors are off. Operation of the short-circuit protection network will be explained in Section 12.5.3.

12.3.3 The Input Stage

The 741 circuit consists of three stages: an input differential stage, an intermediate single-ended high-gain stage, and an output-buffering stage. The input stage consists of transistors Q_1 through Q_7, with biasing performed by Q_8, Q_9, and Q_{10}. Transistors Q_1 and Q_2 act as emitter followers, causing the input resistance to be high and delivering the differential input signal to the differential common-base amplifier formed by Q_3 and Q_4. Thus the input stage is the differential version of the common-collector common-base configuration discussed in Section 7.6.3.

Transistors Q_5, Q_6, and Q_7 and resistors R_1, R_2, and R_3 form the load circuit of the input stage. This is an elaborate current-mirror load circuit, which we will analyze in detail in Section 12.5.1. The circuit is based on the base-current-compensated mirror studied in Section 7.5, but it includes two emitter-degeneration resistors R_1 and R_2, and a large resistor R_3 in the emitter of Q_7. It will be shown that this load circuit not only provides a high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection. The output of the input stage is taken single-endedly at the collector of Q_6.

As mentioned in Section 8.6.2, every op-amp circuit includes a *level shifter* whose function is to shift the dc level of the signal so that the signal at the op-amp output can swing positive and negative. In the 741, level shifting is done in the first stage using the lateral *pnp* transistors Q_3 and Q_4. Although lateral *pnp* transistors have poor high-frequency performance, their use in the common-base configuration (which is known to have good high-frequency response) does not seriously impair the op-amp frequency response.

The use of the lateral *pnp* transistors Q_3 and Q_4 in the first stage results in an added advantage: protection of the input-stage transistors Q_1 and Q_2 against emitter–base junction breakdown. Since the emitter–base junction of an *npn* transistor breaks down at about 7 V of reverse bias (see Section 6.9.1), regular *npn* differential stages suffer such a breakdown if, say, the supply voltage is accidentally connected between the input terminals. Lateral *pnp* transistors, however, have high emitter–base breakdown voltages (about 50 V); and because they are connected in series with Q_1 and Q_2, they provide protection of the 741 input transistors, Q_1 and Q_2.

Finally, note that except for using input buffer transistors, the 741 input stage is essentially a current-mirror-loaded differential amplifier. It is quite similar to the input stage of the CMOS amplifier in Fig. 12.1.

12.3.4 The Second Stage

The second or intermediate stage is composed of Q_{16}, Q_{17}, Q_{13B}, and the two resistors R_8 and R_9. Transistor Q_{16} acts as an emitter follower, thus giving the second stage a high input

resistance. This minimizes the loading on the input stage and avoids loss of gain. Also, adding Q_{16} with its 50-kΩ emitter resistance (which is similar to Q_7 and R_3) increases the symmetry of the first stage and thus improves its CMRR. Transistor Q_{17} acts as a common-emitter amplifier with a 100-Ω resistor in the emitter. Its load is composed of the high output resistance of the *pnp* current source Q_{13B} in parallel with the input resistance of the output stage (seen looking into the base of Q_{23}). Using a transistor current source as a load resistance (*active load*) enables one to obtain high gain without resorting to the use of large load resistances, which would occupy a large chip area and require large power-supply voltages.

The output of the second stage is taken at the collector of Q_{17}. Capacitor C_C is connected in the feedback path of the second stage to provide frequency compensation using the Miller compensation technique studied in Section 10.13. It will be shown in Section 12.5 that the relatively small capacitor C_C gives the 741 a dominant pole at about 4 Hz. Furthermore, pole splitting causes other poles to be shifted to much higher frequencies, giving the op amp a uniform –20-dB/decade gain rolloff with a unity-gain bandwidth of about 1 MHz. It should be pointed out that although C_C is small in value, the chip area that it occupies is about 13 times that of a standard *npn* transistor!

12.3.5 The Output Stage

The purpose of the output stage (Chapter 11) is to provide the amplifier with a low output resistance. In addition, the output stage should be able to supply relatively large load currents without dissipating an unduly large amount of power in the IC. The 741 uses an efficient class AB output stage, which we shall study in detail in Section 12.5.

The output stage of the 741 consists of the complementary pair Q_{14} and Q_{20}, where Q_{20} is a *substrate pnp* (see Appendix A). Transistors Q_{18} and Q_{19} are fed by current source Q_{13A} and bias the output transistors Q_{14} and Q_{20}. Transistor Q_{23} (which is another substrate *pnp*) acts as an emitter follower, thus minimizing the loading effect of the output stage on the second stage.

12.3.6 Device Parameters

In the following sections we shall carry out a detailed analysis of the 741 circuit. For the standard *npn* and *pnp* transistors, the following parameters will be used:

$$npn: \quad I_S = 10^{-14}\text{A}, \beta = 200, V_A = 125\ \text{V}$$

$$pnp: \quad I_S = 10^{-14}\text{A}, \beta = 50, V_A = 50\ \text{V}$$

In the 741 circuit the nonstandard devices are Q_{13}, Q_{14}, and Q_{20}. Transistor Q_{13} will be assumed to be equivalent to two transistors, Q_{13A} and Q_{13B}, with parallel base–emitter junctions and having the following saturation currents:

$$I_{SA} = 0.25 \times 10^{-14}\text{A} \qquad I_{SB} = 0.75 \times 10^{-14}\text{A}$$

Transistors Q_{14} and Q_{20} will be assumed to each have an area three times that of a standard device. Output transistors usually have relatively large areas, to be able to supply large load currents and dissipate relatively large amounts of power with only a moderate increase in device temperature.

EXERCISES

12.10 For the standard *npn* transistor whose parameters are given in Section 12.3.6, find approximate values for the following parameters at $I_C = 1$ mA: V_{BE}, g_m, r_e, r_π, and r_o.
Ans. 633 mV; 40 mA/V; 25 Ω; 5 kΩ; 125 kΩ

12.11 For the circuit in Fig. E12.11, neglect base currents and use the exponential i_C–v_{BE} relationship to show that

$$I_3 = I_1\sqrt{\frac{I_{S3}I_{S4}}{I_{S1}I_{S2}}}$$

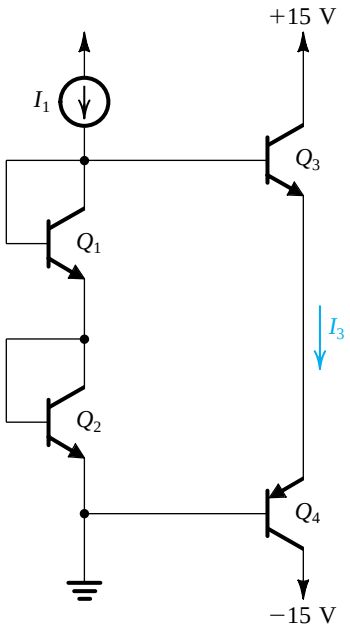


Figure E12.11

12.4 DC Analysis of the 741

In this section, we shall carry out a dc analysis of the 741 circuit to determine the bias point of each device. For the dc analysis of an op-amp circuit, the input terminals are grounded. Theoretically speaking, this should result in zero dc voltage at the output. However, because the op amp has very large gain, any slight approximation in the analysis will show that the output voltage is far from being zero and is close to either $+V_{CC}$ or $-V_{EE}$. In actual practice, an op amp left open-loop will have an output voltage saturated close to one of the two supplies. To overcome this problem in the dc analysis, it will be assumed that the op amp is connected in a negative feedback loop that stabilizes the output dc voltage to zero volts.

12.4.1 Reference Bias Current

The reference bias current I_{REF} is generated in the branch composed of the two diode-connected transistors Q_{11} and Q_{12} and resistor R_5. With reference to Fig. 12.13, we can write

$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

For $V_{CC} = V_{EE} = 15$ V and $V_{BE11} = V_{EB12} \simeq 0.7$ V, we have $I_{REF} = 0.73$ mA.

12.4.2 Input-Stage Bias

Transistor Q_{11} is biased by I_{REF}, and the voltage developed across it is used to bias Q_{10}, which has a series emitter resistance R_4. This part of the circuit is redrawn in Fig. 12.14 and can be recognized as the Widlar current source studied in Section 7.5.5. From the circuit, and assuming β_{10} to be large, we have

$$V_{BE11} - V_{BE10} = I_{C10}R_4$$

Thus

$$V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10}R_4 \tag{12.75}$$

where it has been assumed that $I_{S10} = I_{S11}$. Substituting the known values for I_{REF} and R_4, this equation can be solved by trial and error to determine I_{C10}. For our case, the result is $I_{C10} = 19$ μA.

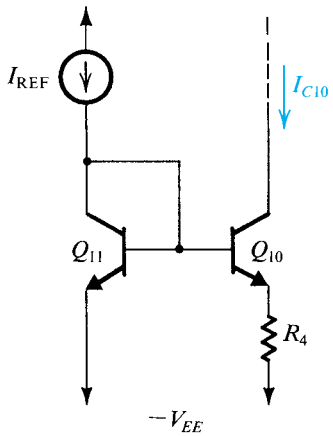


Figure 12.14 The Widlar current source that biases the input stage.

EXERCISE

D12.12 Design the Widlar current source of Fig. 12.14 to generate a current $I_{C10} = 10$ μA given that $I_{REF} = 1$ mA. If at a collector current of 1 mA, $V_{BE} = 0.7$ V, find V_{BE11} and V_{BE10}.
Ans. $R_4 = 11.5$ kΩ; $V_{BE11} = 0.7$ V; $V_{BE10} = 0.585$ V

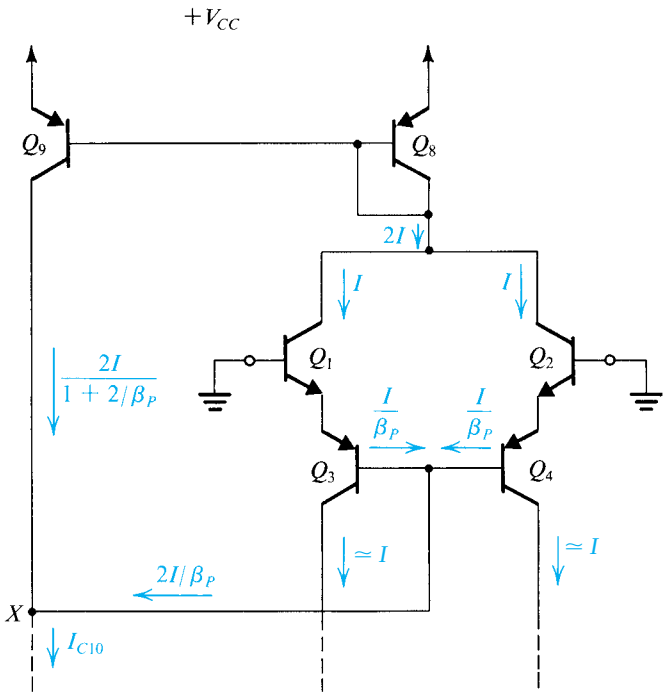


Figure 12.15 The dc analysis of the 741 input stage.

Having determined I_{C10}, we proceed to determine the dc current in each of the input-stage transistors. Part of the input stage is redrawn in Fig. 12.15. From symmetry, we see that

$$I_{C1} = I_{C2}$$

Denote this current by I. We see that if the *npn* β is high, then

$$I_{E3} = I_{E4} \simeq I$$

and the base currents of Q_3 and Q_4 are equal, with a value of $I/(\beta_P + 1) \simeq I/\beta_P$, where β_P denotes β of the *pnp* devices.

The current mirror formed by Q_8 and Q_9 is fed by an input current of $2I$. Using the result in Eq. (7.69), we can express the output current of the mirror as

$$I_{C9} = \frac{2I}{1 + 2/\beta_P}$$

We can now write a node equation for node X in Fig. 12.15 and thus determine the value of I. If $\beta_P \gg 1$, then this node equation gives

$$2I \simeq I_{C10}$$

For the 741, $I_{C10} = 19\ \mu A$; thus $I \simeq 9.5\ \mu A$. We have thus determined that

$$I_{C1} = I_{C2} \simeq I_{C3} = I_{C4} = 9.5\ \mu A$$

At this point, we should note that transistors Q_1 through Q_4, Q_8, and Q_9 form a **negative-feedback loop**, which works to stabilize the value of I at approximately $I_{C10}/2$. To appreciate this fact, assume that for some reason the current I in Q_1 and Q_2 increases. This will

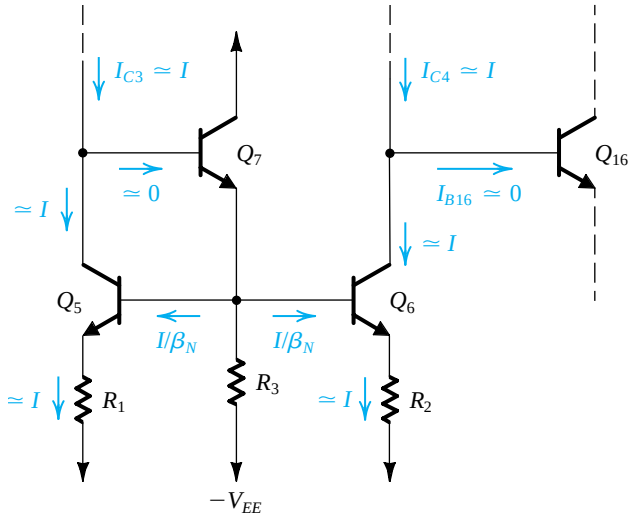


Figure 12.16 The dc analysis of the 741 input stage, continued.

cause the current pulled from Q_8 to increase, and the output current of the Q_8–Q_9 mirror will correspondingly increase. However, since I_{C10} remains constant, node X forces the combined base currents of Q_3 and Q_4 to decrease. This in turn will cause the emitter currents of Q_3 and Q_4, and hence the collector currents of Q_1 and Q_2, to decrease. This is opposite in direction to the change originally assumed. Hence the feedback is negative, and it stabilizes the value of I.

Figure 12.16 shows the remainder of the 741 input stage. This part of the circuit is fed by $I_{C3} = I_{C4} \simeq I$. Transistors Q_5 and Q_6 are identical and have equal resistances R_1 and R_2 in their emitters; thus,

$$I_{C5} = I_{C6} \tag{12.76}$$

Now if the base currents of Q_7 and Q_{16} can be neglected, then

$$I_{C5} \simeq I_{C3} \simeq I \tag{12.77}$$

and

$$I_{C6} \simeq I_{C4} \simeq I \tag{12.78}$$

Thus both the symmetry of Q_5 and Q_6 and the node equations at their collectors force their currents to be equal and to equal I. As will be shown shortly, not only are the base currents of Q_7 and Q_{16} negligible, but their values are also reasonably close, which is an added help.

The bias current of Q_7 can be determined from

$$I_{C7} \simeq I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3} \tag{12.79}$$

where β_N denotes β of the *npn* transistors. To determine V_{BE6} we use the transistor exponential relationship and write

$$V_{BE6} = V_T \ln \frac{I}{I_S}$$

Substituting $I_S = 10^{-14}$ A and $I = 9.5$ μA results in $V_{BE6} = 517$ mV. Then substituting in Eq. (12.79) yields $I_{C7} = 10.5$ μA. Note that the base current of Q_7 at approximately 0.05 μA is indeed negligible in comparison to the value of I, as has been assumed.

12.4.3 Input Bias and Offset Currents

The **input bias current** of an op amp is defined (Chapters 2 and 8) as

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

For the 741 we obtain

$$I_B = \frac{I}{\beta_N}$$

Using $\beta_N = 200$, yields $I_B = 47.5$ nA. Note that this value is reasonably small and is typical of general-purpose op amps that use BJTs in the input stage. Much lower input bias currents (in the picoamp or femtoamp range) can be obtained using a FET input stage. Also, there exist techniques for reducing the input bias current of bipolar-input op amps.

Because of possible mismatches in the β values of Q_1 and Q_2, the input base currents will not be equal. Given the value of the β mismatch, one can use Eq. (8.131) to calculate the **input offset current**, defined as

$$I_{OS} = |I_{B1} - I_{B2}|$$

12.4.4 Input Offset Voltage

From Chapter 8 we know that the input offset voltage is determined primarily by mismatches between the two sides of the input stage. In the 741 op amp, the input offset voltage is due to mismatches between Q_1 and Q_2, between Q_3 and Q_4, between Q_5 and Q_6, and between R_1 and R_2. Evaluation of the components of V_{OS} corresponding to the various mismatches follows the method outlined in Section 8.4. Basically, we find the current that results at the output of the first stage due to the particular mismatch being considered. Then we find the differential input voltage that must be applied to reduce the output current to zero.

12.4.5 Input Common-Mode Range

The **input common-mode range** is the range of input common-mode voltages over which the input stage remains in the linear active mode. Refer to Fig. 12.13. We see that in the 741 circuit the input common-mode range is determined at the upper end by saturation of Q_1 and Q_2, and at the lower end by saturation of Q_3 and Q_4.

EXERCISE

12.13 Neglect the voltage drops across R_1 and R_2 and assume that $V_{CC} = V_{EE} = 15$ V. Show that the input common-mode range of the 741 is approximately –12.9 V to +14.7 V. (Assume that $V_{BE} \simeq 0.6$ V and that to avoid saturation $V_{CB} \geq -0.3$ V for an *npn* transistor, and $V_{BC} \geq -0.3$ V for a *pnp* transistor.)

12.4.6 Second-Stage Bias

If we neglect the base current of Q_{23} then we see from Fig. 12.13 that the collector current of Q_{17} is approximately equal to the current supplied by current source Q_{13B}. Because Q_{13B} has a scale current 0.75 times that of Q_{12}, its collector current will be $I_{C13B} \simeq 0.75 I_{REF}$, where we have assumed that $\beta_P \gg 1$. Thus $I_{C13B} = 550\ \mu A$ and $I_{C17} \simeq 550\ \mu A$. At this current level the base–emitter voltage of Q_{17} is

$$V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618\ \text{mV}$$

The collector current of Q_{16} can be determined from

$$I_{C16} \simeq I_{E16} = I_{B17} + \frac{I_{E17} R_8 + V_{BE17}}{R_9}$$

This calculation yields $I_{C16} = 16.2\ \mu A$. Note that the base current of Q_{16} at 0.08 μA will indeed be negligible compared to the input-stage bias I, as we have assumed.

12.4.7 Output-Stage Bias

Figure 12.17 shows the output stage of the 741 with the short-circuit-protection circuitry omitted. Current source Q_{13A} delivers a current of $0.25 I_{REF}$ (because I_S of Q_{13A} is 0.25

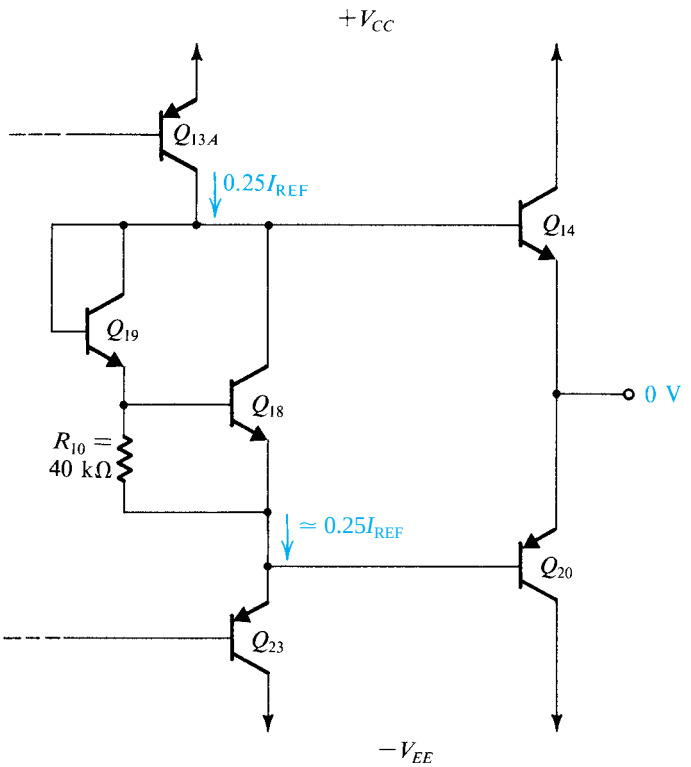


Figure 12.17 The 741 output stage without the short-circuit protection devices.

times the I_S of Q_{12}) to the network composed of Q_{18}, Q_{19}, and R_{10}. If we neglect the base currents of Q_{14} and Q_{20}, then the emitter current of Q_{23} will also be equal to $0.25I_{REF}$. Thus

$$I_{C23} \simeq I_{E23} \simeq 0.25I_{REF} = 180\ \mu A$$

Thus we see that the base current of Q_{23} is only $180/50 = 3.6\ \mu A$, which is negligible compared to I_{C17}, as we have assumed.

If we assume that V_{BE18} is approximately 0.6 V, we can determine the current in R_{10} as 15 μA. The emitter current of Q_{18} is therefore

$$I_{E18} = 180 - 15 = 165\ \mu A$$

Also,

$$I_{C18} \simeq I_{E18} = 165\ \mu A$$

At this value of current we find that $V_{BE18} = 588$ mV, which is quite close to the value assumed. The base current of Q_{18} is $165/200 = 0.8\ \mu A$, which can be added to the current in R_{10} to determine the Q_{19} current as

$$I_{C19} \simeq I_{E19} = 15.8\ \mu A$$

The voltage drop across the base–emitter junction of Q_{19} can now be determined as

$$V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530\ \text{mV}$$

As mentioned in Section 12.3.5, the purpose of the Q_{18}–Q_{19} network is to establish two V_{BE} drops between the bases of the output transistors Q_{14} and Q_{20}. This voltage drop, V_{BB}, can be now calculated as

$$V_{BB} = V_{BE18} + V_{BE19} = 588 + 530 = 1.118\ \text{V}$$

Since V_{BB} appears across the series combination of the base–emitter junctions of Q_{14} and Q_{20}, we can write

$$V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$

Using the calculated value of V_{BB} and substituting $I_{S14} = I_{S20} = 3 \times 10^{-14}$ A, we determine the collector currents as

$$I_{C14} = I_{C20} = 154\ \mu A$$

This is the small current at which the class AB output stage is biased.

12.4.8 Summary

For future reference, Table 12.1 provides a listing of the values of the collector bias currents of the 741 transistors.

Table 12.1 DC Collector Currents of the 741 Circuit (μA)

Q_1	9.5	Q_8	19	Q_{13B}	550	Q_{19}	15.8
Q_2	9.5	Q_9	19	Q_{14}	154	Q_{20}	154
Q_3	9.5	Q_{10}	19	Q_{15}	0	Q_{21}	0
Q_4	9.5	Q_{11}	730	Q_{16}	16.2	Q_{22}	0
Q_5	9.5	Q_{12}	730	Q_{17}	550	Q_{23}	180
Q_6	9.5	Q_{13A}	180	Q_{18}	165	Q_{24}	0
Q_7	10.5						

EXERCISE

12.14 If in the circuit of Fig. 12.17 the Q_{18}–Q_{19} network is replaced by two diode-connected transistors, find the current in Q_{14} and Q_{20}. (*Hint:* Use the result of Exercise 12.11.)
Ans. 540 μA

12.5 Small-Signal Analysis of the 741

12.5.1 The Input Stage

Figure 12.18 shows part of the 741 input stage for the purpose of performing small-signal analysis. Note that since the collectors of Q_1 and Q_2 are connected to a constant dc voltage, they are shown grounded. Also, the constant-current biasing of the bases of Q_3 and Q_4 is equivalent to having the common base terminal open-circuited.

The differential signal v_i applied between the input terminals effectively appears across four equal emitter resistances connected in series—those of Q_1, Q_2, Q_3, and Q_4. As a result, emitter signal currents flow as indicated in Fig. 12.18 with

$$i_e = \frac{v_i}{4r_e} \tag{12.80}$$

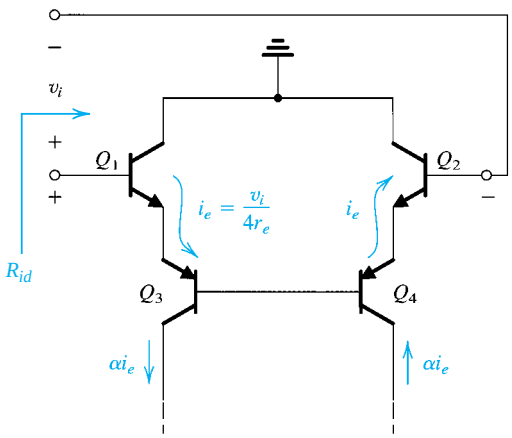


Figure 12.18 Small-signal analysis of the 741 input stage.

where r_e denotes the emitter resistance of each of Q_1 through Q_4. Thus

$$r_e = \frac{V_T}{I} = \frac{25\text{ mV}}{9.5\ \mu\text{A}} = 2.63\ \text{k}\Omega$$

Thus the four transistors Q_1 through Q_4 supply the load circuit with a pair of complementary current signals αi_e, as indicated in Fig. 12.18.

The input differential resistance of the op amp can be obtained from Fig. 12.18 as

$$R_{id} = 4(\beta_N + 1)r_e \tag{12.81}$$

For $\beta_N = 200$, we obtain $R_{id} = 2.1$ MΩ.

Proceeding with the input-stage analysis, we show in Fig. 12.19 the load circuit fed with the complementary pair of current signals found earlier. Neglecting the signal current in the base of Q_7, we see that the collector signal current of Q_5 is approximately equal to the input current αi_e. Now, since Q_5 and Q_6 are identical and their bases are tied together, and since equal resistances are connected in their emitters, it follows that their collector signal currents must be equal. Thus the signal current in the collector of Q_6 is forced to be equal to αi_e. In other words, the load circuit functions as a current mirror.

Now consider the output node of the input stage. The output current i_o is given by

$$i_o = 2\alpha i_e \tag{12.82}$$

The factor of 2 in this equation indicates that conversion from differential to single-ended is performed without losing half the signal. The trick, of course, is the use of the current mirror to invert one of the current signals and then add the result to the other current signal (see Section 8.5).

Equations (12.80) and (12.82) can be combined to obtain the transconductance of the input stage, G_{m1}:

$$G_{m1} \equiv \frac{i_o}{v_i} = \frac{\alpha}{2r_e} \tag{12.83}$$

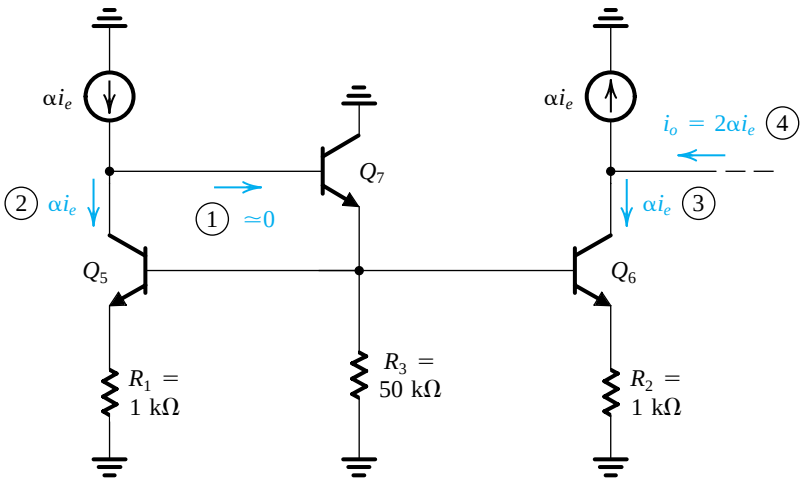


Figure 12.19 The load circuit of the input stage fed by the two complementary current signals generated by Q_1 through Q_4 in Fig. 12.18. Circled numbers indicate the order of the analysis steps.

Substituting $r_e = 2.63\ \text{k}\Omega$ and $\alpha \simeq 1$ yields $G_{m1} = 1/5.26\ \text{mA/V}$. The expression for G_{m1} can be written in the alternate form

$$G_{m1} = \frac{1}{2} g_{m1} \tag{12.83′}$$

where g_{m1} is the transconductance of each of Q_1 to Q_4.

EXERCISE

12.15 For the circuit in Fig. 12.19, find in terms of i_e: (a) the signal voltage at the base of Q_6; (b) the signal current in the emitter of Q_7; (c) the signal current in the base of Q_7; (d) the signal voltage at the base of Q_7; (e) the input resistance seen by the left-hand-side signal current source αi_e. (*Note:* For simplicity, assume that $I_{C7} \simeq I_{C5} = I_{C6}$.)

Ans. (a) $3.63\ \text{k}\Omega \times i_e$; (b) $0.08 i_e$; (c) $0.0004 i_e$; (d) $3.84\ \text{k}\Omega \times i_e$; (e) $3.84\ \text{k}\Omega$

To complete our modeling of the 741 input stage, we must find its output resistance R_{o1}. This is the resistance seen "looking back" into the collector terminal of Q_6 in Fig. 12.19. Thus R_{o1} is the parallel equivalent of the output resistance of the current source supplying the signal current αi_e, and the output resistance of Q_6. The first component is the resistance looking into the collector of Q_4 in Fig. 12.18. Finding this resistance is considerably simplified if we assume that the common bases of Q_3 and Q_4 are at a *virtual ground*. This of course happens only when the input signal v_i is applied in a complementary fashion. Nevertheless, this assumption does not result in a large error.

Assuming that the base of Q_4 is at virtual ground, the resistance we are after is R_{o4}, indicated in Fig. 12.20(a). This is the output resistance of a common-base transistor that has a resistance (r_e of Q_2) in its emitter. To find R_{o4} we may use the following expression (Eq. 7.51):

$$R_o = r_o[1 + g_m(R_e \| r_\pi)] \tag{12.84}$$

Substituting $R_e = r_e \equiv 2.63\ \text{k}\Omega$ and $r_o = V_A/I$, where $V_A = 50\ \text{V}$ and $I = 9.5\ \mu\text{A}$ (thus $r_o = 5.26\ \text{M}\Omega$), and neglecting r_π since it is $(\beta + 1)$ times larger than R_E, results in $R_{o4} = 10.5\ \text{M}\Omega$.

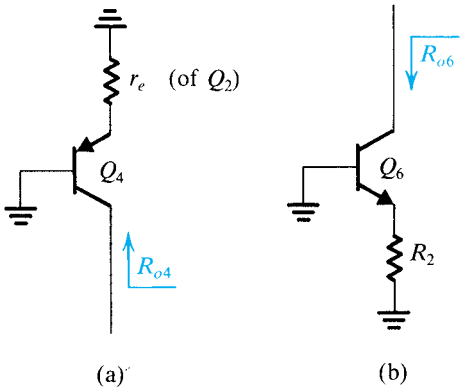


Figure 12.20 Simplified circuits for finding the two components of the output resistance R_{o1} of the first stage.

The second component of the output resistance is that seen looking into the collector of Q_6 in Fig. 12.19 with the αi_e generator set to 0. Although the base of Q_6 is not at signal ground, we shall assume that the signal voltage at the base is small enough to make this approximation valid. The circuit then takes the form shown in Fig. 12.20(b), and R_{o6} can be determined using Eq. (12.84) with $R_e = R_2$. Thus $R_{o6} \simeq 18.2\ \text{M}\Omega$.

Finally, we combine R_{o4} and R_{o6} in parallel to obtain the output resistance of the input stage, R_{o1}, as $R_{o1} = 6.7\ \text{M}\Omega$.

Figure 12.21 shows the equivalent circuit that we have derived for the input stage.

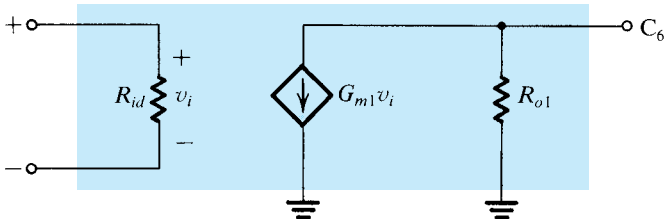


Figure 12.21 Small-signal equivalent circuit for the input stage of the 741 op amp.

Example 12.3

We wish to find the input offset voltage resulting from a 2% mismatch between the resistances R_1 and R_2 in Fig. 12.13.

Solution

Consider first the situation when both input terminals are grounded, and assume that $R_1 = R$ and $R_2 = R + \Delta R$, where $\Delta R/R = 0.02$. From Fig. 12.22 we see that while Q_5 still conducts a current equal to I, the current in Q_6 will be smaller by ΔI. The value of ΔI can be found from

$$V_{BE5} + IR = V_{BE6} + (I - \Delta I)(R + \Delta R)$$

Thus

$$V_{BE5} - V_{BE6} = I\Delta R - \Delta I(R + \Delta R) \tag{12.85}$$

The quantity on the left-hand side is in effect the change in V_{BE} due to a change in I_E of ΔI. We may therefore write

$$V_{BE5} - V_{BE6} \simeq \Delta I r_e \tag{12.86}$$

Equations (12.85) and (12.86) can be combined to obtain

$$\frac{\Delta I}{I} = \frac{\Delta R}{R + \Delta R + r_e} \tag{12.87}$$

Substituting $R = 1\ \text{k}\Omega$ and $r_e = 2.63\ \text{k}\Omega$ shows that a 2% mismatch between R_1 and R_2 gives rise to an output current $\Delta I = 5.5 \times 10^{-3} I$. To reduce this output current to zero we have to apply an input voltage V_{OS} given by

$$V_{OS} = \frac{\Delta I}{G_{m1}} = \frac{5.5 \times 10^{-3} I}{G_{m1}} \tag{12.88}$$

Substituting $I = 9.5\ \mu A$ and $G_{m1} = 1/5.26$ mA/V results in the offset voltage $V_{OS} \simeq 0.3$ mV.

It should be pointed out that the offset voltage calculated is only one component of the input offset voltage of the 741. Other components arise because of mismatches in transistor characteristics. The 741 offset voltage is specified to be typically 2 mV.

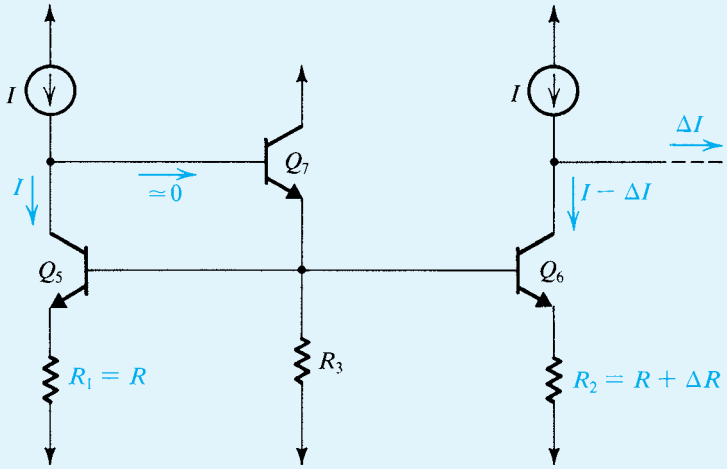


Figure 12.22 Input stage with both inputs grounded and a mismatch ΔR between R_1 and R_2.

Example 12.4

It is required to find the CMRR of the 741 input stage. Assume that the circuit is balanced except for mismatches in the current-mirror load that result in an error ε_m in the mirror's current-transfer ratio; that is, the ratio becomes $(1 - \varepsilon_m)$.

Solution

In Section 8.5.4 we analyzed the common-mode operation of the current-mirror-loaded differential amplifier and derived an expression for its CMRR. The situation in the 741 input stage, however, differs substantially because of the feedback loop that regulates the bias current. Since this feedback loop is sensitive to the common-mode signal, as will be seen shortly, the loop operates to reduce the common-mode gain and, correspondingly, to increase the CMRR. Hence, its action is referred to as **common-mode feedback**.

Figure 12.23 shows the 741 input stage with a common-mode signal v_{icm} applied to both input terminals. We have assumed that as a result of v_{icm}, a signal current i flows as shown. Since the stage is balanced, both sides carry the same current i.

Example 12.4 *continued*

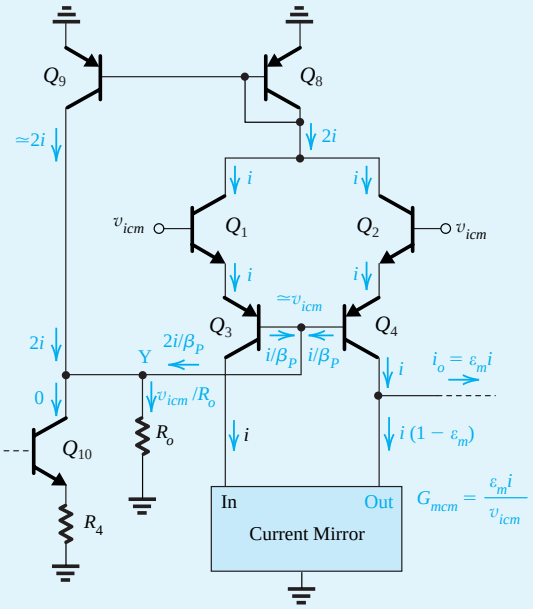


Figure 12.23 Example 12.4: Analysis of the common-mode gain of the 741 input stage. Note that $R_o = R_{o9} \,\|\, R_{o10}$, has been "pulled out" and shown seperately, leaving behind ideal current sources Q_9 and Q_{10}.

Our objective now is to determine how i relates to v_{icm}. Toward that end, observe that for common-mode inputs, both sides of the differential amplifier, that is, $Q_1 - Q_3$ and $Q_2 - Q_4$, act as followers, delivering a signal almost equal to v_{icm} to the common-base node of Q_3 and Q_4. Now, this node Y is connected to the collectors of two current sources, Q_9 and Q_{10}. Denoting the total resistance between node Y and ground R_o, we write

$$R_o = R_{o9} \,\|\, R_{o10} \tag{12.89}$$

In Fig. 12.23 we have "pulled R_o out," thus leaving behind ideal current sources Q_9 and Q_{10}. Since the current in Q_{10} is constant, we show Q_{10} in Fig. 12.23 as having a zero incremental current. Transistor Q_9, on the other hand, provides a current approximately equal to that fed into Q_8, which is $2i$. This is the feedback current. Since Q_8 senses the *sum* of the currents in the two sides of the differential amplifier, the feedback loop operates only on the common-mode signal and is insensitive to any difference signal.

Proceeding with the analysis, we now can write a node equation at Y,

$$2i + \frac{2i}{\beta_P} = \frac{v_{icm}}{R_o} \tag{12.90}$$

Assuming $\beta_P \gg 1$, this equation simplifies to

$$i \simeq \frac{v_{icm}}{2R_o} \tag{12.91}$$

Having determined i, we now proceed to complete our analysis by finding the output current i_o. From the circuit in Fig. 12.23, we see that

$$i_o = \varepsilon_m i \tag{12.92}$$

Thus the common-mode transconductance of the input stage is given by

$$G_{mcm} \equiv \frac{i_o}{v_{icm}} = \frac{\varepsilon_m i}{v_{icm}}$$

Substituting for i from Eq. (12.91) gives

$$G_{mcm} = \frac{\varepsilon_m}{2R_o} \tag{12.93}$$

Finally, the CMRR can be found as the ratio of the differential transconductance G_{m1} found in Eq. (12.83′) and the common-mode transconductance G_{mcm},

$$\text{CMRR} \equiv \frac{G_{m1}}{G_{mcm}} = 2g_{m1}R_o/\varepsilon_m \tag{12.94}$$

where g_{m1} is the transconductance of Q_1. Now substituting for R_o from Eq. (12.89), we obtain

$$\text{CMRR} = 2g_{m1}(R_{o9} \parallel R_{o10})/\varepsilon_m \tag{12.95}$$

Before leaving this example, we observe that if the feedback were not present, the $2i$ term in Eq. (12.90) would be absent and the current i would become $\beta_P(v_{icm}/2R_o)$, which is β_P times higher than that when feedback is present. In other words, common-mode feedback reduces i, hence the common-mode transconductance and the common-mode gain, by a factor β_P.

EXERCISES

12.16 Show that if the source of the imbalance in the current-mirror load is that while $R_1 = R$, $R_2 = R + \Delta R$, the error ε_m is given by

$$\varepsilon_m = \frac{\Delta R}{R + r_{e5} + \Delta R}$$

Evaluate ε_m for $\Delta R/R = 0.02$.
Ans. $\varepsilon_m = 5.5 \times 10^{-3}$

12.17 Refer to Fig. 12.23 and assume that the bases of Q_9 and Q_{10} are at approximately constant voltages (signal ground). Find R_{o9}, R_{o10}, and hence R_o. Use $V_A = 125$ V for *npn* and 50 V for *pnp* transistors. Use the bias current values in Table 12.1.
Ans. $R_{o9} = 2.63\ \text{M}\Omega$; $R_{o10} = 31.1\ \text{M}\Omega$; $R_o = 2.43\ \text{M}\Omega$

12.18 Use the results of Exercises 12.16 and 12.17 to determine G_{mcm} and CMRR of the 741 input stage. What would the CMRR be if the common-mode feedback were not present? Assume $\beta_P = 50$.
Ans. $G_{mcm} = 1.13 \times 10^{-6}$ mA/V; CMRR $= 1.68 \times 10^5$ or 104.5 dB; without common-mode feedback, CMRR = 70.5 dB

12.5.2 The Second Stage

Figure 12.24 shows the 741 second stage prepared for small-signal analysis. In this section we shall analyze the second stage to determine the values of the parameters of the equivalent circuit shown in Fig. 12.25.

Input Resistance The input resistance R_{i2} can be found by inspection to be

$$R_{i2} = (\beta_{16} + 1)\{r_{e16} + [R_9 \parallel (\beta_{17} + 1)(r_{e17} + R_8)]\} \tag{12.96}$$

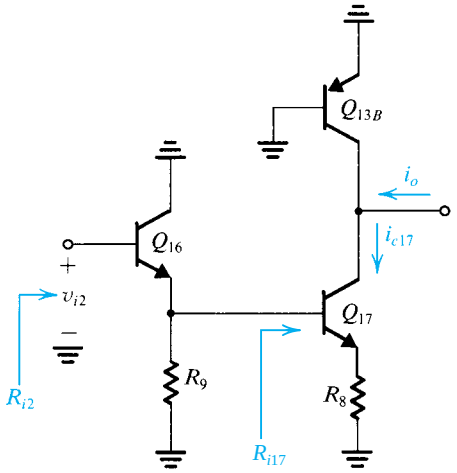


Figure 12.24 The 741 second stage prepared for small-signal analysis.

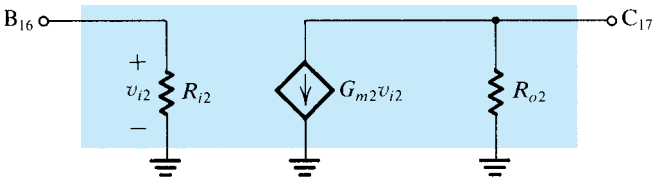


Figure 12.25 Small-signal equivalent-circuit model of the second stage.

Substituting the appropriate parameter values yields $R_{i2} \simeq 4\ \text{M}\Omega$.

Transconductance From the equivalent circuit of Fig. 12.25, we see that the transconductance G_{m2} is the ratio of the *short-circuit output current* to the input voltage. Short-circuiting the output terminal of the second stage (Fig. 12.24) to ground makes the signal current through the output resistance of Q_{13B} zero, and the output short-circuit current becomes equal to the collector signal current of Q_{17} (i_{c17}). This latter current can be easily related to v_{i2} as follows:

$$i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8} \tag{12.97}$$

$$v_{b17} = v_{i2}\frac{(R_9 \| R_{i17})}{(R_9 \| R_{i17}) + r_{e16}} \tag{12.98}$$

$$R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \tag{12.99}$$

where we have neglected r_{o16} because $r_{o16} \gg R_9$. These equations can be combined to obtain

$$G_{m2} \equiv \frac{i_{c17}}{v_{i2}} \tag{12.100}$$

which, for the 741 parameter values, is found to be $G_{m2} = 6.5$ mA/V.

Output Resistance To determine the output resistance R_{o2} of the second stage in Fig. 12.24, we ground the input terminal and find the resistance looking back into the output terminal.

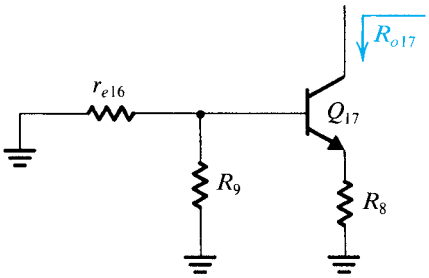


Figure 12.26 Definition of R_{o17}.

It follows that R_{o2} is given by

$$R_{o2} = (R_{o13B} \| R_{o17}) \tag{12.101}$$

where R_{o13B} is the resistance looking into the collector of Q_{13B} while its base and emitter are connected to ground. It can be easily seen that

$$R_{o13B} = r_{o13B} \tag{12.102}$$

For the 741 component values we obtain $R_{o13B} = 90.9$ kΩ.

The second component in Eq. (12.101), R_{o17}, is the resistance seen looking into the collector of Q_{17}, as indicated in Fig. 12.26. Since the resistance between the base of Q_{17} and ground is relatively small, one can considerably simplify matters by assuming that the base is grounded. Doing this, we can use Eq. (12.84) to determine R_{o17}. For our case, the result is $R_{o17} \simeq 787$ kΩ. Combining R_{o13B} and R_{o17} in parallel yields $R_{o2} = 81$ kΩ.

Thévenin Equivalent Circuit The second-stage equivalent circuit can be converted to the Thévenin form, as shown in Fig. 12.27. Note that the stage open-circuit voltage gain is $-G_{m2}R_{o2}$.

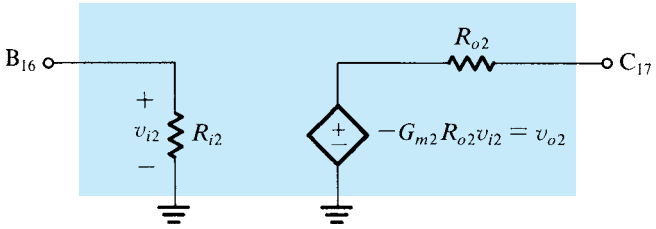


Figure 12.27 Thévenin form of the small-signal model of the second stage.

EXERCISES

12.19 Use Eq. (12.96) to show that $R_{i2} \simeq 4$ MΩ.

12.20 Use Eqs. (12.97) to (12.100) to verify that G_{m2} is 6.5 mA/V.

12.21 Verify that $R_{o2} \simeq 81$ kΩ.

12.22 Find the open-circuit voltage gain of the second stage of the 741.
Ans. −526.5 V/V

12.5.3 The Output Stage

The 741 output stage is shown in Fig. 12.28 without the short-circuit-protection circuitry. The stage is shown driven by the second-stage transistor Q_{17} and loaded with a 2-kΩ resistance. The circuit is of the AB class (Section 11.4), with the network composed of Q_{18}, Q_{19}, and R_{10} providing the bias of the output transistors Q_{14} and Q_{20}. The use of this network rather than two diode-connected transistors in series enables biasing the output transistors at a low current (0.15 mA) in spite of the fact that the output devices are three times as large as the standard devices. This result is obtained by arranging that the current in Q_{19} is very small and thus its V_{BE} is also small. We analyzed the dc bias in Section 12.4.7.

Another feature of the 741 output stage worth noting is that the stage is driven by an emitter follower Q_{23}. As will be shown, this emitter follower provides added buffering, which makes the op-amp gain almost independent of the parameters of the output transistors.

Output Voltage Limits The maximum positive output voltage is limited by the saturation of current-source transistor Q_{13A}. Thus,

$$v_{O\max} = V_{CC} - |V_{CE\,\text{sat}}| - V_{BE14} \tag{12.103}$$

which is about 1 V below V_{CC}. The minimum output voltage (i.e., maximum negative amplitude) is limited by the saturation of Q_{17}. Neglecting the voltage drop across R_8, we obtain

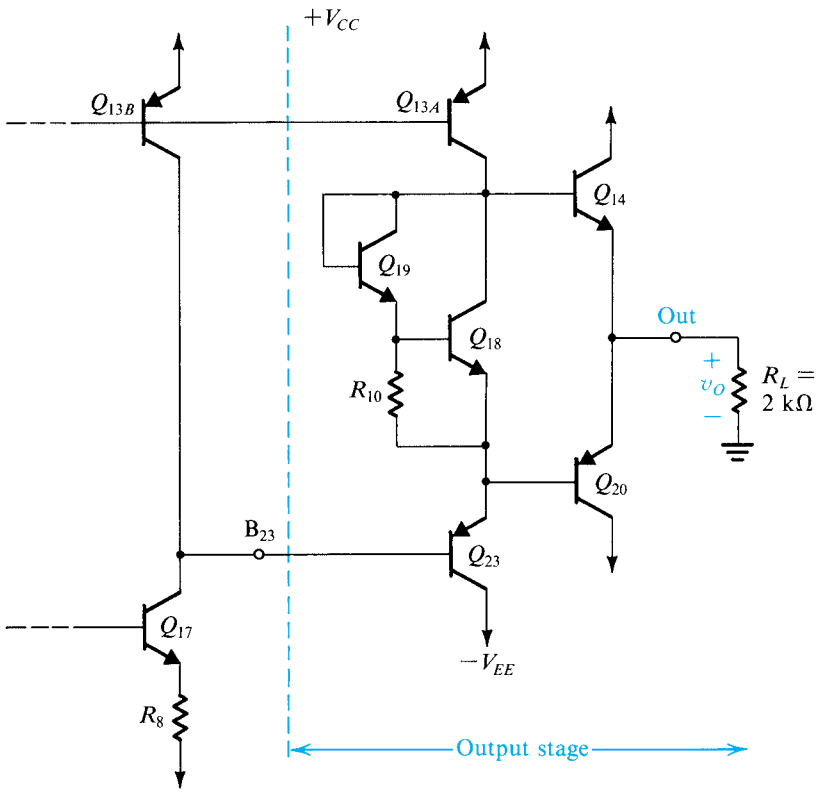


Figure 12.28 The 741 output stage without the short-circuit-protection circuitry.

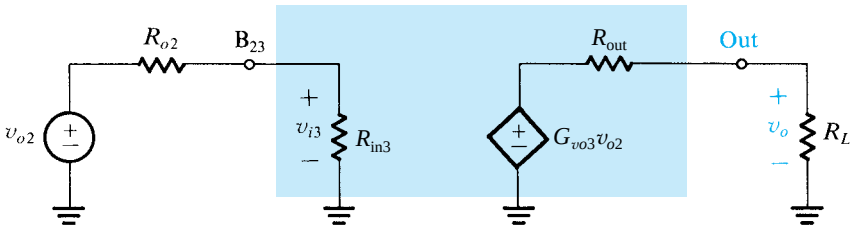


Figure 12.29 Model for the 741 output stage.

$$v_{O\min} = -V_{EE} + V_{CE\text{sat}} + V_{EB23} + V_{EB20} \tag{12.104}$$

which is about 1.5 V above $-V_{EE}$.

Small-Signal Model We shall now carry out a small-signal analysis of the output stage for the purpose of determining the values of the parameters of the equivalent-circuit model shown in Fig. 12.29. The model is shown fed by v_{o2}, which is the open-circuit output voltage of the second stage. From Fig. 12.27, v_{o2} is given by

$$v_{o2} = -G_{m2}R_{o2}v_{i2} \tag{12.105}$$

where G_{m2} and R_{o2} were previously determined as $G_{m2} = 6.5$ mA/V and $R_{o2} = 81$ kΩ. Resistance R_{in3} is the input resistance of the output stage determined with the amplifier loaded with R_L. Although the effect of loading an amplifier stage on its input resistance is negligible in the input and second stages, this is not the case in general in an output stage. Defining R_{in3} in this manner enables correct evaluation of the voltage gain of the second stage, A_2, as

$$A_2 \equiv \frac{v_{i3}}{v_{i2}} = -G_{m2}R_{o2}\frac{R_{\text{in3}}}{R_{\text{in3}} + R_{o2}} \tag{12.106}$$

To determine R_{in3}, assume that one of the two output transistors—say, Q_{20}—is conducting a current of, say, 5 mA while Q_{14} is cutoff. It follows that the input resistance looking into the base of Q_{20} is approximately $\beta_{20}R_L$. Assuming $\beta_{20} = 50$, for $R_L = 2$ kΩ, the input resistance of Q_{20} is 100 kΩ. This resistance appears in parallel with the series combination of the output resistance of Q_{13A} ($r_{o13A} \simeq 280$ kΩ) and the resistance of the Q_{18}–Q_{19} network. The latter resistance is very small (about 160 Ω; see later: Exercise 12.23). Thus the total resistance in the emitter of Q_{23} is approximately (100 kΩ ‖ 280 kΩ) or 74 kΩ and the input resistance R_{in3} is given by

$$R_{\text{in3}} \simeq \beta_{23} \times 74 \text{ kΩ}$$

which for $\beta_{23} = 50$ is $R_{\text{in3}} \simeq 3.7$ MΩ. Since $R_{o2} = 81$ kΩ, we see that $R_{\text{in3}} \gg R_{o2}$, and the value of R_{in3} will have little effect on the performance of the op amp. Still we can use the value obtained for R_{in3} to determine the gain of the second stage using Eq. (12.106) as $A_2 = -515$ V/V. The value of A_2 will be needed in Section 12.6 in connection with the frequency-response analysis.

Continuing with the determination of the equivalent circuit-model-parameters, we note from Fig. 12.29 that G_{vo3} is the **open-circuit overall voltage gain** of the output stage,

$$G_{vo3} = \left.\frac{v_o}{v_{o2}}\right|_{R_L=\infty} \tag{12.107}$$

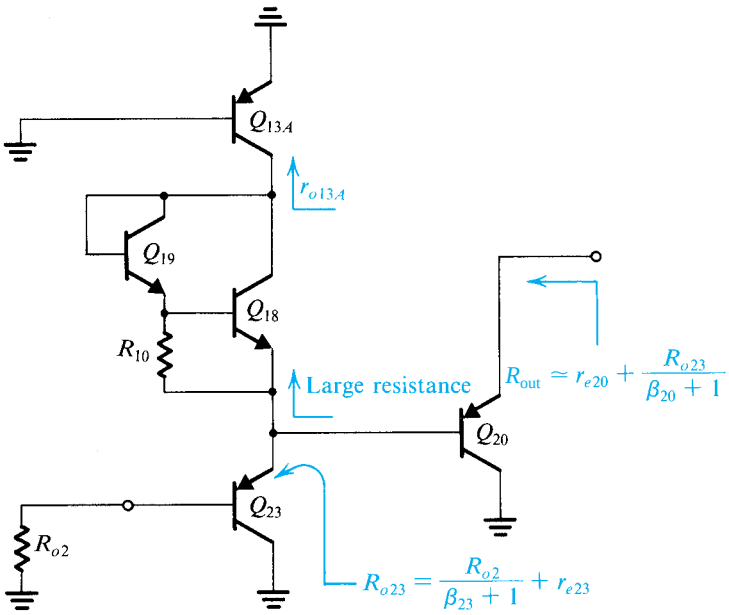


Figure 12.30 Circuit for finding the output resistance R_{out}.

With $R_L = \infty$, the gain of the emitter-follower output transistor (Q_{14} or Q_{20}) will be nearly unity. Also, with $R_L = \infty$ the resistance in the emitter of Q_{23} will be very large. This means that the gain of Q_{23} will be nearly unity and the input resistance of Q_{23} will be very large. We thus conclude that $G_{vo3} \simeq 1$.

Next, we shall find the value of the output resistance of the op amp, R_{out}. For this purpose refer to the circuit shown in Fig. 12.30. In accordance with the definition of R_{out} from Fig. 12.29, the input source feeding the output stage is grounded, but its resistance (which is the output resistance of the second stage, R_{o2}) is included. We have assumed that the output voltage v_O is negative, and thus Q_{20} is conducting most of the current; transistor Q_{14} has therefore been eliminated. The exact value of the output resistance will of course depend on which transistor (Q_{14} or Q_{20}) is conducting and on the value of load current. Nevertheless, we wish to find an estimate of R_{out}.

As indicated in Fig. 12.30, the resistance seen looking into the emitter of Q_{23} is

$$R_{o23} = \frac{R_{o2}}{\beta_{23}+1} + r_{e23} \tag{12.108}$$

Substituting $R_{o2} = 81$ kΩ, $\beta_{23} = 50$, and $r_{e23} = 25/0.18 = 139$ Ω yields $R_{o23} = 1.73$ kΩ. This resistance appears in parallel with the series combination of r_{o13A} and the resistance of the Q_{18}–Q_{19} network. Since r_{o13A} alone (0.28 MΩ) is much larger than R_{o23}, the effective resistance between the base of Q_{20} and ground is approximately equal to R_{o23}. Now we can find the output resistance R_{out} as

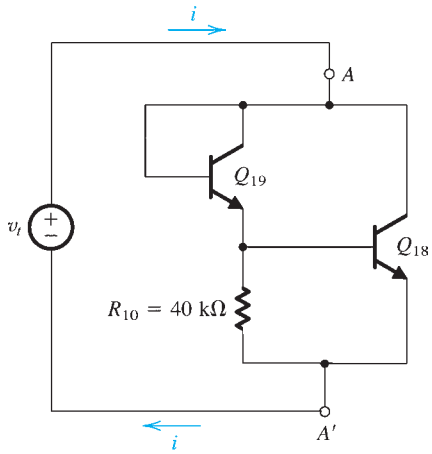
$$R_{\text{out}} = \frac{R_{o23}}{\beta_{20}+1} + r_{e20} \tag{12.109}$$

For $\beta_{20} = 50$, the first component of R_{out} is 34 Ω. The second component depends critically on the value of output current. For an output current of 5 mA, r_{e20} is 5 Ω and R_{out} is 39 Ω. To this value we must add the resistance R_7 (27 Ω) (see Fig. 12.13), which is included for short-circuit protection. The output resistance of the 741 is specified to be typically 75 Ω.

EXERCISES

12.23 Using a simple (r_π, g_m) model for each of the two transistors Q_{18} and Q_{19} in Fig. E12.23, find the small-signal resistance between A and A'. (*Note:* From Table 12.1, $I_{C18} = 165\ \mu A$ and $I_{C19} \simeq 16\ \mu A$.

Ans. 163 Ω



$$r_{AA'} \equiv \frac{v_t}{i}$$

Figure E12.23

12.24 Figure E12.24 shows the circuit for determining the op-amp output resistance when v_O is positive and Q_{14} is conducting most of the current. Using the resistance of the Q_{18}–Q_{19} network calculated in Exercise 12.23 and neglecting the large output resistance of Q_{13A}, find R_{out} when Q_{14} is sourcing an output current of 5 mA.

Ans. 14.4 Ω

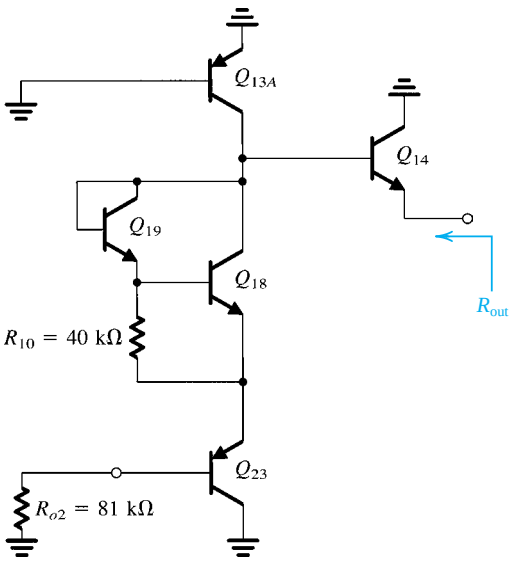


Figure E12.24

Output Short-Circuit Protection If the op-amp output terminal is short-circuited to one of the power supplies, one of the two output transistors could conduct a large amount of current. Such a large current can result in sufficient heating to cause burnout of the IC (Chapter 11). To guard against this possibility, the 741 op amp is equipped with a special circuit for short-circuit protection. The function of this circuit is to limit the current in the output transistors in the event of a short circuit.

Refer to Fig. 12.13. Resistance R_6 together with transistor Q_{15} limits the current that would flow out of Q_{14} in the event of a short circuit. Specifically, if the current in the emitter of Q_{14} exceeds about 20 mA, the voltage drop across R_6 exceeds 540 mV, which turns Q_{15} on. As Q_{15} turns on, its collector robs some of the current supplied by Q_{13A}, thus reducing the base current of Q_{14}. This mechanism thus limits the maximum current that the op amp can source (i.e., supply from the output terminal in the outward direction) to about 20 mA.

Limiting of the maximum current that the op amp can sink, and hence the current through Q_{20}, is done by a mechanism similar to the one discussed above. The relevant circuit is composed of R_7, Q_{21}, Q_{24}, and Q_{22}. For the components shown, the current in the inward direction is limited also to about 20 mA.

12.6 Gain, Frequency Response, and Slew Rate of the 741

In this section we shall evaluate the overall small-signal voltage gain of the 741 op amp. We shall then consider the op amp's frequency response and its slew-rate limitation.

12.6.1 Small-Signal Gain

The overall small-signal gain can be found from the cascade of the equivalent circuits derived in the preceding sections for the three op-amp stages. This cascade is shown in Fig. 12.31, loaded with $R_L = 2\ \text{k}\Omega$, which is the typical value used in measuring and specifying the 741 data. The overall gain can be expressed as

$$\frac{v_o}{v_i} = \frac{v_{i2}}{v_i}\frac{v_{o2}}{v_{i2}}\frac{v_o}{v_{o2}} \tag{12.110}$$

$$= -G_{m1}(R_{o1} \| R_{i2})(-G_{m2}R_{o2})G_{vo3}\frac{R_L}{R_L + R_{\text{out}}} \tag{12.111}$$

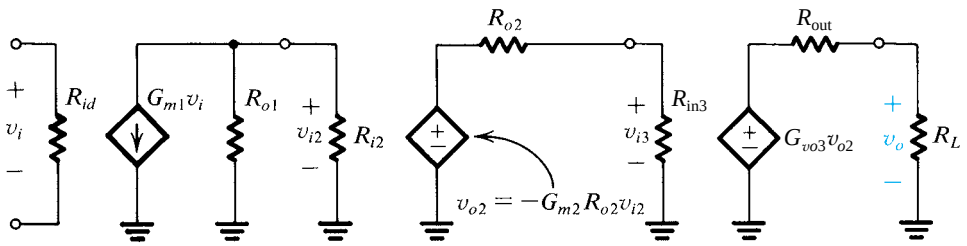


Figure 12.31 Cascading the small-signal equivalent circuits of the individual stages for the evaluation of the overall voltage gain.

Using the values found earlier yields for the overall open-circuit voltage gain,

$$A_0 \equiv \frac{v_o}{v_i} = -476.1 \times (-526.5) \times 0.97 = 243{,}147 \text{ V/V} \quad (12.112)$$
$$\equiv 107.7 \text{ dB}$$

12.6.2 Frequency Response

The 741 is an internally compensated op amp. It employs the Miller compensation technique, studied in Section 10.13.3, to introduce a dominant low-frequency pole. Specifically, a 30-pF capacitor (C_C) is connected in the negative-feedback path of the second stage. An approximate estimate of the frequency of the dominant pole can be obtained as follows.

From Miller's theorem (Section 9.4.4), we see that the effective capacitance due to C_C between the base of Q_{16} and ground is (see Fig. 12.13)

$$C_{\text{in}} = C_C(1 + |A_2|) \quad (12.113)$$

where A_2 is the second-stage gain. Use of the value calculated for A_2 in Section 12.5.3, $A_2 = -515$, results in $C_{\text{in}} = 15{,}480$ pF. Since this capacitance is quite large, we shall neglect all other capacitances between the base of Q_{16} and signal ground. The total resistance between this node and ground is

$$R_t = R_{o1} \,\|\, R_{i2}$$
$$= 6.7 \text{ M}\Omega \,\|\, 4 \text{ M}\Omega = 2.5 \text{ M}\Omega \quad (12.114)$$

Thus the dominant pole has a frequency f_P given by

$$f_P = \frac{1}{2\pi C_{\text{in}} R_t} = 4.1 \text{ Hz} \quad (12.115)$$

It should be noted that this approach is equivalent to using the approximate formula in Eq. (10.116).

As discussed in Section 10.13.3, Miller compensation provides an additional advantageous effect, namely, pole splitting. As a result, the other poles of the circuit are moved to very high frequencies. This has been confirmed by computer-aided analysis [see Gray et al (2000)].

Assuming that all nondominant poles are at very high frequencies, the calculated values give rise to the Bode plot shown in Fig. 12.32, where $f_{3\text{dB}} = f_P$. The unity-gain bandwidth f_t can be calculated from

$$f_t = A_0 f_{3\text{dB}} \quad (12.116)$$

Thus,

$$f_t = 243{,}147 \times 4.1 \simeq 1 \text{ MHz} \quad (12.117)$$

Although this Bode plot implies that the phase shift at f_t is −90° and thus that the phase margin is 90°, in practice a phase margin of about 80° is obtained. The excess phase shift (about 10°) is due to the nondominant poles. This phase margin is sufficient to provide stable operation of closed-loop amplifiers with any value of feedback factor β. This convenience of

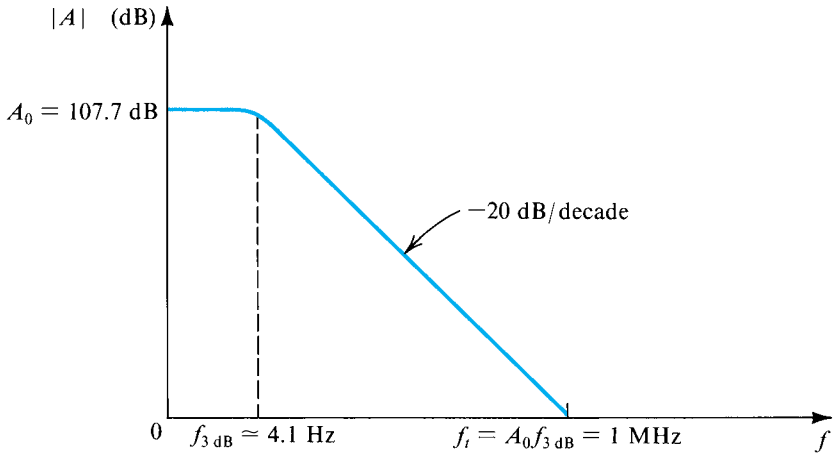


Figure 12.32 Bode plot for the 741 gain, neglecting nondominant poles.

use of the internally compensated 741 is achieved at the expense of a great reduction in open-loop gain and hence in the amount of negative feedback. In other words, if one requires a closed-loop amplifier with a gain of 1000, then the 741 is *overcompensated* for such an application, and one would be much better off designing one's own compensation (assuming, of course, the availability of an op amp that is not already internally compensated).

12.6.3 A Simplified Model

Figure 12.33 shows a simplified model of the 741 op amp in which the high-gain second stage, with its feedback capacitance C_C, is modeled by an ideal integrator. In this model, the gain of the second stage is assumed to be sufficiently large that a virtual ground appears at its input. For this reason the output resistance of the input stage and the input resistance of the second stage have been omitted. Furthermore, the output stage is assumed to be an ideal unity-gain follower. Except for the presence of the output stage, this model is identical to that which we used for the two-stage CMOS amplifier in Section 12.1.4 (Fig. 12.3).

Analysis of the model in Fig. 12.33 gives

$$A(s) \equiv \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_C} \tag{12.118}$$

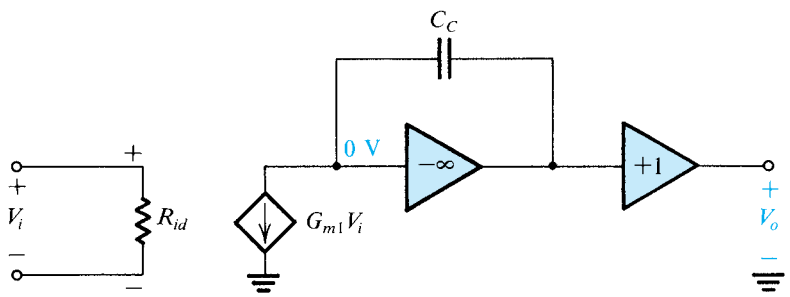


Figure 12.33 A simple model for the 741 based on modeling the second stage as an integrator.

Thus,

$$A(j\omega) = \frac{G_{m1}}{j\omega C_C} \tag{12.119}$$

and the magnitude of gain becomes unity at $\omega = \omega_t$, where

$$\omega_t = \frac{G_{m1}}{C_C} \tag{12.120}$$

Substituting $G_{m1} = 1/5.26$ mA/V and $C_C = 30$ pF yields

$$f_t = \frac{\omega_t}{2\pi} \simeq 1 \text{ MHz} \tag{12.121}$$

which is equal to the value calculated before. It should be pointed out, however, that this model is valid only at frequencies $f \gg f_{3\text{dB}}$. At such frequencies the gain falls off with a slope of −20 dB/decade, just like that of an integrator.

12.6.4 Slew Rate

The slew-rate limitation of op amps is discussed in Chapter 2. Here we shall illustrate the origin of the slewing phenomenon in the context of the 741 circuit. This development is similar to that we presented for the CMOS op-amp in Section 12.1.6.

Consider the unity-gain follower of Fig. 12.34 with a step of, say, 10 V applied at the input. Because of amplifier dynamics, its output will not change in zero time. Thus immediately after the input is applied, almost the entire value of the step will appear as a differential signal between the two input terminals. This large input voltage causes the input stage to be **overdriven**, and its small-signal model no longer applies. Rather, half the stage cuts off and the other half conducts all the current. Specifically, reference to Fig. 12.13 shows that a large positive differential input voltage causes Q_1 and Q_3 to conduct all the available bias current ($2I$) while Q_2 and Q_4 will be cut off. The current mirror Q_5, Q_6, and Q_7 will still function, and Q_6 will produce a collector current of $2I$.

Using the observations above, and modeling the second stage as an ideal integrator, results in the model of Fig. 12.35. From this circuit we see that the output voltage will be a ramp with a slope of $2I/C_C$:

$$v_O(t) = \frac{2I}{C_C}t \tag{12.122}$$

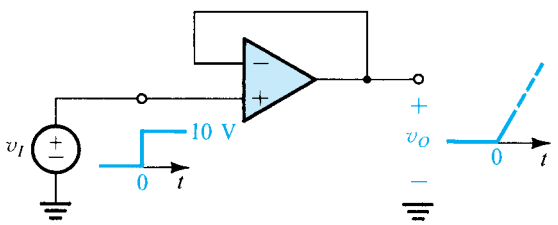


Figure 12.34 A unity-gain follower with a large step input. Since the output voltage cannot change instantaneously, a large differential voltage appears between the op-amp input terminals.

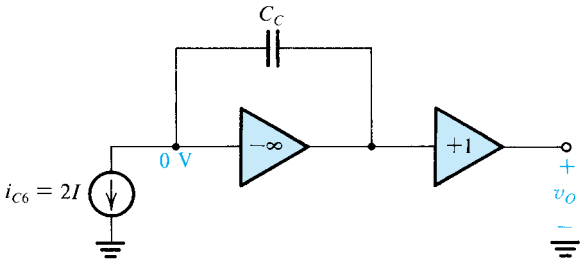


Figure 12.35 Model for the 741 op amp when a large positive differential signal is applied.

Thus the slew rate SR is given by

$$SR = \frac{2I}{C_C} \tag{12.123}$$

For the 741, $I = 9.5\ \mu A$ and $C_C = 30$ pF, resulting in $SR = 0.63\ V/\mu s$.

It should be pointed out that this is a rather simplified model of the slewing process. More detail can be found in Gray et al., (2000).

EXERCISE

12.25 Use the value of the slew rate calculated above to find the full-power bandwidth f_M of the 741 op amp. Assume that the maximum output is ±10 V.
Ans. 10 kHz

12.6.5 Relationship Between f_t and SR

A simple relationship exists between the unity-gain bandwidth f_t and the slew rate SR. This relationship is obtained by combining Eqs. (12.120), (12.123), and

$$SR = \frac{2I}{G_{m1}}\omega_t \tag{12.124}$$

and then using Eq. (12.83′) to obtain

$$SR = \frac{4I}{g_{m1}}\omega_t \tag{12.125}$$

Now, since g_{m1} is the transconductance of each of Q_1 through Q_4,

$$g_{m1} = \frac{I}{V_T} \tag{12.126}$$

Thus,

$$SR = 4V_T\omega_t \tag{12.127}$$

As a check, for the 741 we have

$$SR = 4 \times 25 \times 10^{-3} \times 2\pi \times 10^6 = 0.63\ V/\mu s$$

which is the result obtained previously. Observe that Eq. (12.127) is of the same form as Eq. (12.42), which applies to the two-stage CMOS op amp. Here, $4V_T$ replaces V_{OV}. Since, typically, V_{OV} will be two to three times the value of $4V_T$, a two-stage CMOS op amp with an f_t equal to that of the 741 exhibits a slew rate that is two to three times as large as that of the 741.

A general form for the relationship between SR and ω_t for an op amp with a structure similar to that of the 741 (including the two-stage CMOS circuit) is

$$SR = \omega_t/a \tag{12.128}$$

where a is the constant of proportionality relating the transconductance of the first stage G_{m1}, to the *total* bias current of the input differential stage. That is, for the 741 circuit $G_{m1} = a(2I)$, while for the CMOS circuit of Fig. 12.1, $G_{m1} = aI$.[3] For a given ω_t, a higher value of SR is obtained by making a smaller; that is, the total bias current is kept constant and G_{m1} is reduced. This is a viable technique for increasing slew rate. It is referred to as the **G_m-reduction method** (see Exercise 12.27).

EXERCISES

12.26 Consider the integrator model of the op amp in Fig. 12.33. Find the value of the resistor that, when connected across C_C, provides the correct value of the dc gain.
Ans. 1279 MΩ

D12.27 If a resistance R_E is included in each of the emitter leads of Q_3 and Q_4 show that $SR = 4(V_T + IR_E/2)\omega_t$. Hence find the value of R_E that would double the 741 slew rate while keeping ω_t and I unchanged. What are the new values of C_C, the dc gain, and the 3-dB frequency?
Ans. 5.26 kΩ; 15 pF; 101.7 dB (a 6-dB decrease); 8.2 Hz

12.7 Modern Techniques for the Design of BJT Op Amps

Although the ingenious techniques employed in the design of the 741 op amp have stood the test of time, they are now more than 40 years old! Technological advances have resulted in changes in the user requirements of general-purpose bipolar op amps. The resulting more demanding specifications have in turn posed new challenges to analog IC designers who, as they have done repeatedly before, are responding with new and exciting circuits. In this section we present a sample of recently developed design techniques. For more on this rather advanced topic the reader is referred to the Analog Circuits section of the bibliography in Appendix G.

12.7.1 Special Performance Requirements

Many of the special performance requirements stem from the need to operate modern op amps from power supplies of much lower voltages. Thus while the 741-type op amp operated from

[3]The difference is just a matter of notation; We used I to denote the total bias current of the input differential stage of the CMOS circuit, and we used $2I$ for the 741 case!

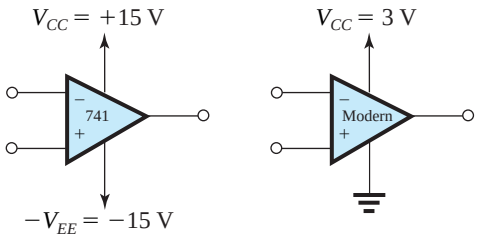


Figure 12.36 Power supply requirements have changed considerably. Modern BJT op amps are required to operate from a single supply V_{CC} of 2 to 3 V.

±15-V power supplies, many modern BJT op amps are required to operate from a *single power supply of only 2* V *to 3* V. This is done for a number of reasons, including the following.

1. Modern small-feature-size IC fabrication technologies require low power-supply voltages.
2. Compatibility must be achieved with other parts of the system that use low-voltage supplies.
3. Power dissipation must be minimized, especially for battery-operated equipment.

As Fig. 12.36 indicates, there are two important changes: the use of a single ground-referenced power supply V_{CC}, and the low value of V_{CC}. Both of these requirements give rise to changes in performance specifications and pose new design challenges. In the following we discuss two of the resulting changes.

Rail-to-Rail Input Common-Mode Range Recall that the input common-mode range of an op amp is the range of common-mode input voltages for which the op amp operates properly and meets its performance specifications, such as voltage gain and CMRR. Op amps of the 741 type operate from ±15-V supplies and exhibit an input common-mode range that extends to within a couple of volts of each supply. Such a gap between the input common-mode range and the power supply is obviously unacceptable if the op amp is to be operated from a single supply that is only 2 V to 3 V. Indeed we will now show that these single-supply, low-voltage op amps need to have an input common-mode range that extends over the entire supply voltage, 0 to V_{CC}, referred to as rail-to-rail input common mode range.

Consider first the inverting op-amp configuration shown in Fig. 12.37(a). Since the positive input terminal is connected to ground (which is the voltage of the negative-supply rail),

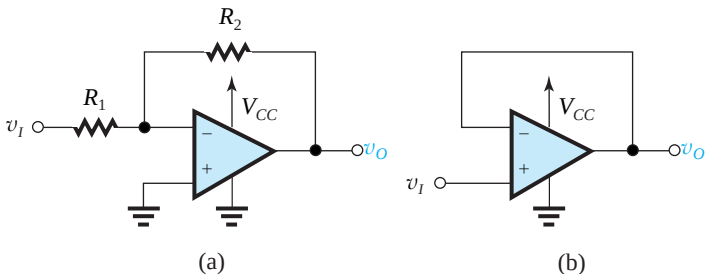


Figure 12.37 **(a)** In the inverting configuration, the *+ive* op-amp input is connected to ground; thus it is imperative that the input common-mode range includes ground. **(b)** In the unity-gain follower configuration, $v_{ICM} = v_I$; thus it is highly desirable for the input common-mode range to include ground and V_{CC}.

ground voltage has to be within the allowable input common-mode range. In fact, because for positive output voltages the voltage at the inverting input terminal can go slightly negative, the input common-mode range should extend below the negative-supply rail (ground).

Next consider the unity-gain voltage follower obtained by applying 100% negative feedback to an op amp, as shown in Fig. 12.37(b). Here the input common-mode voltage is equal to the input signal v_I. To maximize the usefulness of this buffer amplifier, its input signal v_I should be allowed to extend from 0 to V_{CC}, especially since V_{CC} is only 2 to 3 V. Thus the input common-mode range should include also the positive supply rail. As will be seen shortly, modern BJT op amps can operate over an input common-mode voltage range that extends a fraction of a volt beyond its two supply rails: that is, more than rail-to-rail operation!

Near Rail-to-Rail Output Signal Swing In the 741 op amp, we were satisfied with an output that can swing to within 2 V or so of each of the supply rails. With a supply of ±15 V, this capacity resulted in a respectable ±13-V output range. However, to limit the output swing to within 2 V of the supply rails in an op amp operating from a single 3-V supply would result in an unusable device! Thus, here too, we require near rail-to-rail operation. As we shall see in Section 12.7.5, this requirement forces us to adopt a whole new approach to output-stage design.

Device Parameters The technology we shall use in the examples, exercises, and problems for this section has the following characteristics:

$$\begin{aligned} &npn \text{ Transistors:} \quad \beta = 40 \qquad V_A = 30\ V \\ &pnp \text{ Transistors:} \quad \beta = 10 \qquad |V_A| = 20\ V \end{aligned}$$

For both, $|V_{BE}| \simeq 0.7$ V and $|V_{CE\text{sat}}| \simeq 0.1$ V. It is important to note that we will assume that for this technology, the transistor will remain in the active mode for $|V_{CE}|$ as low as 0.1 V (in other words, that 0.6 V is needed to forward-bias the CBJ).

12.7.2 Bias Design

As in the 741 circuit, the bias design of modern BJT amplifiers makes extensive use of current mirrors and current-steering circuits (Sections 7.4 and 7.5). Typically, however, the bias currents are small (in the micro amp range). Thus, the Widlar current source (Section 7.5.5) is especially popular here. As well, emitter-degeneration resistors (in the tens-of-kilohm range) are frequently used.

Figure 12.38 shows a self-biased current-reference source that utilizes a Widlar circuit formed by Q_1, Q_2, and R_2, and a current mirror Q_3–Q_4 with matched emitter-degeneration resistors R_3 and R_4. The circuit establishes a current I in each of the four transistors, with the value of I determined as follows. Neglecting base currents and r_o's for simplicity, we write

$$V_{BE1} = V_T \ln\left(\frac{I}{I_{S1}}\right)$$

$$V_{BE2} = V_T \ln\left(\frac{I}{I_{S2}}\right)$$

Thus,

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right)$$

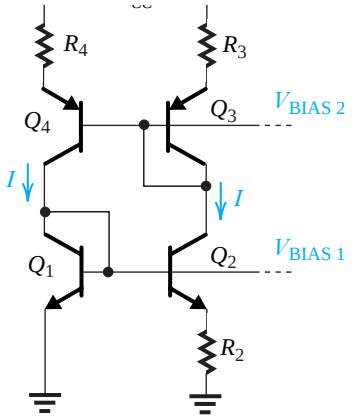


Figure 12.38 A self-biased current-reference source utilizing a Widler circuit to generate $I = V_T/R_2 \ln(I_{S2}/I_{S1})$ The bias voltages V_{BIAS1} and V_{BIAS2} are utilized in other parts of the op-amp circuit for biasing other transistors.

But,

$$V_{BE1} - V_{BE2} = IR_2$$

Thus,

$$I = \frac{V_T}{R_2} \ln\left(\frac{I_{S2}}{I_{S1}}\right) \tag{12.129}$$

Thus the value of I is determined by R_2 and the ratio of the emitter areas of Q_1 and Q_2. Also, observe that I is independent of V_{CC}, a highly desirable outcome. Neglecting the temperature dependence of R_2, we see that I is directly PTAT (*p*roportional *t*o the *a*bsolute *t*emperature T). It follows that transistors biased by I or mirrored versions of it will exhibit g_m's that are constant independent of temperature!

EXERCISE

D12.28 Design the circuit in Fig. 12.38 to generate a current $I = 10$ μA. Utilize transistors Q_1 and Q_2 having their areas in a 1:2 ratio. Assume that Q_3 and Q_4 are matched and design for a 0.2-V drop across each of R_3 and R_4. Specify the values of R_2, R_3, and R_4.
Ans. 1.73 kΩ; 20 kΩ; 20 kΩ

The circuit in Fig. 12.38 provides a bias line V_{BIAS1} with a voltage equal to V_{BE1}. This can be used to bias other transistors and thus generate currents proportional to I by appropriately scaling their emitter areas. Similarly, the circuit provides a bias line V_{BIAS2} at a voltage $(IR_3 + V_{EB3})$ below V_{CC}. This bias line can be used to bias other transistors and thus generate constant currents proportional to I by appropriately scaling emitter areas and emitter-degeneration resistances. These ideas are illustrated in Fig. 12.39.

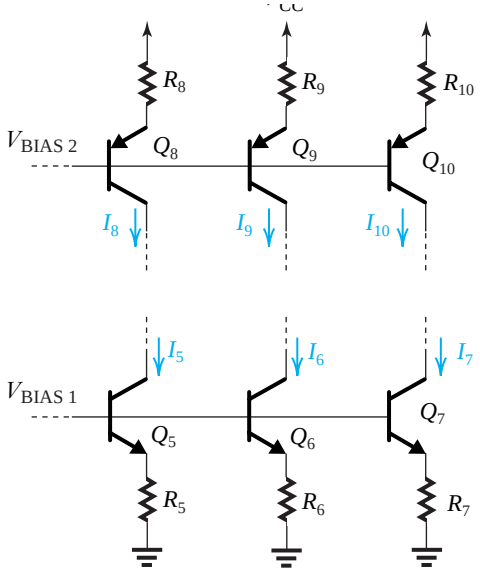


Figure 12.39 The bias lines V_{BIAS1} and V_{BIAS2} provided by the circuit in Fig. 12.38 are utilized to bias other transistors and generate constant current I_5 to I_{10}. Both the transistor area and the emitter degeneration resistance value have to be appropriately scaled.

EXERCISE

D12.29 Refer to the circuit in Fig. 12.39 and assume that the V_{BIAS2} line is connected to the corresponding line in Fig. 12.38. It is required to generate currents $I_8 = 10\ \mu A$, $I_9 = 20\ \mu A$, and $I_{10} = 5\ \mu A$. Specify the required emitter areas of Q_8, Q_9, and Q_{10} as ratios of the emitter area of Q_3. Also specify the values required for R_8, R_9, and R_{10}. Use the values of R_3 and R_4 found in Exercise 12.28. Ignore base currents.

Ans. 1, 2, 0.5; 20 kΩ, 10 kΩ, 40 kΩ

12.7.3 Design of the Input Stage to Obtain Rail-to-Rail V_{ICM}

The classical differential input stage with current-mirror load is shown in Fig. 12.40(a). This is essentially the core of the 741 input stage, except that here we are using a single positive power supply. As well, the CMOS counterpart of this circuit is utilized in nearly every

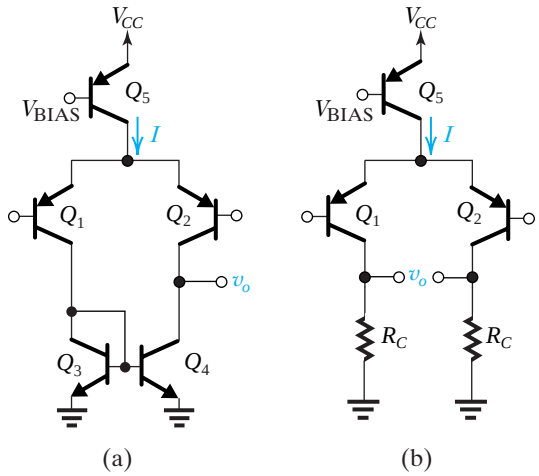


Figure 12.40 For the input common-mode range to include ground voltage, the classical current-mirror-loaded input stage in **(a)** has to be replaced with the resistively-loaded configuration in **(b)** with the dc voltage drop across R_C limited to 0.2–0.3 V.

CMOS op-amp design (see Section 12.1). Unfortunately, this very popular circuit does not meet our requirement of rail-to-rail common-mode operation.

Consider first the low end of the input common-mode range. The value of $V_{ICM\min}$ is limited by the need to keep Q_1 in the active mode. Specifically, since the collector of Q_1 is at a voltage $V_{BE3} \simeq 0.7$ V, we see that the voltage applied to the base of Q_1 cannot go lower than 0.1 V without causing the collector–base junction of Q_1 to become forward biased. Thus $V_{ICM\min} = 0.1$ V, and the input common-mode range does *not* include ground voltage as required.

The only way to extend $V_{ICM\min}$ to 0 V is to lower the voltage at the collector of Q_1. This in turn can be achieved only by abandoning the use of the current-mirror load and utilizing instead resistive loads, as shown in Fig. 12.40(b). Observe that in effect we are *going back* to the resistively loaded differential pair with which we began our study of differential amplifiers in Chapter 8!

The minimum allowed value of V_{ICM} in the circuit of Fig. 12.40(b) is still of course limited by the need to keep Q_1 and Q_2 in the active mode. This in turn is achieved by avoiding V_{ICM} values that cause the base voltages of Q_1 and Q_2 to go below their collector voltages by more than 0.6 V,

$$V_{ICM\min} = V_{R_C} - 0.6 \text{ V}$$

where V_{R_C} is the voltage drop across each of R_{C1} and R_{C2}. Now if V_{R_C} is selected to be 0.2 to 0.3 V, then $V_{ICM\min}$ will be –0.4 V to –0.3 V, which is exactly what we need.

The major drawback of replacing the current-mirror load with resistive loads is that the differential gain realized is considerably reduced,

$$\frac{v_o}{v_{id}} = -g_{m1,2}R_C$$
$$= -\frac{I/2}{V_T} R_C = -\frac{V_{R_C}}{V_T}$$

where we have neglected r_o for simplicity. Thus for $V_{R_C} = 0.3$ V, the gain realized is only 12 V/V. As we will see shortly, this low-gain problem can be solved by cascoding.

Next consider the upper end of the input common-mode range. Reference to the circuit in Fig. 12.40(b) shows that the maximum voltage that can be applied to the bases of Q_1 and Q_2 is limited by the need to keep the current-source transistor in the active mode. This in turn is achieved by ensuring that the voltage across Q_5, V_{EC5} does not fall below 0.1 V or so. Thus the maximum value of V_{ICM} will be a voltage $V_{EB1,2}$ or approximately 0.7 V lower,

$$V_{ICM\max} = V_{CC} - 0.1 - 0.7 = V_{CC} - 0.8$$

That is, the upper end of the input common-mode range is at least 0.8 V below V_{CC}, a severe limitation.

To recap, while the circuit in Fig. 12.40(b) has $V_{ICM\min}$ of a few tenths of a volt below the negative power-supply rail (at ground voltage), the upper end of V_{ICM} is rather far from V_{CC},

$$-0.3 \le V_{ICM} \le V_{CC} - 0.8$$

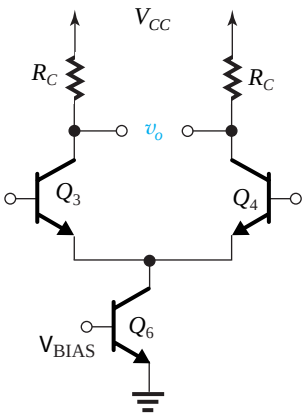


Figure 12.41 The complement of the circuit in Fig. 12.40(b). While the input common-mode range of the circuit in Figure 12.40(b) extends below ground, here it extends above V_{CC}. Connecting the two circuits in parallel, as will be shown, results in a rail-to-rail V_{ICM} range.

where we have assumed $V_{R_C} = 0.3$ V. To extend the upper end of V_{ICM}, we adopt a solution similar to that used in the CMOS case (Section 12.2.6, Fig. 12.11), namely, we utilize a parallel complementary input stage. Toward that end, note that the *npn* version of the circuit of Fig. 12.40(b), shown in Fig. 12.41, has a common-input range of

$$0.8 \le V_{ICM} \le V_{CC} + 0.3$$

where we have assumed that $V_{R_C} = 0.3$ V. Thus, as expected, the high end meets our specifications and in fact is above the positive supply rail by 0.3 V. The lower end, however, does not; but this should cause us no concern because the lower end will be looked after by the *pnp* pair. Finally, note that there is a range of V_{ICM} in which both the *pnp* and the *npn* circuits will be active and properly operating,

$$0.8 \le V_{ICM} \le V_{CC} - 0.8$$

Figure 12.42 shows an input stage that achieves more than rail-to-rail input common-mode range by utilizing a *pnp* differential pair (Q_1, Q_2) and an *npn* differential pair (Q_3, Q_4), connected in parallel. To keep the diagram simple, we are not showing the parallel connection of the input terminals; the + input terminals are assumed to be connected together, and similarly for the – input terminals. In order to increase the gain obtained from the resistively loaded differential pairs, a folded cascode stage is added. Here R_7 and R_8 are the resistive loads of the *pnp* pair Q_1–Q_2, and Q_7–Q_8 are its cascode transistors. Similarly, R_9 and R_{10} are the resistive loads of the *npn* pair Q_3–Q_4, and Q_9–Q_{10} are its cascode transistors. Observe that the cascode transistors do "double duty." For instance, Q_7–Q_8 operate as the cascode devices for Q_1–Q_2 and at the same time as current-source loads for Q_9–Q_{10}. A similar statement can be made about Q_9–Q_{10}. The output voltage of the first stage, v_{od}, is taken between the collectors of the cascode devices.

For $V_{ICM} \ll 0.8$ V, the *npn* stage will be inactive and the gain is determined by the transconductance G_m of the Q_1–Q_2 pair together with the output resistance seen between the collectors of the cascode transistors. At the other end of V_{ICM}, that is, $V_{ICM} \gg V_{CC} - 0.8$, the Q_1–Q_2 stage will be inactive, and the gain will be determined by the transconductance G_m of the Q_3–Q_4 pair and the output resistance between the collectors of the cascode devices. In the overlap region $0.8 \le V_{ICM} \le V_{CC} - 0.8$, both the *pnp* and *npn* stages will be active and their effective transconductances G_m add up, thus resulting in a higher gain. The dependence of the differential gain on the input common-mode V_{ICM} is usually undesirable

and can be reduced considerably by arranging that one of the two differential pairs is turned off when the other one is active.[4]

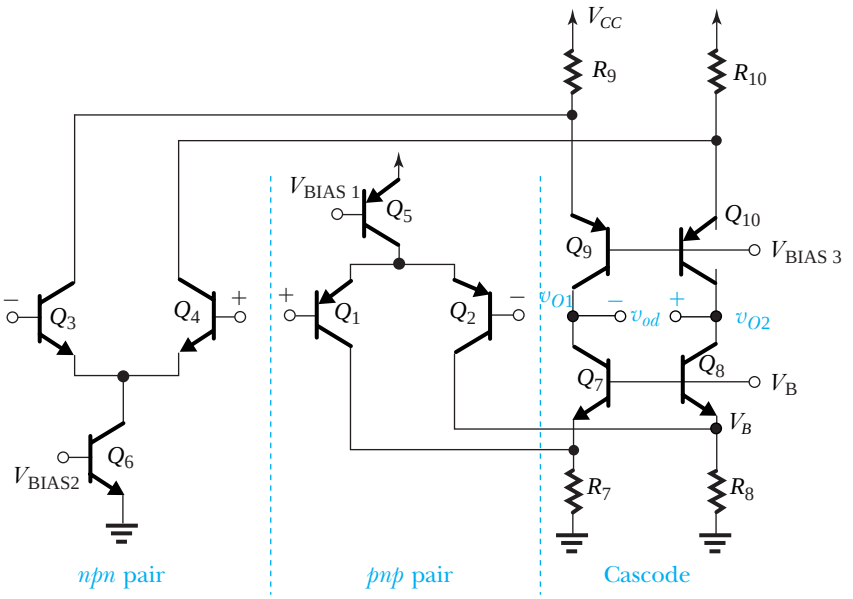


Figure 12.42 Input stage with rail-to-rail input common-mode range and a folded-cascode stage to increase the gain. Note that all the bias voltages including V_{BIAS3} and V_B are generated elsewhere on the chip.

Example 12.5

It is required to find the input resistance and the voltage gain of the input stage shown in Fig. 12.42. Let $V_{ICM} \ll 0.8$ V so that the Q_3–Q_4 pair is off. Assume that Q_5 supplies 10 μA, that each of Q_7 to Q_{10} is biased at 10 μA, and that all four cascode transistors are operating in the active mode. The input resistance of the second stage of the op amp (not shown) is $R_L = 2$ MΩ. The emitter-degeneration resistances are $R_7 = R_8 = 20$ kΩ, and $R_9 = R_{10} = 30$ kΩ. Recall that the device parameters are $\beta_N = 40$, $\beta_P = 10$, $V_{An} = 30$ V, $|V_{Ap}| = 20$ V.

Solution

Since the stage is fully balanced, we can use the differential half-circuit shown in Fig. 12.43(a). The input resistance R_{id} is twice the value of $r_{\pi 1}$,

$$R_{id} = 2r_{\pi 1} = 2\beta_P / g_{m1}$$

where

$$g_{m1} = \frac{I_{C1}}{V_T} = \frac{5 \times 10^{-6}}{25 \times 10^{-3}} = 0.2 \text{ mA/V}$$

[4]This is done in the NE5234 op amp, whose circuit is described and analyzed in great detail in Gray et al., (2009).

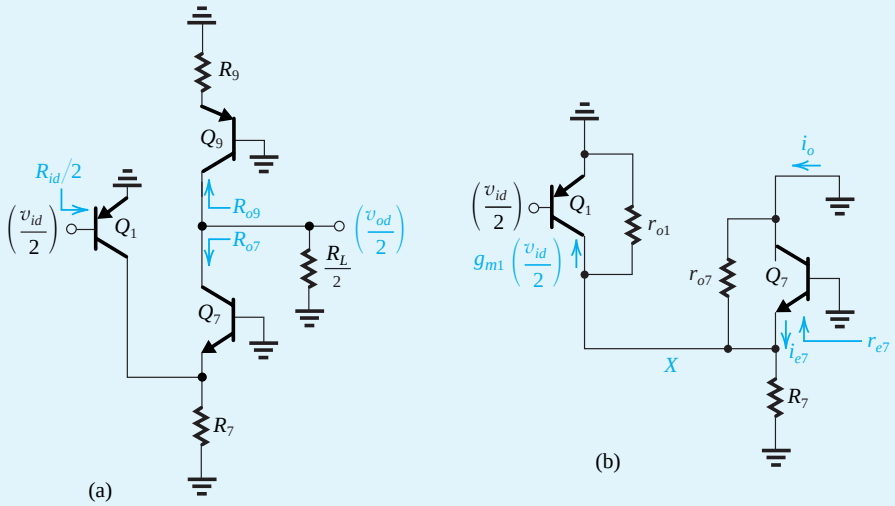


Figure 12.43 (**a**) Differential half circuit for the input stage shown in Fig. 12.42 with $V_{ICM} \ll 0.8$ V. (**b**) Determining $G_{m1} = i_o/(v_{id}/2)$

Thus,

$$R_{id} = \frac{2 \times 10}{0.2} = 100 \text{ k}\Omega$$

To find the short-circuit transconductance, we short the output to ground as shown in Fig. 12.43(b) and find G_{m1} as

$$G_{m1} = \frac{i_{c7}}{v_{id}/2}$$

At node X we have four parallel resistances to ground,

$$r_{o1} = \frac{|V_{Ap}|}{I_{C1}} = \frac{20 \text{ V}}{5 \text{ μA}} = 4 \text{ MΩ}$$

$$R_7 = 20 \text{ kΩ}$$

$$r_{o7} = \frac{V_{An}}{I_{C7}} = \frac{30 \text{ V}}{10 \text{ μA}} = 3 \text{ MΩ}$$

$$r_{e7} \simeq \frac{1}{g_{m7}} = \frac{V_T}{I_{C7}} = \frac{25 \text{ mV}}{10 \text{ μA}} = 2.5 \text{ kΩ}$$

Obviously r_{o1} and r_{o7} are very large and can be neglected. Then, the portion of $g_{m1}(v_{id}/2)$ that flows into the emitter proper of Q_7 can be found from

$$i_{e7} \simeq \left(g_{m1}\left(\frac{v_{id}}{2}\right)\frac{R_7}{R_7 + r_{e7}}\right)$$

$$= g_{m1}\left(\frac{v_{id}}{2}\right)\frac{20}{20 + 2.5} = 0.89 g_{m1}\left(\frac{v_{id}}{2}\right)$$

and the output short-circuit current i_o is

$$i_o \simeq i_{e7} = 0.89 g_{m1}(v_{id}/2)$$

Example 12.5 *continued*

Thus,

$$G_{m1} \equiv \frac{i_o}{v_{id}/2} = 0.89 g_{m1} = 0.89 \times 0.2 = 0.18 \text{ mA/V}$$

To find the voltage gain, we need to determine the total resistance between the output node and ground for the circuit in Fig. 12.43(a),

$$R = R_{o9} \parallel R_{o7} \parallel (R_L/2)$$

The resistance R_{o9} is the output resistance of Q_9, which has an emitter-degeneration resistance R_9. Thus R_{o9} can be found using Eq. (7.50),

$$R_{o9} = r_{o9} + (R_9 \parallel r_{\pi 9})(1 + g_{m9} r_{o9})$$

where

$$r_{o9} = \frac{|V_{Ap}|}{I_{C9}} = \frac{20 \text{ V}}{10 \text{ μA}} = 2 \text{ MΩ}$$

$$g_{m9} = \frac{I_{C9}}{V_T} = \frac{10 \text{ μA}}{25 \text{ mV}} = 0.4 \text{ mA/V}$$

$$r_{\pi 9} = \frac{\beta_P}{g_{m9}} = \frac{10}{0.4 \text{ mA/V}} = 25 \text{ kΩ}$$

Thus

$$R_{o9} = 2 + (30 \parallel 25) \times 10^{-3}(1 + 0.4 \times 2 \times 10^3)$$
$$= 12.9 \text{ MΩ}$$

The resistance R_{o7} is the output resistance of Q_7, which has an emitter-degeneration resistance $(R_7 \parallel r_{o1}) \simeq R_7$. Thus,

$$R_{o7} = r_{o7} + (R_7 \parallel r_{\pi 7})(1 + g_{m7} r_{o7})$$

where

$$r_{o7} = \frac{V_{An}}{I_{C7}} = \frac{30 \text{ V}}{10 \text{ μA}} = 3 \text{ MΩ}$$

$$g_{m7} = \frac{I_{C7}}{V_T} = \frac{10 \text{ μA}}{25 \text{ mV}} = 0.4 \text{ mA/V}$$

$$r_{\pi 7} = \frac{\beta_N}{g_{m7}} = \frac{40}{0.4} = 100 \text{ kΩ}$$

Thus,

$$R_{o7} = 3 + (20 \parallel 100) \times 10^{-3}(1 + 0.4 \times 3 \times 10^3)$$
$$= 23 \text{ MΩ}$$

$$\frac{R_L}{2} = \frac{2 \text{ MΩ}}{2} = 1 \text{ MΩ}$$

The total resistance R can now be found as

$$R = 12.9 \parallel 23 \parallel 1 = 0.89 \text{ M}\Omega$$

Finally, we can find the voltage gain as

$$A_d = \frac{v_{od}/2}{v_{id}/2} = G_{m1}R_1$$

$$= 0.18 \times 0.89 \times 10^3 = 160 \text{ V/V}$$

12.7.4 Common-Mode Feedback to Control the dc Voltage at the Output of the Input Stage

For the cascode circuit in Fig. 12.42 to operate properly and provide high output resistance and thus high voltage gain, the cascode transistors Q_7 through Q_{10} must operate in the active mode at all times. However, relying solely on matching will not be sufficient to ensure that the currents supplied by Q_9 and Q_{10} are exactly equal to the currents supplied by Q_7 and Q_8. Any small mismatch ΔI between the two sets of currents will be multiplied by the large output resistance between each of the collector nodes and ground, and thus there will be large changes in the voltages v_{O1} and v_{O2}. These changes in turn can cause one set of the current sources (i.e., Q_7–Q_8 or Q_9–Q_{10}) to saturate. We therefore need a circuit that detects the change in the dc or common-mode component V_{CM} of v_{O1} and v_{O2},

$$V_{CM} = \frac{1}{2}(v_{O1} + v_{O2}) \tag{12.130}$$

and adjusts the bias voltage on the bases of Q_7 and Q_8, V_B, to restore current equality. This negative-feedback loop should be insensitive to the differential signal components of v_{O1} and v_{O2}; otherwise it would reduce the differential gain. Thus the feedback loop should provide **common-mode feedback** (CMF).

Figure 12.44 shows the cascode circuit with the CMF circuit shown as a black box. The CMF circuit accepts v_{O1} and v_{O2} as inputs and provides the bias voltage V_B as output. In a particular implementation we will present shortly, the CMF circuit has the transfer characteristic

$$V_B = V_{CM} + 0.4 \tag{12.131}$$

By keeping V_B higher than V_{CM} by only 0.4 V, the CMF circuit ensures that Q_7 and Q_8 remain active (0.6 V is needed for saturation).

The nominal value of V_B is determined by the quiescent current of Q_7 through Q_{10}, the quiescent value of I_1 and I_2, and the value of R_7 and R_8. The resulting nominal value of V_B and the corresponding value of V_{CM} from Eq. (12.131) are designed to ensure that Q_9 and Q_{10} operate in the active mode. Here, it is important to recall that V_{BIAS3} is determined by the rest of the op-amp bias circuit.

To see how the CMF circuit regulates the dc voltage V_{CM}, assume that for some reason V_B is higher than it should be and as a result the currents of Q_7 and Q_8 exceed the currents supplied by Q_9 and Q_{10} by an increment ΔI. When multiplied by the total resistance between each of the output nodes and ground, the increment ΔI will result in a large

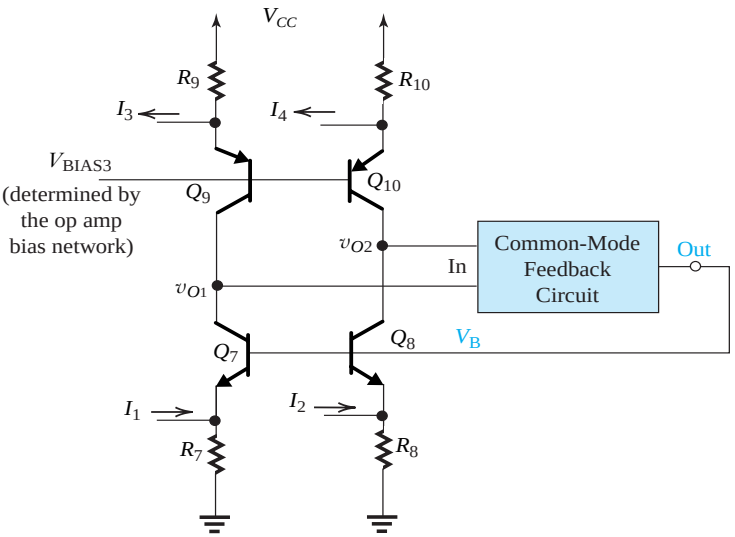


Figure 12.44 The cascode output circuit of the input stage and the CMF circuit that responds to the common-mode component $V_{CM} = \frac{1}{2}(v_{O1} + v_{O2})$ by adjusting V_B so that Q_7–Q_8 conduct equal currents to Q_9–Q_{10}, and Q_7–Q_{10} operate in the active mode.

negative voltage increment in v_{O1} and v_{O2}. The CMF circuit responds by lowering V_B to the value that restores the equality of currents. The change in V_B needed to restore equilibrium is usually small (see Example 12.6 below) and according to Eq. (12.131) the corresponding change in V_{CM} will be equally small. Thus we see negative feedback in action: It minimizes the initial change and thus keeps V_{CM} nearly constant at its nominal value, which is designed to operate Q_7 through Q_{10} in the active region.

We conclude by considering briefly a possible implementation of the CMF circuit. Figure 12.45 shows the second stage of an op-amp circuit. The circuit is fed by the outputs of the input stage, v_{O1} and v_{O2},

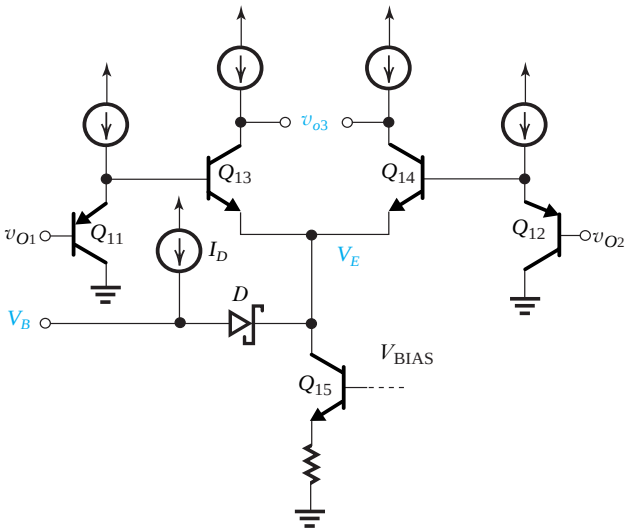


Figure 12.45 An op amp second stage incorporating the common-mode feedback circuit for the input stage. Note that the circuit generates the voltage V_B needed to bias the cascode circuit in the first stage. Diode D is a Schottky-barrier diode which exhibits a forward voltage drop of about 0.4V.

$$v_{O1} = V_{CM} + v_d/2$$
$$v_{O2} = V_{CM} - v_d/2$$

In addition to amplifying the differential component of v_d, the circuit generates a dc voltage V_B,

$$V_B = V_{CM} + 0.4$$

To see how the circuit works, note that Q_{11} and Q_{12} are emitter followers that minimize the loading of the second stage on the input stage. The emitter followers deliver to the bases of the differential pair Q_{13}–Q_{14} voltages that are almost equal to v_{O1} and v_{O2} but dc shifted by $V_{EB11,12}$. Thus the voltage at the emitters of Q_{13}–Q_{14} will be

$$V_E = V_{CM} + V_{EB11,12} - V_{BE13,14}$$

which reduces to

$$V_E \simeq V_{CM}$$

The voltage V_B is simply equal to V_E plus the voltage drop of diode D_1. The latter is a **Schottky barrier diode** (SBD), which features a low forward drop of about 0.4 V. Thus,

$$V_B = V_E + V_D = V_{CM} + 0.4$$

as required.

Example 12.6

Consider the operation of the circuit in Fig. 12.44. Assume that $V_{ICM} \ll 0.8$ V and thus the *npn* input pair (Fig. 12.42) is off. Hence $I_3 = I_4 = 0$. Also assume that only dc voltages are present and thus $I_1 = I_2 = 5\ \mu$A. Each of Q_7 to Q_{10} is biased at 10 μA, $V_{CC} = 3$ V, $V_{\text{BIAS3}} = V_{CC} - 1$, $R_7 = R_8 = 20\ \text{k}\Omega$, and $R_9 = R_{10} = 30\ \text{k}\Omega$. Neglect base currents and neglect the loading effect of the CMF circuit on the output nodes of the cascode circuit. The CMF circuit provides $V_B = V_{CM} + 0.4$.

(a) Determine the nominal values of V_B and V_{CM}. Does the value of V_{CM} ensure operation in the active mode for Q_7 through Q_{10}?

(b) If the CMF circuit were not present, what would be the change in v_{O1} and v_{O2} (i.e., in V_{CM}) as a result of a current mismatch $\Delta I = 0.3\ \mu$A between Q_7–Q_8 and Q_9–Q_{10}? Use the output resistance values found in Example 12.5.

(c) Now, if the CMF circuit is connected, what change will it cause in V_B to eliminate the current mismatch ΔI? What is the corresponding change in V_{CM} from its nominal value?

Solution

(a) The nominal value of V_B is found as follows:

$$V_B = V_{BE7} + (I_{E7} + I_1)R_7$$
$$\simeq 0.7 + (10 + 5) \times 10^{-3} \times 20$$
$$= 1\ \text{V}$$

Example 12.6 *continued*

The nominal value of V_{CM} can now be found from

$$V_{CM} = V_B - 0.4 = 1 - 0.4 = 0.6 \text{ V}$$

For $Q_7 - Q_8$ to be active,

$$V_{CM} > V_{B7,8} - 0.6$$

that is,

$$V_{CM} > 0.4 \text{ V}$$

For $Q_9 - Q_{10}$ to be active

$$V_{CM} < V_{\text{BIAS3}} + 0.6$$

That is,

$$V_{CM} < V_{CC} - 1 + 0.6$$

resulting in

$$V_{CM} < 2.6 \text{ V}$$

Thus, for all four cascode transistors to operate in the active mode,

$$0.4 \text{ V} < V_{CM} < 2.6 \text{ V}$$

Thus the nominal value of 0.6 V ensures active mode operation.

(b) For $I_{C9} - I_{C7} = I_{C10} - I_{C8} = \Delta I$,

$$\Delta V_{CM} = \Delta I R_{o1}$$

where R_{o1} is the output resistance between the collectors of Q_7 and Q_9 and ground,

$$R_{o1} = R_{o7} \parallel R_{o9}$$

In Example 12.5 we found that $R_{o7} = 23 \text{ M}\Omega$ and $R_{o9} = 12.9$; thus,

$$R_{o1} = 23 \parallel 12.9 = 8.3 \text{ M}\Omega$$

Thus,

$$\Delta V_{CM} = 0.3 \times 8.3 \simeq 2.5 \text{ V}$$

Now if ΔV_{CM} is positive,

$$V_{CM} = 0.6 + 2.5 = 3.1 \text{ V}$$

which exceeds the 2.6 V maximum allowed value before $Q_9 - Q_{10}$ saturate. If ΔV_{CM} is negative,

$$V_{CM} = 0.6 - 2.5 = -1.9 \text{ V}$$

which is far below the +0.4 V needed to keep $Q_7 - Q_8$ in the active mode. Thus, in the absence of CMF, a current mismatch of $\pm 0.3 \ \mu\text{A}$ would cause one set of the cascode transistors (depending on the polarity of ΔI) to saturate.

(c) With the CFB circuit in place, the feedback will adjust V_B by ΔV_B so that the currents in Q_7 and Q_8 will change by a increment equal to ΔI, thus restoring current equality. Since a change ΔV_B results in

$$\Delta I_{C7} = \Delta I_{C8} = \frac{\Delta V_B}{r_{e7} + R_7}$$

then

$$\Delta I = \frac{\Delta V_B}{r_{e7} + R_7}$$

$$\Delta V_B = \Delta I(r_{e7} + R_7)$$

$$= 0.3\ \mu\text{A}\left(\frac{25\ \text{mV}}{10\ \mu\text{A}} + 20\ \text{k}\Omega\right)$$

$$= 0.3 \times 22.5 = 6.75\ \text{mV}$$

Correspondingly

$$\Delta V_{CM} = \Delta V_B = 6.75\ \text{mV}$$

Thus, to restore the current equality, the change required in V_B and V_{CM} is only 6.75 mV.

12.7.5 Output-Stage Design for Near Rail-to-Rail Output Swing

As mentioned earlier, modern low-voltage bipolar op amps cannot afford to use the classical emitter-follower-based class AB output stage; it would consume too much of the power supply voltage. Instead, a complementary pair of common-emitter transistors are utilized, as shown in Fig. 12.46. The output transistors Q_P and Q_N are operated in a class AB fashion. Typically, i_L can be as high as 10 mA to 15 mA and is determined by v_O and R_L. For $i_L = 0$, $i_P = i_N = I_Q$, where the quiescent current I_Q is normally a fraction of a milliamp.

The output stage in Fig. 12.46 is driven by two *separate but equal signals*, v_{BP} and v_{BN}. When v_{BP} and v_{BN} are high, Q_N supplies the load current in the direction opposite to that shown[5] and the output voltage v_O can swing to within 0.1 V or so of ground. In the meantime, Q_P is inactive. Nevertheless, in order to minimize crossover distortion, Q_P is

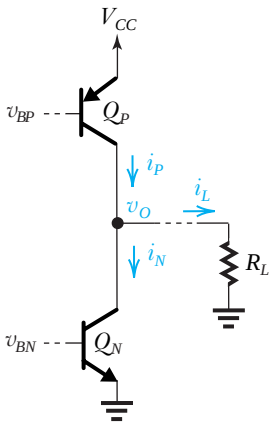


Figure 12.46 In order to provide v_O that can swing to within 0.1 V of V_{CC} and ground, a near rail-to-rail operation, the output stage utilizes common-emitter transistors. Note that the driving signals V_{BP} and V_{BN} are separate but identical.

[5]For this to happen, either R_L is returned to the positive supply (rather than ground) or R_L is capacitively coupled to the amplifier output.

prevented from turning off and is forced (as will be shown shortly) to conduct a minimum current of about $I_Q/2$.

The opposite happens when v_{BP} and v_{BN} are low: Q_P supplies the load current i_L in the direction indicated, and v_O can go up as high as $V_{CC} - 0.1$ V. In the meantime, Q_N is inactive but is prevented from turning off and forced to conduct a minimum current of about $I_Q/2$.

From the description above, we see that v_O can swing to within 0.1 V of each of the supply rails. This near rail-to-rail operation is the major advantage of this CE output stage. Its disadvantage is the relatively high output resistance. However, given that the op amp will almost always be used with a negative-feedback loop, the closed-loop output resistance can still be very low.

A Buffer/Driver Stage The output transistors can be called on to supply currents in the 10 mA to 15 mA range. When this happens, the base currents of Q_P and Q_N can be substantial (recall that $\beta_P \simeq 10$ and $\beta_N \simeq 40$). Such large currents cannot usually be supplied directly by the amplifier stage preceding the output stage. Rather a buffer/driver stage is usually needed, as shown in Fig. 12.47. Here an emitter follower Q_3 is used to drive Q_N. However, because of the low β_P, a double buffer consisting of complementary emitter followers Q_1 and Q_2 is used to drive Q_P. The driver stage is fed by two separate but identical signals v_{IP} and v_{IN} that come from the preceding amplifier stage (which is usually the second stage) in the op amp circuit.[6]

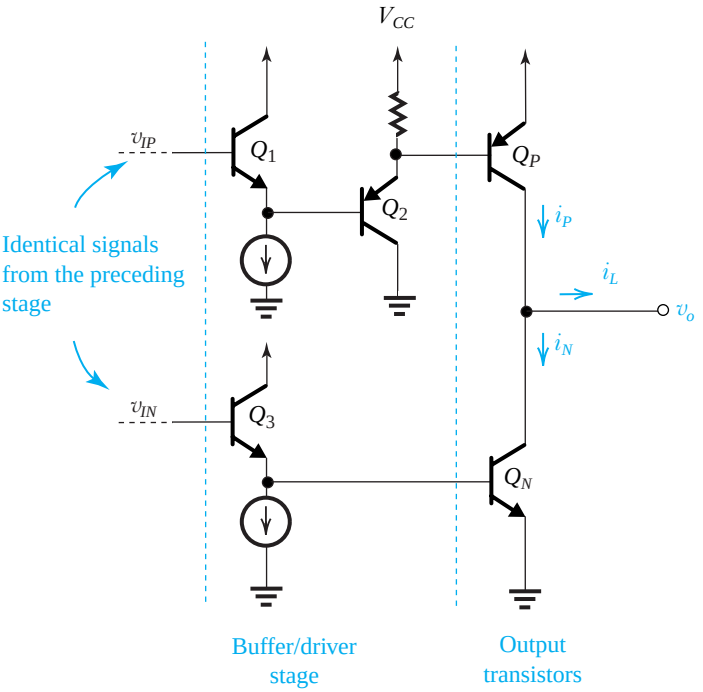


Figure 12.47 The output stage which is operated as class AB needs emitter follower buffers/drives to reduce the loading on the preceding stage and to provide the current gain necessary to drive Q_P and Q_N.

[6]An interesting approach for generating two identical outputs in the second stage is utilized in the NE5234 (see Gray et al., 2009).

EXERCISE

12.30 (a) For the circuit in Fig. 12.47, find the current gain from each of the v_{IP} and v_{IN} terminals to the output in terms of β_P and β_N.

(b) For $i_L = \pm 10$ mA, how much signal current is needed at the v_{IP} and v_{IN} inputs?

Ans. (a) $\beta_N\beta_P^2$, β_N^2; (b) 2.5 μA, 6.25 μA

Establishing I_Q and Maintaining a Minimum Current in the Inactive Transistor We next consider the circuit for establishing the quiescent current I_Q in Q_N and Q_P and for maintaining a minimum current of $I_Q/2$ in the inactive output transistor. Figure 12.48 shows a fuller version of the output stage. In addition to the output transistors Q_P–Q_N and the buffer/driver stage, which we have already discussed, the circuit includes two circuit blocks whose operation we shall now explain.

The first is the circuit composed of the differential pair Q_6–Q_7 and associated transistors Q_4 and Q_5, and resistors R_4 and R_5. This circuit measures the currents in the output transistors, i_P and i_N, and arranges for the current I to divide between Q_6 and Q_7 according to the ratio i_N/i_P, and provides a related output voltage v_E. Specifically, it can be shown [Problem 12.73] that

$$i_{C6} = I\,\frac{i_N}{i_P + i_N} \tag{12.132}$$

$$i_{C7} = I\,\frac{i_P}{i_P + i_N} \tag{12.133}$$

$$v_E = V_T \ln\left[\frac{i_N\, i_P}{i_N + i_P}\,\frac{I}{I_{SN}\, I_{S7}}\right] \tag{12.134}$$

where I_{SN} and I_{S7} are the saturation currents of Q_N and Q_7, respectively. Observe that for $i_P \gg i_N$, $i_{C6} \simeq 0$ and $i_{C7} \simeq I$. Thus Q_6 turns off and Q_7 conducts all of I. The emitter voltage v_E becomes

$$v_E \simeq V_T \ln\left(\frac{i_N}{I_{SN}}\right) + V_T \ln\left(\frac{I}{I_{S7}}\right)$$

Thus,

$$v_E = V_T \ln\left(\frac{i_N}{I_{SN}}\right) + V_{EB7} \tag{12.135}$$

This equation simply states that $v_E = v_{BEN} + V_{EB7}$, which could have been directly obtained from the circuit diagram in Fig. 12.48. The important point to note, however, is that since V_{EB7} is a constant, v_E is determined by the current i_N in the inactive transistor, Q_N. In the other extreme case of $i_N \gg i_P$, $i_{C6} \simeq I$, $i_{C7} \simeq 0$; thus Q_7 turns off and Q_6 conducts all of I. In this case we can use Eq. (12.134) to show that

$$v_E = V_T \ln\left(\frac{i_P}{I_{SN}}\right) + V_{EB6} \tag{12.136}$$

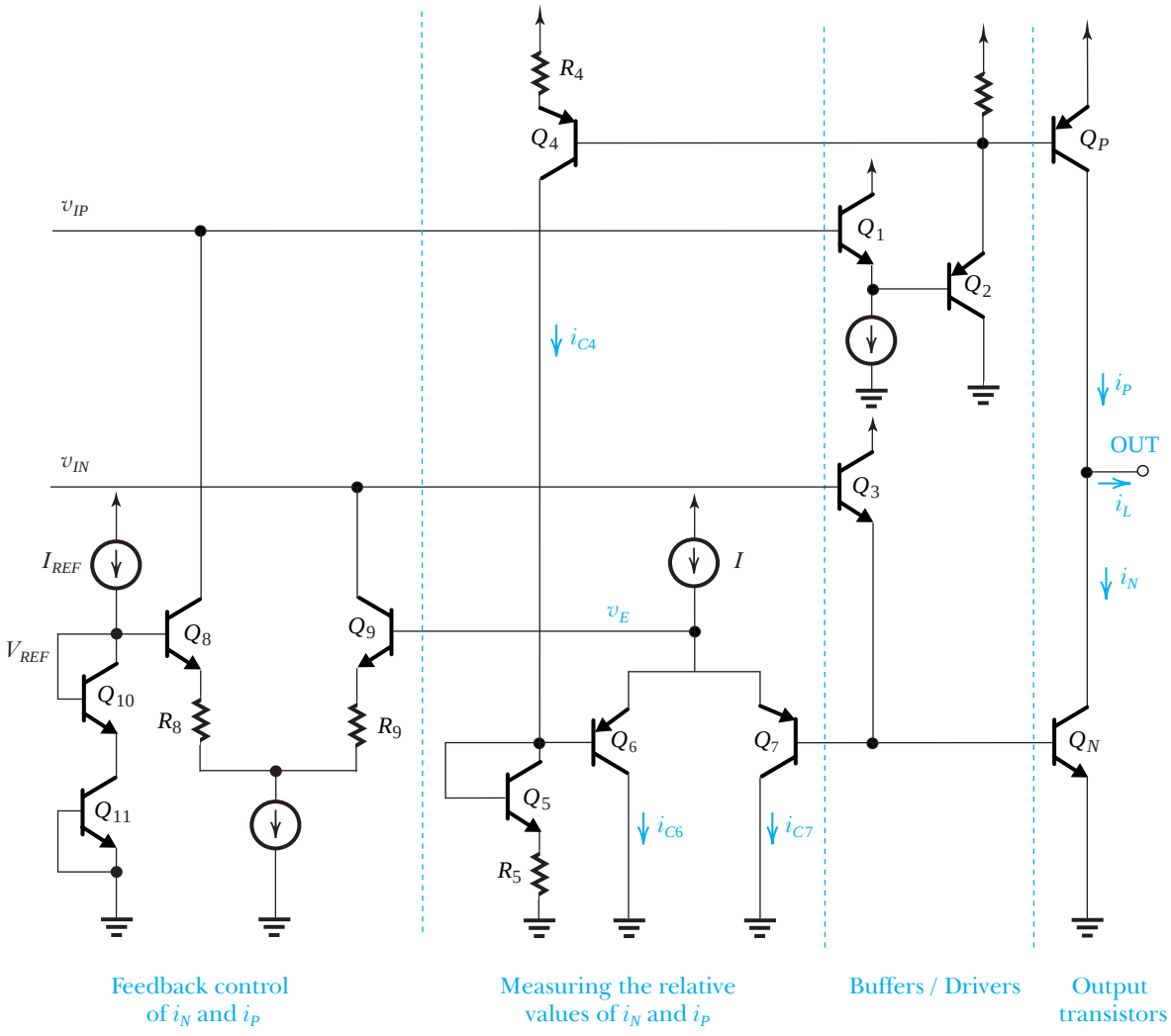


Figure 12.48 A more complete version of the output stage showing the circuits that establish the quiescent current in Q_P and Q_N. As well, this circuit forces a minimum current of $(I_Q/2)$ to follow in the inactive output transistor, thus preventing the transistor from turning off and minimizing crossover distortion.

Thus, here too, since V_{EB6} is a constant, v_E is determined by the current in the inactive transistor, Q_P.

The second circuit block is a differential amplifier composed of Q_8–Q_9 with their emitter-degeneration resistors R_8, R_9. The voltage v_E generated by the measuring circuit is fed to one input of the differential amplifier, and the other input is fed with a reference voltage V_{REF} generated by passing a reference current I_{REF} through the series connection of diode-connected transistors Q_{10} and Q_{11}. This differential amplifier takes part in a negative- feedback loop that uses the value of v_E to control the currents i_P and i_N through the nodes v_{IP} and v_{IN}. The objective of the feedback control is to set the current in the inactive output transistor to a minimum value. To see how the feedback operates, consider the case when $i_P \gg i_N$, and thus Q_N is the inactive transistor. In this case, Q_6 turns off, Q_7 conducts all of I, and v_E is given by Eq. (12.135). Now, if for some reason i_N falls below its minimum intended value, v_E decreases,

causing i_{C9} to decrease. This in turn will cause the node v_{IN} to rise and the voltage at the base of Q_N will eventually rise, thus increasing i_N to its intended value.

Analytically, we can obtain a relationship between i_N and i_P as follows. Assume that the loop gain of the feedback loop that is anchored by the differential amplifier Q_8–Q_9 is high enough to force the two input terminals to the same voltage, that is,

$$v_E = V_{\text{REF}} = V_T \ln \frac{I_{\text{REF}}}{I_{S10}} + V_T \ln \frac{I_{\text{REF}}}{I_{S11}}$$

Substituting for v_E from Eq. (12.134) results in

$$\frac{i_N\, i_P}{i_N + i_P} = \left(\frac{I_{\text{REF}}^2}{I}\right)\left(\frac{I_{SN}}{I_{S10}}\right)\left(\frac{I_{S7}}{I_{S11}}\right) \tag{12.137}$$

Observe that the quantity on the right-hand side is a constant. In the quiescent case, $i_N = i_P = I_Q$, Eq. (12.137) yields

$$I_Q = 2\left(\frac{I_{\text{REF}}^2}{I}\right)\left(\frac{I_{SN}}{I_{S10}}\right)\left(\frac{I_{S7}}{I_{S11}}\right) \tag{12.138}$$

Thus, the constant on the right-hand side of Eq. (12.137) is $I_Q/2$, and we can rewrite (12.137) as

$$\frac{i_N\, i_P}{i_N + i_P} = \frac{1}{2} I_Q \tag{12.139}$$

Equation (12.139) clearly shows that for $i_N \gg i_P$, $i_P \simeq \frac{1}{2} I_Q$, and that for $i_P \gg i_N$, $i_N \simeq \frac{1}{2} I_Q$. Thus the circuit not only establishes the quiescent current I_Q (Eq. 12.138) but also sets the minimum current in the inactive output transistor at $\frac{1}{2} I_Q$.

EXERCISE

D12.31 For the circuit in Fig. 12.48, determine the value that I_{REF} should have so that Q_N and Q_P have a quiescent current $I_Q = 0.4$ mA. Assume that the transistor areas are scaled so that $I_{SN}/I_{S10} = 10$ and $I_{S7}/I_{S11} = 2$. Let $I = 10$ μA. Also, if i_L in the direction out of the amplifier is 10 mA, find i_P and i_N.

Ans. $I_{\text{REF}} = 10$ μA; $i_P \simeq 10.2$ mA, $i_N \simeq 0.2$ mA

Summary

- Most CMOS op amps are designed to operate as part of a VLSI circuit and thus are required to drive only small capacitive loads. Therefore, most do not have a low-output-resistance stage.
- There are basically two approaches to the design of CMOS op amps: a two-stage configuration and a single-stage topology utilizing the folded-cascode circuit.
- In the two-stage CMOS op amp, approximately equal gains are realized in the two stages.
- The threshold mismatch ΔV_t together with the low transconductance of the input stage result in a larger input offset voltage for CMOS op amps than for bipolar units.
- Miller compensation is employed in the two-stage CMOS op amp, but a series resistor is required to place the transmission zero at either $s = \infty$ or on the negative real axis.
- CMOS op amps have higher slew rates than their bipolar counterparts with comparable f_t values.
- Use of the cascode configuration increases the gain of a CMOS amplifier stage by about two orders of magnitude, thus making possible a single-stage op amp.
- The dominant pole of the folded-cascode op amp is determined by the total capacitance at the output node, C_L. Increasing C_L improves the phase margin at the expense of reducing the bandwidth.
- By using two complementary input differential pairs in parallel, the input common-mode range can be extended to equal the entire power-supply voltage, providing so-called rail-to-rail operation at the input.
- The output voltage swing of the folded-cascode op amp can be extended by utilizing a wide-swing current mirror in place of the cascode mirror.
- The internal circuit of the 741 op amp embodies many of the design techniques employed in bipolar analog integrated circuits.
- The 741 circuit consists of an input differential stage, a high-gain single-ended second stage, and a class AB output stage. Though 40 years old, this structure is typical of most BJT op amps and is known as the two-stage topology (not counting the output stage). It is also the same structure used in the two-stage CMOS op amp of Section 12.1.
- To obtain low input offset voltage and current, and high CMRR, the 741 input stage is designed to be perfectly balanced. The CMRR is increased by common-mode feedback, which also stabilizes the dc operating point.
- To obtain high input resistance and low input bias current, the input stage of the 741 is operated at a very low current level.
- In the 741, output short-circuit protection is accomplished by turning on a transistor that takes away most of the base current drive of the output transistor.
- The use of Miller frequency compensation in the 741 circuit enables locating the dominant pole at a very low frequency, while utilizing a relatively small compensating capacitance.
- Two-stage op amps can be modeled as a transconductance amplifier feeding an ideal integrator with C_C as the integrating capacitor.
- The slew rate of a two-stage op amp is determined by the first-stage bias current and the frequency-compensation capacitor.
- While the 741 and its generation of op amps nominally operate from ± 15-V power supplies, modern BJT op amps typically utilize a single ground-referenced supply of only 2 V to 3 V.
- Operation from a single low-voltage supply gives rise to a number of new important specifications including a common-mode input range that extends beyond the supply rails (i.e., more than rail-to-rail operation) and a near rail-to-rail output voltage swing.
- The rail-to-rail input common-mode range is achieved by using resistive loads (instead of current-mirror loads) for the input differential pair as well as utilizing two complementary differential amplifiers in parallel.
- To increase the gain of the input stage above that achieved with resistive loads, the folded-cascode configuration is utilized.
- To regulate the dc bias voltages at the outputs of the differential folded-cascode stage so as to maintain active-mode operation at all times, common-mode feedback is employed.
- The output stage of a low-voltage op amp utilizes a complementary pair of common-emitter transistors. This allows v_O to swing to within 0.1 V or so from each of the supply rails. The disadvantage is a high open-loop output resistance. This, however, is substantially reduced when negative feedback is applied around the op amp.
- Modern output stages operate in the class AB mode and utilize interesting feedback techniques to set the quiescent current as well as to ensure that the inactive output transistor does not turn off, a precaution that avoids increases in crossover distortion.

Computer Simulation Problems

SIM Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multism simulations for all the indicated problems can be found in the corresponding files on the CD. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

* difficult problem; ** more difficult; *** very challenging and/or time-consuming; D: design problem.

Section 12.1: The Two-Stage CMOS Op Amp

12.1 A particular design of the two-stage CMOS operational amplifier of Fig. 12.1 utilizes ±1-V power supplies. All transistors are operated at overdrive voltages of 0.15-V magnitude. The process technology provides devices with $V_{tn} = |V_{tp}| = 0.45$ V. Find the input common-mode range and the range allowed for v_O.

12.2 The CMOS op amp of Fig. 12.1 is fabricated in a process for which $V'_{An} = 25$ V/μm and $|V'_{Ap}| = 20$ V/μm. Find A_1, A_2, and A_v if all devices are 0.5-μm long and are operated at equal overdrive voltages of 0.2-V magnitude. Also, determine the op-amp output resistance obtained when the second stage is biased at 0.4 mA. What do you expect the output resistance of a unity-gain voltage amplifier to be, using this op amp?

D 12.3 The CMOS op amp of Fig. 12.1 is fabricated in a process for which $|V'_A|$ for all devices is 24 V/μm. If all transistors have $L = 0.5$ μm and are operated at equal overdrive voltages, find the magnitude of the overdrive voltage required to obtain a dc open-loop gain of 6400 V/V.

12.4 This problem is identical to Problem 8.107.

Consider the circuit in Fig. 12.1 with the device geometries shown at the bottom of this page. Let $I_{REF} = 225$ μA, $|V_t|$ for all devices = 0.75 V, $\mu_n C_{ox} = 180$ μA/V^2, $\mu_p C_{ox} = 60$ μA/V^2, $|V_A|$ for all devices = 9 V, $V_{DD} = V_{SS} = 1.5$ V. Determine the width of Q_6, W, that will ensure that the op amp will not have a systematic offset voltage. Then, for all devices, evaluate I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, and r_o. Provide your results in a table. Also find A_1, A_2, the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on the bias currents.

D 12.5 Design the two-stage CMOS op amp in Fig. 12.1 to provide a CMRR of about 80 dB. If all the transistors are operated at equal overdrive voltages of 0.15 V and have equal channel lengths, find the minimum required channel length. For this technology, $|V'_A| = 20$ V/μm.

D 12.6 A particular implementation of the CMOS amplifier of Figs. 12.1 and 12.2 provides $G_{m1} = 0.3$ mA/V, $G_{m2} = 0.6$ mA/V, $r_{o2} = r_{o4} = 222$ kΩ, $r_{o6} = r_{o7} = 111$ kΩ, and $C_2 = 1$ pF.

(a) Find the frequency of the second pole, f_{P2}.
(b) Find the value of the resistance R which when placed in series with C_C causes the transmission zero to be located at $s = \infty$.
(c) With R in place, as in (b), find the value of C_C that results in the highest possible value of f_t while providing a phase margin of 80°. What value of f_t is realized? What is the corresponding frequency of the dominant pole?
(d) To what value should C_C be changed to double the value of f_t? At the new value of f_t, what is the phase shift introduced by the second pole? To reduce this excess phase shift to 10° and thus obtain an 80° phase margin, as before, what value should R be changed to?

D 12.7 A two-stage CMOS op amp similar to that in Fig. 12.1 is found to have a capacitance between the output node and ground of 0.5 pF. If it is desired to have a unity-gain bandwidth f_t of 150 MHz with a phase margin of 75° what must g_{m6} be set to? Assume that a resistance R is connected in series with the frequency-compensation capacitor C_C and adjusted to place the transmission zero at infinity. What value should R have? If the first stage is operated at $|V_{OV}| = 0.15$ V, what is the value of slew rate obtained? If the first-stage bias current $I = 100$ μA, what is the required value of C_C?

D 12.8 A CMOS op amp with the topology shown in Fig. 12.1 is designed to provide $G_{m1} = 1$ mA/V and $G_{m2} = 5$ mA.

(a) Find the value of C_C that results in $f_t = 100$ MHz.
(b) What is the maximum value that C_2 can have while achieving a 70° phase margin?

D 12.9 A CMOS op amp with the topology shown in Fig. 12.1 but with a resistance R included in series with C_C is designed to provide $G_{m1} = 1$ mA/V and $G_{m2} = 2$ mA/V.

(a) Find the value of C_C that results in $f_t = 100$ MHz.
(b) For $R = 500$ Ω, what is the maximum allowed value of C_2 for which a phase margin of at least 60° is obtained?

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L (μm/μm)	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5

12.10 A two-stage CMOS op amp resembling that in Fig. 12.1 is found to have a slew rate of 60 V/μs and a unity-gain bandwidth f_t of 50 MHz.

(a) Estimate the value of the overdrive voltage at which the input-stage transistors are operating.
(b) If the first-stage bias current $I = 100$ μA, what value of C_C must be used?
(c) For a process for which $\mu_p C_{ox} = 50$ μA/V^2, what W/L ratio applies for Q_1 and Q_2?

D 12.11 Sketch the circuit of a two-stage CMOS amplifier having the structure of Fig. 12.1 but utilizing NMOS transistors in the input stage (i.e., Q_1 and Q_2).

D 12.12 (a) Show that the PSRR$^-$ of a CMOS two-stage op amp for which all transistors have the same channel length and are operated at equal $|V_{OV}|$ is given by

$$\text{PSRR}^- = 2\left|\frac{V_A}{V_{OV}}\right|^2$$

(b) For $|V_{OV}| = 0.2$ V, what is the minimum channel length required to obtain a PSRR$^-$ of 80 dB? For the technology available, $|V_A'| = 20$ V/μm.

Section 12.2: The Folded-Cascode Op Amp

D 12.13 If the circuit of Fig. 12.8 utilizes ±1.65-V power supplies and the power dissipation is to be limited to 1 mW, find the values of I_B and I. To avoid turning off the current mirror during slewing, select I_B to be 20% larger than I.

D 12.14 For the folded-cascode op amp in Fig. 12.9 utilizing power supplies of ±1 V, find the values of V_{BIAS1}, V_{BIAS2}, and V_{BIAS3} to maximize the allowable range of V_{ICM} and v_O. Assume that all transistors are operated at equal overdrive voltages of 0.15 V. Assume $|V_t|$ for all devices is 0.45 V. Specify the maximum range of V_{ICM} and of v_O.

D 12.15 For the folded-cascode op-amp circuit of Figs. 12.8 and 12.9 with bias currents $I = 96$ μA and $I_B = 120$ μA, and with all transistors operated at overdrive voltages of 0.2 V, find the W/L ratios for all devices. Assume that the technology available is characterized by $k_n' = 400$ μA/V^2 and $k_p' = 100$ μA/V^2.

12.16 Consider a design of the cascode op amp of Fig. 12.9 for which $I = 96$ μA and $I_B = 120$ μA. Assume that all transistors are operated at $|V_{OV}| = 0.2$ V and that for all devices, $|V_A| = 12$ V. Find G_m, R_o, and A_v. Also, if the op amp is connected in the feedback configuration shown in Fig. P12.16, find the voltage gain and output resistance of the closed-loop amplifier.

D 12.17 Consider the folded-cascode op amp of Fig. 12.8 when loaded with a 10-pF capacitance. What should the bias current I be to obtain a slew rate of at least 10 V/μs? If the input-stage transistors are operated at overdrive voltages of 0.2 V, what is the unity-gain bandwidth realized? If the two nondominant poles have the same frequency of 25 MHz, what is the phase margin obtained? If it is required to have a phase margin of 75°, what must f_t be reduced to? By what amount should C_L be increased? What is the new value of SR?

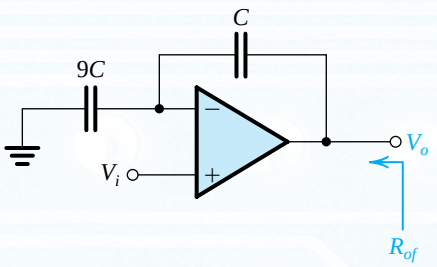


Figure P12.16

D 12.18 Design the folded-cascode circuit of Fig. 12.9 to provide voltage gain of 80 dB and a unity-gain frequency of 10 MHz when $C_L = 10$ pF. Design for $I_B = I$, and operate all devices at the same $|V_{OV}|$. Utilize transistors with 1-μm channel length for which $|V_A|$ is specified to be 20 V. Find the required overdrive voltages and bias currents. What slew rate is achieved? Also, for $k_n' = 2.5\,k_p' = 200$ μA/V^2, specify the required width of each of the 11 transistors used.

D 12.19 Sketch the circuit that is complementary to that in Fig. 12.9, that is, one that uses an input p-channel differential pair.

12.20 For the circuit in Fig. 12.11, assume that all transistors are operating at equal overdrive voltages of 0.2-V magnitude and have $|V_t| = 0.5$ V and that $V_{DD} = V_{SS} = 1.65$ V. Find (a) the range over which the NMOS input stage operates, (b) the range over which the PMOS input stage operates, (c) the range over which both operate (the overlap range), and (d) the input common-mode range.

12.21 A particular design of the wide-swing current mirror of Fig. 12.12(b) utilizes devices having $W/L = 25$, $k_n' = 200$ μA/V^2, and $V_t = 0.5$ V. For $I_{REF} = 100$ μA, what value of V_{BIAS} is needed? Also give the voltages that you expect to appear at all nodes and specify the minimum voltage allowable at the output terminal. If V_A is specified to be 10 V, what is the output resistance of the mirror?

D 12.22 For the folded-cascode circuit of Fig. 12.8, let the total capacitance to ground at each of the source nodes of Q_3 and Q_4 be denoted C_P. Assuming that the incremental resistance between the drain of Q_3 and ground is small, Show that the pole that arises at the interface between the

first and second stages has a frequency $f_P \simeq g_{m3}/2\pi C_P$. Now, if this is the only nondominant pole, what is the largest value that C_P can be (expressed as a fraction of C_L) while a phase margin of 75° is achieved? Assume that all transistors are operated at the same bias current and overdrive voltage.

Section 12.3: The 741 Op-Amp Circuit

12.23 In the 741 op-amp circuit of Fig. 12.13, Q_1, Q_2, Q_5, and Q_6 are biased at collector currents of 9.5 μA; Q_{16} is biased at a collector current of 16.2 μA; and Q_{17} is biased at a collector current of 550 μA. All these devices are of the "standard *npn*" type, having $I_S = 10^{-14}$ A, $\beta = 200$, and $V_A = 125$ V. For each of these transistors, find V_{BE}, g_m, r_e, r_π, and r_o. Provide your results in table form. (Note that these parameter values are utilized in the text in the analysis of the 741 circuit.)

D 12.24 For the (mirror) bias circuit shown in Fig. E12.11 and the result verified in the associated exercise, find I_1 for the case in which $I_{S3} = 3 \times 10^{-14}$ A, $I_{S4} = 6 \times 10^{-14}$ A, and $I_{S1} = I_{S2} = 10^{-14}$ A and for which a bias current $I_3 = 154$ μA is required.

12.25 Transistor Q_{13} in the circuit of Fig. 12.13 consists, in effect, of two transistors whose emitter–base junctions are connected in parallel and for which $I_{SA} = 0.25 \times 10^{-14}$ A, $I_{SB} = 0.75 \times 10^{-14}$ A, $\beta = 50$, and $V_A = 50$ V. For operation at a total emitter current of 0.73 mA, find values for the parameters V_{EB}, g_m, r_e, r_π, and r_o for the A and B devices.

12.26 In the circuit of Fig. 12.13, Q_1 and Q_2 exhibit emitter–base breakdown at 7 V, while for Q_3 and Q_4 such a breakdown occurs at about 50 V. What differential input voltage would result in the breakdown of the input-stage transistors?

D *12.27 Figure P12.27 shows the CMOS version of the circuit in Fig. E12.11. Find the relationship between I_3 and I_1 in terms of k_1, k_2, k_3, and k_4 of the four transistors, assuming the threshold voltages of all devices to be equal in magnitude. Note that k denotes $\mu C_{ox} W/L$. In the event that $k_1 = k_2$ and $k_3 = k_4 = 16k_1$, find the required value of I_1 to yield a bias current in Q_3 and Q_4 of 1.6 mA.

Section 12.4: DC Analysis of the 741

D 12.28 For the 741 circuit, estimate the input reference current I_{REF} in the event that ±5-V supplies are used. Find a more precise value assuming that for the two BJTs involved, $I_S = 10^{-14}$ A. What value of R_5 would be necessary to reestablish the same bias current for ±5-V supplies as exists for ±15 V in the original design?

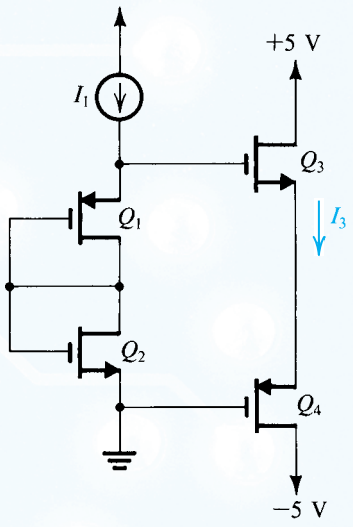


Figure P12.27

D 12.29 Design the Widlar current source of Fig. 12.14 to generate a current $I_{C10} = 10$ μA given that $I_{REF} = 0.2$ mA. If for the transistors, $I_S = 10^{-14}$ A, find V_{BE11} and V_{BE10}. Assume β to be high.

12.30 Consider the dc analysis of the 741 input stage shown in Fig. 12.15. For what value of β_P do the currents in Q_1 and Q_2 differ from the ideal value of $I_{C10}/2$ by 10%?

D 12.31 Consider the dc analysis of the 741 input stage shown in Fig. 12.15 for the situation in which $I_{S9} = 2I_{S8}$. For $I_{C10} = 19$ μA and assuming β_P to be high, what does I become? Redesign the Widlar source to reestablish $I_{C1} = I_{C2} = 9.5$ μA.

12.32 For the mirror circuit shown in Fig. 12.16 with the bias and component values given in the text for the 741 circuit, what does the current in Q_6 become if R_2 is shorted?

D 12.33 It is required to redesign the circuit of Fig. 12.16 by selecting a new value for R_3 so that when the base currents are *not* neglected, the collector currents of Q_5, Q_6, and Q_7 all become equal, assuming that the input current $I_{C3} = 9.4$ μA. Find the new value of R_3 and the three currents. Recall that $\beta_N = 200$.

12.34 Consider the input circuit of the 741 op amp of Fig. 12.13 when the emitter current of Q_8 is about 19 μA. If β of Q_1 is 150 and that of Q_2 is 200, find the input bias current I_B and the input offset current I_{OS} of the op amp.

12.35 For a particular application, consideration is being given to selecting 741 ICs for input bias and offset currents limited to 50 nA and 4 nA, respectively. Assuming other

aspects of the selected units to be normal, what minimum β_N and what β_N variation are implied?

12.36 A manufacturing problem in a 741 op amp causes the current transfer ratio of the mirror circuit that loads the input stage to become 0.8 A/A. For input devices (Q_1–Q_4) appropriately matched and with high β, and normally biased at 9.5 μA, what input offset voltage results?

D 12.37 Consider the design of the second stage of the 741. What value of R_9 would be needed to reduce I_{C16} to 9.5 μA?

D 12.38 Reconsider the 741 output stage as shown in Fig. 12.17, in which R_{10} is adjusted to make $I_{C19} = I_{C18}$. What is the new value of R_{10}? What values of I_{C14} and I_{C20} result?

D *12.39 An alternative approach to providing the voltage drop needed to bias the output transistors is the V_{BE}–multiplier circuit shown in Fig. P12.39. Design the circuit to provide a terminal voltage of 1.118 V (the same as in the 741 circuit). Base your design on half the current flowing through R_1, and assume that $I_S = 10^{-14}$ A and $\beta = 200$. What is the incremental resistance between the two terminals of the V_{BE}–multiplier circuit?

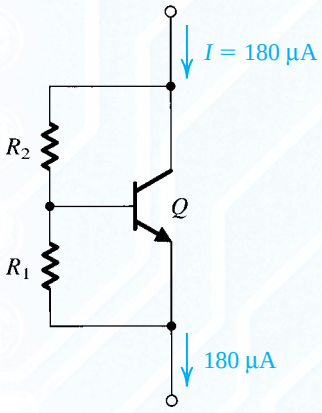


Figure P12.39

12.40 For the circuit of Fig. 12.13, what is the total current required from the power supplies when the op amp is operated in the linear mode, but with no load? Hence, estimate the quiescent power dissipation in the circuit. (*Hint:* Use the data given in Table 12.1.)

Section 12.5: Small-Signal Analysis of the 741

12.41 Consider the 741 input stage as modeled in Fig. 12.18, with two additional *npn* diode-connected transistors, Q_{1a} and Q_{2a}, connected between the present *npn* and *pnp* devices, one per side. Convince yourself that each of the additional devices will be biased at the same current as Q_1 to Q_4—that is, 9.5 μA. What does R_{id} become? What does G_{m1} become? What is the value of R_{o4} now? What is the output resistance of the first stage, R_{o1}? What is the new open-circuit voltage gain, $G_{m1}R_{o1}$? Compare these values with the original ones.

D 12.42 What relatively simple change can be made to the mirror load of stage 1 to increase its output resistance, say by a factor of 2?

12.43 Repeat Exercise 12.15 with $R_1 = R_2$ replaced by 2-kΩ resistors.

***12.44** In Example 12.3 we investigated the effect of a mismatch between R_1 and R_2 on the input offset voltage of the op amp. Conversely, R_1 and R_2 can be deliberately mismatched (using the circuit shown in Fig. P12.44, for example) to compensate for the op-amp input offset voltage.

(a) Show that an input offset voltage V_{OS} can be compensated for (i.e., reduced to zero) by creating a relative mismatch $\Delta R/R$ between R_1 and R_2,

$$\frac{\Delta R}{R} = \frac{V_{OS}}{2V_T}\frac{1 + r_e/R}{1 - V_{OS}/2V_T}$$

where r_e is the emitter resistance of each of Q_1 to Q_6, and R is the nominal value of R_1 and R_2. (*Hint:* Use Eq. 12.87)
(b) Find $\Delta R/R$ to trim a 5-mV offset to zero.
(c) What is the maximum offset voltage that can be trimmed this way (corresponding to R_2 completely shorted)?

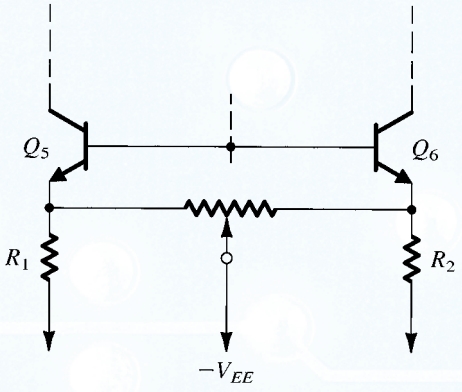


Figure P12.44

12.45 Through a processing imperfection, the β of Q_4 in Fig. 12.13 is reduced to 20, while the β of Q_3 remains at its regular value of 50. Find the input offset voltage that this mismatch introduces. (*Hint:* Follow the general procedure outlined in Example 12.3.)

12.46 Consider the circuit of Fig. 12.13 modified to include resistors R in series with the emitters of each of Q_8 and Q_9. What does the resistance looking into the collector of Q_9, R_{o9}, become? For what value of R does it equal R_{o10}? For this case, what does R_o looking to the left of node Y become?

***12.47** What is the effect on the differential gain of the 741 op amp of short-circuiting one, or the other, or both, of R_1 and R_2 in Fig. 12.13? (Refer to Fig. 12.19.) For simplicity, assume $\beta = \infty$.

12.48 It is required to show that the loop gain of the common-mode feedback loop shown in Fig. 12.23 is approximately equal to β_P. To determine the loop gain, connect both input terminals to ground. Break the loop at the input to the Q_8–Q_9 current mirror, connecting the Q_1–Q_2 collectors to signal ground. (This is because the original resistance between the collectors and ground is r_{e8}, which is small.) Apply a test current I_t to Q_8 and determine the returned current I_r in the common collectors' connection to ground, then find the loop gain as $-I_r/I_t$. Assume that r_π of Q_1 to Q_4 is much lower than R_o and that β_N, $\beta_P \gg 1$.

12.49 An alternative approach to that presented in Example 12.4 for determining the CMRR of the 741 input stage is investigated in this problem. Rather than performing the analysis on the closed loop shown in Fig. 12.23, we observe that the negative feedback increases the resistance at node Y by the amount of negative feedback. Thus, we can break the loop at Y and connect a resistance $R_f = (1 + A\beta)R_o$ between the common base connection of Q_3–Q_4 and ground. We can then determine the current i and G_{mcm}. Using the fact that the loop gain is approximately equal to β_P (Problem 12.48) show that this approach yields an identical result to that found in Example 12.4.

12.50 Consider a variation on the design of the 741 second stage in which $R_8 = 50\ \Omega$. What R_{i2} and G_{m2} correspond?

12.51 In the analysis of the 741 second stage, note that R_{o2} is affected most strongly by the low value of R_{o13B}. Consider the effect of placing appropriate resistors in the emitters of Q_{12}, Q_{13A}, and Q_{13B} on this value. What resistor in the emitter of Q_{13B} would be required to make R_{o13B} equal to R_{o17} and thus R_{o2} half as great? What resistors in each of the other emitters would be required?

12.52 For a 741 employing ±5-V supplies, $|V_{BE}| = 0.6$ V and $|V_{CE\,sat}| = 0.2$ V, find the output voltage limits that apply.

D 12.53 Consider an alternative to the present 741 output stage in which Q_{23} is not used, that is, in which its base and emitter are joined. Reevaluate the reflection of $R_L = 2$ kΩ to the collector of Q_{17}. What does A_2 become?

12.54 Consider the positive current-limiting circuit involving Q_{13A}, Q_{15}, and R_6. Find the current in R_6 at which the collector current of Q_{15} equals the current available from Q_{13A} (180 μA) minus the base current of Q_{14}. (You need to perform a couple of iterations.)

D 12.55 Consider the 741 sinking-current limit involving R_7, Q_{21}, Q_{24}, R_{11}, and Q_{22}. For what current through R_7 is the current in Q_{22} equal to the maximum current available from the input stage (i.e., the current in Q_8)? What simple change would you make to reduce this current limit to 10 mA?

Section 12.6: Gain, Frequency Response, and Slew Rate of the 741

12.56 Using the data provided in Eq. (12.112) (alone) for the overall gain of the 741 with a 2-kΩ load, and realizing the significance of the factor 0.97 in relation to the load, calculate the open-circuit voltage gain, the output resistance, and the gain with a load of 200 Ω.

12.57 A 741 op amp has a phase margin of 75°. If the excess phase shift is due to a second single pole, what is the frequency of this pole?

12.58 A 741 op amp has a phase margin of 75°. If the op amp has nearly coincident second and third poles, what is their frequency?

D *12.59 For a modified 741 whose second pole is at 5 MHz, what dominant-pole frequency is required for 80° phase margin with a closed-loop gain of 100? Assuming C_C continues to control the dominant pole, what value of C_C would be required?

12.60 An internally compensated op amp having an f_t of 10 MHz and dc gain of 10^6 utilizes Miller compensation around an inverting amplifier stage with a gain of –1000. If space exists for at most a 50-pF capacitor, what resistance level must be reached at the input of the Miller amplifier for compensation to be possible?

12.61 Consider the integrator op-amp model shown in Fig. 12.33. For $G_{m1} = 5$ mA/V, $C_C = 100$ pF, and a resistance of 2×10^7 Ω shunting C_C, sketch and label a Bode plot for the magnitude of the open-loop gain. If G_{m1} is related to the first-stage bias current as $G_{m1} = I/2V_T$, find the slew rate of this op amp.

12.62 For an amplifier with a slew rate of 10 V/μs, what is the full-power bandwidth for outputs of ±10 V? What unity-gain bandwidth, ω_t, would you expect if the topology was similar to that of the 741?

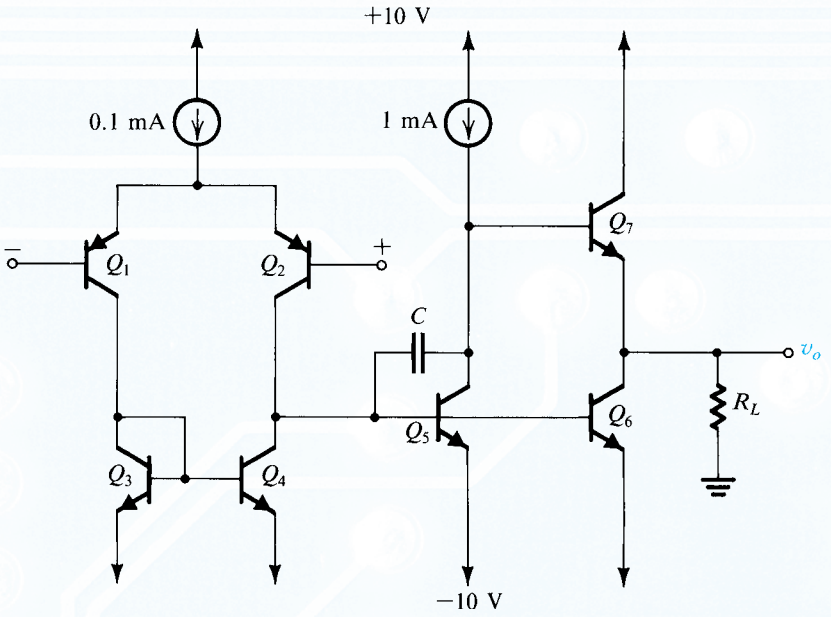


Figure P12.63

D ***12.63** Figure P12.63 shows a circuit suitable for op-amp applications. For all transistors $\beta = 100$, $V_{BE} = 0.7$ V, and $r_o = \infty$.

(a) For inputs grounded and output held at 0 V (by negative feedback) find the collector currents of all transistors. Neglect base currents.
(b) Calculate the input resistance.
(c) Calculate the gain of the amplifier with a load of 5 kΩ.
(d) With load as in (c) calculate the value of the capacitor C required for a 3-dB frequency of 100 Hz.

Section 12.7: Modern Techniques for the Design of BJT Op Amps

Unless otherwise specified, for the problems in this section assume $\beta_N = 40$, $\beta_P = 10$, $V_{An} = 30$ V, $|V_{Ap}| = 20$ V, $|V_{BE}| = 0.7$ V, $|V_{CEsat}| = 0.1$ V.

D **12.64** Design the circuit in Fig. 12.38 to generate a current $I = 6$ μA. Utilize transistors Q_1 and Q_2 having areas in a ratio of 1:4. Assume that Q_3 and Q_4 are matched and design for a 0.2-V drop across each of R_3 and R_4. Specify the values of R_2, R_3, and R_4. Ignore base currents.

D **12.65** Consider the circuit of Fig. 12.38 for the case designed in Exercise 12.28, namely, $I = 10$ μA, $I_{S2}/I_{S1} = 2$, $R_2 = 1.73$ kΩ, $R_3 = R_4 = 20$ kΩ. Augment the circuit with *npn* transistors Q_5 and Q_6 with emitters connected to ground and bases connected to V_{BIAS1}, to generate constant currents of 10 μA and 40 μA, respectively. What should the emitter areas of Q_5 and Q_6 be relative to that of Q_1? What value of a resistance R_6 will, when connected in the emitter of Q_6, reduce the current generated by Q_6 to 10 μA? Assuming that the V_{BIAS1} line has a low incremental resistance to ground, find the output resistance of current source Q_5 and of current source Q_6 with R_6 connected. Ignore base currents.

D **12.66** (a) Find the input common-mode range of the circuit in Fig. 12.40(a). Let $V_{CC} = 3$ V and $V_{BIAS} = 2.3$ V.

(b) Give the complementary version of the circuit in Fig. 12.40(a), that is, the one in which the differential pair is *npn*. For the same conditions as in (a), what is the input common-mode range?

12.67 For the circuit in Fig. 12.40(b), let $V_{CC} = 3$ V, $V_{BIAS} = 2.3$ V, $I = 20$ μA, and $R_C = 20$ kΩ. Find the input common-mode range and the differential voltage gain v_o/v_{id}. Neglect base currents.

12.68 For the circuit in Fig. 12.41, let $V_{CC} = 3$ V, $V_{BIAS} = 0.7$ V, and $I_{C6} = 10$ μA. Find R_C that results in a differential gain of 10 V/V. What is the input common-mode range and the input differential resistance? Ignore base currents except when calculating R_{id}.

12.69 It is required to find the input resistance and the voltage gain of the input stage shown in Fig. 12.42. Let $V_{ICM} \ll 0.8$ V so that the Q_3–Q_4 pair is off. Assume that

Q_5 supplies 6 μA, that each of Q_7 to Q_{10} is biased at 6 μA, and that all four cascode transistors are operating in the active mode. The input resistance of the second stage of the op amp is 1.3 MΩ. The emitter degeneration resistances are $R_7 = R_8 = 22$ kΩ, and $R_9 = R_{10} = 33$ kΩ. [*Hint*: Refer to Fig. 12.43.]

D 12.70 Consider the equivalent half-circuit shown in Fig. 12.43. Assume that in the original circuit, Q_1 is biased at a current I, Q_7 and Q_9 are biased at $2I$, the dc voltage drop across R_7 is 0.2 V, and the dc voltage drop across R_9 is 0.3 V. Find the open-circuit voltage gain (i.e., the voltage gain for $R_L = \infty$). Also find the output resistance in terms of I. Now with R_L connected, find the voltage gain in terms of (IR_L). For $R_L = 2$ MΩ, find I that will result in the voltage gains of 160 V/V and 320 V/V.

***12.71** (a) For the circuit in Fig. 12.44, show that the loop gain of the common-mode feedback loop is

$$A\beta \simeq \frac{R_{o9} \parallel R_{o7}}{r_{e7} + R_7}$$

Recall that the CMF circuit realizes the transfer characteristic $V_B = V_{CM} + 0.4$. Ignore the loading effect of the CMF circuit on the collectors of the cascode transistors.
(b) For the values in Example 12.6, calculate the loop gain $A\beta$.
(c) In Example 12.6, we found that with the CMF absent, a current mismatch $\Delta I = 0.3$ μA gives rise to $\Delta V_{CM} = 2.5$ V. Now, with the CMF present, use the value of loop gain found in (b) to calculate the expected ΔV_{CM} and compare to the value found by a different approach in Example 12.6. [*Hint*: Recall that negative feedback reduces change by a factor equal to $(1 + A\beta)$.]

12.72 The output stage in Fig. 12.46 operates at a quiescent current I_Q of 0.4 mA. The maximum current i_L that the stage can provide in either direction is 10 mA. Also, the output stage is equipped with a feedback circuit that maintains a minimum current of $I_Q/2$ in the inactive output transistor.

(a) What is the allowable range of v_O?
(b) For $i_L = 0$, what is the output resistance of the op amp?
(c) If the open-loop gain of the op amp is 100,000 V/V, find the closed-loop output resistance obtained when the op amp is connected in the unity-gain voltage follower configuration, with $i_L = 0$.
(d) If the op amp is sourcing a load current $i_L = 10$ mA, find i_P, i_N, and the open-loop output resistance.
(e) Repeat (d) for the case of the open-loop op amp sinking a load current of 10 mA.

12.73 It is required to derive the expressions in Eqs. (12.132) and (12.133). Toward that end, first find v_{B7} in terms of v_{BEN} and hence i_N. Then find v_{B6} in terms of i_P. For the latter purpose note that Q_4 measures v_{EBP} and develops a current $i_4 = (v_{EBP} - v_{EB4})/R_4$. This current is supplied to the series connection of Q_5 and R_5 where $R_5 = R_4$. In the expression you obtain for v_{B6}, use the relationship

$$\frac{I_{SP}}{I_{S4}} = \frac{I_{SN}}{I_{S5}}$$

to express v_{B6} in terms of i_P and I_{SN}. Now with v_{B6} and v_{B7} determined, find i_{C6} and i_{C7}.

12.74 It is required to derive the expression for v_E in Eq. (12.134). Toward that end, note from the circuit in Fig. 12.48 that $v_E = v_{EB7} + v_{BEN}$ and note that Q_N conducts a current i_N and Q_7 conducts a current i_{C7} given by Eq. (12.133).

D 12.75 For the output stage in Fig. 12.48, find the current I_{REF} that results in a quiescent current $I_Q = 0.36$ mA. Assume that $I = 10$ μA, Q_N has eight times the area of Q_{10}, and Q_7 has four times the area of Q_{11}. What is the minimum current in Q_N and Q_P?