14.4 CHARACTERISTICS OF STANDARD TTL

Because of its historical popularity and continued importance, TTL will be studied further in this and the next sections. In this section we shall consider some of the important characteristics of standard TTL gates. Special improved forms of TTL will be dealt with in Section 14.5.

Transfer Characteristic

Figure 14.23 shows the TTL gate together with a sketch of its voltage transfer characteristic drawn in a piecewise-linear fashion. The actual characteristic is, of course, a smooth curve. We shall now explain the transfer characteristic and calculate the various break-points and slopes. It will be assumed that the output terminal of the gate is open.

Segment *AB* is obtained when transistor Q_1 is saturated, Q_2 and Q_3 are off, and Q_4 and D are on. The output voltage is approximately two diode drops below V_{CC}. At point *B* the phase splitter (Q_2) begins to turn on because the voltage at its base reaches 0.6 V (0.5 V + V_{CEsat} of Q_1).

Over segment *BC*, transistor Q_1 remains saturated, but more and more of its base current *I* gets diverted to its base–collector junction and into the base of Q_2, which operates as a linear amplifier. Transistor Q_4 and diode D remain on, with Q_4 acting as an emitter follower. Meanwhile the voltage at the base of Q_3, although increasing, remains insufficient to turn Q_3 on (less than 0.6 V).

Let us now find the slope of segment *BC* of the transfer characteristic. Let the input v_I increase by an increment Δv_I. This increment appears at the collector of Q_1, since the saturated Q_1 behaves (approximately) as a three-terminal short circuit as far as signals are

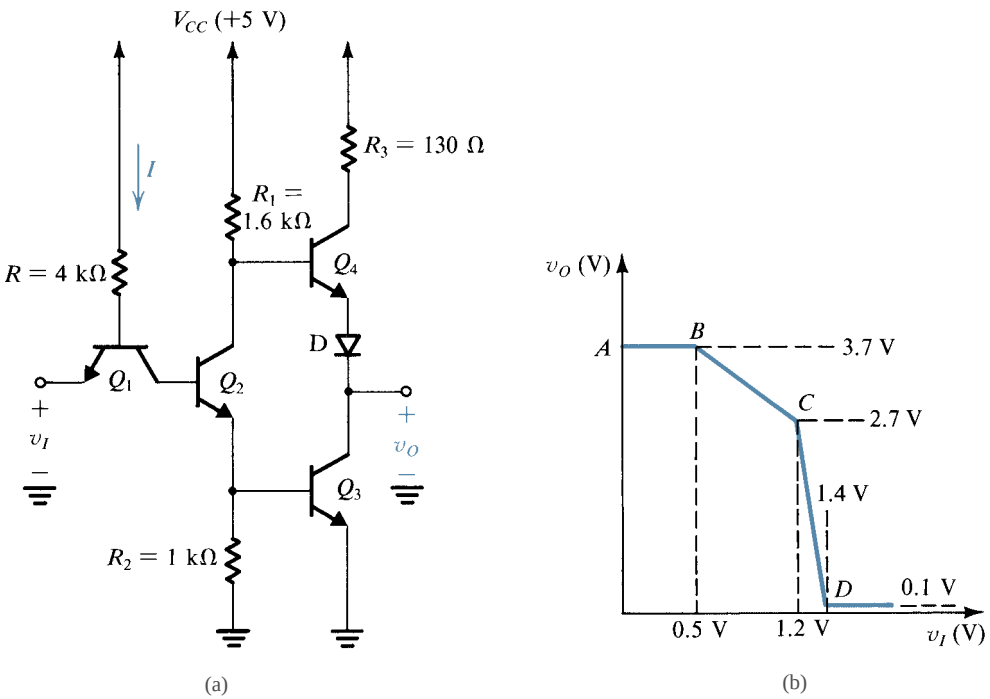

FIGURE 14.23 The TTL gate and its voltage transfer characteristic.

concerned. Thus at the base of Q_2 we have a signal Δv_I. Neglecting the loading of emitter follower Q_4 on the collector of Q_2, we can find the gain of the phase splitter from

$$\frac{v_{c2}}{v_{b2}} = \frac{-\alpha_2 R_1}{r_{e2} + R_2} \tag{14.6}$$

The value of r_{e2} will obviously depend on the current in Q_2. This current will range from zero (as Q_2 begins to turn on) to the value that results in a voltage of about 0.6 V at the emitter of Q_2 (the base of Q_3). This value is about 0.6 mA and corresponds to point C on the transfer characteristic. Assuming an average current in Q_2 of 0.3 mA, we obtain $r_{e2} \simeq 83\ \Omega$. For $\alpha = 0.98$, Eq. (14.6) results in a gain value of 1.45. Since the gain of the output follower Q_4 is close to unity, the overall gain of the gate, which is the slope of the BC segment, is about –1.45.

As already implied, breakpoint C is determined by Q_3 starting to conduct. The corresponding input voltage can be found from

$$\begin{aligned} v_I(C) &= V_{BE3} + V_{BE2} - V_{CE\text{sat}}(Q_1) \\ &= 0.6 + 0.7 - 0.1 = 1.2\ \text{V} \end{aligned}$$

At this point the emitter current of Q_2 is approximately 0.6 mA. The collector current of Q_2 is also approximately 0.6 mA; neglecting the base current of Q_4, the voltage at the collector of Q_2 is

$$v_{C2}(C) = 5 - 0.6 \times 1.6 \cong 4\ \text{V}$$

Thus Q_2 is still in the active mode. The corresponding output voltage is

$$v_O(C) = 4 - 0.65 - 0.65 = 2.7\ \text{V}$$

As v_I is increased past the value of $v_I(C) = 1.2$ V, Q_3 begins to conduct and operates in the active mode. Meanwhile, Q_1 remains saturated, and Q_2 and Q_4 remain in the active mode. The circuit behaves as an amplifier until Q_2 and Q_3 saturate and Q_4 cuts off. This occurs at point D on the transfer characteristic, which corresponds to an input voltage $v_I(D)$ obtained from

$$\begin{aligned} v_I(D) &= V_{BE3} + V_{BE2} + V_{BC1} - V_{BE1} \\ &= 0.7 + 0.7 + 0.7 - 0.7 = 1.4\ \text{V} \end{aligned}$$

Note that we have in effect assumed that at point D transistor Q_1 is still saturated, but with $V_{CE\text{sat}} \simeq 0$. To see how this comes about, note that from point B on, more and more of the base current of Q_1 is diverted to its base–collector junction. Thus while the drop across the base–collector junction increases, that across the base–emitter junction decreases. At point D these drops become almost equal. For $v_I > v_I(D)$ the base–emitter junction of Q_1 cuts off; thus Q_1 leaves saturation and enters the inverse active mode.

Calculation of gain over the segment CD is a relatively complicated task. This is due to the fact that there are two paths from input to output: one through Q_3 and one through Q_4. A simple but gross approximation for the gain of this segment can be obtained from the coordinates of points C and D in Fig. 14.23(b), as follows:

$$\begin{aligned} \text{Gain} &= -\frac{v_O(C) - v_O(D)}{v_I(D) - v_I(C)} \\ &= -\frac{2.7 - 0.1}{1.4 - 1.2} = -13\ \text{V/V} \end{aligned}$$

From the transfer curve of Fig. 14.23(b) we can determine the critical points and the noise margins as follows: $V_{OH} = 3.7$ V; V_{IL} is somewhere in the range of 0.5 V to 1.2 V, and thus a conservative estimate would be 0.5 V; $V_{OL} = 0.1$ V; $V_{IH} = 1.4$ V; $NM_H = V_{OH} - V_{IH} = 2.3$ V; and $NM_L = V_{IL} - V_{OL} = 0.4$ V. It should be noted that these values are computed assuming that the gate is not loaded and without taking into account power-supply or temperature variations.

EXERCISE

14.11 Taking into account the fact that the voltage across a forward-biased *pn* junction changes by about −2 mV/°C, find the coordinates of points *A*, *B*, *C*, and *D* of the gate transfer characteristic at −55°C and at +125°C. Assume that the characteristic in Fig. 14.23(b) applies at 25°C, and neglect the small temperature coefficient of V_{CEsat}.

Ans. At −55°C: (0, 3.38), (0.66, 3.38), (1.52, 2.16), (1.72, 0.1); at +125°C: (0, 4.1), (0.3, 4.1), (0.8, 3.46), (1.0, 0.1)

Manufacturers' Specifications

Manufacturers of TTL usually provide curves for the gate transfer characteristic, the input *i*–*v* characteristic, and the output *i*–*v* characteristic, measured at the limits of the specified operating temperature range. In addition, guaranteed values are usually given for the parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH}. For standard TTL (known as the 74 series) these values are $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V, $V_{IL} = 0.8$ V, and $V_{IH} = 2$ V. These limit values are guaranteed for a specified tolerance in power-supply voltage and for a maximum fan-out of 10. From our discussion in Section 14.3 we know that the maximum fan-out is determined by the maximum current that Q_3 can sink while remaining in saturation and while maintaining a saturation voltage lower than a guaranteed maximum ($V_{OL} = 0.4$ V). Calculations performed in Section 14.3 indicate the possibility of a maximum fan-out of 20 to 30. Thus the figure specified by the manufacturer is appropriately conservative.

The parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH} can be used to compute the noise margins as follows:

$$NM_H = V_{OH} - V_{IH} = 0.4 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.4 \text{ V}$$

EXERCISES

14.12 In Section 14.3 we found that when the gate input is high, the base current of Q_3 is approximately 2.6 mA. Assume that this value applies at 25°C and that at this temperature $V_{BE} \simeq 0.7$ V. Taking into account the −2-mV/°C temperature coefficient of V_{BE} and neglecting all other changes, find the base current of Q_3 at −55°C and at +125°C.

Ans. 2.2 mA; 3 mA

14.13 Figure E14.13 shows sketches of the i_L–v_O characteristics of a TTL gate when the output is low. Use these characteristics together with the results of Exercise 14.12 to calculate the value of β of transistor Q_3 at –55°C, +25°C, and +125°C.

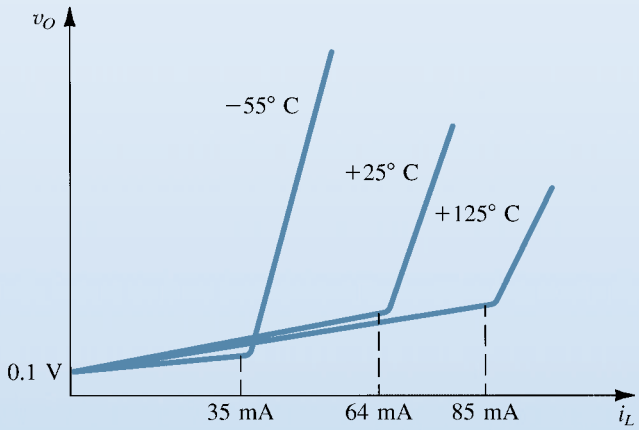

FIGURE E14.13

Ans. 16; 25; 28

Propagation Delay

The propagation delay of TTL gates is defined conventionally as the time between the 1.5-V points of corresponding edges of the input and output waveforms. For standard TTL (also known as *medium-speed* TTL) t_P is typically about 10 ns.

As far as power dissipation is concerned it can be shown (see Exercise 14.14) that when the gate output is high the gate dissipates 5 mW, and when the output is low the dissipation is 16.7 mW. Thus the average dissipation is 11 mW, resulting in a delay-power product of about 100 pJ.

EXERCISE

14.14 Calculate the value of the supply current (I_{CC}), and hence the power dissipated in the TTL gate, when the output terminal is open and the input is (a) low at 0.2 V (see Fig. 14.22) and (b) high at +5 V (see Fig. 14.20).

Ans. (a) 1 mA, 5 mW; (b) 3.33 mA, 16.7 mW

Dynamic Power Dissipation

In Section 14.3 the occurrence of supply current spikes was explained. These spikes give rise to additional power drain from the V_{CC} supply. This **dynamic power** is also dissipated in the gate circuit. It can be evaluated by multiplying the average current due to the spikes by V_{CC}, as illustrated by the solution of Exercise 14.15.

EXERCISE

14.15 Consider a TTL gate that is switched on and off at the rate of 1 MHz. Assume that each time the gate is turned off (that is, the output goes high) a supply-current pulse of 30-mA amplitude and 2-ns width occurs. Also assume that no current spike occurs when the gate is turned on. Calculate the average supply current due to the spikes, and the dynamic power dissipation.

Ans. 60 μA; 0.3 mW

The TTL NAND Gate

Figure 14.24 shows the basic TTL gate. Its most important feature is the **multiemitter transistor** Q_1 used at the input. Figure 14.25 shows the structure of the multiemitter transistor.

It can be easily verified that the gate of Fig. 14.24 performs the NAND function. The output will be high if one (or both) of the inputs is (are) low. The output will be low in only

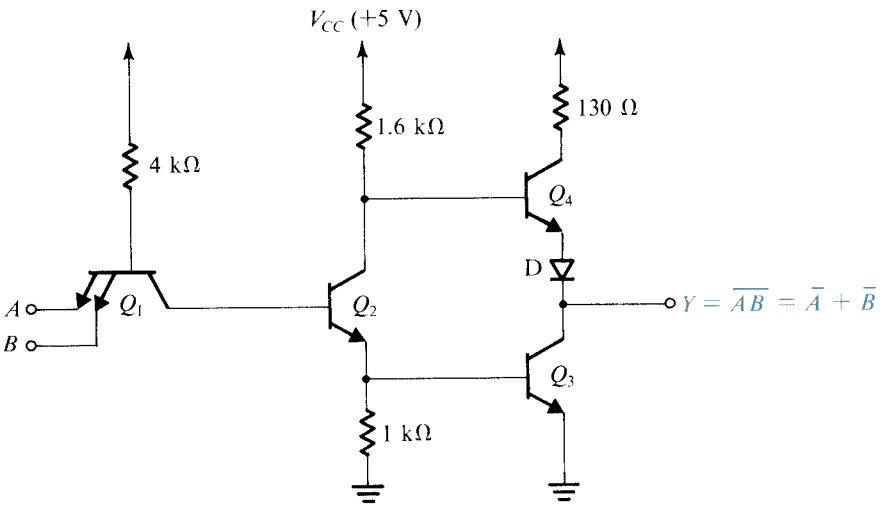

FIGURE 14.24 The TTL NAND gate.

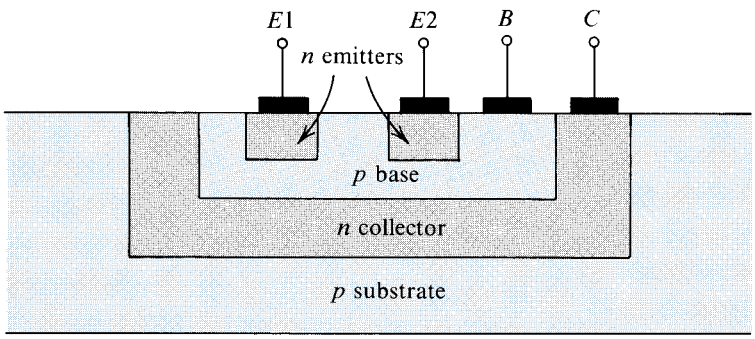

FIGURE 14.25 Structure of the multiemitter transistor Q_1.

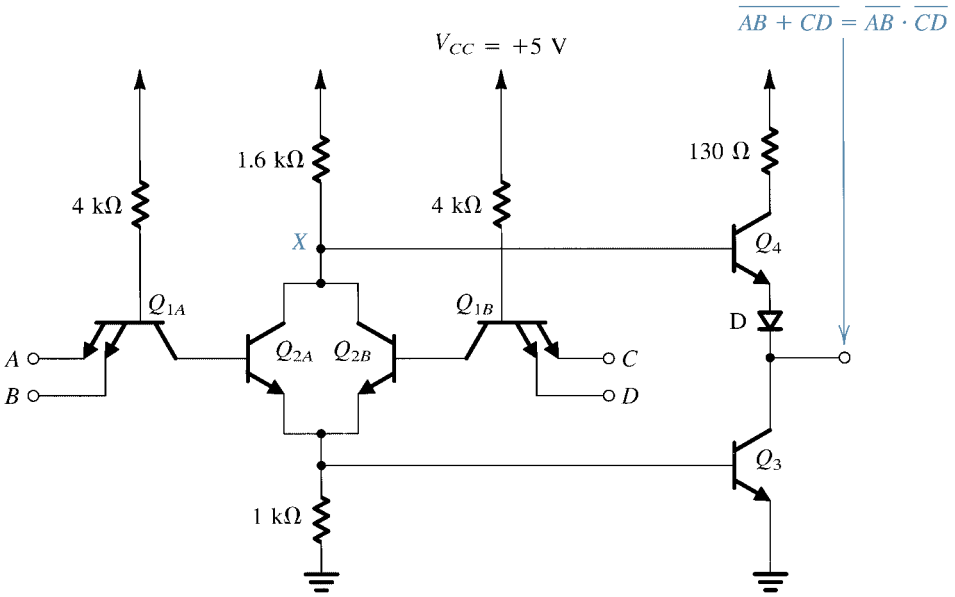

FIGURE 14.26 A TTL AND-OR-INVERT gate.

one case: when both inputs are high. Extension to more than two inputs is straightforward and is achieved by diffusing additional emitter regions.

Although theoretically an unused input terminal may be left open-circuited, this is generally not a good practice. An open-circuit input terminal acts as an "antenna" that "picks up" interfering signals and thus could cause erroneous gate switching. An unused input terminal should therefore be connected to the positive power supply *through a resistance* (of, say, 1 kΩ). In this way the corresponding base–emitter junction of Q_1 will be reverse-biased and thus will have no effect on the operation of the gate. The series resistance is included in order to limit the current in case of breakdown of the base–emitter junction due to transients on the power supply.

Other TTL Logic Circuits

On a TTL MSI chip there are many cases in which logic functions are implemented using "stripped-down" versions of the basic TTL gate. As an example we show in Fig. 14.26 the TTL implementation of the AND-OR-INVERT function. As shown, the phase-splitter transistors of two gates are connected in parallel, and a single output stage is used. The reader is urged to verify that the logic function realized is as indicated.

At this point it should be noted that the totem-pole output stage of TTL does *not* allow connecting the output terminals of two gates to realize the AND function of their outputs (known as the wired-AND connection). To see the reason for this, consider two gates whose outputs are connected together, and let one gate have a high output and the other have a low output. Current will flow from Q_4 of the first gate through Q_3 of the second gate. The current value will fortunately be limited by the 130-Ω resistance. Obviously, however, no useful logic function is realized by this connection.

The lack of wired-AND capability is a drawback of TTL. Nevertheless, the problem is solved in a number of ways, including doing the paralleling at the phase-splitter stage, as illustrated in Fig. 14.26. Another solution consists of deleting the emitter-follower transistor

altogether. The result is an output stage consisting solely of the common-emitter transistor Q_3 without even a collector resistance. Obviously, one can connect the outputs of such gates together to a common collector resistance and achieve a wired-AND capability. TTL gates of this type are known as **open-collector TTL.** The obvious disadvantage is the slow rise time of the output waveform.

Another useful variant of TTL is the **tristate** output arrangement explored in Exercise 14.16.

EXERCISE

14.16 The circuit shown in Fig. E14.16 is called tristate TTL. Verify that when the terminal labeled $\overline{\text{Third state}}$ is high, the gate functions normally and that when this terminal is low, both transistors Q_3 and Q_4 cut off and the output of the gate is an open circuit. The latter state is the third state, or the high-output-impedance state.

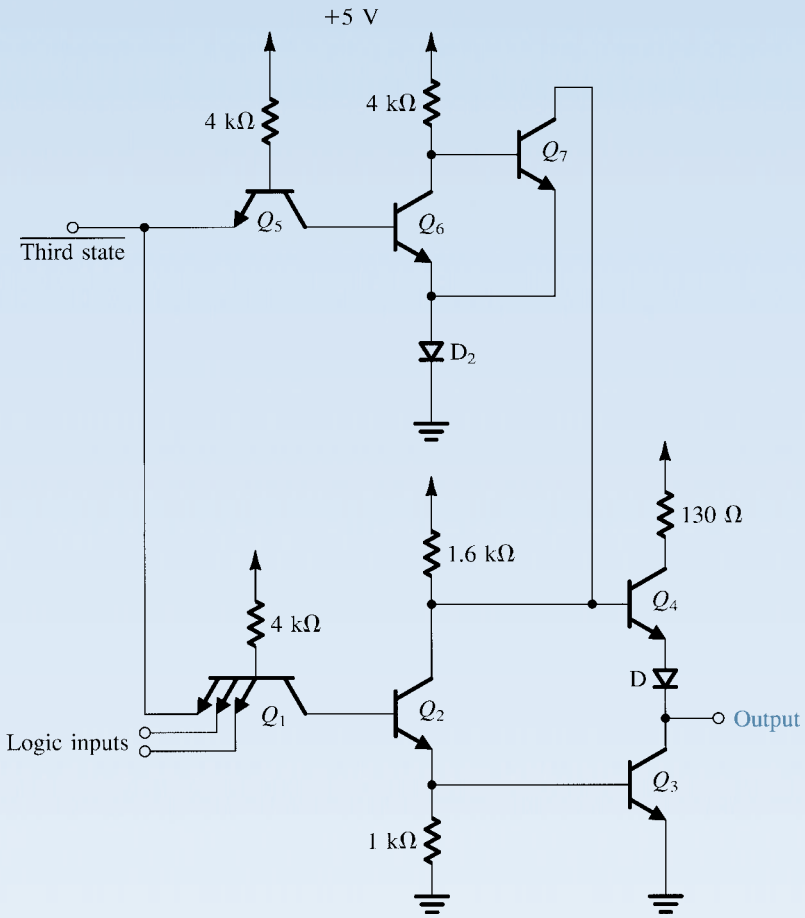

FIGURE E14.16

Tristate TTL enables the connection of a number of TTL gates to a common output line (or *bus*). At any particular time the signal on the bus will be determined by the one TTL gate