CHAPTER 17

# Signal Generators and Waveform-Shaping Circuits

IN THIS CHAPTER YOU WILL LEARN

1. That an oscillator circuit that generates sine waves can be implemented by connecting a frequency-selective network in the positive-feedback path of an amplifier.
2. The conditions under which sustained oscillations are obtained and the frequency of the oscillations.
3. How to design nonlinear circuits to control the amplitude of the sine wave obtained in a linear oscillator.
4. A variety of circuits for implementing a linear sine-wave oscillator.
5. How op amps can be combined with resistors and capacitors to implement precision multivibrator circuits.
6. How a bistable circuit can be connected in a feedback loop with an op-amp integrator to implement a generator of square and triangular waveforms.
7. The application of one of the most popular IC chips of all time, the 555 timer, in the design of generators of pulse and square waveforms.
8. How a triangular waveform can be shaped by a nonlinear circuit to provide a sine waveform.
9. How op amps and diodes can be combined to implement a variety of high-precision rectifier circuits.

## Introduction

In the design of electronic systems, the need frequently arises for signals having prescribed standard waveforms, for example, sinusoidal, square, triangular, or pulse. Systems in which standard signals are required include computer and control systems where clock pulses are needed for, among other things, timing; communication systems where signals of a variety of waveforms are utilized as information carriers; and test and measurement systems where signals, again of a variety of waveforms, are employed for testing and characterizing electronic devices and circuits. In this chapter we study signal-generator circuits.

There are two distinctly different approaches for the generation of sinusoids, perhaps the most commonly used of the standard waveforms. The first approach, studied in Sections 17.1 to 17.3, employs a **positive-feedback loop** consisting of an amplifier and an RC or LC **frequency-selective network**. The amplitude of the generated sine waves is limited, or set, using a nonlinear mechanism, implemented either with a separate circuit or using the nonlinearities of the amplifying device itself. In spite of this, these circuits, which generate sine waves utilizing resonance phenomena, are known as **linear oscillators**. The name clearly distinguishes them from the circuits that generate sinusoids by way of the second approach. In these circuits, a sine wave is obtained by appropriately shaping a triangular waveform. We study waveform-shaping circuits in Section 17.8, following the study of triangular-waveform generators.

Circuits that generate square, triangular, pulse (etc.) waveforms, called **nonlinear oscillators** or **function generators**, employ circuit building blocks known as **multivibrators**. There are three types of multivibrator: the **bistable** (Section 17.4), the **astable** (Section 17.5), and the **monostable** (Section 17.6). The multivibrator circuits presented in this chapter employ op amps and are intended for precision analog applications. Bistable and monostable multivibrator circuits using digital logic gates were studied in Chapter 15.

A general and versatile scheme for the generation of square and triangular waveforms is obtained by connecting a bistable multivibrator and an op-amp integrator in a feedback loop (Section 17.5). Similar results can be obtained using a commercially available versatile IC chip, the 555 timer (Section 17.7). The chapter includes also a study of precision circuits that implement the rectifier functions introduced in Chapter 4. The circuits studied here (Section 17.9), however, are intended for applications that demand precision, such as in instrumentation systems, including waveform generation.

## 17.1 Basic Principles of Sinusoidal Oscillators

In this section, we study the basic principles of the design of linear sine-wave oscillators. In spite of the name *linear oscillator,* some form of nonlinearity has to be employed to provide control of the amplitude of the output sine wave. In fact, all oscillators are essentially nonlinear circuits. This complicates the task of analysis and design of oscillators: No longer is one able to apply transform ($s$-plane) methods directly. Nevertheless, techniques have been developed by which the design of sinusoidal oscillators can be performed in two steps: The first step is a linear one, and frequency-domain methods of feedback circuit analysis can be readily employed. Subsequently, a nonlinear mechanism for amplitude control can be provided.

### 17.1.1 The Oscillator Feedback Loop

The basic structure of a sinusoidal oscillator consists of an amplifier and a frequency-selective network connected in a positive-feedback loop, such as that shown in block diagram form in Fig. 17.1. Although no input signal will be present in an actual oscillator circuit, we include an input signal here to help explain the principle of operation. It is important to note that unlike the negative-feedback loop of Fig. 10.1, here the feedback signal $x_f$ is summed with a *positive* sign. Thus the gain-with-feedback is given by

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)} \tag{17.1}$$

where we note the negative sign in the denominator.

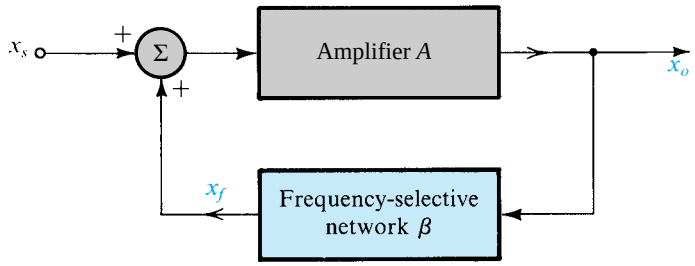



**Figure 17.1** The basic structure of a sinusoidal oscillator. A positive-feedback loop is formed by an amplifier and a frequency-selective network. In an actual oscillator circuit, no input signal will be present; here an input signal $x_s$ is employed to help explain the principle of operation.

According to the definition of loop gain in Chapter 10, the loop gain of the circuit in Fig. 17.1 is $-A(s)\beta(s)$. However, for our purposes here it is more convenient to drop the minus sign and define the loop gain $L(s)$ as

$$L(s) \equiv A(s)\beta(s) \tag{17.2}$$

The characteristic equation thus becomes

$$1 - L(s) = 0 \tag{17.3}$$

Note that this new definition of loop gain[1] corresponds directly to the actual gain seen around the feedback loop of Fig. 17.1.

## 17.1.2 The Oscillation Criterion

If at a specific frequency $f_0$ the loop gain $A\beta$ is equal to unity, it follows from Eq. (17.1) that $A_f$ will be infinite. That is, at this frequency the circuit will have a finite output for zero input signal. Such a circuit is by definition an oscillator. Thus the condition for the feedback loop of Fig. 17.1 to provide sinusoidal oscillations of frequency $\omega_0$ is

$$L(j\omega_0) \equiv A(j\omega_0)\beta(j\omega_0) = 1 \tag{17.4}$$

That is, *at $\omega_0$ the phase of the loop gain should be zero and the magnitude of the loop gain should be unity.* This is known as the **Barkhausen criterion**. Note that for the circuit to oscillate at one frequency, the oscillation criterion should be satisfied only at one frequency (i.e., $\omega_0$); otherwise the resulting waveform will not be a simple sinusoid.

An intuitive feeling for the Barkhausen criterion can be gained by considering once more the feedback loop of Fig. 17.1. For this loop to *produce* and *sustain* an output $x_o$ with no input applied ($x_s = 0$), the feedback signal $x_f$

$$x_f = \beta x_o$$

should be sufficiently large that when multiplied by $A$ it produces $x_o$, that is,

$$Ax_f = x_o$$

[1] For both the negative-feedback loop in Fig. 10.1 and the positive-feedback loop in Fig. 17.1, the loop gain $L = A\beta$. However, the negative sign with which the feedback signal is summed in the negative-feedback loop results in the characteristic equation being $1 + L = 0$. In the positive-feedback loop, the feedback signal is summed with a positive sign, thus resulting in the characteristic equation $1 - L = 0$.

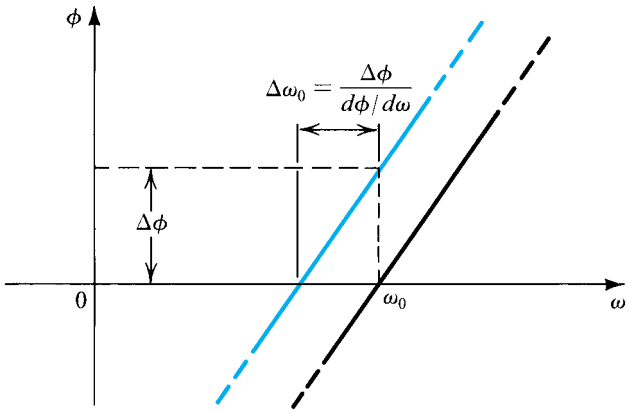



**Figure 17.2** Dependence of the oscillator-frequency stability on the slope of the phase response. A steep phase response (i.e., large $d\phi/d\omega$) results in a small $\Delta\omega_0$ for a given change in phase $\Delta\phi$ [resulting from a change (due, for example, to temperature) in a circuit component].

that is,

$$A\beta x_o = x_o$$

which results in

$$A\beta = 1$$

It should be noted that the *frequency of oscillation* $\omega_0$ is determined solely by the phase characteristics of the feedback loop; the loop oscillates at the frequency for which the phase is zero. It follows that the stability of the frequency of oscillation will be determined by the manner in which the phase $\phi(\omega)$ of the feedback loop varies with frequency. A "steep" function $\phi(\omega)$ will result in a more stable frequency. This can be seen if one imagines a change in phase $\Delta\phi$ due to a change in one of the circuit components. If $d\phi/d\omega$ is large, the resulting change in $\omega_0$ will be small, as illustrated in Fig. 17.2.

An alternative approach to the study of oscillator circuits consists of examining the circuit poles, which are the roots of the **characteristic equation** (Eq. 17.3). For the circuit to produce **sustained oscillations** at a frequency $\omega_0$ the characteristic equation has to have roots at $s = \pm j\omega_0$. Thus $1 - A(s)\beta(s)$ should have a factor of the form $s^2 + \omega_0^2$.

## EXERCISES

**17.1** Consider a sinusoidal oscillator formed of an amplifier with a gain of 2 and a second-order bandpass filter. Find the pole frequency and the center-frequency gain of the filter needed to produce sustained oscillations at 1 kHz.

**Ans.** 1 kHz; 0.5

### 17.1.3 Nonlinear Amplitude Control

The oscillation condition, the Barkhausen criterion, just discussed, guarantees sustained oscillations in a mathematical sense. It is well known, however, that the parameters of any physical system cannot be maintained constant for any length of time. In other words, suppose we work hard to make $A\beta = 1$ at $\omega = \omega_0$, and then the temperature changes and $A\beta$ becomes slightly less than unity. Obviously, oscillations will cease in this case. Conversely, if $A\beta$ exceeds unity, oscillations will grow in amplitude. We therefore need a mechanism for forcing $A\beta$ to remain equal to unity *at the desired value of output amplitude*. This task is accomplished by providing a nonlinear circuit for gain control.

Basically, the function of the gain-control mechanism is as follows: First, to ensure that oscillations will start, one designs the circuit such that $A\beta$ is slightly greater than unity. This corresponds to designing the circuit so that the poles are in the right half of the $s$ plane. Thus as the power supply is turned on, oscillations will grow in amplitude. When the amplitude reaches the desired level, the nonlinear network comes into action and causes the loop gain to be reduced to exactly unity. In other words, the poles will be "pulled back" to the $j\omega$ axis. This action will cause the circuit to sustain oscillations at this desired amplitude. If, for some reason, the loop gain is reduced below unity, the amplitude of the sine wave will diminish. This will be detected by the nonlinear network, which will cause the loop gain to increase to exactly unity.

As will be seen, there are two basic approaches to the implementation of the nonlinear amplitude-stabilization mechanism. The first approach makes use of a limiter circuit (see Chapter 4). Oscillations are allowed to grow until the amplitude reaches the level to which the limiter is set. When the limiter comes into operation, the amplitude remains constant. Obviously, the limiter should be "soft" to minimize nonlinear distortion. Such distortion, however, is reduced by the filtering action of the frequency-selective network in the feedback loop. In fact, in one of the oscillator circuits studied in Section 17.2, the sine waves are hard limited, and the resulting square waves are applied to a bandpass filter present in the feedback loop. The "purity" of the output sine waves will be a function of the selectivity of this filter. That is, the higher the $Q$ of the filter, the less the harmonic content of the sine-wave output.

The other mechanism for amplitude control utilizes an element whose resistance can be controlled by the amplitude of the output sinusoid. By placing this element in the feedback circuit so that its resistance determines the loop gain, the circuit can be designed to ensure that the loop gain reaches unity at the desired output amplitude. Diodes, or JFETs operated in the triode region,[2] are commonly employed to implement the controlled-resistance element.

### 17.1.4 A Popular Limiter Circuit for Amplitude Control

We conclude this section by presenting a limiter circuit that is frequently employed for the amplitude control of op-amp oscillators, as well as in a variety of other applications. The circuit is more precise and versatile than those presented in Chapter 4.

The limiter circuit is shown in Fig. 17.3(a), and its transfer characteristic is depicted in Fig. 17.3(b). To see how the transfer characteristic is obtained, consider first the case of a small (close to zero) input signal $v_I$ and a small output voltage $v_O$, so that $v_A$ is positive and $v_B$ is negative. It can be easily seen that both diodes $D_1$ and $D_2$ will be off. Thus all of the

[2] We have not studied JFETs in this book. However, the disk accompanying the book includes material on JFETs and JFET circuits. The same material can also be found on the book's website.

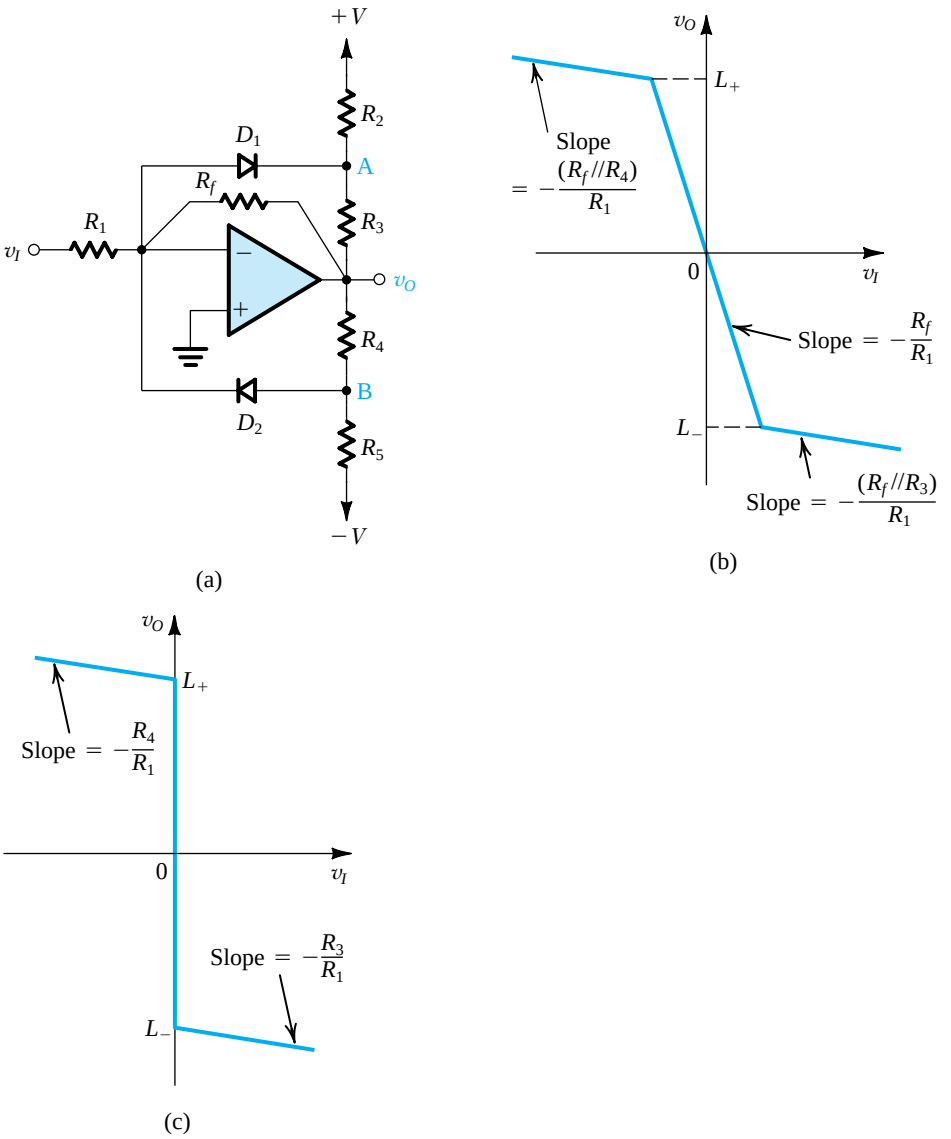



**Figure 17.3** **(a)** A popular limiter circuit. **(b)** Transfer characteristic of the limiter circuit; $L_-$ and $L_+$ are given by Eqs. (17.8) and (17.9), respectively. **(c)** When $R_f$ is removed, the limiter turns into a comparator with the characteristic shown.

input current $v_I/R_1$ flows through the feedback resistance $R_f$, and the output voltage is given by

$$v_O = -(R_f/R_1)v_I \tag{17.5}$$

This is the linear portion of the limiter transfer characteristic in Fig. 17.3(b). We now can use superposition to find the voltages at nodes A and B in terms of $\pm V$ and $v_O$ as

$$v_A = V\frac{R_3}{R_2 + R_3} + v_O\frac{R_2}{R_2 + R_3} \tag{17.6}$$

$$v_B = -V\frac{R_4}{R_4 + R_5} + v_O\frac{R_5}{R_4 + R_5} \tag{17.7}$$

As $v_I$ goes positive, $v_O$ goes negative (Eq. 17.5), and we see from Eq. (17.7) that $v_B$ will become more negative, thus keeping $D_2$ off. Equation (17.6) shows, however, that $v_A$ becomes less positive. Then, if we continue to increase $v_I$, a negative value of $v_O$ will be reached at which $v_A$ becomes −0.7 V or so and diode $D_1$ conducts. If we use the constant-voltage-drop model for $D_1$ and denote the voltage drop $V_D$, the value of $v_O$ at which $D_1$ conducts can be found from Eq. (17.6). This is the negative limiting level, which we denote $L_-$,

$$L_- = -V\frac{R_3}{R_2} - V_D\left(1 + \frac{R_3}{R_2}\right) \tag{17.8}$$

The corresponding value of $v_I$ can be found by dividing $L_-$ by the limiter gain $-R_f/R_1$. If $v_I$ is increased beyond this value, more current is injected into $D_1$, and $v_A$ remains at approximately $-V_D$. Thus the current through $R_2$ remains constant, and the additional diode current flows through $R_3$. Thus $R_3$ appears in effect in parallel with $R_f$, and the incremental gain (ignoring the diode resistance) is $-(R_f \| R_3)/R_1$. To make the slope of the transfer characteristic small in the limiting region, a low value should be selected for $R_3$.

The transfer characteristic for negative $v_I$ can be found in a manner identical to that just employed. It can be easily seen that for negative $v_I$, diode $D_2$ plays an identical role to that played by diode $D_1$ for positive $v_I$. We can use Eq. (17.7) to find the positive limiting level $L_+$

$$L_+ = V\frac{R_4}{R_5} + V_D\left(1 + \frac{R_4}{R_5}\right) \tag{17.9}$$

and the slope of the transfer characteristic in the positive limiting region is $-(R_f \| R_4)/R_1$. We thus see that the circuit of Fig. 17.3(a) functions as a soft limiter, with the limiting levels $L_+$ and $L_-$, and the limiting gains independently adjustable by the selection of appropriate resistor values.

Finally, we note that increasing $R_f$ results in a higher gain in the linear region while keeping $L_+$ and $L_-$ unchanged. In the limit, removing $R_f$ altogether results in the transfer characteristic of Fig. 17.3(c), which is that of a comparator. That is, the circuit compares $v_I$ with the comparator reference value of 0 V: $v_I > 0$ results in $v_O \simeq L_-$, and $v_I < 0$ yields $v_O \simeq L_+$.

## EXERCISES

**17.2** For the circuit of Fig. 17.3(a) with $V = 15$ V, $R_1 = 30$ kΩ, $R_f = 60$ kΩ, $R_2 = R_5 = 9$ kΩ, and $R_3 = R_4 = 3$ kΩ, find the limiting levels and the value of $v_I$ at which the limiting levels are reached. Also determine the limiter gain and the slope of the transfer characteristic in the positive and negative limiting regions. Assume that $V_D = 0.7$ V.

**Ans.** ±5.93 V; ±2.97 V; −2; −0.095

## 17.2 Op Amp–RC Oscillator Circuits

In this section we shall study some practical oscillator circuits utilizing op amps and RC networks.

### 17.2.1 The Wien-Bridge Oscillator

One of the simplest oscillator circuits is based on the Wien bridge. Figure 17.4 shows a Wien-bridge oscillator without the nonlinear gain-control network. The circuit consists of an op amp connected in the noninverting configuration, with a closed-loop gain of $1 + R_2/R_1$. In the feedback path of this positive-gain amplifier an RC network is connected. The loop gain can be easily obtained by multiplying the transfer function $V_a(s)/V_o(s)$ of the feedback network by the amplifier gain,

$$L(s) = \left[1 + \frac{R_2}{R_1}\right] \frac{Z_p}{Z_p + Z_s}$$

$$= \frac{1 + R_2/R_1}{1 + Z_s Y_p}$$

Thus,

$$L(s) = \frac{1 + R_2/R_1}{3 + sCR + 1/sCR} \tag{17.10}$$

Substituting $s = j\omega$ results in

$$L(j\omega) = \frac{1 + R_2/R_1}{3 + j(\omega CR - 1/\omega CR)} \tag{17.11}$$

The loop gain will be a real number (i.e., the phase will be zero) at one frequency given by

$$\omega_0 CR = \frac{1}{\omega_0 CR}$$

That is,

$$\omega_0 = 1/CR \tag{17.12}$$

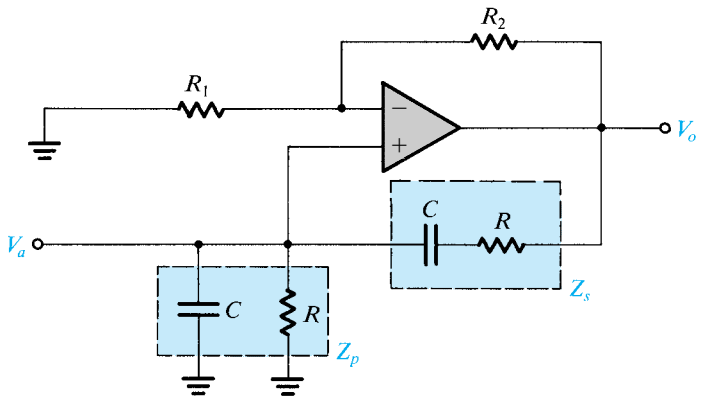



**Figure 17.4** A Wien-bridge oscillator without amplitude stabilization.

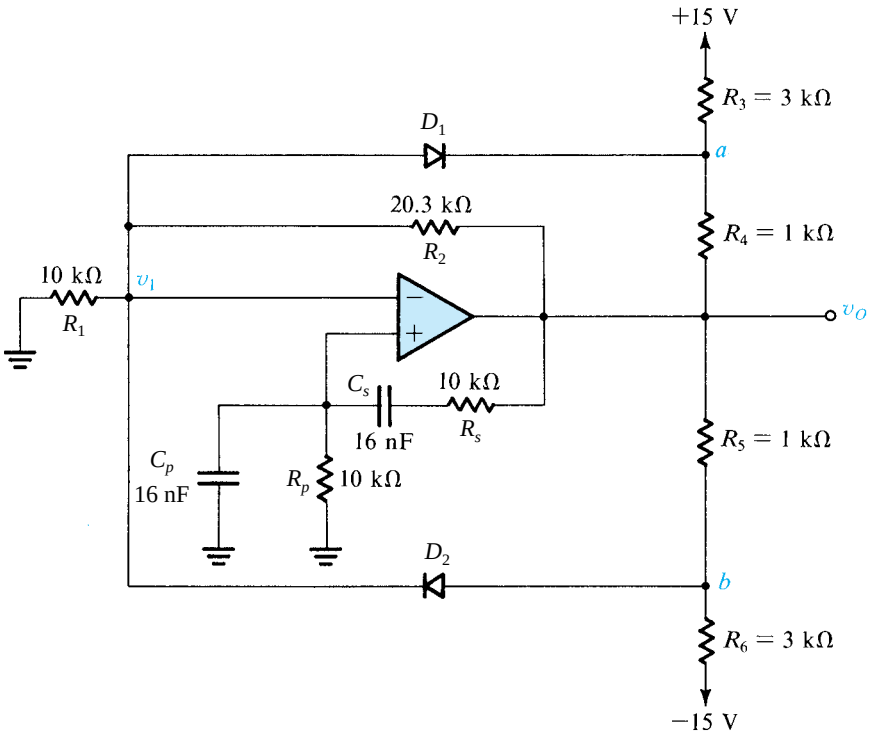



**Figure 17.5** A Wien-bridge oscillator with a limiter used for amplitude control.

To obtain sustained oscillations at this frequency, one should set the magnitude of the loop gain to unity. This can be achieved by selecting

$$R_2/R_1 = 2 \tag{17.13}$$

To ensure that oscillations will start, one chooses $R_2/R_1$ slightly greater than 2. The reader can easily verify that if $R_2/R_1 = 2 + \delta$, where $\delta$ is a small number, the roots of the characteristic equation $1 - L(s) = 0$ will be in the right half of the $s$ plane.

The amplitude of oscillation can be determined and stabilized by using a nonlinear control network. Two different implementations of the amplitude-controlling function are shown in Figs. 17.5 and 17.6. The circuit in Fig. 17.5 employs a symmetrical feedback limiter of the type studied in Section 17.1.3. It is formed by diodes $D_1$ and $D_2$ together with resistors $R_3$, $R_4$, $R_5$, and $R_6$. The limiter operates in the following manner: At the positive peak of the output voltage $v_O$, the voltage at node $b$ will exceed the voltage $v_1$ (which is about $\frac{1}{3}v_O$), and diode $D_2$ conducts. This will clamp the positive peak to a value determined by $R_5$, $R_6$, and the negative power supply. The value of the positive output peak can be calculated by setting $v_b = v_1 + V_{D2}$ and writing a node equation at node $b$ while neglecting the current through $D_2$. Similarly, the negative peak of the output sine wave will be clamped to the value that causes diode $D_1$ to conduct. The value of the negative peak can be determined by setting $v_a = v_1 - V_{D1}$ and writing an equation at node $a$ while neglecting the current through $D_1$. Finally, note that to obtain a symmetrical output waveform, $R_3$ is chosen equal to $R_6$, and $R_4$ equal to $R_5$.

## EXERCISES

**17.3** For the circuit in Fig. 17.5: (a) Disregarding the limiter circuit, find the location of the closed-loop poles. (b) Find the frequency of oscillation. (c) With the limiter in place, find the amplitude of the output sine wave (assume that the diode drop is 0.7 V).
**Ans.** (a) $(10^5/16)(0.015 \pm j)$; (b) 1 kHz; (c) 21.36 V (peak-to-peak)

The circuit of Fig. 17.6 employs an inexpensive implementation of the parameter-variation mechanism of amplitude control. Potentiometer $P$ is adjusted until oscillations just start to grow. As the oscillations grow, the diodes start to conduct, causing the effective resistance between $a$ and $b$ to decrease. Equilibrium will be reached at the output amplitude that causes the loop gain to be exactly unity. The output amplitude can be varied by adjusting potentiometer $P$.

As indicated in Fig. 17.6, the output is taken at point $b$ rather than at the op-amp output terminal because the signal at $b$ has lower distortion than that at $a$. To appreciate this point, note that the voltage at $b$ is proportional to the voltage at the op-amp input terminals and that the latter is a filtered (by the RC network) version of the voltage at node $a$. Node $b$, however, is a high-impedance node, and a buffer will be needed if a load is to be connected.

## EXERCISES

**17.4** For the circuit in Fig. 17.6 find the following: (a) The setting of potentiometer $P$ at which oscillations just start. (b) The frequency of oscillation.
**Ans.** (a) 20 kΩ to ground; (b) 1 kHz

### 17.2.2 The Phase-Shift Oscillator

The basic structure of the phase-shift oscillator is shown in Fig. 17.7. It consists of a negative-gain amplifier ($-K$) with a three-section (third-order) RC ladder network in the feedback. The circuit will oscillate at the frequency for which the phase shift of the RC network is 180°. Only at this frequency will the total phase shift around the loop be 0° or 360°. Here we should note that the reason for using a three-section RC network is that three is the minimum number of sections (i.e., lowest order) that is capable of producing a 180° phase shift at a finite frequency.

For oscillations to be sustained, the value of $K$ should be equal to the inverse of the magnitude of the RC network transfer function at the frequency of oscillation. However, to ensure that oscillations start, the value of $K$ has to be chosen slightly higher than the value that satisfies the unity-loop-gain condition. Oscillations will then grow in magnitude until limited by some nonlinear control mechanism.

Figure 17.8 shows a practical phase-shift oscillator with a feedback limiter, consisting of diodes $D_1$ and $D_2$ and resistors $R_1$, $R_2$, $R_3$, and $R_4$ for amplitude stabilization. To start

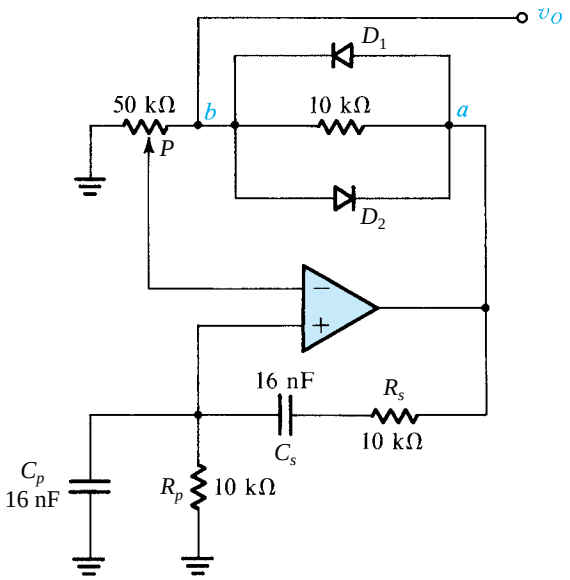



**Figure 17.6** A Wien-bridge oscillator with an alternative method for amplitude stabilization.

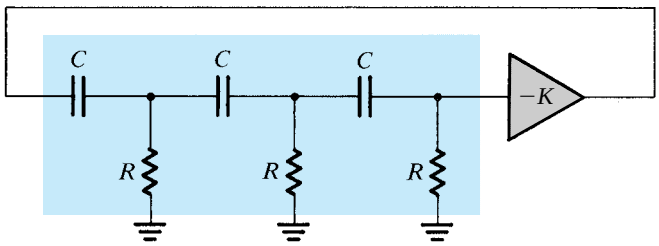



**Figure 17.7** A phase-shift oscillator.

oscillations, $R_f$ has to be made slightly greater than the minimum required value. Although the circuit stabilizes more rapidly and provides sine waves with more stable amplitude, if $R_f$ is made much larger than this minimum, the price paid is an increased output distortion.

## EXERCISES

**17.5** Consider the circuit of Fig. 17.8 *without* the limiter. Break the feedback loop at $X$ and find the loop gain $A\beta \equiv V_o(j\omega)/V_x(j\omega)$. To do this, it is easier to start at the output and work backward, finding the various currents and voltages, and eventually $V_x$ in terms of $V_o$.

**Ans.** $\dfrac{\omega^2 C^2 R R_f}{4 + j(3\omega CR - 1/\omega CR)}$

**17.6** Use the expression derived in Exercise 17.5 to find the frequency of oscillation $f_0$ and the minimum required value of $R_f$ for oscillations to start in the circuit of Fig. 17.8.

**Ans.** $\omega_0 = 1/\sqrt{3}\,CR$; $R_f \geq 12\,R$; $f_0 = 574.3$ Hz; $R_f = 120$ kΩ

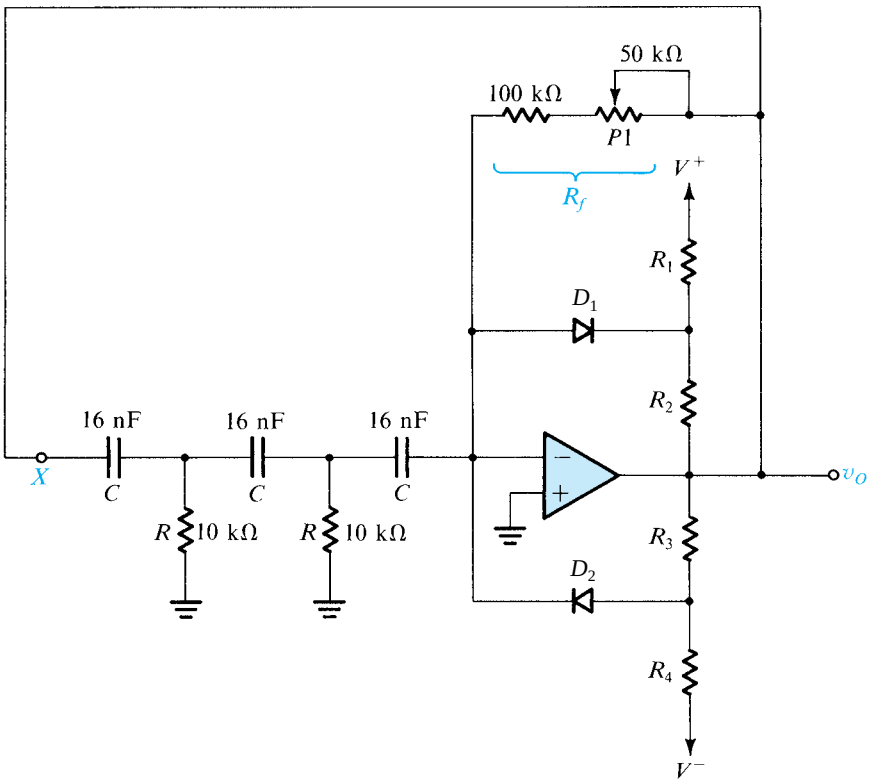



**Figure 17.8** A practical phase-shift oscillator with a limiter for amplitude stabilization.

### 17.2.3 The Quadrature Oscillator

The **quadrature oscillator** is based on the two-integrator loop studied in Section 16.7. As an active filter, the loop is damped to locate the poles in the left half of the $s$ plane. Here, no such damping will be used, since we wish to locate the poles on the $j\omega$ axis to provide sustained oscillations. In fact, to ensure that oscillations start, the poles are initially located in the right half-plane and then "pulled back" by the nonlinear gain control.

Figure 17.9 shows a practical quadrature oscillator. Amplifier 1 is connected as an inverting Miller integrator with a limiter in the feedback for amplitude control. Amplifier 2 is connected as a noninverting integrator (thus replacing the cascade connection of the Miller integrator and the inverter in the two-integrator loop of Fig. 16.25b). To understand the operation of this noninverting integrator, consider the equivalent circuit shown in Fig. 17.9(b). Here, we have replaced the integrator input voltage $v_{O1}$ and the series resistance $2R$ by the Norton equivalent composed of a current source $v_{O1}/2R$ and a parallel resistance $2R$. Now, since $v_{O2} = 2v$, where $v$ is the voltage at the input of op amp 2, the current through $R_f$ will be $(2v - v)/R_f = v/R_f$ in the direction from output to input. Thus $R_f$ gives rise to a negative input resistance, $-R_f$, as indicated in the equivalent circuit of Fig. 17.9(b). Nominally, $R_f$ is made equal to $2R$, and thus $-R_f$ cancels $2R$, and at the input we are left with a current source $v_{O1}/2R$ feeding a capacitor $C$. The result is that $v = \frac{1}{C}\int_0^t \frac{v_{O1}}{2R}dt$ and $v_{O2} = 2v = \frac{1}{CR}\int_0^t v_{O1}dt$. That is, for $R_f = 2R$, the circuit functions as a perfect noninverting integrator. If, however, $R_f$ is made smaller than $2R$, a net negative resistance appears in parallel with $C$.

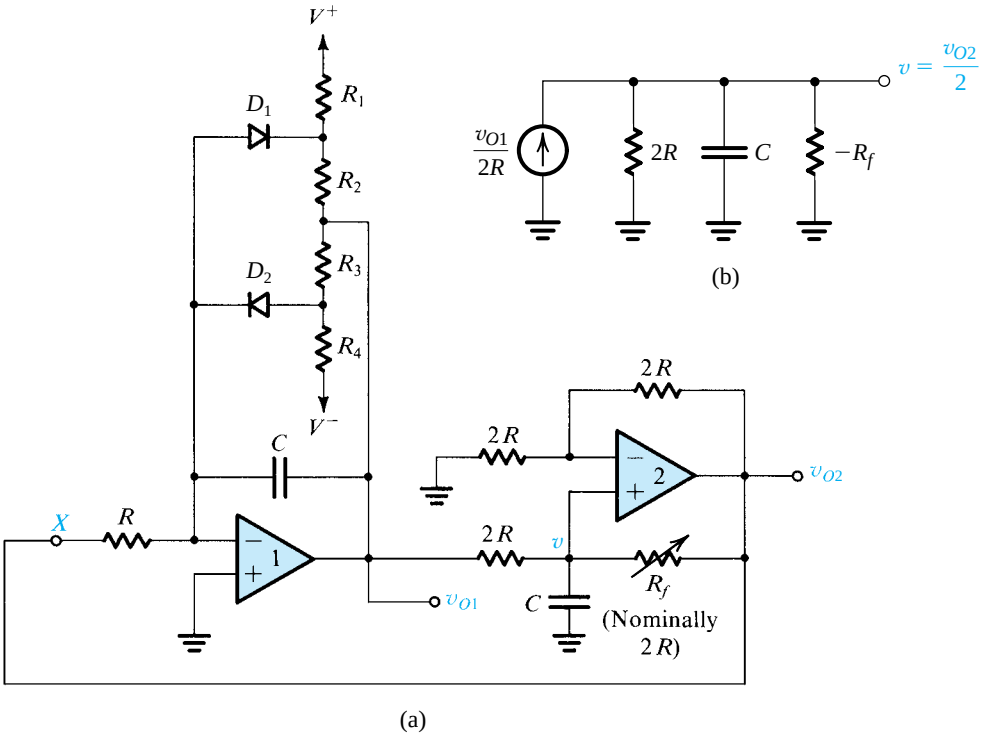



**Figure 17.9** **(a)** A quadrature-oscillator circuit. **(b)** Equivalent circuit at the input of op amp 2.

Returning to the oscillator circuit in Fig. 17.9(a), we note that the resistance $R_f$ in the positive-feedback path of op amp 2 is made variable, with a nominal value of $2R$. Decreasing the value of $R_f$ moves the poles to the right half-plane (Problem 17.19) and ensures that the oscillations start. Too much positive feedback, although it results in better amplitude stability, also results in higher output distortion (because the limiter has to operate "harder"). In this regard, note that the output $v_{O2}$ will be "purer" than $v_{O1}$ because of the filtering action provided by the second integrator on the peak-limited output of the first integrator.

If we disregard the limiter and break the loop at $X$, the loop gain can be obtained as

$$L(s) \equiv \frac{V_{o2}}{V_x} = -\frac{1}{s^2C^2R^2} \tag{17.14}$$

Thus the loop will oscillate at frequency $\omega_0$, given by

$$\omega_0 = \frac{1}{CR} \tag{17.15}$$

Finally, it should be pointed out that the name *quadrature oscillator* is used because the circuit provides two sinusoids with 90° phase difference. This is the case because $v_{O2}$ is the integral of $v_{O1}$. There are many applications for which quadrature sinusoids are required.

## 17.2.4 The Active-Filter-Tuned Oscillator

The last oscillator circuit that we shall discuss is quite simple both in principle and in design. Nevertheless, the approach is general and versatile and can result in high-quality (i.e., low-distortion) output sine waves. The basic principle is illustrated in Fig. 17.10. The

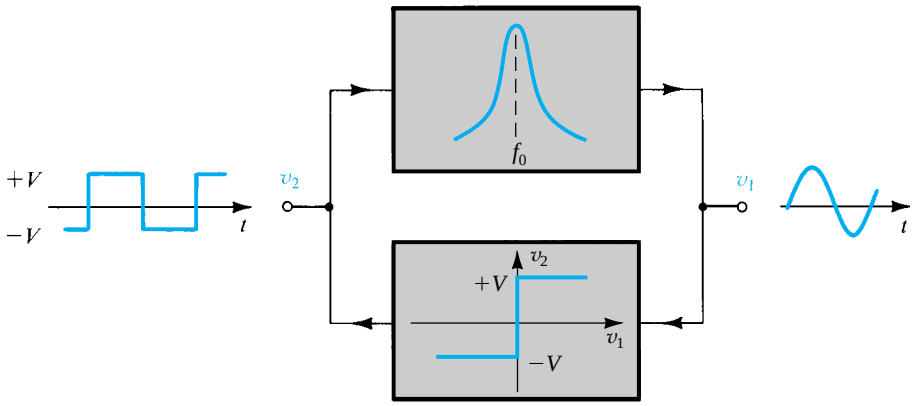



**Figure 17.10** Block diagram of the active-filter-tuned oscillator.

circuit consists of a high-$Q$ bandpass filter connected in a positive-feedback loop with a hard limiter. To understand how this circuit works, assume that oscillations have already started. The output of the bandpass filter will be a sine wave whose frequency is equal to the center frequency of the filter, $f_0$. The sine-wave signal $v_1$ is fed to the limiter, which produces at its output a square wave whose levels are determined by the limiting levels and whose frequency is $f_0$. The square wave in turn is fed to the bandpass filter, which filters out the harmonics and provides a sinusoidal output $v_1$ at the fundamental frequency $f_0$. Obviously, the purity of the output sine wave will be a direct function of the selectivity (or $Q$ factor) of the bandpass filter.

The simplicity of this approach to oscillator design should be apparent. We have independent control of frequency and amplitude as well as of distortion of the output sinusoid. Any filter circuit with positive gain can be used to implement the bandpass filter. The frequency stability of the oscillator will be directly determined by the frequency stability of the bandpass-filter circuit. Also, a variety of limiter circuits (see Chapter 4) with different degrees of sophistication can be used to implement the limiter block.

Figure 17.11 shows one possible implementation of the active-filter-tuned oscillator. This circuit uses a variation on the bandpass circuit based on the Antoniou inductance-simulation circuit (see Fig. 16.22c). Here resistor $R_2$ and capacitor $C_4$ are interchanged. This makes the output of the lower op amp directly proportional to (in fact, twice as large as) the voltage across the resonator, and we can therefore dispense with the buffer amplifier $K$. The limiter used is a very simple one consisting of a resistance $R_1$ and two diodes.

## EXERCISES

**17.7** Using $C = 16$ nF, find the value of $R$ such that the circuit of Fig. 17.11 produces 1-kHz sine waves. If the diode drop is 0.7 V, find the peak-to-peak amplitude of the output sine wave. (*Hint:* A square wave with peak-to-peak amplitude of $V$ volts has a fundamental component with $4V/\pi$ volts peak-to-peak amplitude.)

**Ans.** 10 kΩ; 3.6 V

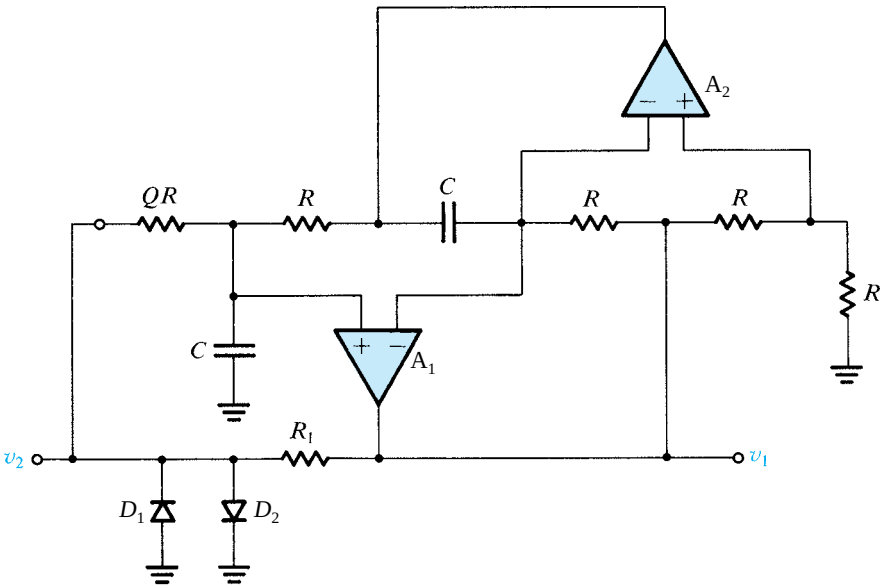



**Figure 17.11** A practical implementation of the active-filter-tuned oscillator.

### 17.2.5 A Final Remark

The op amp–RC oscillator circuits studied are useful for operation in the range 10 Hz to 100 kHz (or perhaps 1 MHz at most). Whereas the lower frequency limit is dictated by the size of passive components required, the upper limit is governed by the frequency-response and slew-rate limitations of op amps. For higher frequencies, circuits that employ transistors together with LC-tuned circuits or crystals are frequently used.[3] These are discussed in Section 17.3.

## 17.3 LC and Crystal Oscillators

Oscillators utilizing transistors (FETs or BJTs), with LC-tuned circuits or crystals as feedback elements, are used in the frequency range of 100 kHz to hundreds of megahertz. They exhibit higher $Q$ than the RC types. However, LC oscillators are difficult to tune over wide ranges, and crystal oscillators operate at a single frequency.

### 17.3.1 LC-Tuned Oscillators

Figure 17.12 shows two commonly used configurations of LC-tuned oscillators. They are known as the **Colpitts oscillator** and the **Hartley oscillator**. Both utilize a parallel LC circuit connected between collector and base (or between drain and gate if a FET is used) with a fraction of the tuned-circuit voltage fed to the emitter (the source in a FET). This

[3] Of course, transistors can be used in place of the op amps in the circuits just studied. At higher frequencies, however, better results are obtained with LC-tuned circuits and crystals.

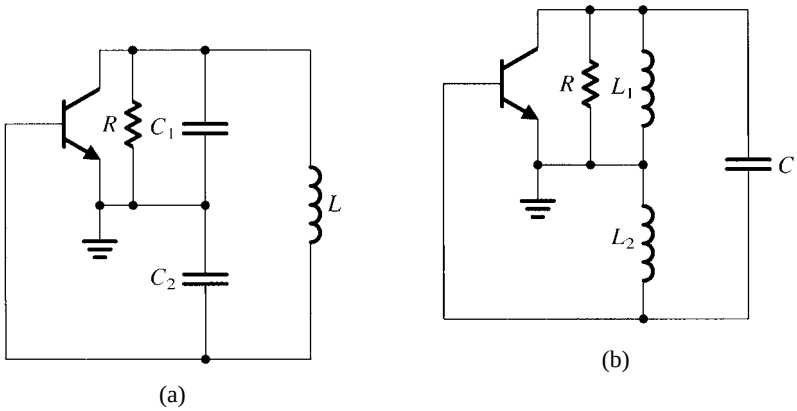



**Figure 17.12** Two commonly used configurations of LC-tuned oscillators: **(a)** Colpitts and **(b)** Hartley.

feedback is achieved by way of a capacitive divider in the Colpitts oscillator and by way of an inductive divider in the Hartley circuit. To focus attention on the oscillator's structure, the bias details are not shown. In both circuits, the resistor $R$ models the combination of the losses of the inductors, the load resistance of the oscillator, and the output resistance of the transistor.

If the frequency of operation is sufficiently low that we can neglect the transistor capacitances, the frequency of oscillation will be determined by the resonance frequency of the parallel-tuned circuit (also known as a *tank circuit* because it behaves as a reservoir for energy storage). Thus for the Colpitts oscillator we have

$$\omega_0 = 1\Big/\sqrt{L\left(\frac{C_1C_2}{C_1+C_2}\right)} \tag{17.16}$$

and for the Hartley oscillator we have

$$\omega_0 = 1/\sqrt{(L_1+L_2)C} \tag{17.17}$$

The ratio $L_1/L_2$ or $C_1/C_2$ determines the feedback factor and thus must be adjusted in conjunction with the transistor gain to ensure that oscillations will start. To determine the oscillation condition for the Colpitts oscillator, we replace the transistor with its equivalent circuit, as shown in Fig. 17.13. To simplify the analysis, we have neglected the transistor capacitance $C_\mu$ ($C_{gd}$ for a FET). Capacitance $C_\pi$ ($C_{gs}$ for a FET), although not shown, can be considered to be a part of $C_2$. The input resistance $r_\pi$ (infinite for a FET) has also been neglected, assuming that at the frequency of oscillation $r_\pi \gg (1/\omega C_2)$. Finally, as mentioned earlier, the resistance $R$ includes $r_o$ of the transistor.

To find the loop gain, we break the loop at the transistor base, apply an input voltage $V_\pi$, and find the returned voltage that appears across the input terminals of the transistor. We then equate the loop gain to unity. An alternative approach is to analyze the circuit and eliminate all current and voltage variables, and thus obtain one equation that governs circuit operation. Oscillations will start if this equation is satisfied. Thus the resulting equation will give us the conditions for oscillation.

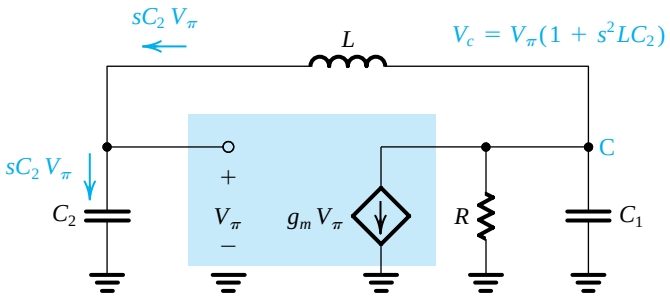



**Figure 17.13** Equivalent circuit of the Colpitts oscillator of Fig. 17.12(a). To simplify the analysis, $C_\mu$ and $r_\pi$ are neglected. We can consider $C_\pi$ to be part of $C_2$, and we can include $r_o$ in $R$.

A node equation at the transistor collector (node C) in the circuit of Fig. 17.13 yields

$$sC_2V_\pi + g_mV_\pi + \left(\frac{1}{R} + s\,C_1\right)(1 + s^2LC_2)V_\pi = 0$$

Since $V_\pi \neq 0$ (oscillations have started), it can be eliminated, and the equation can be rearranged in the form

$$s^3LC_1C_2 + s^2(LC_2/R) + s(C_1 + C_2) + \left(g_m + \frac{1}{R}\right) = 0 \tag{17.18}$$

Substituting $s = j\omega$ gives

$$\left(g_m + \frac{1}{R} - \frac{\omega^2LC_2}{R}\right) + j[\omega(C_1 + C_2) - \omega^3LC_1C_2] = 0 \tag{17.19}$$

For oscillations to start, both the real and imaginary parts must be zero. Equating the imaginary part to zero gives the frequency of oscillation as

$$\omega_0 = 1\Big/\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)} \tag{17.20}$$

which is the resonance frequency of the tank circuit, as anticipated.[4] Equating the real part to zero together with Eq. (17.20) gives

$$C_2/C_1 = g_mR \tag{17.21}$$

which has a simple physical interpretation: For sustained oscillations, the magnitude of the gain from base to collector ($g_mR$) must be equal to the inverse of the voltage ratio provided by the capacitive divider, which from Fig. 17.12(a) can be seen to be $v_{eb}/v_{ce} = C_1/C_2$. Of course, for oscillations to start, the loop gain must be made greater than unity, a condition that can be stated in the equivalent form

$$g_mR > C_2/C_1 \tag{17.22}$$

[4] If $r_\pi$ is taken into account, the frequency of oscillation can be shown to shift slightly from the value given by Eq. (17.20).

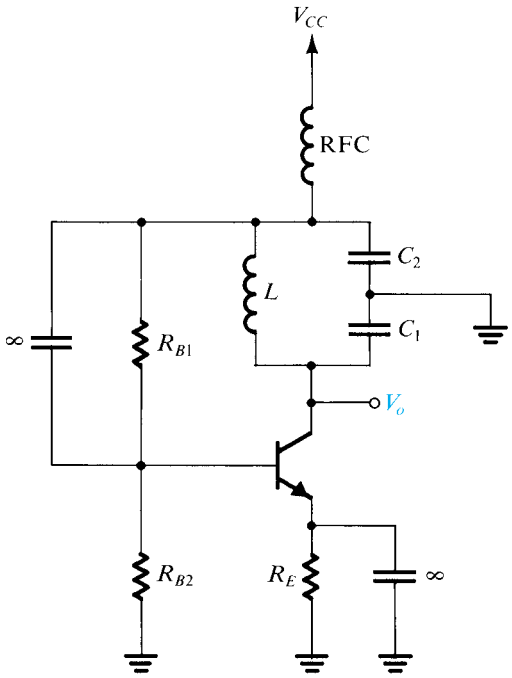



**Figure 17.14** Complete circuit for a Colpitts oscillator.

As oscillations grow in amplitude, the transistor's nonlinear characteristics reduce the effective value of $g_m$ and, correspondingly, reduce the loop gain to unity, thus sustaining the oscillations.

Analysis similar to the foregoing can be carried out for the Hartley circuit (see later: Exercise 17.8). At high frequencies, more accurate transistor models must be used. Alternatively, the *y* parameters of the transistor can be measured at the intended frequency $\omega_0$, and the analysis can then be carried out using the *y*-parameter model (see Appendix C). This is usually simpler and more accurate, especially at frequencies above about 30% of the transistor $f_T$.

As an example of a practical LC oscillator, we show in Fig. 17.14 the circuit of a Colpitts oscillator, complete with bias details. Here the radio-frequency choke (RFC) provides a high reactance at $\omega_0$ but a low dc resistance.

Finally, a few words are in order on the mechanism that determines the amplitude of oscillations in the LC-tuned oscillators discussed above. Unlike the op-amp oscillators that incorporate special amplitude-control circuitry, LC-tuned oscillators utilize the nonlinear $i_C$–$v_{BE}$ characteristics of the BJT (the $i_D$–$v_{GS}$ characteristics of the FET) for amplitude control. Thus these LC-tuned oscillators are known as *self-limiting oscillators*. Specifically, as the oscillations grow in amplitude, the effective gain of the transistor is reduced below its small-signal value. Eventually, an amplitude is reached at which the effective gain is reduced to the point that the Barkhausen criterion is satisfied exactly. The amplitude then remains constant at this value.

Reliance on the nonlinear characteristics of the BJT (or the FET) implies that the collector (drain) current waveform will be nonlinearly distorted. Nevertheless, the output voltage signal will still be a sinusoid of high purity because of the filtering action of the LC-tuned circuit. Detailed analysis of amplitude control, which makes use of nonlinear-circuit techniques, is beyond the scope of this book.

## EXERCISES

**17.8** Show that for the Hartley oscillator of Fig. 17.12(b), the frequency of oscillation is given by Eq. (17.17) and that for oscillations to start $g_m R > (L_1/L_2)$.

**D17.9** Using a BJT biased at $I_C = 1$ mA, design a Colpitts oscillator to operate at $\omega_0 = 10^6$ rad/s. Use $C_1 = 0.01$ μF and assume that the coil available has a $Q$ of 100 (this can be represented by a resistance in parallel with $C_1$ given by $Q/\omega_0 C_1$). Also assume that there is a load resistance at the collector of 2 kΩ and that for the BJT, $r_o = 100$ kΩ. Find $C_2$ and $L$.
**Ans.** 0.66 μF; 100 μH (a somewhat smaller $C_2$ would be used to allow oscillations to grow in amplitude)

### 17.3.2 Crystal Oscillators

A piezoelectric crystal, such as quartz, exhibits electromechanical-resonance characteristics that are very stable (with time and temperature) and highly selective (having very high $Q$ factors). The circuit symbol of a crystal is shown in Fig. 17.15(a), and its equivalent circuit model is given in Fig. 17.15(b). The resonance properties are characterized by a large inductance $L$ (as high as hundreds of henrys), a very small series capacitance $C_s$ (as small as 0.0005 pF), a series resistance $r$ representing a $Q$ factor $\omega_0 L/r$ that can be as high as a few hundred thousand, and a parallel capacitance $C_p$ (a few picofarads). Capacitor $C_p$ represents the electrostatic capacitance between the two parallel plates of the crystal. Note that $C_p \gg C_s$.

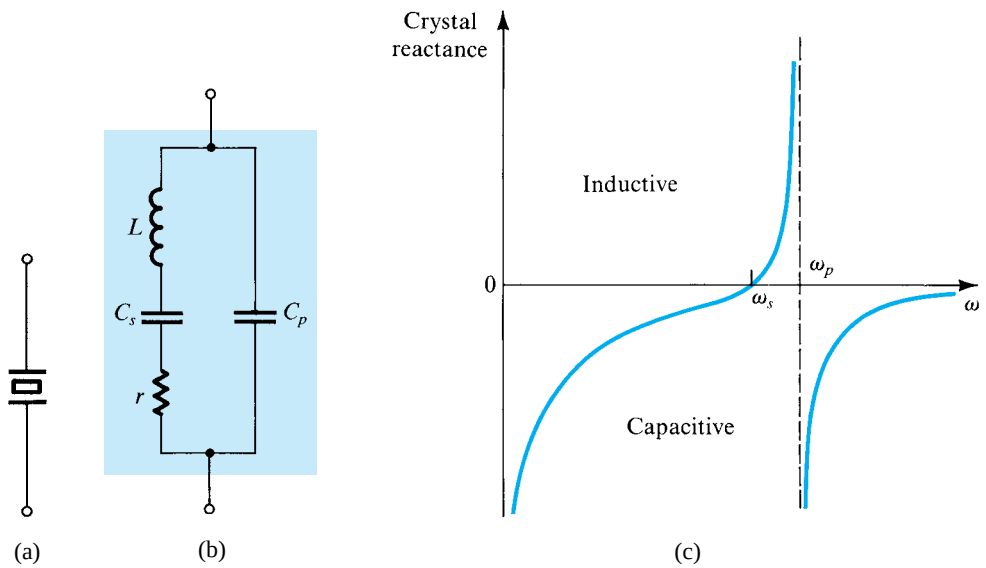



**Figure 17.15** A piezoelectric crystal. **(a)** Circuit symbol. **(b)** Equivalent circuit. **(c)** Crystal reactance versus frequency [note that, neglecting the small resistance $r$, $Z_{\text{crystal}} = jX(\omega)$].

Since the $Q$ factor is very high, we may neglect the resistance $r$ and express the crystal impedance as

$$Z(s) = 1\Big/\left[sC_p + \frac{1}{sL + 1/sC_s}\right]$$

which can be manipulated to the form

$$Z(s) = \frac{1}{sC_p}\,\frac{s^2 + (1/LC_s)}{s^2 + [(C_p + C_s)/LC_sC_p]} \tag{17.23}$$

From Eq. (17.23) and from Fig. 17.15(b), we see that the crystal has two resonance frequencies: a series resonance at $\omega_s$

$$\omega_s = 1/\sqrt{LC_s} \tag{17.24}$$

and a parallel resonance at $\omega_p$

$$\omega_p = 1\Big/\sqrt{L\left(\frac{C_sC_p}{C_s + C_p}\right)} \tag{17.25}$$

Thus for $s = j\omega$ we can write

$$Z(j\,\omega) = -j\frac{1}{\omega C_p}\left(\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}\right) \tag{17.26}$$

From Eqs. (17.24) and (17.25) we note that $\omega_p > \omega_s$. However, since $C_p \gg C_s$, the two resonance frequencies are very close. Expressing $Z(j\omega) = jX(\omega)$, the crystal reactance $X(\omega)$ will have the shape shown in Fig. 17.15(c). We observe that the crystal reactance is inductive over the very narrow frequency band between $\omega_s$ and $\omega_p$. For a given crystal, this frequency band is well defined. Thus we may use the crystal to replace the inductor of the Colpitts oscillator (Fig. 17.12a). The resulting circuit will oscillate at the resonance frequency of the crystal inductance $L$ with the series equivalent of $C_s$ and $(C_p + C_1C_2/(C_1 + C_2))$. Since $C_s$ is much smaller than the three other capacitances, it will be dominant and

$$\omega_0 \simeq 1/\sqrt{LC_s} = \omega_s \tag{17.27}$$

In addition to the basic Colpitts oscillator, a variety of configurations exist for crystal oscillators. Figure 17.16 shows a popular configuration (called the **Pierce oscillator**) utilizing a CMOS inverter (see Section 13.2) as an amplifier. Resistor $R_f$ determines a dc operating point in the high-gain region of the VTC of the CMOS inverter. Resistor $R_1$ together with capacitor $C_1$ provides a low-pass filter that discourages the circuit from oscillating at a higher harmonic of the crystal frequency. Note that this circuit also is based on the Colpitts configuration.

The extremely stable resonance characteristics and the very high $Q$ factors of quartz crystals result in oscillators with very accurate and stable frequencies. Crystals are available with resonance frequencies in the range of a few kilohertz to hundreds of megahertz. Temperature coefficients of $\omega_0$ of 1 or 2 parts per million (ppm) per degree Celsius are achievable. Unfortunately, however, crystal oscillators, being mechanical resonators, are fixed-frequency circuits.

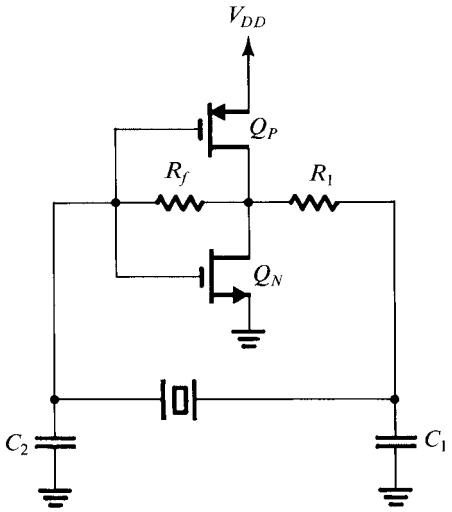



**Figure 17.16** A Pierce crystal oscillator utilizing a CMOS inverter as an amplifier.

## EXERCISES

**17.10** A 2-MHz quartz crystal is specified to have $L = 0.52$ H, $C_s = 0.012$ pF, $C_p = 4$ pF, and $r = 120\ \Omega$. Find $f_s$, $f_p$, and $Q$.
**Ans.** 2.015 MHz; 2.018 MHz; 55,000

# 17.4 Bistable Multivibrators

In this section we begin the study of waveform-generating circuits of the other type—nonlinear oscillators or function generators. These devices make use of a special class of circuits known as **multivibrators**. As mentioned earlier, there are three types of multivibrator: bistable, monostable, and astable. This section is concerned with the first, the bistable multivibrator.[5]

As its name indicates, the **bistable multivibrator** has *two stable states*. The circuit can remain in either stable state indefinitely and moves to the other stable state only when appropriately *triggered*.

## 17.4.1 The Feedback Loop

Bistability can be obtained by connecting a dc amplifier in a positive-feedback loop having a loop gain greater than unity. Such a feedback loop is shown in Fig. 17.17; it consists of an op amp and a resistive voltage divider in the positive-feedback path. To see how bistability is obtained, consider operation with the positive-input terminal of the op amp near ground potential. This is a reasonable starting point, since the circuit has no external excitation.

[5] Digital implementations of multivibrators were presented in Chapter 15. Here, we are interested in implementations utilizing op amps.

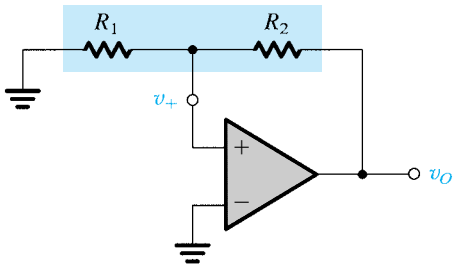



**Figure 17.17** A positive-feedback loop capable of bistable operation.

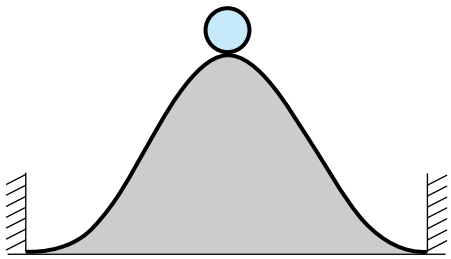


**Figure 17.18** A physical analogy for the operation of the bistable circuit. The ball cannot remain at the top of the hill for any length of time (a state of unstable equilibrium or metastability); the inevitably present disturbance will cause the ball to fall to one side or the other, where it can remain indefinitely (the two stable states).

Assume that the electrical noise that is inevitably present in every electronic circuit causes a small positive increment in the voltage $v_+$. This incremental signal will be amplified by the large open-loop gain $A$ of the op amp, with the result that a much greater signal will appear in the op amp's output voltage $v_O$. The voltage divider ($R_1$, $R_2$) will feed a fraction $\beta \equiv R_1/(R_1 + R_2)$ of the output signal back to the positive-input terminal of the op amp. If $A\beta$ is greater than unity, as is usually the case, the fed-back signal will be greater than the original increment in $v_+$. This *regenerative* process continues until eventually the op amp saturates with its output voltage at the positive-saturation level, $L_+$. When this happens, the voltage at the positive-input terminal, $v_+$, becomes $L_+R_1/(R_1 + R_2)$, which is positive and thus keeps the op amp in positive saturation. This is one of the two stable states of the circuit.

In the description above we assumed that when $v_+$ was near zero volts, a positive increment occurred in $v_+$. Had we assumed the equally probable situation of a negative increment, the op amp would have ended up saturated in the negative direction with $v_O = L_-$ and $v_+ = L_-R_1/(R_1 + R_2)$. This is the other stable state.

We thus conclude that the circuit of Fig. 17.17 has two stable states, one with the op amp in positive saturation and the other with the op amp in negative saturation. The circuit can exist in either of these two states indefinitely. We also note that the circuit cannot exist in the state for which $v_+ = 0$ and $v_O = 0$ for any length of time. This is a state of *unstable equilibrium* (also known as a **metastable state**); any disturbance, such as that caused by electrical noise, causes the bistable circuit to switch to one of its two stable states. This is in sharp contrast to the case when the feedback is negative, causing a virtual short circuit to appear between the op amp's input terminals and maintaining this virtual short circuit in the face of disturbances. A physical analogy for the operation of the bistable circuit is depicted in Fig. 17.18.

## 17.4.2 Transfer Characteristics of the Bistable Circuit

The question naturally arises as to how we can make the bistable circuit of Fig. 17.17 change state. To help answer this crucial question, we derive the transfer characteristics of the

bistable. Reference to Fig. 17.17 indicates that either of the two circuit nodes that are connected to ground can serve as an input terminal. We investigate both possibilities.

Figure 17.19(a) shows the bistable circuit with a voltage $v_I$ applied to the inverting input terminal of the op amp. To derive the transfer characteristic $v_O$–$v_I$, assume that $v_O$ is at one of its two possible levels, say $L_+$, and thus $v_+ = \beta L_+$. Now as $v_I$ is increased from 0 V, we can see from the circuit that nothing happens until $v_I$ reaches a value equal to $v_+$ (i.e., $\beta L_+$). As $v_I$ begins to exceed this value, a net negative voltage develops between the input terminals of the op amp. This voltage is amplified by the open-loop gain of the op amp, and thus $v_O$ goes negative. The voltage divider in turn causes $v_+$ to go negative, thus increasing the net negative input to the op amp and keeping the regenerative process going. This process culminates in

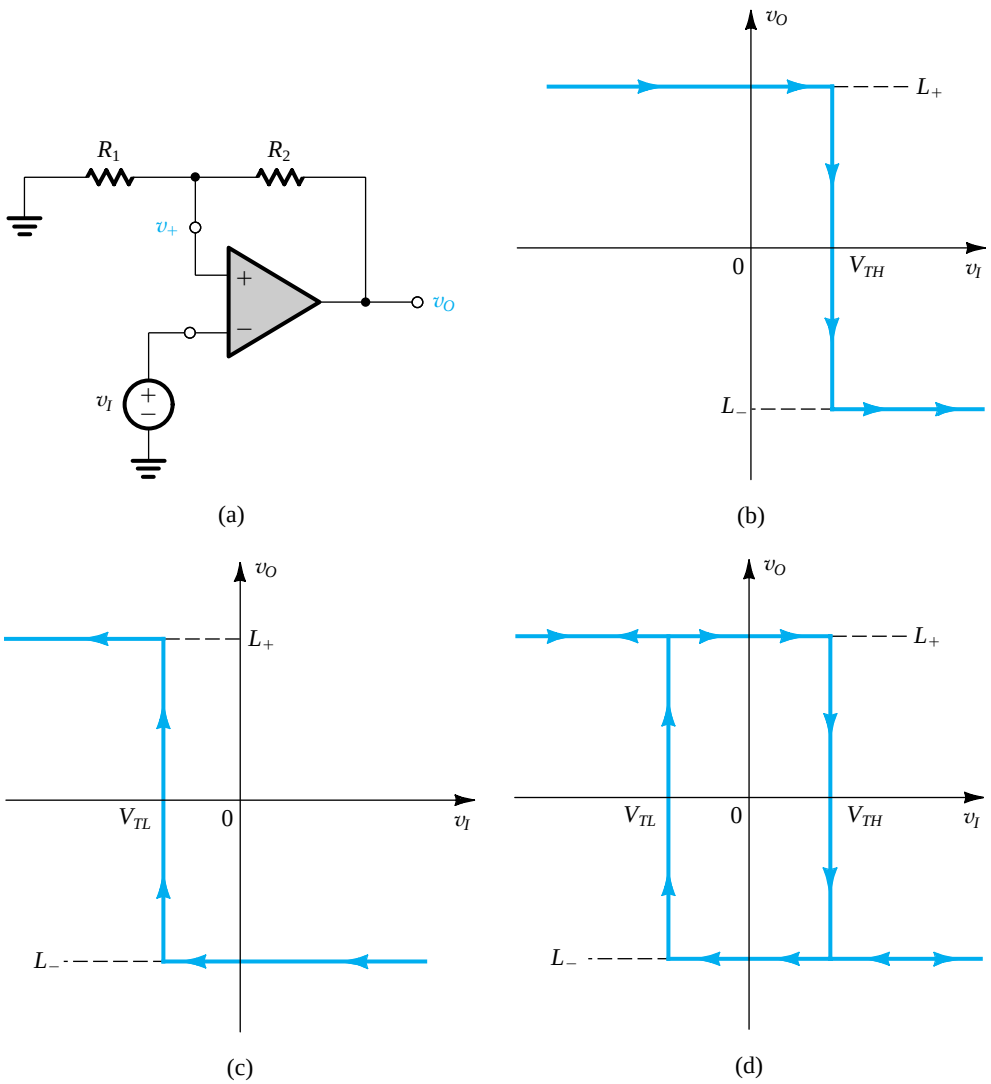



**Figure 17.19** **(a)** The bistable circuit of Fig. 17.17 with the negative input terminal of the op amp disconnected from ground and connected to an input signal $v_I$. **(b)** The transfer characteristic of the circuit in **(a)** for increasing $v_I$. **(c)** The transfer characteristic for decreasing $v_I$. **(d)** The complete transfer characteristics.

the op amp saturating in the negative direction: that is, with $v_O = L_-$ and, correspondingly, $v_+ = \beta L_-$. It is easy to see that increasing $v_I$ further has no effect on the acquired state of the bistable circuit. Figure 17.19(b) shows the transfer characteristic for increasing $v_I$. Observe that the characteristic is that of a comparator with a threshold voltage denoted $V_{TH}$, where $V_{TH} = \beta L_+$.

Next consider what happens as $v_I$ is decreased. Since now $v_+ = \beta L_-$, we see that the circuit remains in the negative-saturation state until $v_I$ goes negative to the point that it equals $\beta L_-$. As $v_I$ goes below this value, a net positive voltage appears between the op amp's input terminals. This voltage is amplified by the op-amp gain and thus gives rise to a positive voltage at the op amp's output. The regenerative action of the positive-feedback loop then sets in and causes the circuit eventually to go to its positive-saturation state, in which $v_O = L_+$ and $v_+ = \beta L_+$. The transfer characteristic for decreasing $v_I$ is shown in Fig. 17.19(c). Here again we observe that the characteristic is that of a comparator, but with a threshold voltage $V_{TL} = \beta L_-$.

The complete transfer characteristics, $v_O$–$v_I$, of the circuit in Fig. 17.19(a) can be obtained by combining the characteristics in Fig. 17.19(b) and (c), as shown in Fig. 17.19(d). As indicated, the circuit changes state at different values of $v_I$, depending on whether $v_I$ is increasing or decreasing. Thus the circuit is said to exhibit *hysteresis;* the width of the hysteresis is the difference between the high threshold $V_{TH}$ and the low threshold $V_{TL}$. Also note that the bistable circuit is in effect a comparator with hysteresis. As will be shown shortly, adding hysteresis to a comparator's characteristics can be very beneficial in certain applications. Finally, observe that because the bistable circuit of Fig. 17.19 switches from the positive state ($v_O = L_+$) to the negative state ($v_O = L_-$) as $v_I$ is increased past the positive threshold $V_{TH}$, the circuit is said to be *inverting*. A bistable circuit with a *noninverting* transfer characteristic will be presented shortly.

### 17.4.3 Triggering the Bistable Circuit

Returning now to the question of how to make the bistable circuit change state, we observe from the transfer characteristics of Fig. 17.19(d) that if the circuit is in the $L_+$ state it can be switched to the $L_-$ state by applying an input $v_I$ of value greater than $V_{TH} \equiv \beta L_+$. Such an input causes a net negative voltage to appear between the input terminals of the op amp, which initiates the regenerative cycle that culminates in the circuit switching to the $L_-$ stable state. Here it is important to note that the input $v_I$ merely initiates or *triggers* regeneration. Thus we can remove $v_I$ with no effect on the regeneration process. In other words, $v_I$ can be simply a pulse of short duration. The input signal $v_I$ is thus referred to as a **trigger signal**, or simply a **trigger**.

The characteristics of Fig. 17.19(d) indicate also that the bistable circuit can be switched to the positive state ($v_O = L_+$) by applying a negative trigger signal $v_I$ of magnitude greater than that of the negative threshold $V_{TL}$.

### 17.4.4 The Bistable Circuit as a Memory Element

We observe from Fig. 17.19(d) that for input voltages in the range $V_{TL} < v_I < V_{TH}$, the output can be either $L_+$ or $L_-$, *depending on the state that the circuit is already in*. Thus, for this input range, the output is determined by the *previous* value of the trigger signal (the trigger signal that caused the circuit to be in its current state). Thus the circuit exhibits *memory.* Indeed, the bistable multivibrator is the basic memory element of digital systems, as we have seen in Chapter 15. Finally, note that in analog circuit applications, such as the ones of concern to us in this chapter, the bistable circuit is also known as a **Schmitt trigger**.

### 17.4.5 A Bistable Circuit with Noninverting Transfer Characteristics

The basic bistable feedback loop of Fig. 17.17 can be used to derive a circuit with noninverting transfer characteristics by applying the input signal $v_I$ (the trigger signal) to the terminal of $R_1$ that is connected to ground. The resulting circuit is shown in Fig. 17.20(a). To obtain the transfer characteristics we first employ superposition to the linear circuit formed by $R_1$ and $R_2$, thus expressing $v_+$ in terms of $v_I$ and $v_O$ as

$$v_+ = v_I \frac{R_2}{R_1 + R_2} + v_O \frac{R_1}{R_1 + R_2} \tag{17.28}$$

From this equation we see that if the circuit is in the positive stable state with $v_O = L_+$, positive values for $v_I$ will have no effect. To trigger the circuit into the $L_-$ state, $v_I$ must be made negative and of such a value as to make $v_+$ decrease below zero. Thus the low threshold $V_{TL}$ can be found by substituting in Eq. (17.28) $v_O = L_+$, $v_+ = 0$, and $v_I = V_{TL}$. The result is

$$V_{TL} = -L_+(R_1/R_2) \tag{17.29}$$

Similarly, Eq. (17.28) indicates that when the circuit is in the negative-output state ($v_O = L_-$), negative values of $v_I$ will make $v_+$ more negative with no effect on operation. To initiate the regeneration process that causes the circuit to switch to the positive state, $v_+$ must be made to go slightly positive. The value of $v_I$ that causes this to happen is the high threshold voltage $V_{TH}$, which can be found by substituting in Eq. (17.28) $v_O = L_-$ and $v_+ = 0$. The result is

$$V_{TH} = -L_-(R_1/R_2) \tag{17.30}$$

The complete transfer characteristic of the circuit of Fig. 17.20(a) is displayed in Fig. 17.20(b). Observe that a positive triggering signal $v_I$ (of value greater than $V_{TH}$) causes the circuit to switch to the positive state ($v_O$ goes from $L_-$ to $L_+$). Thus the transfer characteristic of this circuit is noninverting.

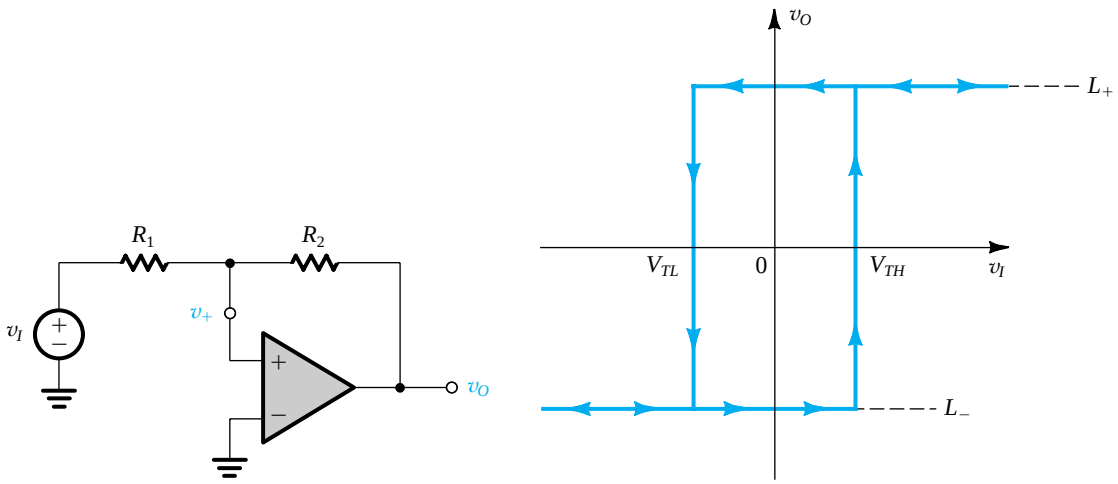
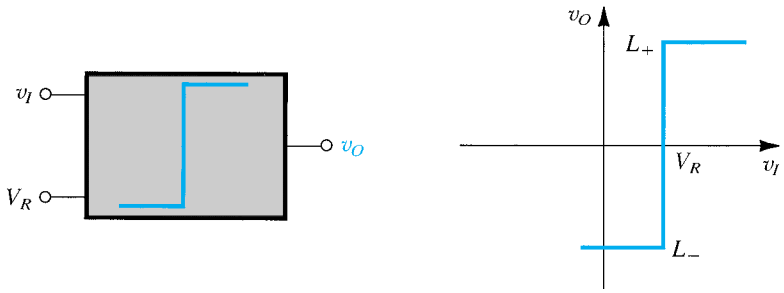



**Figure 17.20** **(a)** A bistable circuit derived from the positive-feedback loop of Fig. 17.17 by applying $v_I$ through $R_1$. **(b)** The transfer characteristic of the circuit in **(a)** is noninverting. (Compare it to the inverting characteristic in Fig. 17.19d.)

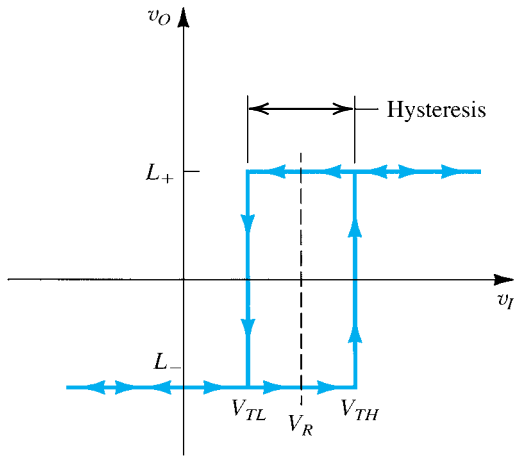
### 17.4.6 Application of the Bistable Circuit as a Comparator

The comparator is an analog-circuit building block that is used in a variety of applications ranging from detecting the level of an input signal relative to a preset threshold value, to the design of analog-to-digital (A/D) converters. Although one normally thinks of the comparator as having a single threshold value (see Fig. 17.21a), it is useful in many applications to add hysteresis to the comparator characteristics. If this is done, the comparator exhibits two threshold values, $V_{TL}$ and $V_{TH}$, symmetrically placed about the desired reference level, as indicated in Fig. 17.21(b). Usually $V_{TH}$ and $V_{TL}$ are separated by a small amount, say 100 mV.

To demonstrate the need for hysteresis, we consider a common application of comparators. It is required to design a circuit that detects and counts the zero crossings of an arbitrary waveform. Such a function can be implemented using a comparator whose threshold is set to 0 V. The comparator provides a step change at its output every time a zero crossing occurs. Each step change can be used to generate a pulse, and the pulses are fed to a counter circuit.




(a)




(b)

**Figure 17.21** **(a)** Block diagram representation and transfer characteristic for a comparator having a reference, or threshold, voltage $V_R$. **(b)** Comparator characteristic with hysteresis.

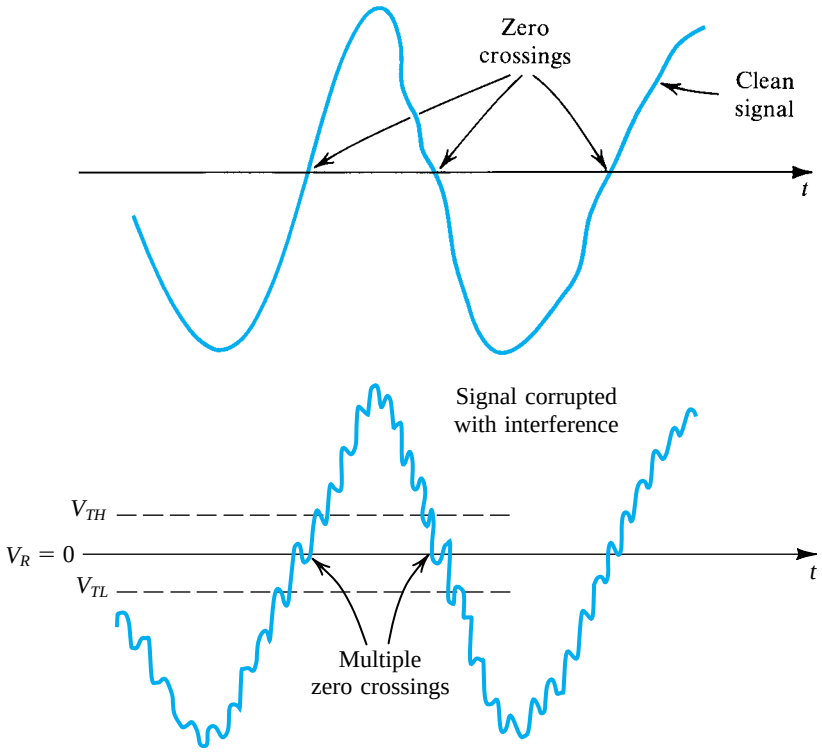



**Figure 17.22** Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference.

Imagine now what happens if the signal being processed has—as it usually does have—interference superimposed on it, say of a frequency much higher than that of the signal. It follows that the signal might cross the zero axis a number of times around each of the zero-crossing points we are trying to detect, as shown in Fig. 17.22. The comparator would thus change state a number of times at each of the zero crossings, and our count would obviously be in error. However, if we have an idea of the expected peak-to-peak amplitude of the interference, the problem can be solved by introducing hysteresis of appropriate width in the comparator characteristics. Then, if the input signal is increasing in magnitude, the comparator with hysteresis will remain in the low state until the input level exceeds the high threshold $V_{TH}$. Subsequently the comparator will remain in the high state even if, owing to interference, the signal decreases below $V_{TH}$. The comparator will switch to the low state only if the input signal is decreased below the low threshold $V_{TL}$. The situation is illustrated in Fig. 17.22, from which we see that including hysteresis in the comparator characteristics provides an effective means for rejecting interference (thus providing another form of filtering).

### 17.4.7 Making the Output Levels More Precise

The output levels of the bistable circuit can be made more precise than the saturation voltages of the op amp are by cascading the op amp with a limiter circuit (see Section 4.6 for a discussion of limiter circuits). Two such arrangements are shown in Fig. 17.23.

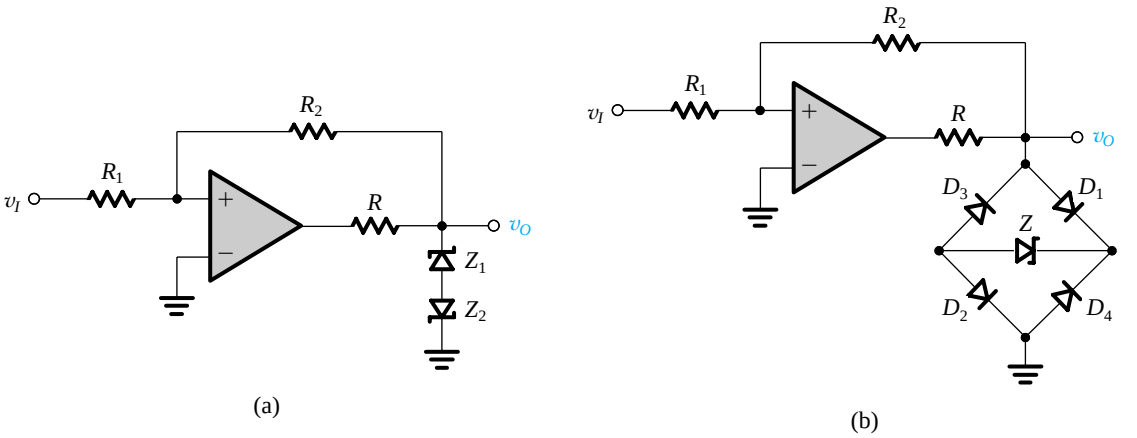



**Figure 17.23** Limiter circuits are used to obtain more precise output levels for the bistable circuit. In both circuits the value of $R$ should be chosen to yield the current required for the proper operation of the zener diodes. **(a)** For this circuit $L_+ = V_{Z_1} + V_D$ and $L_- = -(V_{Z_2} + V_D)$, where $V_D$ is the forward diode drop. **(b)** For this circuit $L_+ = V_Z + V_{D_1} + V_{D_2}$ and $L_- = -(V_Z + V_{D_3} + V_{D_4})$.

## EXERCISES

**D17.11** The op amp in the bistable circuit of Fig. 17.19(a) has output saturation voltages of ±13 V. Design the circuit to obtain threshold voltages of ±5 V. For $R_1 = 10$ kΩ, find the value required for $R_2$.
**Ans.** 16 kΩ

**D17.12** If the op amp in the circuit of Fig. 17.20(a) has ±10-V output saturation levels, design the circuit to obtain ±5-V thresholds. Give suitable component values.
**Ans.** Possible choice: $R_1 = 10$ kΩ and $R_2 = 20$ kΩ

**17.13** Consider a bistable circuit with a noninverting transfer characteristic and let $L_+ = -L_- = 10$ V and $V_{TH} = -V_{TL} = 5$ V. If $v_I$ is a triangular wave with a 0-V average, a 10-V peak amplitude, and a 1-ms period, sketch the waveform of $v_O$. Find the time interval between the zero crossings of $v_I$ and $v_O$.
**Ans.** $v_O$ is a square wave with 0-V average, 10-V amplitude, and 1-ms period and is delayed by 125 μs relative to $v_I$

**17.14** Consider an op amp having saturation levels of ±12 V used without feedback, with the inverting input terminal connected to +3 V and the noninverting input terminal connected to $v_I$. Characterize its operation as a comparator. What are $L_+$, $L_-$, and $V_R$, as defined in Fig. 17.21(a)?
**Ans.** +12 V; −12 V; +3 V

**17.15** In the circuit of Fig. 17.20(a), let $L_+ = -L_- = 10$ V and $R_1 = 1$ kΩ. Find a value for $R_2$ that gives a hysteresis of 100-mV width.
**Ans.** 200 kΩ

## 17.5 Generation of Square and Triangular Waveforms Using Astable Multivibrators

A square waveform can be generated by arranging for a bistable multivibrator to switch states periodically. This can be done by connecting the bistable multivibrator with an RC circuit in a feedback loop, as shown in Fig. 17.24(a). Observe that the bistable multivibrator has an inverting transfer characteristic and can thus be realized using the circuit of Fig. 17.19(a). This results in the circuit of Fig. 17.24(b). We shall show shortly that this circuit has no stable states and thus is appropriately named an **astable multivibrator**.

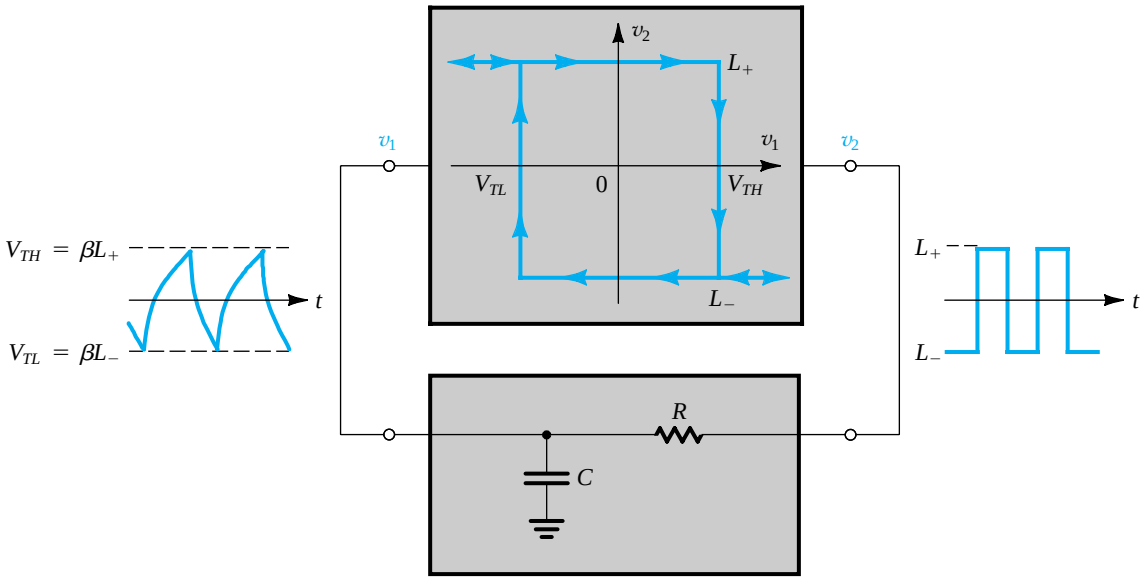
At this point we wish to remind the reader of an important relationship, which we shall employ on many occasions in the following few sections: A capaciter $C$ that is charging or discharging through a resistance $R$ toward a final voltage $V_\infty$ has a voltage $v(t)$,

$$v(t) = V_\infty - (V_\infty - V_{0+})\, e^{-t/\tau}$$

where $V_{0+}$ is the voltage at $t = 0+$ and $\tau = CR$ is the time constant.

### 17.5.1 Operation of the Astable Multivibrator

To see how the astable multivibrator operates, refer to Fig. 17.24(b) and let the output of the bistable multivibrator be at one of its two possible levels, say $L_+$. Capacitor $C$ will charge toward this level through resistor $R$. Thus the voltage across $C$, which is applied to the negative input terminal of the op amp and thus is denoted $v_-$, will rise exponentially toward $L_+$ with a time constant $\tau = CR$. Meanwhile, the voltage at the positive input terminal of the op amp is $v_+ = \beta L_+$. This situation will continue until the capacitor voltage reaches the positive threshold $V_{TH} = \beta L_+$, at which point the bistable multivibrator will




(a)

**Figure 17.24** **(a)** Connecting a bistable multivibrator with inverting transfer characteristics in a feedback loop with an RC circuit results in a square-wave generator.

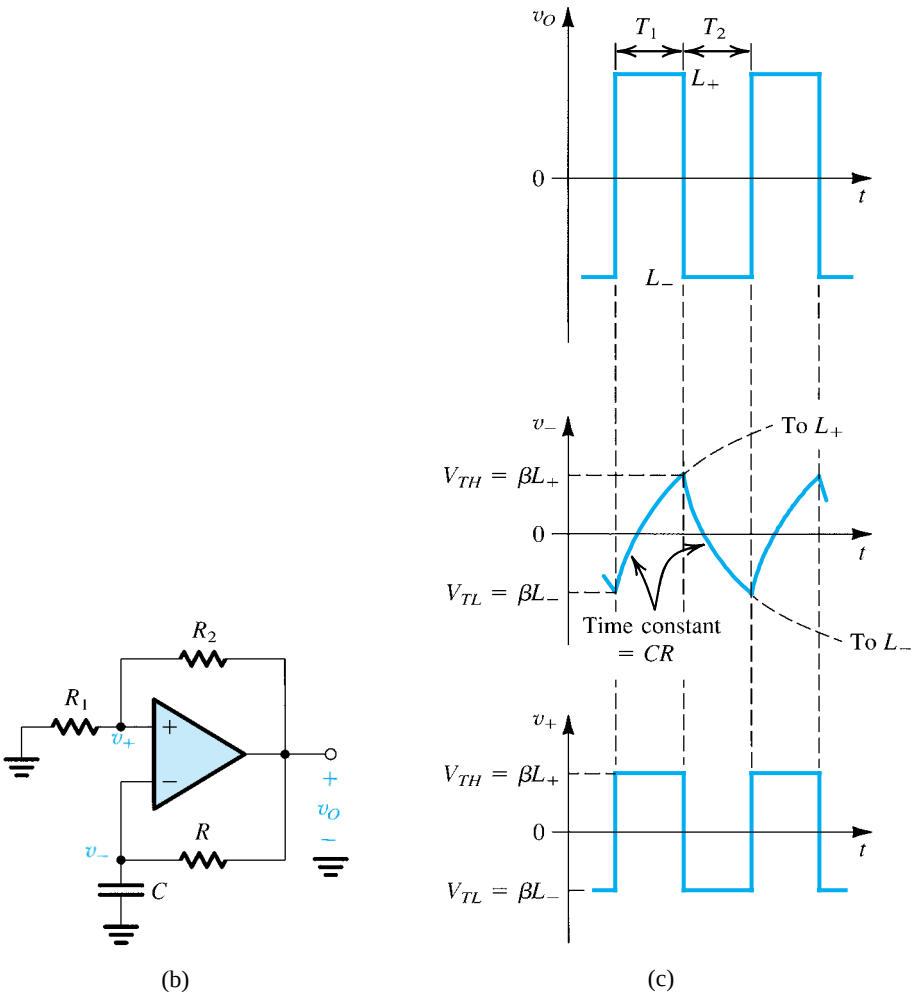



**Figure 17.24** (*Continued*) **(b)** The circuit obtained when the bistable multivibrator is implemented with the circuit of Fig. 17.19(a). **(c)** Waveforms at various nodes of the circuit in **(b)**. This circuit is called an astable multivibrator.

switch to the other stable, state, in which $v_O = L_-$ and $v_+ = \beta L_-$. The capacitor will then start discharging, and its voltage, $v_-$, will decrease exponentially toward $L_-$. This new state will prevail until $v_-$ reaches the negative threshold $V_{TL} = \beta L_-$, at which time the bistable multivibrator switches to the positive-output state, the capacitor begins to charge, and the cycle repeats itself.

From the preceding description we see that the astable circuit oscillates and produces a square waveform at the output of the op amp. This waveform, and the waveforms at the two input terminals of the op amp, are displayed in Fig. 17.24(c). The period $T$ of the square wave can be found as follows: During the charging interval $T_1$ the voltage $v_-$ across the capacitor at any time $t$, with $t = 0$ at the beginning of $T_1$, is given by (see Appendix E)

$$v_- = L_+ - (L_+ - \beta L_-)e^{-t/\tau}$$

where $\tau = CR$. Substituting $v_- = \beta L_+$ at $t = T_1$ gives

$$T_1 = \tau \ln \frac{1 - \beta(L_-/L_+)}{1 - \beta} \tag{17.31}$$

Similarly, during the discharge interval $T_2$ the voltage $v_-$ at any time $t$, with $t = 0$ at the beginning of $T_2$, is given by

$$v_- = L_- - (L_- - \beta L_+)e^{-t/\tau}$$

Substituting $v_- = \beta L_-$ at $t = T_2$ gives

$$T_2 = \tau \ln \frac{1 - \beta(L_+/L_-)}{1 - \beta} \tag{17.32}$$

Equations (17.31) and (17.32) can be combined to obtain the period $T = T_1 + T_2$. Normally, $L_+ = -L_-$, resulting in symmetrical square waves of period $T$ given by

$$T = 2\tau \ln \frac{1 + \beta}{1 - \beta} \tag{17.33}$$

Note that this square-wave generator can be made to have variable frequency by switching different capacitors $C$ (usually in decades) and by continuously adjusting $R$ (to obtain continuous frequency control within each decade of frequency). Also, the waveform across $C$ can be made almost triangular by using a small value for the parameter $\beta$. However, triangular waveforms of superior linearity can be easily generated using the scheme discussed next.

Before leaving this section, however, note that although the astable circuit has no stable states, it has two *quasi-stable* states and remains in each for a time interval determined by the time constant of the RC network and the thresholds of the bistable multivibrator.

## EXERCISES

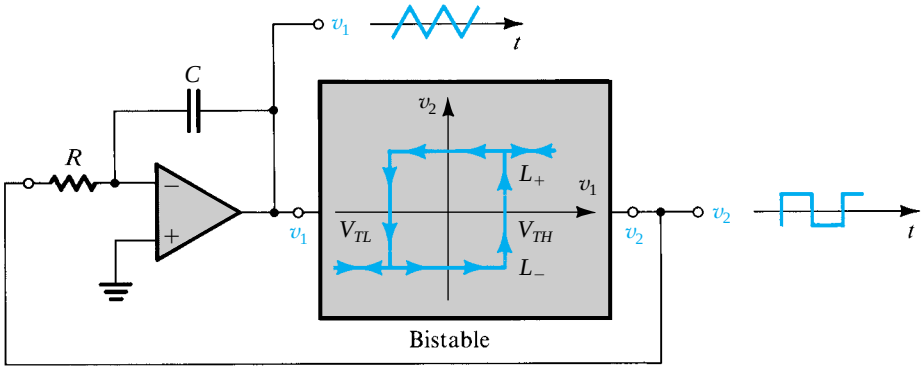
**17.16** For the circuit in Fig. 17.24(b), let the op-amp saturation voltages be ±10 V, $R_1$ =100 kΩ, $R_2 = R = 1$ MΩ, and $C = 0.01$ μF. Find the frequency of oscillation.
**Ans.** 274 Hz

**17.17** Consider a modification of the circuit of Fig. 17.24(b) in which $R_1$ is replaced by a pair of diodes connected in parallel in opposite directions. For $L_+ = -L_- = 12$ V, $R_2 = R = 10$ kΩ, $C = 0.1$ μF, and the diode voltage as a constant denoted $V_D$, find an expression for frequency as a function of $V_D$. If $V_D = 0.70$ V at 25°C with a $TC$ of –2 mV/°C, find the frequency at 0°C, 25°C, 50°C, and 100°C. Note that the output of this circuit can be sent to a remotely connected frequency meter to provide a digital readout of temperature.
**Ans.** $f = 500/\ln[(12 + V_D)/(12 - V_D)]$ Hz; 3995 Hz, 4281 Hz, 4611 Hz, 5451 Hz

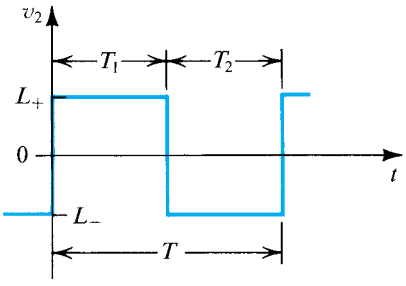
## 17.5.2 Generation of Triangular Waveforms

The exponential waveforms generated in the astable circuit of Fig. 17.24 can be changed to triangular by replacing the low-pass RC circuit with an integrator. (The integrator is, after all, a low-pass circuit with a corner frequency at dc.) The integrator causes linear charging and discharging of the capacitor, thus providing a triangular waveform. The resulting circuit is shown in Fig. 17.25(a). Observe that because the integrator is inverting, it is necessary to invert the characteristics of the bistable circuit. Thus the bistable circuit required here is of the noninverting type and can be implemented using the circuit of Fig. 17.20.

We now proceed to show how the feedback loop of Fig. 17.25(a) oscillates and generates a triangular waveform $v_1$ at the output of the integrator and a square waveform $v_2$ at the output of the bistable circuit: Let the output of the bistable circuit be at $L_+$. A current equal to $L_+/R$ will flow into the resistor $R$ and through capacitor $C$, causing the output of the integrator to *linearly* decrease with a slope of $-L_+/CR$, as shown in Fig. 17.25(c). This will continue until the integrator output reaches the lower threshold $V_{TL}$ of the bistable circuit, at which point the bistable circuit will switch states, its output becoming negative and equal to $L_-$. At this moment the current through $R$ and $C$ will reverse direction, and its value will become equal to $|L_-|/R$. It follows that the integrator output will start to increase linearly with a positive slope equal to $|L_-|/CR$. This will continue until the integrator output voltage reaches the positive threshold of the bistable circuit, $V_{TH}$. At this point the bistable circuit




(a)

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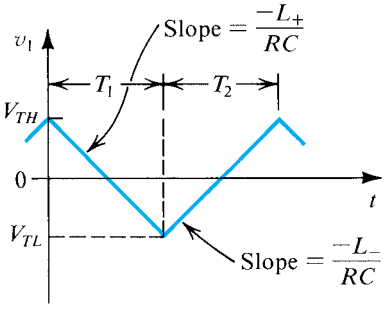



(c)

**Figure 17.25** A general scheme for generating triangular and square waveforms.

switches, its output becomes positive ($L_+$), the current into the integrator reverses direction, and the output of the integrator starts to decrease linearly, beginning a new cycle.

From the discussion above, it is relatively easy to derive an expression for the period $T$ of the square and triangular waveforms. During the interval $T_1$ we have, from Fig. 17.25(c),

$$\frac{V_{TH} - V_{TL}}{T_1} = \frac{L_+}{CR}$$

from which we obtain

$$T_1 = CR\frac{V_{TH} - V_{TL}}{L_+} \tag{17.34}$$

Similarly, during $T_2$ we have

$$\frac{V_{TH} - V_{TL}}{T_2} = \frac{-L_-}{CR}$$

from which we obtain

$$T_2 = CR\frac{V_{TH} - V_{TL}}{-L_-} \tag{17.35}$$

Thus to obtain symmetrical square waves we design the bistable circuit to have $L_+ = -L_-$.

## EXERCISES

**D17.18** Consider the circuit of Fig. 17.25(a) with the bistable circuit realized by the circuit in Fig. 17.20(a). If the op amps have saturation voltages of ±10 V, and if a capacitor $C = 0.01$ μF and a resistor $R_1 = 10$ kΩ are used, find the values of $R$ and $R_2$ (note that $R_1$ and $R_2$ are associated with the bistable circuit of Fig. 17.20a) such that the frequency of oscillation is 1 kHz and the triangular waveform has a 10-V peak-to-peak amplitude.

**Ans.** 50 kΩ; 20 kΩ

## 17.6 Generation of a Standardized Pulse—The Monostable Multivibrator

In some applications the need arises for a pulse of known height and width generated in response to a trigger signal. Because the width of the pulse is predictable, its trailing edge can be used for timing purposes—that is, to initiate a particular task at a specified time. Such a standardized pulse can be generated by the third type of multivibrator, the **monostable multivibrator**.

The monostable multivibrator has one stable state in which it can remain indefinitely. It also has a quasi-stable state to which it can be triggered and in which it stays for a predetermined interval equal to the desired width of the output pulse. When this interval expires, the monostable multivibrator returns to its stable state and remains there, awaiting another triggering signal. The action of the monostable multivibrator has given rise to its alternative name, the *one shot*.

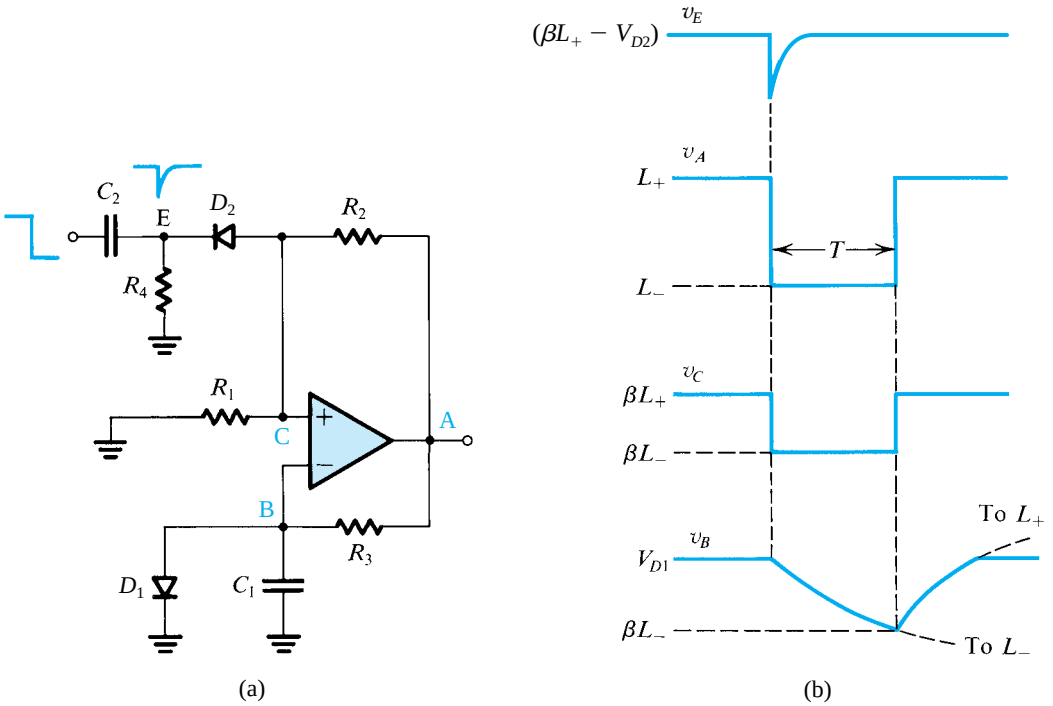



**Figure 17.26** **(a)** An op-amp monostable circuit. **(b)** Signal waveforms in the circuit of **(a)**.

Figure 17.26(a) shows an op-amp monostable circuit. We observe that this circuit is an augmented form of the astable circuit of Fig. 17.24(b). Specifically, a clamping diode $D_1$ is added across the capacitor $C_1$, and a trigger circuit composed of capacitor $C_2$, resistor $R_4$, and diode $D_2$ is connected to the noninverting input terminal of the op amp. The circuit operates as follows: In the stable state, which prevails in the absence of the triggering signal, the output of the op amp is at $L_+$ and diode $D_1$ is conducting through $R_3$ and thus clamping the voltage $v_B$ to one diode drop above ground. We select $R_4$ much larger than $R_1$, so that diode $D_2$ will be conducting a very small current and the voltage $v_C$ will be very closely determined by the voltage divider $R_1$, $R_2$. Thus $v_C = \beta L_+$, where $\beta = R_1/(R_1 + R_2)$. The stable state is maintained because $\beta L_+$ is greater than $V_{D1}$.

Now consider the application of a negative-going step at the trigger input and refer to the signal waveforms shown in Fig. 17.26(b). The negative triggering edge is coupled to the cathode of diode $D_2$ via capacitor $C_2$, and thus $D_2$ conducts heavily and pulls node C down. If the trigger signal is of sufficient height to cause $v_C$ to go below $v_B$, the op amp will see a net negative input voltage and its output will switch to $L_-$. This in turn will cause $v_C$ to go negative to $\beta L_-$, keeping the op amp in its newly acquired state. Note that $D_2$ will then cut off, thus isolating the circuit from any further changes at the trigger input terminal.

The negative voltage at A causes $D_1$ to cut off, and $C_1$ begins to discharge exponentially toward $L_-$ with a time constant $C_1R_3$. The monostable multivibrator is now in its *quasi-stable state*, which will prevail until the declining $v_B$ goes below the voltage at node C, which is $\beta L_-$. At this instant the op-amp output switches back to $L_+$ and the voltage at node C goes back to $\beta L_+$. Capacitor $C_1$ then charges toward $L_+$ until diode $D_1$ turns on and the circuit returns to its stable state.

From Fig. 17.26(b), we observe that a negative pulse is generated at the output during the quasi-stable state. The duration $T$ of the output pulse is determined from the exponential waveform of $v_B$,

$$v_B(t) = L_- - (L_- - V_{D1})e^{-t/C_1R_3}$$

by substituting $v_B(T) = \beta L_-$,

$$\beta L_- = L_- - (L_- - V_{D1})e^{-T/C_1R_3}$$

which yields

$$T = C_1R_3 \ln\left(\frac{V_{D1} - L_-}{\beta L_- - L_-}\right) \tag{17.36}$$

For $V_{D1} \ll |L_-|$, this equation can be approximated by

$$T \simeq C_1R_3 \ln\left(\frac{1}{1-\beta}\right) \tag{17.37}$$

Finally, note that the monostable circuit should not be triggered again until capacitor $C_1$ has been recharged to $V_{D1}$; otherwise the resulting output pulse will be shorter than normal. This recharging time is known as the **recovery period**. Circuit techniques exist for shortening the recovery period.

## EXERCISES

**17.19** For the monostable circuit of Fig. 17.26(a), find the value of $R_3$ that will result in a 100-μs output pulse for $C_1 = 0.1$ μF, $\beta = 0.1$, $V_D = 0.7$ V, and $L_+ = -L_- = 12$ V.
**Ans.** 6171 Ω

## 17.7 Integrated-Circuit Timers

Commercially available integrated-circuit packages exist that contain the bulk of the circuitry needed to implement monostable and astable multivibrators with precise characteristics. In this section we discuss the most popular of such ICs, the **555 timer**. Introduced in 1972 by the Signetics Corporation as a bipolar integrated circuit, the 555 is also available in CMOS technology and from a number of manufacturers.[6]

### 17.7.1 The 555 Circuit

Figure 17.27 shows a block diagram representation of the 555 timer circuit [for the actual circuit, refer to Grebene (1984)]. The circuit consists of two comparators, an SR flip-flop, and a transistor $Q_1$ that operates as a switch. One power supply ($V_{CC}$) is required for operation, with the supply voltage typically 5 V. A resistive voltage divider, consisting of the three

[6] In a recent article in *IEEE Spectrum* (May 2009), the 555 was selected as one of the "25 Microchips That Shook the World."

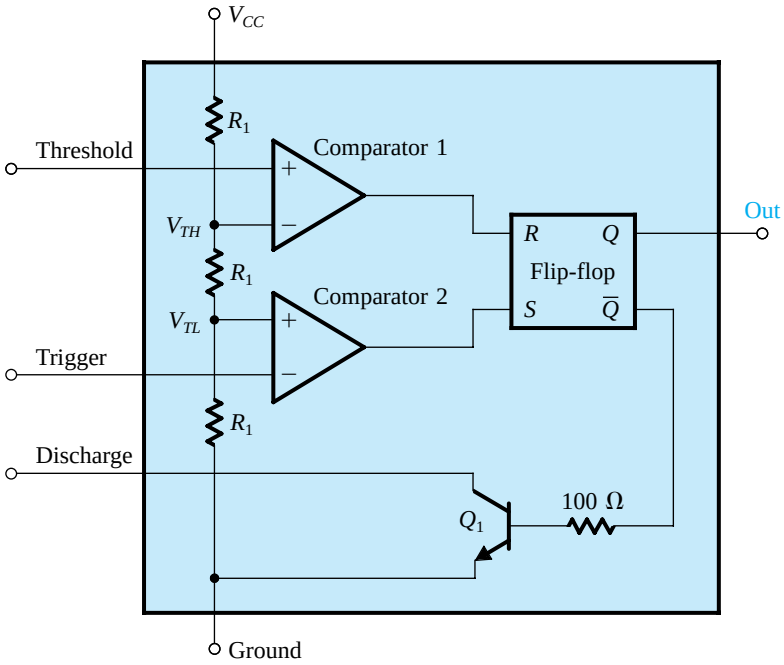



**Figure 17.27** A block diagram representation of the internal circuit of the 555 integrated-circuit timer.

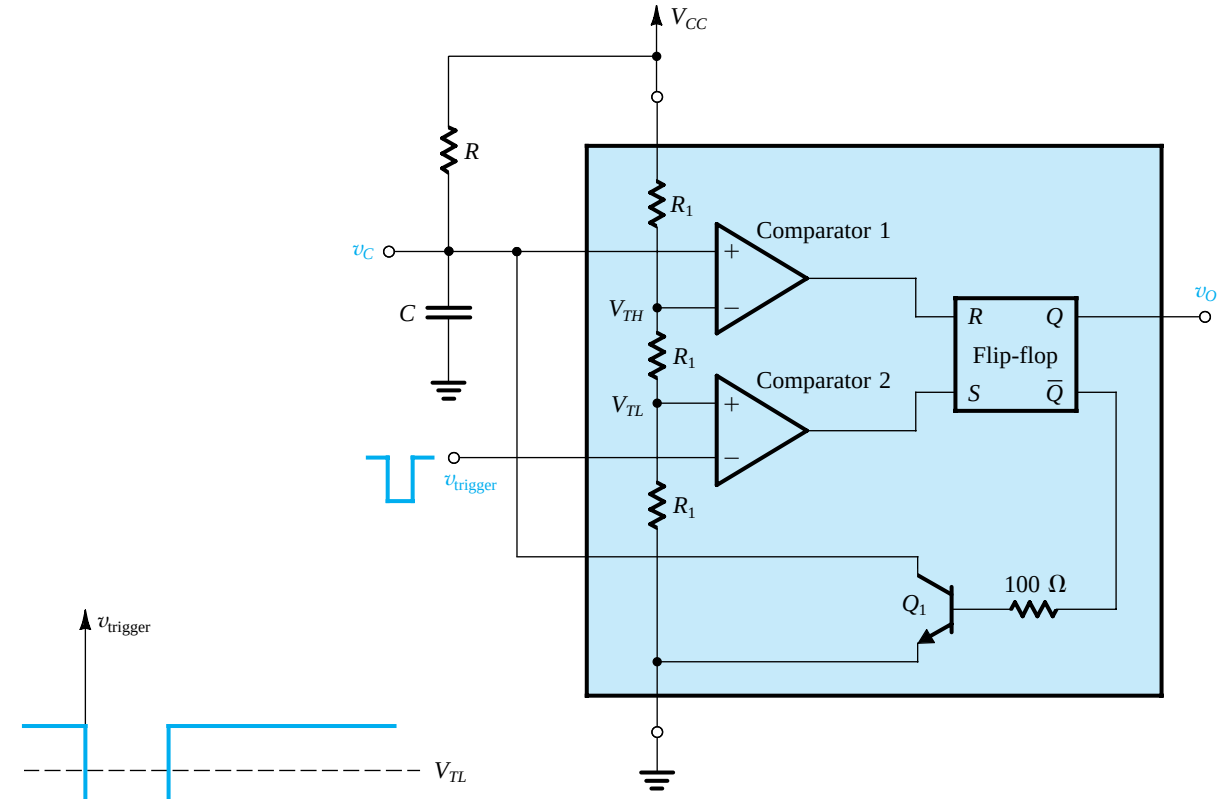
equal-valued resistors labeled $R_1$, is connected across $V_{CC}$ and establishes the reference (threshold) voltages for the two comparators. These are $V_{TH} = \frac{2}{3}V_{CC}$ for comparator 1 and $V_{TL} = \frac{1}{3}V_{CC}$ for comparator 2.

We studied SR flip-flops in Chapter 15. For our purposes here we note that an SR flip-flop is a bistable circuit having complementary outputs, denoted $Q$ and $\overline{Q}$. In the *set* state, the output at $Q$ is "high" (approximately equal to $V_{CC}$) and that at $\overline{Q}$ is "low" (approximately equal to 0 V). In the other stable state, termed the *reset* state, the output at $Q$ is low and that at $\overline{Q}$ is high. The flip-flop is set by applying a high level ($V_{CC}$) to its set input terminal, labeled $S$. To reset the flip-flop, a high level is applied to the reset input terminal, labeled $R$. Note that the reset and set input terminals of the flip-flop in the 555 circuit are connected to the outputs of comparator 1 and comparator 2, respectively.

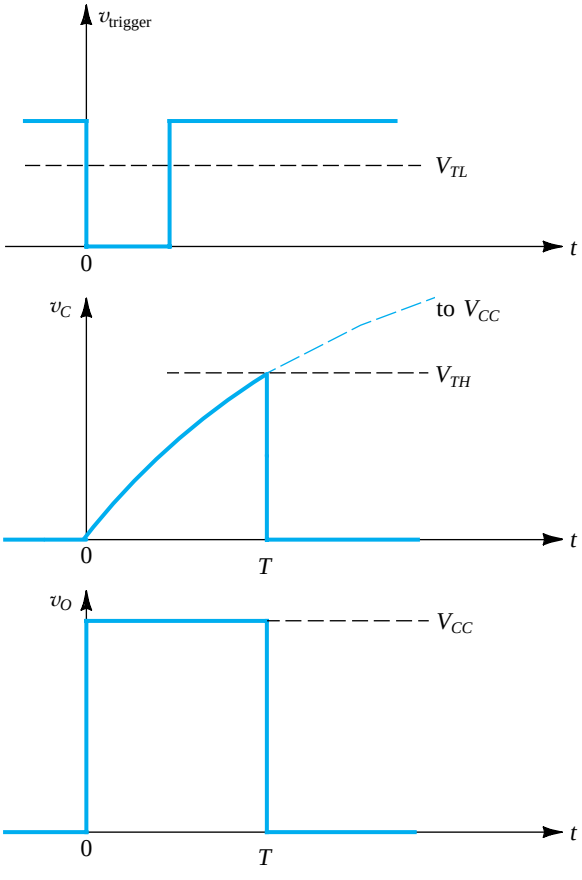
The positive-input terminal of comparator 1 is brought out to an external terminal of the 555 package, labeled Threshold. Similarly, the negative-input terminal of comparator 2 is connected to an external terminal labeled Trigger, and the collector of transistor $Q_1$ is connected to a terminal labeled Discharge. Finally, the $Q$ output of the flip-flop is connected to the output terminal of the timer package, labeled Out.

## 17.7.2 Implementing a Monostable Multivibrator Using the 555 IC

Figure 17.28(a) shows a monostable multivibrator implemented using the 555 IC together with an external resistor $R$ and an external capacitor $C$. In the stable state the flip-flop will be in the reset state, and thus its $\overline{Q}$ output will be high, turning on transistor $Q_1$. Transistor $Q_1$ will be saturated, and thus $v_C$ will be close to 0 V, resulting in a low level at the output of comparator 1. The voltage at the trigger input terminal, labeled $v_{\text{trigger}}$, is kept high (greater than $V_{TL}$), and thus the output of comparator 2 also will be low. Finally, note that since the flip-flop is in the reset state, $Q$ will be low and thus $v_O$ will be close to 0 V.




(a)




(b)

**Figure 17.28** **(a)** The 555 timer connected to implement a monostable multivibrator. **(b)** Waveforms of the circuit in **(a)**.

To trigger the monostable multivibrator, a negative input pulse is applied to the trigger input terminal. As $v_{\text{trigger}}$ goes below $V_{TL}$, the output of comparator 2 goes to the high level, thus setting the flip-flop. Output $Q$ of the flip-flop goes high, and thus $v_O$ goes high, and output $\overline{Q}$ goes low, turning off transistor $Q_1$. Capacitor $C$ now begins to charge up through resistor $R$, and its voltage $v_C$ rises exponentially toward $V_{CC}$, as shown in Fig. 17.28(b). The monostable multivibrator is now in its quasi-stable state. This state prevails until $v_C$ reaches and begins to exceed the threshold of comparator 1, $V_{TH}$, at which time the output of comparator 1 goes high, resetting the flip-flop. Output $\overline{Q}$ of the flip-flop now goes high and turns on transistor $Q_1$. In turn, transistor $Q_1$ rapidly discharges capacitor $C$, causing $v_C$ to go to 0 V. Also, when the flip-flop is reset, its $Q$ output goes low, and thus $v_O$ goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.

From the description above we see that the monostable multivibrator produces an output pulse $v_O$ as indicated in Fig. 17.28(b). The width of the pulse, $T$, is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 17.28(b) as follows: Denoting the instant at which the trigger pulse is applied as $t = 0$, the exponential waveform of $v_C$ can be expressed as

$$v_C = V_{CC}(1 - e^{-t/CR}) \tag{17.38}$$

Substituting $v_C = V_{TH} = \frac{2}{3}V_{CC}$ at $t = T$ gives

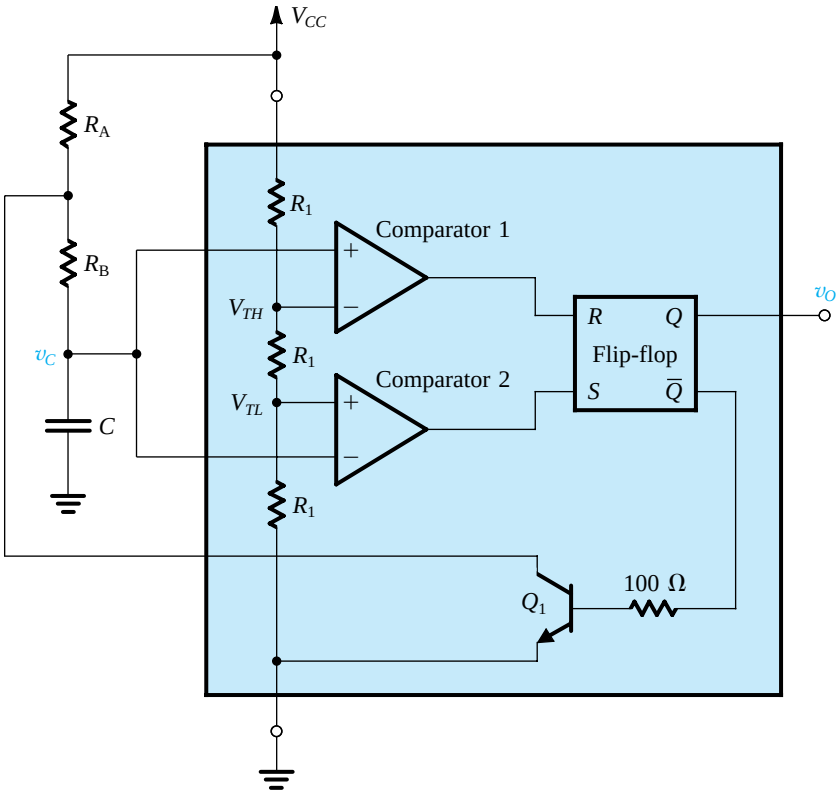
$$T = CR \ln 3 \simeq 1.1CR \tag{17.39}$$

Thus the pulse width is determined by the external components $C$ and $R$, which can be selected to have values as precise as desired.

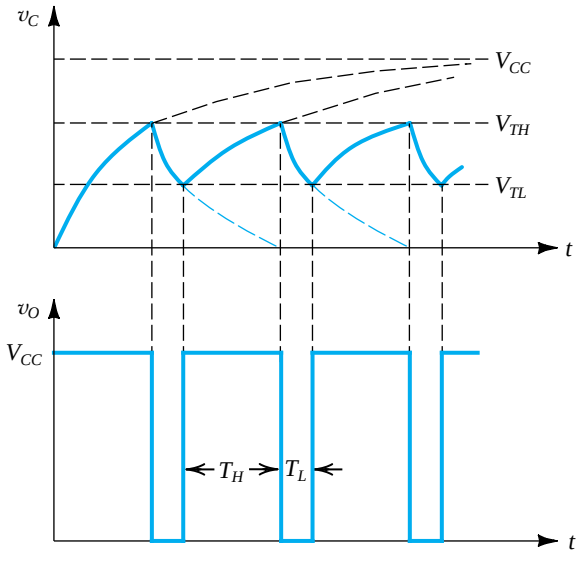
### 17.7.3 An Astable Multivibrator Using the 555 IC

Figure 17.29(a) shows the circuit of an astable multivibrator employing a 555 IC, two external resistors, $R_A$ and $R_B$, and an external capacitor $C$. To see how the circuit operates, refer to the waveforms depicted in Fig. 17.29(b). Assume that initially $C$ is discharged and the flip-flop is set. Thus $v_O$ is high and $Q_1$ is off. Capacitor $C$ will charge up through the series combination of $R_A$ and $R_B$, and the voltage across it, $v_C$, will rise exponentially toward $V_{CC}$. As $v_C$ crosses the level equal to $V_{TL}$, the output of comparator 2 goes low. This, however, has no effect on the circuit operation, and the flip-flop remains set. Indeed, this state continues until $v_C$ reaches and begins to exceed the threshold of comparator 1, $V_{TH}$. At this instant of time, the output of comparator 1 goes high and resets the flip-flop. Thus $v_O$ goes low, $\overline{Q}$ goes high, and transistor $Q_1$ is turned on. The saturated transistor $Q_1$ causes a voltage of approximately zero volts to appear at the common node of $R_A$ and $R_B$. Thus $C$ begins to discharge through $R_B$ and the collector of $Q_1$. The voltage $v_C$ decreases exponentially with a time constant $CR_B$ toward 0 V. When $v_C$ reaches the threshold of comparator 2, $V_{TL}$, the output of comparator 2, goes high and sets the flip-flop. The output $v_O$ then goes high, and $\overline{Q}$ goes low, turning off $Q_1$. Capacitor $C$ begins to charge through the series equivalent of $R_A$ and $R_B$, and its voltage rises exponentially toward $V_{CC}$ with a time constant $C(R_A + R_B)$. This rise continues until $v_C$ reaches $V_{TH}$, at which time the output of comparator 1 goes high, resetting the flip-flop, and the cycle continues.

From the description above we see that the circuit of Fig. 17.29(a) oscillates and produces a square waveform at the output. The frequency of oscillation can be determined as follows.




(a)




(b)

**Figure 17.29** **(a)** The 555 timer connected to implement an astable multivibrator. **(b)** Waveforms of the circuit in **(a)**.

Reference to Fig. 17.29(b) indicates that the output will be high during the interval $T_H$, in which $v_C$ rises from $V_{TL}$ to $V_{TH}$. The exponential rise of $v_C$ can be described by

$$v_C = V_{CC} - (V_{CC} - V_{TL})e^{-t/C(R_A+R_B)} \tag{17.40}$$

where $t = 0$ is the instant at which the interval $T_H$ begins. Substituting $v_C = V_{TH} = \frac{2}{3}V_{CC}$ at $t = T_H$ and $V_{TL} = \frac{1}{3}V_{CC}$ results in

$$T_H = C(R_A + R_B)\ln 2 \simeq 0.69\, C(R_A + R_B) \tag{17.41}$$

We also note from Fig. 17.29(b) that $v_O$ will be low during the interval $T_L$, in which $v_C$ falls from $V_{TH}$ to $V_{TL}$. The exponential fall of $v_C$ can be described by

$$v_C = V_{TH}e^{-t/CR_B} \tag{17.42}$$

where we have taken $t = 0$ as the beginning of the interval $T_L$. Substituting $v_C = V_{TL} = \frac{1}{3}V_{CC}$ at $t = T_L$ and $V_{TH} = \frac{2}{3}V_{CC}$ results in

$$T_L = CR_B \ln 2 \simeq 0.69\, CR_B \tag{17.43}$$

Equations (17.41) and (17.43) can be combined to obtain the period $T$ of the output square wave as

$$T = T_H + T_L = 0.69\, C(R_A + 2R_B) \tag{17.44}$$

Also, the **duty cycle** of the output square wave can be found from Eqs. (17.41) and (17.43):

$$\text{Duty cycle} \equiv \frac{T_H}{T_H + T_L} = \frac{R_A + R_B}{R_A + 2R_B} \tag{17.45}$$

Note that the duty cycle will always be greater than 0.5 (50%); it approaches 0.5 if $R_A$ is selected to be much smaller than $R_B$ (unfortunately, at the expense of supply current).

## EXERCISES

**17.20** Using a 10-nF capacitor $C$, find the value of $R$ that yields an output pulse of 100 μs in the monostable circuit of Fig. 17.28(a).
**Ans.** 9.1 kΩ

**D17.21** For the circuit in Fig. 17.29(a), with a 1-nF capacitor, find the values of $R_A$ and $R_B$ that result in an oscillation frequency of 100 kHz and a duty cycle of 75%.
**Ans.** 7.2 kΩ, 3.6 kΩ

## 17.8 Nonlinear Waveform-Shaping Circuits

Diodes or transistors can be combined with resistors to synthesize two-port networks having arbitrary nonlinear transfer characteristics. Such two-port networks can be employed in

**waveform shaping**—that is, changing the waveform of an input signal in a prescribed manner to produce a waveform of a desired shape at the output. In this section we illustrate this application by a concrete example: the **sine-wave shaper**. This is a circuit whose purpose is to change the waveform of an input triangular-wave signal to a sine wave. Though simple, the sine-wave shaper is a practical building block used extensively in function generators. This method of generating sine waves should be contrasted to that using linear oscillators (Sections 17.1–17.3). Although linear oscillators produce sine waves of high purity, they are not convenient at very low frequencies. Also, linear oscillators are in general more difficult to tune over wide frequency ranges. In the following we discuss two distinctly different techniques for designing sine-wave shapers.

## 17.8.1 The Breakpoint Method

In the breakpoint method the desired nonlinear transfer characteristic (in our case the sine function shown in Fig. 17.30) is implemented as a piecewise linear curve. Diodes are utilized as switches that turn on at the various breakpoints of the transfer characteristic, thus switching into the circuit additional resistors that cause the transfer characteristic to change slope.

Consider the circuit shown in Fig. 17.31(a). It consists of a chain of resistors connected across the entire symmetrical voltage supply $+V$, $-V$. The purpose of this voltage divider is to generate reference voltages that will serve to determine the breakpoints in the transfer characteristic. In our example these reference voltages are denoted $+V_2$, $+V_1$, $-V_1$, $-V_2$. Note that

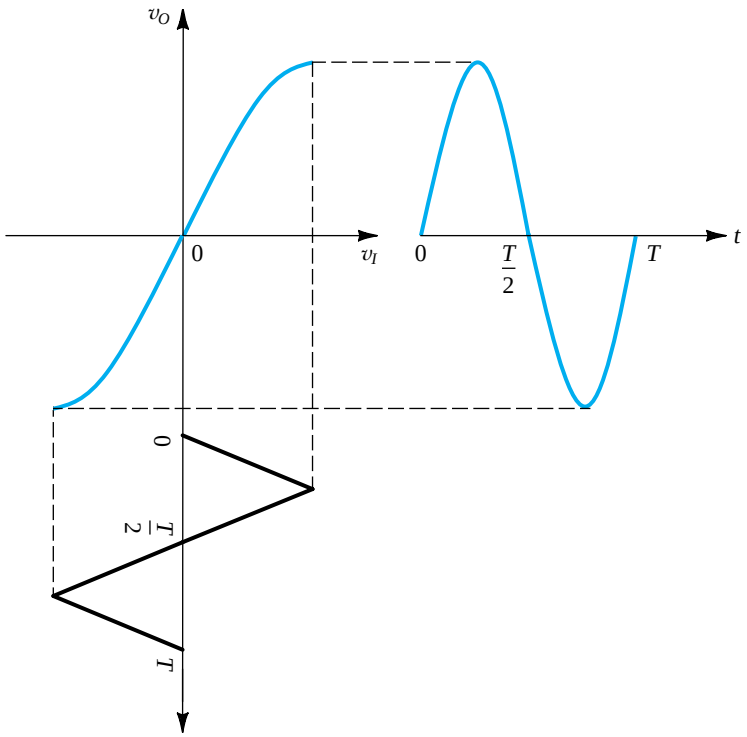



**Figure 17.30** Using a nonlinear (sinusoidal) transfer characteristic to shape a triangular waveform into a sinusoid.

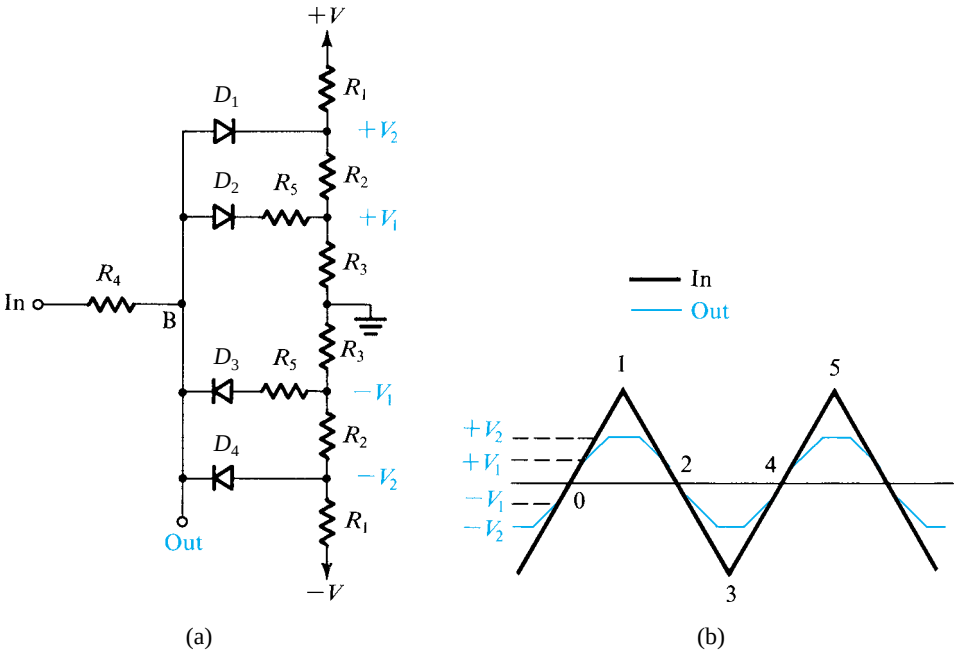



**Figure 17.31** **(a)** A three-segment sine-wave shaper. **(b)** The input triangular waveform and the output approximately sinusoidal waveform.

the entire circuit is symmetrical, driven by a symmetrical triangular wave and generating a symmetrical sine-wave output. The circuit approximates each quarter-cycle of the sine wave by three straight-line segments; the breakpoints between these segments are determined by the reference voltages $V_1$ and $V_2$.

The circuit works as follows: Let the input be the triangular wave shown in Fig. 17.31(b), and consider first the quarter-cycle defined by the two points labeled 0 and 1. When the input signal is less in magnitude than $V_1$, none of the diodes conducts. Thus zero current flows through $R_4$, and the output voltage at B will be equal to the input voltage. But as the input rises to $V_1$ and above, $D_2$ (assumed ideal) begins to conduct. Assuming that the conducting $D_2$ behaves as a short circuit, we see that, for $v_I > V_1$,

$$v_O = V_1 + (v_I - V_1)\frac{R_5}{R_4 + R_5}$$

This implies that as the input continues to rise above $V_1$, the output follows, but with a reduced slope. This gives rise to the second segment in the output waveform, as shown in Fig. 17.31(b). Note that in developing the equation above we have assumed that the resistances in the voltage divider are low enough in value to cause the voltages $V_1$ and $V_2$ to be constant independent of the current coming from the input.

Next consider what happens as the voltage at point B reaches the second breakpoint determined by $V_2$. At this point, $D_1$ conducts, thus limiting the output $v_O$ to $V_2$ (plus, of course, the voltage drop across $D_1$ if it is not assumed to be ideal). This gives rise to the third segment, which is flat, in the output waveform. The overall result is to "bend" the waveform and shape it into an approximation of the first quarter-cycle of a sine wave. Then, beyond the

peak of the input triangular wave, as the input voltage decreases, the process unfolds, the output becoming progressively more like the input. Finally, when the input goes sufficiently negative, the process begins to repeat at $-V_1$ and $-V_2$ for the negative half-cycle.

Although the circuit is relatively simple, its performance is surprisingly good. A measure of goodness usually taken is to quantify the purity of the output sine wave by specifying the percentage **total harmonic distortion** (THD). This is the percentage ratio of the rms voltage of all harmonic components above the fundamental frequency (which is the frequency of the triangular wave) to the rms voltage of the fundamental (see also Chapter 11). Interestingly, one reason for the good performance of the diode shaper is the beneficial effects produced by the nonideal $i$–$v$ characteristics of the diodes—that is, the exponential knee of the junction diode as it goes into forward conduction. The consequence is a relatively smooth transition from one line segment to the next.

Practical implementations of the breakpoint sine-wave shaper employ six to eight segments (compared with the three used in the example above). Also, transistors are usually employed to provide more versatility in the design, with the goal being increased precision and lower THD (see Grebene, 1984, pages 592–595).

## 17.8.2 The Nonlinear-Amplification Method

The other method we discuss for the conversion of a triangular wave into a sine wave is based on feeding the triangular wave to the input of an amplifier having a nonlinear transfer characteristic that approximates the sine function. One such amplifier circuit consists of a differential pair with a resistance connected between the two emitters, as shown in Fig. 17.32. With appropriate choice of the values of the bias current $I$ and the resistance $R$, the differential amplifier can be made to have a transfer characteristic that closely approximates that shown in Fig. 17.30. Observe that for small $v_I$ the transfer characteristic of the circuit of Fig. 17.32 is almost linear, as a sine waveform is near its zero crossings. At large values of $v_I$ the nonlinear characteristics of the BJTs reduce the gain of the amplifier and cause the transfer characteristic to bend, approximating the sine wave as it approaches its peak. (More details on this circuit can be found in Grebene, 1984, pages 595–597.)

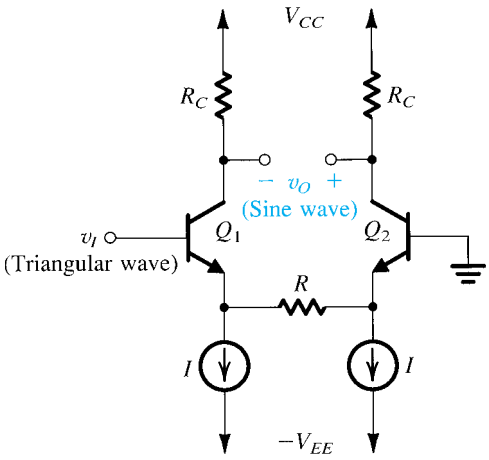



**Figure 17.32** A differential pair with an emitter-degeneration resistance used to implement a triangular-wave to sine-wave converter. Operation of the circuit can be graphically described by Fig. 17.30.

## EXERCISES

**D17.22** The circuit in Fig. E17.22 is required to provide a three-segment approximation to the nonlinear $i$–$v$ characteristic, $i = 0.1v^2$, where $v$ is the voltage in volts and $i$ is the current in milliamperes. Find the values of $R_1$, $R_2$, and $R_3$ such that the approximation is perfect at $v = 2$ V, 4 V, and 8 V. Calculate the error in current value at $v = 3$ V, 5 V, 7 V, and 10 V. Assume ideal diodes.

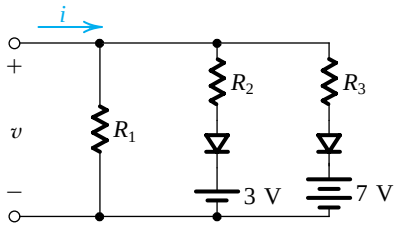



**Figure E17.22**

**Ans.** 5 kΩ, 1.25 kΩ, 1.25 kΩ; –0.3 mA, +0.1 mA, –0.3 mA, 0

**17.23** A detailed analysis of the circuit in Fig. 17.32 shows that its optimum performance occurs when the values of $I$ and $R$ are selected so that $RI = 2.5V_T$, where $V_T$ is the thermal voltage. For this design, the peak amplitude of the input triangular wave should be $6.6V_T$, and the corresponding sine wave across $R$ has a peak value of $2.42V_T$. For $I = 0.25$ mA and $R_C = 10$ kΩ, find the peak amplitude of the sine-wave output $v_O$. Assume $\alpha \simeq 1$.

**Ans.** 4.84 V

# 17.9 Precision Rectifier Circuits

Rectifier circuits were studied in Chapter 4, where the emphasis was on their application in power-supply design. In such applications, the voltages being rectified are usually much greater than the diode voltage drop, rendering the exact value of the diode drop unimportant to the proper operation of the rectifier. Other applications exist, however, where this is not the case. For instance, in instrumentation applications, the signal to be rectified can be of a very small amplitude, say 0.1 V, making it impossible to employ the conventional rectifier circuits. Also, in instrumentation applications, the need arises for rectifier circuits with very precise transfer characteristics.

In this section we study circuits that combine diodes and op amps to implement a variety of rectifier circuits with precise characteristics. Precision rectifiers, which can be considered a special class of wave-shaping circuits, find application in the design of instrumentation systems. An introduction to precision rectifiers was presented in Chapter 4. This material, however, is repeated here for the reader's convenience.

## 17.9.1 Precision Half-Wave Rectifier—The "Superdiode"

Figure 17.33(a) shows a precision half-wave-rectifier circuit consisting of a diode placed in the negative-feedback path of an op amp, with $R$ being the rectifier load resistance. The circuit works as follows: If $v_I$ goes positive, the output voltage $v_A$ of the op amp will go positive and the diode will conduct, thus establishing a closed feedback path between the op amp's output terminal and the negative input terminal. This negative-feedback path will

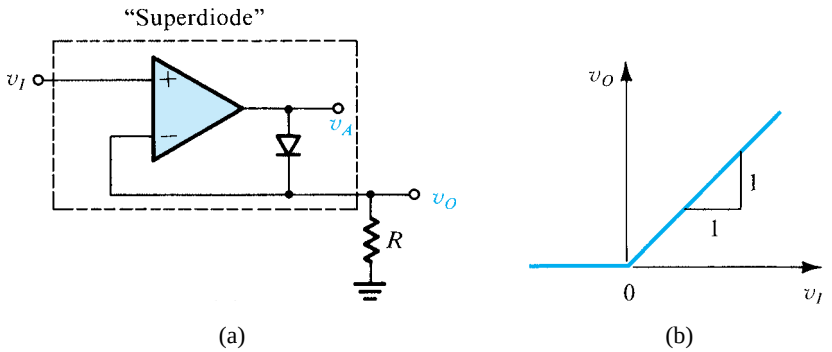



**Figure 17.33** **(a)** The "superdiode" precision half-wave rectifier; **(b)** its almost ideal transfer characteristic. Note that when $v_I > 0$ and the diode conducts, the op amp supplies the load current, and the source is conveniently buffered, an added advantage.

cause a virtual short circuit to appear between the two input terminals of the op amp. Thus the voltage at the negative input terminal, which is also the output voltage $v_O$, will equal (to within a few millivolts) that at the positive input terminal, which is the input voltage $v_I$,

$$v_O = v_I \quad v_I \geq 0$$

Note that the offset voltage ($\simeq 0.5$ V) exhibited in the simple half-wave-rectifier circuit is no longer present. For the op-amp circuit to start operation, $v_I$ has to exceed only a negligibly small voltage equal to the diode drop divided by the op amp's open-loop gain. In other words, the straight-line transfer characteristic $v_O$–$v_I$ almost passes through the origin. This makes this circuit suitable for applications involving very small signals.

Consider now the case when $v_I$ goes negative. The op amp's output voltage $v_A$ will tend to follow and go negative. This will reverse-bias the diode, and no current will flow through resistance $R$, causing $v_O$ to remain equal to 0 V. Thus for $v_I < 0$, $v_O = 0$. Since in this case the diode is off, the op amp will be operating in an open-loop fashion and its output will be at the negative saturation level.

The transfer characteristic of this circuit will be that shown in Fig. 17.33(b), which is almost identical to the ideal characteristic of a half-wave rectifier. The nonideal diode characteristics have been almost completely masked by placing the diode in the negative-feedback path of an op amp. This is another dramatic application of negative feedback. The combination of diode and op amp, shown in the dashed box in Fig. 17.33(a), is appropriately referred to as a "superdiode."

As usual, though, not all is well. The circuit of Fig. 17.33 has some disadvantages: When $v_I$ goes negative and $v_O = 0$, the entire magnitude of $v_I$ appears between the two input terminals of the op amp. If this magnitude is greater than a few volts, the op amp may be damaged unless it is equipped with what is called "overvoltage protection" (a feature that most modern IC op amps have). Another disadvantage is that when $v_I$ is negative, the op amp will be saturated. Although not harmful to the op amp, saturation should usually be avoided, since getting the op amp out of the saturation region and back into its linear region of operation requires some time. This time delay will obviously slow down circuit operation and limit the frequency of operation of the superdiode half-wave-rectifier circuit.

## 17.9.2 An Alternative Circuit

An alternative precision rectifier circuit that does not suffer from the disadvantages mentioned above is shown in Fig. 17.34. The circuit operates in the following manner: For

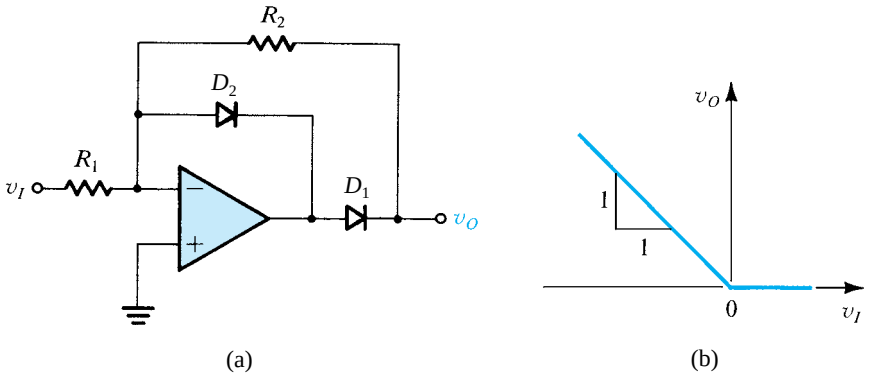



**Figure 17.34** **(a)** An improved version of the precision half-wave rectifier: Diode $D_2$ is included to keep the feedback loop closed around the op amp during the off times of the rectifier diode $D_1$, thus preventing the op amp from saturating. **(b)** The transfer characteristic for $R_2 = R_1$.

positive $v_I$, diode $D_2$ conducts and closes the negative-feedback loop around the op amp. A virtual ground therefore will appear at the inverting input terminal, and the op amp's output will be *clamped* at one diode drop below ground. This negative voltage will keep diode $D_1$ off, and no current will flow in the feedback resistance $R_2$. It follows that the rectifier output voltage will be zero.

As $v_I$ goes negative, the voltage at the inverting input terminal will tend to go negative, causing the voltage at the op amp's output terminal to go positive. This will cause $D_2$ to be reverse-biased and hence to be cut off. Diode $D_1$, however, will conduct through $R_2$, thus establishing a negative-feedback path around the op amp and forcing a virtual ground to appear at the inverting input terminal. The current through the feedback resistance $R_2$ will be equal to the current through the input resistance $R_1$. Thus for $R_1 = R_2$ the output voltage $v_O$ will be

$$v_O = -v_I \quad v_I \leq 0$$

The transfer characteristic of the circuit is shown in Fig. 17.34(b). Note that unlike the situation for the circuit shown in Fig. 17.33, here the slope of the characteristic can be set to any desired value, including unity, by selecting appropriate values for $R_1$ and $R_2$.

As mentioned before, the major advantage of the improved half-wave-rectifier circuit is that the feedback loop around the op amp remains closed at all times. Hence the op amp remains in its linear operating region, avoiding the possibility of saturation and the associated time delay required to "get out" of saturation. Diode $D_2$ "catches" the op-amp output voltage as it goes negative and clamps it to one diode drop below ground; hence $D_2$ is called a "catching diode."

### 17.9.3 An Application: Measuring AC Voltages

As one of the many possible applications of the precision rectifier circuits discussed in this section, consider the basic ac voltmeter circuit shown in Fig. 17.35. The circuit consists of a half-wave rectifier—formed by op amp $A_1$, diodes $D_1$ and $D_2$, and resistors $R_1$ and $R_2$—and a first-order low-pass filter—formed by op amp $A_2$, resistors $R_3$ and $R_4$, and capacitor $C$. For an input sinusoid having a peak amplitude $V_p$ the output $v_1$ of the rectifier will consist of a half sine wave having a peak amplitude of $V_p R_2/R_1$ . It can be shown using Fourier series analysis that the waveform of $v_1$ has an average value of $(V_p/\pi)(R_2/R_1)$ in addition to

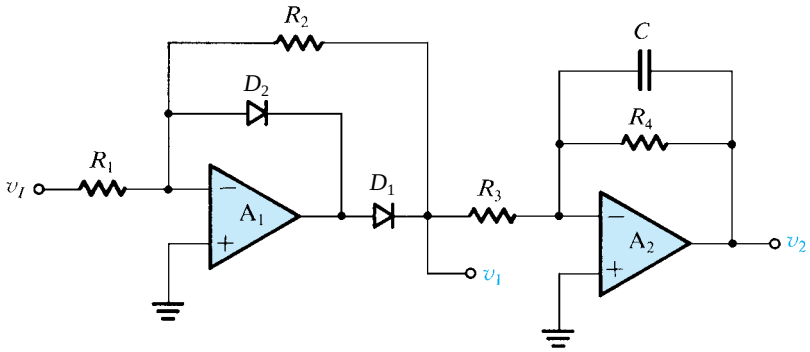



**Figure 17.35** A simple ac voltmeter consisting of a precision half-wave rectifier followed by a first-order low-pass filter.

## EXERCISES

**17.24** Consider the operational rectifier or superdiode circuit of Fig. 17.33(a), with $R = 1$ kΩ. For $v_I = 10$ mV, 1 V, and −1 V, what are the voltages that result at the rectifier output and at the output of the op amp? Assume that the op amp is ideal and that its output saturates at ±12 V. The diode has a 0.7-V drop at 1-mA current, and the voltage drop changes by 0.1 V per decade of current change.
**Ans.** 10 mV, 0.51 V; 1 V, 1.7 V; 0 V, –12 V

**17.25** If the diode in the circuit of Fig. 17.33(a) is reversed, what is the transfer characteristic $v_O$ as a function of $v_I$?
**Ans.** $v_O = 0$ for $v_I \geq 0$; $v_O = v_I$ for $v_I \leq 0$

**17.26** Consider the circuit in Fig. 17.34(a) with $R_1 = 1$ kΩ and $R_2 = 10$ kΩ. Find $v_O$ and the voltage at the amplifier output for $v_I = +1$ V, −10 mV, and −1 V. Assume the op amp to be ideal with saturation voltages of ±12 V. The diodes have 0.7-V voltage drops at 1 mA, and the voltage drop changes by 0.1 V per decade of current change.
**Ans.** 0 V, –0.vm7 V; 0.1 V, 0.6 V; 10 V, 10.7 V

**17.27** If the diodes in the circuit of Fig. 17.34(a) are reversed, what is the transfer characteristic $v_O$ as a function of $v_I$?
**Ans.** $v_O = -(R_2/R_1)v_I$ for $v_I \geq 0$; $v_O = 0$ for $v_I \leq 0$

**17.28** Find the transfer characteristic for the circuit in Fig. E17.28.

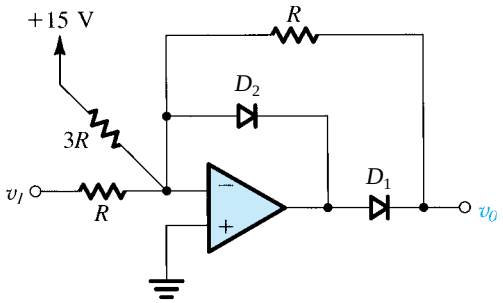



**Figure E17.28**

**Ans.** $v_O = 0$ for $v_I \geq -5$ V; $v_O = -v_I - 5$ for $v_I \leq -5$ V

harmonics of the frequency $\omega$ of the input signal. To reduce the amplitudes of all these harmonics to negligible levels, the corner frequency of the low-pass filter should be chosen to be much smaller than the lowest expected frequency $\omega_{\text{min}}$ of the input sine wave. This leads to

$$\frac{1}{CR_4} \ll \omega_{\text{min}}$$

Then the output voltage $v_2$ will be mostly dc, with a value

$$V_2 = -\frac{V_p}{\pi}\frac{R_2}{R_1}\frac{R_4}{R_3}$$

where $R_4/R_3$ is the dc gain of the low-pass filter. Note that this voltmeter essentially measures the average value of the negative parts of the input signal but can be calibrated to provide rms readings for input sinusoids.

### 17.9.4 Precision Full-Wave Rectifier

We now derive a circuit for a precision full-wave rectifier. From Chapter 4 we know that full-wave rectification is achieved by inverting the negative halves of the input-signal waveform and applying the resulting signal to another diode rectifier. The outputs of the two rectifiers are then joined to a common load. Such an arrangement is depicted in Fig. 17.36, which also shows the waveforms at various nodes. Now replacing diode $D_A$ with a superdiode, and replacing diode $D_B$ and the inverting amplifier with the inverting precision half-wave rectifier of Fig. 17.34 but without the catching diode, we obtain the precision full-wave-rectifier circuit of Fig. 17.37(a).

To see how the circuit of Fig. 17.37(a) operates, consider first the case of positive input at A. The output of $A_2$ will go positive, turning $D_2$ on, which will conduct through $R_L$ and thus close the feedback loop around $A_2$. A virtual short circuit will thus be established between the two input terminals of $A_2$, and the voltage at the negative-input terminal, which is the output voltage of the circuit, will become equal to the input. Thus no current will flow through $R_1$ and $R_2$, and the voltage at the inverting input of $A_1$ will be equal to the input and hence positive. Therefore the output terminal (F) of $A_1$ will go negative until $A_1$ saturates. This causes $D_1$ to be turned off.

Next consider what happens when A goes negative. The tendency for a negative voltage at the negative input of $A_1$ causes F to rise, making $D_1$ conduct to supply $R_L$ and allowing the feedback loop around $A_1$ to be closed. Thus a virtual ground appears at the negative input of $A_1$, and the two equal resistances $R_1$ and $R_2$ force the voltage at C, which is the output

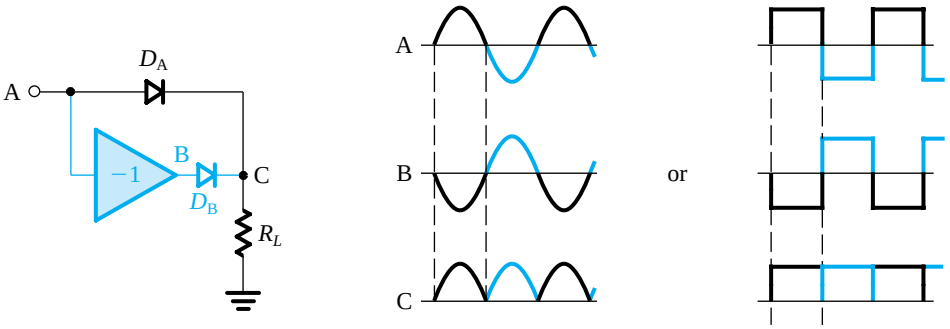



**Figure 17.36** Principle of full-wave rectification.

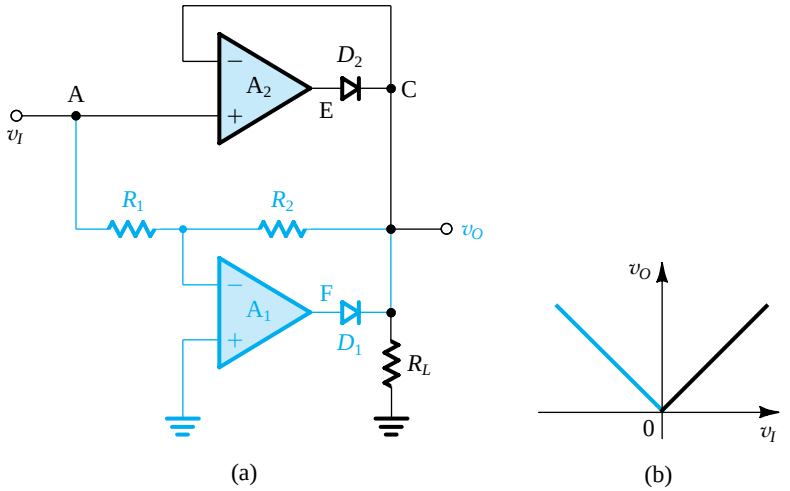



**Figure 17.37** **(a)** Precision full-wave rectifier based on the conceptual circuit of Fig. 17.36. **(b)** Transfer characteristic of the circuit in **(a)**.

## EXERCISES

**17.29** In the full-wave rectifier circuit of Fig. 17.37(a), let $R_1 = R_2 = R_L = 10$ kΩ and assume the op amps to be ideal except for output saturation at ±12 V. When conducting a current of 1 mA, each diode exhibits a voltage drop of 0.7 V, and this voltage changes by 0.1 V per decade of current change. Find $v_O$, $v_E$, and $v_F$ corresponding to $v_I = +0.1$ V, +1 V, +10 V, –0.1 V, and –10 V.

**Ans.** + 0.1 V, + 0.6 V, –12 V; +1 V, +1.6 V, –12 V; +10 V, +10.7 V, –12 V; + 0.1 V, –12 V, + 0.63 V; +1 V, –12 V, + 1.63 V; +10 V, –12 V, +10.73 V

**D17.30** The block diagram shown in Fig. E17.30(a) gives another possible arrangement for implementing the absolute-value or full-wave-rectifier operation depicted symbolically in Fig. E17.30(b). The block diagram consists of two boxes: a half-wave rectifier, which can be implemented by the circuit in Fig. 17.34(a) after reversing both diodes, and a weighted inverting summer. Convince yourself that this block diagram does in fact realize the absolute-value operation. Then draw a complete circuit diagram, giving reasonable values for all resistors.

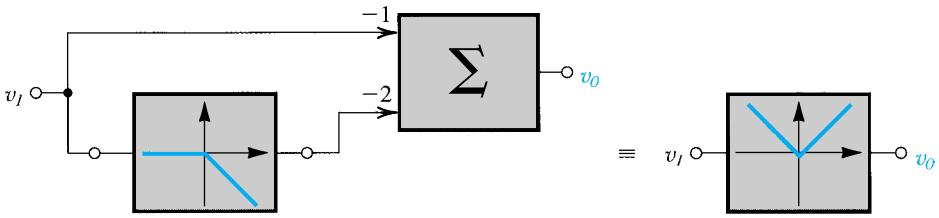



**Figure E17.30**

voltage, to be equal to the negative of the input voltage at A and thus positive. The combination of positive voltage at C and negative voltage at A causes the output of $A_2$ to saturate in the negative direction, thus keeping $D_2$ off.

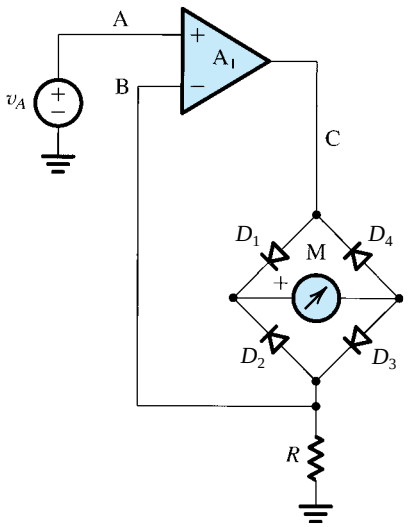



**Figure 17.38** Use of the diode bridge in the design of an ac voltmeter.

The overall result is perfect full-wave rectification, as represented by the transfer characteristic in Fig. 17.37(b). This precision is, of course, a result of placing the diodes in op-amp feedback loops, thus masking their nonidealities. This circuit is one of many possible precision full-wave-rectifier or **absolute-value circuits**. Another related implementation of this function is examined in Exercise 17.30.

### 17.9.5 A Precision Bridge Rectifier for Instrumentation Applications

The bridge rectifier circuit studied in Chapter 4 can be combined with an op amp to provide useful precision circuits. One such arrangement is shown in Fig. 17.38. This circuit causes a current equal to $|v_A|/R$ to flow through the moving-coil meter M. Thus the meter provides a reading that is proportional to the average of the absolute value of the input voltage $v_A$. All the nonidealities of the meter and of the diodes are masked by placing the bridge circuit in the negative-feedback loop of the op amp. Observe that when $v_A$ is positive, current flows from the op-amp output through $D_1$, M, $D_3$, and $R$. When $v_A$ is negative, current flows into the op-amp output through $R$, $D_2$, M, and $D_4$. Thus the feedback loop remains closed for both polarities of $v_A$. The resulting virtual short circuit at the input terminals of the op amp causes a replica of $v_A$ to appear across $R$. The circuit of Fig. 17.38 provides a relatively accurate high-input-impedance ac voltmeter using an inexpensive moving-coil meter.

## EXERCISES

**D17.31** In the circuit of Fig. 17.38, find the value of $R$ that would cause the meter to provide a full-scale reading when the input voltage is a sine wave of 5 V rms. Let meter M have a 1-mA, 50-Ω movement (i.e., its resistance is 50 Ω, and it provides full-scale deflection when the average current through it is 1 mA). What are the approximate maximum and minimum voltages at the op amp's output? Assume that the diodes have constant 0.7-V drops when conducting.

**Ans.** 4.5 kΩ; +8.55 V; −8.55 V

### 17.9.6 Precision Peak Rectifiers

Including the diode of the peak rectifier studied in Chapter 4 inside the negative-feedback loop of an op amp, as shown in Fig. 17.39, results in a precision peak rectifier. The diode–op-amp combination will be recognized as the superdiode of Fig. 17.33(a). Operation of the circuit in Fig. 17.39 is quite straightforward. For $v_I$ greater than the output voltage, the op amp will drive the diode on, thus closing the negative-feedback path and causing the op amp to act as a follower. The output voltage will therefore follow that of the input, with the op amp supplying the capacitor-charging current. This process continues until the input reaches its peak value. Beyond the positive peak, the op amp will see a negative voltage between its input terminals. Thus its output will go negative to the saturation level and the diode will turn off. Except for possible discharge through the load resistance, the capacitor will retain a voltage equal to the positive peak of the input. Inclusion of a load resistance is essential if the circuit is required to detect reductions in the magnitude of the positive peak.

### 17.9.7 A Buffered Precision Peak Detector

When the peak detector is required to hold the value of the peak for a long time, the capacitor should be buffered, as shown in the circuit of Fig. 17.40. Here op amp $A_2$, which should have high input impedance and low input bias current, is connected as a voltage follower. The remainder of the circuit is quite similar to the half-wave-rectifier circuit of Fig. 17.34. While diode $D_1$ is the essential diode for the peak-rectification operation, diode $D_2$ acts as a catching diode to prevent negative saturation, and the associated delays, of op amp $A_1$. During the holding state, follower $A_2$ supplies $D_2$ with a small current through $R$. The output of op amp $A_1$ will then be clamped at one diode drop below the input voltage. Now if the input $v_I$ increases above the value stored on $C$, which is equal to the output voltage $v_O$, op amp $A_1$ sees

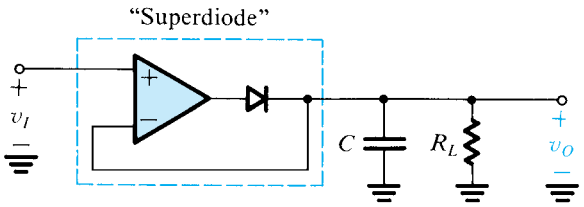



**Figure 17.39** A precision peak rectifier obtained by placing the diode in the feedback loop of an op amp.

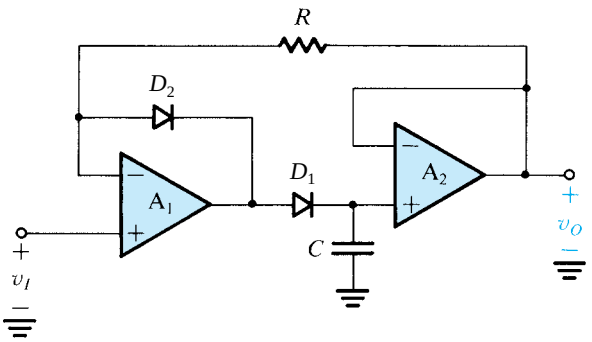



**Figure 17.40** A buffered precision peak rectifier.

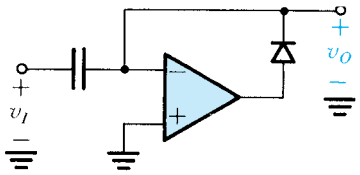



**Figure 17.41** A precision clamping circuit.

a net positive input that drives its output toward the positive saturation level, turning off diode $D_2$. Diode $D_1$ is then turned on and capacitor $C$ is charged to the new positive peak of the input, after which time the circuit returns to the holding state. Finally, note that this circuit has a low-impedance output.

### 17.9.8 A Precision Clamping Circuit

By replacing the diode in the clamping circuit studied in Chapter 4 with a "superdiode," the precision clamp of Fig. 17.41 is obtained. Operation of this circuit should be self-explanatory.

## Summary

- There are two distinctly different types of signal generator: the linear oscillator, which utilizes some form of resonance, and the nonlinear oscillator or function generator, which employs a switching mechanism implemented with a multivibrator circuit.
- A linear oscillator can be realized by placing a frequency-selective network in the feedback path of an amplifier (an op amp or a transistor). The circuit will oscillate at the frequency at which the total phase shift around the loop is zero, provided that the magnitude of loop gain at this frequency is equal to, or greater than, unity.
- If in an oscillator the magnitude of loop gain is greater than unity, the amplitude will increase until a nonlinear amplitude-control mechanism is activated.
- The Wien-bridge oscillator, the phase-shift oscillator, the quadrature oscillator, and the active-filter-tuned oscillator are popular configurations for frequencies up to about 1 MHz. These circuits employ RC networks together with op amps or transistors. For higher frequencies, LC-tuned or crystal-tuned oscillators are utilized. A popular configuration is the Colpitts circuit.
- Crystal oscillators provide the highest possible frequency accuracy and stability.
- There are three types of multivibrator: bistable, monostable, and astable. Op-amp circuit implementations of multivibrators are useful in analog-circuit applications that require high precision.
- The bistable multivibrator has two stable states and can remain in either state indefinitely. It changes state when triggered. A comparator with hysteresis is bistable.
- A monostable multivibrator, also known as a one-shot, has one stable state, in which it can remain indefinitely. When triggered, it goes into a quasi-stable state in which it remains for a predetermined interval, thus generating, at its output, a pulse of known width.
- An astable multivibrator has no stable state. It oscillates between two quasi-stable states, remaining in each for a predetermined interval. It thus generates a periodic waveform at the output.
- A feedback loop consisting of an integrator and a bistable multivibrator can be used to generate triangular and square waveforms.
- The 555 timer, a commercially available IC, can be used with external resistors and a capacitor to implement high-quality monostable and astable multivibrators.
- A sine waveform can be generated by feeding a triangular waveform to a sine-wave shaper. A sine-wave shaper can be implemented either by using diodes (or transistors) and resistors, or by using an amplifier having a nonlinear transfer characteristic that approximates the sine function.
- Diodes can be combined with op amps to implement precision rectifier circuits in which negative feed-back serves to mask the nonidealities of the diode characteristics.

Problems involving design are marked with D throughout the text. As well, problems are marked with asterisks to describe their degree of difficulty. Difficult problems are marked with an asterisk (*); more difficult problems with two asterisks (**); and very challenging and/or time-consuming problems with three asterisks (***).

## Section 17.1: Basic Principles of Sinusoidal Oscillators

***17.1** Consider a sinusoidal oscillator consisting of an amplifier having a frequency-independent gain $A$ (where $A$ is positive) and a second-order bandpass filter with a pole frequency $\omega_0$, a pole $Q$ denoted $Q$, and a center-frequency gain $K$.

(a) Find the frequency of oscillation, and the condition that $A$ and $K$ must satisfy for sustained oscillation.
(b) Derive an expression for $d\phi/d\omega$, evaluated at $\omega = \omega_0$.
(c) Use the result of (b) to find an expression for the per-unit change in frequency of oscillation resulting from a phase-angle change of $\Delta\phi$, in the amplifier transfer function.

$$\textit{Hint: } \frac{d}{dx}(\tan^{-1} y) = \frac{1}{1+y^2}\frac{dy}{dx}$$

**17.2** For the oscillator described in Problem 17.1, show that, independent of the value of $A$ and $K$, the poles of the circuit lie at a radial distance of $\omega_0$. Find the value of $AK$ that results in poles appearing (a) on the $j\omega$ axis, and (b) in the right-half of the $s$ plane, at a horizontal distance from the $j\omega$ axis of $\omega_0/(2Q)$.

**D 17.3** Sketch a circuit for a sinusoidal oscillator formed by an ideal op amp connected in the noninverting configuration and a bandpass filter implemented by an RLC resonator (such as that in Fig. 16.18d). What should the amplifier gain be to obtain sustained oscillation? What is the frequency of oscillation? Find the percentage change in $\omega_0$ resulting from a change of +1% in the value of (a) $L$, (b) $C$, and (c) $R$.

**17.4** An oscillator is formed by loading a transconductance amplifier having a positive gain with a parallel RLC circuit and connecting the output directly to the input (thus applying positive feedback with a factor $\beta = 1$). Let the transconductance amplifier have an input resistance of 10 kΩ and an output resistance of 10 kΩ. The LC resonator has $L = 10$ μH, $C = 1000$ pF, and $Q = 100$. For what value of transconductance $G_m$ will the circuit oscillate? At what frequency?

**17.5** In a particular oscillator characterized by the structure of Fig. 17.1, the frequency-selective network exhibits a loss of 20 dB and a phase shift of 180° at $\omega_0$. What is the minimum gain and the phase shift that the amplifier must have for oscillation to begin?

**D 17.6** Consider the circuit of Fig. 17.3(a) with $R_f$ removed to realize the comparator function. Find suitable values for all resistors so that the comparator output levels are ±6 V and the slope of the limiting characteristic is 0.1. Use power-supply voltages of ±10 V and assume the voltage drop of a conducting diode to be 0.7 V.

**D 17.7** Consider the circuit of Fig. 17.3(a) with $R_f$ removed to realize the comparator function. Sketch the transfer characteristic. Show that by connecting a dc source $V_B$ to the virtual ground of the op amp through a resistor $R_B$, the transfer characteristic is shifted along the $v_I$ axis to the point $v_I = -(R_1/R_B)V_B$. Utilizing available ±15-V dc supplies for $\pm V$ and for $V_B$, find suitable component values so that the limiting levels are ±5 V and the comparator threshold is at $v_I = +5$ V. Neglect the diode voltage drop (i.e., assume that $V_D = 0$). The input resistance of the comparator is to be 100 kΩ, and the slope in the limiting regions is to be ≤0.05 V/V. Use standard 5% resistors (see Appendix H).

**17.8** Denoting the zener voltages of $Z_1$ and $Z_2$ by $V_{Z1}$ and $V_{Z2}$ and assuming that in the forward direction the voltage drop is approximately 0.7 V, sketch and clearly label the transfer characteristics $v_O$–$v_I$ of the circuits in Fig. P17.8. Assume the op amps to be ideal.

## Section 17.2: Op Amp–RC Oscillator Circuits

**17.9** For the Wien-bridge oscillator circuit in Fig. 17.4, show that the transfer function of the feedback network $[V_a(s)/V_o(s)]$ is that of a bandpass filter. Find $\omega_0$ and $Q$ of the poles, and find the center-frequency gain.

**17.10** For the Wien-bridge oscillator of Fig. 17.4, let the closed-loop amplifier (formed by the op amp and the resistors $R_1$ and $R_2$) exhibit a phase shift of –0.1 rad in the neighborhood of $\omega = 1/CR$. Find the frequency at which oscillations can occur in this case in terms of $CR$. (*Hint:* Use Eq. 17.11.)

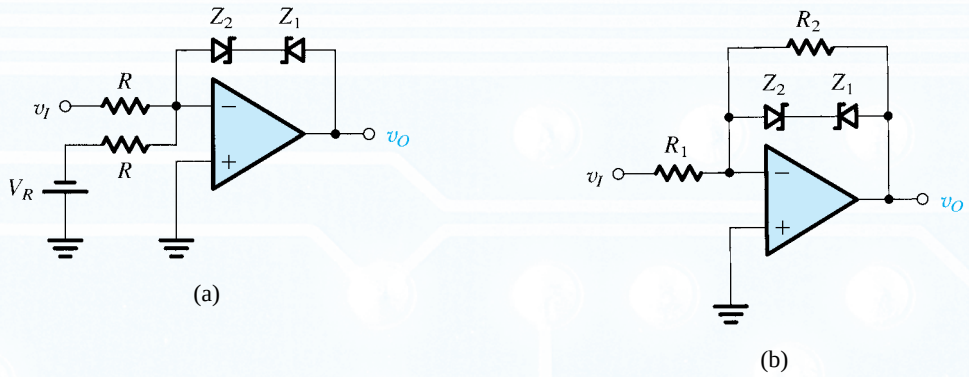



**Figure P17.8**

**17.11** For the Wien-bridge oscillator of Fig. 17.4, use the expression for loop gain in Eq. (17.10) to find the poles of the closed-loop system. Give the expression for the pole $Q$, and use it to show that to locate the poles in the right half of the $s$ plane, $R_2/R_1$ must be selected to be greater than 2.

**D*17.12** Reconsider Exercise 17.3 with $R_3$ and $R_6$ increased to reduce the output voltage. What values are required for a peak-to-peak output of 10 V? What results if $R_3$ and $R_6$ are open-circuited?

**17.13** For the circuit in Fig. P17.13, find $L(s)$, $L(j\omega)$, the frequency for zero loop phase, and $R_2/R_1$ for oscillation.

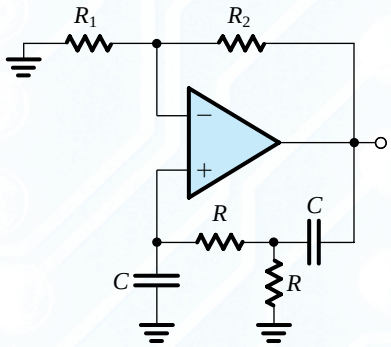



**Figure P17.13**

**17.14** Repeat Problem 17.13 for the circuit in Fig. P17.14.

***17.15** Consider the circuit of Fig. 17.6 with the 50-kΩ potentiometer replaced by two fixed resistors: 10 kΩ between the op amp's negative input and ground, and 18 kΩ. Modeling each diode as a 0.65-V battery in series with a 100-Ω resistance, find the peak-to-peak amplitude of the output sinusoid.

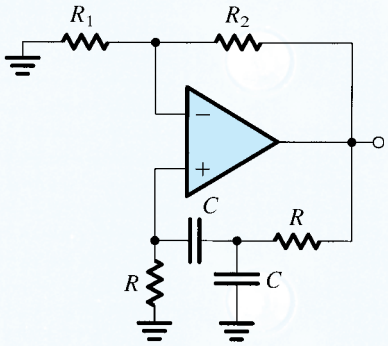



**Figure P17.14**

**D**17.16** Redesign the circuit of Fig. 17.6 for operation at 10 kHz using the same values of resistance. If at 10 kHz the op amp provides an excess phase shift (lag) of 5.7°, what will be the frequency of oscillation? (Assume that the phase shift introduced by the op amp remains constant for frequencies around 10 kHz.) To restore operation to 10 kHz, what change must be made in the shunt resistor of the Wien bridge? Also, to what value must $R_2/R_1$ be changed?

***17.17** For the circuit of Fig. 17.8, connect an additional $R = 10$ kΩ resistor in series with the rightmost capacitor $C$. For this modification (and ignoring the amplitude stabilization circuitry) find the loop gain $A\beta$ by breaking the circuit at node $X$. Find $R_f$ for oscillation to begin, and find $f_0$.

**D 17.18** For the circuit in Fig. P17.18, break the loop at node $X$ and find the loop gain (working backward for simplicity to find $V_x$ in terms of $V_o$). For $R = 10$ kΩ, find $C$ and $R_f$ to obtain sinusoidal oscillations at 10 kHz.

***17.19** Consider the quadrature-oscillator circuit of Fig. 17.9 without the limiter. Let the resistance $R_f$ be equal to

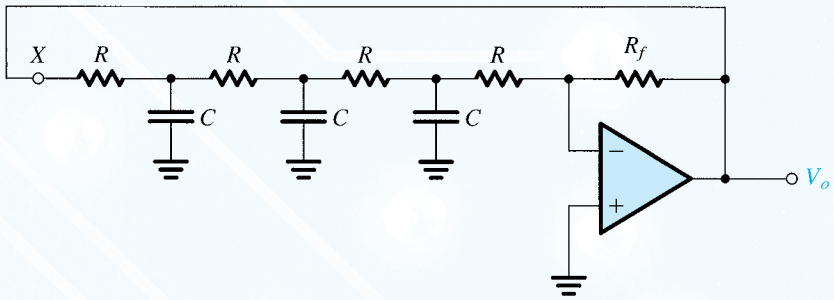



**Figure P17.18**

$2R/(1+\Delta)$, where $\Delta \ll 1$. Show that the poles of the characteristic equation are in the right-half $s$ plane and given by $s \simeq (1/CR)[(\Delta/4) \pm j]$.

***17.20** Assuming that the diode-clipped waveform in Exercise 17.7 is nearly an ideal square wave and that the resonator $Q$ is 20, provide an estimate of the distortion in the output sine wave by calculating the magnitude (relative to the fundamental) of

(a) the second harmonic
(b) the third harmonic
(c) the fifth harmonic
(d) the rms of harmonics to the tenth

Note that a square wave of amplitude $V$ and frequency $\omega$ is represented by the series

$$\frac{4V}{\pi}\left(\sin \omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \frac{1}{7}\sin 7\omega t + \cdots\right)$$

## Section 17.3: LC and Crystal Oscillators

****17.21** Figure P17.21 shows four oscillator circuits of the Colpitts type, complete with bias detail. For each circuit, derive an equation governing circuit operation and find the frequency of oscillation and the gain condition that ensures that oscillations start.

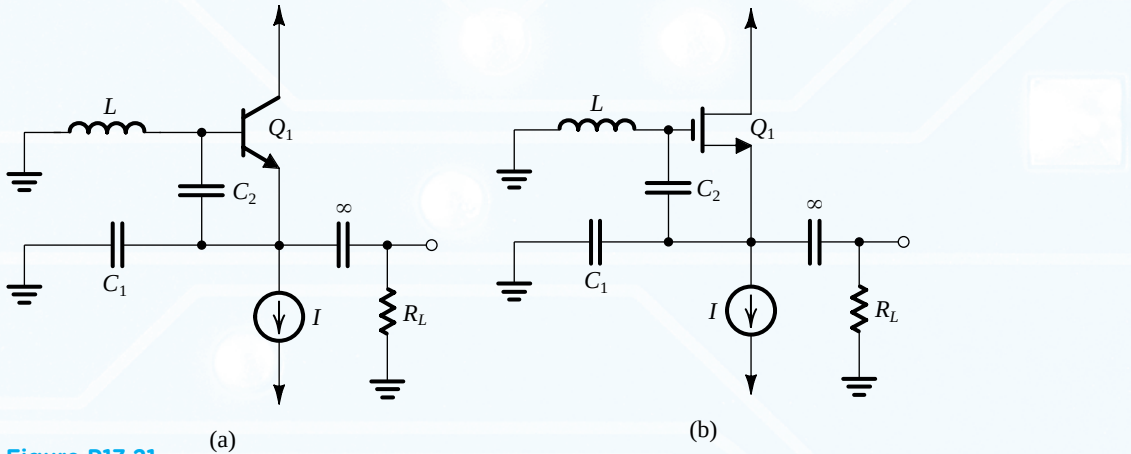
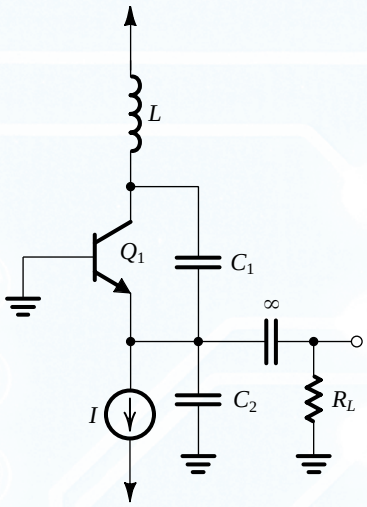



**Figure P17.21**

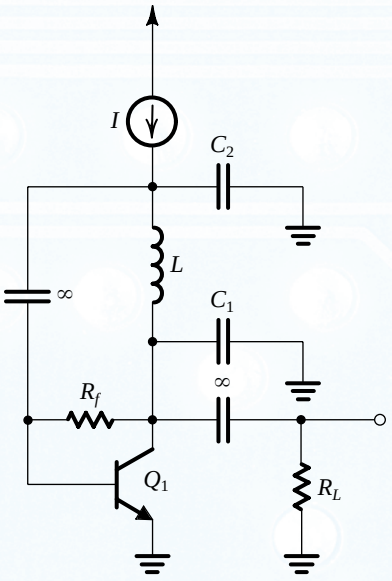
****17.22** Consider the oscillator circuit in Fig. P17.22, and assume for simplicity that $\beta = \infty$.

(a) Find the frequency of oscillation and the minimum value of $R_C$ (in terms of the bias current $I$) for oscillation to start.
(b) If $R_C$ is selected equal to $(1/I)$ kΩ, where $I$ is in milliamperes, convince yourself that oscillations will start. If oscillations grow to the point that $V_o$ is large enough to turn the BJTs on and off, show that the voltage at the collector of $Q_2$ will be a square wave of 1 V peak to peak. Estimate the peak-to-peak amplitude of the output sine wave $V_o$.

**17.23** Consider the Pierce crystal oscillator of Fig. 17.16 with the crystal as specified in Exercise 17.10. Let $C_1$ be variable in the range 1 pF to 10 pF, and let $C_2$ be fixed at 10 pF. Find the range over which the oscillation frequency can be tuned. (*Hint:* Use the result in the statement leading to the expression in Eq. 17.27.)




(c)




(Assume $R_f \gg \omega_0 L$)

(d)

**Figure P17.21** (*Continued*)

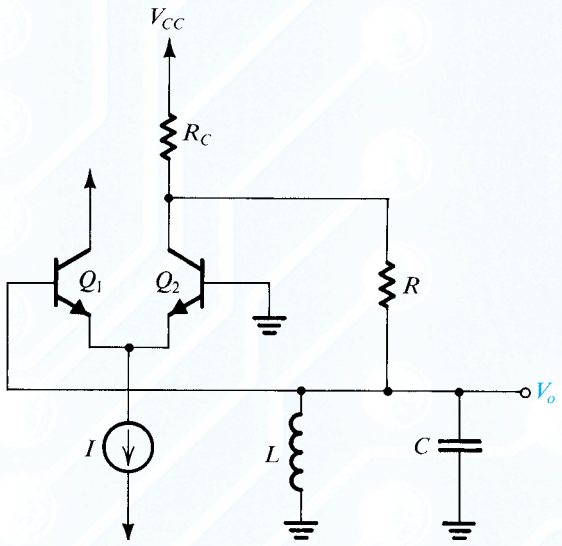



**Figure P17.22**

## Section 17.4: Bistable Multivibrators

**17.24** Consider the bistable circuit of Fig. 17.19(a) with the op amp's positive-input terminal connected to a positive-voltage source $V$ through a resistor $R_3$.

(a) Derive expressions for the threshold voltages $V_{TL}$ and $V_{TH}$ in terms of the op amp's saturation levels $L_+$ and $L_-$, $R_1$, $R_2$, $R_3$, and $V$.
(b) Let $L_+ = -L_- = 13$ V, $V = 15$ V, and $R_1 = 10$ kΩ. Find the values of $R_2$ and $R_3$ that result in $V_{TL} = +4.9$ V and $V_{TH} = +5.1$ V.

**17.25** Consider the bistable circuit of Fig. 17.20(a) with the op amp's negative-input terminal disconnected from ground and connected to a reference voltage $V_R$.

(a) Derive expressions for the threshold voltages $V_{TL}$ and $V_{TH}$ in terms of the op amp's saturation levels $L_+$ and $L_-$, $R_1$, $R_2$, and $V_R$.
(b) Let $L_+ = -L_- = V$ and $R_1 = 10$ kΩ. Find $R_2$ and $V_R$ that result in threshold voltages of 0 and $V/10$.

**17.26** For the circuit in Fig. P17.26, sketch and label the transfer characteristic $v_O$–$v_I$. The diodes are assumed to have a constant 0.7-V drop when conducting, and the op amp saturates at ±12 V. What is the maximum diode current?

**17.27** Consider the circuit of Fig. P17.26 with $R_1$ eliminated and $R_2$ short-circuited. Sketch and label the transfer characteristic $v_O$–$v_I$. Assume that the diodes have a constant 0.7-V drop when conducting and that the op amp saturates at ±12 V.

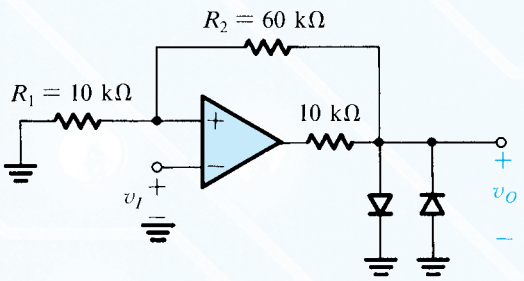



Figure P17.26

*17.28 Consider a bistable circuit having a noninverting transfer characteristic with $L_+ = -L_- = 12$ V, $V_{TL} = -1$ V, and $V_{TH} = +1$ V.

(a) For a 0.5-V-amplitude sine-wave input having zero average, what is the output?
(b) Describe the output if a sinusoid of frequency $f$ and amplitude of 1.1 V is applied at the input. By how much can the average of this sinusoidal input shift before the output becomes a constant value?

D 17.29 Design the circuit of Fig. 17.23(a) to realize a transfer characteristic with ±7.5-V output levels and ±7.5-V threshold values. Design so that when $v_I = 0$ V a current of 0.1 mA flows in the feedback resistor and a current of 1 mA flows through the zener diodes. Assume that the output saturation levels of the op amp are ±12 V. Specify the voltages of the zener diodes and give the values of all resistors.

## Section 17.5: Generation of Square and Triangular Waveforms Using Astable Multivibrators

17.30 Find the frequency of oscillation of the circuit in Fig. 17.24(b) for the case $R_1 = 10$ kΩ, $R_2 = 16$ kΩ, $C = 10$ nF, and $R = 62$ kΩ.

D 17.31 Augment the astable multivibrator circuit of Fig. 17.24(b) with an output limiter of the type shown in Fig. 17.23(b). Design the circuit to obtain an output square wave with 5-V amplitude and 1-kHz frequency using a 10-nF capacitor $C$. Use $\beta = 0.462$, and design for a current in the resistive divider approximately equal to the average current in the RC network over a half-cycle. Assuming ±13-V op-amp saturation voltages, arrange for the zener to operate at a current of 1 mA.

D 17.32 Using the scheme of Fig. 17.25, design a circuit that provides square waves of 10 V peak to peak and triangular waves of 10 V peak to peak. The frequency is to be 1 kHz. Implement the bistable circuit with the circuit of Fig. 17.23(b). Use a 0.01-μF capacitor and specify the values of all resistors and the required zener voltage. Design for a minimum zener current of 1 mA and for a maximum current in the resistive divider of 0.2 mA. Assume that the output saturation levels of the op amps are ±13 V.

D*17.33 The circuit of Fig. P17.33 consists of an inverting bistable multivibrator with an output limiter and a noninverting integrator. Using equal values for all resistors except $R_7$ and a 0.5-nF capacitor, design the circuit to obtain a square wave at the output of the bistable multivibrator of 15-V peak-to-peak amplitude and 10-kHz frequency. Sketch and label the waveform at the integrator output. Assuming ±13-V op-amp saturation levels, design for a minimum zener current of 1 mA. Specify the zener voltage required, and give the values of all resistors.

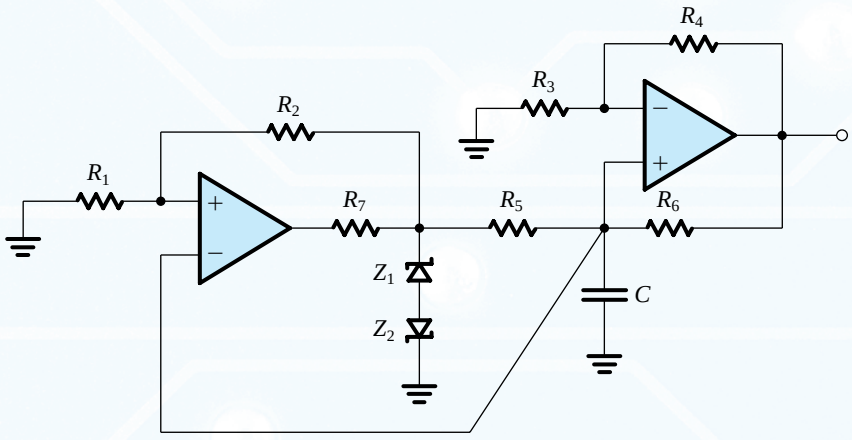



Figure P17.33

## Section 17.6: Generation of a Standardized Pulse—The Monostable Multivibrator

***17.34** Figure P17.34 shows a monostable multivibrator circuit. In the stable state, $v_O = L_+$, $v_A = 0$, and $v_B = -V_{\text{ref}}$. The circuit can be triggered by applying a positive input pulse of height greater than $V_{\text{ref}}$. For normal operation, $C_1R_1 \ll CR$. Show the resulting waveforms of $v_O$ and $v_A$. Also, show that the pulse generated at the output will have a width $T$ given by

$$T = CR \ln\left(\frac{L_+ - L_-}{V_{\text{ref}}}\right)$$

Note that this circuit has the interesting property that the pulse width can be controlled by changing $V_{\text{ref}}$.

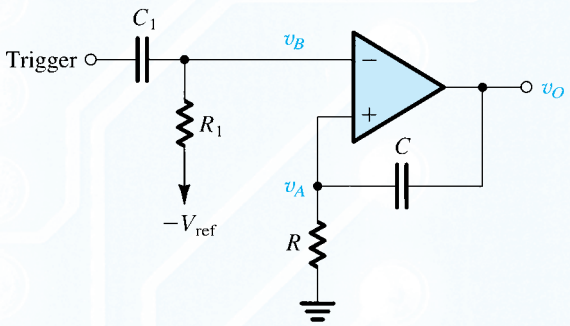



**Figure P17.34**

**17.35** For the monostable circuit considered in Exercise 17.19, calculate the recovery time.

**D*17.36** Using the circuit of Fig. 17.26, with a nearly ideal op amp for which the saturation levels are ±13 V, design a monostable multivibrator to provide a negative output pulse of 100-μs duration. Use capacitors of 0.1 nF and 1 nF. Wherever possible, choose resistors of 100 kΩ in your design. Diodes have a drop of 0.7 V. What is the minimum input step size that will ensure triggering? How long does the circuit take to recover to a state in which retriggering is possible with a normal output?

## Section 17.7: Integrated-Circuit Timers

**17.37** Consider the 555 circuit of Fig. 17.27 when the Threshold and the Trigger input terminals are joined together and connected to an input voltage $v_I$. Verify that the transfer characteristic $v_O$–$v_I$ is that of an inverting bistable circuit with thresholds $V_{TL} = \frac{1}{3}V_{CC}$ and $V_{TH} = \frac{2}{3}V_{CC}$ and output levels of 0 and $V_{CC}$.

**17.38** (a) Using a 1-nF capacitor $C$ in the circuit of Fig. 17.28(a), find the value of $R$ that results in an output pulse of 10-μs duration.
(b) If the 555 timer used in (a) is powered with $V_{CC} = 15$ V, and assuming that $V_{TH}$ can be varied externally (i.e., it need not remain equal to $\frac{2}{3}V_{CC}$), find its required value so that the pulse width is increased to 20 μs, with other conditions the same as in (a).

**D 17.39** Using a 680-pF capacitor, design the astable circuit of Fig. 17.29(a) to obtain a square wave with a 50-kHz frequency and a 75% duty cycle. Specify the values of $R_A$ and $R_B$.

***17.40** The node in the 555 timer at which the voltage is $V_{TH}$ (i.e., the inverting input terminal of comparator 1) is usually connected to an external terminal. This allows the user to change $V_{TH}$ externally (i.e., $V_{TH}$ no longer remains at $\frac{2}{3}V_{CC}$). Note, however, that whatever the value of $V_{TH}$ becomes, $V_{TL}$ always remains $\frac{1}{2}V_{TH}$.

(a) For the astable circuit of Fig. 17.29, rederive the expressions for $T_H$ and $T_L$, expressing them in terms of $V_{TH}$ and $V_{TL}$.
(b) For the case $C = 1$ nF, $R_A = 7.2$ kΩ, $R_B = 3.6$ kΩ, and $V_{CC} = 5$ V, find the frequency of oscillation and the duty cycle of the resulting square wave when no external voltage is applied to the terminal $V_{TH}$.
(c) For the design in (b), let a sine-wave signal of a much lower frequency than that found in (b) and of 1-V peak amplitude be capacitively coupled to the circuit node $V_{TH}$. This signal will cause $V_{TH}$ to change around its quiescent value of $\frac{2}{3}V_{CC}$, and thus $T_H$ will change correspondingly—a modulation process. Find $T_H$, and find the frequency of oscillation and the duty cycle at the two extreme values of $V_{TH}$.

## Section 17.8: Nonlinear Waveform-Shaping Circuits

**D*17.41** The two-diode circuit shown in Fig. P17.41 can provide a crude approximation to a sine-wave output when driven by a triangular waveform. To obtain a good approximation, we select the peak of the triangular waveform, $V$, so that the slope of the desired sine wave at the zero crossings is equal to that of the triangular wave. Also, the value of $R$ is selected so that when $v_I$ is at its peak, the output voltage is equal to the desired peak of the sine wave. If the diodes exhibit a voltage drop of 0.7 V at 1-mA current, changing at the rate of 0.1 V per decade, find the values of $V$ and $R$ that will yield an approximation to a sine waveform of 0.7-V peak amplitude. Then find the angles $\theta$ (where $\theta = 90°$ when $v_I$ is at its peak) at which the output of the circuit, in volts, is 0.7, 0.65, 0.6, 0.55, 0.5, 0.4, 0.3, 0.2, 0.1, and 0. Use the angle values obtained to determine the values of the exact sine wave (i.e., 0.7 sin $\theta$), and thus find the percentage error of this circuit as a sine shaper. Provide your results in tabular form.

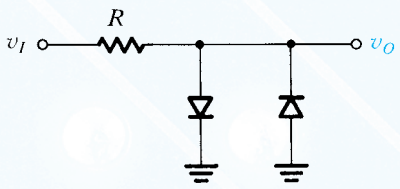



Figure P17.41

**D 17.42** Design a two-segment sine-wave shaper using a 10-kΩ-input resistor, two diodes, and two clamping voltages. The circuit, fed by a 10-V peak-to-peak triangular wave, should limit the amplitude of the output signal via a 0.7-V diode to a value corresponding to that of a sine wave whose zero-crossing slope matches that of the triangle. What are the clamping voltages you have chosen?

**17.43** Show that the output voltage of the circuit in Fig. P17.43 is given by

$$v_O = -V_T \ln\left(\frac{v_I}{I_S R}\right), \quad v_I > 0$$

where $I_S$ is the saturation current of the diode and $V_T$ is the thermal voltage. Since the output voltage is proportional to the logarithm of the input voltage, the circuit is known as a **logarithmic amplifier**. Such amplifiers find application in situations where it is desired to compress the signal range.

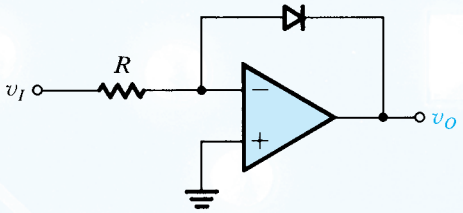



Figure P17.43

**17.44** Verify that the circuit in Fig. P17.44 implements the transfer characteristic $v_O = v_1 v_2$ for $v_1, v_2 > 0$. Such a circuit is known as an analog multiplier. Check the circuit's performance for various combinations of input voltage of values, say, 0.5 V, 1 V, 2 V, and 3 V. Assume all diodes to be identical, with 700-mV drop at 1-mA current. Note that a *squarer* can easily be produced using a single input (e.g., $v_1$) connected via a 0.5-kΩ resistor (rather than the 1-kΩ resistor shown).

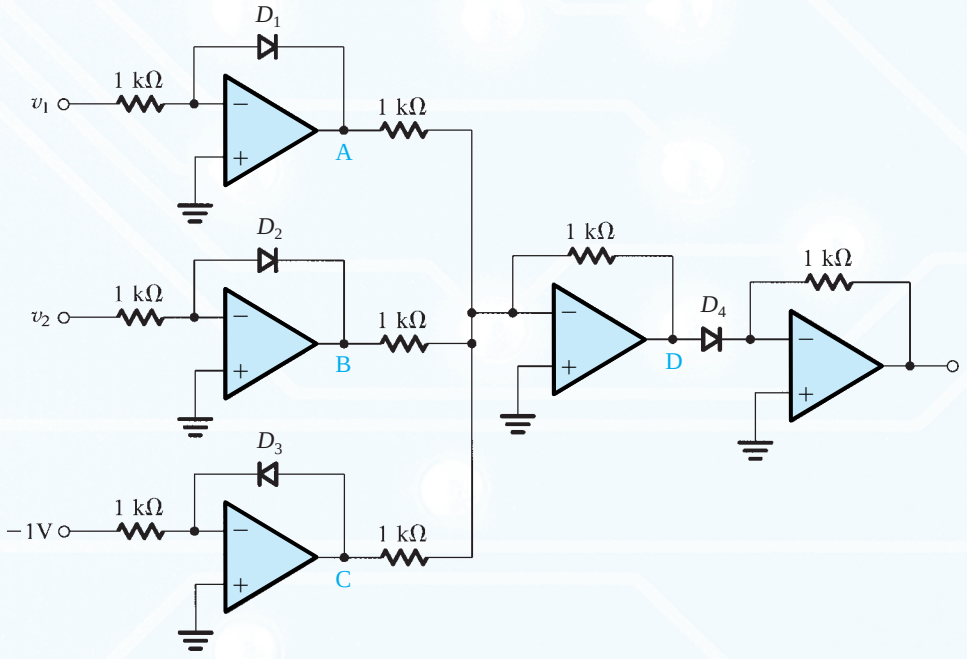



Figure P17.44

**17.45 Detailed analysis of the circuit in Fig. 17.32 shows that optimum performance (as a sine shaper) occurs when the values of $I$ and $R$ are selected so that $RI = 2.5V_T$, where $V_T$ is the thermal voltage, and the peak amplitude of the input triangular wave is $6.6V_T$. If the output is taken across $R$ (i.e., between the two emitters), find $v_I$ corresponding to $v_O = 0.25V_T$, $0.5V_T$, $V_T$, $1.5V_T$, $2V_T$, $2.4V_T$, and $2.42V_T$. Plot $v_O$–$v_I$ and compare to the ideal curve given by

$$v_O = 2.42\,V_T \sin\left(\frac{v_I}{6.6\,V_T} \times 90°\right)$$

## Section 17.9: Precision Rectifier Circuits

17.46 Two superdiode circuits connected to a common-load resistor and having the same input signal have their diodes reversed, one with cathode to the load, the other with anode to the load. For a sine-wave input of 10 V peak to peak, what is the output waveform? Note that each half-cycle of the load current is provided by a separate amplifier, and that while one amplifier supplies the load current, the other amplifier idles. This idea, called class-B operation (see Chapter 11), is important in the implementation of power amplifiers.

D 17.47 The superdiode circuit of Fig. 17.33(a) can be made to have gain by connecting a resistor $R_2$ in place of the short circuit between the cathode of the diode and the negative-input terminal of the op amp, and a resistor $R_1$ between the negative-input terminal and ground. Design the circuit for a gain of 2. For a 10-V peak-to-peak input sine wave, what is the average output voltage resulting?

D 17.48 Provide a design of the inverting precision rectifier shown in Fig. 17.34(a) in which the gain is –2 for negative inputs and zero otherwise, and the input resistance is 100 kΩ. What values of $R_1$ and $R_2$ do you choose?

D*17.49 Provide a design for a voltmeter circuit similar to the one in Fig. 17.35, which is intended to function at frequencies of 10 Hz and above. It should be calibrated for sine-wave input signals to provide an output of +10 V for an input of 1 V rms. The input resistance should be as high as possible. To extend the bandwidth of operation, keep the gain in the ac part of the circuit reasonably small. As well, the design should result in reduction of the size of the capacitor $C$ required. The largest value of resistor available is 1 MΩ.

17.50 Plot the transfer characteristic of the circuit in Fig. P17.50.

17.51 Plot the transfer characteristics $v_{O1}$–$v_I$ and $v_{O2}$–$v_I$ of the circuit in Fig. P17.51.

17.52 Sketch the transfer characteristics of the circuit in Fig. P17.52.

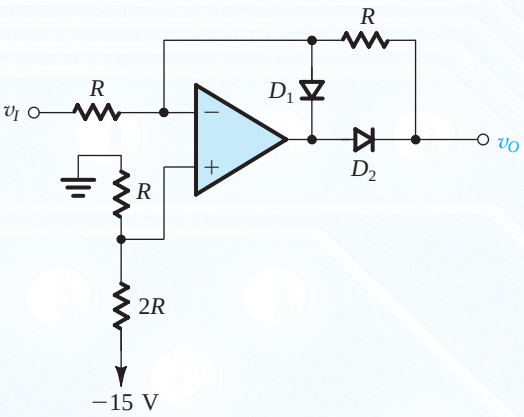



Figure P17.50

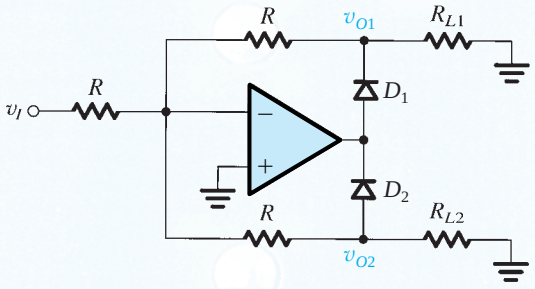



Figure P17.51

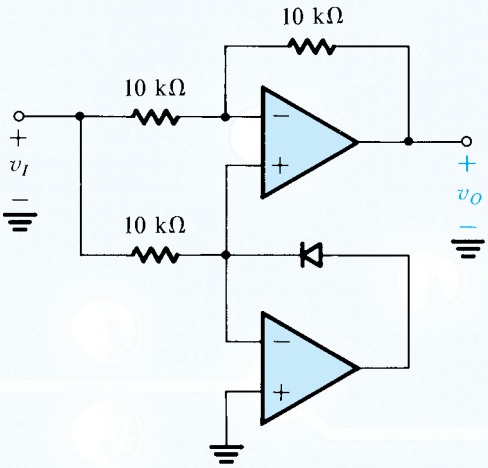



Figure P17.52

D 17.53 A circuit related to that in Fig. 17.38 is to be used to provide a current proportional to $v_A (v_A \geq 0)$ to a light-emitting diode (LED). The value of the current is to

be independent of the diode's nonlinearities and variability. Indicate how this may be done easily.

*17.54 In the precision rectifier of Fig. 17.38, the resistor $R$ is replaced by a capacitor $C$. What happens? For equivalent performance with a sine-wave input of 60-Hz frequency with $R = 1$ kΩ, what value of $C$ should be used? What is the response of the modified circuit at 120 Hz? At 180 Hz? If the amplitude of $v_A$ is kept fixed, what new function does this circuit perform? Now consider the effect of a waveform change on both circuits (the one with $R$ and the one with $C$). For a triangular-wave input of 60-Hz frequency that produces an average meter current of 1 mA in the circuit with $R$, what does the average meter current become when $R$ is replaced with the $C$ whose value was just calculated?

*17.55 A positive-peak rectifier utilizing a fast op amp and a junction diode in a superdiode configuration, and a 10-μF capacitor initially uncharged, is driven by a series of 10-V pulses of 10-μs duration. If the maximum output current that the op amp can supply is 10 mA, what is the voltage on the capacitor following one pulse? Two pulses? Ten pulses? How many pulses are required to reach 0.5 V? 1.0 V? 2.0 V?

**D** 17.56 Consider the buffered precision peak rectifier shown in Fig. 17.40 when connected to a triangular input of 1-V peak-to-peak amplitude and 1000-Hz frequency. It utilizes an op amp whose bias current (directed into $A_2$) is 10 nA and diodes whose reverse leakage current is 1 nA. What is the smallest capacitor that can be used to guarantee an output ripple less than 1%?