CHAPTER 8

Differential and Multistage Amplifiers

IN THIS CHAPTER YOU WILL LEARN

1. The essence of the operation of the MOS and the bipolar differential amplifiers: how they reject common-mode noise or interference and amplify differential signals.
2. The analysis and design of MOS and BJT differential amplifiers.
3. Differential-amplifier circuits of varying complexity; utilizing passive resistive loads, current-source loads, and cascodes—the building blocks we studied in Chapter 7.
4. An ingenious and highly popular differential-amplifier circuit that utilizes a current-mirror load.
5. The structure, analysis, and design of amplifiers composed of two or more stages in cascade. Two practical examples are studied in detail: a two-stage CMOS op amp and a four-stage bipolar op amp.

Introduction

The differential-pair or differential-amplifier configuration is the most widely used building block in analog integrated-circuit design. For instance, the input stage of every op amp is a differential amplifier. Also, the BJT differential amplifier is the basis of a very-high-speed logic circuit family, studied briefly in Chapter 14, called emitter-coupled logic (ECL).

Initially invented in the 1940s for use with vacuum tubes, the basic differential-amplifier configuration was subsequently implemented with discrete bipolar transistors. However, it was the advent of integrated circuits that has made the differential pair extremely popular in both bipolar and MOS technologies. There are two reasons why differential amplifiers are so well suited for IC fabrication: First, as we shall shortly see, the performance of the differential pair depends critically on the matching between the two sides of the circuit. Integrated-circuit fabrication is capable of providing matched devices whose parameters track over wide ranges of changes in environmental conditions. Second, by their very nature, differential amplifiers utilize more components (approaching twice as many) than single-ended circuits. Here again, the reader will recall from the discussion in Section 7.1 that a significant advantage of integrated-circuit technology is the availability of large numbers of transistors at relatively low cost.

We assume that the reader is familiar with the basic concept of a differential amplifier as presented in Section 2.1. Nevertheless it is worthwhile to answer the question: Why differential? Basically, there are two reasons for using differential in preference to single-ended amplifiers. First, differential circuits are much less sensitive to noise and

interference than single-ended circuits. To appreciate this point, consider two wires carrying a small differential signal as the voltage difference between the two wires. Now, assume that there is an interference signal that is coupled to the two wires, either capacitively or inductively. As the two wires are physically close together, the interference voltages on the two wires (i.e., between each of the two wires and ground) will be equal. Since, in a differential system, only the difference signal between the two wires is sensed, it will contain no interference component!

The second reason for preferring differential amplifiers is that the differential configuration enables us to bias the amplifier and to couple amplifier stages together without the need for bypass and coupling capacitors such as those utilized in the design of discrete-circuit amplifiers (Sections 5.8 and 6.8). This is another reason why differential circuits are ideally suited for IC fabrication where large capacitors are impossible to fabricate economically.

The major topic of this chapter is the differential amplifier in both its MOS and bipolar implementations. As will be seen, the design and analysis of differential amplifiers makes extensive use of the material on single-stage amplifiers presented in Chapters 5 through 7. We will follow the study of differential amplifiers with examples of practical multistage amplifiers, again in both MOS and bipolar technologies.

8.1 The MOS Differential Pair

Figure 8.1 shows the basic MOS differential-pair configuration. It consists of two matched transistors, Q_1 and Q_2, whose sources are joined together and biased by a constant-current source I. The latter is usually implemented by a MOSFET circuit of the type studied in Sections 7.4 and 7.5. For the time being, we assume that the current source is ideal and that it has infinite output resistance. Although each drain is shown connected to the positive supply through a resistance R_D, in most cases active (current-source) loads are employed, as will be seen shortly. For the time being, however, we will explain the essence of the differential-pair operation utilizing simple resistive loads. Whatever type of load is used, it is essential that the MOSFETs not enter the triode region of operation.

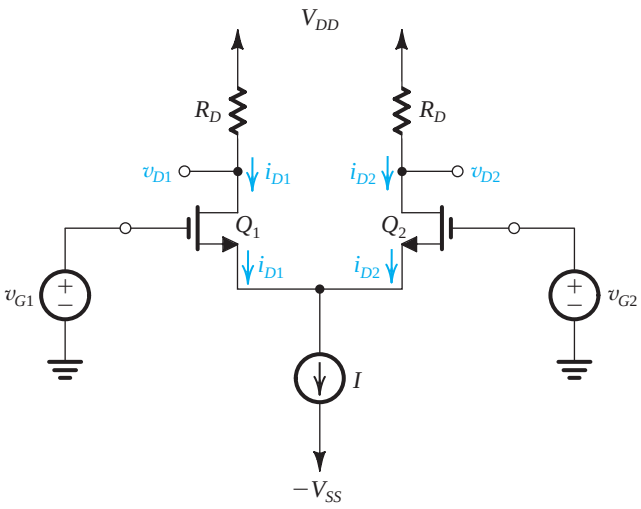


Figure 8.1 The basic MOS differential-pair configuration.

8.1.1 Operation with a Common-Mode Input Voltage

To see how the differential pair works, consider first the case when the two gate terminals are joined together and connected to a voltage V_{CM}, called the **common-mode voltage**. That is, as shown in Fig. 8.2, $v_{G1} = v_{G2} = V_{CM}$. Since Q_1 and Q_2 are matched, the current I will divide equally between the two transistors. Thus, $i_{D1} = i_{D2} = I/2$, and the voltage at the sources, V_S, will be

$$V_S = V_{CM} - V_{GS} \tag{8.1}$$

where V_{GS} is the gate-to-source voltage corresponding to a drain current of $I/2$. Neglecting channel-length modulation, V_{GS} and $I/2$ are related by

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \tag{8.2}$$

or in terms of the overdrive voltage V_{OV},

$$V_{OV} = V_{GS} - V_t \tag{8.3}$$

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 \tag{8.4}$$

$$V_{OV} = \sqrt{I/k_n'(W/L)} \tag{8.5}$$

The voltage at each drain will be

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2} R_D \tag{8.6}$$

Thus, the difference in voltage between the two drains will be zero.

Now, let us vary the value of the common-mode voltage V_{CM}. We see that, as long as Q_1 and Q_2 remain in the saturation region, the current I will divide equally between Q_1 and Q_2 and the voltages at the drains will not change. Thus the differential pair does *not* respond to (i.e., it *rejects*) common-mode input signals.

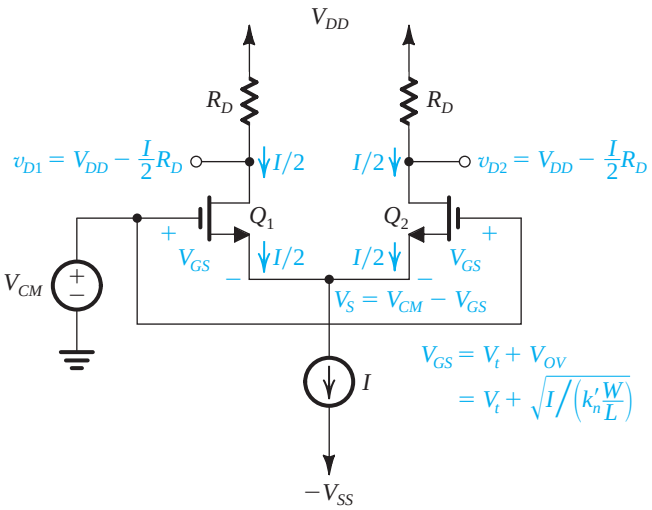


Figure 8.2 The MOS differential pair with a common-mode input voltage V_{CM}.

An important specification of a differential amplifier is its **input common-mode range**. This is the range of V_{CM} over which the differential pair operates properly. The highest value of V_{CM} is limited by the requirement that Q_1 and Q_2 remain in saturation, thus

$$V_{CM\max} = V_t + V_{DD} - \frac{I}{2}R_D \tag{8.7}$$

The lowest value of V_{CM} is determined by the need to allow for a sufficient voltage across the current source I for it to operate properly. If a voltage V_{CS} is needed across the current source, then

$$V_{CM\min} = -V_{SS} + V_{CS} + V_t + V_{OV} \tag{8.8}$$

Example 8.1

For the MOS differential pair with a common-mode voltage V_{CM} applied, as shown in Fig. 8.2, let $V_{DD} = V_{SS} = 1.5$ V, $k_n'(W/L) = 4$ mA/V^2, $V_t = 0.5$ V, $I = 0.4$ mA, and $R_D = 2.5$ kΩ, and neglect channel-length modulation. Assume that the current source I requires a minimum voltage of 0.4 V to operate properly.

(a) Find V_{OV} and V_{GS} for each transistor.
(b) For $V_{CM} = 0$, find V_S, I_{D1}, I_{D2}, V_{D1}, and V_{D2}.
(c) Repeat (b) for $V_{CM} = +1$ V.
(d) Repeat (b) for $V_{CM} = -0.2$ V.
(e) What is the highest permitted value of V_{CM}?
(f) What is the lowest value allowed for V_{CM}?

Solution

(a) With $v_{G1} = v_{G2} = V_{CM}$, we see that $V_{GS1} = V_{GS2}$. Now, since the transistors are matched, I will divide equally between the two transistors,

$$I_{D1} = I_{D2} = \frac{I}{2}$$

Thus,

$$\frac{I}{2} = \frac{1}{2}k_n'(W/L)V_{OV}^2$$

$$\frac{0.4}{2} = \frac{1}{2} \times 4V_{OV}^2$$

which results in

$$V_{OV} = 0.316 \text{ V}$$

and thus,

$$V_{GS} = V_t + V_{OV} = 0.5 + 0.316 \simeq 0.82 \text{ V}$$

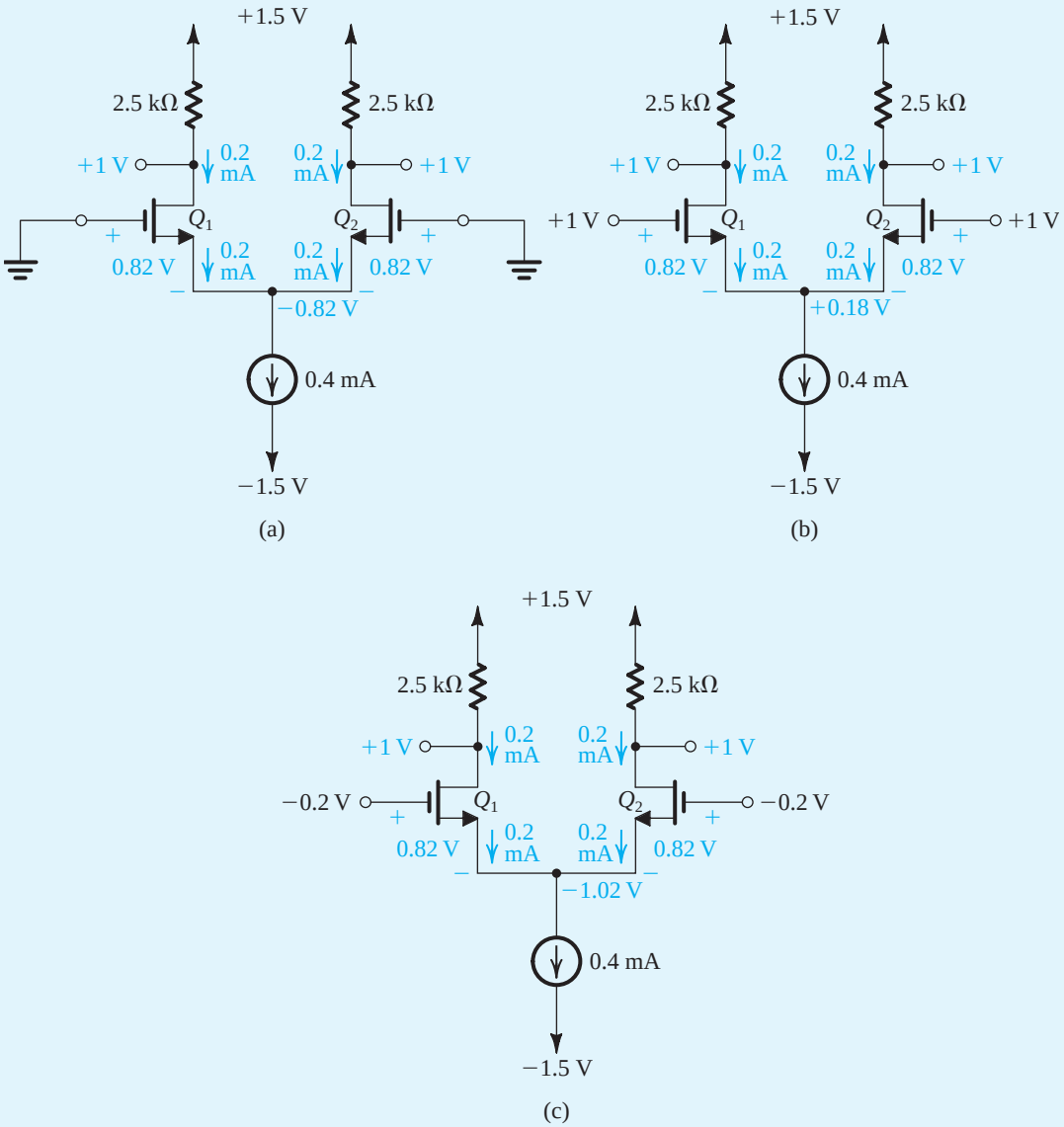


Figure 8.3 Circuits for Example 8.1. Effects of varying V_{CM} on the operation of the differential pair.

(b) The analysis for the case $V_{CM} = 0$ is shown in Fig. 8.3(a) from which we see that

$$V_S = V_G - V_{GS} = 0 - 0.82 = -0.82 \text{ V}$$

$$I_{D1} = I_{D2} = \frac{I}{2} = 0.2 \text{ mA}$$

Example 8.1 *continued*

$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2} R_D$$
$$= 1.5 - 0.2 \times 2.5 = 1 \text{ V}$$

(c) The analysis for the case $V_{CM} = +1$ V is shown in Fig. 8.3(b) from which we see that

$$V_S = V_G - V_{GS} = 1 - 0.82 = +0.18 \text{ V}$$
$$I_{D1} = I_{D2} = \frac{I}{2} = 0.2 \text{ mA}$$
$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2} R_D = 1.5 - 0.2 \times 2.5 = +1 \text{ V}$$

Observe that the transistors remain in the saturation region as assumed. Also observe that I_{D1}, I_{D2}, V_{D1}, and V_{D2} remain unchanged even though the common-mode voltage V_{CM} changed by 1 V.

(d) The analysis for the case $V_{CM} = -0.2$ V is shown in Fig. 8.3(c), from which we see that

$$V_S = V_G - V_{GS} = -0.2 - 0.82 = -1.02 \text{ V}$$

It follows that the current source I now has a voltage across it of

$$V_{CS} = -V_S - (-V_{SS}) = -1.02 + 1.5 = 0.48 \text{ V}$$

which is greater than the minimum required value of 0.4 V. Thus, the current source is still operating properly and delivering a constant current $I = 0.4$ mA and hence

$$I_{D1} = I_{D1} = \frac{I}{2} = 0.2 \text{ mA}$$
$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2} R_D = +1 \text{ V}$$

So, here again the differential circuit is not responsive to the change in the common-mode voltage V_{CM}.

(e) The highest value of V_{CM} is that which causes Q_1 and Q_2 to leave saturation and enter the triode region. Thus,

$$V_{CM\max} = V_t + V_D$$
$$= 0.5 + 1 = +1.5 \text{ V}$$

(f) The lowest value allowed for V_{CM} is that which reduces the voltage across the current source I to the minimum required of $V_{CS} = 0.4$ V. Thus,

$$V_{CM\min} = -V_{SS} + V_{CS} + V_{GS}$$
$$= -1.5 + 0.4 + 0.82 = -0.28 \text{ V}$$

Thus, the input common-mode range is

$$-0.28 \text{ V} \le V_{CM} \le +1.5 \text{ V}$$

EXERCISE

8.1 For the amplifier in Example 8.1, find the input common-mode range for the case in which the two drain resistances R_D are increased by a factor of 2.
Ans. –0.28 V to 1.0 V

8.1.2 Operation with a Differential Input Voltage

Next we apply a difference or differential input voltage by grounding the gate of Q_2 (i.e., setting $v_{G2} = 0$) and applying a signal v_{id} to the gate of Q_1, as shown in Fig. 8.4. We can see that since $v_{id} = v_{GS1} - v_{GS2}$, if v_{id} is positive, v_{GS1} will be greater than v_{GS2} and hence i_{D1} will be greater than i_{D2} and the difference output voltage $(v_{D2} - v_{D1})$ will be positive. On the other hand, when v_{id} is negative, v_{GS1} will be lower than v_{GS2}, i_{D1} will be smaller than i_{D2}, and correspondingly v_{D1} will be higher than v_{D2}; in other words, the difference or differential output voltage $(v_{D2} - v_{D1})$ will be negative.

From the above, we see that the differential pair responds to **difference-mode** or **differential input signals** by providing a corresponding differential output signal between the two drains. At this point, it is useful to inquire about the value of v_{id} that causes the entire bias current I to flow in one of the two transistors. In the positive direction, this happens when v_{GS1} reaches the value that corresponds to $i_{D1} = I$, and v_{GS2} is reduced to a value equal to the threshold voltage V_t, at which point $v_S = -V_t$. The value of v_{GS1} can be found from

$$I = \frac{1}{2}\left(k_n' \frac{W}{L}\right)(v_{GS1} - V_t)^2$$

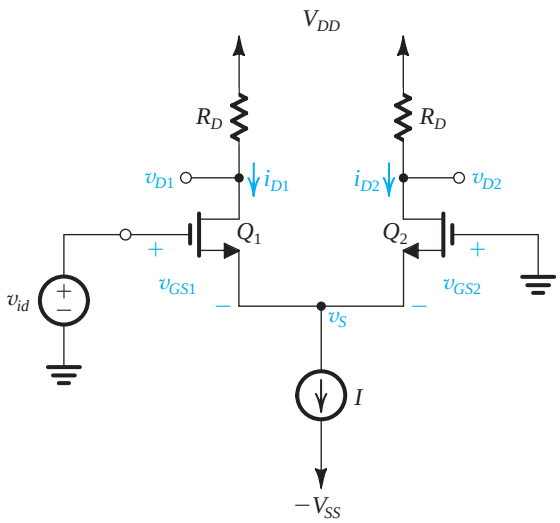


Figure 8.4 The MOS differential pair with a differential input signal v_{id} applied. With v_{id} positive: $v_{GS1} > v_{GS2}$, $i_{D1} > i_{D2}$, and $v_{D1} < v_{D2}$; thus $(v_{D2} - v_{D1})$ will be positive. With v_{id} negative: $v_{GS1} < v_{GS2}$, $i_{D1} < i_{D2}$, and $v_{D1} > v_{D2}$; thus $(v_{D2} - v_{D1})$ will be negative.

as

$$\begin{aligned} v_{GS1} &= V_t + \sqrt{2I/k_n'(W/L)} \\ &= V_t + \sqrt{2}V_{OV} \end{aligned} \tag{8.9}$$

where V_{OV} is the overdrive voltage corresponding to a drain current of $I/2$ (Eq. 8.5). Thus, the value of v_{id} at which the entire bias current I is steered into Q_1 is

$$\begin{aligned} v_{id\max} &= v_{GS1} + v_S \\ &= V_t + \sqrt{2}V_{OV} - V_t \\ &= \sqrt{2}V_{OV} \end{aligned} \tag{8.10}$$

If v_{id} is increased beyond $\sqrt{2}V_{OV}$, i_{D1} remains equal to I, v_{GS1} remains equal to $(V_t + \sqrt{2}V_{OV})$, and v_S rises correspondingly, thus keeping Q_2 off. In a similar manner we can show that in the negative direction, as v_{id} reaches $-\sqrt{2}V_{OV}$, Q_1 turns off and Q_2 conducts the entire bias current I. Thus the current I can be steered from one transistor to the other by varying v_{id} in the range

$$-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV}$$

which defines the range of differential-mode operation. Finally, observe that we have assumed that Q_1 and Q_2 remain in saturation even when one of them is conducting the entire current I.

EXERCISE

8.2 For the MOS differential pair specified in Example 8.1 find (a) the value of v_{id} that causes Q_1 to conduct the entire current I, and the corresponding values of v_{D1} and v_{D2}; (b) the value of v_{id} that causes Q_2 to conduct the entire current I, and the corresponding values of v_{D1} and v_{D2}; (c) the corresponding range of the differential output voltage $(v_{D2} - v_{D1})$.

Ans. (a) +0.45 V, 0.5 V, 1.5 V; (b) –0.45 V, 1.5 V, 0.5 V; (c) +1 V to –1 V

To use the differential pair as a linear amplifier, we keep the differential input signal v_{id} small. As a result, the current in one of the transistors (Q_1 when v_{id} is positive) will increase by an increment ΔI proportional to v_{id}, to $(I/2 + \Delta I)$. Simultaneously, the current in the other transistor will decrease by the same amount to become $(I/2 - \Delta I)$. A voltage signal $-\Delta I R_D$ develops at one of the drains and an opposite-polarity signal, $\Delta I R_D$, develops at the other drain. Thus the output voltage taken between the two drains will be $2\Delta I R_D$, which is proportional to the differential input signal v_{id}. The small-signal operation of the differential pair will be studied in detail in Section 8.2.

8.1.3 Large-Signal Operation

We shall now derive expressions for the drain currents i_{D1} and i_{D2} in terms of the input differential signal $v_{id} \equiv v_{G1} - v_{G2}$. The derivation assumes that the differential pair is perfectly matched and neglects channel-length modulation ($\lambda = 0$). Thus these expressions do not depend on the details of the circuit to which the drains are connected, and we do not show

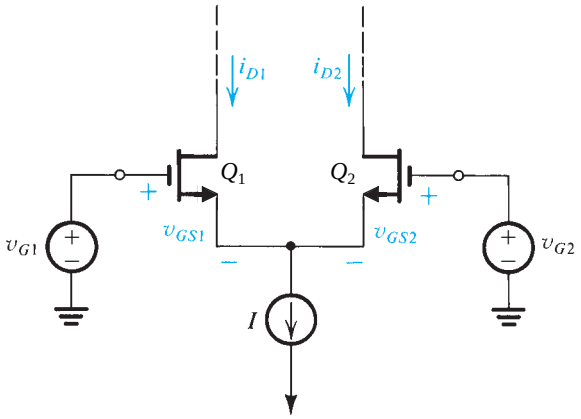


Figure 8.5 The MOSFET differential pair for the purpose of deriving the transfer characteristics, i_{D1} and i_{D2} versus $v_{id} = v_{G1} - v_{G2}$.

these connections in Fig. 8.5; we simply assume that the circuit maintains Q_1 and Q_2 in the saturation region of operation at all times.

To begin with, we express the drain currents of Q_1 and Q_2 as

$$i_{D1} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS1} - V_t)^2 \tag{8.11}$$

$$i_{D2} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS2} - V_t)^2 \tag{8.12}$$

Taking the square roots of both sides of each of Eqs. (8.11) and (8.12), we obtain

$$\sqrt{i_{D1}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} (v_{GS1} - V_t) \tag{8.13}$$

$$\sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} (v_{GS2} - V_t) \tag{8.14}$$

Subtracting Eq. (8.14) from Eq. (8.13) and substituting

$$v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id} \tag{8.15}$$

results in

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} v_{id} \tag{8.16}$$

The constant-current bias imposes the constraint

$$i_{D1} + i_{D2} = I \tag{8.17}$$

Equations (8.16) and (8.17) are two equations in the two unknowns i_{D1} and i_{D2} and can be solved as follows: Squaring both sides of Eq. (8.16) and substituting for $i_{D1} + i_{D2} = I$ gives

$$2\sqrt{i_{D1} i_{D2}} = I - \frac{1}{2} k_n' \frac{W}{L} v_{id}^2$$

Substituting for i_{D2} from Eq. (8.17) as $i_{D2} = I - i_{D1}$ and squaring both sides of the resulting equation provides a quadratic equation in i_{D1} that can be solved to yield

$$i_{D1} = \frac{I}{2} \pm \sqrt{k_n' \frac{W}{L} I} \left(\frac{v_{id}}{2}\right) \sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n' \frac{W}{L}}}$$

Now, since the increment in i_{D1} above the bias value of $I/2$ must have the same polarity as v_{id}, only the root with the "+" sign in the second term is physically meaningful; thus,

$$i_{D1} = \frac{I}{2} + \sqrt{k_n' \frac{W}{L} I} \left(\frac{v_{id}}{2}\right) \sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n' \frac{W}{L}}} \tag{8.18}$$

The corresponding value of i_{D2} is found from $i_{D2} = I - i_{D1}$ as

$$i_{D2} = \frac{I}{2} - \sqrt{k_n' \frac{W}{L} I} \left(\frac{v_{id}}{2}\right) \sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n' \frac{W}{L}}} \tag{8.19}$$

At the bias (quiescent) point, $v_{id} = 0$, leading to

$$i_{D1} = i_{D2} = \frac{I}{2} \tag{8.20}$$

Correspondingly,

$$v_{GS1} = v_{GS2} = V_{GS} \tag{8.21}$$

where

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 \tag{8.22}$$

This relationship enables us to replace $k_n'(W/L)$ in Eqs. (8.18) and (8.19) with I/V_{OV}^2 to express i_{D1} and i_{D2} in the alternative form

$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \tag{8.23}$$

$$i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \tag{8.24}$$

These two equations describe the effect of applying a differential input signal v_{id} on the currents i_{D1} and i_{D2}. They can be used to obtain the normalized plots, i_{D1}/I and i_{D2}/I versus v_{id}/V_{OV}, shown in Fig. 8.6. Note that at $v_{id} = 0$, the two currents are equal to $I/2$. Making v_{id} positive causes i_{D1} to increase and i_{D2} to decrease by equal amounts, to keep the sum constant, $i_{D1} + i_{D2} = I$. The current is steered entirely into Q_1 when v_{id} reaches the value $\sqrt{2}V_{OV}$, as we found out earlier. For v_{id} negative, identical statements can be made by interchanging i_{D1} and i_{D2}. In this case, $v_{id} = -\sqrt{2}V_{OV}$ steers the current entirely into Q_2. Finally, note that the plots in Fig. 8.6 are universal, as they apply to any MOS differential pair.

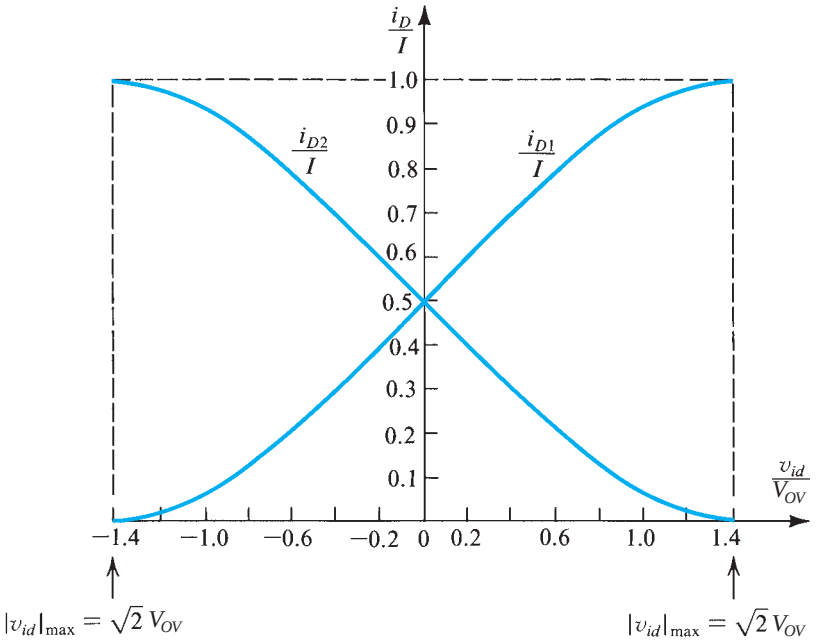


Figure 8.6 Normalized plots of the currents in a MOSFET differential pair. Note that V_{OV} is the overdrive voltage at which Q_1 and Q_2 operate when conducting drain currents equal to $I/2$, the equilibrium situation. Note that these graphs are universal and apply to any MOS differential pair.

The transfer characteristics of Eqs. (8.23) and (8.24) and Fig. 8.6 are obviously nonlinear. This is due to the term involving v_{id}^2. Since we are interested in obtaining linear amplification from the differential pair, we will strive to make this term as small as possible. For a given value of V_{OV}, the only thing we can do is keep $(v_{id}/2)$ much smaller than V_{OV}, which is the condition for the small-signal approximation. It results in

$$i_{D1} \simeq \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \tag{8.25}$$

and

$$i_{D2} \simeq \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \tag{8.26}$$

which, as expected, indicate that i_{D1} increases by an increment i_d, and i_{D2} decreases by the same amount, i_d, where i_d is proportional to the differential input signal v_{id},

$$i_d = \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \tag{8.27}$$

Recalling from our study of the MOSFET in Chapter 5 (also refer to Table 7.A.3), that a MOSFET biased at a current I_D has a transconductance $g_m = 2I_D/V_{OV}$, we recognize the factor (I/V_{OV}) in Eq. (8.27) as g_m of each of Q_1 and Q_2, which are biased at $I_D = I/2$. Now, why $v_{id}/2$? Simply because v_{id} divides equally between the two devices with $v_{gs1} = v_{id}/2$ and $v_{gs2} = -v_{id}/2$, which causes Q_1 to have a current increment i_d and Q_2 to have a current decrement i_d. We shall analyze

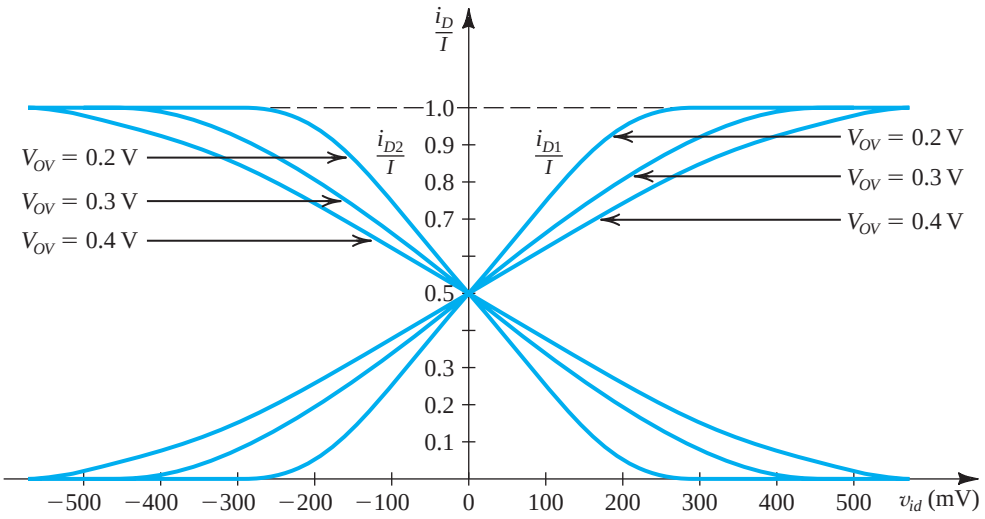


Figure 8.7 The linear range of operation of the MOS differential pair can be extended by operating the transistor at a higher value of V_{OV}.

the small-signal operation of the MOS differential pair shortly. At this time, however, we wish to return to Eqs. (8.23) and (8.24) and note that for a given v_{id}, linearity can be increased by increasing the overdrive voltage V_{OV} at which each of Q_1 and Q_2 is operating. This can be done by using smaller W/L ratios. The price paid for the increased linearity is a reduction in g_m and hence a reduction in gain. In this regard, we observe that the normalized plot of Fig. 8.6, though compact, masks this design degree of freedom. Figure 8.7 shows plots of the transfer characteristics $i_{D1,2}/I$ versus v_{id} for various values of V_{OV}. These graphs clearly illustrate the linearity–transconductance trade-off obtained by changing the value of V_{OV}: The linear range of operation can be extended by operating the MOSFETs at a higher V_{OV} (by using smaller W/L ratios) at the expense of reducing g_m and hence the gain. This trade-off is based on the assumption that the bias current I is being kept constant. The bias current can, of course, be increased to obtain a higher g_m. The expense for doing this, however, is increased power dissipation, a serious limitation in IC design.

EXERCISE

8.3 A MOS differential pair is operated at a bias current I of 0.4 mA. If $\mu_n C_{ox}$ = 0.2 mA/V^2, find the required values of W/L and the resulting g_m if the MOSFETs are operated at V_{OV} = 0.2, 0.3, and 0.4 V. For each value, give the maximum $|v_{id}|$ for which the term involving v_{id}^2 in Eqs. (8.23) and (8.24), namely $((v_{id}/2)/V_{OV})^2$, is limited to 0.1.

Ans.

V_{ov} (V)	0.2	0.3	0.4
W/L	50	22.2	12.5
g_m (mA/V)	2	1.33	1
$\|v_{id}\|_{max}$ (mV)	126	190	253

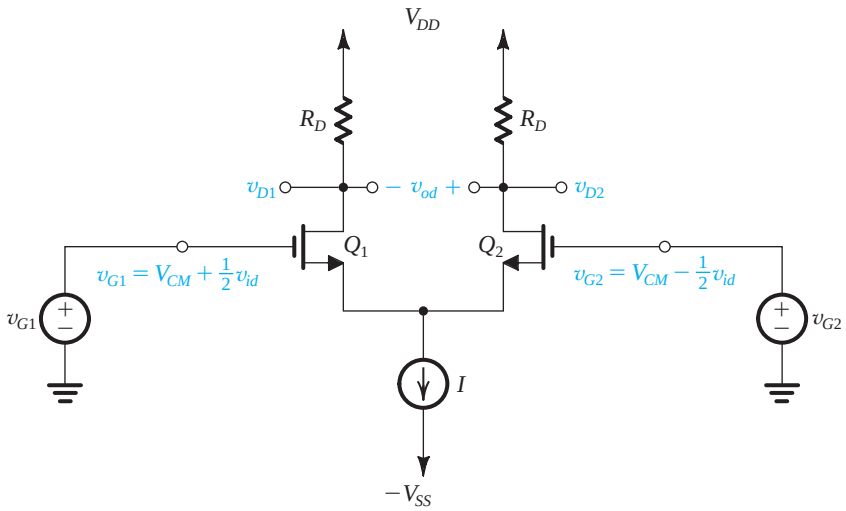
8.2 Small-Signal Operation of the MOS Differential Pair

In this section we build on the understanding gained of the basic operation of the differential pair and consider in some detail its operation as a linear amplifier.

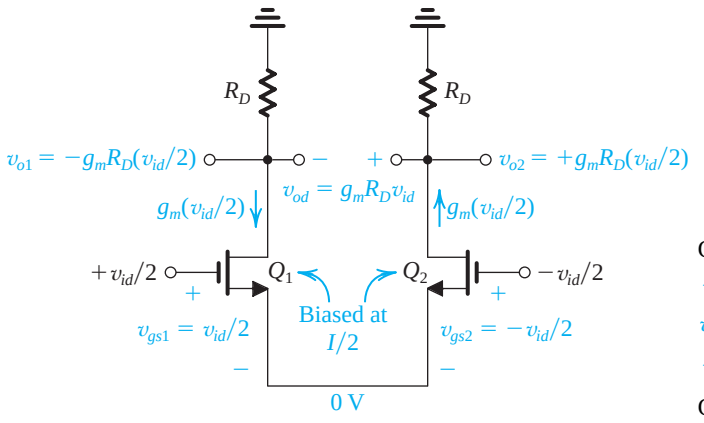
8.2.1 Differential Gain

Figure 8.8(a) shows the MOS differential amplifier with input voltages

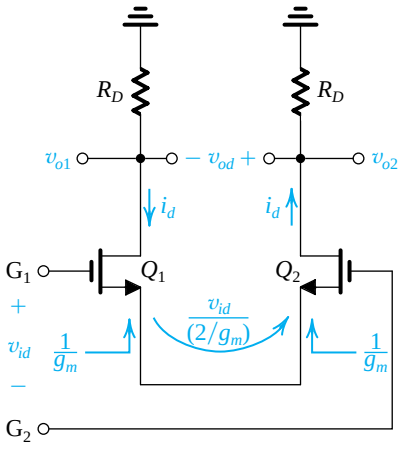
$$v_{G1} = V_{CM} + \tfrac{1}{2}v_{id} \tag{8.28}$$



(a)



(b)



(c)

Figure 8.8 Small-signal analysis of the MOS differential amplifier. **(a)** The circuit with a common-mode voltage applied to set the dc bias voltage at the gates and with v_{id} applied in a complementary (or balanced) manner. **(b)** The circuit prepared for small-signal analysis. **(c)** An alternative way of looking at the small-signal operation of the circuit.

and

$$v_{G2} = V_{CM} - \tfrac{1}{2}v_{id} \tag{8.29}$$

Here, V_{CM} denotes a common-mode dc voltage within the input common-mode range of the differential amplifier. It is needed in order to set the dc voltage of the MOSFET gates. Typically V_{CM} is at the middle value of the power supply. Thus, for our case, where two complementary supplies are utilized, V_{CM} is typically 0 V.

The differential input signal v_{id} is applied in a **complementary** (or **balanced**) manner; that is, v_{G1} is increased by $v_{id}/2$ and v_{G2} is decreased by $v_{id}/2$. This would be the case, for instance, if the differential amplifier were fed from the output of another differential-amplifier stage. Sometimes, however, the differential input is applied in a single-ended fashion, as we saw earlier in Fig. 8.4. The difference in the performance resulting is too subtle a point for our current needs.

As indicated in Fig. 8.8(a) the amplifier output can be taken either between one of the drains and ground or between the two drains. In the first case, the resulting **single-ended outputs** v_{o1} and v_{o2} will be riding on top of the dc voltages at the drains, $(V_{DD} - \frac{I}{2}R_D)$. This is not the case when the output is taken between the two drains; the resulting **differential** output v_{od} (having a 0-V dc component) will be entirely a signal component. We will see shortly that there are other significant advantages to taking the output voltage differentially.

Our objective now is to analyze the small-signal operation of the differential amplifier of Fig. 8.8(a) to determine its voltage gain in response to the differential input signal v_{id}. Toward that end we show in Fig. 8.8(b) the circuit with the power supplies grounded, the bias current source I removed, and V_{CM} eliminated; that is, only signal quantities are indicated. For the time being we will neglect the effect of the MOSFET r_o. Finally note that each of Q_1 and Q_2 is biased at a dc current of $I/2$ and is operating at an overdrive voltage V_{OV}.

From the symmetry of the circuit and because of the balanced manner in which v_{id} is applied, we observe that the signal voltage at the joint source connection must be zero, acting as a sort of **virtual ground**. Thus Q_1 has a gate-to-source voltage signal $v_{gs1} = v_{id}/2$ and Q_2 has $v_{gs2} = -v_{id}/2$. Assuming $v_{id}/2 \ll V_{OV}$, the condition for the small-signal approximation, the changes resulting in the drain currents of Q_1 and Q_2 will be proportional to v_{gs1} and v_{gs2}, respectively. Thus Q_1 will have a drain current increment $g_m(v_{id}/2)$ and Q_2 will have a drain current decrement $g_m(v_{id}/2)$, where g_m denotes the equal transconductances of the two devices,

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}} \tag{8.30}$$

These results correspond to those obtained earlier using the large-signal transfer characteristics and imposing the small-signal condition, Eqs. (8.25) to (8.27).

It is useful at this point to observe again that a signal ground is established at the source terminals of the transistors *without resorting to the use of a large bypass capacitor*, clearly a major advantage of the differential-pair configuration.

The essence of differential-pair operation is that it provides complementary current signals in the drains; what we do with the resulting pair of complementary current signals is, in a sense, a separate issue. Here, of course, we are simply passing the two current signals through a pair of matched resistors, R_D, and thus obtaining the drain voltage signals

$$v_{o1} = -g_m \frac{v_{id}}{2} R_D \tag{8.31}$$

and

$$v_{o2} = +g_m \frac{v_{id}}{2} R_D \tag{8.32}$$

If the output is taken in a single-ended fashion, the resulting gain becomes

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2}g_m R_D \tag{8.33}$$

or

$$\frac{v_{o2}}{v_{id}} = \frac{1}{2}g_m R_D \tag{8.34}$$

Alternatively, if the output is taken differentially, the gain becomes

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D \tag{8.35}$$

Thus another advantage of taking the output differentially is an increase in gain by a factor of 2 (6 dB). It should be noted, however, that although differential outputs are preferred, a single-ended output is needed in some applications. We will have more to say about this later.

An alternative and useful way of viewing the operation of the differential pair in response to a differential input signal v_{id} is illustrated in Fig. 8.8(c). Here we are making use of the fact that the resistance between gate and source of a MOSFET, looking into the source, is $1/g_m$. As a result, between G_1 and G_2 we have a total resistance, in the source circuit, of $2/g_m$. It follows that we can obtain the current i_d simply by dividing v_{id} by $2/g_m$, as indicated in the figure.

8.2.2 The Differential Half-Circuit

When a symmetrical differential amplifier is fed with a differential signal in a balanced manner, as in the case in Fig. 8.8, the performance can be determined by considering only half the circuit. The equivalent differential half-circuit is shown in Fig. 8.9. It has a grounded source, a result of the virtual ground that appears on the common sources' terminal of the MOSFETs in the differential pair. Note that Q_1 is operating at a drain bias current of $(I/2)$ and an overdrive voltage V_{OV}.

The differential gain A_d can be determined directly from the half-circuit. For instance, if we wish to take r_o of Q_1 and Q_2 into account, we can use the half-circuit with the following result:

$$A_d = g_m(R_D \| r_o) \tag{8.36}$$

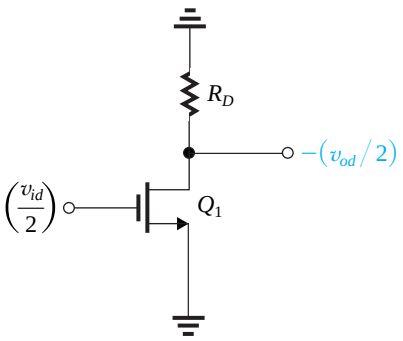


Figure 8.9 The equivalent differential half-circuit of the differential amplifier of Fig. 8.8. Here Q_1 is biased at $I/2$ and is operating at V_{OV}. This circuit can be used to determine the differential voltage gain of the differential amplifier $A_d = v_{od}/v_{id}$.

More significantly, the frequency response of the differential gain can be determined by analyzing the half-circuit, as we shall do in Chapter 9.

Example 8.2

Give the differential half-circuit of the differential amplifier shown in Fig. 8.10(a). Assume that Q_1 and Q_2 are perfectly matched. Neglecting r_o, determine the differential voltage gain $A_d \equiv v_{od}/v_{id}$.

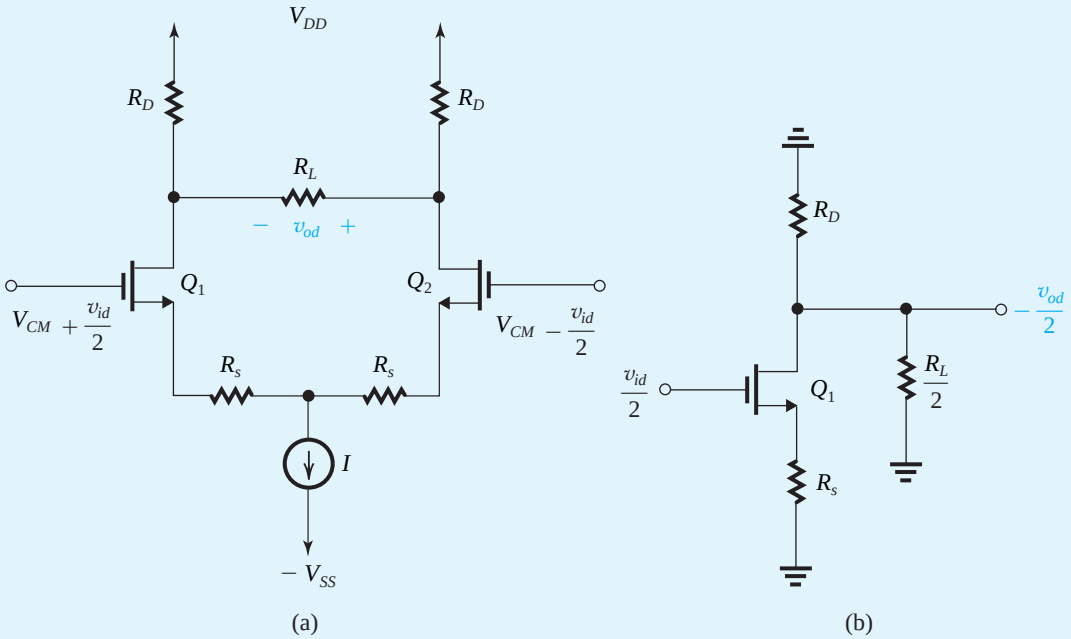


Figure 8.10 (**a**) Differential amplifier for Example 8.2. (**b**) Differential half-circuit.

Solution

Since the circuit is symmetrical and is fed with v_{id} in a balanced manner, the differential half-circuit will be as shown in Fig. 8.10(b). Observe that because the line of symmetry passes through the middle of R_L, the half-circuit has a resistance $R_L/2$ connected between drain and ground. Also note that the virtual ground appears on the node between the two resistances R_s. As a result, the half-circuit has a source-degeneration resistance R_s.

Now, neglecting r_o of the half-circuit transistor Q_1, we can obtain the gain as the ratio of the total resistance in the drain to the total resistance in the source as

$$\frac{-v_{od}/2}{v_{id}/2} = -\frac{R_D \parallel (R_L/2)}{1/g_m + R_s}$$

with the result that

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{R_D \parallel (R_L/2)}{1/g_m + R_s} \tag{8.37}$$

EXERCISE

8.4 A MOS differential amplifier is operated at a total current of 0.8 mA, using transistors with a W/L ratio of 100, $\mu_n C_{ox} = 0.2$ mA/V^2, $V_A = 20$ V, and $R_D = 5$ kΩ. Find V_{OV}, g_m, r_o, and A_d.
Ans. 0.2 V; 4 mA/V; 50 kΩ; 18.2 V/V

8.2.3 The Differential Amplifier with Current-Source Loads

To obtain higher gain, the passive resistances R_D can be replaced with current sources, as shown in Fig. 8.11(a). Here the current sources are realized with PMOS transistors Q_3 and Q_4, and V_G is a dc bias voltage that ensures that Q_3 and Q_4 each conducts a current equal to $I/2$. The differential voltage gain A_d can be found from the differential half-circuit shown in Fig. 8.11(b) as

$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1} \| r_{o3})$$

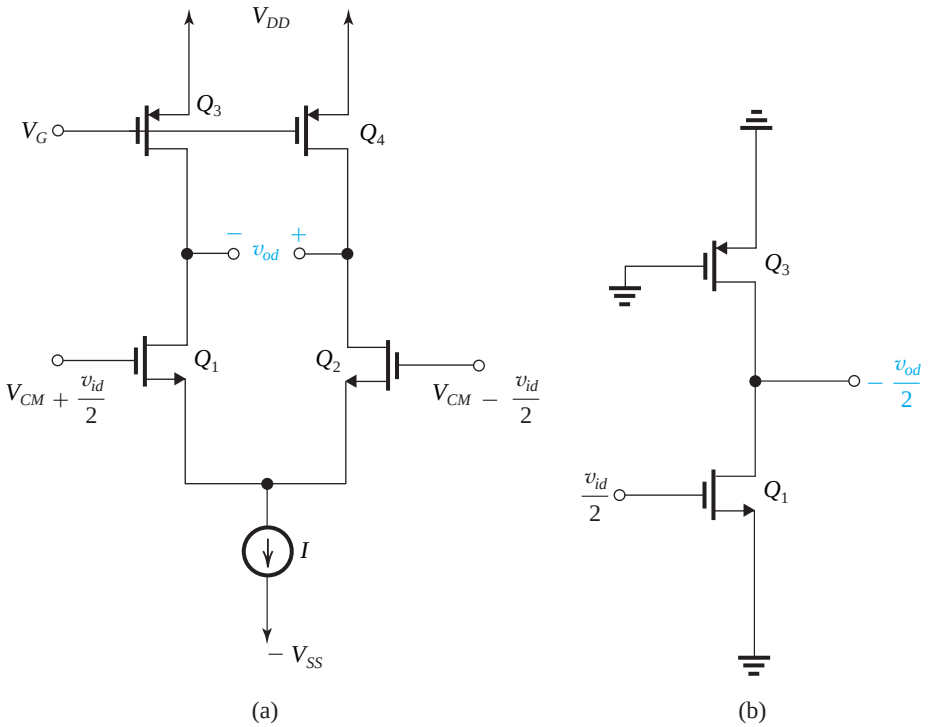


Figure 8.11 **(a)** Differential amplifier with current-source loads formed by Q_3 and Q_4. **(b)** Differential half-circuit of the amplifier in **(a)**.

EXERCISE

8.5 The differential amplifier of Fig. 8.11(a) is fabricated in a 0.18-µm CMOS technology for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 400\ \mu A/V^2$, $|V_t| = 0.5$ V, and $|V_A'| = 10$ V/µm. If the bias current $I = 200$ µA and all transistors have a channel length twice the minimum and are operating at $|V_{OV}| = 0.2$ V, find W/L for each of Q_1, Q_2, Q_3, and Q_4, and determine the differential voltage gain A_d.
Ans. $(W/L)_{1,2} = 12.5$; $(W/L)_{3,4} = 50$; $A_d = 18$ V/V

8.2.4 Cascode Differential Amplifier

The gain of the differential amplifier can be increased by utilizing the cascode configuration studied in Section 7.3. Figure 8.12(a) shows a CMOS differential amplifier with cascoding

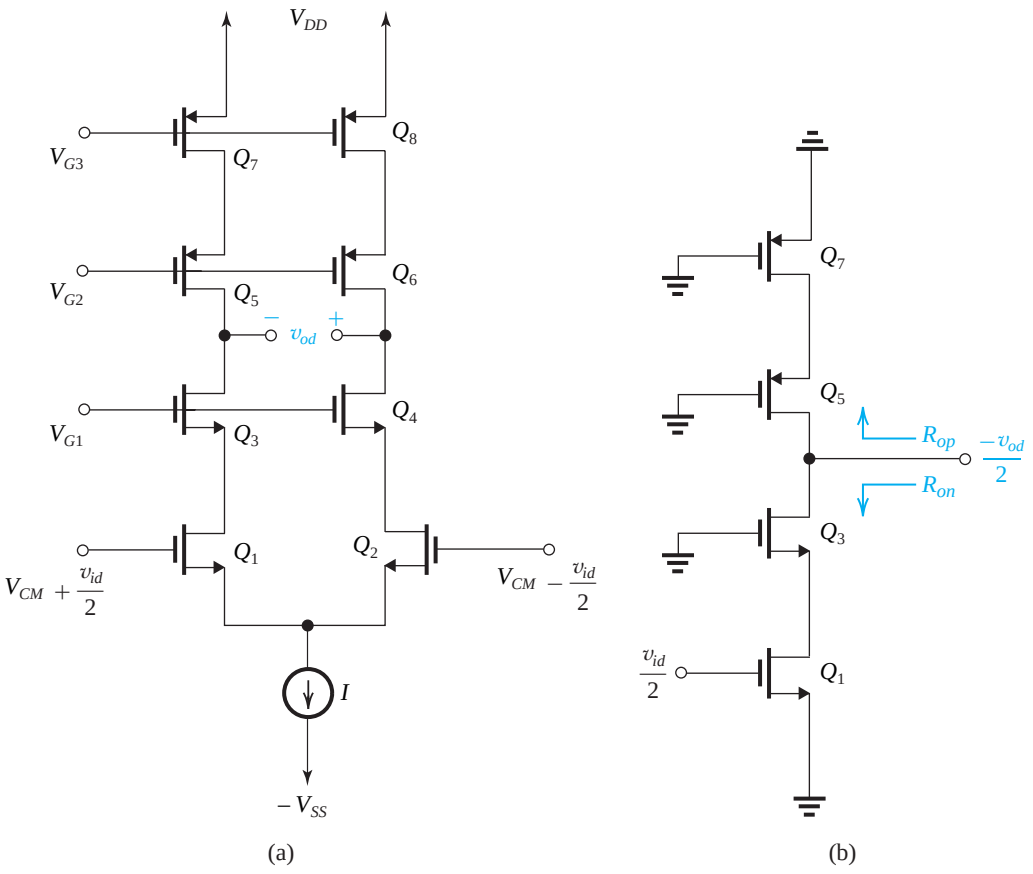


Figure 8.12 **(a)** Cascode differential amplifier; and **(b)** its differential half circuit.

applied to the amplifying transistors Q_1 and Q_2 via transistors Q_3 and Q_4, and to the current-source transistors Q_7 and Q_8 via transistors Q_5 and Q_6. The differential voltage gain can be found from the differential half-circuit shown in Fig. 8.12(b) as

$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}(R_{on} \| R_{op}) \tag{8.38}$$

where

$$R_{on} = (g_{m3}r_{o3})r_{o1} \tag{8.39}$$

and,

$$R_{op} = (g_{m5}r_{o5})r_{o7} \tag{8.40}$$

EXERCISE

8.6 The CMOS cascode differential amplifier of Fig. 8.12(a) is fabricated in a 0.18-μm technology for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 400\ \mu A/V^2$, $|V_t| = 0.5$ V, and $|V_A'| = 10$ V/μm. If the bias current $I = 200$ μA, and all transistors have a channel length twice the minimum and are operating at $|V_{OV}| = 0.2$ V, find W/L for each of Q_1 to Q_8, and determine the differential voltage gain A_d.
Ans. $(W/L)_{1,2,3,4} = 12.5$; $(W/L)_{5,6,7,8} = 50$; $A_d = 648$ V/V

8.2.5 Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)

Thus far, we have seen that the differential amplifier responds to a differential input signal and completely rejects a common-mode signal. This latter point was made very clearly at the outset of our discussion of differential amplifiers and was illustrated in Example 8.1, where we saw that changes in V_{CM} over a wide range resulted in no change in the voltage at either of the two drains. This highly desirable result is, however, a consequence of our assumption that the current source that supplies the bias current I is ideal. As we shall now show, if we consider the more realistic situation of the current source having a finite output resistance R_{SS}, the common-mode gain will no longer be zero.

Figure 8.13(a) shows a MOS differential amplifier biased with a current source having an output resistance R_{SS}. As before, the dc voltage at the input is defined by V_{CM}. Here, however, we also have an incremental signal v_{icm} applied to both input terminals. This common-mode input signal can represent an interference signal or noise that is picked up by both inputs and is clearly undesirable. Our objective now is to find how much of v_{icm} makes its way to the output of the amplifier.

Before we determine the common-mode gain of the amplifier, we wish to address the question of the effect of R_{SS} on the bias current of Q_1 and Q_2. That is, with v_{icm} set to zero, the bias current in each of Q_1 and Q_2 will no longer be $I/2$ but will be larger than $I/2$ by an amount determined by V_{CM} and R_{SS}. However, since R_{SS} is usually very large, this additional dc current in each of Q_1 and Q_2 is usually small and we shall neglect it, thus assuming

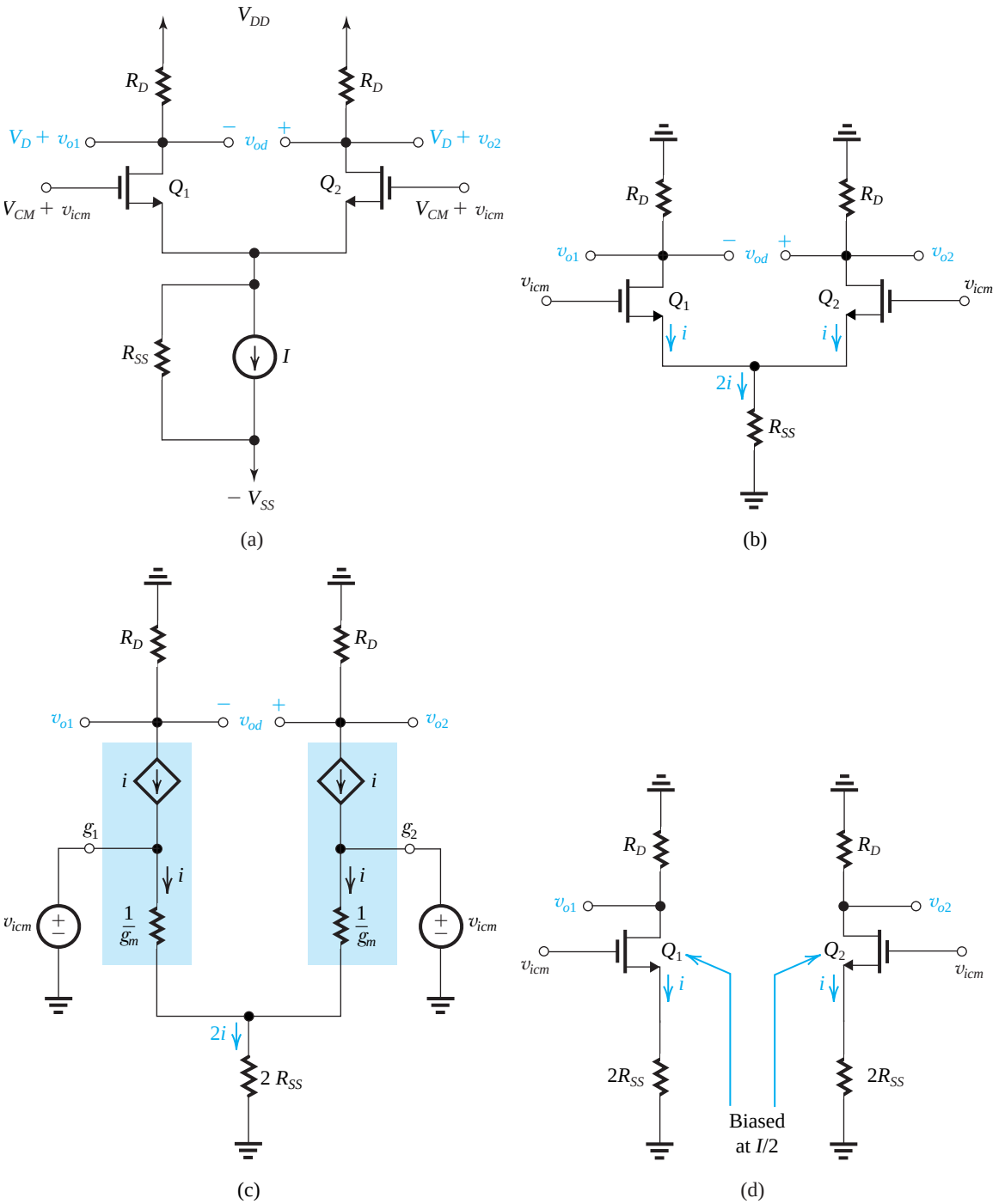


Figure 8.13 **(a)** A MOS differential amplifier with a common-mode input signal v_{icm} superimposed on the input dc common-mode voltage V_{CM}. **(b)** The amplifier circuit prepared for small-signal analysis. **(c)** The amplifier circuit with the transistors replaced with their T model and r_o neglected. **(d)** The circuit in **(b)** split into its two halves; each half is called the "CM half circuit."

that Q_1 and Q_2 continue to operate at a bias current of $I/2$. The reader might also be wondering about the effect of R_{SS} on the differential gain. The answer here is very simple: The virtual ground that develops on the common-source terminal results in a zero signal current through R_{SS}; hence R_{SS} has no effect on the value of A_d.

To determine the response of the differential amplifier to the common-mode input signal v_{icm}, consider the circuit in Fig. 8.13(b), where we have replaced each of V_{DD} and V_{SS} by a short circuit and I by an open circuit. The circuit is obviously symmetrical, and thus the two transistors will carry equal signal currents, denoted i. The value of i can be easily determined by replacing each of Q_1 and Q_2 with its T model and, for simplicity, neglecting r_o. The resulting equivalent circuit is shown in Fig. 8.13(c), from which we can write

$$v_{icm} = \frac{i}{g_m} + 2iR_{SS} \tag{8.41}$$

Thus,

$$i = \frac{v_{icm}}{1/g_m + 2R_{SS}} \tag{8.42}$$

The voltages at the drain of Q_1 and Q_2 can now be found as

$$v_{o1} = v_{o2} = -R_D i$$

resulting in

$$v_{o1} = v_{o2} = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm} \tag{8.43}$$

It follows that both v_{o1} and v_{o2} will be corrupted by the common-mode signal v_{icm} and will be given approximately by

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \simeq -\frac{R_D}{2R_{SS}} \tag{8.44}$$

where we have assumed that $2R_{SS} \gg 1/g_m$. Nevertheless, because $v_{o1} = v_{o2}$, the differential output voltage v_{od} will remain free of common-mode interference:

$$v_{od} = v_{o2} - v_{o1} = 0 \tag{8.45}$$

Thus the circuit still rejects common-mode signals! Unfortunately, however, this will not be the case if the circuit is not perfectly symmetrical, as we shall now show.

Before proceeding further, it is useful to observe that all the above results can be obtained by considering only half the differential amplifier. Figure 8.13(d) shows the two half-circuits of the differential amplifier that apply for common-mode analysis. To see the equivalence, observe that each of the two half-circuits indeed carries a current i given by Eq. (8.42) and the voltages at the source terminals are equal ($v_s = 2iR_{SS}$). Thus the two sources can be joined, returning the circuit to the original form in Fig. 8.13(b). Each of the circuits in Fig. 8.13(d) is known as the **common-mode half-circuit**. Note the difference between the CM half-circuit and the differential half-circuit.

Effect of R_D Mismatch When the two drain resistances exhibit a mismatch ΔR_D, as they inevitably do, the common-mode voltages at the two drains will no longer be equal. Rather, if the load of Q_1 is R_D and that of Q_2 is $(R_D + \Delta R_D)$, the drain signal voltages arising from v_{icm} will be

$$v_{o1} \simeq -\frac{R_D}{2R_{SS}} v_{icm} \tag{8.46}$$

and

$$v_{o2} \simeq -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm} \tag{8.47}$$

Thus,

$$v_{od} = v_{o2} - v_{o1} = -\frac{\Delta R_D}{2R_{SS}} v_{icm} \tag{8.48}$$

and we can find the common-mode gain A_{cm} as

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} \tag{8.49}$$

which can be expressed in the alternate form

$$A_{cm} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right) \tag{8.49′}$$

It follows that a mismatch in the drain resistances causes the differential amplifier to have a finite common-mode gain. Thus, a portion of the interference or noise signal v_{icm} will appear as a component of v_{od}. A measure of the effectiveness of the differential amplifier in amplifying differential-mode signals and rejecting common-mode interference is the ratio of the magnitude of its differential gain $|A_d|$ to the magnitude of its common-mode gain $|A_{cm}|$. This ratio is termed **common-mode rejection ratio (CMRR)**. Thus,

$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|} \tag{8.50a}$$

and is usually expressed in decibels,

$$\text{CMRR (dB)} = 20 \log \frac{|A_d|}{|A_{cm}|} \tag{8.50b}$$

For the case of a MOS differential amplifier with drain resistances R_D that exhibit a mismatch ΔR_D, the CMRR can be found as the ratio of A_d in Eq. (8.35) to A_{cm} in Eq. (8.49), thus

$$\text{CMRR} = (2g_m R_{SS}) \Big/ (\Delta R_D / R_D) \tag{8.50c}$$

It follows that to obtain a high CMRR, we should utilize a bias current source with a high output resistance R_{SS}, and we should strive to obtain a high degree of matching between the drain resistances (i.e., keep $\Delta R_D / R_D$ small).

EXERCISE

8.7 A MOS differential pair operated at a bias current of 0.8 mA employs transistors with $W/L = 100$ and $\mu_n C_{ox} = 0.2$ mA/V^2, using $R_D = 5$ kΩ and $R_{SS} = 25$ kΩ. Find the differential gain, the common-mode gain when the drain resistances have a 1% mismatch, and the CMRR.
Ans. 20 V/V; 0.001 V/V; 86 dB

Effect of g_m Mismatch on CMRR Another possible mismatch between the two halves of the MOS differential pair is a mismatch in g_m of the two transistors. For the purpose of

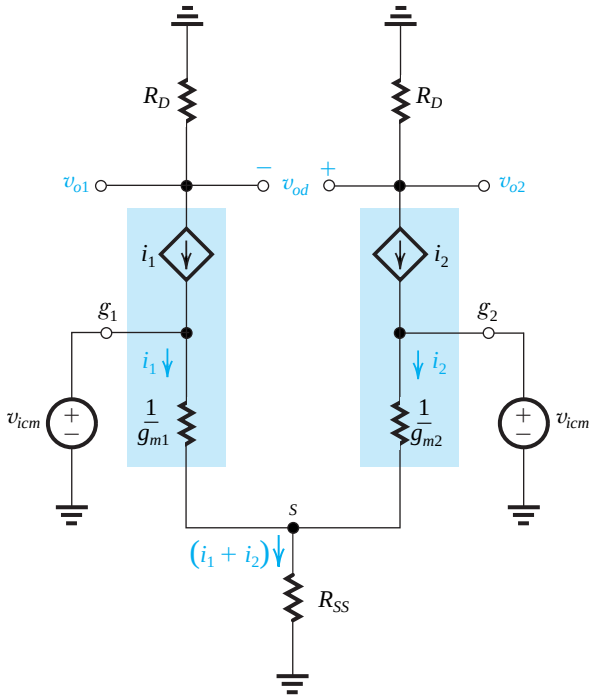


Figure 8.14 Analysis of the MOS differential amplifier with an input common-mode signal v_{icm} in the case the two transistors have a g_m mismatch.

finding the effect of a g_m mismatch on CMRR, let

$$g_{m1} = g_m + \frac{1}{2}\Delta g_m \tag{8.51}$$

$$g_{m2} = g_m - \frac{1}{2}\Delta g_m \tag{8.52}$$

That is,

$$g_{m1} - g_{m2} = \Delta g_m \tag{8.53}$$

Since the circuit is no longer symmetrical, we cannot employ the common-mode half-circuit. Rather, we shall return to the original circuit of Fig. 8.13(a) and replace each of Q_1 and Q_2 with its T equivalent-circuit model. The result is the equivalent circuit shown in Fig. 8.14. Examination of this circuit reveals that the voltages between gate and source for the two transistors are equal (and equal to $v_{icm} - v_s$). Thus,

$$i_1(1/g_{m1}) = i_2(1/g_{m2}) \tag{8.54}$$

From which we can obtain $i_1 + i_2$ as

$$i_1 + i_2 = i_1\left(1 + \frac{g_{m2}}{g_{m1}}\right) \tag{8.55}$$

Now the voltage between the gate of Q_1 and ground which is equal to v_{icm} can be expressed as

$$v_{icm} = i_1/g_{m1} + (i_1 + i_2)R_{SS}$$
$$= i_1/g_{m1} + i_1\left(1 + \frac{g_{m2}}{g_{m1}}\right)R_{SS}$$

which can be rearranged to obtain i_1 in terms of v_{icm} as

$$i_1 = \frac{g_{m1}v_{icm}}{1 + (g_{m1} + g_{m2})R_{SS}} \tag{8.56}$$

We can then use Eq. (8.54) together with Eq. (8.56) to express i_2 as

$$i_2 = \frac{g_{m2}v_{icm}}{1 + (g_{m1} + g_{m2})R_{SS}} \tag{8.57}$$

The voltages v_{o1} and v_{o2} can now be obtained:

$$v_{o1} = -i_1R_D = -\frac{g_{m1}R_D}{1 + (g_{m1} + g_{m2})R_{SS}}v_{icm} \tag{8.58}$$

$$v_{o2} = -i_2R_D = -\frac{g_{m2}R_D}{1 + (g_{m1} + g_{m2})R_{SS}}v_{icm} \tag{8.59}$$

The differential output voltage v_{od} is then obtained as

$$v_{od} = v_{o2} - v_{o1} = \frac{(g_{m1} - g_{m2})R_D}{1 + (g_{m1} + g_{m2})R_{SS}}v_{icm} \tag{8.60}$$

Substituting for g_{m1} and g_{m2} from Eqs. (8.51) and (8.52), respectively, gives

$$v_{od} = \frac{\Delta g_m R_D}{1 + 2\ g_m R_{SS}}v_{icm}$$

Thus the common-mode gain resulting from a mismatch Δg_m can be expressed as

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{\Delta g_m R_D}{1 + 2\ g_m R_{SS}} \tag{8.61}$$

which can be approximated by

$$A_{cm} \simeq \left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m}\right) \tag{8.62}$$

and the corresponding CMRR will be

$$\text{CMRR} = (2g_m R_{SS})\Big/\left(\frac{\Delta g_m}{g_m}\right) \tag{8.63}$$

Thus to keep CMRR high, we have to use a biasing current source with a high output resistance R_{SS} and, of course, strive to maintain a high degree of matching between Q_1 and Q_2.

EXERCISE

8.8 For the MOS amplifier specified in Exercise 8.7, compute the CMRR resulting from a 1% mismatch in g_m.
Ans. 86 dB

Example 8.3

In this example we consider the design of the current source that supplies the bias current of a MOS differential amplifier. Let it be required to achieve a CMRR of 100 dB and assume that the only source of mismatch between Q_1 and Q_2 is a 2% mismatch in their W/L ratios. Let $I = 200\ \mu A$ and assume that all transistors are to be operated at $V_{OV} = 0.2$ V. For the 0.18-μm CMOS fabrication process available, $V_A' = 5$ V/μm. If a simple current source is utilized for I, what channel length is required? If a cascode current source is utilized, what channel length is needed for the two transistors in the cascode?

Solution

A mismatch in W/L results in a g_m mismatch that can be found from the expression of g_m:

$$g_m = \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right) I_D} \tag{8.64}$$

It can be seen that an error of 2% in W/L will result in an error in g_m of 1%. That is, the 2% mismatch in the W/L ratios of Q_1 and Q_2 will result in a 1% mismatch in their g_m values. The resulting CMRR can be found from Eq. (8.64), repeated here:

$$\text{CMRR} = (2g_m R_{SS}) \Big/ \left(\frac{\Delta g_m}{g_m}\right)$$

Now, a 100-dB CMRR corresponds to a ratio of 10^5; thus,

$$10^5 = (2g_m R_{SS})/0.01 \tag{8.65}$$

The value of g_m can be found from

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times (I/2)}{V_{OV}}$$
$$= \frac{2 \times 0.1}{0.2} = 1 \text{ mA/V}$$

Substituting in Eq. (8.65) gives

$$R_{SS} = 500\ \text{k}\Omega$$

Now if the current source is implemented with a single transistor, its r_o must be

$$r_o = R_{SS} = 500\ \text{k}\Omega$$

Thus,

$$\frac{V_A}{I} = 500\ \text{k}\Omega$$

Substituting $I = 200\ \mu A$, we find the required value of V_A as

$$V_A = 100\ \text{V}$$

Since $V_A = V_A' L = 5L$, the required value of L will be

$$L = 20\ \mu\text{m}$$

which is very large!

Example 8.3 *continued*

Using a cascode current source, we have

$$R_{SS} = (g_m r_o) r_o$$

where

$$g_m = \frac{2I}{V_{OV}} = \frac{2 \times 0.2}{0.2} = 2 \text{ mA/V}$$

Thus,

$$500 = 2 \times r_o^2$$

$$r_o = 15.81 \text{ k}\Omega$$

and the required V_A now becomes

$$15.81 = \frac{V_A}{I} = \frac{V_A}{0.2}$$

$$V_A = 3.16 \text{ V}$$

which implies a channel length for each of the two transistors in the cascode of

$$L = \frac{3.16}{V_A'} = \frac{3.16}{5} = 0.63 \text{ μm}$$

a considerable reduction from the case of a simple current source.

Differential versus Single-Ended Output The above study of common-mode rejection was predicated on the assumption that the output of the differential amplifier is taken differentially, that is, between the drains of Q_1 and Q_2. In some cases one might decide to take the output single-endedly; that is, between one of the drains and ground. If this is done, the CMRR is reduced dramatically. This can be seen from the above analysis, where the common-mode gain in the absence of mismatches is zero if the output is taken differentially and finite (Eq. 8.44) if the output is taken single-endedly. When mismatches are taken into account, the CM gain for the differential-output case departs from zero but remains much lower than the value obtained for single-ended output (Eq. 8.44).

We conclude that to obtain a large CMRR, the output of the differential amplifier must be taken differentially. The subject of converting the output signal from differential to single-ended without loss of CMRR will be studied in Section 8.5.

8.3 The BJT Differential Pair

Figure 8.15 shows the basic BJT differential-pair configuration. It is very similar to the MOSFET circuit and consists of two matched transistors, Q_1 and Q_2, whose emitters are joined together and biased by a constant-current source I. The latter is usually implemented by a transistor circuit of the type studied in Sections 7.4 and 7.5. Although each collector is shown connected to the positive supply voltage V_{CC} through a resistance R_C, this connection is not essential to the operation of the differential pair—that is, in some applications the two collectors may be connected to current sources rather than resistive loads. It is essential, though, that the collector circuits be such that Q_1 and Q_2 never enter saturation.

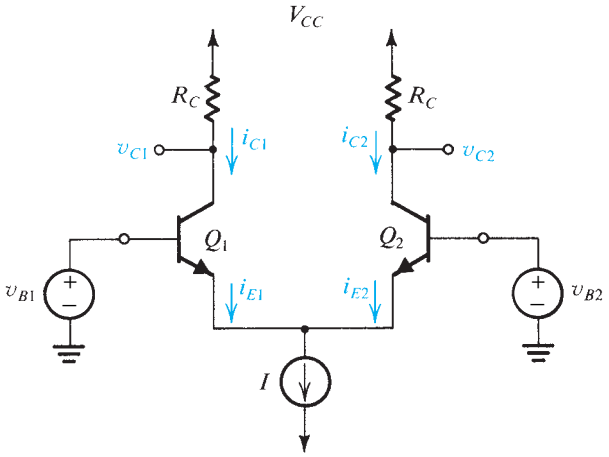


Figure 8.15 The basic BJT differential-pair configuration.

8.3.1 Basic Operation

To see how the BJT differential pair works, consider first the case of the two bases joined together and connected to a common-mode voltage V_{CM}. That is, as shown in Fig. 8.16(a), $v_{B1} = v_{B2} = V_{CM}$. Since Q_1 and Q_2 are matched, and assuming an ideal bias current source I with infinite output resistance, it follows that the current I will remain constant and from symmetry that I will divide equally between the two devices. Thus $i_{E1} = i_{E2} = I/2$, and the voltage at the

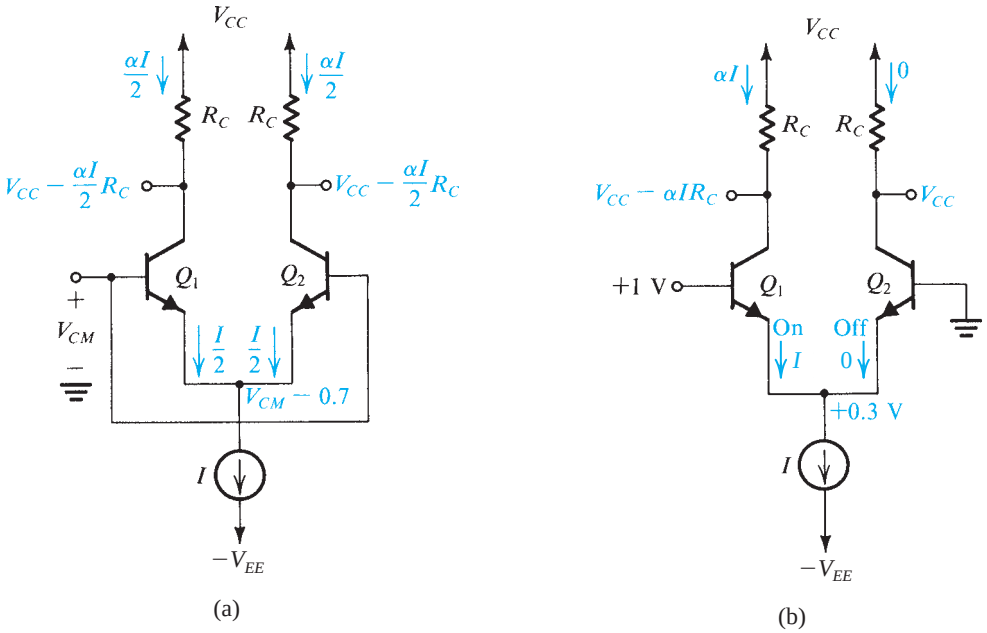


Figure 8.16 Different modes of operation of the BJT differential pair: **(a)** the differential pair with a common-mode input voltage V_{CM}; **(b)** the differential pair with a "large" differential input signal; **(c)** the differential pair with a large differential input signal of polarity opposite to that in **(b)**; **(d)** the differential pair with a small differential input signal v_i. Note that we have assumed the bias current source I to be ideal (i.e., it has an infinite output resistance) and thus I remains constant with the change in V_{CM}.

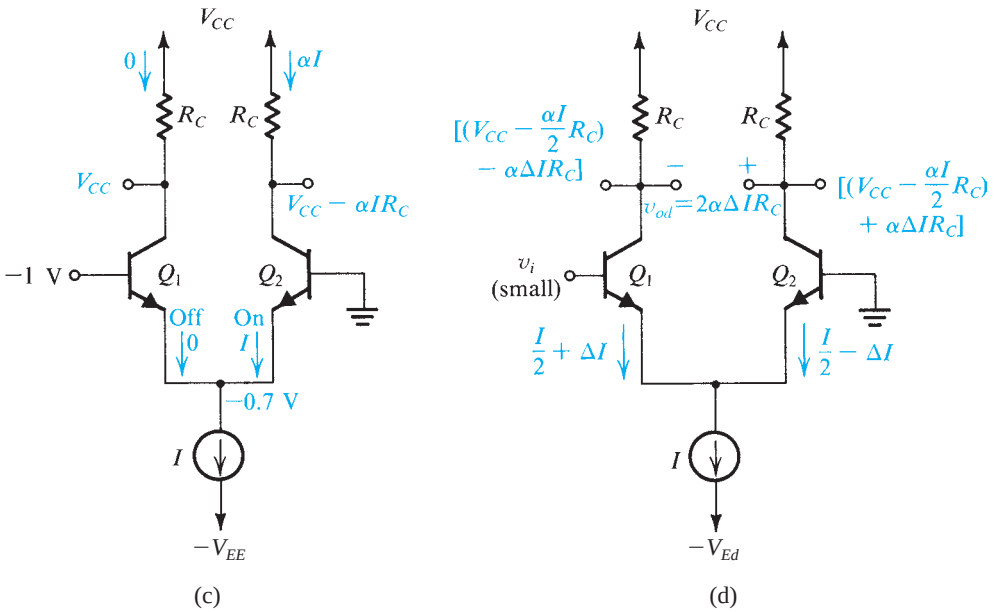


Figure 8.16 *continued.*

emitters will be $V_{CM} - V_{BE}$, where V_{BE} is the base–emitter voltage (assumed in Fig 8.16a to be approximately 0.7 V) corresponding to an emitter current of $I/2$. The voltage at each collector will be $V_{CC} - \frac{1}{2}\alpha I R_C$, and the difference in voltage between the two collectors will be zero.

Now let us vary the value of the common-mode input voltage V_{CM}. Obviously, as long as Q_1 and Q_2 remain in the active region, and the current source I has sufficient voltage across it to operate properly, the current I will still divide equally between Q_1 and Q_2, and the voltages at the collectors will not change. Thus the differential pair does not respond to (i.e., it *rejects*) changes in the common-mode input voltage.

As another experiment, let the voltage v_{B2} be set to a constant value, say, zero (by grounding B_2), and let $v_{B1} = +1$ V (see Fig. 8.16b). With a bit of reasoning it can be seen that Q_1 will be on and conducting all of the current I and that Q_2 will be off. For Q_1 to be on (with $V_{BE1} = 0.7$ V), the emitter has to be at approximately +0.3 V, which keeps the EBJ of Q_2 reverse-biased. The collector voltages will be $v_{C1} = V_{CC} - \alpha I R_C$ and $v_{C2} = V_{CC}$.

Let us now change v_{B1} to −1 V (Fig. 8.16c). Again with some reasoning it can be seen that Q_1 will turn off, and Q_2 will carry all the current I. The common emitter will be at –0.7 V, which means that the EBJ of Q_1 will be reverse biased by 0.3 V. The collector voltages will be $v_{C1} = V_{CC}$ and $v_{C2} = V_{CC} - \alpha I R_C$.

From the foregoing, we see that the differential pair certainly responds to large difference-mode (or differential) signals. In fact, with relatively small difference voltages we are able to steer the entire bias current from one side of the pair to the other. This current-steering property of the differential pair allows it to be used in logic circuits, as will be demonstrated in Chapter 14.

To use the BJT differential pair as a linear amplifier, we apply a very small differential signal (a few millivolts), which will result in one of the transistors conducting a current of $I/2 + \Delta I$; the current in the other transistor will be $I/2 - \Delta I$, with ΔI being proportional to the difference input voltage (see Fig. 8.16d). The output voltage taken between the two collectors will be $2\alpha \Delta I R_C$, which is proportional to the differential input signal v_i. The small-signal operation of the differential pair will be studied shortly.

EXERCISE

8.9 Find v_E, v_{C1}, and v_{C2} in the circuit of Fig. E8.9. Assume that $|v_{BE}|$ of a conducting transistor is approximately 0.7 V and that $\alpha \simeq 1$.

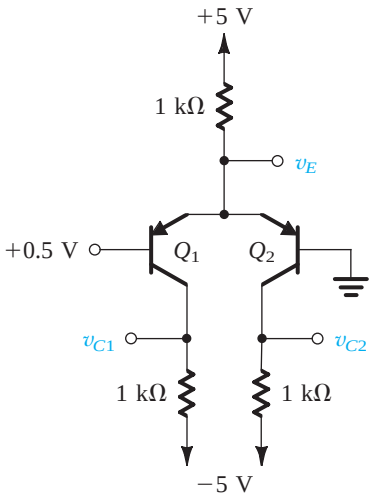


Figure E8.9

Ans. +0.7 V; –5 V; –0.7 V

8.3.2 Input Common-Mode Range

Refer to the circuit in Fig. 8.16(a). The allowable range of V_{CM} is determined at the upper end by Q_1 and Q_2 leaving the active mode and entering saturation. Thus

$$V_{CM\max} \simeq V_C + 0.4 = V_{CC} - \alpha\frac{I}{2}R_C + 0.4 \tag{8.66}$$

The lower end of the V_{CM} range is determined by the need to provide a certain minimum voltage V_{CS} across the current source I to ensure its proper operation. Thus,

$$V_{CM\min} = -V_{EE} + V_{CS} + V_{BE} \tag{8.67}$$

EXERCISE

8.10 Determine the input common-mode range for a bipolar differential amplifier operating from ±2.5-V power supplies and biased with a simple current source that delivers a constant current of 0.4 mA and requires a minimum of 0.3 V for its proper operation. The collector resistances $R_C = 5$ kΩ.

Ans. –1.5 V to +1.9 V

8.3.3 Large-Signal Operation

We now present a general analysis of the BJT differential pair of Fig. 8.15. If we denote the voltage at the common emitter by v_E and neglecting the Early effect, the exponential relationship applied to each of the two transistors may be written

$$i_{E1} = \frac{I_S}{\alpha} e^{(v_{B1}-v_E)/V_T} \tag{8.68}$$

$$i_{E2} = \frac{I_S}{\alpha} e^{(v_{B2}-v_E)/V_T} \tag{8.69}$$

These two equations can be combined to obtain

$$\frac{i_{E1}}{i_{E2}} = e^{(v_{B1}-v_{B2})/V_T}$$

which can be manipulated to yield

$$\frac{i_{E1}}{i_{E1}+i_{E2}} = \frac{1}{1+e^{(v_{B2}-v_{B1})/V_T}} \tag{8.70}$$

$$\frac{i_{E2}}{i_{E1}+i_{E2}} = \frac{1}{1+e^{(v_{B1}-v_{B2})/V_T}} \tag{8.71}$$

The circuit imposes the additional constraint

$$i_{E1} + i_{E2} = I \tag{8.72}$$

Using Eq. (8.72) together with Eqs. (8.70) and (8.71) and substituting $v_{B1} - v_{B2} = v_{id}$ gives

$$i_{E1} = \frac{I}{1+e^{-v_{id}/V_T}} \tag{8.73}$$

$$i_{E2} = \frac{I}{1+e^{v_{id}/V_T}} \tag{8.74}$$

The collector currents i_{C1} and i_{C2} can be obtained simply by multiplying the emitter currents in Eqs. (8.73) and (8.74) by α, which is normally very close to unity.

The fundamental operation of the differential amplifier is illustrated by Eqs. (8.73) and (8.74). First, note that the amplifier responds only to the difference voltage v_{id}. That is, if $v_{B1} = v_{B2} = V_{CM}$, the current I divides equally between the two transistors irrespective of the value of the common-mode voltage V_{CM}. This is the essence of differential-amplifier operation, which also gives rise to its name.

Another important observation is that a relatively small difference voltage v_{id} will cause the current I to flow almost entirely in one of the two transistors. Figure 8.17 shows a plot of the two collector currents (assuming $\alpha \simeq 1$) as a function of the differential input signal. This is a normalized plot that can be used universally. Observe that a difference voltage of about $4V_T$ ($\simeq$100 mV) is sufficient to switch the current almost entirely to one side of the BJT pair. Note that this is much smaller than the corresponding voltage for the MOS pair, $\sqrt{2}V_{OV}$. The fact that such a small signal can switch the current from one side of the BJT differential pair to the other means that the BJT differential pair can be used as a fast current switch (Chapter 14).

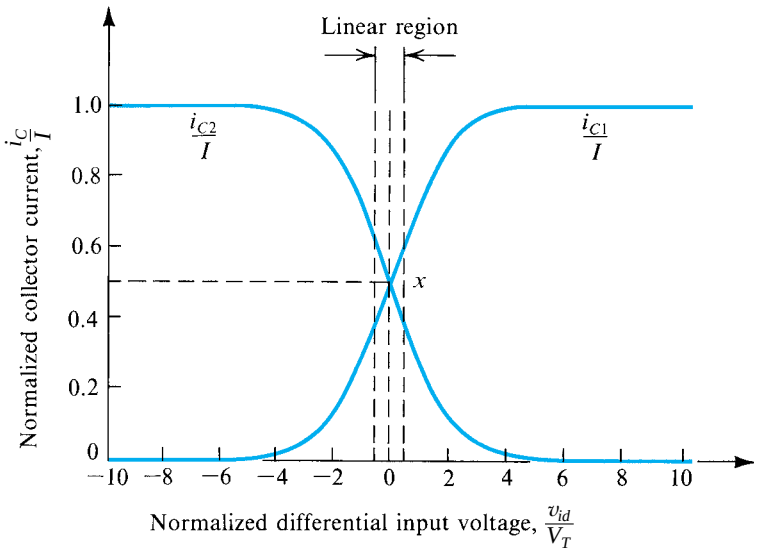


Figure 8.17 Transfer characteristics of the BJT differential pair of Fig. 8.15 assuming $\alpha \simeq 1$.

The nonlinear transfer characteristics of the differential pair, shown in Fig. 8.17, will not be utilized any further in this chapter. Rather, in the following we shall be interested specifically in the application of the differential pair as a small-signal amplifier. For this purpose, the difference input signal is limited to less than about $V_T/2$ in order that we may operate on a linear segment of the characteristics around the midpoint x (in Fig. 8.17).

Before leaving the large-signal operation of the differential BJT pair, we wish to point out an effective technique frequently employed to extend the linear range of operation. It consists of including two equal resistances R_e in series with the emitters of Q_1 and Q_2, as shown in Fig. 8.18(a). The resulting transfer characteristics for three different values of R_e are sketched in Fig. 8.18(b). Observe that expansion of the linear range is obtained at the expense of reduced G_m (which is the slope of the transfer curve at $v_{id} = 0$) and hence reduced gain. This result should come as no surprise; R_e here is performing in exactly the same way as the emitter resistance R_e does in the CE amplifier with emitter degeneration (see Section 6.6.4). Finally, we also note that this linearization technique is in effect the bipolar counterpart of the technique employed for the MOS differential pair (Fig. 8.7). In the latter case, however, V_{OV} was varied by changing the transistors' W/L ratio, a design tool with no counterpart in the BJT.

EXERCISE

8.11 For the BJT differential pair of Fig. 8.15, find the value of input differential signal that is sufficient to cause $i_{E1} = 0.99I$.
Ans. 115 mV

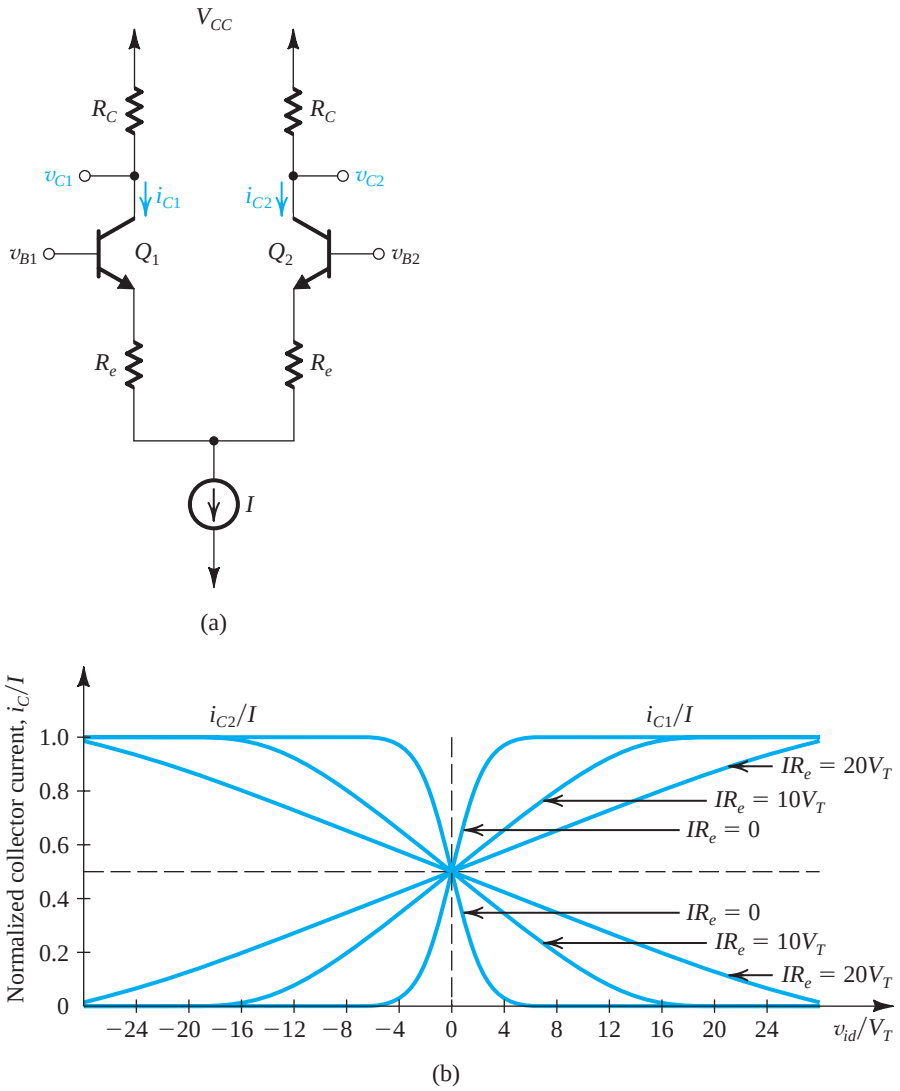


Figure 8.18 The transfer characteristics of the BJT differential pair **(a)** can be linearized **(b)** (i.e., the linear range of operation can be extended) by including resistances in the emitters.

8.3.4 Small-Signal Operation

In this section we shall study the application of the BJT differential pair in small-signal amplification. Figure 8.19 shows the BJT differential pair with a difference voltage signal v_{id} applied between the two bases. Implied is that the dc level at the input—that is, the common-mode input voltage—has been somehow established. For instance, one of the two input terminals can be grounded and v_{id} applied to the other input terminal. Alternatively, the differential amplifier may be fed from the output of another differential amplifier. In the latter case, the voltage at one of the input terminals will be $V_{CM} + v_{id}/2$ while that at the other input terminal will be $V_{CM} - v_{id}/2$.

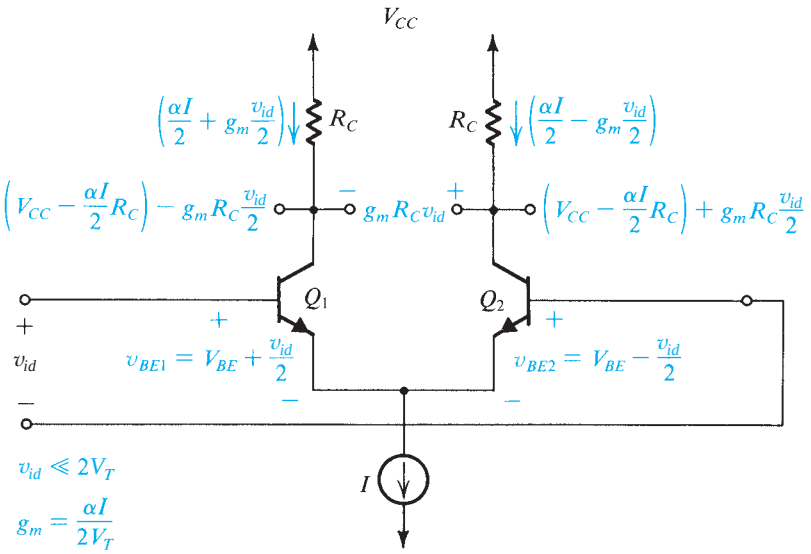


Figure 8.19 The currents and voltages in the differential amplifier when a small differential input signal v_{id} is applied.

The Collector Currents When v_{id} Is Applied For the circuit of Fig. 8.19, we may use Eqs. (8.73) and (8.74) to write

$$i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}} \tag{8.75}$$

$$i_{C2} = \frac{\alpha I}{1 + e^{v_{id}/V_T}} \tag{8.76}$$

Multiplying the numerator and the denominator of the right-hand side of Eq. (8.75) by $e^{v_{id}/2V_T}$ gives

$$i_{C1} = \frac{\alpha I e^{v_{id}/2V_T}}{e^{v_{id}/2V_T} + e^{-v_{id}/2V_T}}$$

Assume that $v_{id} \ll 2V_T$. We may thus expand the exponential $e^{\pm v_{id}/2V_T}$ in a series and retain only the first two terms:

$$i_{C1} \simeq \frac{\alpha I(1 + v_{id}/2V_T)}{1 + v_{id}/2V_T + 1 - v_{id}/2V_T}$$

Thus

$$i_{C1} = \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \tag{8.77}$$

Similar manipulations can be applied to Eq. (8.76) to obtain

$$i_{C2} = \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \tag{8.78}$$

Equations (8.77) and (8.78) tell us that when $v_{id} = 0$, the bias current I divides equally between the two transistors of the pair. Thus each transistor is biased at an emitter current of $I/2$. When a "small-signal" v_{id} is applied differentially (i.e., between the two bases), the collector current

of Q_1 increases by an increment i_c and that of Q_2 decreases by an equal amount. This ensures that the sum of the total currents in Q_1 and Q_2 remains constant, as constrained by the current-source bias. The incremental (or signal) current component i_c is given by

$$i_c = \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \tag{8.79}$$

Equation (8.79) has an easy interpretation. First, note from the symmetry of the circuit (Fig. 8.19) that the differential signal v_{id} should divide equally between the base–emitter junctions of the two transistors. Thus the total base–emitter voltages will be

$$v_{BE}|_{Q1} = V_{BE} + \frac{v_{id}}{2}$$

$$v_{BE}|_{Q2} = V_{BE} - \frac{v_{id}}{2}$$

where V_{BE} is the dc BE voltage corresponding to an emitter current of $I/2$. Therefore, the collector current of Q_1 will increase by $g_m v_{id}/2$ and the collector current of Q_2 will decrease by $g_m v_{id}/2$. Here g_m denotes the transconductance of Q_1 and of Q_2, which are equal and given by

$$g_m = \frac{I_C}{V_T} = \frac{\alpha I/2}{V_T} \tag{8.80}$$

Thus Eq. (8.79) simply states that $i_c = g_m v_{id}/2$.

An Alternative Viewpoint There is an extremely useful alternative interpretation of the results above. Assume the current source I to be ideal. Its incremental resistance then will be infinite. Thus the voltage v_{id} appears across a total resistance of $2r_e$, where

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{I/2} \tag{8.81}$$

Correspondingly there will be a signal current i_e, as illustrated in Fig. 8.20, given by

$$i_e = \frac{v_{id}}{2r_e} \tag{8.82}$$

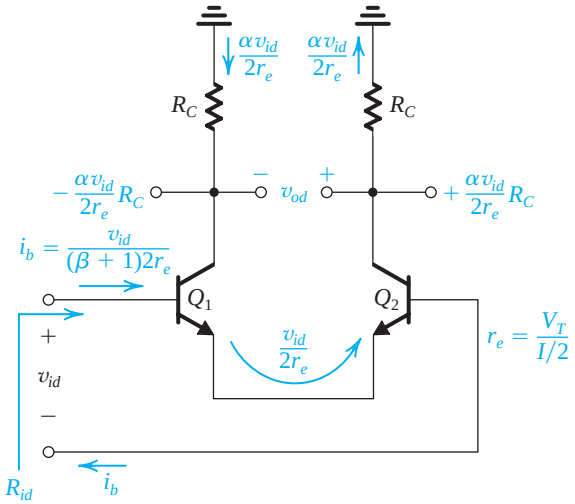


Figure 8.20 A simple technique for determining the signal currents in a differential amplifier excited by a differential voltage signal v_{id}; dc quantities are not shown.

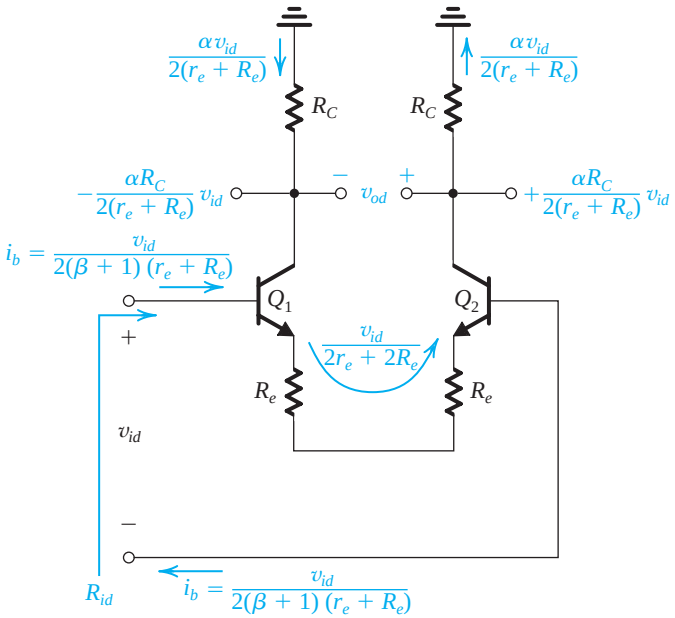


Figure 8.21 A differential amplifier with emitter resistances. Only signal quantities are shown (in color).

Thus the collector of Q_1 will exhibit a current increment i_c and the collector of Q_2 will exhibit a current decrement i_c:

$$i_c = \alpha i_e = \frac{\alpha v_{id}}{2r_e} = g_m \frac{v_{id}}{2} \tag{8.83}$$

Note that in Fig. 8.20 we have shown signal quantities only. It is implied, of course, that each transistor is biased at an emitter current of $I/2$.

This method of analysis is particularly useful when resistances are included in the emitters, as shown in Fig. 8.21. For this circuit we have

$$i_e = \frac{v_{id}}{2r_e + 2R_e} \tag{8.84}$$

Input Differential Resistance Unlike the MOS differential amplifier, which has an infinite input resistance, the bipolar differential pair exhibits a finite input resistance, a result of the finite β of the BJT.

The input differential resistance is the resistance seen between the two bases; that is, it is the resistance seen by the differential input signal v_{id}. For the differential amplifier in Figs. 8.19 and 8.20 it can be seen that the base current of Q_1 shows an increment i_b and the base current of Q_2 shows an equal decrement,

$$i_b = \frac{i_e}{\beta + 1} = \frac{v_{id}/2r_e}{\beta + 1} \tag{8.85}$$

Thus the differential input resistance R_{id} is given by

$$R_{id} \equiv \frac{v_{id}}{i_b} = (\beta + 1)2r_e = 2r_\pi \tag{8.86}$$

This result is just a restatement of the familiar resistance-reflection rule; namely, *the resistance seen between the two bases is equal to the total resistance in the emitter circuit multiplied by* $(\beta+1)$. We can employ this rule to find the input differential resistance for the circuit in Fig. 8.21 as

$$R_{id} = (\beta + 1)(2r_e + 2R_e) \tag{8.87}$$

Differential Voltage Gain We have established that for small difference input voltages ($v_{id} \ll 2V_T$; i.e., v_{id} smaller than about 20 mV), the collector currents are given by

$$i_{C1} = I_C + g_m \frac{v_{id}}{2} \tag{8.88}$$

$$i_{C2} = I_C - g_m \frac{v_{id}}{2} \tag{8.89}$$

where

$$I_C = \frac{\alpha I}{2} \tag{8.90}$$

Thus the total voltages at the collectors will be

$$v_{C1} = (V_{CC} - I_C R_C) - g_m R_C \frac{v_{id}}{2} \tag{8.91}$$

$$v_{C2} = (V_{CC} - I_C R_C) + g_m R_C \frac{v_{id}}{2} \tag{8.92}$$

The quantities in parentheses are simply the dc voltages at each of the two collectors.

As in the MOS case, the output voltage signal of a bipolar differential amplifier can be taken *differentially* (i.e., between the two collectors, $v_{od} = v_{c2} - v_{c1}$). The differential gain of the differential amplifier will be

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_C \tag{8.93}$$

For the differential amplifier with resistances in the emitter leads (Fig. 8.21), the differential gain is given by

$$A_d = \frac{\alpha(2R_C)}{2r_e + 2R_e} \simeq \frac{R_C}{r_e + R_e} \tag{8.94}$$

This equation is a familiar one: It states that *the voltage gain is equal to the ratio of the total resistance in the collector circuit* $(2R_C)$ *to the total resistance in the emitter circuit* $(2r_e + 2R_e)$.

The Differential Half-Circuit As in the MOS case, the differential gain of the BJT differential amplifier can be obtained by considering its differential half-circuit. Figure 8.22(a) shows a differential amplifier fed by a differential signal v_{id} that is applied in a **complementary** (**push–pull** or **balanced**) manner. That is, while the base of Q_1 is raised by $v_{id}/2$, the base of Q_2 is lowered by $v_{id}/2$. We have also included the output resistance R_{EE} of the bias current source. From symmetry, it follows that the signal voltage at the emitters will be zero. Thus the circuit is equivalent to the two common-emitter amplifiers shown in Fig. 8.22(b), where each of the two transistors is biased at an emitter current of $I/2$. Note that the finite output resistance R_{EE} of the current source will have no effect on the operation. The equivalent circuit in Fig. 8.22(b) is valid for differential operation only.

In many applications the differential amplifier is not fed in a complementary fashion; rather, the input signal may be applied to one of the input terminals while the other terminal

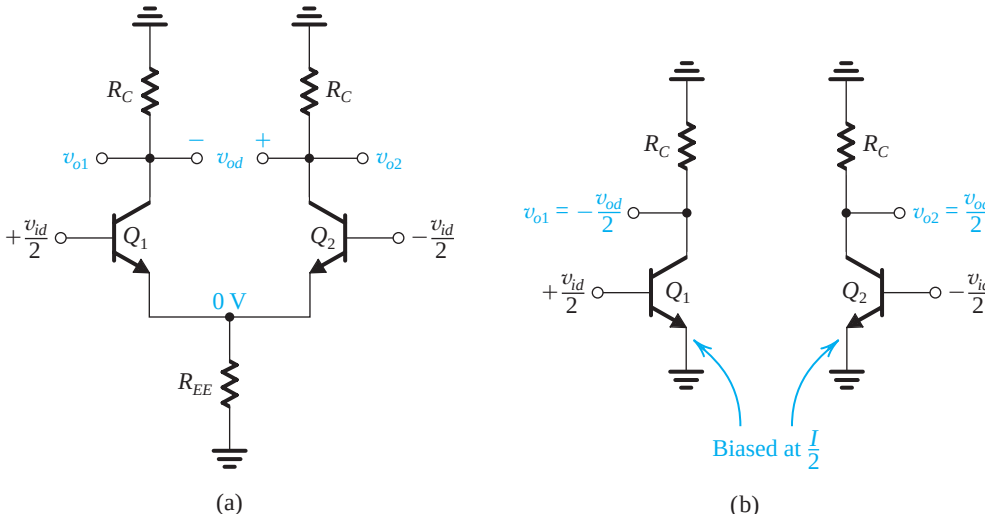


Figure 8.22 Equivalence of the BJT differential amplifier in **(a)** to the two common-emitter amplifiers in **(b).** This equivalence applies only for differential input signals. Either of the two common-emitter amplifiers in **(b)** can be used to find the differential gain, differential input resistance, frequency response, and so on, of the differential amplifier.

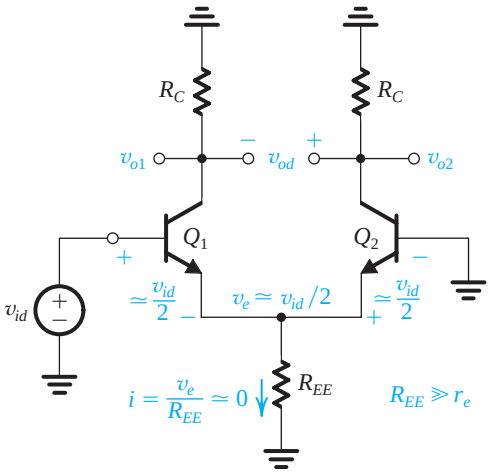


Figure 8.23 The differential amplifier fed in a single-ended fashion.

is grounded, as shown in Fig. 8.23. In this case the signal voltage at the emitters will not be zero, and thus the resistance R_{EE} will have an effect on the operation. Nevertheless, if R_{EE} is large ($R_{EE} \gg r_e$), as is usually the case,[1] then v_{id} will still divide equally (approximately) between the two junctions, as shown in Fig. 8.23. Thus the operation of the differential amplifier in this case will be almost identical to that in the case of symmetric feed, and the common-emitter equivalence can still be employed.

Since in Fig. 8.22, $v_{o2} = -v_{o1} = v_{od}/2$, the two common-emitter transistors in Fig. 8.22(b) yield similar results about the performance of the differential amplifier. Thus only one is needed to analyze the differential small-signal operation of the differential amplifier, and it

[1]Note that R_{EE} appears in parallel with the much smaller r_e of Q_2.

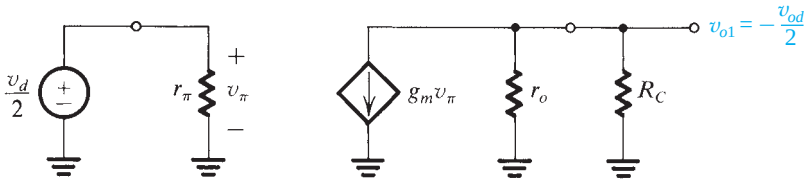


Figure 8.24 Equivalent-circuit model of the differential half-circuit formed by Q_1 in Fig. 8.22(b).

is known as the **differential half-circuit**. If we take the common-emitter transistor fed with $+v_{id}/2$ as the differential half-circuit and replace the transistor with its low-frequency, equivalent-circuit model, the circuit in Fig. 8.24 results. In evaluating the model parameters r_π, g_m, and r_o, we must recall that the half-circuit is biased at $I/2$. The voltage gain of the differential amplifier is equal to the voltage gain of the half-circuit—that is, $v_{o1}/(v_{id}/2)$. Here, we note that including r_o will modify the gain expression in Eq. (8.93) to

$$A_d = g_m(R_C \parallel r_o) \tag{8.95}$$

The input differential resistance of the differential amplifier is twice that of the half-circuit—that is, $2r_\pi$. Finally, we note that the differential half-circuit of the amplifier of Fig. 8.21 is a common-emitter transistor with a resistance R_e in the emitter lead.

8.3.5 Common-Mode Gain and CMRR

Figure 8.25 shows a bipolar differential amplifier with an input common-mode signal v_{icm}. Here R_{EE} is the output resistance of the bias current source I. We wish to find the voltages that result from v_{icm} at the collectors of Q_1 and Q_2, v_{o1} and v_{o2}, and between the two collectors, v_{od}. Toward that end, we make use of the **common-mode half-circuits** shown in Fig. 8.25(b). The signal v_{o1} that appears at the collector of Q_1 in response to v_{icm} will be

$$v_{o1} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \tag{8.96}$$

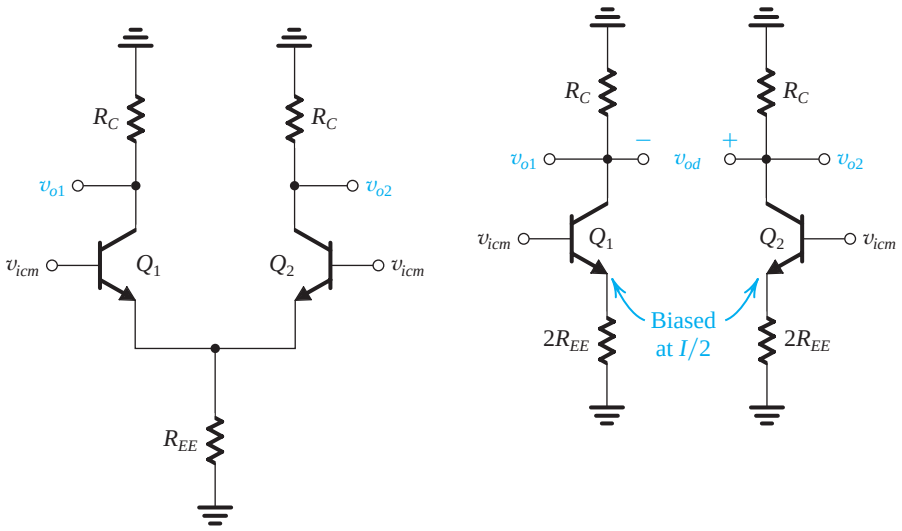
Similarly, v_{o2} will be

$$v_{o2} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \tag{8.97}$$

where we have neglected the transistor r_o, for simplicity. The differential output signal v_{od} can be obtained as

$$v_{od} = v_{o2} - v_{o1} = 0$$

Thus, while the voltages at the two collectors will contain common-mode noise or interference components, the output differential voltage will be free from such interference. This condition, however, is based on the assumption of perfect matching between the two sides of the differential amplifier. Any mismatch will result in v_{od} acquiring a component proportional to v_{icm}. For example, consider the case of a mismatch ΔR_C between the two collector resistances: If the collector of Q_1 has a collector resistance R_C,



(a) (b)

Figure 8.25 **(a)** The differential amplifier fed by a common-mode input signal v_{icm}. **(b)** Equivalent "half-circuits" for common-mode calculations.

$$v_{o1} = -\frac{\alpha R_C}{2R_{EE} + r_e} v_{icm}$$

and the collector of Q_2 has a collector resistance $(R_C + \Delta R_C)$,

$$v_{o2} = -\frac{\alpha(R_C + \Delta R_C)}{2R_{EE} + r_e} v_{icm}$$

then the differential output voltage v_{od} will be

$$\begin{aligned} v_{od} &\equiv v_{o2} - v_{o1} \\ &= -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} v_{icm} \end{aligned}$$

and the common-mode gain will be

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} \tag{8.98}$$

Since $\alpha \simeq 1$, $r_e \ll 2R_{EE}$, Eq. (8.98) can be approximated and written in the form

$$A_{cm} \simeq -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta R_C}{R_C}\right) \tag{8.99}$$

The common-mode rejection ratio can now be found from

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|}$$

together with using Eqs. (8.93) and (8.99), with the result that

$$\text{CMRR} = (2g_m R_{EE}) \Big/ \left(\frac{\Delta R_C}{R_C}\right) \tag{8.100}$$

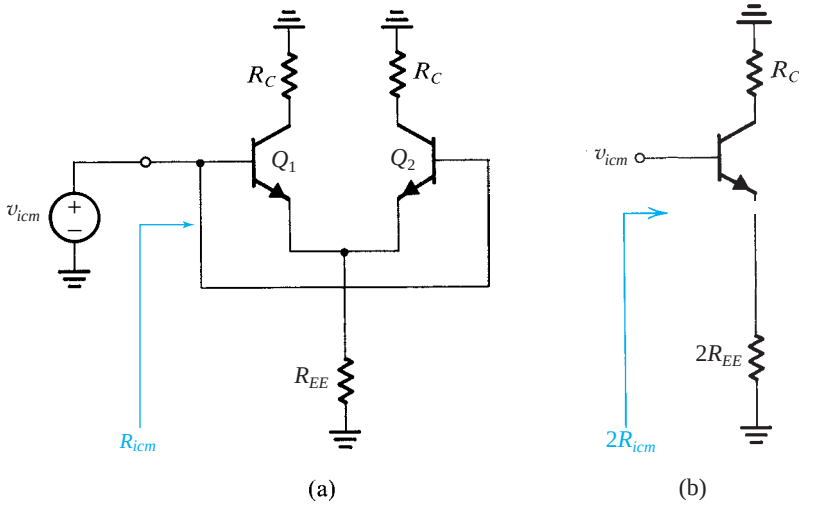


Figure 8.26 **(a)** Definition of the input common-mode resistance R_{icm}. **(b)** The equivalent common-mode half-circuit.

which is similar in form to the expression for the MOS pair [Eq. (8.50)]. Thus, to obtain a high CMRR, we design the current source to have a large output resistance R_{EE} and strive for close matching of the collector resistances.

Common-Mode Input Resistance The definition of the common-mode input resistance R_{icm} is illustrated in Fig. 8.26(a). Figure 8.26(b) shows the equivalent common-mode half-circuit; its input resistance is $2R_{icm}$. The value of $2R_{icm}$ can be determined by analyzing the circuit of Fig. 8.26(b) while taking r_o into account (because R_{EE} and R_C can be equal to, *or* larger than, r_o). The analysis is straightforward but tedious and can be shown [Problem 8.79] to yield the following result

$$R_{icm} \simeq \beta R_{EE} \frac{1 + R_C/\beta r_o}{1 + \dfrac{R_C + 2R_{EE}}{r_o}} \tag{8.101}$$

Example 8.4

The differential amplifier in Fig. 8.27 uses transistors with $\beta = 100$. Evaluate the following:

(a) The input differential resistance R_{id}.
(b) The overall differential voltage gain v_{od}/v_{sig} (neglect the effect of r_o).
(c) The worst-case common-mode gain if the two collector resistances are accurate to within ±1%.
(d) The CMRR, in dB.
(e) The input common-mode resistance (assuming that the Early voltage $V_A = 100$ V).

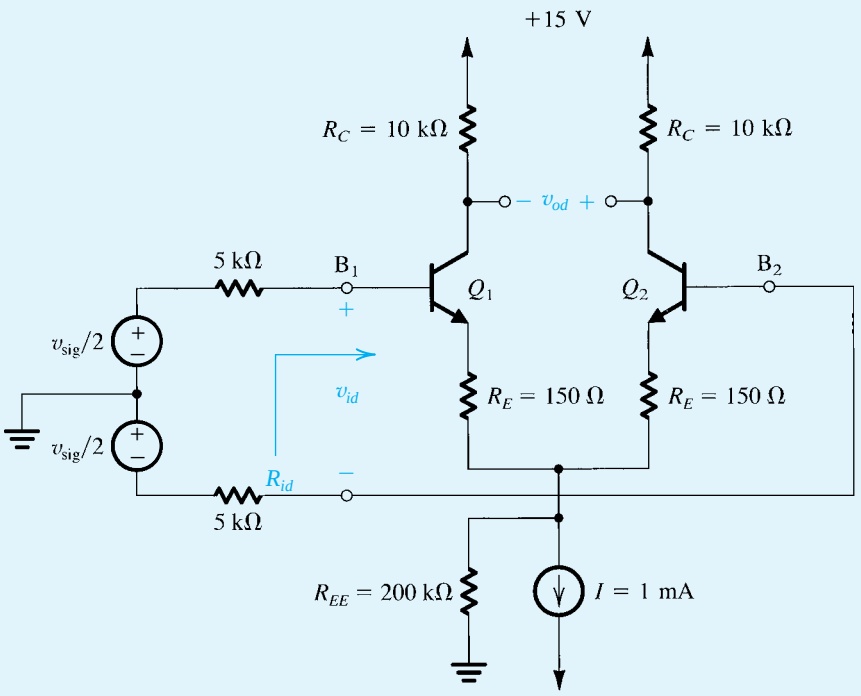


Figure 8.27 Circuit for Example 8.4.

Solution

(a) Each transistor is biased at an emitter current of 0.5 mA. Thus

$$r_{e1} = r_{e2} = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{0.5 \text{ mA}} = 50 \ \Omega$$

The input differential resistance can now be found as

$$R_{id} = 2(\beta+1)(r_e + R_E)$$

$$= 2 \times 101 \times (50 + 150) \simeq 40 \text{ k}\Omega$$

(b) The voltage gain from the signal source to the bases of Q_1 and Q_2 is

$$\frac{v_{id}}{v_{\text{sig}}} = \frac{R_{id}}{R_{\text{sig}} + R_{id}}$$

$$= \frac{40}{5 + 5 + 40} = 0.8 \text{ V/V}$$

The voltage gain from the bases to the output is

$$\frac{v_{od}}{v_{id}} \simeq \frac{\text{Total resistance in the collectors}}{\text{Total resistance in the emitters}}$$

Example 8.4 *continued*

$$= \frac{2R_C}{2(r_e + R_E)} = \frac{2 \times 10}{2(50 + 150) \times 10^{-3}} = 50 \text{ V/V}$$

The overall differential voltage gain can now be found as

$$A_d = \frac{v_{od}}{v_{\text{sig}}} = \frac{v_{id}}{v_{\text{sig}}} \frac{v_{od}}{v_{id}} = 0.8 \times 50 = 40 \text{ V/V}$$

(c) Using Eq. (8.99),

$$|A_{cm}| = \frac{R_C}{2R_{EE}} \frac{\Delta R_C}{R_C}$$

where $\Delta R_C = 0.02R_C$ in the worst case. Thus,

$$|A_{cm}| = \frac{10}{2 \times 200} \times 0.02 = 5 \times 10^{-4} \text{ V/V}$$

(d) $$\text{CMRR} = 20 \log \frac{|A_d|}{|A_{cm}|}$$

$$= 20 \log \frac{40}{5 \times 10^{-4}} = 98 \text{ dB}$$

$$r_o = \frac{V_A}{I/2} = \frac{100}{0.5} = 200 \text{ k}\Omega$$

(e) Using Eq. (8.101),

$$R_{icm} = 6.6 \text{ M}\Omega$$

EXERCISES

8.12 For the circuit in Fig. 8.19, let $I = 1$ mA, $V_{CC} = 15$ V, $R_C = 10$ kΩ, with $\alpha = 1$, and let the input voltages be: $v_{B1} = 5 + 0.005 \sin 2\pi \times 1000t$, volts, and $v_{B2} = 5 - 0.005 \sin 2\pi \times 1000t$, volts. (a) If the BJTs are specified to have v_{BE} of 0.7 V at a collector current of 1 mA, find the voltage at the emitters. (b) Find g_m for each of the two transistors. (c) Find i_C for each of the two transistors. (d) Find v_C for each of the two transistors. (e) Find the voltage between the two collectors. (f) Find the gain experienced by the 1000-Hz signal.

Ans. (a) 4.317 V; (b) 20 mA/V; (c) $i_{C1} = 0.5 + 0.1 \sin 2\pi \times 1000t$, mA and $i_{C2} = 0.5 - 0.1 \sin 2\pi \times 1000t$, mA; (d) $v_{C1} = 10 - 1 \sin 2\pi \times 1000t$, V and $v_{C2} = 10 + 1 \sin 2\pi \times 1000t$, V; (e) $v_{C2} - v_{C1} = 2 \sin 2\pi \times 1000t$, V; (f) 200 V/V

8.13 A bipolar differential amplifier utilizes a simple (i.e., a single CE transistor) current source to supply a bias current I of 200 μA, and simple current-source loads formed by *pnp* transistors. For all transistors, $\beta = 100$ and $|V_A| = 10$ V. Find g_m, R_C, $|A_d|$, R_{id}, R_{EE}, CMRR (if the two load transistors exhibit a 1% mismatch in their r_o's), and R_{icm}.

Ans. 4 mA/V; 100 kΩ ; 400 V/V; 50 kΩ, 50 kΩ; 86 dB; 1.67 MΩ

8.4 Other Nonideal Characteristics of the Differential Amplifier

8.4.1 Input Offset Voltage of the MOS Differential Pair

Consider the basic MOS differential amplifier with both inputs grounded, as shown in Fig. 8.28(a). If the two sides of the differential pair were perfectly matched (i.e., Q_1 and Q_2 identical and $R_{D1} = R_{D2} = R_D$), then current I would split equally between Q_1 and Q_2, and V_O would be zero. But practical circuits exhibit mismatches that result in a dc output voltage V_O even with both inputs grounded. We call V_O the **output dc offset voltage**. More commonly, we divide V_O by the differential gain of the amplifier, A_d, to obtain a quantity known as the **input offset voltage**, V_{OS},

$$V_{OS} = V_O/A_d \tag{8.102}$$

We can see that if we apply a voltage $-V_{OS}$ between the input terminals of the differential amplifier, then the output voltage will be reduced to zero (see Fig. 8.28b). This observation gives rise to the usual definition of the input offset voltage. It should be noted, however, that since the offset voltage is a result of device mismatches, its polarity is not known a priori.

Three factors contribute to the dc offset voltage of the MOS differential pair: mismatch in load resistances, mismatch in W/L, and mismatch in V_t. We shall consider the three contributing factors one at a time.

For the differential pair shown in Fig. 8.28(a) consider first the case where Q_1 and Q_2 are perfectly matched but R_{D1} and R_{D2} show a mismatch ΔR_D; that is,

$$R_{D1} = R_D + \frac{\Delta R_D}{2} \tag{8.103}$$

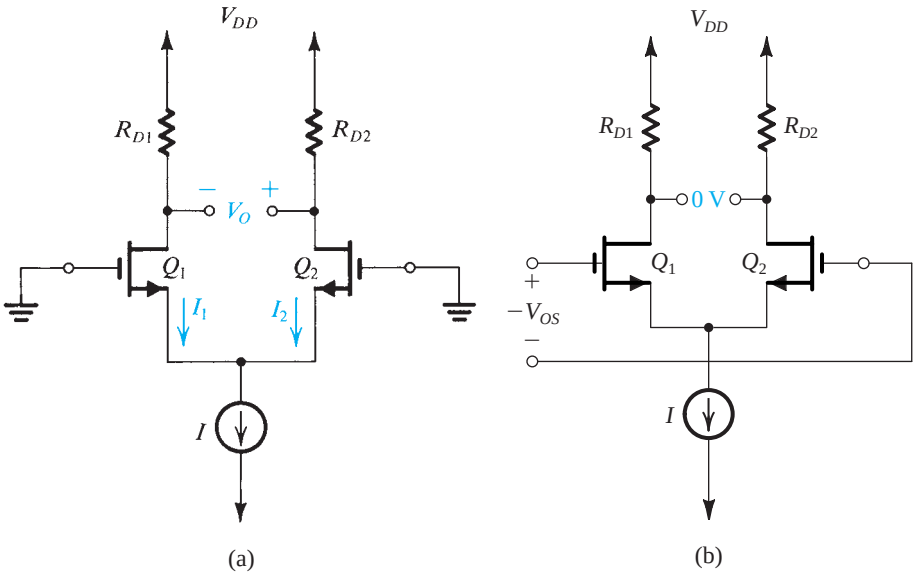


Figure 8.28 **(a)** The MOS differential pair with both inputs grounded. Owing to device and resistor mismatches, a finite dc output voltage V_O results. **(b)** Application of a voltage equal to the input offset voltage V_{OS} to the input terminals with opposite polarity reduces V_O to zero.

$$R_{D2} = R_D - \frac{\Delta R_D}{2} \tag{8.104}$$

Because Q_1 and Q_2 are matched, the current I will split equally between them. Nevertheless, because of the mismatch in load resistances, the output voltages V_{D1} and V_{D2} will be

$$V_{D1} = V_{DD} - \frac{I}{2}\left(R_D + \frac{\Delta R_D}{2}\right)$$

$$V_{D2} = V_{DD} - \frac{I}{2}\left(R_D - \frac{\Delta R_D}{2}\right)$$

Thus the differential output voltage V_O will be

$$\begin{aligned} V_O &= V_{D2} - V_{D1} \\ &= \left(\frac{I}{2}\right)\Delta R_D \end{aligned} \tag{8.105}$$

The corresponding input offset voltage is obtained by dividing V_O by the gain $g_m R_D$ and substituting for g_m from Eq. (8.30). The result is

$$V_{OS} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta R_D}{R_D}\right) \tag{8.106}$$

Thus the offset voltage is directly proportional to V_{OV} and, of course, to $\Delta R_D/R_D$. As an example, consider a differential pair in which the two transistors are operating at an overdrive voltage of 0.2 V and each drain resistance is accurate to within ±1%. It follows that the worst-case resistor mismatch will be

$$\frac{\Delta R_D}{R_D} = 0.02$$

and the resulting input offset voltage will be

$$|V_{OS}| = 0.1 \times 0.02 = 2 \text{ mV}$$

Next, consider the effect of a mismatch in the W/L ratios of Q_1 and Q_2, expressed as

$$\left(\frac{W}{L}\right)_1 = \frac{W}{L} + \frac{1}{2}\Delta\left(\frac{W}{L}\right) \tag{8.107}$$

$$\left(\frac{W}{L}\right)_2 = \frac{W}{L} - \frac{1}{2}\Delta\left(\frac{W}{L}\right) \tag{8.108}$$

Such a mismatch causes the current I to no longer divide equally between Q_1 and Q_2. Rather, because $V_{GS1} = V_{GS2}$, the current conducted by each of Q_1 and Q_2 will be proportional to its W/L ratio, and we can easily show that

$$I_1 = \frac{I}{2}\left[1 + \frac{\Delta(W/L)}{2(W/L)}\right] \tag{8.109}$$

$$I_2 = \frac{I}{2}\left[1 - \frac{\Delta(W/L)}{2(W/L)}\right] \tag{8.110}$$

Dividing the current difference,

$$\frac{I}{2}\frac{\Delta(W/L)}{(W/L)}$$

by g_m gives the input offset voltage (due to the mismatch in W/L values).[2] Thus

$$V_{OS} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta(W/L)}{(W/L)}\right) \tag{8.111}$$

Here again we note that V_{OS}, resulting from a (W/L) mismatch, is proportional to V_{OV} and, as expected, $\Delta(W/L)$.

Finally, we consider the effect of a mismatch ΔV_t between the two threshold voltages,

$$V_{t1} = V_t + \frac{\Delta V_t}{2} \tag{8.112}$$

$$V_{t2} = V_t - \frac{\Delta V_t}{2} \tag{8.113}$$

The current I_1 will be given by

$$I_1 = \frac{1}{2}k_n'\frac{W}{L}\left(V_{GS} - V_t - \frac{\Delta V_t}{2}\right)^2$$

$$= \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2\left[1 - \frac{\Delta V_t}{2(V_{GS} - V_t)}\right]^2$$

which, for $\Delta V_t \ll 2(V_{GS} - V_t)$ [that is, $\Delta V_t \ll 2V_{OV}$], can be approximated as

$$I_1 \simeq \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2\left(1 - \frac{\Delta V_t}{V_{GS} - V_t}\right)$$

Similarly,

$$I_2 \simeq \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2\left(1 + \frac{\Delta V_t}{V_{GS} - V_t}\right)$$

We recognize that

$$\frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 = \frac{I}{2}$$

and the current increment (decrement) in Q_2 (Q_1) is

$$\Delta I = \frac{I}{2}\frac{\Delta V_t}{V_{GS} - V_t} = \frac{I}{2}\frac{\Delta V_t}{V_{OV}}$$

Dividing the current difference $2\Delta I$ by g_m gives the input offset voltage (due to ΔV_t). Thus,

$$V_{OS} = \Delta V_t \tag{8.114}$$

a very logical result! For modern MOS technology ΔV_t can be as high as a few mV. Finally, we note that since the three sources for offset voltage are not correlated, an estimate of the total input offset voltage can be found as

$$V_{OS} = \sqrt{\left(\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{OV}}{2}\frac{\Delta(W/L)}{W/L}\right)^2 + (\Delta V_t)^2} \tag{8.115}$$

[2]We are skipping a step in the derivation: Rather than multiplying the current difference by R_C and dividing the resulting output offset by $A_d = g_m R_C$, we are simply dividing the current difference by g_m.

EXERCISE

8.14 For the MOS differential pair specified in Exercise 8.4, find the three components of the input offset voltage. Let $\Delta R_D/R_D = 2\%$, $\Delta(W/L)/(W/L) = 2\%$, and $\Delta V_t = 2$ mV. Use Eq. (8.115) to obtain an estimate of the total V_{OS}.
Ans. 2 mV; 2 mV; 2 mV; 3.5 mV

8.4.2 Input Offset Voltage of the Bipolar Differential Amplifier

The offset voltage of the bipolar differential pair shown in Fig. 8.29(a) can be determined in a manner analogous to that used above for the MOS pair. Note, however, that in the bipolar case there is no analog to the V_t mismatch of the MOSFET pair. Here the output offset results from mismatches in the load resistances R_{C1} and R_{C2} and from junction area, β, and other mismatches in Q_1 and Q_2. Consider first the effect of the load mismatch. Let

$$R_{C1} = R_C + \frac{\Delta R_C}{2} \tag{8.116}$$

$$R_{C2} = R_C - \frac{\Delta R_C}{2} \tag{8.117}$$

and assume that Q_1 and Q_2 are perfectly matched. It follows that current I will divide equally between Q_1 and Q_2, and thus

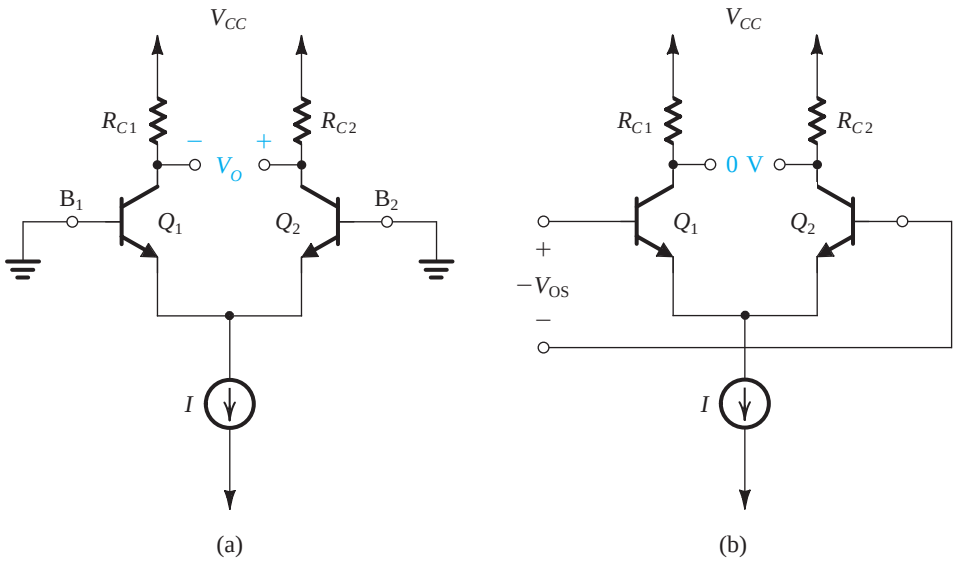


Figure 8.29 **(a)** The BJT differential pair with both inputs grounded. Device mismatches result in a finite dc output V_O. **(b)** Application of the input offset voltage $V_{OS} \equiv V_O/A_d$ to the input terminals with opposite polarity reduces V_O to zero.

$$V_{C1} = V_{CC} - \left(\frac{\alpha I}{2}\right)\left(R_C + \frac{\Delta R_C}{2}\right)$$

$$V_{C2} = V_{CC} - \left(\frac{\alpha I}{2}\right)\left(R_C - \frac{\Delta R_C}{2}\right)$$

Thus the output voltage will be

$$V_O = V_{C2} - V_{C1} = \alpha\left(\frac{I}{2}\right)(\Delta R_C)$$

and the input offset voltage will be

$$V_{OS} = \frac{\alpha(I/2)(\Delta R_C)}{A_d} \tag{8.118}$$

Substituting $A_d = g_m R_C$ and

$$g_m = \frac{\alpha I/2}{V_T}$$

gives

$$|V_{OS}| = V_T\left(\frac{\Delta R_C}{R_C}\right) \tag{8.119}$$

An important point to note is that in comparison to the corresponding expression for the MOS pair (Eq. 8.106) here the offset is proportional to V_T rather than $V_{OV}/2$. V_T at 25 mV is 3 to 6 times lower than $V_{OV}/2$. Hence bipolar differential pairs exhibit lower offsets than their MOS counterparts. As an example, consider the situation of collector resistors that are accurate to within ±1%. Then the worst case mismatch will be

$$\frac{\Delta R_C}{R_C} = 0.02$$

and the resulting input offset voltage will be

$$|V_{OS}| = 25 \times 0.02 = 0.5 \text{ mV}$$

Next consider the effect of mismatches in transistors Q_1 and Q_2. In particular, let the transistors have a mismatch in their emitter–base junction areas. Such an area mismatch gives rise to a proportional mismatch in the scale currents I_S,

$$I_{S1} = I_S + \frac{\Delta I_S}{2} \tag{8.120}$$

$$I_{S2} = I_S - \frac{\Delta I_S}{2} \tag{8.121}$$

Refer to Fig. 8.29(a) and note that $V_{BE1} = V_{BE2}$. Thus, the current I will split between Q_1 and Q_2 in proportion to their I_S values, resulting in

$$I_{E1} = \frac{I}{2}\left(1 + \frac{\Delta I_S}{2I_S}\right) \tag{8.122}$$

$$I_{E2} = \frac{I}{2}\left(1 - \frac{\Delta I_S}{2I_S}\right) \tag{8.123}$$

It follows that the output offset voltage will be

$$V_O = \alpha\left(\frac{I}{2}\right)\left(\frac{\Delta I_S}{I_S}\right)R_C$$

and the corresponding input offset voltage will be

$$|V_{OS}| = V_T\left(\frac{\Delta I_S}{I_S}\right) \tag{8.124}$$

As an example, an area mismatch of 4% gives rise to $\Delta I_S/I_S = 0.04$ and an input offset voltage of 1 mV. Here again we note that the offset voltage is proportional to V_T rather than to the much larger V_{OV}, which determines the offset of the MOS pair due to $\Delta(W/L)$ mismatch.

Since the two contributions to the input offset voltage are usually not correlated, an estimate of the total input offset voltage can be found as

$$\begin{aligned} V_{OS} &= \sqrt{\left(V_T\frac{\Delta R_C}{R_C}\right)^2 + \left(V_T\frac{\Delta I_S}{I_S}\right)^2} \\ &= V_T\sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2} \end{aligned} \tag{8.125}$$

There are other possible sources for input offset voltage such as mismatches in the values of β and r_o. Some of these are investigated in the end-of-chapter problems. Finally, it should be noted that there is a popular scheme for compensating for the offset voltage. It involves introducing a deliberate mismatch in the values of the two collector resistances such that the differential output voltage is reduced to zero when both input terminals are grounded. Such an **offset-nulling** scheme is explored in Problem 8.81.

8.4.3 Input Bias and Offset Currents of the Bipolar Differential Amplifier

In a perfectly symmetric differential pair the two input terminals carry equal dc currents; that is,

$$I_{B1} = I_{B2} = \frac{I/2}{\beta+1} \tag{8.126}$$

This is the **input bias current** of the differential amplifier.

Mismatches in the amplifier circuit and most importantly a mismatch in β make the two input dc currents unequal. The resulting difference is the **input offset current**, I_{OS}, given as

$$I_{OS} = |I_{B1} - I_{B2}| \tag{8.127}$$

Let

$$\beta_1 = \beta + \frac{\Delta\beta}{2}$$

$$\beta_2 = \beta - \frac{\Delta\beta}{2}$$

then

$$I_{B1} = \frac{I}{2}\frac{1}{\beta+1+\Delta\beta/2} \simeq \frac{I}{2}\frac{1}{\beta+1}\left(1-\frac{\Delta\beta}{2\beta}\right) \tag{8.128}$$

$$I_{B2} = \frac{I}{2}\frac{1}{\beta+1-\Delta\beta/2} \simeq \frac{I}{2}\frac{1}{\beta+1}\left(1+\frac{\Delta\beta}{2\beta}\right) \tag{8.129}$$

$$I_{OS} = \frac{I}{2(\beta+1)}\left(\frac{\Delta\beta}{\beta}\right) \tag{8.130}$$

Formally, the input bias current I_B is defined as follows:

$$I_B \equiv \frac{I_{B1}+I_{B2}}{2} = \frac{I}{2(\beta+1)} \tag{8.131}$$

Thus

$$I_{OS} = I_B\left(\frac{\Delta\beta}{\beta}\right) \tag{8.132}$$

As an example, a 10% β mismatch results in an offset current that is one-tenth the value of the input bias current.

Finally note that a great advantage of the MOS differential pair is that it does not suffer from a finite input bias current or from mismatches thereof!

8.4.4 A Concluding Remark

We conclude this section by noting that the definitions presented here are identical to those presented in Chapter 2 for op amps. In fact, as will be seen in Chapter 12, it is the input differential stage in an op-amp circuit that primarily determines the op-amp dc offset voltage, input bias and offset currents, and input common-mode range.

EXERCISE

8.15 For a BJT differential amplifier utilizing transistors having $\beta = 100$, matched to 10% or better, and areas that are matched to 10% or better, along with collector resistors that are matched to 2% or better, find V_{OS}, I_B, and I_{OS}. The dc bias current I is 100 μA.
Ans. 2.55 mV; 0.5 μA; 50 nA

8.5 The Differential Amplifier with Active Load

The differential amplifiers we have studied thus far have been of the differential output variety; that is, the output is taken between the two drains (or two collectors) rather than between one of the drains (collectors) and ground. Taking the output differentially has two major advantages:

1. It decreases the common-mode gain and increases the common-mode rejection ratio (CMRR) dramatically. Recall that while the drain (collector) voltages change somewhat in response to a common-mode input signal, the difference between the drain (collector) voltages remains essentially zero except for a small change due to the mismatches inevitably present in the circuit.
2. It increases the differential gain by a factor of 2 (6 dB) because the output is the difference between two voltages of equal magnitude and opposite sign.

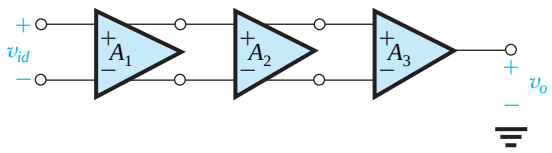


Figure 8.30 A three-stage amplifier consisting of two differential-in, differential-out stages, A_1 and A_2, and a differential-in, single-ended-out stage A_3.

These advantages are sufficiently compelling that at least the first stage in an IC amplifier such as an op amp is **differential-in**, **differential-out**. The differential transmission of the signal on the chip also minimizes its susceptibility to corruption with noise and interference, which usually occur in a common-mode fashion. Nevertheless, it is usually required at some point to convert the signal from differential to single-ended; for instance, to connect it to an off-chip load. Figure 8.30 shows a block diagram of a three-stage amplifier in which the first two stages are of the differential-in, differential out type, and the third has a single-ended output, that is, an output that is referenced to ground. We now address the question of conversion from differential to single-ended.

8.5.1 Differential to Single-Ended Conversion

Figure 8.31 illustrates the simplest, most basic approach for differential-to-single-ended conversion. It consists of simply ignoring the drain current signal of Q_1 and eliminating its drain resistor altogether, and taking the output between the drain of Q_2 and ground. The obvious drawback of this scheme is that we lose a factor of 2 (or 6 dB) in gain as a result of "wasting" the drain signal current of Q_1. A much better approach would be to find a way of utilizing the drain-current signal of Q_1, and that is exactly what the circuit we are about to discuss accomplishes.

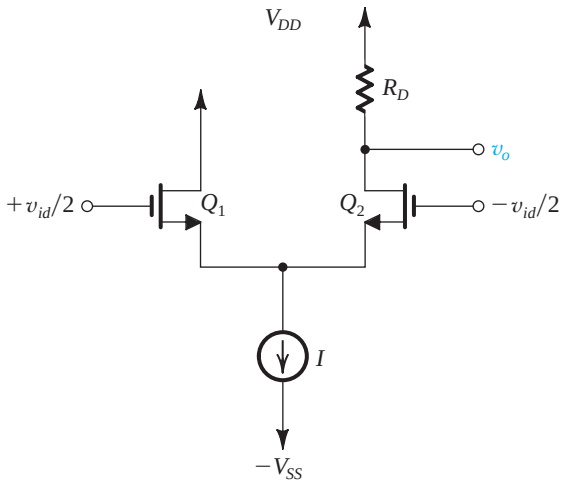


Figure 8.31 A simple but inefficient approach for differential to single-ended conversion.

8.5.2 The Active-Loaded MOS Differential Pair

Figure 8.32(a) shows a MOS differential pair formed by transistors Q_1 and Q_2, loaded by a current mirror formed by transistors Q_3 and Q_4. To see how this circuit operates consider first the quiescent or equilibrium state with the two input terminals connected to a dc voltage equal to the common-mode equilibrium value, in this case 0 V, as shown in Fig. 8.32(b). Assuming perfect matching, the bias current I divides equally between Q_1 and Q_2. The drain current of Q_1, $I/2$, is fed to the input transistor of the mirror, Q_3. Thus, a replica of this current is provided by the output transistor of the mirror, Q_4. Observe that at the output node the two currents $I/2$ balance each other out, leaving a zero current to flow out to the next stage or to a load (not shown). If Q_4 is perfectly matched to Q_3, its drain voltage will track the voltage at the drain of Q_3; thus in equilibrium the voltage at the output will be $V_{DD} - V_{SG3}$. It

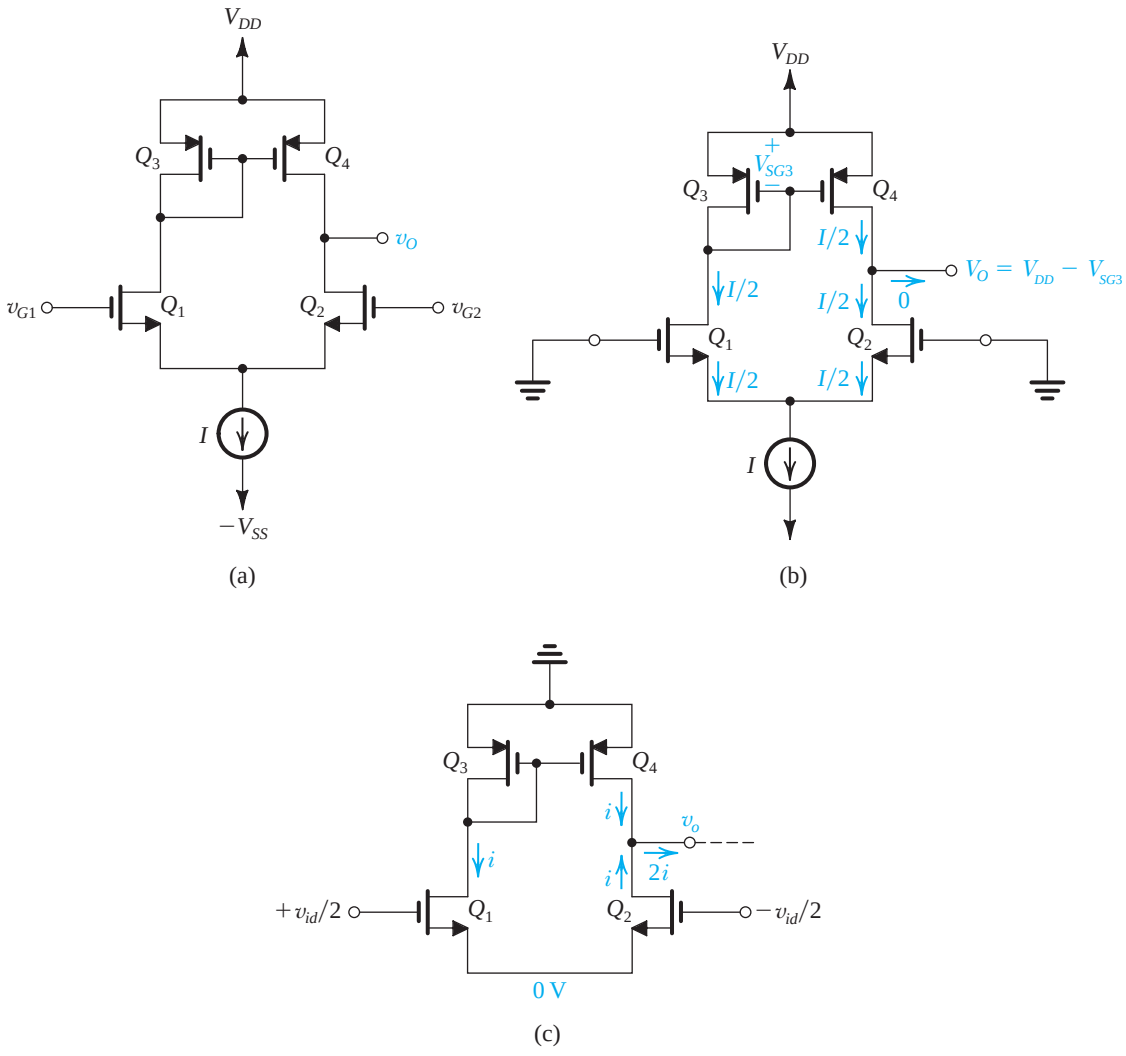


Figure 8.32 **(a)** The active-loaded MOS differential pair. **(b)** The circuit at equilibrium assuming perfect matching. **(c)** The circuit with a differential input signal applied and neglecting the r_o of all transistors.

should be noted, however, that in practical implementations, there will always be mismatches, resulting in a net dc current at the output. In the absence of a load resistance, this current will flow into the output resistances of Q_2 and Q_4 and thus can cause a large deviation in the output voltage from the ideal value. Therefore, this circuit is always designed so that the dc bias voltage at the output node is defined by a feedback circuit rather than by simply relying on the matching of Q_4 and Q_3. We shall see how this is done later.

Next, consider the circuit with a differential input signal v_{id} applied to the input, as shown in Fig. 8.32(c). Since we are now investigating the small-signal operation of the circuit, we have removed the dc supplies (including the current source I). Also, for the time being let us ignore r_o of all transistors. As Fig. 8.32(c) shows, a virtual ground will develop at the common-source terminal of Q_1 and Q_2. Transistor Q_1 will conduct a drain signal current $i = g_{m1}v_{id}/2$, and transistor Q_2 will conduct an equal but opposite current i. The drain signal current i of Q_1 is fed to the input of the $Q_3 - Q_4$ mirror, which responds by providing a replica in the drain of Q_4. Now, at the output node we have two currents, each equal to i, which sum together to provide an output current $2i$. It is this factor of 2, which is a result of the current-mirror action, that makes it possible to convert the signal to single-ended form (i.e., between the output node and ground) with no loss of gain! If a load resistance is connected to the output node, the current $2i$ flows through it and thus determines the output voltage v_o. In the absence of a load resistance, the output voltage is determined by the output current $2i$ and the output resistance of the circuit, as we shall shortly see.

8.5.3 Differential Gain of the Active-Loaded MOS Pair

As we learned in Chapter 7, the output resistance r_o of the transistor plays a significant role in the operation of active-loaded amplifiers. Therefore, we shall now take r_o into account and derive an expression for the differential gain v_o/v_{id} of the active-loaded MOS differential pair. Unfortunately, because the circuit is *not* symmetrical a virtual ground will *not* develop at the common source terminal, contrary to the qualitative description presented above (where the r_o's were neglected). Thus we will not be able to use the differential half-circuit technique. Rather, we shall perform the derivation from first principles: We will represent the output of the circuit by the equivalent circuit shown in Fig. 8.33 and find the short-circuit transconductance G_m and the output resistance R_o. Then, the gain will be determined as $G_m R_o$.

Determining the Transconductance G_m Figure 8.34(a) shows the circuit[3] prepared for determining G_m. Note that we have short-circuited the output to ground in order to find G_m as

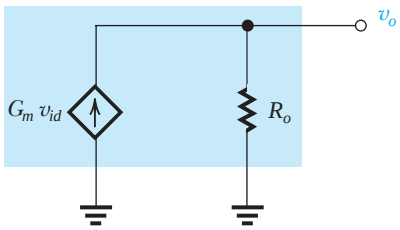


Figure 8.33 Output equivalent circuit of the amplifier in Fig. 8.32(a) for differential input signals.

[3]Note that rather than replacing each transistor with its small-signal model, we are, for simplicity, using the models implicitly. Thus we have "pulled r_o out" of each transistor and shown it separately so that the drain current becomes $g_m v_{gs}$.

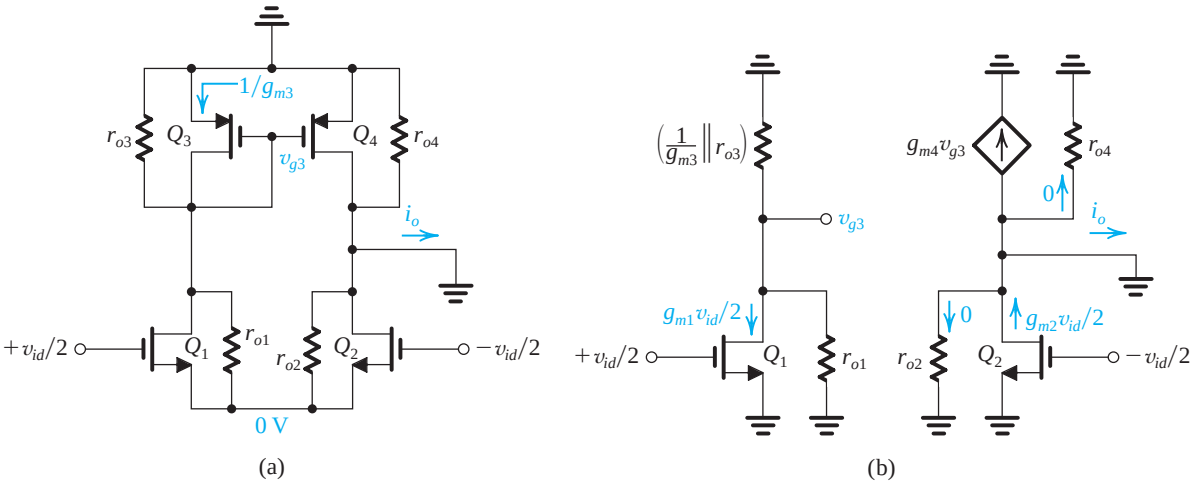


Figure 8.34 Determining the short-circuit transconductance $G_m \equiv i_o/v_{id}$ of the active-loaded MOS differential pair.

i_o/v_{id}. Although the original circuit is not symmetrical, when the output is shorted to ground, the circuit becomes almost symmetrical. This is because the voltage between the drain of Q_1 and ground is very small. This in turn is due to the low resistance between that node and ground which is almost equal to $1/g_{m3}$. Thus, we can now invoke symmetry and assume that a virtual ground will appear at the source of Q_1 and Q_2 and in this way obtain the equivalent circuit shown in Fig. 8.34(b). Here we have replaced the diode-connected transistor Q_3 by its equivalent resistance $[(1/g_{m3})\|r_{o3}]$. The voltage v_{g3} that develops at the common-gate node of the mirror can be found by multiplying the drain current of Q_1 $(g_{m1}v_{id}/2)$, by the total resistance between the drain of Q_1 and ground.

$$v_{g3} = -g_{m1}\left(\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}} \| r_{o3} \| r_{o1}\right) \tag{8.133}$$

which for the usual case of r_{o1} and $r_{o3} \gg (1/g_{m3})$ reduces to

$$v_{g3} \simeq -\left(\frac{g_{m1}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) \tag{8.134}$$

This voltage controls the drain current of Q_4 resulting in a current of $g_{m4}v_{g3}$. Note that the ground at the output node causes the currents in r_{o2} and r_{o4} to be zero. Thus the output current i_o will be

$$i_o = -g_{m4}v_{g3} + g_{m2}\left(\frac{v_{id}}{2}\right) \tag{8.135}$$

Substituting for v_{g3} from Eq. (8.134) gives

$$i_o = g_{m1}\left(\frac{g_{m4}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) + g_{m2}\left(\frac{v_{id}}{2}\right)$$

Now, since $g_{m3} = g_{m4}$ and $g_{m1} = g_{m2} = g_m$, the current i_o becomes

$$i_o = g_m v_{id}$$

from which G_m is found to be

$$G_m = g_m \tag{8.136}$$

Thus the short-circuit transconductance of the circuit is equal to g_m of each of the two transistors of the differential pair.[4] Here we should note that in the absence of the current-mirror action, G_m would be equal to $g_m/2$.

Determining the Output Resistance R_o Figure 8.35 shows the circuit for determining the output resistance R_o. Observe that we have set v_{id} to zero, resulting in the ground connections at the gates of Q_1 and Q_2. We have applied a test voltage v_x in order to determine R_o,

$$R_o \equiv \frac{v_x}{i_x}$$

Analysis of this circuit is considerably simplified by observing the current transmission around the circuit by simply following the circled numbers. The current i that enters Q_2 must exist at its source. It then enters Q_1, exiting at the drain to feed the $Q_3 - Q_4$ mirror. Since for the diode-connected transistor Q_3, $1/g_{m3}$ is much smaller than r_{o3}. most of the current i flows into the drain proper of Q_3. The mirror responds by providing an equal current i in the drain of Q_4. The relationship between i and v_x can be determined by observing that at the output node

$$i = v_x/R_{o2}$$

where R_{o2} is the output resistance of Q_2. Now, Q_2 is a CG transistor and has in its source lead the input resistance R_{in1} of the CG transistor Q_1. Noting that the load resistance of Q_1

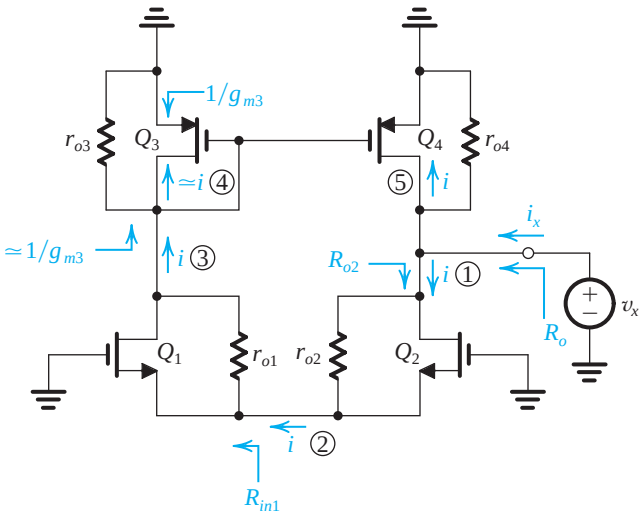


Figure 8.35 Circuit for determining R_o. The circled numbers indicate the order of the analysis steps.

[4]Because the circuit of Fig. 8.34(a) is not perfectly symmetrical, the voltage at the common-source terminal will not be exactly zero. Nevertheless, it can be shown that the voltage will be very small and the transconductance G_m will indeed be very close to g_m.

is $[(1/g_{m3}) \| r_{o3}]$, which is approximately $1/g_{m3}$, we can obtain R_{in1} by using the expression for the input resistance of a CG transistor (adapt Eq. 7.35 by replacing the subscript 2 by 1),

$$R_{in1} = \frac{r_{o1} + R_L}{g_{m1} r_{o1}}$$
$$= \frac{1}{g_{m1}} + \frac{1/g_{m3}}{g_{m1} r_{o1}} \simeq \frac{1}{g_{m1}}$$

We then use this value of R_{in1} to determine R_{o2} using the expression in Eq. (7.38) as follows:

$$R_{o2} = R_{in1} + r_{o2} + g_{m2} r_{o2} R_{in1}$$
$$= \frac{1}{g_{m1}} + r_{o2} + \left(\frac{g_{m2}}{g_{m1}}\right) r_{o2}$$

which, for $g_{m1} = g_{m2} = g_m$ and $g_{m2} r_{o2} \gg 1$, yields

$$R_{o2} \simeq 2 r_{o2} \tag{8.137}$$

Returning to the output node, we write

$$i_x = i + i + \frac{v_x}{r_{o4}}$$
$$= 2i + \frac{v_x}{r_{o4}} = 2\frac{v_x}{R_{o2}} + \frac{v_x}{r_{o4}}$$

Substituting for R_{o2} from Eq. (8.137), we obtain

$$i_x = 2\frac{v_x}{2 r_{o2}} + \frac{v_x}{r_{o4}}$$

Thus,

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} \| r_{o4} \tag{8.138}$$

which is an intuitively appealing result.

Determining the Differential Gain Equations (8.136) and (8.138) can be combined to obtain the differential gain A_d as

$$A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_m (r_{o2} \| r_{o4}) \tag{8.139}$$

For the case $r_{o2} = r_{o4} = r_o$,

$$A_d = \frac{1}{2} g_m r_o = \frac{A_0}{2} \tag{8.140}$$

where A_0 is the intrinsic gain of the MOS transistor.

8.5.4 Common-Mode Gain and CMRR

Although its output is single-ended, the active-loaded MOS differential amplifier has a low common-mode gain and, correspondingly, a high CMRR. Figure 8.36(a) shows the circuit with v_{icm} applied and with the power supplies eliminated except, of course, for the output resistance R_{SS} of the bias-current source I. Although the circuit is not symmetrical and hence

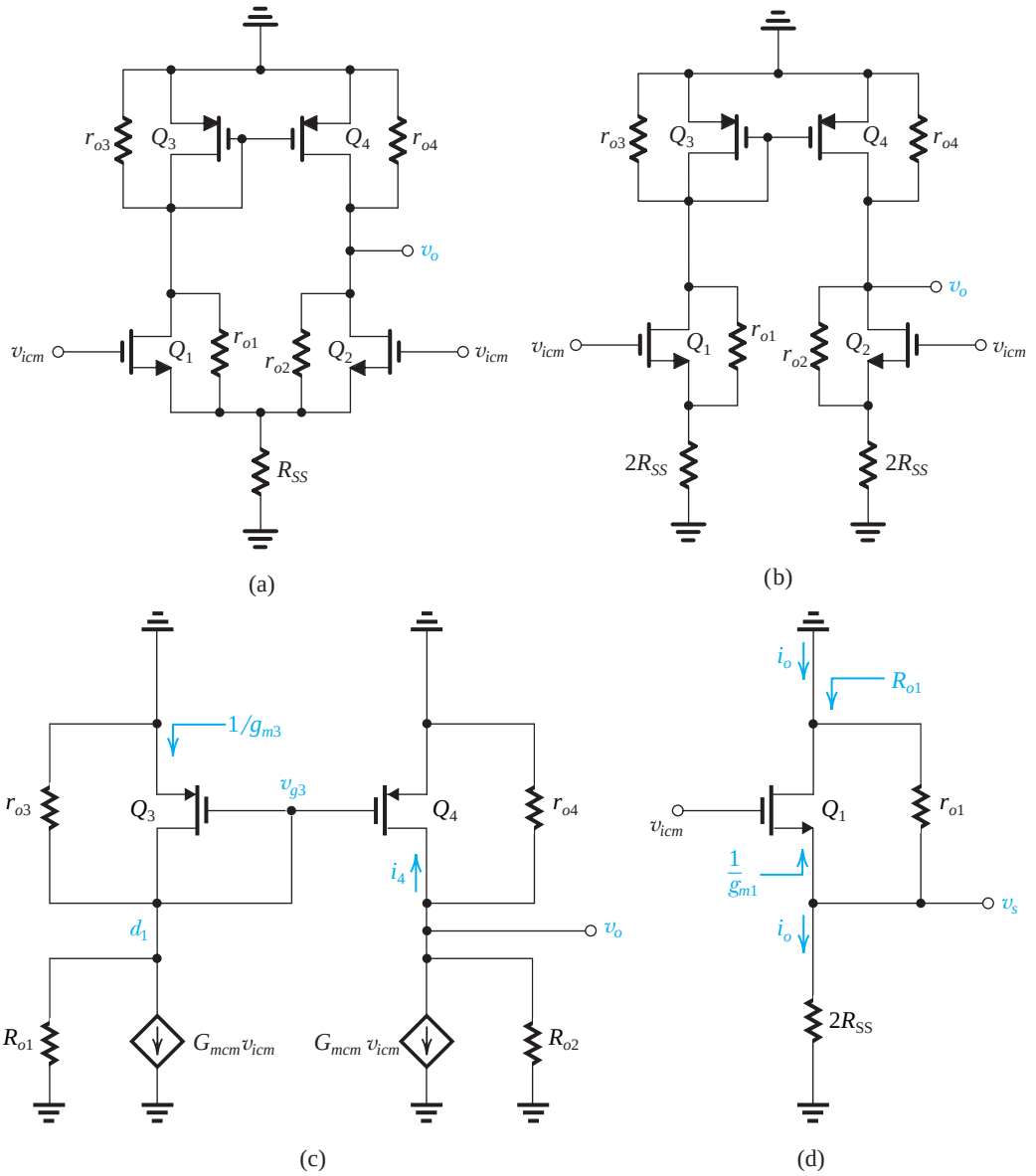


Figure 8.36 Analysis of the active-loaded MOS differential amplifier to determine its common-mode gain.

we cannot use the common-mode half-circuit, we can split R_{SS} equally between Q_1 and Q_2 as shown in Fig. 8.36b. It can now be seen that each of Q_1 and Q_2 is a CS transistor with a large source degeneration resistance $2R_{SS}$.

Each of Q_1 and Q_2 together with their degeneration resistances can be replaced by equivalent circuits composed of a controlled source $G_{mcm}v_{icm}$ and an output resistance $R_{o1,2}$, as shown in Fig. 8.36(c). To determine G_{mcm} we short circuit the drain to ground, as shown in Fig. 8.36(d) for Q_1. Observe that $2R_{SS}$ and r_{o1} appear in parallel. Thus the voltage at the source terminal can be found from the voltage divider consisting of $1/g_{m1}$ and $(2R_{SS} \parallel r_{o1})$ as

$$v_s = v_{icm}\frac{(2R_{SS} \parallel r_{o1})}{(2R_{SS} \parallel r_{o1}) + (1/g_{m1})}$$

$$\simeq v_{icm}$$

The short-circuit drain current i_o can be seen to be equal to the current through $2R_{SS}$; thus,

$$i_o = \frac{v_{icm}}{2R_{SS}}$$

which leads to

$$G_{mcm} \equiv \frac{i_o}{v_{icm}} = \frac{1}{2R_{SS}} \tag{8.141}$$

The output resistance R_{o1} can be determined using the expression for R_o of a CS transistor with an emitter-degeneration resistance (Eq. 7.38) to obtain

$$R_{o1} = 2R_{SS} + r_{o1} + (g_{m1}r_{o1})(2R_{SS}) \tag{8.142}$$

Similar results can be obtained for Q_2, namely, the same G_{mcm} and an output resistance R_{o2} given by

$$R_{o2} = 2R_{SS} + r_{o2} + (g_{m2}r_{o2})(2R_{SS}) \tag{8.143}$$

Returning to the circuit in Fig. 8.36(c), the voltage v_{g3} can be obtained by multiplying $G_{mcm}v_{icm}$ by the total resistance between the d_1 node and ground,

$$v_{g3} = -G_{mcm}v_{icm}\left(R_{o1} \parallel r_{o3} \parallel \frac{1}{g_{m3}}\right) \tag{8.144}$$

This voltage in turn determines the current i_4 as

$$i_4 = g_{m4}v_{gs3} = g_{m4}v_{g3}$$

Thus,

$$i_4 = -g_{m4}G_{mcm}v_{icm}\left(R_{o1} \parallel r_{o3} \parallel \frac{1}{g_{m3}}\right) \tag{8.145}$$

Finally, we can obtain the output voltage v_o by writing for the output node,

$$G_{mcm}v_{icm} + i_4 + \frac{v_o}{R_{o2}} + \frac{v_o}{r_{o4}} = 0$$

Substituting for i_4 from Eq. (8.145) and for G_{mcm} from Eq. (8.141) yields

$$v_o = -v_{icm}\frac{r_{o4} \parallel R_{o2}}{2R_{SS}}\left[1 - g_{m4}\left(R_{o1} \parallel r_{o3} \parallel \frac{1}{g_{m3}}\right)\right]$$

Since $R_{o2} \gg r_{o4}$ and $R_{o1} \gg r_{o3}$, we can neglect both. Also, substituting $g_{m4} = g_{m3}$, we obtain the following expression for A_{cm},

$$A_{cm} \equiv \frac{v_o}{v_{icm}} \simeq -\frac{r_{o4}}{2R_{SS}}\frac{1}{1 + g_{m3}r_{o3}} \tag{8.146}$$

This expression can be further simplified by noting that $g_{m3}r_{o3} \gg 1$ and $r_{o3} = r_{o4}$ with the result that

$$A_{cm} \simeq -\frac{1}{2g_{m3}R_{SS}} \tag{8.146'}$$

Since R_{SS} is usually large, at least equal to r_o, A_{cm} will be small. The common-mode rejection ratio (CMRR) can now be obtained by utilizing Eqs. (8.139) and (8.146′),

$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|} = [g_m(r_{o2} \| r_{o4})][2g_{m3}R_{SS}] \tag{8.147}$$

which for $r_{o2} = r_{o4} = r_o$ and $g_{m3} = g_m$ simplifies to

$$\text{CMRR} = (g_m r_o)(g_m R_{SS}) \tag{8.148}$$

We observe that to obtain a large CMRR, we select an implementation of the biasing current source I that features a high output resistance. Such circuits include the cascode current source and the Wilson current source studied in Section 7.5.

EXERCISE

8.16 An active-loaded MOS differential amplifier of the type shown in Fig. 8.32(a) is specified as follows: $(W/L)_n = 100$, $(W/L)_p = 200$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 0.2$ mA/V^2, $V_{An} = |V_{Ap}| = 20$ V, $I = 0.8$ mA, $R_{SS} = 25$ kΩ. Calculate G_m, R_o, A_d, $|A_{cm}|$, and CMRR.
Ans. 4 mA/V; 25 kΩ; 100 V/V; 0.005 V/V; 20,000 or 86 dB

8.5.5 The Bipolar Differential Pair with Active Load

The bipolar version of the active-loaded differential pair is shown in Fig. 8.37(a). The circuit structure and operation are very similar to those of its MOS counterpart except that here we have to contend with the effects of finite β and the resulting finite input resistance at the base, r_π. For the time being, however, we shall ignore the effect of finite β on the dc bias of the four transistors and assume that in equilibrium all transistors are operating at a dc current of $I/2$.

Differential Gain To obtain an expression for the differential gain, we apply an input differential signal v_{id} as shown in the equivalent circuit in Fig. 8.37(b). Note that the output is connected to ground in order to determine the overall short-circuit transconductance $G_m \equiv i_o/v_{id}$. Also, as in the MOS case, we have assumed that the circuit is sufficiently balanced so that a virtual ground develops on the common emitter terminal. This assumption is predicated on the fact that the voltage signal at the collector of Q_1 will be small as a result of the low resistance between that node and ground (approximately equal to r_{e3}). The voltage v_{b3} can be found from

$$v_{b3} = -g_{m1}\left(\frac{v_{id}}{2}\right)(r_{e3} \| r_{o3} \| r_{o1} \| r_{\pi 4})$$

Of the four resistances in the parallel equivalent on the right-hand side, r_{e3} is much smaller than the other three and thus dominates, with the result that

$$v_{b3} \simeq -g_{m1} r_{e3}\left(\frac{v_{id}}{2}\right) \tag{8.149}$$

Since $v_{b4} = v_{b3}$, the collector current of Q_4 will be

$$g_{m4} v_{b4} = -g_{m4} g_{m1} r_{e3}\left(\frac{v_{id}}{2}\right) \tag{8.150}$$

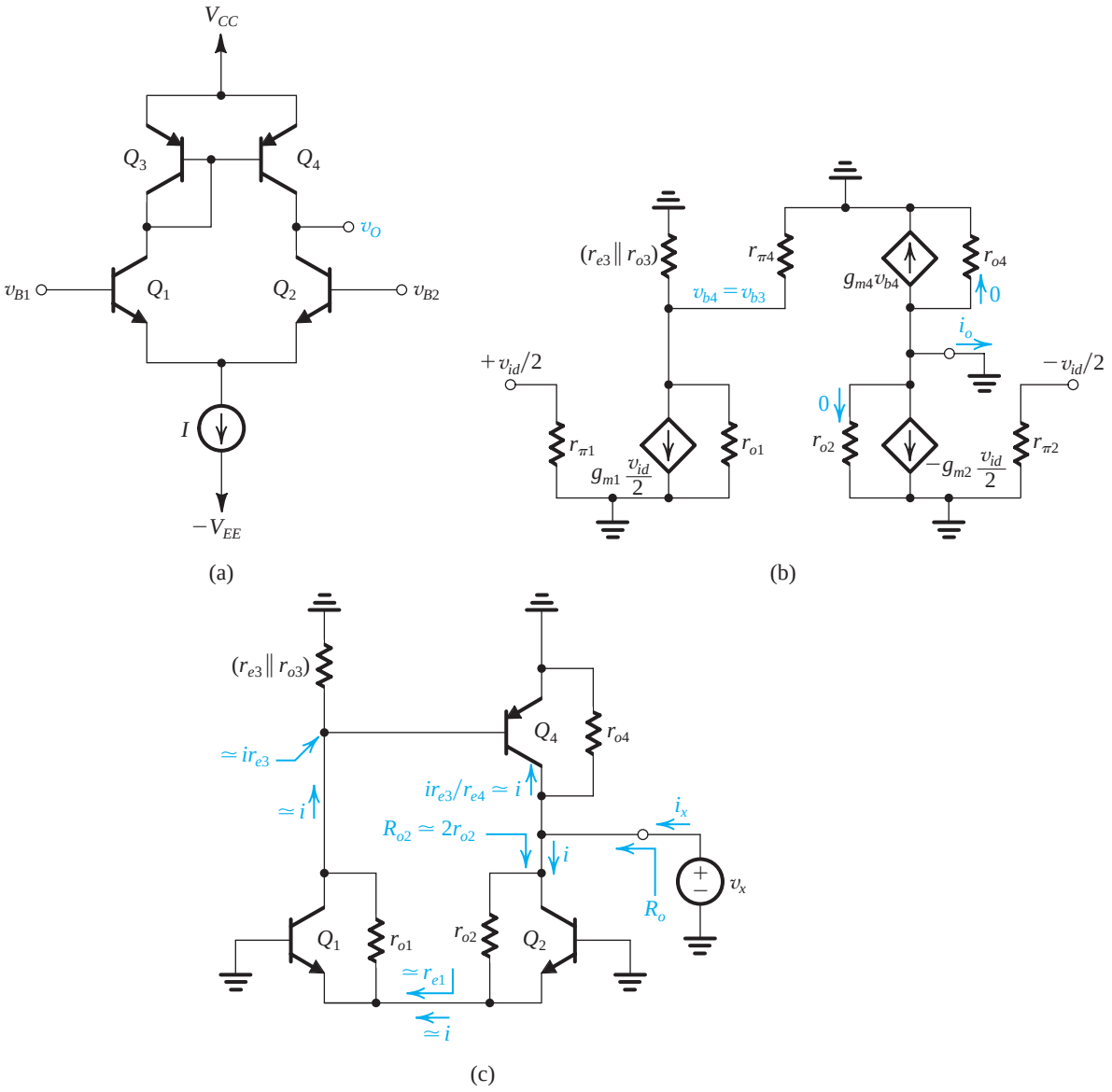


Figure 8.37 **(a)** Active-loaded bipolar differential pair. **(b)** Small-signal equivalent circuit for determining the transconductance $G_m \equiv i_o/v_{id}$. **(c)** Equivalent circuit for determining the output resistance $R_o \equiv v_x/i_x$.

The output current i_o can be found from a node equation at the output as

$$i_o = g_{m2}\left(\frac{v_{id}}{2}\right) - g_{m4}v_{b4} \tag{8.151}$$

Using Eq. (8.150), we obtain

$$i_o = g_{m2}\left(\frac{v_{id}}{2}\right) + g_{m4}g_{m1}r_{e3}\left(\frac{v_{id}}{2}\right) \tag{8.152}$$

Since all devices are operating at the same bias current, $g_{m1} = g_{m2} = g_{m4} = g_m$, where

$$g_m \simeq \frac{I/2}{V_T} \tag{8.153}$$

and $r_{e3} = \alpha_3/g_{m3} = \alpha/g_m \simeq 1/g_m$. Thus, for G_m, Eq. (8.152) yields

$$G_m = g_m \tag{8.154}$$

which is identical to the result found for the MOS circuit.

Next we determine the output resistance of the amplifier utilizing the equivalent circuit shown in Fig. 8.37(c). We urge the reader to carefully examine this circuit and to note that the analysis is very similar to that for the MOS pair. Note specifically that the total resistance between the collector of Q_1 and ground is approximately r_{e3}. Now, since this is a relatively low resistance, the input resistance of the CB transistor Q_1 will be approximately equal to its r_e, that is, r_{e1}. Then, the output resistance R_{o2} of transistor Q_2 can be found using Eq. (7.50) by noting that the resistance R_e in the emitter of Q_2 is approximately equal to r_{e1}; thus,

$$\begin{aligned} R_{o2} &\simeq r_{o2}[1 + g_{m2}(r_{e1} \| r_{\pi 2})] \\ &\simeq r_{o2}(1 + g_{m2} r_{e1}) \\ &\simeq 2r_{o2} \end{aligned} \tag{8.155}$$

where we made use of the fact that corresponding parameters of all four transistors are equal.

The current i can now be found as

$$i = \frac{v_x}{R_{o2}} = \frac{v_x}{2r_{o2}} \tag{8.156}$$

and the current i_x can be obtained from a node equation at the output as

$$i_x = 2i + \frac{v_x}{r_{o4}} = \frac{v_x}{r_{o2}} + \frac{v_x}{r_{o4}}$$

Thus,

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} \| r_{o4} \tag{8.157}$$

This expression simply says that the output resistance of the amplifier is equal to the parallel equivalent of the output resistance of the differential pair and the output resistance of the current mirror; a result identical to that obtained for the MOS pair.

Equations (8.154) and (8.157) can now be combined to obtain the differential gain,

$$A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_m(r_{o2} \| r_{o4}) \tag{8.158}$$

and since $r_{o2} = r_{o4} = r_o$, we can simplify Eq. (8.158) to

$$A_d = \tfrac{1}{2} g_m r_o \tag{8.159}$$

Although this expression is identical to that found for the MOS circuit, the gain here is much larger because $g_m r_o$ for the BJT is more than an order of magnitude greater than $g_m r_o$ of a MOSFET. The downside, however, lies in the low input resistance of BJT amplifiers. Indeed, the equivalent circuit of Fig. 8.37(b) indicates that, as expected, the differential input resistance of the differential amplifier is equal to $2r_\pi$,

$$R_{id} = 2r_\pi \tag{8.160}$$

in sharp contrast to the infinite input resistance of the MOS amplifier. Thus, while the voltage gain realized in an active-loaded BJT amplifier stage is large, when a subsequent BJT stage is

connected to the output, its inevitably low input resistance will drastically reduce the overall voltage gain.

Common-Mode Gain and CMRR The common-mode gain A_{cm} and the common-mode rejection ratio (CMRR) can be found following a procedure identical to that utilized in the MOS case. Figure 8.38 shows the circuit prepared for common-mode signal analysis. As we have done in the MOS case, we will represent each of Q_1 and Q_2 together with their emitter resistances by a short-circuit output current $i_{1,2}$ and an output resistance $R_{o1,2}$. The short-circuit output currents of Q_1 and Q_2 are given by

$$i_1 \simeq i_2 \simeq \frac{v_{icm}}{2R_{EE}} \tag{8.161}$$

It can be shown that the output resistances of Q_1 and Q_2, R_{o1} and R_{o2}, are very large compared with the other resistances between the collector nodes of Q_1 and Q_2 ground, and hence can be neglected. Then, the voltage v_{b3} at the common base connection of Q_3 and Q_4 can be found by multiplying i_1 by the total resistance between the common base node and ground as

$$v_{b3} = -i_1\left(\frac{1}{g_{m3}} \| r_{\pi 3} \| r_{o3} \| r_{\pi 4}\right) \tag{8.162}$$

In response to v_{b3} transistor Q_4 provides a collector current $g_{m4}v_{b3}$. At the output node we can write the equation

$$\frac{v_o}{r_{o4}} + g_{m4}v_{b3} + i_2 = 0 \tag{8.163}$$

Substituting for v_{b3} from Eq. (8.162) and for i_1 and i_2 from Eq. (8.161) gives

$$\begin{aligned} A_{cm} \equiv \frac{v_o}{v_{icm}} &= \frac{r_{o4}}{2R_{EE}}\left[g_{m4}\left(\frac{1}{g_{m3}} \| r_{\pi 3} \| r_{o3} \| r_{\pi 4}\right) - 1\right] \\ &= -\frac{r_{o4}}{2R_{EE}} \frac{\dfrac{1}{r_{\pi 3}} + \dfrac{1}{r_{\pi 4}} + \dfrac{1}{r_{o3}}}{g_{m3} + \dfrac{1}{r_{\pi 3}} + \dfrac{1}{r_{\pi 4}} + \dfrac{1}{r_{o3}}} \end{aligned} \tag{8.164}$$

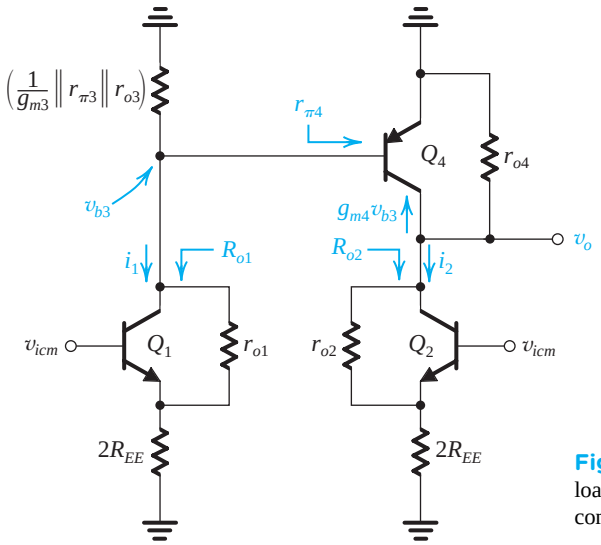


Figure 8.38 Analysis of the bipolar active-loaded differential amplifier to determine the common-mode gain.

where we have assumed $g_{m3} = g_{m4}$. Now, for $r_{\pi 4} = r_{\pi 3}$ and $r_{o3} \gg r_{\pi 3},\ r_{\pi 4}$, Eq. (8.164) gives

$$A_{cm} \simeq -\frac{r_{o4}}{2R_{EE}} \frac{\frac{2}{r_{\pi 3}}}{g_{m3} + \frac{2}{r_{\pi 3}}}$$

$$\simeq -\frac{r_{o4}}{2R_{EE}} \frac{2}{\beta_3} = -\frac{r_{o4}}{\beta_3 R_{EE}} \tag{8.165}$$

Using A_d from Eq. (8.158) enables us to obtain the CMRR as

$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|} = g_m(r_{o2} \| r_{o4})\left(\frac{\beta_3 R_{EE}}{r_{o4}}\right) \tag{8.166}$$

For $r_{o2} = r_{o4} = r_o$,

$$\text{CMRR} = \tfrac{1}{2}\beta_3 g_m R_{EE} \tag{8.167}$$

from which we observe that to obtain a large CMRR, the circuit implementing the bias current source should have a large output resistance R_{EE}. This is possible with, say, a Wilson current mirror (Section 7.5.3).

Before leaving the subject of the CM gain of the active-loaded differential amplifier, it is useful to reflect on the origin of its finite common-mode gain: It is simply due to the current transmission error introduced by the current-mirror load. In the case of the MOS circuit, this error is due to the finite r_{o3}; in the case of the bipolar mirror, the error is due to the finite β [Problem 8.98].

EXERCISE

8.17 For the active-loaded BJT differential amplifier let $I = 0.8$ mA, $V_A = 100$ V, and $\beta = 160$. Find G_m, R_o, A_d, and R_{id}. If the bias current source is implemented with a simple *npn* current mirror, find R_{EE}, A_{cm}, and CMRR.

Ans. 16 mA/V; 125 kΩ; 2000 V/V; 20 kΩ; 125 kΩ; –0.0125 V/V; 160,000 or 104 dB

Systematic Input Offset Voltage In addition to the random offset voltages that result from the mismatches inevitably present in the differential amplifier, the active-loaded bipolar differential pair suffers from a systematic offset voltage. This is due to the error in the current transfer ratio of the current-mirror load caused by the finite β of the *pnp* transistors that make up the mirror. To see how this comes about, refer to Fig. 8.39. Here the inputs are grounded and the transistors are assumed to be perfectly matched. Thus, the bias current I will divide equally between Q_1 and Q_2 with the result that their two collectors conduct equal currents of $\alpha I/2$. The collector current of Q_1 is fed to the input of the current mirror. From Section 7.4 we know that the current-transfer ratio of the mirror is

$$\frac{I_4}{I_3} = \frac{1}{1 + \frac{2}{\beta_P}} \tag{8.168}$$

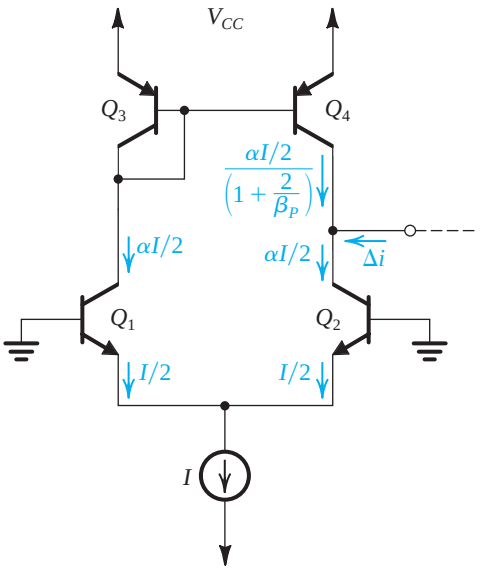


Figure 8.39 The active-loaded BJT differential pair suffers from a systematic input offset voltage resulting from the error in the current-transfer ratio of the current mirror.

where β_P is the value of β of the *pnp* transistors Q_3 and Q_4. Thus the collector current of Q_4 will be

$$I_4 = \frac{\alpha I/2}{1+\frac{2}{\beta_P}} \tag{8.169}$$

which does not exactly balance the collector current of Q_2. It follows that the current difference Δi will flow into the output terminal of the amplifier with

$$\begin{aligned}\Delta i &= \frac{\alpha I}{2} - \frac{\alpha I/2}{1+\frac{2}{\beta_P}} \\ &= \frac{\alpha I}{2}\frac{2/\beta_P}{1+\frac{2}{\beta_P}} \\ &\simeq \frac{\alpha I}{\beta_P}\end{aligned} \tag{8.170}$$

To reduce this output current to zero, an input voltage V_{OS} has to be applied with a value of

$$V_{OS} = -\frac{\Delta i}{G_m}$$

Substituting for Δi from Eq. (8.170) and for $G_m = g_m = (\alpha I/2)/V_T$, we obtain for the input offset voltage the expression

$$V_{OS} = -\frac{\alpha I/\beta_P}{\alpha I/2V_T} = -\frac{2V_T}{\beta_P} \tag{8.171}$$

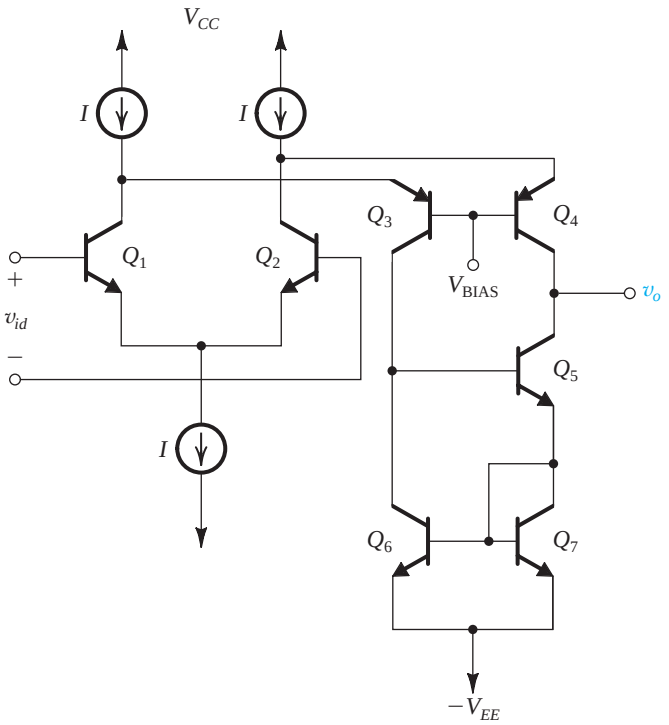


Figure 8.40 An active-loaded bipolar differential amplifier employing a folded cascode stage (Q_3 and Q_4) and a Wilson current-mirror load (Q_5, Q_6, and Q_7).

As an example, for $\beta_p = 50$, $V_{OS} = -1$ mV. To reduce V_{OS}, an improved current mirror such as the Wilson circuit studied in Section 7.5.3 should be used. Such a circuit provides the added advantage of increased output resistance and hence voltage gain. However, to realize the full advantage of the higher output resistance of the active load, the output resistance of the differential pair should be raised by utilizing a cascode stage. Figure 8.40 shows such an arrangement: A folded cascode stage formed by *pnp* transistors Q_3 and Q_4 is utilized to raise the output resistance looking into the collector of Q_4 to $\beta_4 r_{o4}$. A Wilson mirror formed by transistors Q_5, Q_6, and Q_7 is used to implement the active load. From Section 7.5.3 we know that the output resistance of the Wilson mirror (i.e., looking into the collector of Q_5) is $\beta_5(r_{o5}/2)$. Thus the output resistance of the amplifier is given by

$$R_o = \left[\beta_4 r_{o4} \parallel \beta_5 \frac{r_{o5}}{2}\right] \tag{8.172}$$

The transconductance G_m remains equal to g_m of Q_1 and Q_2. Thus the differential voltage gain becomes

$$A_d = g_m\left[\beta_4 r_{o4} \parallel \beta_5 \frac{r_{o5}}{2}\right] \tag{8.173}$$

which can be very large. Further examples of improved-performance differential amplifiers will be studied in Chapter 12.

EXERCISE

8.18 Find G_m and R_{o4}, R_{o5}, R_o, and A_d for the differential amplifier in Fig. 8.40 under the following conditions: $I = 1$ mA, $\beta_P = 50$, $\beta_N = 100$, and $V_A = 100$ V.
Ans. 20 mA/V; 10 MΩ; 10 MΩ; 5 MΩ; 10^5 V/V or 100 dB

8.6 Multistage Amplifiers

Practical transistor amplifiers usually consist of a number of stages connected in cascade. In addition to providing gain, the first (or input) stage is usually required to provide a high input resistance in order to avoid loss of signal level when the amplifier is fed from a high-resistance source. In a differential amplifier the input stage must also provide large common-mode rejection. The function of the middle stages of an amplifier cascade is to provide the bulk of the voltage gain. In addition, the middle stages provide such other functions as the conversion of the signal from differential mode to single-ended mode (unless, of course, the amplifier output also is differential) and the shifting of the dc level of the signal in order to allow the output signal to swing both positive and negative. These two functions and others will be illustrated later in this section and in greater detail in Chapter 12.

Finally, the main function of the last (or output) stage of an amplifier is to provide a low output resistance in order to avoid loss of gain when a low-valued load resistance is connected to the amplifier. Also, the output stage should be able to supply the current required by the load in an efficient manner—that is, without dissipating an unduly large amount of power in the output transistors. We have already studied one type of amplifier configuration suitable for implementing output stages, namely, the source follower and the emitter follower. It will be shown in Chapter 11 that the source and emitter followers are not optimum from the point of view of power efficiency and that other, more appropriate circuit configurations exist for output stages that are required to supply large amounts of output power. In fact, we will encounter some such output stages in the op-amp circuit examples studied in Chapter 12.

To illustrate the circuit structure and the method of analysis of multistage amplifiers, we will present two examples: a two-stage CMOS op amp and a four-stage bipolar op amp.

8.6.1 A Two-Stage CMOS Op Amp

Figure 8.41 shows a popular structure for CMOS op amps known as the **two-stage configuration**. The circuit utilizes two power supplies, which can range from ±2.5 V for the 0.5-μm technology down to ±0.9 V for the 0.18-μm technology. A reference bias current I_{REF} is generated either externally or using on-chip circuits. One such circuit will be discussed shortly. The current mirror formed by Q_8 and Q_5 supplies the differential pair $Q_1 - Q_2$ with bias current. The W/L ratio of Q_5 is selected to yield the desired value for the input-stage bias current I (or $I/2$ for each of Q_1 and Q_2). The input differential pair is actively loaded with the current mirror formed by Q_3 and Q_4. Thus the input stage is identical to that studied in Section 8.5

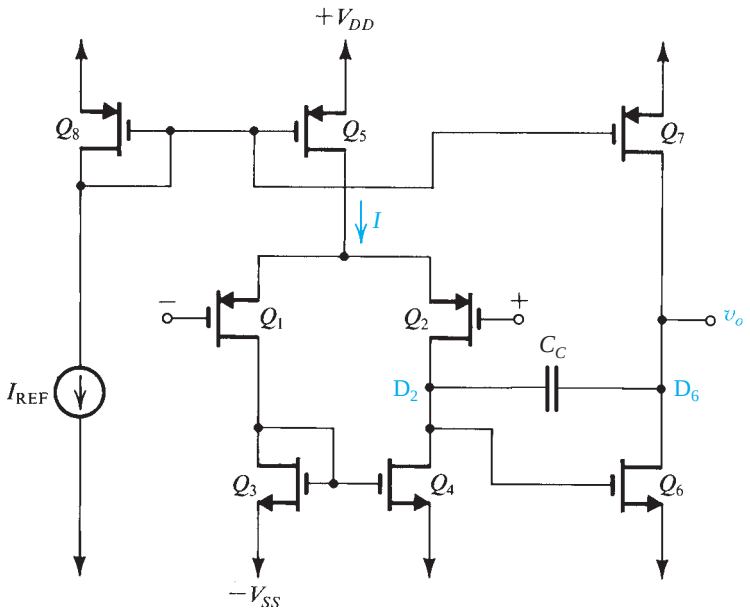


Figure 8.41 Two-stage CMOS op-amp configuration.

(except that here the differential pair is implemented with PMOS transistors and the current mirror with NMOS).

The second stage consists of Q_6, which is a common-source amplifier loaded with the current-source transistor Q_7. A capacitor C_C is included in the negative-feedback path of the second stage. Its function will be explained in Chapter 9, when we study the frequency response of amplifiers.

A striking feature of the circuit in Fig. 8.41 is that it does *not* have a low-output-resistance stage. In fact, the output resistance of the circuit is equal to $(r_{o6} \parallel r_{o7})$ and is thus rather high. This circuit, therefore, is not suitable for driving low-impedance loads. Nevertheless, the circuit is very popular and is used frequently for implementing op amps in VLSI circuits, where the op amp needs to drive only a small capacitive load, for example, in switched-capacitor circuits (Chapter 17). The simplicity of the circuit results in an op amp of reasonably good quality realized in a very small chip area.

Voltage Gain The voltage gain of the first stage was found in Section 8.5 to be given by

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \tag{8.174}$$

where g_{m1} is the transconductance of each of the transistors of the first stage, that is, Q_1 and Q_2.

The second stage is current-source-loaded, common-source amplifier whose voltage gain is given by

$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \tag{8.175}$$

The dc open-loop gain of the op amp is the product of A_1 and A_2.

Example 8.5

Consider the circuit in Fig. 8.41 with the following device geometries (in μm).

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8

Let $I_{REF} = 90$ μA, $V_{tn} = 0.7$ V, $V_{tp} = -0.8$ V, $\mu_n C_{ox} = 160$ μA/V^2, $\mu_p C_{ox} = 40$ μA/V^2, $|V_A|$ (for all devices) = 10 V, $V_{DD} = V_{SS} = 2.5$ V. For all devices, evaluate I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, and r_o. Also find A_1, A_2, the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on bias current.

Solution

Refer to Fig. 8.41. Since Q_8 and Q_5 are matched, $I = I_{REF}$. Thus Q_1, Q_2, Q_3, and Q_4 each conducts a current equal to $I/2 = 45$ μA. Since Q_7 is matched to Q_5 and Q_8, the current in Q_7 is equal to $I_{REF} = 90$ μA. Finally, Q_6 conducts an equal current of 90 μA.

With I_D of each device known, we use

$$I_D = \tfrac{1}{2}(\mu C_{ox})(W/L)V_{OV}^2$$

to determine $|V_{OV}|$ for each transistor. Then we find $|V_{GS}|$ from $|V_{GS}| = |V_t| + |V_{OV}|$. The results are given in Table 8.1.

The transconductance of each device is determined from

$$g_m = 2I_D/|V_{OV}|$$

The value of r_o is determined from

$$r_o = |V_A|/I_D$$

The resulting values of g_m and r_o are given in Table 8.1.

The voltage gain of the first stage is determined from

$$\begin{aligned} A_1 &= -g_{m1}(r_{o2} \parallel r_{o4}) \\ &= -0.3(222 \parallel 222) = -33.3 \text{ V/V} \end{aligned}$$

The voltage gain of the second stage is determined from

$$\begin{aligned} A_2 &= -g_{m6}(r_{o6} \parallel r_{o7}) \\ &= -0.6(111 \parallel 111) = -33.3 \text{ V/V} \end{aligned}$$

Table 8.1

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
I_D (μA)	45	45	45	45	90	90	90	90
$\|V_{OV}\|$ (V)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
$\|V_{GS}\|$ (V)	1.1	1.1	1	1	1.1	1	1.1	1.1
g_m (mA/V)	0.3	0.3	0.3	0.3	0.6	0.6	0.6	0.6
r_o (kΩ)	222	222	222	222	111	111	111	111

Example 8.5 *continued*

Thus the overall dc open-loop gain is

$$A_0 = A_1A_2 = (-33.3)\times(-33.3) = 1109 \text{ V/V}$$

or

$$20\log 1109 = 61 \text{ dB}$$

The lower limit of the input common-mode range is the value of input voltage at which Q_1 and Q_2 leave the saturation region. This occurs when the input voltage falls below the voltage at the drain of Q_1 by $|V_{tp}|$ volts. Since the drain of Q_1 is at $-2.5 + 1 = -1.5$ V, then the lower limit of the input common-mode range is -2.3 V.

The upper limit of the input common-mode range is the value of input voltage at which Q_5 leaves the saturation region. Since for Q_5 to operate in saturation the voltage across it (i.e., V_{SD5}) should at least be equal to the overdrive voltage at which it is operating (i.e., 0.3 V), the highest voltage permitted at the drain of Q_5 should be +2.2 V. It follows that the highest value of v_{ICM} should be

$$v_{ICM\max} = 2.2 - 1.1 = 1.1 \text{ V}$$

The highest allowable output voltage is the value at which Q_7 leaves the saturation region, which is $V_{DD} - |V_{OV7}| = 2.5 - 0.3 = 2.2$ V. The lowest allowable output voltage is the value at which Q_6 leaves saturation, which is $-V_{SS} + V_{OV6} = -2.5 + 0.3 = -2.2$ V. Thus, the output voltage range is -2.2 V to +2.2 V.

Input Offset Voltage The device mismatches inevitably present in the input stage give rise to an input offset voltage. The components of this input offset voltage can be calculated using the methods developed in Section 8.4.1. Because device mismatches are random, the resulting offset voltage is referred to as **random offset**. This is to distinguish it from another type of input offset voltage that can be present even if all appropriate devices are perfectly matched. This predictable or **systematic offset** can be minimized by careful design. Although it occurs also in BJT op amps, and we have encountered it in Section 8.5.5, it is usually much more pronounced in CMOS op amps because their gain-per-stage is rather low.

To see how systematic offset can occur in the circuit of Fig. 8.41, let the two input terminals be grounded. If the input stage is perfectly balanced, then the voltage appearing at the drain of Q_4 will be equal to that at the drain of Q_3, which is $(-V_{SS} + V_{GS4})$. Now this is also the voltage that is fed to the gate of Q_6. In other words, a voltage equal to V_{GS4} appears between gate and source of Q_6. Thus the drain current of Q_6, I_6, will be related to the drain current of Q_4, which is equal to $I/2$, by the relationship

$$I_6 = \frac{(W/L)_6}{(W/L)_4}(I/2) \tag{8.176}$$

In order for no offset voltage to appear at the output, this current must be exactly equal to the current supplied by Q_7. The latter current is related to the current I of the parallel transistor Q_5 by

$$I_7 = \frac{(W/L)_7}{(W/L)_5}I \tag{8.177}$$

Now, the condition for making $I_6 = I_7$ can be found from Eqs. (8.176) and (8.177) as

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5} \tag{8.178}$$

If this condition is not met, a systematic offset will result. From the specification of the device geometries in Example 8.5, we can verify that condition (8.178) is satisfied, and, therefore, the op amp analyzed in that example should not exhibit a systematic input offset voltage.

EXERCISE

8.19 Consider the CMOS op amp of Fig. 8.41 when fabricated in a 0.8-μm CMOS technology for which $\mu_n C_{ox} = 3\mu_p C_{ox} = 90\ \mu A/V^2$, $|V_t| = 0.8$ V, and $V_{DD} = V_{SS} = 2.5$ V. For a particular design, $I = 100\ \mu A$, $(W/L)_1 = (W/L)_2 = (W/L)_5 = 200$, and $(W/L)_3 = (W/L)_4 = 100$.

(a) Find the (W/L) ratios of Q_6 and Q_7 so that $I_6 = 100\ \mu A$.

(b) Find the overdrive voltage, $|V_{OV}|$, at which each of Q_1, Q_2, and Q_6 is operating.

(c) Find g_m for Q_1, Q_2, and Q_6.

(d) If $|V_A| = 10$ V, find r_{o2}, r_{o4}, r_{o6}, and r_{o7}.

(e) Find the voltage gains A_1 and A_2, and the overall gain A.

Ans. (a) $(W/L)_6 = (W/L)_7 = 200$; (b) 0.129 V, 0.129 V, 0.105 V; (c) 0.775 mA/V, 0.775 mA/V, 1.90 mA/V; (d) 200 kΩ, 200 kΩ, 100 kΩ, 100 kΩ; (e) –77.5 V/V, –95 V/V, 7363 V/V

A Bias Circuit That Stabilizes g_m

We conclude this section by presenting a bias circuit for the two-stage CMOS op amp. The circuit presented has the interesting and useful property of providing a bias current whose value is independent of both the supply voltage and the MOSFET threshold voltage. Furthermore, the transconductances of the transistors biased by this circuit have values that are determined only by a single resistor and the device dimensions.

The bias circuit is shown in Fig. 8.42. It consists of two deliberately mismatched transistors, Q_{12} and Q_{13}, with Q_{12} usually about four times wider than Q_{13}. A resistor R_B is connected in series with the source of Q_{12}. Since, as will be shown, R_B determines both the bias current I_B and the transconductance g_{m12}, its value should be accurate and stable; in most applications, R_B would be an off-chip resistor. In order to minimize the channel-length modulation effect on Q_{12}, we include a cascode transistor Q_{10} and a matched diode-connected transistor Q_{11} to provide a bias voltage for Q_{10}. Finally, a p-channel current mirror formed by a pair of matched devices, Q_8 and Q_9, both replicates the current I_B back to Q_{11} and Q_{13}, and provides a bias line for Q_5 and Q_7 of the CMOS op-amp circuit of Fig. 8.41.[5]

The circuit operates as follows: The current mirror (Q_8, Q_9) causes Q_{13} to conduct a current equal to that in Q_{12}, that is, I_B. Thus,

$$I_B = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{12}(V_{GS12} - V_t)^2 \tag{8.179}$$

and,

$$I_B = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{13}(V_{GS13} - V_t)^2 \tag{8.180}$$

From the circuit, we see that the gate-source voltages of Q_{12} and Q_{13} are related by

$$V_{GS13} = V_{GS12} + I_B R_B$$

[5]We denote the bias current of this circuit by I_B. If this circuit is utilized to bias the CMOS op amp of Fig. 8.41, then I_B becomes the reference current I_{REF}.

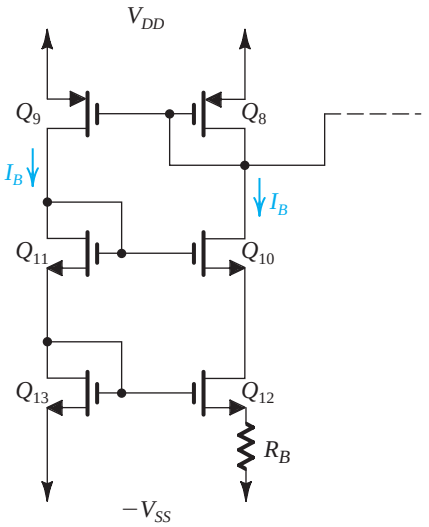


Figure 8.42 Bias circuit for the CMOS op amp.

Subtracting V_t from both sides of this equation and using Eqs. (8.179) and (8.180) to replace $(V_{GS12} - V_t)$ and $(V_{GS13} - V_t)$ results in

$$\sqrt{\frac{2I_B}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_B}{\mu_n C_{ox}(W/L)_{12}}} + I_B R_B \tag{8.181}$$

This equation can be rearranged to yield

$$I_B = \frac{2}{\mu_n C_{ox}(W/L)_{12} R_B^2}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right)^2 \tag{8.182}$$

from which we observe that I_B is determined by the dimensions of Q_{12} and the value of R_B and by the ratio of the dimensions of Q_{12} and Q_{13}. Furthermore, Eq. (8.182) can be rearranged to the form

$$R_B = \frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{12} I_B}}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right)$$

in which we recognize the factor $\sqrt{2\mu_n C_{ox}(W/L)_{12} I_B}$ as g_{m12}; thus,

$$g_{m12} = \frac{2}{R_B}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right) \tag{8.183}$$

This is a very interesting result: g_{m12} is determined solely by the value of R_B and the ratio of the dimensions of Q_{12} and Q_{13}. Furthermore, since g_m of a MOSFET is proportional to $\sqrt{I_D(W/L)}$, each transistor biased by the circuit of Fig. 8.42; that is, each transistor whose bias current is derived from I_B will have a g_m value that is a multiple of g_{m12}. Specifically, the ith n-channel MOSFET will have

$$g_{mi} = g_{m12}\sqrt{\frac{I_{Di}(W/L)_i}{I_B(W/L)_{12}}}$$

and the ith p-channel device will have

$$g_{mi} = g_{m12}\sqrt{\frac{\mu_p I_{Di}(W/L)_i}{\mu_n I_B (W/L)_{12}}}$$

Finally, it should be noted that the bias circuit of Fig. 8.42 employs **positive feedback**, and thus care should be exercised in its design to avoid unstable performance. Instability is avoided by making Q_{12} wider than Q_{13}, as has already been pointed out. Nevertheless, some form of instability may still occur; in fact, the circuit can operate in a stable state in which all currents are zero. To get it out of this state, current needs to be injected into one of its nodes, to "kick start" its operation. Feedback and stability will be studied in Chapter 10.

EXERCISES

8.20 Consider the bias circuit of Fig. 8.42 for the case of $(W/L)_8 = (W/L)_9 = (W/L)_{10} = (W/L)_{11} = (W/L)_{13} = 20$ and $(W/L)_{12} = 80$. The circuit is fabricated in a process technology for which $\mu_n C_{ox} = 90\ \mu A/V^2$. Find the value of R_B that results in a bias current $I_B = 10\ \mu A$. Also, find the transconductance g_{m12}.
Ans. 5.27 kΩ; 0.379 mA/V

D8.21 Design the bias circuit of Fig. 8.42 to operate with the CMOS op amp of Example 8.5. Use Q_8 and Q_9 as identical devices with Q_8 having the dimensions given in Example 8.5. Transistors Q_{10}, Q_{11}, and Q_{13} are to be identical, with the same g_m as Q_8 and Q_9. Transistor Q_{12} is to be four times as wide as Q_{13}. Find the required value of R_B. What is the voltage drop across R_B? Also give the values of the dc voltages at the gates of Q_{12}, Q_{10}, and Q_8.
Ans. 1.67 kΩ; 150 mV; −1.5 V; −0.5 V; +1.4 V

8.6.2 A Bipolar Op Amp

Our second example of multistage amplifiers is the four-stage bipolar op amp shown in Fig. 8.43. The circuit consists of four stages. The **differential-in**, **differential-out** input stage consists of transistors Q_1 and Q_2, which are biased by current source Q_3. The second stage is also a differential-input amplifier, but its output is taken single-endedly at the collector of Q_5. This stage is formed by Q_4 and Q_5, which are biased by the current source Q_6. Note that the conversion from differential to single-ended as performed by the second stage results in a loss of gain by a factor of 2. In the more elaborate method for accomplishing this conversion studied in Section 8.5, a current mirror was used as an active load.

In addition to providing some voltage gain, the third stage, consisting of the *pnp* transistor Q_7, provides the essential function of *shifting the dc level* of the signal. Thus, while the signal at the collector of Q_5 is not allowed to swing below the voltage at the base of Q_5 (+10 V), the signal at the collector of Q_7 can swing negatively (and positively, of course). From our study of op amps in Chapter 2, we know that the output terminal of the op amp should be capable of both positive and negative voltage swings. Therefore every op-amp circuit includes a **level-shifting** arrangement. Although the use of the complementary *pnp* transistor provides a simple solution to the level-shifting problem, other forms of level shifter exist, one of which will be discussed in Chapter 12. Furthermore, note that level shifting is

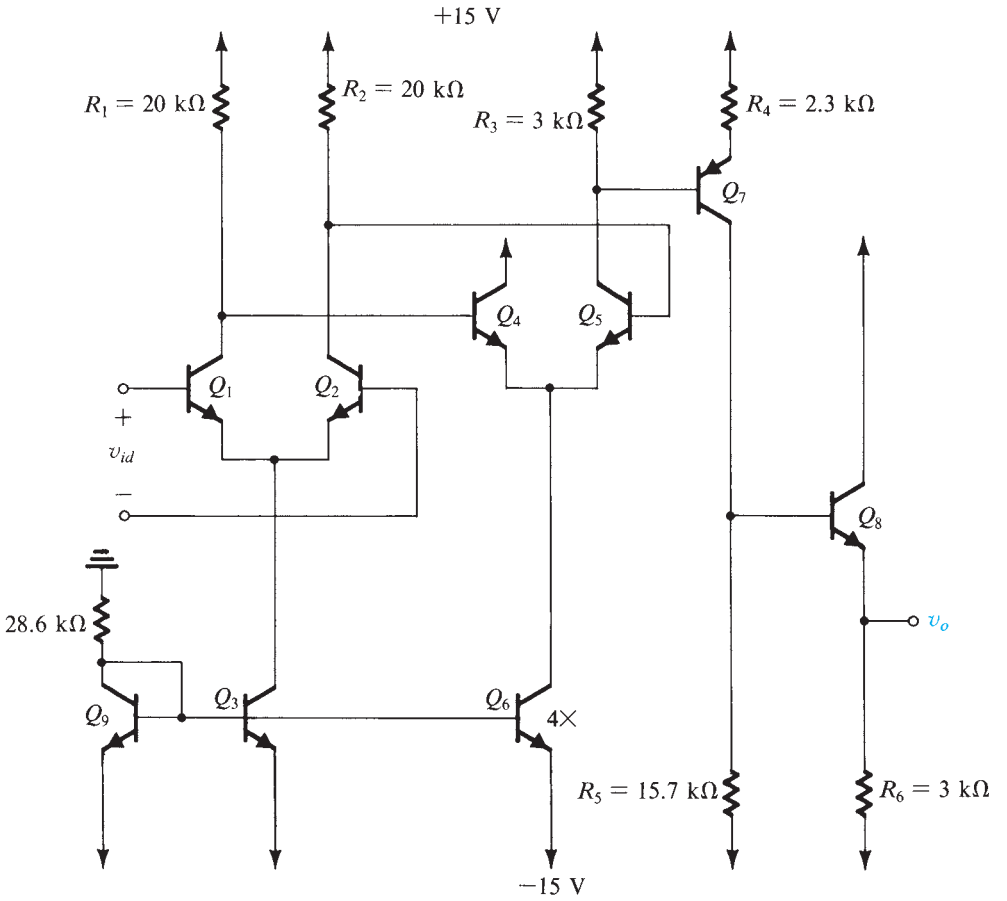


Figure 8.43 A four-stage bipolar op amp.

accomplished in the CMOS op amp we have been studying by using complementary devices for the two stages: that is, *p*-channel for the first stage and *n*-channel for the second stage.

The output stage of the op amp consists of emitter follower Q_8. As we know from our study of op amps in Chapter 2, ideally the output operates around zero volts. This and other features of the BJT op amp will be illustrated in Example 8.6.

Example 8.6

In this example, we analyze the dc bias of the bipolar op-amp circuit of Fig. 8.43. Toward that end, Fig. 8.44 shows the circuit with the two input terminals connected to ground.

(a) Perform an approximate dc analysis (assuming $\beta \gg 1$, $|V_{BE}| \simeq 0.7$ V, and neglecting the Early effect) to calculate the dc currents and voltages everywhere in the circuit. Note that Q_6 has four times the area of each of Q_9 and Q_3.
(b) Calculate the quiescent power dissipation in this circuit.

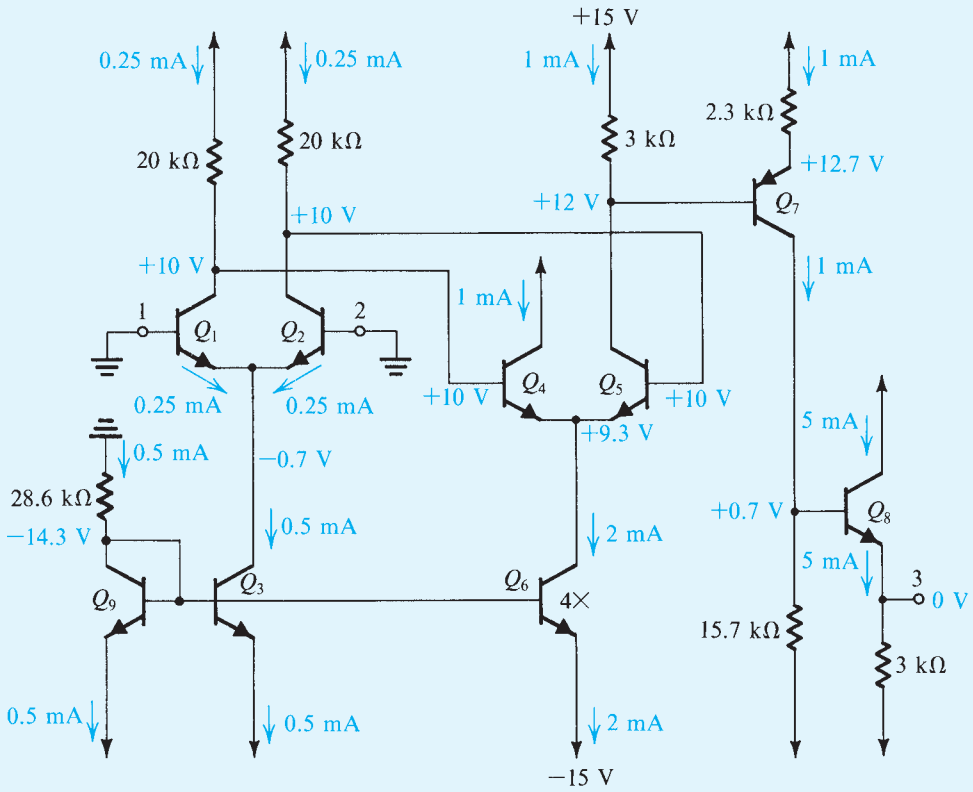


Figure 8.44 Circuit for Example 8.6.

(c) If transistors Q_1 and Q_2 have $\beta = 100$, calculate the input bias current of the op amp.
(d) What is the input common-mode range of this op amp?

Solution

(a) The values of all dc currents and voltages are indicated on the circuit diagram. These values were calculated by ignoring the base current of every transistor—that is, by assuming β to be very high. The analysis starts by determining the current through the diode-connected transistor Q_9 to be 0.5 mA. Then we see that transistor Q_3 conducts 0.5 mA and transistor Q_6 conducts 2 mA. The current-source transistor Q_3 feeds the differential pair (Q_1, Q_2) with 0.5 mA. Thus each of Q_1 and Q_2 will be biased at 0.25 mA. The collectors of Q_1 and Q_2 will be at $[+15 - 0.25 \times 20] = +10$ V.

Proceeding to the second differential stage formed by Q_4 and Q_5, we find the voltage at their emitters to be $[+10 - 0.7] = 9.3$ V. This differential pair is biased by the current-source transistor Q_6, which supplies a current of 2 mA; thus Q_4 and Q_5 will each be biased at 1 mA. We can now calculate the voltage at the collector of Q_5 as $[+15 - 1 \times 3] = +12$ V. This will cause the voltage at the emitter of the *pnp* transistor Q_7 to be +12.7 V, and the emitter current of Q_7 will be $(+15 - 12.7)/2.3 = 1$ mA.

The collector current of Q_7, 1 mA, causes the voltage at the collector to be $[-15 + 1 \times 15.7] = +0.7$ V. The emitter of Q_8 will be 0.7 V below the base; thus output terminal 3 will be at 0 V. Finally, the emitter current of Q_8 can be calculated to be $[0 - (-15)]/3 = 5$ mA.

Example 8.6 *continued*

(b) To calculate the power dissipated in the circuit in the quiescent state (i.e., with zero input signal) we simply evaluate the dc current that the circuit draws from each of the two power supplies. From the +15 V supply the dc current is $I^+ = 0.25 + 0.25 + 1 + 1 + 1 + 5 = 8.5$ mA. Thus the power supplied by the positive power supply is $P^+ = 15 \times 8.5 = 127.5$ mW. The –15-V supply provides a current I^- given by $I^- = 0.5 + 0.5 + 2 + 1 + 5 = 9$ mA. Thus the power provided by the negative supply is $P^- = 15 \times 9 = 135$ mW. Adding P^+ and P^- provides the total power dissipated in the circuit P_D: $P_D = P^+ + P^- = 262.5$ mW.

(c) The input bias current of the op amp is the average of the dc currents that flow in the two input terminals (i.e., in the bases of Q_1 and Q_2). These two currents are equal (because we have assumed matched devices); thus the bias current is given by

$$I_B = \frac{I_{E1}}{\beta + 1} \simeq 2.5\ \mu\text{A}$$

(d) The upper limit on the input common-mode voltage is determined by the voltage at which Q_1 and Q_2 leave the active mode and enter saturation. This will happen if the input voltage exceeds the collector voltage, which is +10 V, by about 0.4 V. Thus the upper limit of the common-mode range is +10.4 V.

The lower limit of the input common-mode range is determined by the voltage at which Q_3 leaves the active mode and thus ceases to act as a constant-current source. This will happen if the collector voltage of Q_3 goes below the voltage at its base, which is –14.3 V, by more than 0.4 V. It follows that the input common-mode voltage should not go lower than –14.7 + 0.7 = –14 V. Thus the common-mode range is –14 V to +10.4 V.

Example 8.7

Use the dc bias quantities evaluated in Example 8.6 to analyze the circuit in Fig. 8.43, to determine the input resistance, the voltage gain, and the output resistance.

Solution

The input differential resistance R_{id} is given by

$$R_{id} = r_{\pi 1} + r_{\pi 2}$$

Since Q_1 and Q_2 are each operating at an emitter current of 0.25 mA, it follows that

$$r_{e1} = r_{e2} = \frac{25}{0.25} = 100\ \Omega$$

Assume $\beta = 100$; then

$$r_{\pi 1} = r_{\pi 2} = 101 \times 100 = 10.1\ \text{k}\Omega$$

Thus,

$$R_{id} = 20.2\ \text{k}\Omega$$

To evaluate the gain of the first stage, we first find the input resistance of the second stage, R_{i2},

$$R_{i2} = r_{\pi 4} + r_{\pi 5}$$

Q_4 and Q_5 are each operating at an emitter current of 1 mA; thus

$$r_{e4} = r_{e5} = 25\ \Omega$$

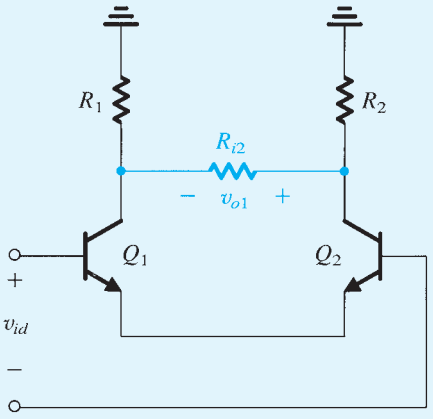


Figure 8.45 Equivalent circuit for calculating the gain of the input stage of the amplifier in Fig. 8.43.

$$r_{\pi 4} = r_{\pi 5} = 101 \times 25 = 2.525 \text{ k}\Omega$$

Thus $R_{i2} = 5.05$ kΩ. This resistance appears between the collectors of Q_1 and Q_2, as shown in Fig. 8.45. Thus the gain of the first stage will be

$$A_1 \equiv \frac{v_{o1}}{v_{id}} \simeq \frac{\text{Total resistance in collector circuit}}{\text{Total resistance in emitter circuit}}$$

$$= \frac{R_{i2} \parallel (R_1 + R_2)}{r_{e1} + r_{e2}}$$

$$= \frac{5.05 \text{ k}\Omega \parallel 40 \text{ k}\Omega}{200 \ \Omega} = 22.4 \text{ V/V}$$

Figure 8.46 shows an equivalent circuit for calculating the gain of the second stage. As indicated, the input voltage to the second stage is the output voltage of the first stage, v_{o1}. Also shown is the resistance R_{i3}, which is the input resistance of the third stage formed by Q_7. The value of R_{i3} can be found by

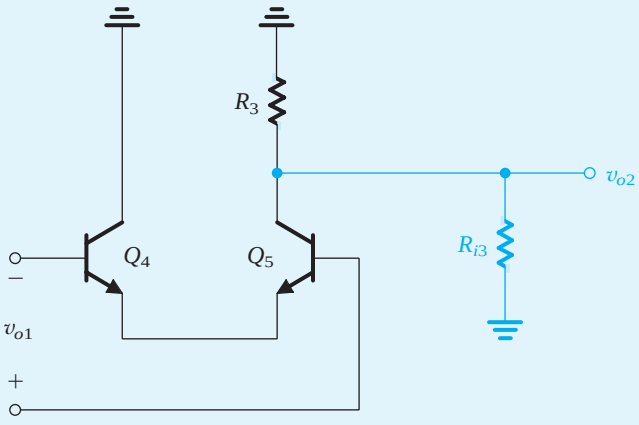


Figure 8.46 Equivalent circuit for calculating the gain of the second stage of the amplifier in Fig. 8.43.

Example 8.7 *continued*

multiplying the total resistance in the emitter of Q_7 by $(\beta+1)$:

$$R_{i3} = (\beta+1)(R_4 + r_{e7})$$

Since Q_7 is operating at an emitter current of 1 mA,

$$r_{e7} = \frac{25}{1} = 25\ \Omega$$
$$R_{i3} = 101 \times 2.325 = 234.8\ \text{k}\Omega$$

We can now find the gain A_2 of the second stage as the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit:

$$A_2 \equiv \frac{v_{o2}}{v_{o1}} \simeq -\frac{R_3 \parallel R_{i3}}{r_{e4} + r_{e5}}$$
$$= -\frac{3\ \text{k}\Omega \parallel 234.8\ \text{k}\Omega}{50\ \Omega} = -59.2\ \text{V/V}$$

To obtain the gain of the third stage we refer to the equivalent circuit shown in Fig. 8.47, where R_{i4} is the input resistance of the output stage formed by Q_8. Using the resistance-reflection rule, we calculate the value of R_{i4} as

$$R_{i4} = (\beta+1)(r_{e8} + R_6)$$

where

$$r_{e8} = \frac{25}{5} = 5\ \Omega$$
$$R_{i4} = 101(5 + 3000) = 303.5\ \text{k}\Omega$$

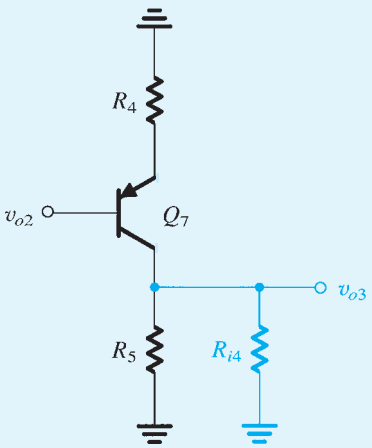


Figure 8.47 Equivalent circuit for evaluating the gain of the third stage in the amplifier circuit of Fig. 8.43.

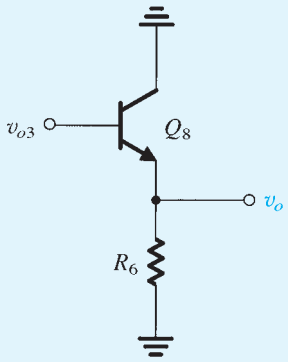


Figure 8.48 Equivalent circuit of the output stage of the amplifier circuit of Fig. 8.43.

The gain of the third stage is given by

$$A_3 \equiv \frac{v_{o3}}{v_{o2}} \simeq -\frac{R_5 \,\|\, R_{i4}}{r_{e7} + R_4}$$

$$= -\frac{15.7\ \text{k}\Omega \,\|\, 303.5\ \text{k}\Omega}{2.325\ \text{k}\Omega} = -6.42\ \text{V/V}$$

Finally, to obtain the gain A_4 of the output stage we refer to the equivalent circuit in Fig. 8.48 and write

$$A_4 \equiv \frac{v_o}{v_{o3}} = \frac{R_6}{R_6 + r_{e8}}$$

$$= \frac{3000}{3000 + 5} = 0.998 \simeq 1$$

The overall voltage gain of the amplifier can then be obtained as follows:

$$\frac{v_o}{v_{id}} = A_1 A_2 A_3 A_4 = 8513\ \text{V/V}$$

or 78.6 dB.

To obtain the output resistance R_o we "grab hold" of the output terminal in Fig. 8.43 and look back into the circuit. By inspection we find

$$R_o = R_6 \,\|\, [r_{e8} + R_5/(\beta + 1)]$$

which gives

$$R_o = 152\ \Omega$$

EXERCISE

8.22 Use the results of Example 8.7 to calculate the overall voltage gain of the amplifier in Fig. 8.43 when it is connected to a source having a resistance of 10 kΩ and a load of 1 kΩ.
Ans. 4943 V/V

Analysis Using Current Gains There is an alternative method for the analysis of bipolar multistage amplifiers that can be somewhat easier to perform in some cases. The method makes use of current gains or more appropriately current-transmission factors. In effect, one traces the transmission of the signal current throughout the amplifier cascade, evaluating all the current transmission factors in turn. We shall illustrate the method by using it to analyze the amplifier circuit of the preceding example.

Figure 8.49 shows the amplifier circuit prepared for small-signal analysis. We have indicated on the circuit diagram the signal currents through all the circuit branches. Also indicated are the input resistances of all four stages of the amplifier. These should be evaluated before commencing the following analysis.

The purpose of the analysis is to determine the overall voltage gain (v_o/v_{id}). Toward that end, we express v_o in terms of the signal current in the emitter of Q_8, i_{e8}, and v_{id} in terms of the input signal current i_i, as follows:

$$v_o = R_6 i_{e8}$$

$$v_{id} = R_{i1} i_i$$

Thus, the voltage gain can be expressed in terms of the current gain (i_{e8}/i_i) as

$$\frac{v_o}{v_{id}} = \frac{R_6}{R_{i1}} \frac{i_{e8}}{i_i}$$

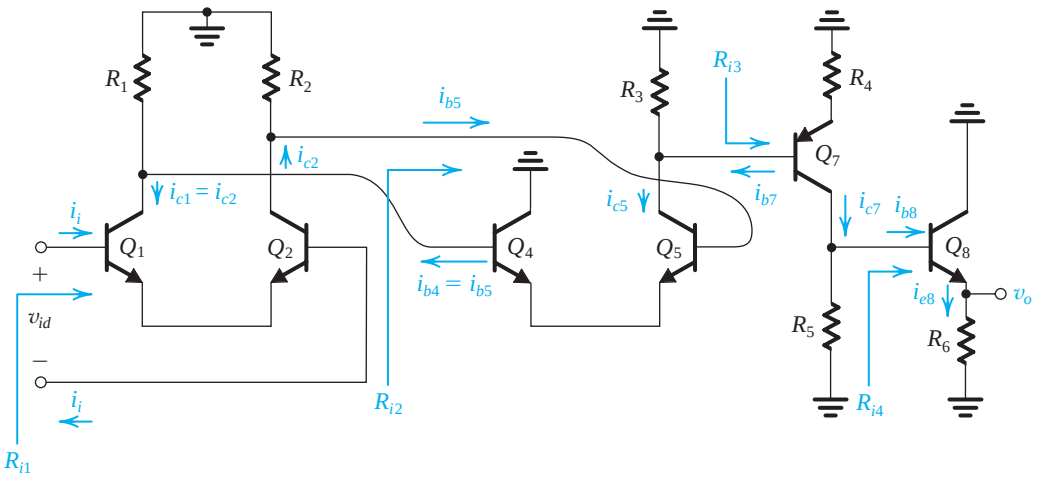


Figure 8.49 The circuit of the multistage amplifier of Fig. 8.43 prepared for small-signal analysis. Indicated are the signal currents throughout the amplifier and the input resistances of the four stages.

Next, we expand the current gain (i_{e8}/i_i) in terms of the signal currents throughout the circuit as follows:

$$\frac{i_{e8}}{i_i} = \frac{i_{e8}}{i_{b8}} \times \frac{i_{b8}}{i_{c7}} \times \frac{i_{c7}}{i_{b7}} \times \frac{i_{b7}}{i_{c5}} \times \frac{i_{c5}}{i_{b5}} \times \frac{i_{b5}}{i_{c2}} \times \frac{i_{c2}}{i_i}$$

Each of the current-transmission factors on the right-hand side is either the current gain of a transistor or the ratio of a current divider. Thus, reference to Fig. 8.49 enables us to find these factors by inspection:

$$\frac{i_{e8}}{i_{b8}} = \beta_8 + 1$$

$$\frac{i_{b8}}{i_{c7}} = \frac{R_5}{R_5 + R_{i4}}$$

$$\frac{i_{c7}}{i_{b7}} = \beta_7$$

$$\frac{i_{b7}}{i_{c5}} = \frac{R_3}{R_3 + R_{i3}}$$

$$\frac{i_{c5}}{i_{b5}} = \beta_5$$

$$\frac{i_{b5}}{i_{c2}} = \frac{(R_1 + R_2)}{(R_1 + R_2) + R_{i2}}$$

$$\frac{i_{c2}}{i_i} = \beta_2$$

These ratios can be easily evaluated and their values used to determine the voltage gain.

With a little practice, it is possible to carry out such an analysis very quickly, forgoing explicitly labeling the signal currents on the circuit diagram. One simply "walks through" the circuit, from input to output, or vice versa, determining the current-transmission factors one at a time, in a chainlike fashion.

EXERCISE

8.23 Use the values of input resistance found in Example 8.7 to evaluate the seven current-transmission factors and hence the overall current gain and voltage gain.

Ans. The current-transmission factors in the order of their listing are 101, 0.0492, 100, 0.0126, 100, 0.8879, 100 A/A; the overall current gain is 55993 A/A; the voltage gain is 8256 V/V. This value differs slightly from that found in Example 8.7, because of the various approximations made in the example (e.g., $\alpha \simeq 1$).

Summary

- The differential-pair or differential-amplifier configuration is the most widely used building block in analog IC design. The input stage of every op amp is a differential amplifier.
- There are two reasons for preferring differential to single-ended amplifiers: Differential amplifiers are insensitive to interference, and they do not need bypass and coupling capacitors.
- For a MOS (bipolar) pair biased by a current source I, each device operates at a drain (collector, assuming $\alpha = 1$) current of $I/2$ and a corresponding overdrive voltage V_{OV} (no analog in bipolar). Each device has $g_m = I/V_{OV}$ ($\alpha I/2V_T$, for bipolar) and $r_o = |V_A|/(I/2)$.
- With the two input terminals connected to a suitable dc voltage V_{CM}, the bias current I of a perfectly symmetrical differential pair divides equally between the two transistors of the pair, resulting in a zero voltage difference between the two drains (collectors). To steer the current completely to one side of the pair, a difference input voltage v_{id} of at least $\sqrt{2}V_{OV}$ ($4V_T$ for bipolar) is needed.
- Superimposing a differential input signal v_{id} on the dc common-mode input voltage V_{CM} such that $v_{I1} = V_{CM} + v_{id}/2$ and $v_{I2} = V_{CM} - v_{id}/2$ causes a virtual signal ground to appear on the common-source (common-emitter) connection. In response to v_{id}, the current in Q_1 increases by $g_m v_{id}/2$ and the current in Q_2 decreases by $g_m v_{id}/2$. Thus, voltage signals of $\pm g_m(R_D \parallel r_o)v_{id}/2$ develop at the two drains (collectors, with R_D replaced by R_C). If the output voltage is taken single-endedly, that is, between one of the drains (collectors) and ground, a differential gain of $\frac{1}{2}g_m(R_D \parallel r_o)$ is realized. When the output is taken differentially, that is, between the two drains (collectors), the differential gain realized is twice as large: $g_m(R_D \parallel r_o)$.
- The analysis of a differential amplifier to determine differential gain, differential input resistance, frequency response of differential gain, and so on is facilitated by employing the differential half-circuit, which is a common-source (common-emitter) transistor biased at $I/2$.
- An input common-mode signal v_{icm} gives rise to drain (collector) voltage signals that are ideally equal and given by $-v_{icm}(R_D/2R_{SS})$ [$-v_{icm}(R_C/2R_{EE})$ for the bipolar pair], where R_{SS} (R_{EE}) is the output resistance of the current source that supplies the bias current I. When the output is taken single-endedly, a common-mode gain of magnitude $|A_{cm}| = R_D/2R_{SS}$ ($R_C/2R_{EE}$ for the bipolar case) results. Taking the output differentially results, in the perfectly matched case, in zero A_{cm} (infinite CMRR). Mismatches between the two sides of the pair make A_{cm} finite even when the output is taken differentially: A mismatch ΔR_D causes $|A_{cm}| = (R_D/2R_{SS})(\Delta R_D/R_D)$; a mismatch Δg_m causes $|A_{cm}| = (R_D/2R_{SS})(\Delta g_m/g_m)$. Corresponding expressions apply for the bipolar pair.
- While the input differential resistance R_{id} of the MOS pair is infinite, that for the bipolar pair is only $2r_\pi$ but can be increased to $2(\beta+1)(r_e + R_e)$ by including resistances R_e in the two emitters. The latter action, however, lowers A_d.
- Mismatches between the two sides of a differential pair result in a differential dc output voltage V_O even when the two input terminals are tied together and connected to a dc voltage V_{CM}. This signifies the presence of an input offset voltage $V_{OS} \equiv V_O/A_d$. In a MOS pair there are three main sources for V_{OS}:

$$\Delta R_D \Rightarrow V_{OS} = \frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}$$

$$\Delta(W/L) \Rightarrow V_{OS} = \frac{V_{OV}}{2}\frac{\Delta(W/L)}{W/L}$$

$$\Delta V_t \Rightarrow V_{OS} = \Delta V_t$$

  For the bipolar pair there are two main sources:

$$\Delta R_C \Rightarrow V_{OS} = V_T\frac{\Delta R_C}{R_C}$$

$$\Delta I_S \Rightarrow V_{OS} = V_T\frac{\Delta I_S}{I_S}$$

- A popular circuit in both MOS and bipolar analog ICs is the current-mirror-loaded differential pair. It realizes a high differential gain $A_d = g_m(R_{o\,\text{pair}} \parallel R_{o\,\text{mirror}})$ and a low common-mode gain, $|A_{cm}| = \frac{1}{2}g_{m3}R_{SS}$ for the MOS circuit ($r_{o4}/\beta_3 R_{EE}$ for the bipolar circuit), as well as performing the differential-to-single-ended conversion with no loss of gain.
- The CMOS two-stage amplifier studied in Section 8.6.1 is intended for use as part of an IC system and thus is required to drive only small capacitive loads. Therefore it does not have an output stage with a low output resistance.
- A multistage amplifier typically consists of three or more stages: an input stage having a high input resistance, a reasonably high gain, and, if differential, a high CMRR; one or two intermediate stages that realize the bulk of the gain; and an output stage having a low output resistance. In designing and analyzing a multistage amplifier, the loading effect of each stage on the one that precedes it, must be taken into account.

Computer Simulation Problems

SIM Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the CD. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.
* difficult problem; ** more difficult; *** very challenging and/or time-consuming; D: design problem.

Section 8.1: The MOS Differential Pair

8.1 For an NMOS differential pair with a common-mode voltage V_{CM} applied, as shown in Fig. 8.2, let $V_{DD} = V_{SS} = 1.0$ V, $k_n' = 0.4$ mA/V^2, $(W/L)_{1,2} = 12.5$, $V_{tn} = 0.5$ V, $I = 0.2$ mA, $R_D = 10$ kΩ, and neglect channel-length modulation.

(a) Find V_{OV} and V_{GS} for each transistor.
(b) For $V_{CM} = 0$, find V_S, I_{D1}, I_{D2}, V_{D1}, and V_{D2}.
(c) Repeat (b) for $V_{CM} = +0.3$ V.
(d) Repeat (b) for $V_{CM} = -0.1$ V.
(e) What is the highest value of V_{CM} for which Q_1 and Q_2 remain in saturation?
(f) If current source I requires a minimum voltage of 0.2 V to operate properly, what is the lowest value allowed for V_S and hence for V_{CM}?

8.2 For the PMOS differential amplifier shown in Fig. P8.2 let $V_{tp} = -0.8$ V and $k_p'W/L = 4$ mA/V^2. Neglect channel-length modulation.

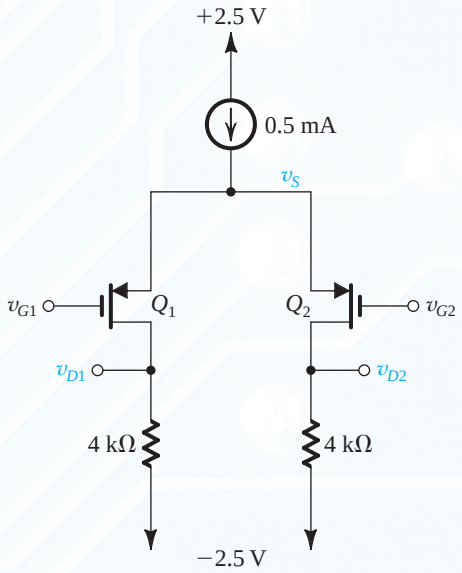


Figure P8.2

(a) For $v_{G1} = v_{G2} = 0$ V, find V_{OV} and V_{GS} for each of Q_1 and Q_2. Also find V_S, V_{D1}, and V_{D2}.
(b) If the current source requires a minimum voltage of 0.5 V, find the input common-mode range.

8.3 For the differential amplifier specified in Problem 8.1 let $v_{G2} = 0$ and $v_{G1} = v_{id}$. Find the value of v_{id} that corresponds to each of the following situations:

(a) $i_{D1} = i_{D2} = 0.1$ mA; (b) $i_{D1} = 0.15$ mA and $i_{D2} = 0.05$ mA; (c) $i_{D1} = 0.2$ mA and $i_{D2} = 0$ (Q_2 just cuts off); (d) $i_{D1} = 0.05$ mA and $i_{D2} = 0.15$ mA; (e) $i_{D1} = 0$ mA (Q_1 just cuts off) and $i_{D2} = 0.2$ mA. For each case, find v_S, v_{D1}, v_{D2}, and $(v_{D2} - v_{D1})$.

SIM **8.4** For the differential amplifier specified in Problem 8.2, let $v_{G2} = 0$ and $v_{G1} = v_{id}$. Find the range of v_{id} needed to steer the bias current from one side of the pair to the other. At each end of this range, give the value of the voltage at the common-source terminal and the drain voltages.

8.5 Consider the differential amplifier specified in Problem 8.1 with G_2 grounded and $v_{G1} = v_{id}$. Let v_{id} be adjusted to the value that causes $i_{D1} = 0.11$ mA and $i_{D2} = 0.09$ mA. Find the corresponding values of v_{GS2}, v_S, v_{GS1}, and hence v_{id}. What is the difference output voltage v_{D2}–v_{D1}? What is the voltage gain $(v_{D2} - v_{D1})/v_{id}$? What value of v_{id} results in $i_{D1} = 0.09$ mA and $i_{D2} = 0.11$ mA?

D **8.6** Design the circuit in Fig. P8.6 to obtain a dc voltage of +0.2V at each of the drains of Q_1 and Q_2 when $v_{G1} = v_{G2} = 0$ V. Operate all transistors at $V_{OV} = 0.2$ V and assume that for the process technology in which the circuit is fabricated, $V_{tn} = 0.5$ V and $\mu_n C_{ox} = 250$ μA/V^2. Neglect channel-length modulation. Determine the values of R, R_D, and the W/L ratios of Q_1, Q_2, Q_3, and Q_4. What is the input common-mode voltage range for your design?

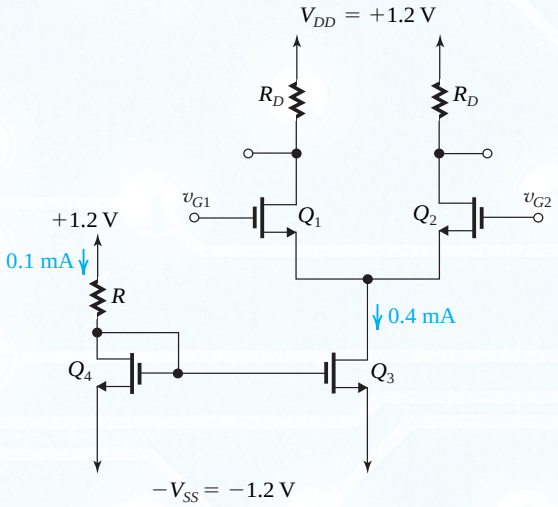


Figure P8.6

8.7 The table providing the answers to Exercise 8.3 shows that as the maximum input signal to be applied to the differential pair is increased, linearity is maintained at the same level by operating at a higher V_{OV}. If $|v_{id}|_{max}$ is to be 160 mV, use the data in the table to determine the required V_{OV} and the corresponding values of W/L and g_m.

8.8 Use Eq. (8.23) to show that if the term involving v_{id}^2 is to be kept to a maximum value of k then the maximum possible fractional change in the transistor current is given by

$$\frac{\Delta I_{max}}{I/2} = 2\sqrt{k(1-k)}$$

and the corresponding maximum value of v_{id} is given by

$$v_{id\,max} = 2\sqrt{k}V_{OV}$$

Evaluate both expressions for $k = 0.01$, 0.1, and 0.2.

8.9 An NMOS differential amplifier utilizes a bias current of 400 μA. The devices have $V_t = 0.5$ V, $W = 20$ μm, and $L = 0.5$ μm, in a technology for which $\mu_n C_{ox} = 200\ \mu A/V^2$. Find V_{GS}, and g_m in the equilibrium state. Also find the value of v_{id} for full-current switching. To what value should the bias current be changed in order to double the value of v_{id} for full-current switching?

D 8.10 Design the MOS differential amplifier of Fig. 8.5 to operate at $V_{OV} = 0.25$ V and to provide a transconductance g_m of 1 mA/V. Specify the W/L ratios and the bias current. The technology available provides $V_t = 0.8$ V and $\mu_n C_{ox} = 100\ \mu A/V^2$.

8.11 Consider the NMOS differential pair illustrated in Fig. 8.5 under the conditions that $I = 100$ μA, using FETs for which $k_n'(W/L) = 400\ \mu A/V^2$, and $V_t = 1$ V. What is the voltage on the common-source connection for $v_{G1} = v_{G2} = 0$? 2 V? What is the relation between the drain currents in each of these situations? Now for $v_{G2} = 0$ V, at what voltages must v_{G1} be placed to reduce i_{D2} by 10%? to increase i_{D2} by 10%? What is the differential voltage, $v_{id} = v_{G2} - v_{G1}$, for which the ratio of drain currents i_{D2}/i_{D1} is 1.0? 0.5? 0.9? 0.99? For the current ratio $i_{D1}/i_{D2} = 20.0$, what differential input is required?

***8.12** (a) For the MOS differential amplifier of Fig. 8.1 with $v_{G1} = V_{CM} + v_{id}/2$ and $v_{G2} = V_{CM} - v_{id}/2$, use Eqns. (8.23) and (8.24) to derive an expression for the output differential voltage $v_{od} \equiv v_{D2} - v_{D1}$ in terms of the input differential voltage v_{id}.
(b) Sketch and clearly label the voltage transfer characteristic (VTC), that is, v_{od} versus v_{id}, over the range $-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV}$, where V_{OV} is the overdrive voltage at which each transistor is operating in the equilibrium state. What is the slope of the nearly linear portion of the VTC near the origin? This is the differential voltage gain.
(c) Show on the same coordinates how the VTC changes if the bias current I is doubled? What is the change in the differential voltage gain?
(d) Prepare another sketch for case (b). Show on the same coordinates what happens to the VTC if the W/L ratio of each transistor is doubled. What is the change in the differential voltage gain?

Section 8.2: Small-Signal Operation of the MOS Differential Pair

8.13 An NMOS differential amplifier is operated at a bias current I of 0.4 mA and has a W/L ratio of 32, $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_A = 10$ V, and $R_D = 5$ kΩ. Find V_{OV}, g_m, r_o, and A_d.

D 8.14 It is required to design an NMOS differential amplifier to operate with a differential input voltage that can be as high as 0.1 V while keeping the nonlinear term under the square root in Eq. (8.23) to a maximum of 0.05. A transconductance g_m of 1 mA/V is needed. Find the required values of V_{OV}, I, and W/L. Assume that the technology available has $\mu_n C_{ox} = 200\ \mu A/V^2$. What differential gain A_d results when $R_D = 10$ kΩ? Assume $\lambda = 0$. What is the resulting output signal corresponding to v_{id} at its maximum value?

D 8.15 Design a MOS differential amplifier to operate from ±1-V power supplies and dissipate no more than 2 mW in the equilibrium state. The differential voltage gain A_d is to be 5 V/V and the output common-mode dc voltage is to be 0.5 V. (*Note*: This is the dc voltage at the drains). Assume $\mu_n C_{ox} = 400\ \mu A/V^2$ and neglect the Early effect. Specify I, R_D, and W/L.

D 8.16 Design a MOS differential amplifier to operate from ±1-V supplies and dissipate no more than 2 mW in its equilibrium state. Select the value of V_{OV} so that the value of v_{id} that steers the current from one side of the pair to the other is 0.4 V. The differential voltage gain A_d is to be 5 V/V. Assume $k_n' = 400\ \mu A/V^2$ and neglect the Early effect. Specify the required values of I, R_D, and W/L.

8.17 An NMOS differential amplifier employing equal drain resistors, $R_D = 47$ kΩ, has a differential gain A_d of 20 V/V.

(a) What is the value of g_m for each of the two transistors?
(b) If each of the two transistors is operating at an overdrive voltage $V_{OV} = 0.2$ V, what must the value of I be?
(c) For $v_{id} = 0$, what is the dc voltage across each R_D?
(d) If v_{id} is 20-mV peak-to-peak sine wave applied in a balanced manner but superimposed on $V_{CM} = 0.5$ V, what is

the lowest value that V_{DD} must have to ensure saturation-mode operation for Q_1 and Q_2 at all times? Assume $V_t = 0.5$ V.

8.18 A MOS differential amplifier is designed to have a differential gain A_d equal to the voltage gain obtained from a common-source amplifier. Both amplifiers utilize the same values of R_D and supply voltages, and all the transistors have the same W/L ratios. What must the bias current I of the differential pair be relative to the bias current I_D of the CS amplifier? What is the ratio of the power dissipation of the two circuits?

8.19 A differential amplifier is designed to have a differential voltage gain equal to the voltage gain of a common-source amplifier. Both amplifiers use the same values of R_D and supply voltages and are designed to dissipate equal amounts of power in their equilibrium or quiescent state. As well, all the transistors use the same channel length. What must the width W of the differential-pair transistors be relative to the width of the CS transistor?

D 8.20 Figure P8.20 shows a MOS differential amplifer with the drain resistors R_D implemented using diode-connected PMOS transistors, Q_3 and Q_4. Let Q_1 and Q_2 be matched, and Q_3 and Q_4 be matched.

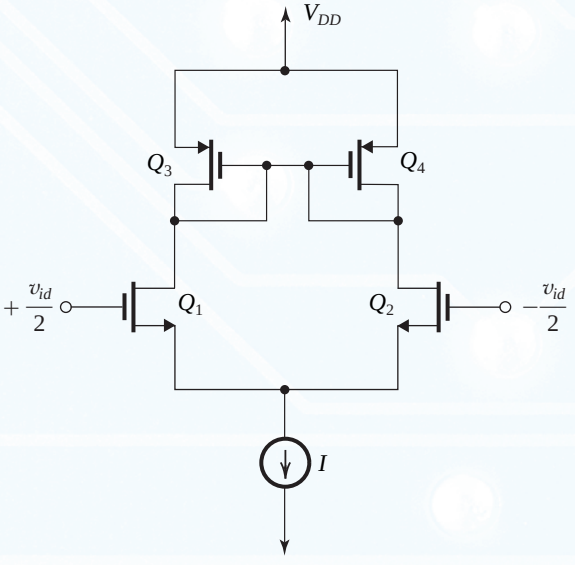


Figure P8.20

(a) Find the differential half-circuit and use it to derive an expression for A_d in terms of $g_{m1,2}$, $g_{m3,4}$, $r_{o1,2}$, and $r_{o3,4}$.
(b) Neglecting the effect of the output resistances r_o, find A_d in terms of μ_n, μ_p, $(W/L)_{1,2}$, and $(W/L)_{3,4}$.
(c) If $\mu_n = 4\mu_p$ and all four transistors have the same channel length, find $(W_{1,2}/W_{3,4})$ that results in $A_d = 10$ V/V.

8.21 Find the differential half-circuit for the differential amplifier shown in Fig. P8.21 and use it to derive an expression for the differential gain $A_d \equiv v_{od}/v_{id}$ in terms of g_m, R_D, and R_s. Neglect the Early effect. What is the gain with $R_s = 0$? What is the value of R_s (in terms of $1/g_m$) that reduces the gain to half this value?

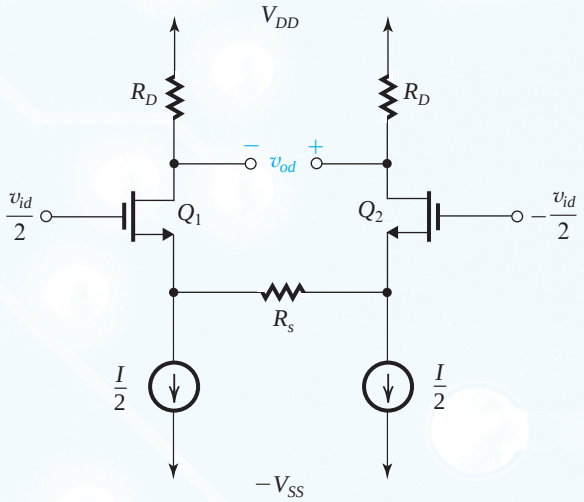


Figure P8.21

***8.22** The resistance R_s in the circuit of Fig. P8.21 can be implemented by using a MOSFET operated in the triode region, as shown in Fig. P8.22. Here Q_3 implements R_s, with the value of R_s determined by the voltage V_C at the gate of Q_3.

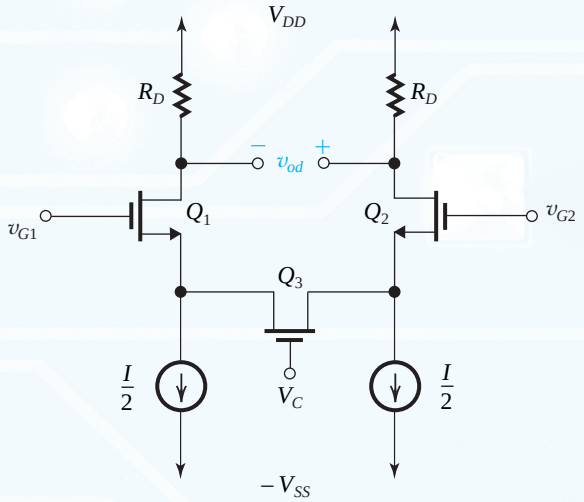


Figure P8.22

(a) With $v_{G1} = v_{G2} = 0$ V, and assuming that Q_1 and Q_2 are operating in saturation, what dc voltages appear at the sources of Q_1 and Q_2. Express these in terms of the overdrive voltage V_{OV} at which each of Q_1 and Q_2 operates, and V_t.
(b) For the situation in (a), what current flows in Q_3? What overdrive voltage V_{OV3} is Q_3 operating at, in terms of V_C, V_{OV}, and V_t?
(c) Now consider the case $v_{G1} = +v_{id}/2$ and $v_{G2} = -v_{id}/2$, where v_{id} is a small signal. Convince yourself that Q_3 now conducts current and operates in the triode region with a small v_{DS}. What resistance r_{DS} does it have, expressed in terms of the overdrive voltage V_{OV3} at which it is operating. This is the resistance R_s. Now if all three transistors have the same W/L, express R_s in terms of V_{OV}, V_{OV3}, and $g_{m1,2}$.

(d) Find V_{OV3} and hence V_C that result in (i) $R_s = 1/g_{m1,2}$; (ii) $R_s = 0.5/g_{m1,2}$.

***8.23** The circuit of Fig. P8.23 shows an effective way of implementing the resistance R_s needed for the circuit in Fig. P8.21. Here R_s is realized as the series equivalent of two MOSFETs Q_3 and Q_4 that are operated in the triode region, thus, $R_s = r_{DS3} + r_{DS4}$. Assume that Q_1 and Q_2 are matched and operate in saturation at an overdrive voltage V_{OV} that corresponds to a drain bias current of $I/2$. Also, assume that Q_3 and Q_4 are matched.

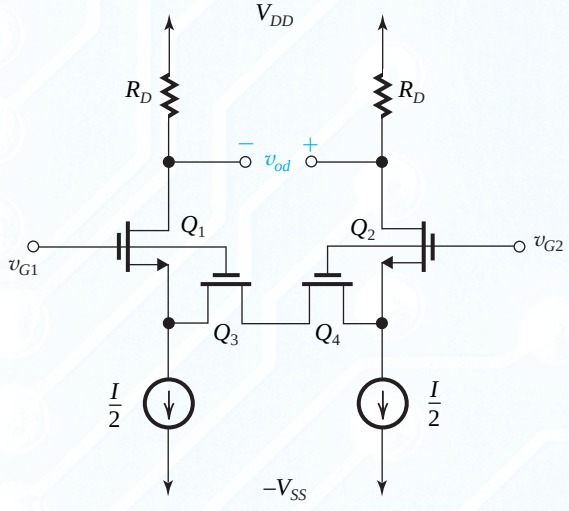


Figure P8.23

(a) With $v_{G1} = v_{G2} = 0$ V, what dc voltages appear at the sources of Q_1 and Q_2? What current flows through Q_3 and Q_4? At what overdrive voltages are Q_3 and Q_4 operating? Find an expression for r_{DS} for each of Q_3 and Q_4 and hence for R_s in terms of $(W/L)_{1,2}$, $(W/L)_{3,4}$, and $g_{m1,2}$.
(b) Now with $v_{G1} = v_{id}/2$ and $v_{G2} = -v_{id}/2$, where v_{id} is a small signal, find an expression of the voltage gain $A_d \equiv v_{od}/v_{id}$ in terms of $g_{m1,2}$, R_D, $(W/L)_{1,2}$, and $(W/L)_{3,4}$.

D *8.24 Figure P8.24 shows a circuit for a differential amplifier with an active load. Here Q_1 and Q_2 form the differential pair, while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2, respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of Q_1 and Q_2 is not shown. It is required to design the circuit to meet the following specifications:

(a) Differential gain $A_d = 80$ V/V.
(b) $I_{REF} = I = 100$ μA.
(c) The dc voltage at the gates of Q_6 and Q_3 is +1.5 V.
(d) The dc voltage at the gates of Q_7, Q_4, and Q_5 is −1.5 V.

The technology available is specified as follows: $\mu_n C_{ox} = 3\mu_p C_{ox} = 90$ μA/V^2; $V_{tn} = |V_{tp}| = 0.7$ V, $V_{An} = |V_{Ap}| = 20$ V. Specify the required value of R and the W/L ratios for all transistors. Also specify I_D and $|V_{GS}|$ at which each transistor is operating. For dc bias calculations you may neglect channel-length modulation.

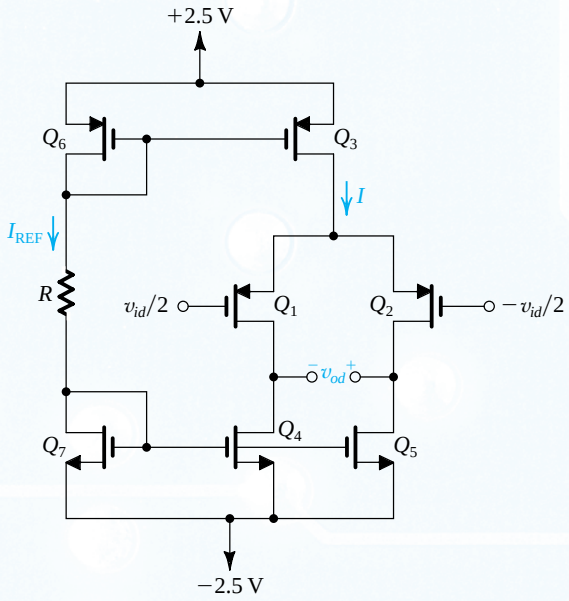


Figure P8.24

8.25 A design error has resulted in a gross mismatch in the circuit of Fig. P8.25. Specifically, Q_2 has twice the W/L ratio of Q_1. If v_{id} is a small sine-wave signal, find:

(a) I_{D1} and I_{D2}.
(b) V_{OV} for each of Q_1 and Q_2.
(c) The differential gain A_d in terms of R_D, I, and V_{OV}.

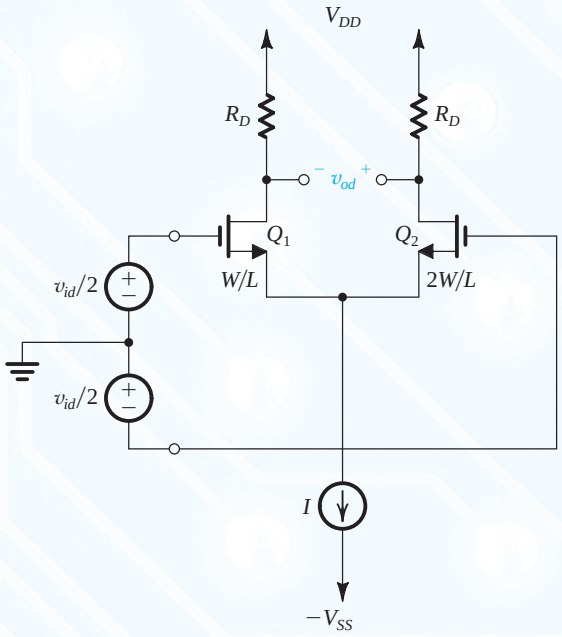


Figure P8.25

D 8.26 For the cascode differential amplifier of Fig. 8.12(a) show that if all transistors have the same channel length and are operated at the same $|V_{OV}|$ and assuming that $V'_{An} = |V'_{Ap}| = |V'_A|$, the differential gain A_d is given by

$$A_d = 2(|V_A|/|V_{OV}|)^2$$

Now design the amplifier to obtain a differential gain of 1000 V/V. Use $|V_{OV}| = 0.2$ V. If $|V'_A| = 10$ V/μm, specify the required channel length L. If g_m is to be as high as possible but the power dissipation in the amplifier (in equilibrium) is to be limited to 1 mW, what bias current I would you use? Let $V_{DD} = -V_{SS} = 0.9$ V.

SIM **8.27** An NMOS differential pair is biased by a current source $I = 0.2$ mA having an output resistance $R_{SS} = 100$ kΩ. The amplifier has drain resistances $R_D = 10$ kΩ, using transistors with $k'_nW/L = 3$ mA/V^2, and r_o that is large. If the output is taken differentially and there is a 1% mismatch between the drain resistances, find $|A_d|$, $|A_{cm}|$, and CMRR.

8.28 For the differential amplifier shown in Fig. P8.2, let Q_1 and Q_2 have $k'_p(W/L) = 4$ mA/V^2, and assume that the bias current source has an output resistance of 30 kΩ. Find $|V_{OV}|$, g_m, $|A_d|$, $|A_{cm}|$, and the CMRR (in dB) obtained with the output taken differentially. The drain resistances are known to have a mismatch of 2%.

SIM **D *8.29** The differential amplifier in Fig. P8.29 utilizes a resistor R_{SS} to establish a 1-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus the dc common-mode voltage V_{CM} cannot be zero. Transistors Q_1 and Q_2 have $k'_nW/L = 2.5$ mA/V^2, $V_t = 0.7$ V, and $\lambda = 0$.

(a) Find the required value of V_{CM}.
(b) Find the value of R_D that results in a differential gain A_d of 8 V/V.
(c) Determine the dc voltage at the drains.
(d) Determine the common-mode gain $\Delta V_{D1}/\Delta V_{CM}$. (*Hint:* You need to take $1/g_m$ into account.)
(e) Use the common-mode gain found in (d) to determine the change in V_{CM} that results in Q_1 and Q_2 entering the triode region.

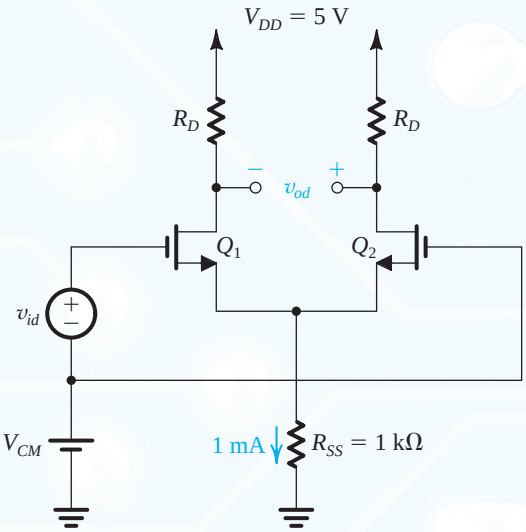


Figure P8.29

***8.30** The objective of this problem is to determine the common-mode gain and hence the CMRR of the differential pair arising from a simultaneous mismatch in g_m and in R_D.

(a) Refer to the circuit in Fig. 8.13(a) and its equivalent in Fig. 8.14, and let the two drain resistors be denoted R_{D1} and R_{D2} where $R_{D1} = R_D + (\Delta R_D/2)$ and $R_{D2} = R_D - (\Delta R_D/2)$. Also let $g_{m1} = g_m + (\Delta g_m/2)$ and $g_{m2} = g_m - (\Delta g_m/2)$. Follow an analysis process similar to that used to derive Eq. (8.63) to show that

$$A_{cm} \simeq \left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m} + \frac{\Delta R_D}{R_D}\right)$$

Note that this equation indicates that R_D can be deliberately varied to compensate for the initial variability in g_m and R_D, that is, to minimize A_{cm}.

(b) In a MOS differential amplifier for which $R_D = 5$ kΩ and $R_{SS} = 25$ kΩ, the common-mode gain is measured and found to be 0.002 V/V. Find the percentage change required in one of the two drain resistors so as to reduce A_{cm} to zero (or close to zero).

D 8.31 A MOS differential amplifier utilizing a simple current source to provide the bias current I is found to have a CMRR of 60 dB. If it is required to raise the CMRR to 100 dB by adding a cascode transistor to the current source, what must the intrinsic gain A_0 of the cascode transistor be? If the cascode transistor is operated at $V_{OV} = 0.2$ V, what must its V_A be? If for the specific technology utilized $V'_A = 10$ V/μm, specify the channel length L of the cascode transistor.

Section 8.3: The BJT Differential Pair

8.32 For the differential amplifier of Fig. 8.16(a) let $I = 0.5$ mA, $V_{CC} = V_{EE} = 2.5$ V, $V_{CM} = -1$ V, $R_C = 8$ kΩ, and $\beta = 100$. Assume that the BJTs have $v_{BE} = 0.7$ V at $i_C = 1$ mA. Find the voltage at the emitters and at the outputs.

8.33 An *npn* differential amplifier with $I = 0.5$ mA, $V_{CC} = V_{EE} = 2.5$ V, and $R_C = 8$ kΩ utilizes BJTs with $\beta = 100$ and $v_{BE} = 0.7$ V at $i_C = 1$ mA. If $v_{B2} = 0$, find V_E, V_{C1}, and V_{C2} obtained with $v_{B1} = +0.5$ V, and with $v_{B1} = -0.5$ V. Assume that the current source requires a minimum of 0.3 V for proper operation.

8.34 An *npn* differential amplifier with $I = 0.5$ mA, $V_{CC} = V_{EE} = 2.5$ V, and $R_C = 8$ kΩ utilizes BJTs with $\beta = 100$ and $v_{BE} = 0.7$ V at $i_C = 1$ mA. Assuming that the bias current is obtained by a simple current source and that all transistors require a minimum v_{CE} of 0.3 V for operation in the active mode, find the input common-mode range.

8.35 Repeat Exercise 8.9 for an input of –0.3 V.

8.36 An *npn* differential pair employs transistors for which $v_{BE} = 690$ mV at $i_C = 1$ mA, and $\beta = 50$. The transistors leave the active mode at $v_{CE} \leq 0.3$ V. The collector resistors $R_C = 82$ kΩ, and the power supplies are ±1.2 V. The bias current $I = 20$ μA and is supplied with a simple current source.

(a) For $v_{B1} = v_{B2} = V_{CM} = 0$ V, find V_E, V_{C1}, and V_{C2}.
(b) Find the input common-mode range.
(c) If $v_{B2} = 0$, find the value of v_{B1} that increases the current in Q_1 by 10%.

8.37 Consider the BJT differential amplifier when fed with a common-mode voltage V_{CM} as shown in Fig. 8.16(a). As is often the case, the supply voltage V_{CC} may not be pure dc but might include a ripple component v_r of small amplitude and a frequency of 120 Hz (see Section 4.5). Thus the supply voltage becomes $V_{CC} + v_r$. Find the ripple component of the collector voltages, v_{C1} and v_{C2}, as well as of the difference output voltage $v_{od} \equiv v_{C2} - v_{C1}$. Comment on the differential amplifier response to this undesirable power-supply ripple.

D 8.38 Consider the differential amplifier of Fig. 8.15 and let the BJT β be very large:

(a) What is the largest input common-mode signal that can be applied while the BJTs remain comfortably in the active region with $v_{CB} = 0$?
(b) If an input difference signal is applied that is large enough to steer the current entirely to one side of the pair, what is the change in voltage at each collector (from the condition for which $v_{id} = 0$)?
(c) If the available power supply V_{CC} is 2.5 V, what value of IR_C should you choose in order to allow a common-mode input signal of ±1.0 V?
(d) For the value of IR_C found in (c), select values for I and R_C. Use the largest possible value for I subject to the constraint that the base current of each transistor (when I divides equally) should not exceed 2 μA. Let $\beta = 100$.

8.39 To provide insight into the possibility of nonlinear distortion resulting from large differential input signals applied to the differential amplifier of Fig. 8.15, evaluate the normalized change in the current i_{E1}, $\Delta i_{E1}/I = (i_{E1} - (I/2))/I$, for differential input signals v_{id} of 5, 10, 20, 30, and 40 mV. Provide a tabulation of the ratio $(\Delta i_{E1}/I)/v_{id}$, which represents the proportional transconductance gain of the differential pair, versus v_{id}. Comment on the linearity of the differential pair as an amplifier.

D 8.40 Design the circuit of Fig. 8.15 to provide a differential output voltage (i.e., one taken between the two collectors) of 1 V when the differential input signal is 10 mV. A current source of 1 mA and a positive supply of +5 V are available. What is the largest possible input common-mode voltage for which operation is as required? Assume $\alpha \simeq 1$.

D *8.41 One of the trade-offs available in the design of the basic differential amplifier circuit of Fig. 8.15 is between the value of the voltage gain and the range of common-mode input voltage. The purpose of this problem is to demonstrate this trade-off.

(a) Use Eqs. (8.73) and (8.74) to obtain i_{C1} and i_{C2} corresponding to a differential input signal of 5 mV (i.e., $v_{B1} - v_{B2} = 5$ mV). Assume β to be very high. Find the resulting voltage dif-

ference between the two collectors ($v_{C2} - v_{C1}$), and divide this value by 5 mV to obtain the voltage gain in terms of (IR_C).
(b) Find the maximum permitted value for V_{CM} while the transistors remain comfortably in the active mode with $v_{CB} = 0$. Express this maximum in terms of V_{CC} and the gain, and hence show that for a given value of V_{CC}, the higher the gain achieved, the lower the common-mode range. Use this expression to find $V_{CM\max}$ corresponding to a gain magnitude of 100, 200, 300, and 400 V/V. For each value, also give the required value of IR_C and the value of R_C for $I = 1$ mA. As an example, discuss what can be achieved with $V_{CC} = 10$ V.

***8.42** For the circuit in Fig. 8.15, assuming $\alpha = 1$ and $IR_C = 5$ V, use Eqs. (8.70) and (8.71) to find i_{C1} and i_{C2}, and hence determine $v_{od} = v_{C2} - v_{C1}$ for input differential signals $v_{id} \equiv v_{B1} - v_{B2}$ of 5 mV, 10 mV, 15 mV, 20 mV, 25 mV, 30 mV, 35 mV, and 40 mV. Plot v_o versus v_{id}, and hence comment on the amplifier linearity. As another way of visualizing linearity, determine the gain (v_o/v_{id}) versus v_{id}. Comment on the resulting graph.

8.43 In a differential amplifier using a 3-mA emitter bias current source, the two BJTs are not matched. Rather, one has twice the emitter junction area of the other. For a differential input signal of zero volts, what do the collector currents become? What difference input is needed to equalize the collector currents? Assume $\alpha = 1$.

8.44 This problem explores the linearization of the transfer characteristics of the differential pair achieved by including emitter-degeneration resistances R_e in the emitters (see Fig. 8.18). Consider the case $I = 200$ µA with the transistors exhibiting $v_{BE} = 690$ mV at $i_C = 1$ mA and assume $\alpha \simeq 1$.

(a) With no emitter resistances R_e, what value of V_{BE} results when $v_{id} = 0$?
(b) With no emitter resistances R_e, use the large-signal model to find i_{C1} and i_{C2} when $v_{id} = 20$ mV.
(c) Now find the value of R_e that will result in the same i_{C1} and i_{C2} as in (b) but with $v_{id} = 200$ mV. Use the large-signal model.
(d) Calculate the effective transconductance G_m as the inverse of the total resistances in the emitter circuits in the cases without and with the R_e's. By what factor is G_m reduced? How does this factor relate to the increase in v_{id}? Comment.

8.45 A BJT differential amplifier uses a 200-µA bias current. What is the value of g_m of each device? If β is 150, what is the differential input resistance?

D 8.46 Design the basic BJT differential amplifier circuit of Fig. 8.19 to provide a differential input resistance of at least 10 kΩ and a differential voltage gain of 100 V/V. The transistor β is specified to be at least 100. The available positive power supply is 5 V.

8.47 For a differential amplifier to which a total difference signal of 10 mV is applied, what is the equivalent signal to its corresponding CE half-circuit? If the emitter current source I is 100 µA, what is r_e of the half-circuit? For a load resistance of 10 kΩ in each collector, what is the half-circuit gain? What magnitude of signal output voltage would you expect at each collector? Between the two collectors?

8.48 A BJT differential amplifier is biased from a 1-mA constant-current source and includes a 200-Ω resistor in each emitter. The collectors are connected to V_{CC} via 12-kΩ resistors. A differential input signal of 0.1 V is applied between the two bases.

(a) Find the signal current in the emitters (i_e) and the signal voltage v_{be} for each BJT.
(b) What is the total emitter current in each BJT?
(c) What is the signal voltage at each collector? Assume $\alpha = 1$.
(d) What is the voltage gain realized when the output is taken between the two collectors?

D 8.49 Design a BJT differential amplifier to amplify a differential input signal of 0.2 V and provide a differential output signal of 5 V. To ensure adequate linearity, it is required to limit the signal amplitude across each base–emitter junction to a maximum of 5 mV. Another design requirement is that the differential input resistance be at least 50 kΩ. The BJTs available are specified to have $\beta \geq 100$. Give the circuit configuration and specify the values of all its components.

D 8.50 Design a bipolar differential amplifier such as that in Fig. 8.19 to operate from ±2.5 V power supplies and to provide differential gain of 40 V/V. The power dissipation in the quiescent state should not exceed 2 mW.

(a) Specify the values of I and R_C. What dc voltage appears at the collectors?
(b) If $\beta = 100$, what is the input differential resistance?
(c) For $v_{id} = 20$ mV, what is the signal voltage at each of the collectors?
(d) For the situation in (c), what is the maximum allowable value of the input common mode voltage, V_{CM}? Recall that to maintain an *npn* BJT in saturation, v_B should not exceed v_C by more than 0.4 V.

D *8.51 In this problem we explore the trade-off between input common-mode range and differential gain in the design of the bipolar BJT. Consider the bipolar differential amplifier in Fig. 8.15 with the input voltages

$$v_{B1} = V_{CM} + (v_{id}/2)$$
$$v_{B2} = V_{CM} - (v_{id}/2)$$

(a) Bearing in mind that for a BJT to remain in the active mode, v_{BC} should not exceed 0.4 V, show that when v_{id}

has a peak $\hat{v}_{id}$, the maximum input common-mode voltage $V_{CM\max}$ is given by

$$V_{CM\max} = V_{CC} + 0.4 - \frac{\hat{v}_{id}}{2} - A_d\left(V_T + \frac{\hat{v}_{id}}{2}\right)$$

(b) For the case $V_{CC} = 5$ V and $\hat{v}_{id} = 10$ mV, use the relationship above to determine $V_{CM\max}$ for the case $A_d = 100$ V/V. Also find the peak output signal $\hat{v}_{od}$ and the required value of IR_C. Now if the power dissipation in the circuit is to be limited to 5 mW in the quiescent state (i.e., with $v_{id} = 0$), find I and R_C. (Remember to include the power drawn from the negative power supply $-V_{EE} = -5$ V.)

(c) If $V_{CM\max}$ is to be 0 V, and all other conditions remain the same, what gain A_d is achievable?

8.52 For the differential amplifier of Fig. 8.15, let $V_{CC} = +5$ V and $IR_C = 4$ V. Find the differential gain A_d. Sketch and clearly label the waveforms for the total collector voltages v_{C1} and v_{C2} for the following two cases:

(a) $v_{B1} = 1 + 0.005\sin(\omega t)$

$v_{B2} = 1 - 0.005\sin(\omega t)$

(b) $v_{B1} = 1 + 0.1\sin(\omega t)$

$v_{B2} = 1 - 0.1\sin(\omega t)$

8.53 Consider a bipolar differential amplifier in which the collector resistors R_C are replaced with simple current sources implemented using *pnp* transistors. Sketch the circuit and give its differential half-circuit. If $V_A = 10$ V for all transistors, find the differential voltage gain achieved.

8.54 For each of the emitter-degenerated differential amplifiers shown in Fig. P8.54, find the differential half-circuit and derive expressions for the differential gain A_d and differential input resistance R_{id}. For each circuit, what dc voltage appears across the bias current source(s) in the quiescent state (i.e., with $v_{id} = 0$). Hence, which of the two circuits will allow a larger negative V_{CM}?

8.55 Consider a bipolar differential amplifier that, in addition to the collector resistances R_C, has a load resistance R_L connected between the two collectors. What does the differential gain A_d become?

8.56 A bipolar differential amplifier having resistance R_e inserted in series with each emitter (as in Fig. 8.21) is biased with a constant current I. When both input terminals are grounded, the dc voltage measured across each R_e is found to be $4V_T$ and that measured across each R_C is found to be $40V_T$. What differential voltage gain A_d do you expect the amplifier to have?

8.57 A bipolar differential amplifier with emitter degeneration resistances R_e and R_e, is fed with the arrangement shown in Fig. P8.57. Derive an expression for the overall differential voltage gain $G_v \equiv v_{od}/v_{sig}$. If R_{sig} is of such a value that $v_{id} = 0.5v_{\text{sig}}$, find the gain G_v in terms of R_C,

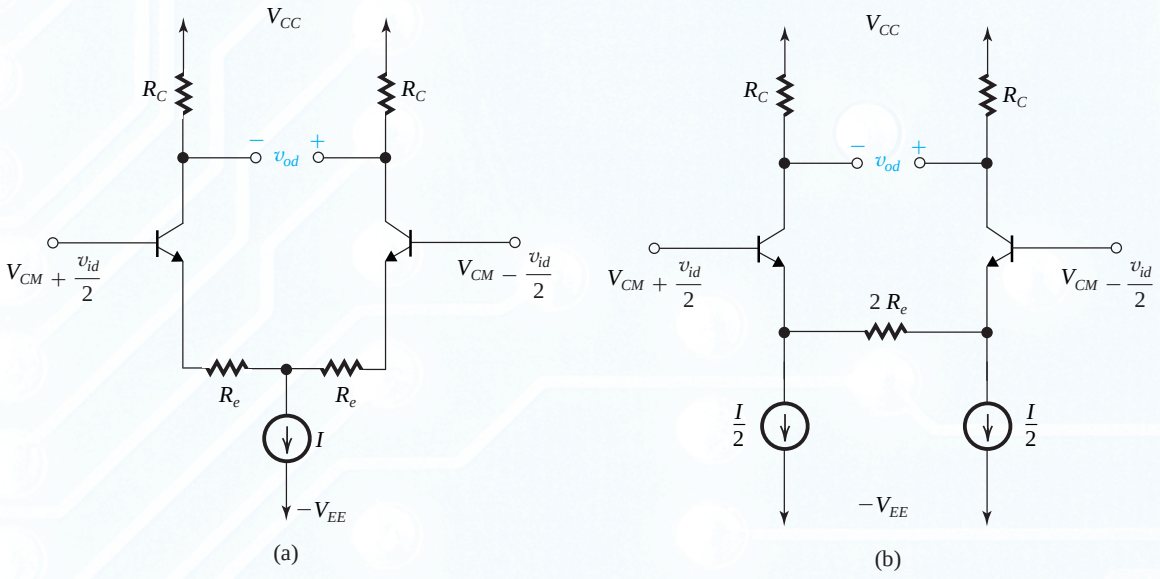


Figure P8.54

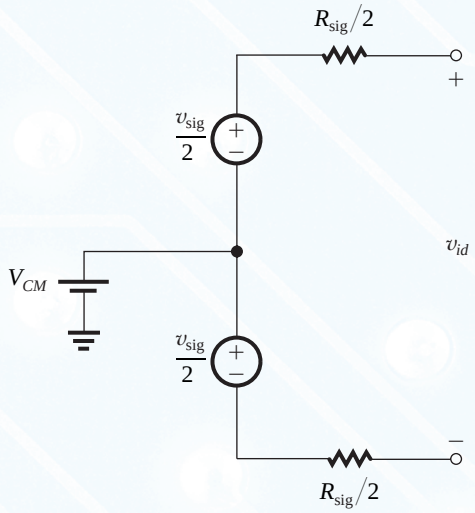


Figure P8.57

r_e, R_e, and α. Now if β is doubled, by what factor does G_v increase?

8.58 A particular differential amplifier operates from an emitter current source whose output resistance is 0.5 MΩ. What resistance is associated with each common-mode half-circuit? For collector resistors of 20 kΩ and 1% tolerance, what is the resulting common-mode gain for output taken (a) single-endedly? and (b) differentially?

8.59 Find the voltage gain and the input resistance of the amplifier shown in Fig. P8.59 assuming $\beta = 100$.

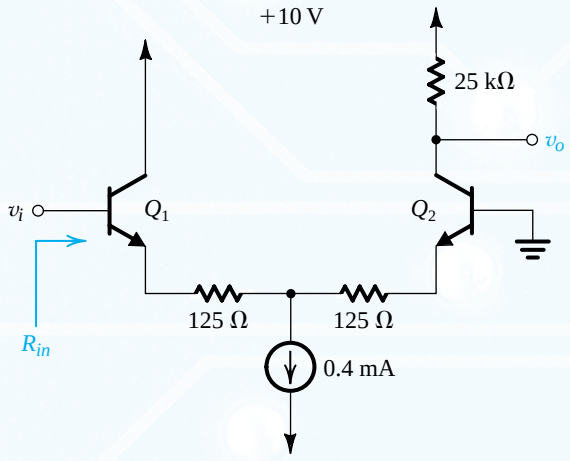


Figure P8.59

8.60 Find the voltage gain and input resistance of the amplifier in Fig. P8.60 assuming that $\beta = 100$.

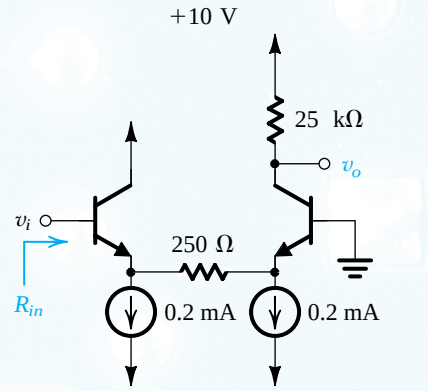


Figure P8.60

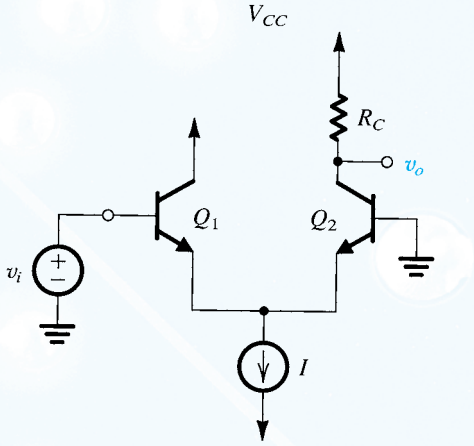


Figure P8.61

8.61 Derive an expression for the small-signal voltage gain v_o/v_i of the circuit shown in Fig. P8.61 in two different ways:

(a) as a differential amplifier
(b) as a cascade of a common-collector stage Q_1 and a common-base stage Q_2

Assume that the BJTs are matched and have a current gain α, and neglect the Early effect. Verify that both approaches lead to the same result.

8.62 The differential amplifier circuit of Fig. P8.62 utilizes a resistor connected to the negative power supply to establish the bias current I.

(a) For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$.
(b) For $v_{B1} = v_{B2} = v_{icm}$, where v_{icm} has a zero average, find the magnitude of the common-mode gain, $|v_o/v_{icm}|$.
(c) Calculate the CMRR.
(d) If $v_{B1} = 0.1 \sin 2\pi \times 60t + 0.005 \sin 2\pi \times 1000t$ volts, and $v_{B2} = 0.1 \sin 2\pi \times 60t - 0.005 \sin 2\pi \times 1000t$, volts, find v_o.

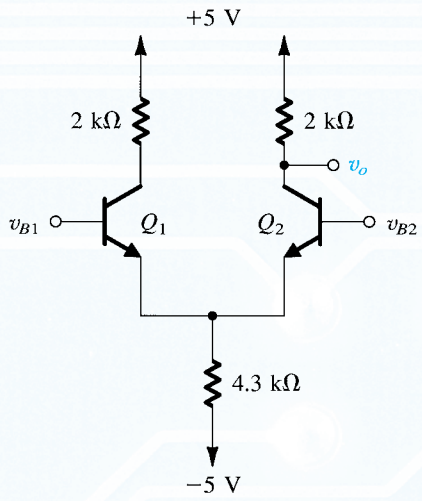


Figure P8.62

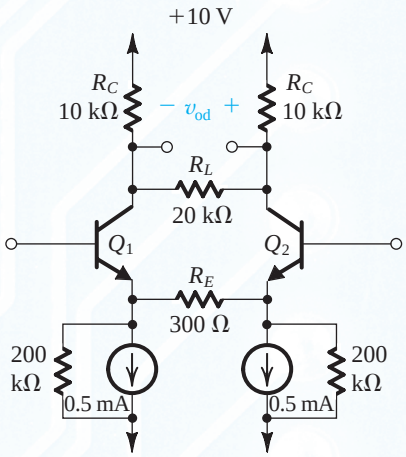


Figure P8.63

8.63 For the differential amplifier shown in Fig. P8.63, identify and sketch the differential half-circuit and the common-mode half-circuit. Find the differential gain, the differential input resistance, the common-mode gain assuming the resistances R_C have 1% tolerance, and the common-mode input resistance. For these transistors, $\beta = 100$ and $V_A = 100$ V.

8.64 Consider the basic differential circuit in which the transistors have $\beta = 100$ and $V_A = 100$ V, with $I = 0.5$ mA, $R_{EE} = 200$ kΩ, and $R_C = 20$ kΩ. The collector resistances are matched to within 1%. Find:

(a) the differential gain
(b) the differential input resistance
(c) the common-mode gain
(d) the common-mode rejection ratio
(e) the input common-mode resistance

8.65 In a differential-amplifier circuit resembling that shown in Fig. 8.26(a), the current generator represented by I and R_{EE} consists of a simple common-emitter transistor operating at 100 μA. For this transistor, and those used in the differential pair, $V_A = 20$ V and $\beta = 50$. What common-mode input resistance would result?

8.66 A bipolar differential amplifier with $I = 0.5$ mA utilizes transistors for which $V_A = 10$ V and $\beta = 100$. The collector resistances $R_C = 10$ kΩ and are matched to within 2%. Find:

(a) the differential gain
(b) the common-mode gain and the CMRR if the bias current I is generated using a simple current mirror
(c) the common-mode gain and the CMRR if the bias current I is generated using a Wilson mirror. (Refer to Eq. 7.81 for R_o of the Wilson mirror.)

D 8.67 It is required to design a differential amplifier to provide the largest possible signal to a pair of 10-kΩ load resistances. The input differential signal is a sinusoid of 5-mV peak amplitude, which is applied to one input terminal while the other input terminal is grounded. The power supply available is 10 V. To determine the required bias current I, derive an expression for the total voltage at each of the collectors in terms of V_{CC} and I in the presence of the input signal. Then impose the condition that both transistors should remain well out of saturation with a minimum v_{CB} of approximately 0 V. Thus determine the required value of I. For this design, what differential gain is achieved? What is the amplitude of the signal voltage obtained between the two collectors? Assume $\alpha \simeq 1$.

D *8.68 Design a BJT differential amplifier that provides two single-ended outputs (at the collectors). The amplifier is to have a differential gain (to each of the two outputs) of at least 100 V/V, a differential input resistance ≥10 kΩ, and a common-mode gain (to each of the two outputs) no greater than 0.1 V/V. Use a 2-mA current source for biasing. Give the complete circuit with component values and suitable power supplies that allow for ±2 V swing at each collector. Specify the minimum value that the output resistance of the bias current source must have. The BJTs available have $\beta \geq 100$. What is the value of the input common-mode resistance when the bias source has the lowest acceptable resistance?

8.69 When the output of a BJT differential amplifier is taken differentially, its CMRR is found to be 40 dB higher than when the output is taken single-endedly. If the only source of common-mode gain when the output is taken differentially is the mismatch in collector resistances, what must this mismatch be (in percent)?

***8.70** In a particular BJT differential amplifier, a production error results in one of the transistors having an emitter–

base junction area that is twice that of the other. With the inputs grounded, how will the emitter bias current split between the two transistors? If the output resistance of the current source is 500 kΩ and the resistance in each collector (R_C) is 12 kΩ, find the common-mode gain obtained when the output is taken differentially. Assume $\alpha \simeq 1$.

Section 8.4: Other Nonideal Characteristics of the Differential Amplifier

D 8.71 An NMOS differential pair is to be used in an amplifier whose drain resistors are 10 kΩ ± 1%. For the pair, $k_n'W/L = 4$ mA/V^2. A decision is to be made concerning the bias current I to be used, whether 160 μA or 360 μA. Contrast the differential gain and input offset voltage for the two possibilities.

D 8.72 An NMOS amplifier, whose designed operating point is at $V_{OV} = 0.2$ V, is suspected to have a variability of V_t of ±5 mV, and of W/L and R_D (independently) of ±2%. What is the worst-case input offset voltage you would expect to find? What is the major contribution to this total offset? If you used a variation of one of the drain resistors to reduce the output offset to zero and thereby compensate for the uncertainties (including that of the other R_D), what percentage change from nominal would you require? If by selection you reduced the contribution of the worst cause of offset by a factor of 10, what change in R_D would be needed?

8.73 An NMOS differential pair operating at a bias current I of 100 μA uses transistors for which $k_n' = 250$ μA/V^2 and $W/L = 10$. Find the three components of input offset voltage under the conditions that $\Delta R_D/R_D = 5\%$, $\Delta(W/L)/(W/L) = 5\%$, and $\Delta V_t = 5$ mV. In the worst case, what might the total offset be? For the usual case of the three effects being independent, what is the offset likely to be?

8.74 A bipolar differential amplifier uses two well-matched transistors but collector load resistors that are mismatched by 8%. What input offset voltage is required to reduce the differential output voltage to zero?

8.75 A bipolar differential amplifier uses two transistors whose scale currents I_S differ by 10%. If the two collector resistors are well matched, find the resulting input offset voltage.

8.76 Modify Eq. (8.119) for the case of a differential amplifier having a resistance R_E connected in the emitter of each transistor. Let the bias current source be I.

8.77 A differential amplifier uses two transistors whose β values are β_1 and β_2. If everything else is matched, show that the input offset voltage is approximately $V_T[(1/\beta_1) - (1/\beta_2)]$. Evaluate V_{OS} for $\beta_1 = 100$ and $\beta_2 = 200$. Assume the differential source resistance to be zero.

8.78 Two possible differential amplifier designs are considered, one using BJTs and the other MOSFETs. In both cases, the collector (drain) resistors are maintained within ±2 % of nominal value. The MOSFETs are operated at $V_{OV} = 300$ mV. What input offset voltage results in each case? What does the MOS V_{OS} become if the devices are increased in width by a factor of 4?

***8.79** A differential amplifier uses two transistors having V_A values of 100 V and 300 V. If everything else is matched, find the resulting input offset voltage. Assume that the two transistors are intended to be biased at a V_{CE} of about 10 V.

***8.80** A differential amplifier is fed in a balanced or push–pull manner, and the source resistance in series with each base is R_s. Show that a mismatch ΔR_s between the values of the two source resistances gives rise to an input offset voltage of approximately $(I/2\beta)\Delta R_s / [1 + (g_m R_s)/\beta]$.

8.81 One approach to "offset correction" involves the adjustment of the values of R_{C1} and R_{C2} so as to reduce the differential output voltage to zero when both input terminals are grounded. This offset-nulling process can be accomplished by utilizing a potentiometer in the collector circuit, as shown in Fig. P8.81. We wish to find the potentiometer setting, represented by the fraction x of its value connected in series with R_{C1}, that is required for nulling the output offset voltage that results from:

(a) R_{C1} being 4% higher than nominal and R_{C2} 4% lower than nominal
(b) Q_1 having an area 20% larger than that of Q_2

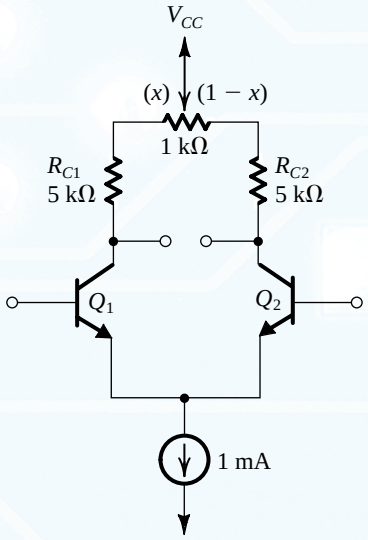


Figure P8.81

8.82 A differential amplifier for which the total emitter bias current is 500 μA uses transistors for which β is specified to lie between 80 and 200. What is the largest possible input bias current? The smallest possible input bias current? The largest possible input offset current?

****8.83** In a particular BJT differential amplifier, a production error results in one of the transistors having an emitter–base junction area twice that of the other. With both inputs grounded, find the current in each of the two transistors and hence the dc offset voltage at the output, assuming that the collector resistances are equal. Use small-signal analysis to find the input voltage that would restore current balance to the differential pair. Repeat using large-signal analysis and compare results.

D 8.84 A large fraction of mass-produced differential-amplifier modules employing 20-kΩ collector resistors is found to have an input offset voltage ranging from +3 mV to −3 mV. By what amount must one collector resistor be adjusted to reduce the input offset to zero? If an adjustment mechanism is devised that raises one collector resistor while correspondingly lowering the other, what resistance change is needed? If a potentiometer connected as shown in Fig. P8.81 is used, what value of potentiometer resistance (specified to 1 significant digit) is needed?

Section 8.5: The Differential Amplifier with Active Load

D 8.85 In an active-loaded differential amplifier of the form shown in Fig. 8.32(a), all transistors are characterized by $k'W/L = 3.2$ mA/V^2, and $|V_A| = 20$ V. Find the bias current I for which the gain $v_o/v_{id} = 100$ V/V.

SIM **D 8.86** It is required to design the active-loaded differential MOS amplifier of Fig. 8.32 to obtain a differential gain of 50 V/V. The technology available provides $\mu_n C_{ox} = 4\mu_p C_{ox} = 400$ μA/V^2, $|V_t| = 0.5$ V, and $|V_A'| = 20$ V/μm and operates from ±1 V supplies. Use a bias current $I = 200$ μA and operate all devices at $|V_{OV}| = 0.2$ V.

(a) Find the W/L ratios of the four transistors.
(b) Specify the channel length required of all transistors.
(c) If $V_{CM} = 0$, what is the allowable range of v_O?
(d) If I is delivered by a simple NMOS current source operated at the same V_{OV} and having the same channel length as the other four transistors, determine the CMRR obtained.

8.87 Consider the active-loaded MOS differential amplifier of Fig. 8.32(a) in two cases:

(a) Current source I is implemented with a simple current mirror.

(b) Current source I is implemented with the modified Wilson current mirror shown in Fig. P8.87.

Recalling that for the simple mirror $R_{SS} = r_o|_{Q_5}$ and for the Wilson mirror $R_{SS} \simeq g_{m7} r_{o7} r_{o5}$, and assuming that all transistors have the same $|V_A|$ and $k'W/L$, show that for case (a)

$$\text{CMRR} = 2\left(\frac{V_A}{V_{OV}}\right)^2$$

and for case (b)

$$\text{CMRR} = 2\sqrt{2}\left(\frac{V_A}{V_{OV}}\right)^3$$

where V_{OV} is the overdrive voltage that corresponds to a drain current of $I/2$. For $k'W/L = 10$ mA/V^2, $I = 1$ mA, and $|V_A| = 10$ V, find CMRR for both cases.

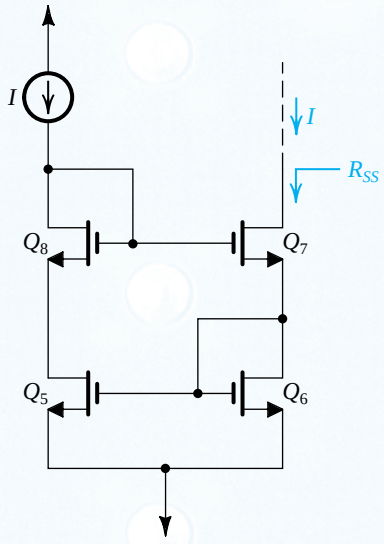


Figure P8.87

D 8.88 Consider an active-loaded differential amplifier such as that shown in Fig. 8.32(a) with the bias current source implemented with the modified Wilson mirror of Fig. P8.87 with $I = 200$ μA. The transistors have $|V_t| = 0.5$ V and $k'W/L = 5$ mA/V^2. What is the lowest value of the total power supply ($V_{DD} + V_{SS}$) that allows each transistor to operate with $|V_{DS}| \geq |V_{GS}|$?

***8.89** (a) Sketch the circuit of an active-loaded MOS differential amplifier in which the input transistors are cascoded and a cascode current mirror is used for the load.
(b) Show that if all transistors are operated at an overdrive voltage V_{OV} and have equal Early voltages $|V_A|$, the gain is given by

$$A_d = 2(V_A/V_{OV})^2$$

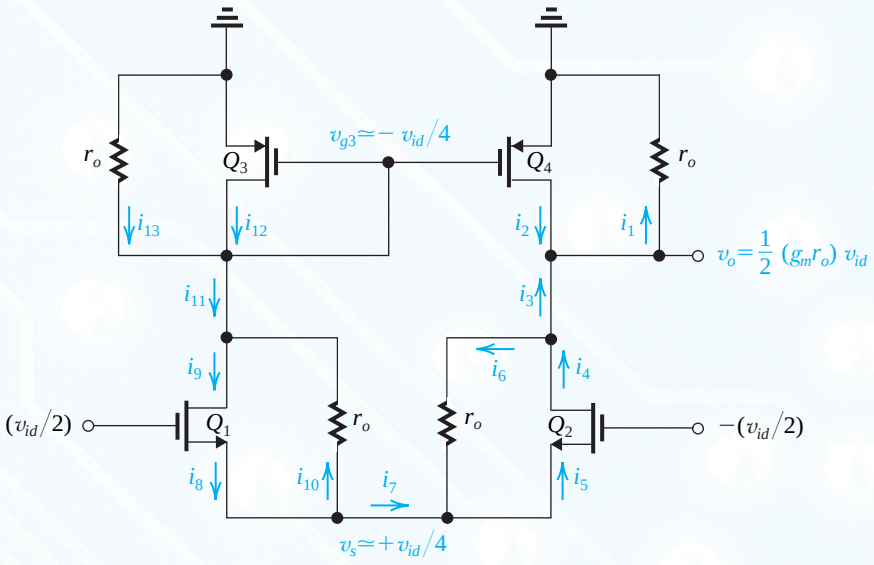


Figure P8.90

Evaluate the gain for $V_{OV} = 0.25$ V and $V_A = 20$ V.

8.90 Figure P8.90 shows the active-loaded MOS differential amplifier prepared for small-signal analysis. To help the reader we have already indicated approximate values for some of the node voltages. For instance, the output voltage $v_o = \frac{1}{2}(g_m r_o) v_{id}$, which we have derived in the text. The voltage at the common sources has been found to be approximately $+v_{id}/4$, which is very far from the virtual ground one might assume. Also, the voltage at the gate of the mirror is approximately $-v_{id}/4$, confirming our contention that the voltage there is vastly different from the output voltage, hence the lack of balance in the circuit and the unavailability of a differential half-circuit. Find the currents labeled i_1 to i_{13}. Determine their values in the sequence of their numbering and reflect on the results. You will find that there is some inconsistency, which is a result of the approximations we have made. Note that all transistors are assumed to be operating at the same $|V_{OV}|$.

8.91 An active-loaded NMOS differential amplifier operates with a bias current I of 100 μA. The NMOS transistors are operated at $V_{OV} = 0.2$ V and the PMOS devices at $|V_{OV}| = 0.3$ V. The Early voltages are 20 V for the NMOS and 12 V for the PMOS transistors. Find G_m, R_o, and A_d. For what value of load resistance is the gain reduced by a factor of 2?

8.92 This problem investigates the effect of transistor mismatches on the input offset voltage of the active-loaded MOS differential amplifier of Fig. 8.32(a). For this purpose, ground both input terminals and short-circuit the output node to ground.

(a) If the amplifying transistors Q_1 and Q_2 exhibit a W/L mismatch of $\Delta(W/L)_A$, find the resulting short-circuit output current and hence show that the corresponding V_{OS} is given by

$$V_{OS1} = (V_{OV}/2)\,\frac{\Delta(W/L)_A}{(W/L)_A}$$

where V_{OV} is the overdrive voltage at which Q_1 and Q_2 are operating.

(b) Repeat for a mismatch $\Delta(W/L)_M$ in the W/L ratios of the mirror transistor Q_3 and Q_4 to show that the corresponding V_{OS} is given by

$$V_{OS2} = (V_{OV}/2)\,\frac{\Delta(W/L)_M}{(W/L)_M}$$

where V_{OV} is the overdrive voltage at which Q_1 and Q_2 are operating.

(c) For a circuit in which all transistors are operated at $|V_{OV}| = 0.2$ V and all W/L ratios are accurate to within ±1 % of nominal, find the worst-case total offset voltage V_{OS}.

8.93 The differential amplifier in Fig. 8.37(a) is operated with $I = 400$ μA, with devices for which $V_A = 16$ V and $\beta = 100$. What differential input resistance, output resistance, equivalent transconductance, and open-circuit voltage gain would you expect? What will the voltage gain be if the input resistance of the subsequent stage is equal to R_{id} of this stage?

D ***8.94** Design the circuit of Fig. 8.37(a) using a basic current mirror to implement the current source I. It is required that the equivalent transconductance be 4 mA/V. Use ±5-V power supplies and BJTs that have $\beta = 125$ and $V_A = 100$ V. Give the complete circuit with component values and specify the differential input resistance R_{id}, the output resistance R_o, the open-circuit voltage gain A_d, the input bias current, the input common-mode range, the common-mode gain, and the CMRR.

D ***8.95** Repeat the design of the amplifier specified in Problem 8.94 utilizing a Widlar current source [Fig. 7.36] to supply the bias current. Assume that the largest resistance available is 2 kΩ.

D **8.96** Modify the design of the amplifier in Problem 8.94 by connecting emitter-degeneration resistances of values that result in $R_{id} = 125$ kΩ. What does A_d become?

8.97 An active-loaded bipolar differential amplifier such as that shown in Fig. 8.37(a) has $I = 0.5$ mA, $V_A = 30$ V, and $\beta = 150$. Find G_m, R_o, A_d, and R_{id}. If the bias-current source is implemented with a simple *npn* current mirror, find R_{EE}, A_{cm}, and CMRR. If the amplifier is fed differentially with a source having a total of 20 kΩ resistance (i.e., 10 kΩ in series with the base lead of each of Q_1 and Q_2), find the overall differential voltage gain.

***8.98** This problem provides a general approach to the determination of the common-mode gain of the active-loaded differential amplifier of either type (MOS and BJT). The method is illustrated in Fig. P8.98, in which we have replaced each of Q_1 and Q_2 together with their source (emitter) resistances $2R_{SS}$ $(2R_{EE})$ with a controlled source $G_{mcm}v_{icm}$ and an output resistance $R_{o1,2}$. For the MOS case, $G_{mcm} = v_{icm}/2R_{SS}$; $v_{icm}/2R_{EE}$ for the bipolar case. Usually R_{o1} and R_{o2} are much larger than the resistances at the respective nodes and can be neglected. The current mirror has been replaced by an equivalent circuit consisting of an input resistance R_{in}, a controlled source with current gain A_m, and an output resistance R_{om}.

(a) Show that the common-mode gain is given approximately by

$$A_{cm} \equiv \frac{v_o}{v_{icm}} \simeq G_{mcm}R_{om}(A_m - 1)$$

(b) For the simple MOS mirror consisting of Q_3 and Q_4, as in Fig. 8.32(a), show that

$$A_m = 1 \Big/ \left[1 + \frac{1}{g_{m3}r_{o3}}\right]$$

and hence derive the expression for the common-mode gain A_{cm} given in Eq. (8.146).

(c) For the simple bipolar mirror consisting of Q_3 and Q_4, as in Fig. 8.37(a), show that

$$A_m = 1 \Big/ \left(1 + \frac{2}{\beta_P}\right)$$

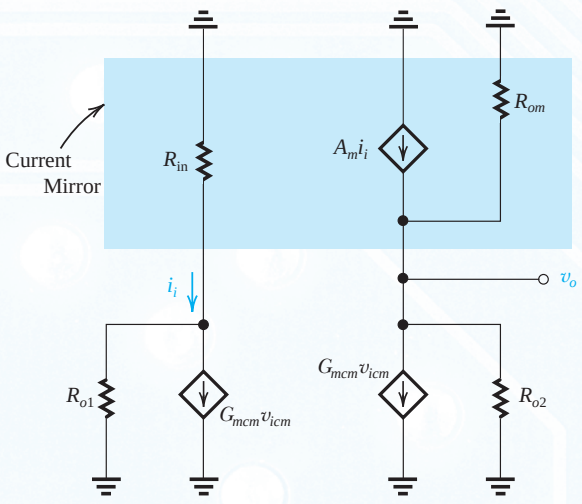


Figure P8.98

and hence derive the expression for the CM gain A_{cm} given in Eq. (8.165).

8.99 For the active-loaded MOS differential pair, replacing the simple current-mirror load by the Wilson mirror of Fig. 7.35(a), find the CM gain. [*Hint*: Use the general formula in Problem 8.98, namely,

$$|A_{cm}| = \frac{R_{om}}{2R_{EE}}(A_m - 1)$$

where R_{om} is the output resistance of the mirror and A_m is its current transfer ratio. Note, however, that this formula will overestimate $|A_{cm}|$ because we are neglecting R_{o2}.]

8.100 For the active-loaded bipolar differential pair, replacing the simple current-mirror load by the base-current-compensated mirror of Fig. 7.33, find the expected systematic input offset voltage. Evaluate V_{OS} for $\beta_P = 50$.

8.101 For the active-loaded bipolar differential pair, replacing the simple current-mirror load by the Wilson mirror of Fig. 7.34(a), find the expected systematic input offset voltage. Evaluate V_{OS} for $\beta_P = 50$.

8.102 Figure P8.102 shows a differential cascode amplifier with an active load formed by a Wilson current mirror. Utilizing the expressions derived in Chapter 7 for the output resistance of a bipolar cascode and the output resistance of the Wilson mirror, and assuming all transistors to be identical, show that the differential voltage gain A_d is given approximately by

$$A_d = \tfrac{1}{3}\beta g_m r_o$$

Evaluate A_d for the case of $\beta = 100$ and $V_A = 30$ V.

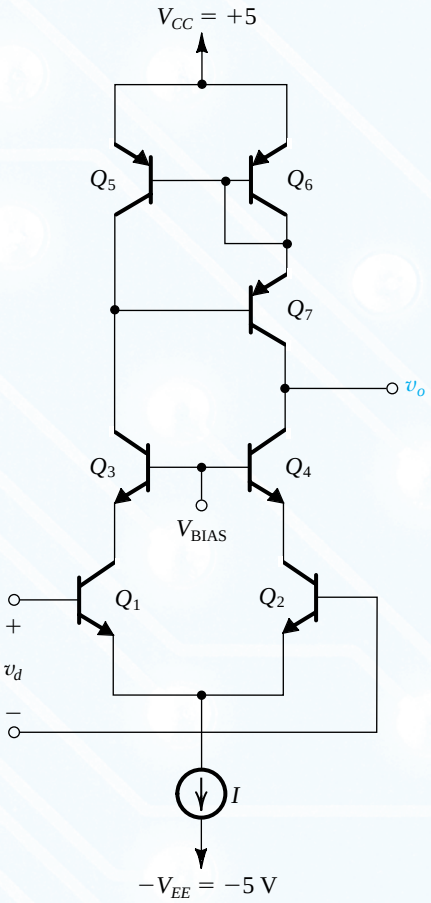


Figure P8.102

D 8.103 Consider the bias design of the Wilson-loaded cascode differential amplifier shown in Fig. P8.102.

(a) What is the largest signal voltage possible at the output without Q_7 saturating? Assume that the CB junction conducts when the voltage across it exceeds 0.4 V.
(b) What should the dc bias voltage established at the output (by an arrangement not shown) be in order to allow for positive output signal swing of 1.5 V?
(c) What should the value of V_{BIAS} be in order to allow for a negative output signal swing of 1.5 V?
(d) What is the upper limit on the input common-mode voltage v_{CM}?

**8.104 Figure P8.104 shows a modified cascode differential amplifier. Here Q_3 and Q_4 are the cascode transistors. However, the manner in which Q_3 is connected with its base current feeding the current mirror Q_7–Q_8 results in very interesting input properties. Note that for simplicity the circuit is shown with the base of Q_2 grounded.

(a) With $v_I = 0$ V dc, find the input bias current I_B assuming all transistors have equal value of β. Compare the case without the Q_7–Q_8 connection.
(b) With $v_I = 0$ V (dc) + v_{id}, find the input signal current i_i and hence the input differential resistance R_{id}. Compare with the case without the Q_7–Q_8 connection. By what factor does R_{id} increase?

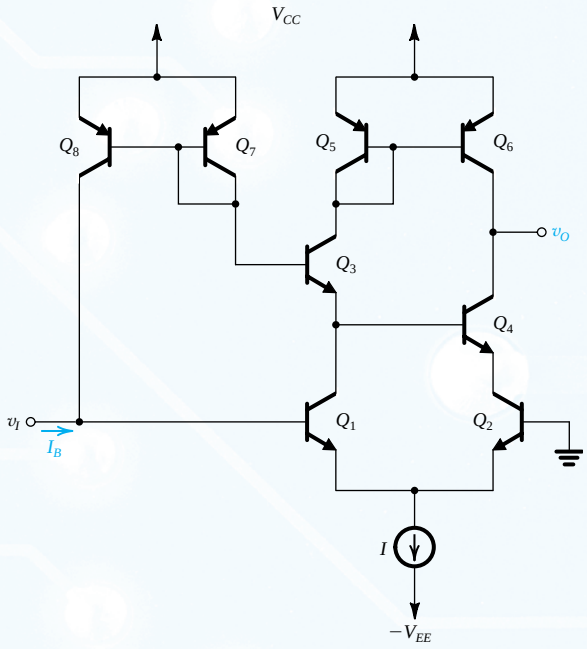


Figure P8.104

8.105 For the folded-cascode differential amplifier of Fig. 8.40, find the value of V_{BIAS} that results in the largest possible positive output swing, while keeping Q_3, Q_4, and the *pnp* transistors that realize the current sources out of saturation. Assume $V_{CC} = V_{EE} = 5$ V. If the dc level at the output is 0 V, find the maximum allowable output signal swing. For I = 0.4 mA, $\beta_P = 50$, $\beta_N = 150$, and $V_A = 120$ V find G_m, R_{o4}, R_{o5}, R_o, and A_d.

8.106 For the BiCMOS differential amplifier in Fig. P8.106 let $V_{DD} = V_{SS} = 3$ V, $I = 0.4$ mA, $k_p'W/L$ = 6.4 mA/V^2; $|V_A|$ for *p*-channel MOSFETs is 10 V, $|V_A|$ for *npn* transistors is 30 V. Find G_m, R_o, and A_d.

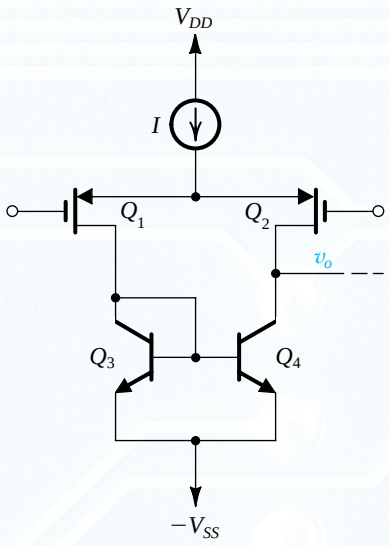


Figure P8.106

Section 8.6: Multistage Amplifiers

8.107 Consider the circuit in Fig. 8.41 with the device geometries (in μm) shown in the Table P8.107. Let I_{REF} = 225 μA, $|V_t|$ = 0.75 V for all devices, $\mu_n C_{ox}$ = 180 μA/V², $\mu_p C_{ox}$ = 60 μA/V², $|V_A|$ = 9 V for all devices, $V_{DD} = V_{SS}$ = 1.5 V. Determine the width of Q_6, W, that will ensure that the op amp will not have a systematic offset voltage. Then, for all devices evaluate I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, and r_o. Provide your results in a table similar to Table 8.1. Also find A_1, A_2, the open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on the bias current.

D ***8.108** The two-stage CMOS op amp in Fig. P8.108 is fabricated in a 0.18-μm technology having $k_n' = 4k_p' = 400$ μA/V², $V_{tn} = -V_{tp} = 0.4$ V.

(a) With A and B grounded, perform a dc design that will result in each of Q_1, Q_2, Q_3, and Q_4 conducting a drain current of 200 μA. Design so that all transistors operate at 0.2 V-overdrive voltages. Specify the W/L ratio required for each MOSFET. Present your results in tabular form. What is the dc voltage at the output (ideally)?
(b) Find the input common-mode range.
(c) Find the allowable range of the output voltage.
(s) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 5 V.

D ***8.109** In a particular design of the CMOS op amp of Fig. 8.41 the designer wishes to investigate the effects of increasing the W/L ratio of both Q_1 and Q_2 by a factor of 4. Assuming that all other parameters are kept unchanged, refer to Example 8.5 to help you answer the following questions:

(a) Find the resulting change in $|V_{OV}|$ and in g_m of Q_1 and Q_2.
(b) What change results in the voltage gain of the input stage? In the overall voltage gain?
(c) What is the effect on the input offset voltages? (You might wish to refer to Section 8.4).

8.110 Consider the amplifier of Fig. 8.41, whose parameters are specified in Example 8.5. If a manufacturing error results in the W/L ratio of Q_7 being 50/0.8, find the current that Q_7 will now conduct. Thus find the systematic offset voltage that will appear at the output. (Use the results of Example 8.5.) Assuming that the open-loop gain will remain approximately unchanged from the value found in Example 8.5, find the corresponding value of input offset voltage, V_{OS}.

8.111 Consider the input stage of the CMOS op amp in Fig. 8.41 with both inputs grounded. Assume that the two sides of the input stage are perfectly matched except that the threshold voltages of Q_3 and Q_4 have a mismatch ΔV_t. Show that a current $g_{m3}\Delta V_t$ appears at the output of the first stage. What is the corresponding input offset voltage?

***8.112** Figure P8.112 shows a bipolar op-amp circuit that resembles the CMOS op amp of Fig. 8.41. Here, the input differential pair Q_1–Q_2 is loaded in a current mirror formed by Q_3 and Q_4. The second stage is formed by the current-source-loaded common-emitter transistor Q_5. Unlike the CMOS circuit, here there is an output stage formed by the emitter follower Q_6. The function of capacitor C_C will be explained later in Chapter 10. All transistors have $\beta = 100$, $|V_{BE}| = 0.7$ V, and $r_o = \infty$.

(a) For inputs grounded and output held at 0 V (by negative feedback, not shown) find the emitter currents of all transistors.
(b) Calculate the gain of the amplifier with $R_L = 10$ kΩ.

Table P8.107

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5

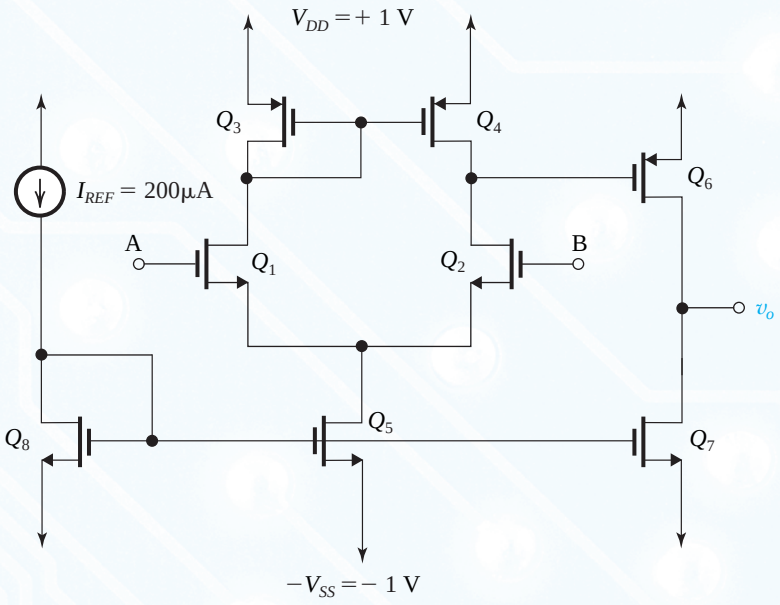


Figure P8.108

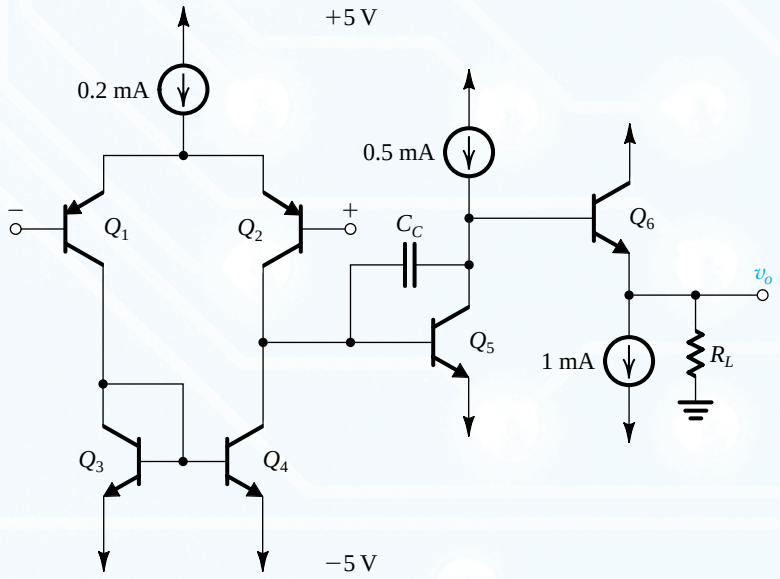


Figure P8.112

D 8.113 It is required to design the circuit of Fig. 8.42 to provide a bias current I_B of 225 μA with Q_8 and Q_9 as matched devices having $W/L = 60/0.5$. Transistors Q_{10}, Q_{11}, and Q_{13} are to be identical and must have the same g_m as Q_8 and Q_9. Transistor Q_{12} is to be four times as wide as Q_{13}. Let $k_n' = 3k_p' = 180\ \mu A/V^2$, and $V_{DD} = V_{SS} = 1.5$ V. Find the required value of R_B. What is the voltage drop across R_B? Also specify the W/L ratios of Q_{10}, Q_{11}, Q_{12}, and Q_{13} and give the expected dc voltages at the gates of Q_{12}, Q_{10}, and Q_8.

8.114 A BJT differential amplifier, biased to have $r_e = 100\ \Omega$ and utilizing two 100-Ω emitter resistors and 5-kΩ loads, drives a second differential stage biased to have $r_e = 50\ \Omega$. All BJTs have $\beta = 100$. What is the voltage gain of the first stage? Also find the input resistance of the first stage, and

the current gain from the input of the first stage to the collectors of the second stage.

8.115 In the multistage amplifier of Fig. 8.43, emitter resistors are to be introduced—100 Ω in the emitter lead of each of the first-stage transistors and 25 Ω for each of the second-stage transistors. What is the effect on input resistance, the voltage gain of the first stage, and the overall voltage gain? Use the bias values found in Example 8.6.

D 8.116 Consider the circuit of Fig. 8.43 and its output resistance. Which resistor has the most effect on the output resistance? What should this resistor be changed to if the output resistance is to be reduced by a factor of 2? What will the amplifier gain become after this change? What other change can you make to restore the amplifier gain to approximately its prior value?

D 8.117 (a) If, in the multistage amplifier of Fig. 8.43, the resistor R_5 is replaced by a constant-current source $\simeq 1$ mA, such that the bias situation is essentially unaffected, what does the overall voltage gain of the amplifier become? Assume that the output resistance of the current source is very high. Use the results of Example 8.7.
(b) With the modification suggested in (a), what is the effect of the change on output resistance? What is the overall gain of the amplifier when loaded by 100 Ω to ground? The original amplifier (before modification) has an output resistance of 152 Ω and a voltage gain of 8513 V/V. What is its gain when loaded by 100 Ω? Comment. Use $\beta = 100$.

***8.118** Figure P8.118 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.

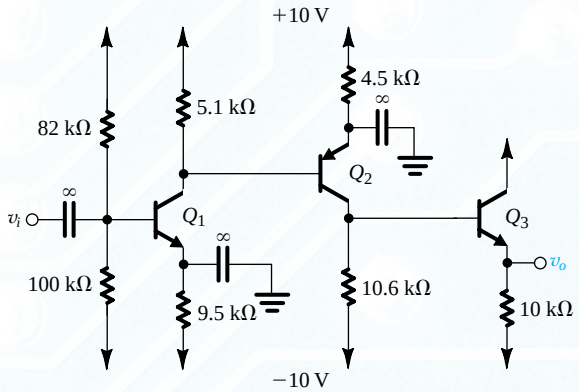


Figure P8.118

(a) Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume $|V_{BE}| = 0.7$ V, $\beta = 100$, and neglect the Early effect.
(b) Find the input resistance and the output resistance.
(c) Use the current-gain method to evaluate the voltage gain v_o/v_i.

****8.119** The MOS differential amplifier shown in Fig. P8.119 utilizes three current mirrors for signal transmission: $Q_4 - Q_6$ has a transmission factor of 2 [i.e., $(W/L)_6/(W/L)_4 = 2$], $Q_3 - Q_5$ has a transmission factor of 1, and $Q_7 - Q_8$ has a transmission factor of 2. All transistors are sized to operate at the same overdrive voltage, $|V_{OV}|$. All transistors have the same Early voltage $|V_A|$.

(a) Provide in tabular form the values of I_D, g_m, and r_o of each of the eight transistors in terms of I, V_{OV}, and V_A.
(b) Show that the differential voltage gain A_d is given by

$$A_d = 2g_{m1}(r_{o6} \| r_{o8}) = V_A/V_{OV}$$

(c) Show that the CM gain is given by

$$|A_{cm}| \simeq \frac{r_{o6} \| r_{o8}}{R_{SS}} \frac{1}{g_{m7} r_{o7}}$$

where R_{SS} is the output resistance of the bias current source I. [*Hint*: Replace each of Q_1 and Q_2 together with their source resistance $2R_{SS}$ with a controlled current-source $v_{icm}/2R_{SS}$ and an output resistance. For each current mirror, the current transfer ratio is given by

$$A_i \simeq A_i \text{ (ideal)} \left(1 - \frac{1}{g_m r_o}\right)$$

where g_m and r_o are the parameters of the input transistor of the mirror.]

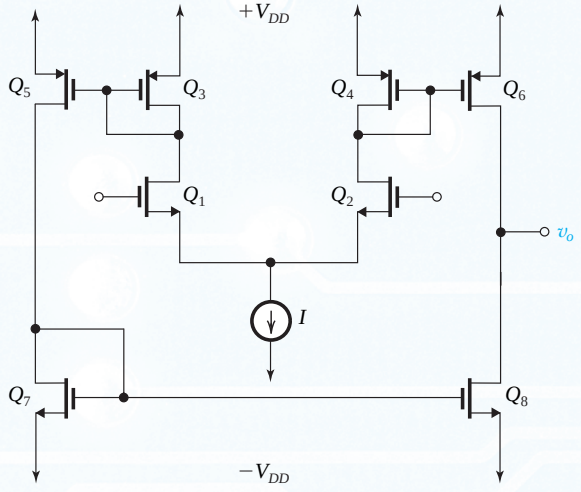


Figure P8.119

(d) If the current-source I is implemented using a simple mirror and the MOS transistor is operated at the same V_{OV}, show that the CMRR is given by

$$\text{CMRR} = 4(V_A/V_{OV})^2$$

(e) Find the input CM range and the output linear range in terms of V_{DD}, $|V_t|$ and $|V_{OV}|$.

D ***8.120** For the circuit shown in Fig. P8.120, which uses a folded cascode involving transistor Q_3, all transistors have $|V_{BE}| = 0.7$ V for the currents involved, $V_A = 200$ V, and $\beta = 100$. The circuit is relatively conventional except for Q_5, which operates in a Class B mode (we will study this in Chapter 11) to provide an increased negative output swing for low-resistance loads.

(a) Perform a bias calculation assuming $|V_{BE}| = 0.7$ V, high β, $V_A = \infty$, $v_+ = v_- = 0$ V, and v_O is stabilized by feedback to about 0 V. Find R so that the reference current I_{REF} is 100 μA. What are the voltages at all the labeled nodes?
(b) Provide in tabular form the bias currents in all transistors together with g_m and r_o for the signal transistors (Q_1, Q_2, Q_3, Q_4, and Q_5) and r_o for Q_C, Q_D, and Q_G.
(c) Now, using $\beta = 100$, find the voltage gain $v_o/(v_+ - v_-)$, and in the process, verify the polarity of the input terminals.
(d) Find the input and output resistances.
(e) Find the input common-mode range for linear operation.
(f) For no load, what is the range of available output voltages, assuming $|V_{CE\,sat}| = 0.3$ V?
(g) Now consider the situation with a load resistance connected from the output to ground. At the positive and negative limits of the output signal swing, find the smallest load resistance that can be driven if one or the other of Q_1 or Q_2 is allowed to cut off.

D ***8.121** In the CMOS op amp shown in Fig. P8.121, all MOS devices have $|V_t| = 1$ V, $\mu_n C_{ox} = 2\mu_p C_{ox} = 40$ μA/V^2, $|V_A| = 50$ V, and $L = 5$ μm. Device widths are indicated on the diagram as multiples of W, where $W = 5$ μm.

(a) Design R to provide a 10-μA reference current.
(b) Assuming $v_O = 0$ V, as established by external feedback, perform a bias analysis, finding all the labeled node voltages, V_{GS} and I_D for all transistors.
(c) Provide in table form I_D, V_{GS}, g_m, and r_o for all devices.
(d) Calculate the voltage gain $v_o/(v_+ - v_-)$, the input resistance, and the output resistance.
(e) What is the input common-mode range?
(f) What is the output signal range for no load?
(g) For what load resistance connected to ground is the output negative voltage limited to −1 V before Q_7 begins to conduct?
(h) For a load resistance one-tenth of that found in (g), what is the output signal swing?

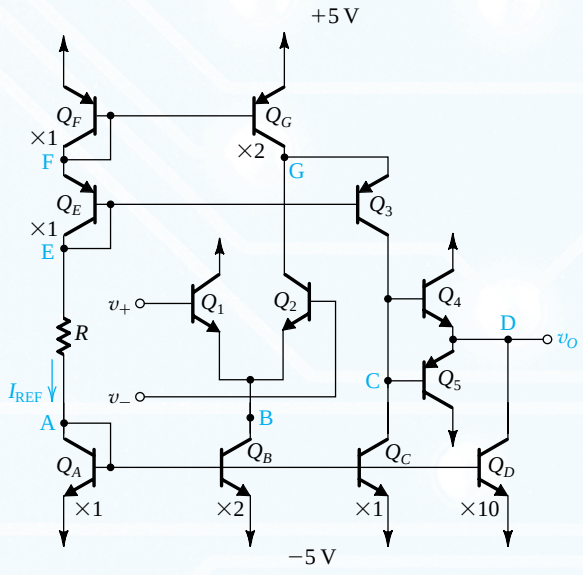


Figure P8.120

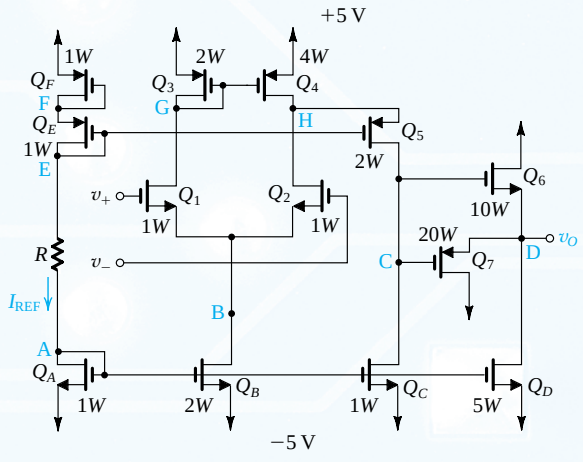


Figure P8.121