

CHAPTER 11

Output Stages and Power Amplifiers

Introduction 911

11.1 Classification of Output Stages 912

11.2 Class A Output Stage 913

11.3 Class B Output Stage 918

11.4 Class AB Output Stage 924

11.5 Biasing the Class AB Circuit 929

11.6 CMOS Class AB Output Stages 933

11.7 Power BJTs 943

11.8 Variations on the Class AB Configuration 950

11.9 IC Power Amplifiers 955

11.10 MOS Power Transistors 962

Summary 967

Problems 968

IN THIS CHAPTER YOU WILL LEARN

1. The classification of amplifier output stages on the basis of the fraction of the cycle of an input sine wave during which the transistor conducts.
2. Analysis and design of a variety of output-stage types ranging from the simple but power-inefficient emitter follower (class A) to the popular push-pull class AB circuit in both bipolar and CMOS technologies.
3. Thermal considerations in the design and fabrication of high-output-power circuits.
4. Useful and interesting circuit techniques employed in the design of power amplifiers.
5. Special types of MOS transistors optimized for high-power applications.

Introduction

An important function of the output stage is to provide the amplifier with a low output resistance so that it can deliver the output signal to the load without loss of gain. Since the output stage is the final stage of the amplifier, it usually deals with relatively large signals. Thus the small-signal approximations and models either are not applicable or must be used with care. Nevertheless, linearity remains a very important requirement. In fact, a measure of goodness of the output stage is the **total harmonic distortion** (THD) it introduces. This is the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms of the fundamental. A high-fidelity audio power amplifier features a THD of the order of a fraction of a percent.

The most challenging requirement in the design of an output stage is for it to deliver the required amount of power to the load in an *efficient* manner. This implies that the power *dissipated* in the output-stage transistors must be as low as possible. This requirement stems mainly from the fact that the power dissipated in a transistor raises its internal **junction temperature**, and there is a maximum temperature (in the range of 150°C to 200°C for silicon devices) above which the transistor is destroyed. A high power-conversion efficiency also may be required to prolong the life of batteries employed in battery-powered circuits, to permit a smaller, lower-cost power supply, or to obviate the need for cooling fans.

We begin this chapter with a study of the various output-stage configurations employed in amplifiers that handle both low and high power. In this context, “high power” generally means greater than 1 W. We then consider the specific requirements of BJTs employed in the design of high-power output stages, called **power transistors**. Special attention will be paid to the thermal properties of such transistors.

A power amplifier is simply an amplifier with a high-power output stage. Examples of discrete- and integrated-circuit power amplifiers will be presented. Since BJTs can handle much larger currents than MOSFETs, they are preferred in the design of output stages. Nevertheless, some interesting CMOS output stages are also studied.

11.1 Classification of Output Stages

Output stages are classified according to the collector current waveform that results when an input signal is applied. Figure 11.1 illustrates the classification for the case of a sinusoidal input signal. The class A stage, whose associated waveform is shown in Fig. 11.1(a), is biased at a current I_C greater than the amplitude of the signal current, \hat{I}_c . Thus the transistor in a class A stage conducts for the entire cycle of the input signal; that is, the conduction angle is 360° . In contrast, the class B stage, whose associated waveform is shown in Fig. 11.1(b), is biased at zero dc current. Thus a transistor in a class B stage conducts for only half the cycle of the input sine wave, resulting in a conduction angle of 180° . As will be seen later,

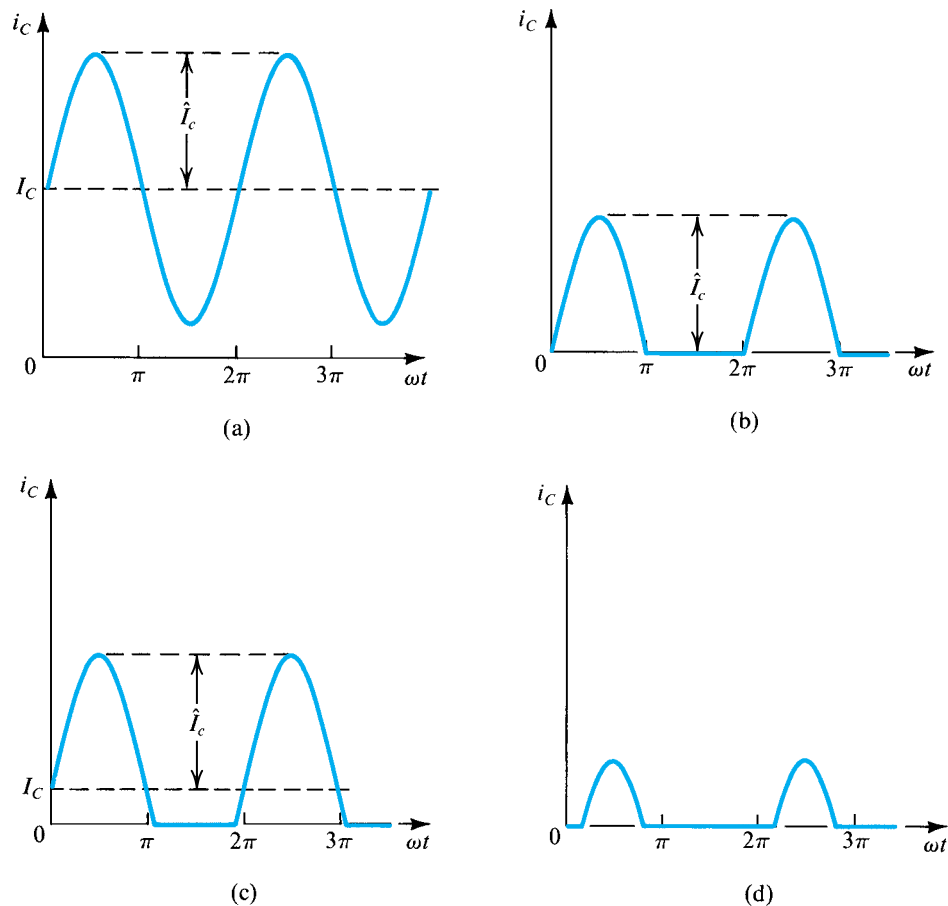


Figure 11.1 Collector current waveforms for transistors operating in (a) class A, (b) class B, (c) class AB, and (d) class C amplifier stages.

the negative halves of the sinusoid will be supplied by another transistor that also operates in the class B mode and conducts during the alternate half-cycles.

An intermediate class between A and B, appropriately named class AB, involves biasing the transistor at a nonzero dc current much smaller than the peak current of the sine-wave signal. As a result, the transistor conducts for an interval slightly greater than half a cycle, as illustrated in Fig. 11.1(c). The resulting conduction angle is greater than 180° but much less than 360° . The class AB stage has another transistor that conducts for an interval slightly greater than that of the negative half-cycle, and the currents from the two transistors are combined in the load. It follows that, during the intervals near the zero crossings of the input sinusoid, both transistors conduct.

Figure 11.1(d) shows the collector-current waveform for a transistor operated as a class C amplifier. Observe that the transistor conducts for an interval shorter than that of a half-cycle; that is, the conduction angle is less than 180° . The result is the periodically pulsating current waveform shown. To obtain a sinusoidal output voltage, this current is passed through a parallel LC circuit, tuned to the frequency of the input sinusoid. The tuned circuit acts as a bandpass filter (Chapter 16) and provides an output voltage proportional to the amplitude of the fundamental component in the Fourier-series representation of the current waveform.

Class A, AB, and B amplifiers are studied in this chapter. They are employed as output stages of op amps and audio power amplifiers. In the latter application, class AB is the preferred choice, for reasons that will be explained in the sections to follow. Class C amplifiers are usually employed for radio-frequency (RF) power amplification (required, e.g., in mobile phones and radio and TV transmitters). The design of class C amplifiers is a rather specialized topic and is not included in this book. However, we should point out that the tuned-resonator oscillator circuits described in Chapter 17 operate inherently in the class C mode.

Although the BJT has been used to illustrate the definition of the various output-stage classes, the same classification applies to output stages implemented with MOSFETs. Furthermore, the classification above extends to amplifier stages other than those used at the output. In this regard, all the common-emitter, common-base, and common-collector amplifiers (and their FET counterparts) studied in earlier chapters fall into the class A category.

11.2 Class A Output Stage

Because of its low output resistance, the emitter follower is the most popular class A output stage. We have already studied the emitter follower in Chapter 6; in the following we consider its large-signal operation.

11.2.1 Transfer Characteristic

Figure 11.2 shows an emitter follower Q_1 biased with a constant current I supplied by transistor Q_2 . Since the emitter current $i_{E1} = I + i_L$, the bias current I must be greater than the largest negative load current; otherwise, Q_1 cuts off and class A operation will no longer be maintained.

The transfer characteristic of the emitter follower of Fig. 11.2 is described by

$$v_O = v_I - v_{BE1} \quad (11.1)$$

where v_{BE1} depends on the emitter current i_{E1} and thus on the load current i_L . If we neglect the relatively small changes in v_{BE1} (60 mV for every factor-of-10 change in emitter current), the

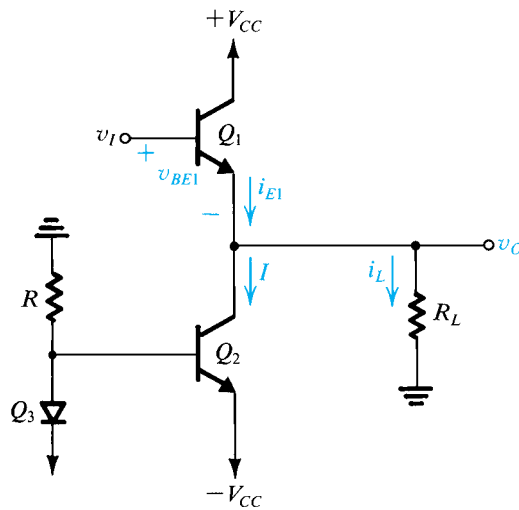


Figure 11.2 An emitter follower (Q_1) biased with a constant current I supplied by transistor Q_2 .

linear transfer curve shown in Fig. 11.3 results. As indicated, the positive limit of the linear region is determined by the saturation of Q_1 ; thus

$$\text{I} \quad v_{O\max} = V_{CC} - V_{CE1\text{sat}} \quad (11.2)$$

In the negative direction, depending on the values of I and R_L , the limit of the linear region is determined either by Q_1 turning off,

$$\text{I} \quad v_{O\min} = -IR_L \quad (11.3)$$

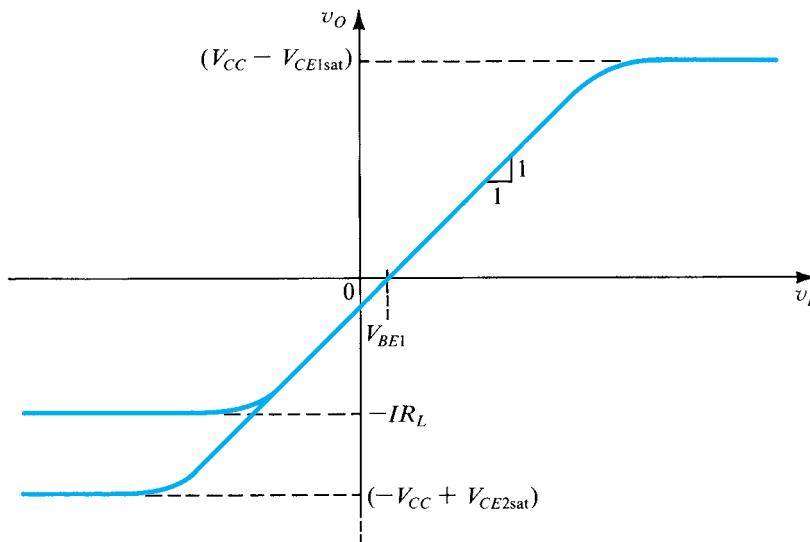


Figure 11.3 Transfer characteristic of the emitter follower in Fig. 11.2. This linear characteristic is obtained by neglecting the change in v_{BE1} with i_L . The maximum positive output is determined by the saturation of Q_1 . In the negative direction, the limit of the linear region is determined either by Q_1 turning off or by Q_2 saturating, depending on the values of I and R_L .

or by Q_2 saturating,

$$v_{O\min} = -V_{CC} + V_{CE2\text{sat}} \quad (11.4) \quad \text{!}$$

The absolutely lowest (most negative) output voltage is that given by Eq. (11.4) and is achieved provided the bias current I is greater than the magnitude of the corresponding load current,

$$I \geq \frac{|-V_{CC} + V_{CE2\text{sat}}|}{R_L} \quad (11.5) \quad \text{!}$$

EXERCISES

D11.1 For the emitter follower in Fig. 11.2, $V_{CC} = 15$ V, $V_{CE\text{sat}} = 0.2$ V, $V_{BE} = 0.7$ V and constant, and β is very high. Find the value of R that will establish a bias current sufficiently large to allow the largest possible output signal swing for $R_L = 1$ k Ω . Determine the resulting output signal swing and the minimum and maximum emitter currents for Q_1 .

Ans. 0.97 k Ω ; -14.8 V to $+14.8$ V; 0 to 29.6 mA

11.2 For the emitter follower of Exercise 11.1, in which $I = 14.8$ mA, consider the case in which v_o is limited to the range -10 V to $+10$ V. Let Q_1 have $v_{BE} = 0.6$ V at $i_C = 1$ mA, and assume $\alpha \approx 1$. Find v_i corresponding to $v_o = -10$ V, 0 V, and $+10$ V. At each of these points, use small-signal analysis to determine the voltage gain v_o/v_i . Note that the incremental voltage gain gives the slope of the v_o -versus- v_i characteristic.

Ans. -9.36 V, 0.67 V, 10.68 V; 0.995 V/V, 0.998 V/V, 0.999 V/V

11.2.2 Signal Waveforms

Consider the operation of the emitter-follower circuit of Fig. 11.2 for sine-wave input. Neglecting $V_{CE\text{sat}}$, we see that if the bias current I is properly selected, the output voltage can swing from $-V_{CC}$ to $+V_{CC}$ with the quiescent value being zero, as shown in Fig. 11.4(a). Figure 11.4(b) shows the corresponding waveform of $v_{CE1} = V_{CC} - v_o$. Now, assuming that the bias current I is selected to allow a maximum negative load current of V_{CC}/R_L , that is,

$$I = V_{CC}/R_L$$

the collector current of Q_1 will have the waveform shown in Fig. 11.4(c). Finally, Fig. 11.4(d) shows the waveform of the **instantaneous power dissipation** in Q_1 ,

$$p_{D1} \equiv v_{CE1}i_{C1} \quad (11.6)$$

11.2.3 Power Dissipation

Figure 11.4(d) indicates that the maximum instantaneous power dissipation in Q_1 is $V_{CC}I$. This is equal to the power dissipation in Q_1 with no input signal applied, that is, the quiescent power dissipation. Thus the emitter-follower transistor dissipates the largest amount of power when $v_o = 0$. Since this condition (no input signal) can easily prevail for prolonged periods of time, transistor Q_1 must be able to withstand a continuous power dissipation of $V_{CC}I$.

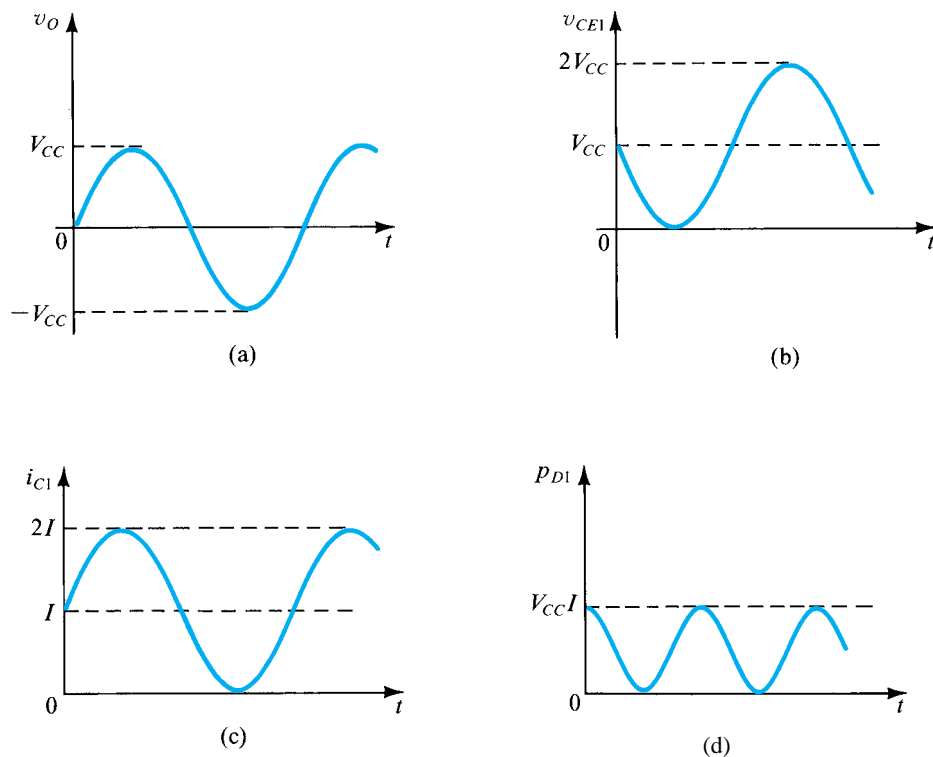


Figure 11.4 Maximum signal waveforms in the class A output stage of Fig. 11.2 under the condition $I = V_{CC}/R_L$ or, equivalently, $R_L = V_{CC}/I$. Note that the transistor saturation voltages have been neglected.

The power dissipation in Q_1 depends on the value of R_L . Consider the extreme case of an output open circuit, that is, $R_L = \infty$. In this case, $i_{C1} = I$ is constant and the instantaneous power dissipation in Q_1 will depend on the instantaneous value of v_O . The maximum power dissipation will occur when $v_O = -V_{CC}$, for in this case v_{CE1} is a maximum of $2V_{CC}$ and $p_{D1} = 2V_{CC}I$. This condition, however, would not normally persist for a prolonged interval, so the design need not be that conservative. Observe that with an open-circuit load, the average power dissipation in Q_1 is $V_{CC}I$. A far more dangerous situation occurs at the other extreme of R_L —specifically, $R_L = 0$. In the event of an output short circuit, a positive input voltage would theoretically result in an infinite load current. In practice, a very large current may flow through Q_1 , and if the short-circuit condition persists, the resulting large power dissipation in Q_1 can raise its junction temperature beyond the specified maximum, causing Q_1 to burn up. To guard against such a situation, output stages are usually equipped with **short-circuit protection**, as will be explained later.

The power dissipation in Q_2 also must be taken into account in designing an emitter-follower output stage. Since Q_2 conducts a constant current I , and the maximum value of v_{CE2} is $2V_{CC}$, the maximum instantaneous power dissipation in Q_2 is $2V_{CC}I$. This maximum, however, occurs when $v_O = V_{CC}$, a condition that would not normally prevail for a prolonged period of time. A more significant quantity for design purposes is the average power dissipation in Q_2 , which is $V_{CC}I$.

Example 11.1

Consider the emitter follower in Fig. 11.2 with $V_{CC} = 10\text{ V}$, $I = 100\text{ mA}$, and $R_L = 100\ \Omega$.

- Find the power dissipated in Q_1 and Q_2 under quiescent conditions ($v_O = 0$).
- For a sinusoidal output voltage of maximum possible amplitude (neglecting $V_{CE\text{sat}}$), find the average power dissipation in Q_1 and Q_2 . Also find the load power.

Solution

- Under quiescent conditions $v_O = 0$, and each of Q_1 and Q_2 conducts a current $I = 100\text{ mA} = 0.1\text{ A}$ and has a voltage $V_{CE} = V_{CC} = 10\text{ V}$, thus

$$P_{D1} = P_{D2} = V_{CC}I = 10 \times 0.1 = 1\text{ W}$$

- For a sinusoidal output voltage of maximum possible amplitude (i.e., 10-V peak), the instantaneous power dissipation in Q_1 will be as shown in Fig. 11.4(d). Thus the average power dissipation in Q_1 will be

$$P_{D1} = \frac{1}{2}V_{CC}I = \frac{1}{2} \times 10 \times 0.1 = 0.5\text{ W}$$

For Q_2 , the current is constant at $I = 0.1\text{ A}$ and the voltage at the collector will have an average value of 0 V. Thus the average voltage across Q_2 will be V_{CC} and the average dissipation will be

$$\begin{aligned} P_{D2} &= I \times v_{CE} \Big|_{\text{average}} \\ &= I \times V_{CC} = 0.1 \times 10 = 1\text{ W} \end{aligned}$$

Finally, the power delivered to the load can be found from

$$\begin{aligned} P_L &= \frac{V_{\text{rms}}^2}{R_L} \\ &= \frac{(10/\sqrt{2})^2}{100} = 0.5\text{ W} \end{aligned}$$

11.2.4 Power-Conversion Efficiency

The power-conversion efficiency of an output stage is defined as

$$\eta \equiv \frac{\text{Load power } (P_L)}{\text{Supply power } (P_S)} \quad (11.7) \quad \text{①}$$

For the emitter follower of Fig. 11.2, assuming that the output voltage is a sinusoid with the peak value \hat{V}_o , the average load power will be

$$P_L = \frac{(\hat{V}_o/\sqrt{2})^2}{R_L} = \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \quad (11.8)$$

Since the current in Q_2 is constant (I), the power drawn from the negative supply¹ is $V_{CC}I$. The *average* current in Q_1 is equal to I , and thus the average power drawn from the positive

¹This does *not* include the power drawn by the biasing resistor R and the diode-connected transistor Q_3 .

supply is $V_{CC}I$. Thus the total average supply power is

$$P_S = 2V_{CC}I \quad (11.9)$$

Equations (11.8) and (11.9) can be combined to yield

$$\begin{aligned} \eta &= \frac{1}{4} \frac{\hat{V}_o^2}{IR_L V_{CC}} \\ &= \frac{1}{4} \left(\frac{\hat{V}_o}{IR_L} \right) \left(\frac{\hat{V}_o}{V_{CC}} \right) \end{aligned} \quad (11.10)$$

Since $\hat{V}_o \leq V_{CC}$ and $\hat{V}_o \leq IR_L$, maximum efficiency is obtained when

$$\hat{V}_o = V_{CC} = IR_L \quad (11.11)$$

The maximum efficiency attainable is 25%. Because this is a rather low figure, the class A output stage is rarely used in high-power applications (>1 W). Note also that in practice the output voltage swing is limited to lower values to avoid transistor saturation and associated nonlinear distortion. Thus the efficiency achieved in practice is usually in the 10% to 20% range.

EXERCISE

11.3 For the emitter follower of Fig. 11.2, let $V_{CC} = 10$ V, $I = 100$ mA, and $R_L = 100 \Omega$. If the output voltage is an 8-V-peak sinusoid, find the following: (a) the power delivered to the load; (b) the average power drawn from the supplies; (c) the power-conversion efficiency. Ignore the loss in Q_3 and R .

Ans. 0.32 W; 2 W; 16%

11.3 Class B Output Stage

Figure 11.5 shows a class B output stage. It consists of a complementary pair of transistors (an *nnp* and a *pnnp*) connected in such a way that both cannot conduct simultaneously.

11.3.1 Circuit Operation

When the input voltage v_I is zero, both transistors are cut off and the output voltage v_O is zero. As v_I goes positive and exceeds about 0.5 V, Q_N conducts and operates as an emitter follower. In this case v_O follows v_I (i.e., $v_O = v_I - v_{BE_N}$) and Q_N supplies the load current. Meanwhile, the emitter–base junction of Q_P will be reverse-biased by the V_{BE} of Q_N , which is approximately 0.7 V. Thus Q_P will be cut off.

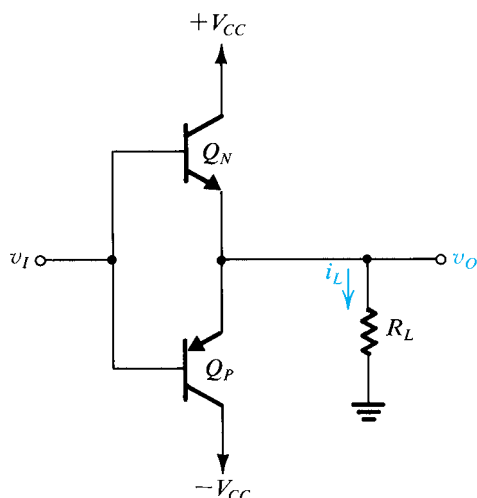


Figure 11.5 A class B output stage.

If the input goes negative by more than about 0.5 V, Q_P turns on and acts as an emitter follower. Again v_O follows v_I (i.e., $v_O = v_I + v_{EBP}$), but in this case Q_P supplies the load current and Q_N will be cut off.

We conclude that the transistors in the class B stage of Fig. 11.5 are biased at zero current and conduct only when the input signal is present. The circuit operates in a **push-pull** fashion: Q_N *pushes* (sources) current into the load when v_I is positive, and Q_P *pulls* (sinks) current from the load when v_I is negative.

11.3.2 Transfer Characteristic

A sketch of the transfer characteristic of the class B stage is shown in Fig. 11.6. Note that there exists a range of v_I centered around zero where both transistors are cut off and v_O is zero. This **dead band** results in the **crossover distortion** illustrated in Fig. 11.7 for the case of an input sine wave. The effect of crossover distortion will be most pronounced when the

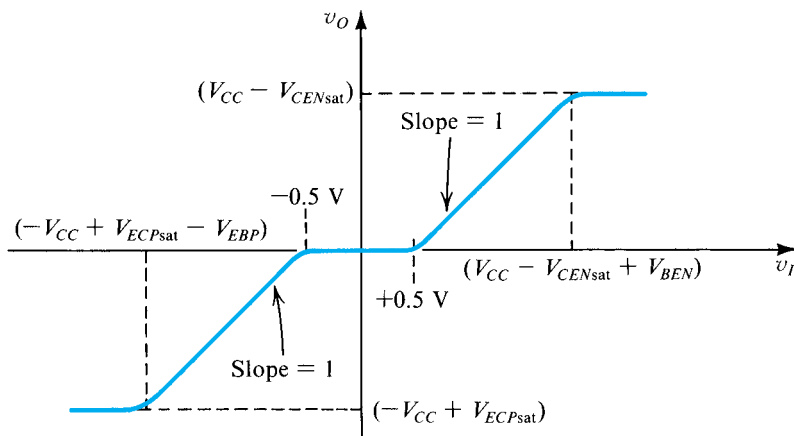


Figure 11.6 Transfer characteristic for the class B output stage in Fig. 11.5.

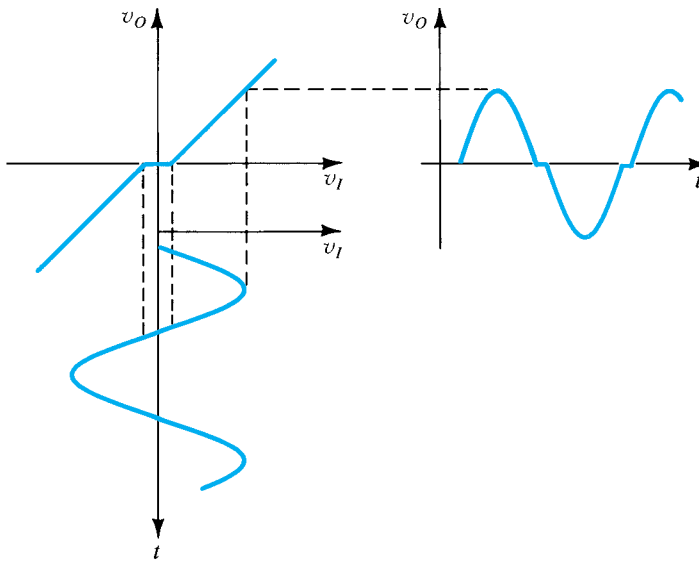


Figure 11.7 Illustrating how the dead band in the class B transfer characteristic results in crossover distortion.

amplitude of the input signal is small. Crossover distortion in audio power amplifiers gives rise to unpleasant sounds.

11.3.3 Power-Conversion Efficiency

To calculate the power-conversion efficiency, η , of the class B stage, we neglect the crossover distortion and consider the case of an output sinusoid of peak amplitude \hat{V}_o . The average load power will be

$$P_L = \frac{1\hat{V}_o^2}{2R_L} \quad (11.12)$$

The current drawn from each supply will consist of half-sine waves of peak amplitude (\hat{V}_o/R_L) . Thus the average current drawn from each of the two power supplies will be $\hat{V}_o/\pi R_L$. It follows that the average power drawn from each of the two power supplies will be the same,

$$P_{S+} = P_{S-} = \frac{1}{\pi R_L} \hat{V}_o V_{CC} \quad (11.13)$$

and the total supply power will be

$$P_S = \frac{2\hat{V}_o}{\pi R_L} V_{CC} \quad (11.14)$$

Thus the efficiency will be given by

$$\eta = \left(\frac{1}{2} \frac{\hat{V}_o^2}{R_L} \right) / \left(\frac{2\hat{V}_o}{\pi R_L} V_{CC} \right) = \frac{\pi}{4} \frac{\hat{V}_o}{V_{CC}} \quad (11.15)$$

It follows that the maximum efficiency is obtained when \hat{V}_o is at its maximum. This maximum is limited by the saturation of Q_N and Q_P to $V_{CC} - V_{CEsat} \approx V_{CC}$. At this value of peak output voltage, the power-conversion efficiency is

$$\eta_{\max} = \frac{\pi}{4} = 78.5\% \quad (11.16) \quad \text{!}$$

This value is much larger than that obtained in the class A stage (25%). Finally, we note that the maximum average power available from a class B output stage is obtained by substituting $\hat{V}_o = V_{CC}$ in Eq. (11.12),

$$P_{L\max} = \frac{1}{2} \frac{V_{CC}^2}{R_L} \quad (11.17) \quad \text{!}$$

11.3.4 Power Dissipation

Unlike the class A stage, which dissipates maximum power under quiescent conditions ($v_o = 0$), the quiescent power dissipation of the class B stage is zero. When an input signal is applied, the *average* power dissipated in the class B stage is given by

$$P_D = P_S - P_L \quad (11.18)$$

Substituting for P_S from Eq. (11.14) and for P_L from Eq. (11.12) results in

$$P_D = \frac{2}{\pi} \frac{\hat{V}_o}{R_L} V_{CC} - \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \quad (11.19)$$

From symmetry we see that half of P_D is dissipated in Q_N and the other half in Q_P . Thus Q_N and Q_P must be capable of safely dissipating $\frac{1}{2}P_D$ watts. Since P_D depends on \hat{V}_o , we must find the worst-case power dissipation, $P_{D\max}$. Differentiating Eq. (11.19) with respect to \hat{V}_o and equating the derivative to zero gives the value of \hat{V}_o that results in maximum average power dissipation as

$$\hat{V}_o|_{P_{D\max}} = \frac{2}{\pi} V_{CC} \quad (11.20) \quad \text{!}$$

Substituting this value in Eq. (11.19) gives

$$P_{D\max} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad (11.21) \quad \text{!}$$

Thus,

$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L} \quad (11.22) \quad \text{!}$$

At the point of maximum power dissipation, the efficiency can be evaluated by substituting for \hat{V}_o from Eq. (11.20) into Eq. (11.15); hence, $\eta = 50\%$.

Figure 11.8 shows a sketch of P_D (Eq. 11.19) versus the peak output voltage \hat{V}_o . Curves such as this are usually given on the data sheets of IC power amplifiers. [Usually, however, P_D is plotted versus P_L , as $P_L = \frac{1}{2}(\hat{V}_o^2/R_L)$, rather than \hat{V}_o .] An interesting observation follows from Fig. 11.8: Increasing \hat{V}_o beyond $2V_{CC}/\pi$ *decreases* the power dissipated in the

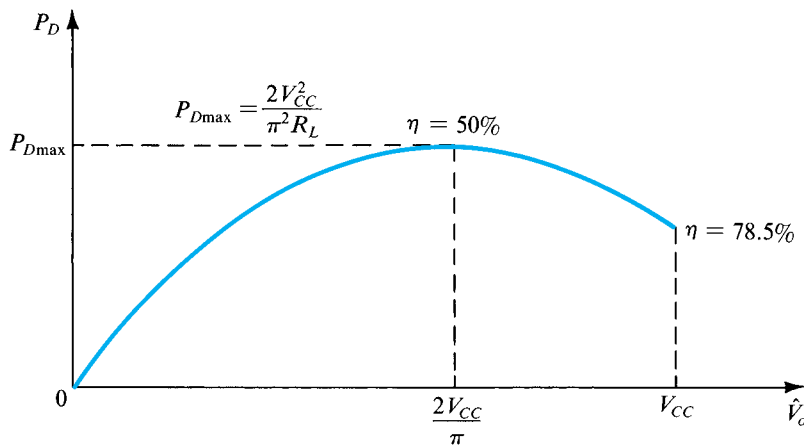


Figure 11.8 Power dissipation of the class B output stage versus amplitude of the output sinusoid.

class B stage while increasing the load power. The price paid is an increase in nonlinear distortion as a result of approaching the saturation region of operation of Q_N and Q_P . Transistor saturation flattens the peaks of the output sine waveform. Unfortunately, this type of distortion cannot be significantly reduced by the application of negative feedback (see Section 10.2), and thus transistor saturation should be avoided in applications requiring low THD.

Example 11.2

It is required to design a class B output stage to deliver an average power of 20 W to an 8- Ω load. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including short-circuit protection circuitry. (The latter will be discussed in Section 11.8.) Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

Solution

Since

$$P_L = \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

then

$$\begin{aligned} \hat{V}_o &= \sqrt{2P_LR_L} \\ &= \sqrt{2 \times 20 \times 8} = 17.9 \text{ V} \end{aligned}$$

Therefore we select $V_{CC} = 23 \text{ V}$.

The peak current drawn from each supply is

$$\hat{I}_o = \frac{\hat{V}_o}{R_L} = \frac{17.9}{8} = 2.24 \text{ A}$$

Since each supply provides a current waveform of half-sinusoids, the average current drawn from each supply will be \hat{I}_o/π . Thus the average power drawn from each supply is

$$P_{S+} = P_{S-} = \frac{1}{\pi} \times 2.24 \times 23 = 16.4 \text{ W}$$

for a total supply power of 32.8 W. The power-conversion efficiency is

$$\eta = \frac{P_L}{P_S} = \frac{20}{32.8} \times 100 = 61\%$$

The maximum power dissipated in each transistor is given by Eq. (11.22); thus,

$$\begin{aligned} P_{DN\max} = P_{DP\max} &= \frac{V_{CC}^2}{\pi^2 R_L} \\ &= \frac{(23)^2}{\pi^2 \times 8} = 6.7 \text{ W} \end{aligned}$$

11.3.5 Reducing Crossover Distortion

The crossover distortion of a class B output stage can be reduced substantially by employing a high-gain op amp and overall negative feedback, as shown in Fig. 11.9. The ± 0.7 -V dead band is reduced to $\pm 0.7/A_0$ volt, where A_0 is the dc gain of the op amp. Nevertheless, the slew-rate limitation of the op amp will cause the alternate turning on and off of the output transistors to be noticeable, especially at high frequencies. A more practical method for reducing and almost eliminating crossover distortion is found in the class AB stage, which will be studied in the next section.

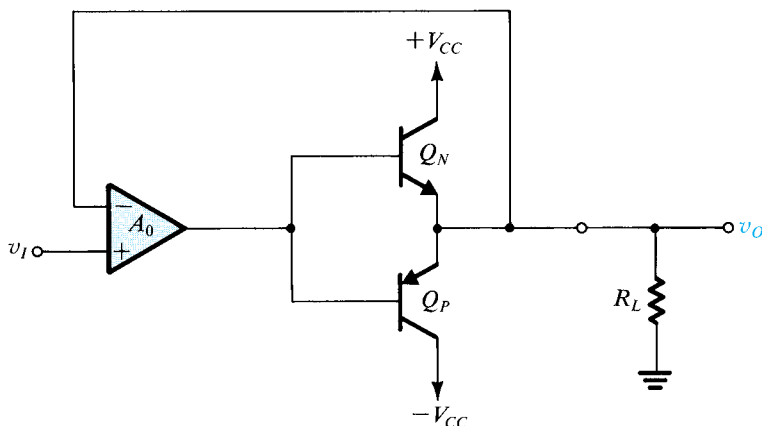


Figure 11.9 Class B circuit with an op amp connected in a negative-feedback loop to reduce crossover distortion.

11.3.6 Single-Supply Operation

The class B stage can be operated from a single power supply, in which case the load is capacitively coupled, as shown in Fig. 11.10. Note that to make the formulas derived in Section 11.3.4 directly applicable, the single power supply is denoted $2V_{CC}$.

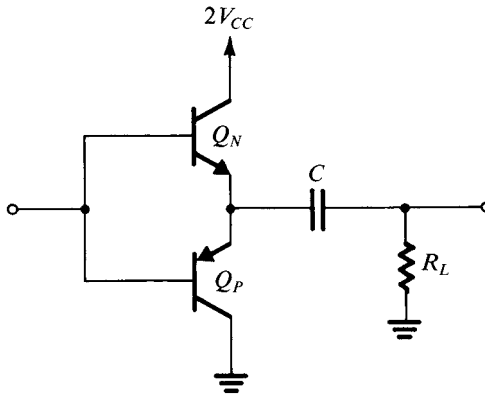


Figure 11.10 Class B output stage operated with a single power supply.

EXERCISE

11.4 For the class B output stage of Fig. 11.5, let $V_{CC} = 6\text{ V}$ and $R_L = 4\ \Omega$. If the output is a sinusoid with 4.5-V peak amplitude, find (a) the output power; (b) the average power drawn from each supply; (c) the power efficiency obtained at this output voltage; (d) the peak currents supplied by v_p , assuming that $\beta_N = \beta_P = 50$; (e) the maximum power that each transistor must be capable of dissipating safely.

Ans. (a) 2.53 W; (b) 2.15 W; (c) 59%; (d) 22.1 mA; (e) 0.91 W

11.4 Class AB Output Stage

Crossover distortion can be virtually eliminated by biasing the complementary output transistors at a small nonzero current. The result is the class AB output stage shown in Fig. 11.11. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P . For $v_I = 0$, $v_O = 0$, and a voltage $V_{BB}/2$ appears across the base-emitter junction of each of Q_N and Q_P . Assuming matched devices,

I

$$i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T} \quad (11.23)$$

The value of V_{BB} is selected to yield the required quiescent current I_Q .

11.4.1 Circuit Operation

When v_I goes positive by a certain amount, the voltage at the base of Q_N increases by the same amount and the output becomes positive at an almost equal value,

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN} \quad (11.24)$$

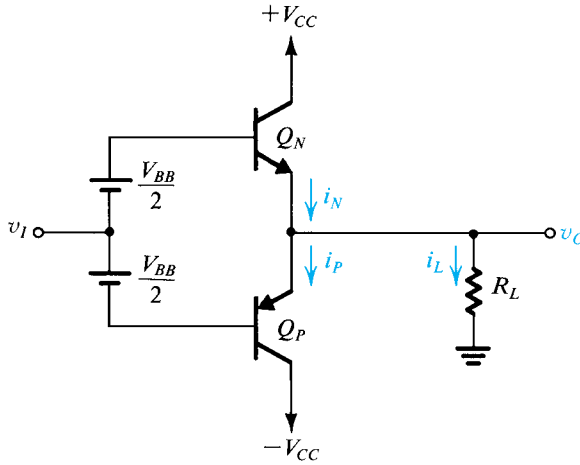


Figure 11.11 Class AB output stage. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P , giving rise to a bias current I_Q given by Eq. (11.23). Thus, for small v_i , both transistors conduct and crossover distortion is almost completely eliminated.

The positive v_o causes a current i_L to flow through R_L , and thus i_N must increase; that is,

$$i_N = i_P + i_L \quad (11.25)$$

The increase in i_N will be accompanied by a corresponding increase in v_{BEN} (above the quiescent value of $V_{BB}/2$). However, since the voltage between the two bases remains constant at V_{BB} , the increase in v_{BEN} will result in an equal decrease in v_{EBP} and hence in i_P . The relationship between i_N and i_P can be derived as follows:

$$\begin{aligned} v_{BEN} + v_{EBP} &= V_{BB} \\ V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} &= 2V_T \ln \frac{I_Q}{I_S} \\ i_N i_P &= I_Q^2 \end{aligned} \quad (11.26)$$

Thus, as i_N increases, i_P decreases by the same ratio while the product remains constant. Equations (11.25) and (11.26) can be combined to yield i_N for a given i_L as the solution to the quadratic equation

$$i_N^2 - i_L i_N - I_Q^2 = 0 \quad (11.27)$$

From the equations above, we can see that for positive output voltages, the load current is supplied by Q_N , which acts as the output emitter follower. Meanwhile, Q_P will be conducting a current that decreases as v_o increases; for large v_o the current in Q_P can be ignored altogether.

For negative input voltages the opposite occurs: The load current will be supplied by Q_P , which acts as the output emitter follower, while Q_N conducts a current that gets smaller as v_i becomes more negative. Equation (11.26), relating i_N and i_P , holds for negative inputs as well.

We conclude that the class AB stage operates in much the same manner as the class B circuit, with one important exception: For small v_i , both transistors conduct, and as v_i is increased or decreased, one of the two transistors takes over the operation. Since the

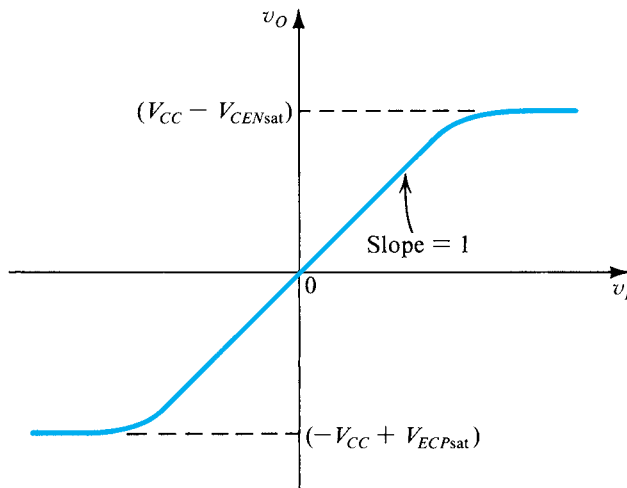


Figure 11.12 Transfer characteristic of the class AB stage in Fig. 11.11.

transition is a smooth one, crossover distortion will be almost totally eliminated. Figure 11.12 shows the transfer characteristic of the class AB stage.

The power relationships in the class AB stage are almost identical to those derived for the class B circuit in Section 11.3. The only difference is that under quiescent conditions the class AB circuit dissipates a power of $V_{CC}I_Q$ per transistor. Since I_Q is usually much smaller than the peak load current, the quiescent power dissipation is usually small. Nevertheless, it can be taken into account easily. Specifically, we can simply add the quiescent dissipation per transistor to its maximum power dissipation with an input signal applied, to obtain the total power dissipation that the transistor must be able to handle safely.

11.4.2 Output Resistance

If we assume that the source supplying v_I is ideal, then the output resistance of the class AB stage can be determined from the circuit in Fig. 11.13 as

$$\text{①} \quad R_{\text{out}} = r_{eN} \parallel r_{eP} \quad (11.28)$$

where r_{eN} and r_{eP} are the small-signal emitter resistances of Q_N and Q_P , respectively. At a given input voltage, the currents i_N and i_P can be determined, and r_{eN} and r_{eP} are given by

$$r_{eN} = \frac{V_T}{i_N} \quad (11.29)$$

$$r_{eP} = \frac{V_T}{i_P} \quad (11.30)$$

Thus,

$$\text{①} \quad R_{\text{out}} = \frac{V_T}{i_N} \parallel \frac{V_T}{i_P} = \frac{V_T}{i_P + i_N} \quad (11.31)$$

Since as i_N increases, i_P decreases, and vice versa, the output resistance remains approximately constant in the region around $v_I = 0$. This, in effect, is the reason for the virtual

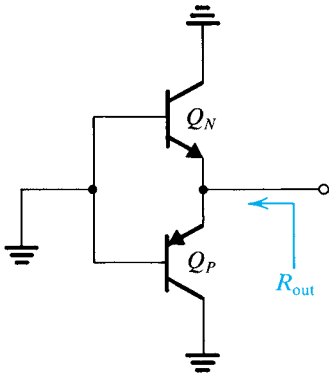


Figure 11.13 Determining the small-signal output resistance of the class AB circuit of Fig. 11.11.

absence of crossover distortion. At larger load currents, either i_N or i_P will be significant, and R_{out} decreases as the load current increases.

Example 11.3

In this example we explore the details of the transfer characteristic, v_O versus v_I , of the class AB circuit in Fig. 11.11. For this purpose let $V_{CC} = 15$ V, $I_Q = 2$ mA, and $R_L = 100$ Ω . Assume that Q_N and Q_P are matched and have $I_S = 10^{-13}$ A. First, determine the required value of the bias voltage V_{BB} . Then, find the transfer characteristic for v_O in the range -10 V to $+10$ V.

Solution

To determine the required value of V_{BB} we use Eq. (11.23) with $I_Q = 2$ mA and $I_S = 10^{-13}$ A. Thus,

$$\begin{aligned} V_{BB} &= 2V_T \ln(I_Q/I_S) \\ &= 2 \times 0.025 \ln(2 \times 10^{-3}/10^{-13}) = 1.186 \text{ V} \end{aligned}$$

The easiest way to determine the transfer characteristic is to work backward; that is, for a given v_O we determine the corresponding value of v_I . We shall outline the process for positive v_O :

1. Assume a value for v_O .
 2. Determine the load current i_L ,
- $$i_L = v_O/R_L$$
3. Use Eq. (11.27) to determine the current conducted by Q_N , i_N .
 4. Determine v_{BEN} from

$$v_{BEN} = V_T \ln(i_N/I_S)$$

5. Determine v_I from

$$v_I = v_O + v_{BEN} - V_{BB}/2$$

Example 11.3 *continued*

It is also useful to find i_P and v_{EBP} as follows:

$$i_P = i_N - i_L$$

$$v_{EBP} = V_T \ln(i_P/I_S)$$

A similar process can be employed for negative v_O . However, symmetry can be utilized, obviating the need to repeat the calculations. The results obtained are displayed in the following table:

v_O (V)	i_L (mA)	i_N (mA)	i_P (mA)	v_{BEN} (V)	v_{EBP} (V)	v_I (V)	v_O/v_I	R_{out} (W)	v_o/v_i
+10.0	100	100.04	0.04	0.691	0.495	10.1	0.99	0.25	1.00
+5.0	50	50.08	0.08	0.673	0.513	5.08	0.98	0.50	1.00
+1.0	10	10.39	0.39	0.634	0.552	1.041	0.96	2.32	0.98
+0.5	5	5.70	0.70	0.619	0.567	0.526	0.95	4.03	0.96
+0.2	2	3.24	1.24	0.605	0.581	0.212	0.94	5.58	0.95
+0.1	1	2.56	1.56	0.599	0.587	0.106	0.94	6.07	0.94
0	0	2	2	0.593	0.593	0	—	6.25	0.94
-0.1	-1	1.56	2.56	0.587	0.599	-0.106	0.94	6.07	0.94
-0.2	-2	1.24	3.24	0.581	0.605	-0.212	0.94	5.58	0.95
-0.5	-5	0.70	5.70	0.567	0.619	-0.526	0.95	4.03	0.96
-1.0	-10	0.39	10.39	0.552	0.634	-1.041	0.96	2.32	0.98
-5.0	-50	0.08	50.08	0.513	0.673	-5.08	0.98	0.50	1.00
-10.0	-100	0.04	100.04	0.495	0.691	-10.1	0.99	0.25	1.00

The table also provides values for the dc gain v_O/v_I as well as the incremental gain v_o/v_i at the various values of v_O . The incremental gain is computed as follows

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + R_{out}}$$

where R_{out} is the small-signal output resistance of the amplifier, given by Eq. (11.31). The incremental gain is the slope of the voltage transfer characteristic, and the magnitude of its variation over the range of v_O is an indication of the linearity of the output stage. Observe that for $0 \leq |v_O| \leq 10$ V, the incremental gain changes from 0.94 to 1.00, about 6%. Also observe as v_O becomes positive, Q_N supplies more and more of i_L and Q_P is correspondingly reduced. The opposite happens for negative v_O .

EXERCISE

- 11.5** To increase the linearity of the class AB output stage, the quiescent current I_Q is increased. The price paid is an increase in quiescent power dissipation. For the output stage considered in Example 11.3:
- Find the quiescent power dissipation.
 - If I_Q is increased to 10 mA, find v_o/v_i at $v_O = 0$ and at $|v_O| = 10$ V, and hence the percentage change. Compare to the case in Example 11.3.
 - Find the quiescent power dissipation for the case in (b).

Ans. (a) 60 mW; (b) 0.988 to 1.00; for a change of 1.2% compared to the 6% change in Example 11.3; (c) 300 mW

11.5 Biasing the Class AB Circuit

In this section we discuss two approaches for generating the voltage V_{BB} required for biasing the class AB output stage.

11.5.1 Biasing Using Diodes

Figure 11.14 shows a class AB circuit in which the bias voltage V_{BB} is generated by passing a constant current I_{BIAS} through a pair of diodes, or diode-connected transistors, D_1 and D_2 . In circuits that supply large amounts of power, the output transistors are large-geometry devices. The biasing diodes, however, need not be large devices, and thus the quiescent current I_Q established in Q_N and Q_P will be $I_Q = nI_{BIAS}$, where n is the ratio of the emitter-junction area of the output devices to the junction area of the biasing diodes. In other words, the saturation (or scale) current I_s of the output transistors is n times that of the biasing diodes. Area ratioing is simple to implement in integrated circuits but difficult to realize in discrete-circuit designs.

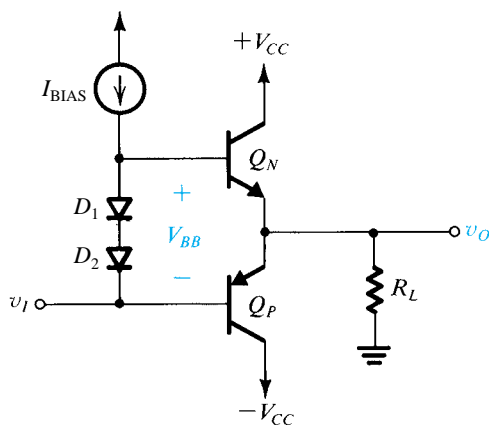


Figure 11.14 A class AB output stage utilizing diodes for biasing. If the junction area of the output devices, Q_N and Q_P , is n times that of the biasing devices D_1 and D_2 , a quiescent current $I_Q = nI_{BIAS}$ flows in the output devices.

When the output stage of Fig. 11.14 is sourcing current to the load, the base current of Q_N increases from I_Q/β_N (which is usually small) to approximately i_L/β_N . This base current drive must be supplied by the current source I_{BIAS} . It follows that I_{BIAS} must be greater than the maximum anticipated base drive for Q_N . This sets a lower limit on the value of I_{BIAS} . Now, since $n = I_Q/I_{BIAS}$, and since I_Q is usually much smaller than the peak load current (<10%), we see that we cannot make n a large number. In other words, we cannot make the diodes much smaller than the output devices. This is a disadvantage of the diode biasing scheme.

From the discussion above we see that the current through the biasing diodes will decrease when the output stage is sourcing current to the load. Thus the bias voltage V_{BB} will also decrease, and the analysis of Section 11.4 must be modified to take this effect into account.

The diode biasing arrangement has an important advantage: It can provide thermal stabilization of the quiescent current in the output stage. To appreciate this point, recall that the class AB output stage dissipates power under quiescent conditions. Power dissipation raises the internal temperature of the BJTs. From Chapter 6 we know that a rise in transistor temperature results in a decrease in its V_{BE} (approximately -2 mV/°C) if the collector current is held constant. Alternatively, if V_{BE} is held constant and the temperature increases, the collector current increases. The increase in collector current increases the power dissipation, which in turn increases the junction

temperature and hence, once more, the collector current. Thus a positive-feedback mechanism exists that can result in a phenomenon called **thermal runaway**. Unless checked, thermal runaway can lead to the ultimate destruction of the BJT. Diode biasing can be arranged to provide a compensating effect that can protect the output transistors against thermal runaway under quiescent conditions. Specifically, if the diodes are in close thermal contact with the output transistors, their temperature will increase by the same amount as that of Q_N and Q_P . Thus V_{BB} will decrease at the same rate as $V_{BEN} + V_{EBF}$, with the result that I_Q remains constant. Close thermal contact is easily achieved in IC fabrication. It is obtained in discrete circuits by mounting the bias diodes on the metal case of Q_N or Q_P .

Example 11.4

Consider the class AB output stage under the conditions that $V_{CC} = 15\text{ V}$, $R_L = 100\ \Omega$, and the output is sinusoidal with a maximum amplitude of 10 V . Let Q_N and Q_P be matched with $I_S = 10^{-13}\text{ A}$ and $\beta = 50$. Assume that the biasing diodes have one-third the junction area of the output devices. Find the value of I_{BIAS} that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors (i.e., at $v_O = 0$). Also find V_{BB} for $v_O = 0$, $+10\text{ V}$, and -10 V .

Solution

The maximum current through Q_N is approximately equal to $i_{L\max} = 10\text{ V}/0.1\text{ k}\Omega = 100\text{ mA}$. Thus the maximum base current in Q_N is approximately 2 mA . To maintain a minimum of 1 mA through the diodes, we select $I_{BIAS} = 3\text{ mA}$. The area ratio of 3 yields a quiescent current of 9 mA through Q_N and Q_P . The quiescent power dissipation is

$$P_{DQ} = 2 \times 15 \times 9 = 270\text{ mW}$$

For $v_O = 0$, the base current of Q_N is $9/51 \approx 0.18\text{ mA}$, leaving a current of $3 - 0.18 = 2.82\text{ mA}$ to flow through the diodes. Since the diodes have $I_S = \frac{1}{3} \times 10^{-13}\text{ A}$, the voltage V_{BB} will be

$$V_{BB} = 2V_T \ln \frac{2.82\text{ mA}}{I_S} = 1.26\text{ V}$$

At $v_O = +10\text{ V}$, the current through the diodes will decrease to 1 mA , resulting in $V_{BB} \approx 1.21\text{ V}$. At the other extreme of $v_O = -10\text{ V}$, Q_N will be conducting a very small current; thus its base current will be negligibly small and all of I_{BIAS} (3 mA) flows through the diodes, resulting in $V_{BB} \approx 1.26\text{ V}$.

EXERCISES

- 11.6** For the circuit of Example 11.4, find i_N and i_P for $v_O = +10\text{ V}$ and $v_O = -10\text{ V}$. (Hint: Use the V_{BB} values found in Example 11.4.)

Ans. 100.1 mA , 0.1 mA ; 0.8 mA , 100.8 mA

- 11.7** If the collector current of a transistor is held constant, its v_{BE} decreases by 2 mV for every 1°C rise in temperature. Alternatively, if v_{BE} is held constant, then i_C increases by approximately $g_m \times 2\text{ mV}$ for every 1°C rise in temperature. For a device operating at $I_C = 10\text{ mA}$, find the change in collector current resulting from an increase in temperature of 5°C .

Ans. 4 mA

11.5.2 Biasing Using the V_{BE} Multiplier

An alternative biasing arrangement that provides the designer with considerably more flexibility in both discrete and integrated designs is shown in Fig. 11.15. The bias circuit consists of transistor Q_1 with a resistor R_1 connected between base and emitter and a feedback resistor R_2 connected between collector and base. The resulting two-terminal network is fed with a constant-current source I_{BIAS} . If we neglect the base current of Q_1 , then R_1 and R_2 will carry the same current I_R , given by

$$I_R = \frac{V_{BE1}}{R_1} \quad (11.32)$$

and the voltage V_{BB} across the bias network will be

$$\begin{aligned} V_{BB} &= I_R(R_1 + R_2) \\ &= V_{BE1} \left(1 + \frac{R_2}{R_1} \right) \end{aligned} \quad (11.33)$$

Thus the circuit simply multiplies V_{BE1} by the factor $(1 + R_2/R_1)$ and is known as the “ V_{BE} multiplier.” The multiplication factor is obviously under the designer’s control and can be used to establish the value of V_{BB} required to yield a desired quiescent current I_Q . In IC design it is relatively easy to control accurately the ratio of two resistances. In discrete-circuit design, a potentiometer can be used, as shown in Fig. 11.16, and is manually set to produce the desired value of I_Q .

The value of V_{BE1} in Eq. (11.33) is determined by the portion of I_{BIAS} that flows through the collector of Q_1 ; that is,

$$I_{C1} = I_{BIAS} - I_R \quad (11.34)$$

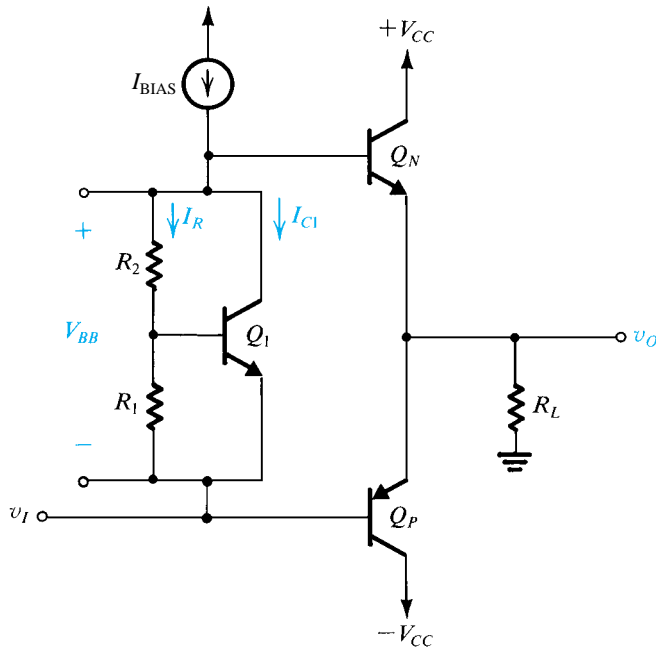


Figure 11.15 A class AB output stage utilizing a V_{BE} multiplier for biasing.

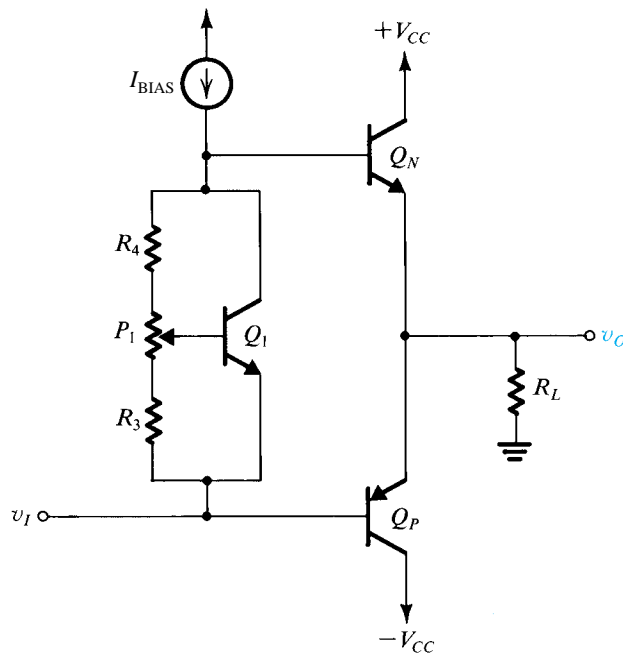


Figure 11.16 A discrete-circuit class AB output stage with a potentiometer used in the V_{BE} multiplier. The potentiometer is adjusted to yield the desired value of quiescent current in Q_N and Q_P .

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}} \quad (11.35)$$

where we have neglected the base current of Q_N , which is normally small both under quiescent conditions and when the output voltage is swinging negative. However, for positive v_O , especially at and near its peak value, the base current of Q_N can become sizable and will reduce the current available for the V_{BE} multiplier. Nevertheless, since large changes in I_{C1} correspond to only small changes in V_{BE1} , the decrease in current will be mostly absorbed by Q_1 , leaving I_R , and hence V_{BB} , almost constant.

EXERCISE

- 11.8** Consider a V_{BE} multiplier with $R_1 = R_2 = 1.2 \text{ k}\Omega$, utilizing a transistor that has $V_{BE} = 0.6 \text{ V}$ at $I_C = 1 \text{ mA}$, and a very high β . (a) Find the value of the current I that should be supplied to the multiplier to obtain a terminal voltage of 1.2 V . (b) Find the value of I that will result in the terminal voltage changing (from the 1.2-V value) by $+50 \text{ mV}$, $+100 \text{ mV}$, $+200 \text{ mV}$, -50 mV , -100 mV , -200 mV .

Ans. (a) 1.5 mA ; (b) 3.24 mA , 7.93 mA , 55.18 mA , 0.85 mA , 0.59 mA , 0.43 mA

Like the diode biasing network, the V_{BE} -multiplier circuit can provide thermal stabilization of I_Q . This is especially true if $R_1 = R_2$, and Q_1 is in close thermal contact with the output transistors.

Example 11.5

It is required to redesign the output stage of Example 11.4 utilizing a V_{BE} multiplier for biasing. Use a small-geometry transistor for Q_1 with $I_s = 10^{-14}$ A and design for a quiescent current $I_Q = 2$ mA.

Solution

Since the peak positive current is 100 mA, the base current of Q_N can be as high as 2 mA. We shall therefore select $I_{BIAS} = 3$ mA, thus providing the multiplier with a minimum current of 1 mA.

Under quiescent conditions ($v_o = 0$ and $i_L = 0$) the base current of Q_N can be neglected and all of I_{BIAS} flows through the multiplier. We now must decide on how this current (3 mA) is to be divided between I_{C1} and I_R . If we select I_R greater than 1 mA, the transistor will be almost cut off at the positive peak of v_o . Therefore, we shall select $I_R = 0.5$ mA, leaving 2.5 mA for I_{C1} .

To obtain a quiescent current of 2 mA in the output transistors, V_{BB} should be

$$V_{BB} = 2V_T \ln \frac{2 \times 10^{-3}}{10^{-13}} = 1.19 \text{ V}$$

We can now determine $R_1 + R_2$ as follows:

$$R_1 + R_2 = \frac{V_{BB}}{I_R} = \frac{1.19}{0.5} = 2.38 \text{ k}\Omega$$

At a collector current of 2.5 mA, Q_1 has

$$V_{BE1} = V_T \ln \frac{2.5 \times 10^{-3}}{10^{-14}} = 0.66 \text{ V}$$

The value of R_1 can now be determined as

$$R_1 = \frac{0.66}{0.5} = 1.32 \text{ k}\Omega$$

and R_2 as

$$R_2 = 2.38 - 1.32 = 1.06 \text{ k}\Omega$$

11.6 CMOS Class AB Output Stages

In this section we study CMOS class AB output stages. We begin with the CMOS counterpart of the BJT class AB output stage studied in the previous section. As we shall see, this circuit suffers from a relatively low output signal-swing, a serious limitation especially in view of the shrinking power-supply voltages characteristic of modern deep-submicron CMOS technologies. We will then look at an attractive alternative circuit that overcomes this problem.

11.6.1 The Classical Configuration

Figure 11.17 shows the classical CMOS class AB output stage. The circuit is the exact counterpart of the bipolar circuit shown in Fig. 11.14 with the biasing diodes implemented with diode-connected transistors Q_1 and Q_2 . The constant current I_{BIAS} flowing through Q_1 and Q_2 establishes a dc bias voltage V_{GG} between the gates of Q_N and Q_P . This voltage in turn

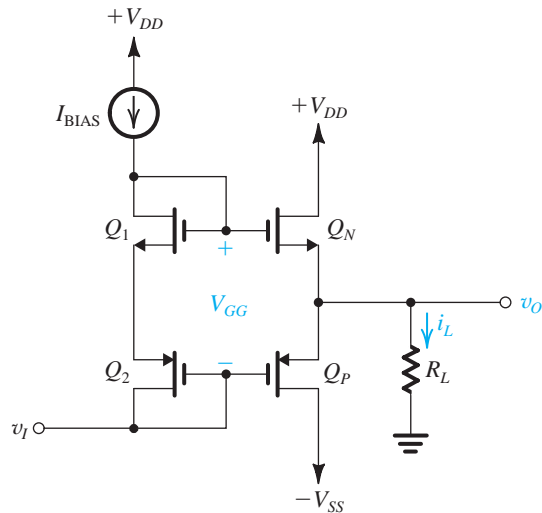


Figure 11.17 Classical CMOS class AB output stage. This circuit is the CMOS counterpart of the BJT circuit in Fig. 11.14 with the biasing diodes implemented with diode-connected MOSFETs, Q_1 and Q_2 .

establishes the quiescent ($v_O = 0$) current I_Q in Q_N and Q_P . Unlike the BJT circuit in Fig. 11.14, here the zero dc gate current of Q_N results in the current through Q_1 and Q_2 remaining constant at I_{BIAS} irrespective of the value of v_O and the load current i_L . Thus V_{GG} remains constant and the circuit is more like the idealized bipolar case shown in Fig. 11.11.

The value of I_Q can be determined by utilizing the $i_D - v_{GS}$ equations for the four MOS transistors for the case $v_O = 0$. Neglecting channel-length modulation, we can write for Q_1 ,

$$I_{D1} = I_{\text{BIAS}} = \frac{1}{2}k_n'(W/L)_1(V_{GS1} - V_{tn})^2 \quad (11.36)$$

and for Q_2 ,

$$I_{D2} = I_{\text{BIAS}} = \frac{1}{2}k_p'(W/L)_2(V_{SG2} - |V_{tp}|)^2 \quad (11.37)$$

Equations (11.36) and (11.37) can be used to find V_{GS1} and V_{SG2} , which when summed yield V_{GG} ; thus,

$$V_{GG} = V_{GS1} + V_{SG2} = V_{tn} + |V_{tp}| + \sqrt{2I_{\text{BIAS}}} \left(\frac{1}{\sqrt{k_n'(W/L)_1}} + \frac{1}{\sqrt{k_p'(W/L)_2}} \right) \quad (11.38)$$

We can follow a similar process for Q_N and Q_P which, for $v_O = 0$, are conducting the quiescent current I_Q ; thus,

$$V_{GG} = V_{GSN} + V_{SGP} = V_{tn} + |V_{tp}| + \sqrt{2I_Q} \left(\frac{1}{\sqrt{k_n'(W/L)_n}} + \frac{1}{\sqrt{k_p'(W/L)_p}} \right) \quad (11.39)$$

Equations (11.38) and (11.39) can be combined to obtain

$$I_Q = I_{\text{BIAS}} \left[\frac{1/\sqrt{k_n'(W/L)_1} + 1/\sqrt{k_p'(W/L)_2}}{1/\sqrt{k_n'(W/L)_n} + 1/\sqrt{k_p'(W/L)_p}} \right]^2 \quad (11.40)$$

which indicates that I_Q is determined by I_{BIAS} together with the (W/L) ratios of the four transistors. For the case Q_1 and Q_2 are matched, that is,

$$k'_p(W/L)_2 = k'_n(W/L)_1 \quad (11.41)$$

and Q_N and Q_P are matched, that is,

$$k'_p(W/L)_p = k'_n(W/L)_n \quad (11.42)$$

Equation (11.40) simplifies to

$$I_Q = I_{\text{BIAS}} \frac{(W/L)_n}{(W/L)_1} \quad (11.43) \quad \text{!}$$

which is an intuitively appealing result.

EXERCISE

11.9 For the CMOS class AB output stage of Fig. 11.17, consider the case of matched Q_1 and Q_2 , and matched Q_N and Q_P . If $I_Q = 1$ mA and $I_{\text{BIAS}} = 0.2$ mA, find (W/L) for each of Q_1 , Q_2 , Q_N , and Q_P so that in the quiescent state each transistor operates at an overdrive voltage of 0.2 V. Let $V_{DD} = V_{SS} = 2.5$ V, $k'_n = 250$ $\mu\text{A}/\text{V}^2$, $k'_p = 100$ $\mu\text{A}/\text{V}^2$, and $V_{tn} = -V_{tp} = 0.5$ V. Also find V_{GG} .

Ans. 40; 100; 200; 500; 1.4 V

A drawback of the CMOS class AB circuit of Fig. 11.17 is the restricted range of output voltage swing. To find the maximum possible value of v_O , refer to Fig. 11.17 and assume that across the bias current source is a dc voltage of V_{BIAS} . We can write for v_O ,

$$v_O = V_{DD} - V_{\text{BIAS}} - v_{GSN} \quad (11.44)$$

The maximum value of v_O will be limited by the need to keep V_{BIAS} to a minimum of V_{OV} of the transistor supplying I_{BIAS} (otherwise the current-source transistor no longer operates in saturation); thus,

$$v_{O\text{max}} = V_{DD} - V_{OV}|_{\text{BIAS}} - v_{GSN} \quad (11.45)$$

Note that when v_O is at its maximum value, Q_N will be supplying most or all of i_L , and v_{GSN} will be large,

$$v_{O\text{max}} = V_{DD} - V_{OV}|_{\text{BIAS}} - V_{tn} - v_{OVN} \quad (11.46) \quad \text{!}$$

where v_{OVN} is the overdrive voltage of Q_N when it is supplying $i_{L\text{max}}$.

EXERCISE

11.10 For the circuit specified in Exercise 11.9, find $v_{O\max}$ when $i_{L\max} = 10$ mA. Assume that Q_N is supplying all of $i_{L\max}$ and that $V_{OV}|_{\text{BIAS}} = 0.2$ V.

Ans. 1.17 V

The minimum allowed value of v_O can be found in a similar way. Here we note that the transistor supplying v_I (not shown) will need a minimum voltage across it of $V_{OV}|_I$. Thus,

$$\textcircled{1} \quad v_{O\min} = -V_{SS} + V_{OV}|_I + |V_{tp}| + |v_{OVp}| \quad (11.47)$$

where $|v_{OVp}|$ is the overdrive voltage of Q_P when sinking the maximum negative value of i_L .

Finally, we observe that the reason for the lower allowable range of v_O in the CMOS circuit is the relatively large value of v_{OVN} and $|v_{OVp}|$; that is, the large values of v_{GSN} and v_{SGP} required to supply the large output currents. In the BJT circuit the corresponding voltages, v_{BEN} and v_{EBP} , remain close to 0.7 V. The overdrive voltages v_{OVN} and $|v_{OVp}|$ can be reduced by making the W/L ratios of Q_N and Q_P large. This, however, can lead to impractically large devices.

11.6.2 An Alternative Circuit Utilizing Common-Source Transistors

The allowable range of v_O can be increased by replacing the source followers with a pair of complementary transistors connected in the common-source configuration, as shown in Fig. 11.18. Here Q_P supplies the load current when v_O is positive and allows v_O to go as high as $(V_{DD} - |v_{OVp}|)$, a much higher value than that given by Eq. (11.46). For negative v_O , Q_N sinks the load current and allows v_O to go as low as $-V_{SS} + v_{OVN}$. This also is larger in magnitude than the value given by Eq. (11.47). Thus, the circuit of Fig. 11.18 provides an output voltage range that is within an overdrive voltage of each of the supplies. The disadvantage of the circuit, however, is its high output resistance,

$$R_{\text{out}} = r_{on} \parallel r_{op} \quad (11.48)$$

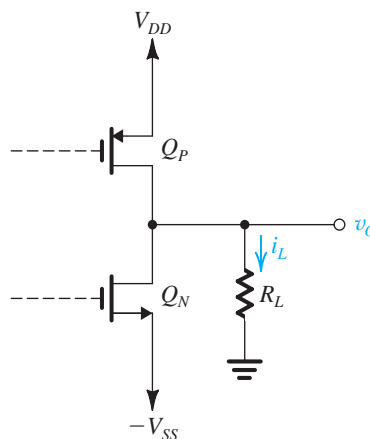


Figure 11.18 An alternative CMOS output stage utilizing a pair of complementary MOSFETs connected in the common-source configuration. The driving circuit is not shown.

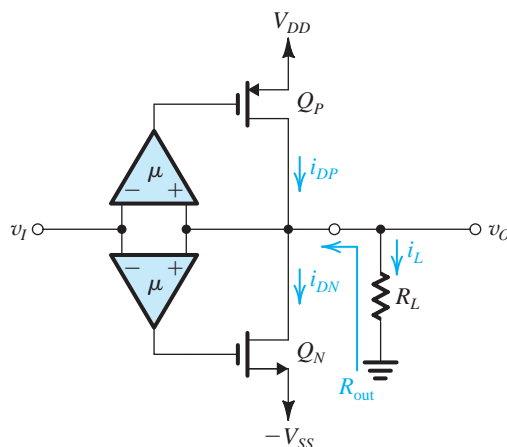


Figure 11.19 Inserting an amplifier in the negative feedback path of each of Q_N and Q_P reduces the output resistance and makes $v_O \approx v_I$; both are desirable properties for the output stage.

To reduce the output resistance, negative feedback is employed as shown in Fig. 11.19. Here an amplifier with gain μ is inserted between drain and gate of each of Q_N and Q_P . For reasons that will become clear shortly, these amplifiers are called **error amplifiers**. To verify that the feedback around each amplifier is negative, assume that v_O increases. The top amplifier will cause the gate voltage of Q_P to increase, thus its v_{SG} decreases and i_{DP} decreases. The decrease in i_{DP} causes v_O to decrease, which is opposite to the initially assumed change, thus verifying that the feedback is negative. A similar process can be used to verify that the feedback around the bottom amplifier also is negative.

From our study of feedback in Chapter 10, we observe that each of the two feedback loops is of the series-shunt type, which is the topology appropriate for a voltage amplifier. Thus, as we shall show shortly, the feedback will reduce the output resistance of the amplifier. Also, observe that if the loop gain is large, the voltage difference between the two input terminals of each feedback amplifier, the error voltage, will be small, resulting in $v_O \approx v_I$.

Both the low output resistance and the near-unity dc gain are highly desirable properties for an output stage.

Output Resistance To derive an expression for the output resistance R_{out} , we consider each half of the circuit separately, find its output resistance, R_{outp} for the top half and R_{outn} for the bottom half, and then obtain the overall output resistance as the parallel equivalent of the two resistances,

$$R_{out} = R_{outn} \parallel R_{outp} \quad (11.49)$$

Figure 11.20(a) shows the top half of the circuit, drawn a little differently to make the feedback topology clearer. Observe that feedback is applied by connecting the output back to the input. Thus the feedback network is the two-port shown in Fig. 11.20(b) and the feedback factor is

$$\beta = 1 \quad (11.50)$$

Including the loading effects of the feedback network results in the *A* circuit shown in Fig. 11.20(c). Note that since we are now interested in incremental quantities, we have

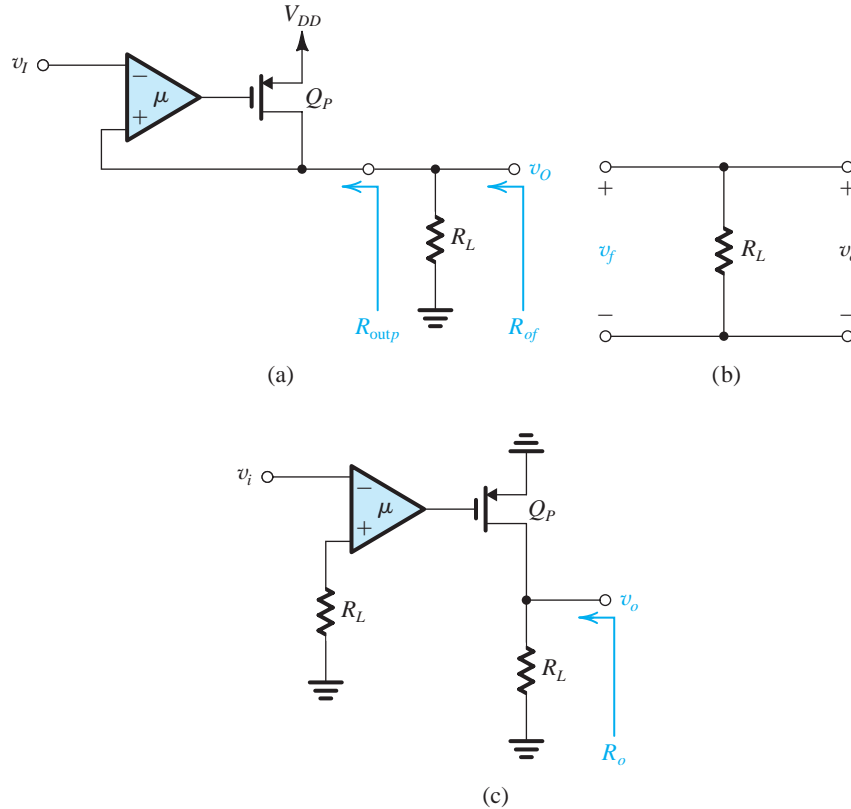


Figure 11.20 Determining the output resistance; (a) The top half of the output stage showing the definition of R_{outp} and R_{of} ; (b) The β circuit; and (c) the A circuit.

replaced V_{DD} with a short circuit to ground. The open-loop gain A can be found from the circuit in Fig. 11.20(c) as

$$A \equiv \frac{v_o}{v_i} = \mu g_{mp} (r_{op} \parallel R_L) \quad (11.51)$$

where we have assumed the input resistance of the amplifier to be infinite and thus resistance R_L at the input has no effect on the gain, and we have utilized implicitly the small-signal model of Q_P . The values of the small-signal parameters g_{mp} and r_{op} are to be evaluated at the current at which Q_P is operating. The open-loop output resistance R_o is found by inspection as

$$R_o = R_L \parallel r_{op} \quad (11.52)$$

The output resistance with feedback R_{of} can now be found as

$$R_{of} = \frac{R_o}{1 + A\beta} = \frac{(R_L \parallel r_{op})}{1 + \mu g_{mp} (r_{op} \parallel R_L)} \quad (11.53)$$

and the output resistance R_{outp} is found by excluding R_L from R_{of} , that is

$$R_{outp} = 1 / \left(\frac{1}{R_{of}} - \frac{1}{R_L} \right) \quad (11.54)$$

which results in

$$R_{outp} = r_{op} \parallel \frac{1}{\mu g_{mp}} \simeq \frac{1}{\mu g_{mp}} \quad (11.55)$$

which can be quite low. A similar development applied to the bottom half of the circuit in Fig. 11.19 results in

$$R_{outn} \simeq 1/\mu g_{mn} \quad (11.56)$$

Combining Eqs. (11.55) and (11.56) gives

$$R_{out} \simeq 1/\mu(g_{mp} + g_{mn}) \quad (11.57)$$



The Voltage Transfer Characteristic Next we derive an expression for the voltage transfer characteristic, v_O versus v_I , of the class AB common-source buffer. Toward that end, we first consider the circuit in the quiescent state, shown in Fig. 11.21(a). Here $v_I = 0$ and $v_O = 0$. Each of the error amplifiers is designed to deliver to the gate of its associated MOSFET the dc voltage required to establish the desired value of quiescent current I_Q . To obtain class AB operation, I_Q is usually selected to be 10% or so of the maximum output current. Referring to Fig. 11.21(a), we can write for Q_P ,

$$I_{DP} = I_Q = \frac{1}{2}k'_p \left(\frac{W}{L}\right)_p (V_{SGP} - |V_{tp}|)^2$$

Substituting $V_{SGP} = |V_{tp}| + V_{OV}$, where V_{OV} is the magnitude of the quiescent overdrive voltage of Q_P , gives

$$I_Q = \frac{1}{2}k'_p \left(\frac{W}{L}\right)_p V_{OV}^2 \quad (11.58)$$

Similarly, we obtain for Q_N

$$I_Q = \frac{1}{2}k'_n \left(\frac{W}{L}\right)_n V_{OV}^2 \quad (11.59)$$

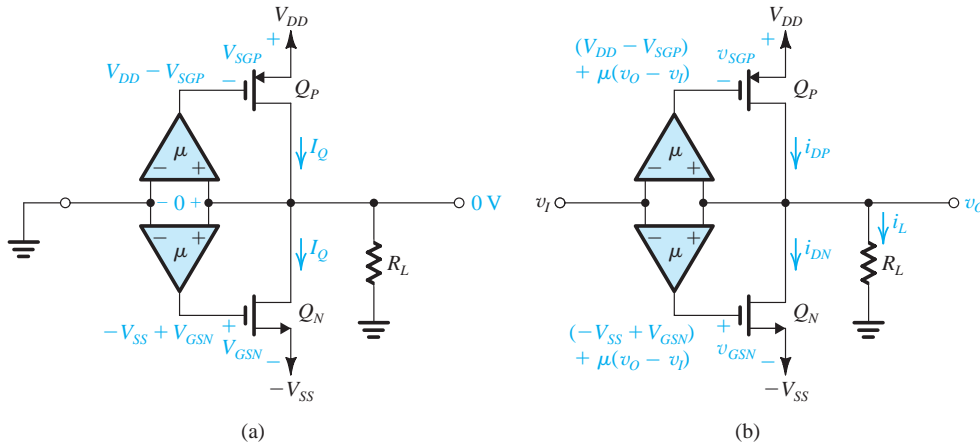


Figure 11.21 Analysis of the CMOS output stage to determine v_O versus v_I : (a) Quiescent conditions; (b) The situation with v_I applied.

Usually the two transistors are matched,

$$k_p \left(\frac{W}{L} \right)_p = k_n \left(\frac{W}{L} \right)_n = k$$

Thus,

$$I_Q = \frac{1}{2} k V_{OV}^2 \quad (11.60)$$

Next consider the situation with v_I applied, illustrated in Fig. 11.21(b). The voltage at the output of each of the error amplifiers increases by $\mu(v_O - v_I)$. Thus v_{SGP} decreases by $\mu(v_O - v_I)$ and v_{GSN} increases by $\mu(v_O - v_I)$, and we can write

$$\begin{aligned} i_{DP} &= \frac{1}{2} k [V_{OV} - \mu(v_O - v_I)]^2 \\ &= \frac{1}{2} k V_{OV}^2 \left[1 - \mu \frac{v_O - v_I}{V_{OV}} \right]^2 \\ &= I_Q \left(1 - \mu \frac{v_O - v_I}{V_{OV}} \right)^2 \end{aligned} \quad (11.61)$$

and

$$i_{DN} = I_Q \left(1 + \mu \frac{v_O - v_I}{V_{OV}} \right)^2 \quad (11.62)$$

At the output node we have

$$i_L = i_{DP} - i_{DN} \quad (11.63)$$

Substituting for $i_L = v_O / R_L$ and for i_{DP} and i_{DN} from Eqs. (11.61) and (11.62), and solving the resulting equation to obtain v_O , results in

$$v_O = \frac{v_I}{1 + \frac{V_{OV}}{4\mu I_Q R_L}} \quad (11.64)$$

Usually $(V_{OV} / 4\mu I_Q R_L) \ll 1$, enabling us to express v_O as

$$v_O \approx v_I \left(1 - \frac{V_{OV}}{4\mu I_Q R_L} \right) \quad (11.65)$$

Thus the gain error is

$$\text{Gain error} \equiv v_O - v_I = -\frac{V_{OV}}{4\mu I_Q R_L} \quad (11.66)$$

Since at the quiescent point,

$$g_{mp} = g_m = \frac{2I_Q}{V_{OV}} \quad (11.67)$$

the gain error can be expressed as

$$\text{Gain error} = -\frac{1}{2\mu g_m R_L} \quad (11.68)$$

Thus selecting a large value for μ results in reducing both the gain error and the output resistance. However, a large μ can make the quiescent current I_Q too dependent on the input offset voltages that are inevitably present in the error amplifiers. Typically, μ is selected in the range 5 to 10. Trade-offs are also present in the selection of I_Q : A large I_Q reduces crossover distortion, R_{out} , and gain error, at the expense of increased quiescent power dissipation.

Example 11.6

In this example we explore the design and operation of a class AB common-source output stage of the type shown in Fig. 11.19, required to operate from a ± 2.5 -V power supply to feed a load resistance $R_L = 100\ \Omega$. The transistors available have $V_{in} = -V_{tp} = 0.5$ V and $k'_n = 2.5k'_p = 250\ \mu\text{A}/\text{V}^2$. The gain error is required to be less than 2.5% and $I_Q = 1$ mA.

Solution

The gain error is given by Eq. (11.66),

$$\text{Gain error} = -\frac{V_{OV}}{4\mu I_Q R_L}$$

We are given the required maximum gain error of -0.025 , $I_Q = 1$ mA, and $R_L = 100\ \Omega$. In order to keep μ low and also obtain as high a g_m as possible [$g_m = 2I_Q/V_{OV}$], we select V_{OV} to be as low as possible. Practically speaking, V_{OV} is usually 0.1 V to 0.2 V. Selecting $V_{OV} = 0.1$ V results in

$$0.025 = \frac{0.1}{4 \times \mu \times 1 \times 10^{-3} \times 100}$$

which yields

$$\mu = 10$$

which is within the typically recommended range.

Figure 11.22(a) shows the circuit in the quiescent state with the various dc voltages and currents indicated. The required (W/L) ratios of Q_N and Q_P can be found as follows:

$$I_Q = \frac{1}{2}k'_p\left(\frac{W}{L}\right)_p V_{OV}^2$$

$$1 \times 10^{-3} = \frac{1}{2} \times 0.1 \times 10^{-3} \left(\frac{W}{L}\right)_p \times (0.1)^2$$

Thus,

$$\left(\frac{W}{L}\right)_p = 2000$$

$$\left(\frac{W}{L}\right)_n = \frac{(W/L)_p}{k'_n/k'_p} = \frac{2000}{2.5} = 800$$

Thus Q_N and Q_P are very large transistors, not an unusual situation in a high-power output stage.

To obtain the output resistance at the quiescent point, we use Eq. (11.57),

$$R_{out} = \frac{1}{\mu(g_{mp} + g_{mn})}$$

Example 11.6 continued

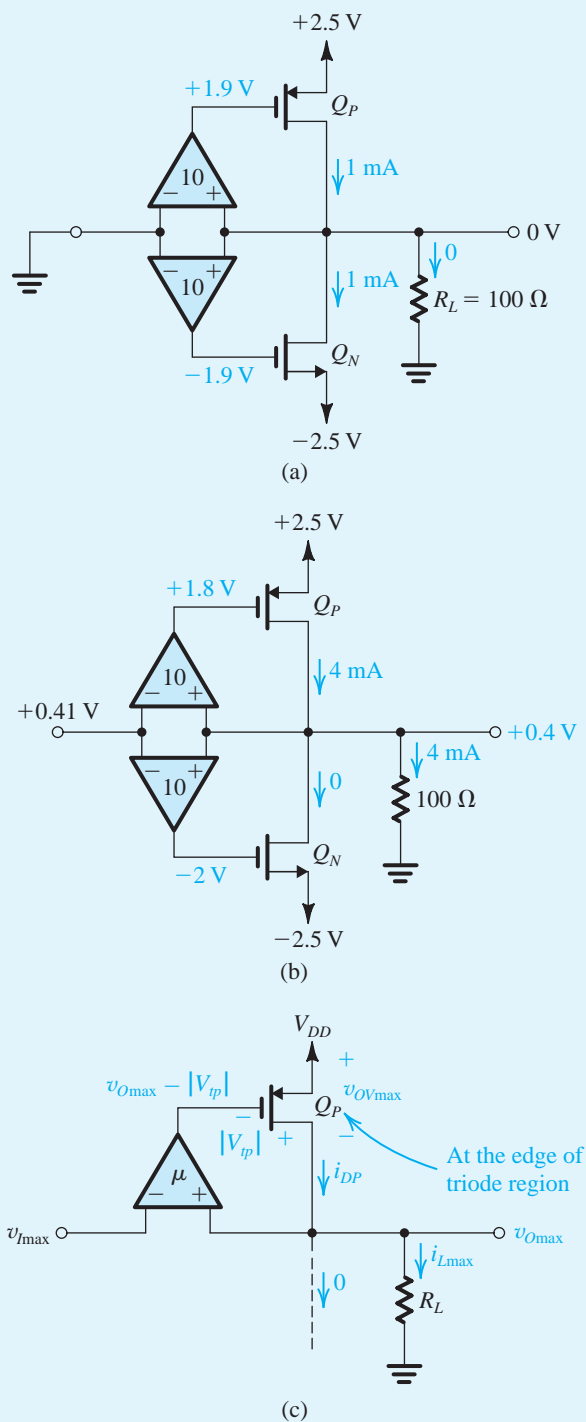


Figure 11.22 (a) Circuit in the quiescent state; (b) circuit at the point at which Q_N turns off; (c) conditions at $v_O = v_{Omax}$.

where

$$g_{mp} = g_{mn} = \frac{2I_Q}{V_{OV}} = \frac{2 \times 1}{0.1} = 20 \text{ mA/V}$$

Thus

$$R_{\text{out}} = \frac{1}{10(0.02 + 0.02)} = 2.5 \text{ } \Omega$$

Next we wish to determine the maximum and minimum allowed values of v_O . Since the circuit is symmetrical, we need to consider only either the positive-output or negative-output case. For v_O positive, Q_P conducts more of the output current i_L . Eventually, Q_N turns off and Q_P conducts all of i_L . To find the value of v_O at which this occurs, note that Q_N turns off when the voltage at its gate drops from the quiescent value of -1.9 V (see Fig. 11.22a) to -2 V , at which point $v_{GSN} = V_{in}$. An equal change of -0.1 V appears at the output of the top amplifier, as shown in Fig. 11.22(b). Analysis of the circuit in Fig. 11.22(b) shows that

$$i_L = i_{DP} = 4 \text{ mA}$$

$$v_O = i_L R_L = 4 \times 10^{-3} \times 100 = 0.4 \text{ V}$$

For $v_O > 0.4 \text{ V}$, Q_P must conduct all the current i_L . The situation at $v_O = v_{O\text{max}}$ is illustrated in Fig. 11.22(c). Analysis of this circuit results, after some straightforward but tedious manipulations, in

$$v_{O\text{max}} \approx 2.05 \text{ V}$$

and

$$i_{L\text{max}} = 20.5 \text{ mA}$$

EXERCISES

- 11.11** Suppose it is required to reduce the size of Q_N and Q_P in the circuit considered in the above example by a factor of 2 while keeping I_Q at 1 mA. What value should be used for V_{OV} ? What is the new value for the gain error and for R_{out} at the quiescent point?

Ans. 0.14 V; -3.5% ; $3.5 \text{ } \Omega$

- 11.12** Show that in the CMOS class AB common-source output stage, Q_N turns off when $v_O = 4I_Q R_L$ and that Q_P turns off when $v_O = -4I_Q R_L$. This is equivalent to saying that one of the transistors turns off when $|i_L|$ reaches $4I_Q$.

11.7 Power BJTs

Transistors that are required to conduct currents in the ampere range and to withstand power dissipation in the watts and tens-of-watts ranges differ in their physical structure, packaging, and specification from the small-signal transistors considered in earlier chapters. In this section we consider some of the important properties of power transistors, especially those

aspects that pertain to the design of circuits of the type discussed earlier. There are, of course, other important applications of power transistors, such as their use as switching elements in power inverters and motor-control circuits. Such applications are not studied in this book.

11.7.1 Junction Temperature

Power transistors dissipate large amounts of power in their collector–base junctions. The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature T_J must not be allowed to exceed a specified maximum, $T_{J\max}$; otherwise the transistor could suffer permanent damage. For silicon devices, $T_{J\max}$ is in the range of 150°C to 200°C.

11.7.2 Thermal Resistance

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor junction will be conducted away from the junction to the transistor case, and from the case to the surrounding environment. In a steady state in which the transistor is dissipating P_D watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

$$T_J - T_A = \theta_{JA} P_D \quad (11.69)$$

where θ_{JA} is the **thermal resistance** between junction and ambience, having the units of degrees Celsius per watt. Note that θ_{JA} simply gives the rise in junction temperature over the ambient temperature for each watt of dissipated power. Since we wish to be able to dissipate large amounts of power without raising the junction temperature above $T_{J\max}$, it is desirable to have, for the thermal resistance θ_{JA} , as small a value as possible. For operation in free air, θ_{JA} depends primarily on the type of case in which the transistor is packaged. The value of θ_{JA} is usually specified on the transistor data sheet.

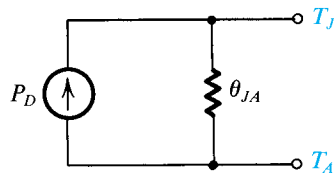


Figure 11.23 Electrical equivalent circuit of the thermal-conduction process; $T_J - T_A = P_D \theta_{JA}$.

Equation (11.69), which describes the thermal-conduction process, is analogous to Ohm's law, which describes the electrical-conduction process. In this analogy, power dissipation corresponds to current, temperature difference corresponds to voltage difference, and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal-conduction process by the electric circuit shown in Fig. 11.23.

11.7.3 Power Dissipation Versus Temperature

The transistor manufacturer usually specifies the maximum junction temperature $T_{J\max}$, the maximum power dissipation at a particular ambient temperature T_{A0} (usually, 25°C), and the

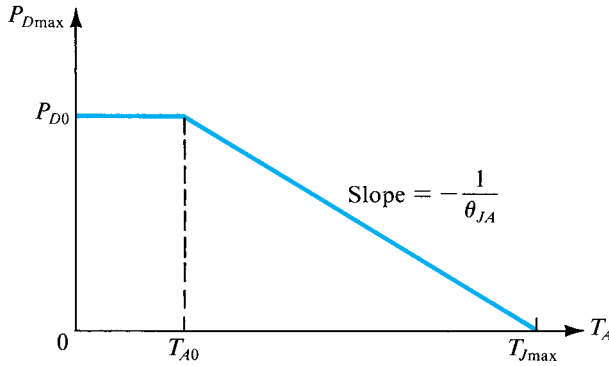


Figure 11.24 Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a “power-derating” curve.

thermal resistance θ_{JA} . In addition, a graph such as that shown in Fig. 11.24 is usually provided. The graph simply states that for operation at ambient temperatures below T_{A0} , the device can safely dissipate the rated value of P_{D0} watts. However, if the device is to be operated at higher ambient temperatures, the maximum allowable power dissipation must be **derated** according to the straight line shown in Fig. 11.24. The **power-derating curve** is a graphical representation of Eq. (11.69). Specifically, note that if the ambient temperature is T_{A0} and the power dissipation is at the maximum allowed (P_{D0}), then the junction temperature will be T_{Jmax} . Substituting these quantities in Eq. (11.69) results in

$$\theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{D0}} \quad (11.70) \quad \text{I}$$

which is the inverse of the slope of the power-derating straight line. At an ambient temperature T_A , higher than T_{A0} , the maximum allowable power dissipation P_{Dmax} can be obtained from Eq. (11.69) by substituting $T_J = T_{Jmax}$; thus,

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}} \quad (11.71) \quad \text{I}$$

Observe that as T_A approaches T_{Jmax} , the allowable power dissipation decreases; the lower thermal gradient limits the amount of heat that can be removed from the junction. In the extreme situation of $T_A = T_{Jmax}$, no power can be dissipated because no heat can be removed from the junction.

Example 11.7

A BJT is specified to have a maximum power dissipation P_{D0} of 2 W at an ambient temperature T_{A0} of 25°C, and a maximum junction temperature T_{Jmax} of 150°C. Find the following:

- The thermal resistance θ_{JA} .
- The maximum power that can be safely dissipated at an ambient temperature of 50°C.
- The junction temperature if the device is operating at $T_A = 25^\circ\text{C}$ and is dissipating 1 W.

Example 11.7 continued

Solution

$$(a) \theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} = \frac{150 - 25}{2} = 62.5^\circ\text{C/W}$$

$$(b) P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

$$(c) T_J = T_A + \theta_{JA} P_D = 25 + 62.5 \times 1 = 87.5^\circ\text{C}$$

11.7.4 Transistor Case and Heat Sink

The thermal resistance between junction and ambience, θ_{JA} , can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (11.72)$$

where θ_{JC} is the thermal resistance between junction and transistor case (package) and θ_{CA} is the thermal resistance between case and ambience. For a given transistor, θ_{JC} is fixed by the device design and packaging. The device manufacturer can reduce θ_{JC} by encapsulating the device in a relatively large metal case and placing the collector (where most of the heat is dissipated) in direct contact with the case. Most high-power transistors are packaged in this fashion. Figure 11.25 shows a sketch of a typical package.

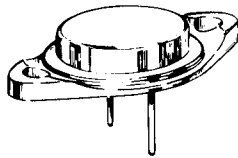


Figure 11.25 The popular TO3 package for power transistors. The case is metal with a diameter of about 2.2 cm; the outside dimension of the “seating plane” is about 4 cm. The seating plane has two holes for screws to bolt it to a heat sink. The collector is electrically connected to the case. Therefore an electrically insulating but thermally conducting spacer is used between the transistor case and the “heat sink.”

Although the circuit designer has no control over θ_{JC} (once a particular transistor has been selected), the designer can considerably reduce θ_{CA} below its free-air value (specified by the manufacturer as part of θ_{JA}). Reduction of θ_{CA} can be effected by providing means to facilitate heat transfer from case to ambience. A popular approach is to bolt the transistor to the chassis or to an extended metal surface. Such a metal surface then functions as a **heat sink**. Heat is easily conducted from the transistor case to the heat sink; that is, the thermal resistance θ_{CS} is usually very small. Also, heat is efficiently transferred (by convection and radiation) from the heat sink to the ambience, resulting in a low thermal resistance θ_{SA} . Thus, if a heat sink is utilized, the case-to-ambience thermal resistance given by

$$\theta_{CA} = \theta_{CS} + \theta_{SA} \quad (11.73)$$

can be small because its two components can be made small by the choice of an appropriate heat sink.² For example, in very high-power applications the heat sink is usually equipped with fins that further facilitate cooling by radiation and convection.

²As noted earlier, the metal case of a power transistor is electrically connected to the collector. Thus an electrically insulating material such as mica is usually placed between the metal case and the metal heat sink. Also, insulating bushings and washers are generally used in bolting the transistor to the heat sink.

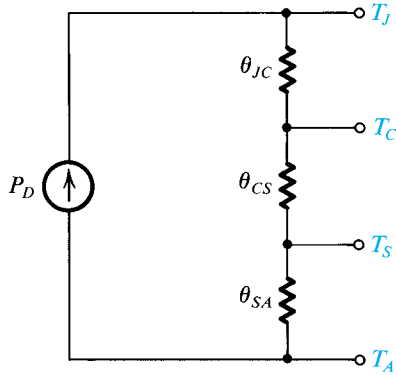


Figure 11.26 Electrical analog of the thermal conduction process when a heat sink is utilized.

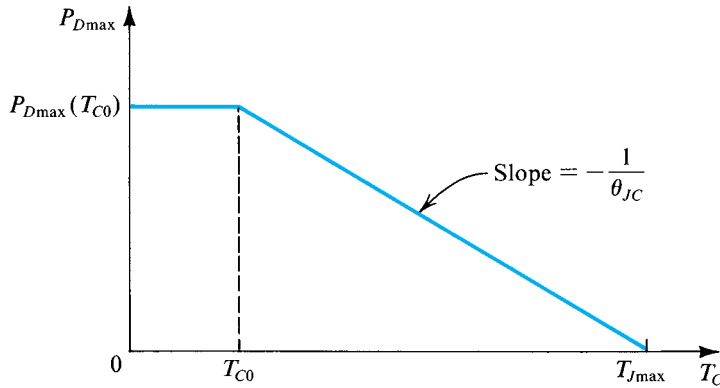


Figure 11.27 Maximum allowable power dissipation versus transistor-case temperature.

The electrical analog of the thermal-conduction process when a heat sink is employed is shown in Fig. 11.26, from which we can write

$$T_J - T_A = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (11.74)$$

As well as specifying θ_{JC} , the device manufacturer usually supplies a derating curve for $P_{D\max}$ versus the case temperature, T_C . Such a curve is shown in Fig. 11.27. Note that the slope of the power-derating straight line is $-1/\theta_{JC}$. For a given transistor, the maximum power dissipation at a *case temperature* T_{C0} (usually 25°C) is much greater than that at an *ambient temperature* T_{A0} (usually 25°C). If the device can be maintained at a case temperature T_C , $T_{C0} \leq T_C \leq T_{J\max}$, then the maximum safe power dissipation is obtained when $T_J = T_{J\max}$,

$$P_{D\max} = \frac{T_{J\max} - T_C}{\theta_{JC}} \quad (11.75)$$

Example 11.8

A BJT is specified to have $T_{j\max} = 150^\circ\text{C}$ and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_C = 25^\circ\text{C}$$

$$2 \text{ W at } T_A = 25^\circ\text{C}$$

Above 25°C , the maximum power dissipation is to be derated linearly with $\theta_{JC} = 3.12^\circ\text{C/W}$ and $\theta_{JA} = 62.5^\circ\text{C/W}$. Find the following:

- The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A = 50^\circ\text{C}$.
- The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C , but with a heat sink for which $\theta_{CS} = 0.5^\circ\text{C/W}$ and $\theta_{SA} = 4^\circ\text{C/W}$. Find the temperature of the case and of the heat sink.
- The maximum power that can be dissipated safely if an *infinite heat sink* is used and $T_A = 50^\circ\text{C}$.

Solution

(a)

$$P_{D\max} = \frac{T_{j\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

(b) With a heat sink, θ_{JA} becomes

$$\begin{aligned}\theta_{JA} &= \theta_{JC} + \theta_{CS} + \theta_{SA} \\ &= 3.12 + 0.5 + 4 = 7.62^\circ\text{C/W}\end{aligned}$$

Thus,

$$P_{D\max} = \frac{150 - 50}{7.62} = 13.1 \text{ W}$$

Figure 11.28 shows the thermal equivalent circuit with the various temperatures indicated.

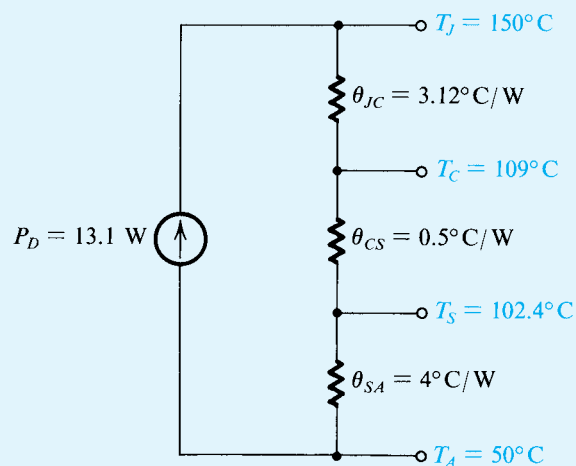


Figure 11.28 Thermal equivalent circuit for Example 11.8.

- (c) An infinite heat sink, if it existed, would cause the case temperature T_C to equal the ambient temperature T_A . The infinite heat sink has $\theta_{CA} = 0$. Obviously, one cannot buy an infinite heat sink; nevertheless, this terminology is used by some manufacturers to describe the power-detrating curve of Fig. 11.27. The abscissa is then labeled T_A and the curve is called “power dissipation versus ambient temperature with an infinite heat sink.” For our example, with infinite heat sink,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC}} = \frac{150 - 50}{3.12} = 32 \text{ W}$$

The advantage of using a heat sink is clearly evident from Example 11.8: With a heat sink, the maximum allowable power dissipation increases from 1.6 W to 13.1 W. Also note that although the transistor considered can be called a “40-W transistor,” this level of power dissipation cannot be achieved in practice; it would require an infinite heat sink and an ambient temperature $T_A \leq 25^\circ\text{C}$.

EXERCISE

- 11.13** The 2N6306 power transistor is specified to have $T_{J\max} = 200^\circ\text{C}$ and $P_{D\max} = 125 \text{ W}$ for $T_C \leq 25^\circ\text{C}$. For $T_C \geq 25^\circ\text{C}$, $\theta_{JC} = 1.4^\circ\text{C/W}$. If in a particular application this device is to dissipate 50 W and operate at an ambient temperature of 25°C , find the maximum thermal resistance of the heat sink that must be used (i.e., θ_{SA}). Assume $\theta_{CS} = 0.6^\circ\text{C/W}$. What is the case temperature, T_C ?

Ans. 1.5°C/W ; 130°C

11.7.5 The BJT Safe Operating Area

In addition to specifying the maximum power dissipation at different case temperatures, power-transistor manufacturers usually provide a plot of the boundary of the safe operating area (SOA) in the i_C – v_{CE} plane. The SOA specification takes the form illustrated by the sketch in Fig. 11.29; the following paragraph numbers correspond to the boundaries on the sketch.

1. The maximum allowable current $I_{C\max}$. Exceeding this current on a continuous basis can result in melting the wires that bond the device to the package terminals.
2. The maximum power dissipation hyperbola. This is the locus of the points for which $v_{CE}i_C = P_{D\max}$ (at T_{C0}). For temperatures $T_C > T_{C0}$, the power-detrating curves described in Section 11.7.4 should be used to obtain the applicable $P_{D\max}$ and thus a correspondingly lower hyperbola. Although the operating point can be allowed to move temporarily above the hyperbola, the *average* power dissipation should not be allowed to exceed $P_{D\max}$.
3. The **second-breakdown** limit. Second breakdown is a phenomenon that results because current flow across the emitter–base junction is not uniform. Rather, the current density is greatest near the periphery of the junction. This “**current crowding**” gives rise to increased localized power dissipation and hence temperature rise (at locations called **hot spots**). Since a temperature rise causes an increase in current, a localized form of **thermal runaway** can occur, leading to junction destruction.

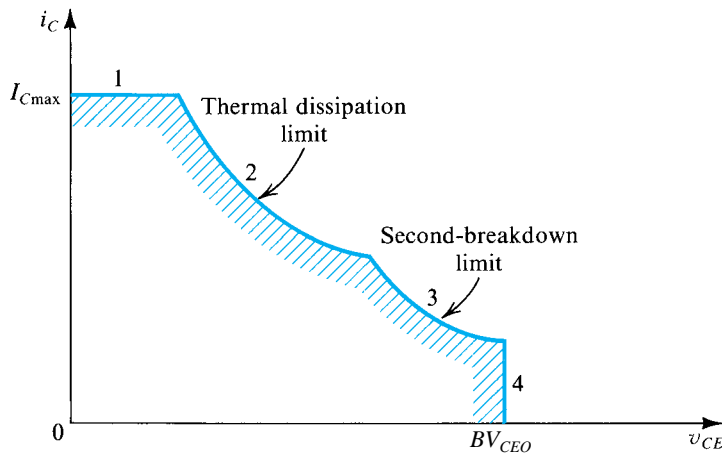


Figure 11.29 Safe operating area (SOA) of a BJT.

4. The collector-to-emitter breakdown voltage, BV_{CEO} . The instantaneous value of v_{CE} should never be allowed to exceed BV_{CEO} ; otherwise, avalanche breakdown of the collector–base junction may occur (see Section 6.9).

Finally, it should be mentioned that logarithmic scales are usually used for i_C and v_{CE} , leading to an SOA boundary that consists of straight lines.

11.7.6 Parameter Values of Power Transistors

Owing to their large geometry and high operating currents, power transistors display typical parameter values that can be quite different from those of small-signal transistors. The important differences are as follows:

1. At high currents, the exponential i_C – v_{BE} relationship exhibits a factor of 2 reduction in the exponent; that is, $i_C = I_S e^{v_{BE}/2V_T}$.
2. β is low, typically 30 to 80, but can be as low as 5. Here, it is important to note that β has a positive temperature coefficient.
3. At high currents, r_π becomes very small (a few ohms) and r_x becomes important (r_x is defined and explained in Section 9.2.2).
4. f_T is low (a few megahertz), C_μ is large (hundreds of picofarads), and C_π is even larger. (These parameters are defined and explained in Section 9.2.2).
5. I_{CBO} is large (a few tens of microamps) and, as usual, doubles for every 10°C rise in temperature.
6. BV_{CEO} is typically 50 to 100 V but can be as high as 500 V.
7. I_{Cmax} is typically in the ampere range but can be as high as 100 A.

⊕ 11.8 Variations on the Class AB Configuration

In this section, we discuss a number of circuit improvements and protection techniques for the BJT class AB output stage.

11.8.1 Use of Input Emitter Followers

Figure 11.30 shows a class AB circuit biased using transistors Q_1 and Q_2 , which also function as emitter followers, thus providing the circuit with a high input resistance. In effect, the circuit functions as a unity-gain buffer amplifier. Since all four transistors are usually matched, the quiescent current ($v_I = 0$, $R_L = \infty$) in Q_3 and Q_4 is equal to that in Q_1 and Q_2 . Resistors R_3 and R_4 are usually very small and are included to compensate for possible mismatches between Q_3 and Q_4 and to guard against the possibility of thermal runaway due to temperature differences between the input- and output-stage transistors. The latter point can be appreciated by noting that an increase in the current of, say, Q_3 causes an increase in the voltage drop across R_3 and a corresponding decrease in V_{BE3} . Thus R_3 provides negative feedback that helps stabilize the current through Q_3 .

Because the circuit of Fig. 11.30 requires high-quality *pnp* transistors, it is not suitable for implementation in conventional monolithic IC technology. However, excellent results have been obtained with this circuit implemented in hybrid thick-film technology (Wong and Sherwin, 1979). This technology permits component trimming, for instance, to minimize the output offset voltage. The circuit can be used alone or together with an op amp to provide increased output driving capability. The latter application will be discussed in the next section.

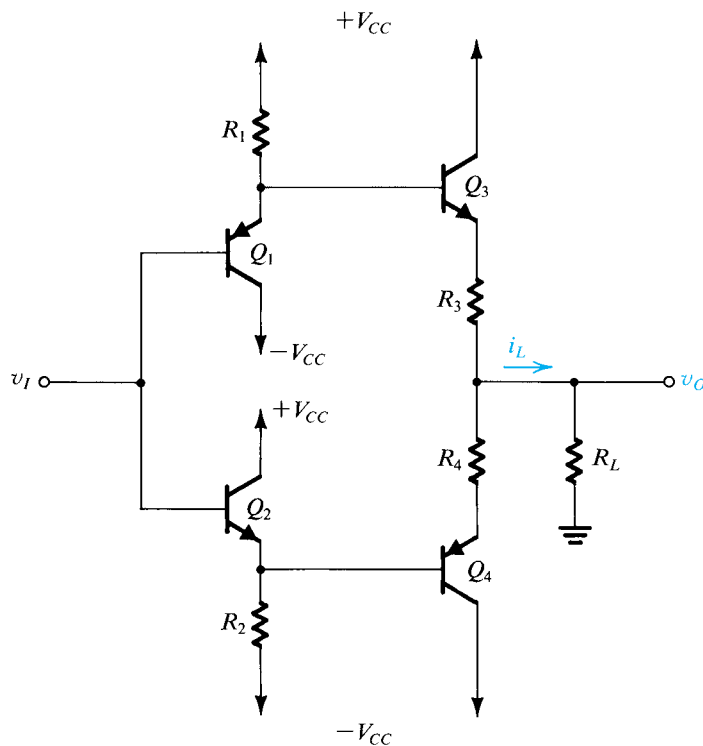


Figure 11.30 A class AB output stage with an input buffer. In addition to providing a high input resistance, the buffer transistors Q_1 and Q_2 bias the output transistors Q_3 and Q_4 .

EXERCISE

11.14 (Note: Although very instructive, this exercise is rather long.) Consider the circuit of Fig. 11.30 with $R_1 = R_2 = 5 \text{ k}\Omega$, $R_3 = R_4 = 0 \Omega$, and $V_{CC} = 15 \text{ V}$. Let the transistors be matched with $I_S = 3.3 \times 10^{-14} \text{ A}$ and $\beta = 200$. (These are the values used in the LH002 manufactured by National Semiconductor, except that $R_3 = R_4 = 2 \Omega$ there.) (a) For $v_i = 0$ and $R_L = \infty$, find the quiescent current in each of the four transistors and v_o . (b) For $R_L = \infty$, find i_{C1} , i_{C2} , i_{C3} , i_{C4} , and v_o for $v_i = +10 \text{ V}$ and -10 V . (c) Repeat (b) for $R_L = 100 \Omega$.

Ans. (a) 2.87 mA; 0 V; (b) for $v_i = +10 \text{ V}$: 0.88 mA, 4.87 mA, 1.95 mA, 1.95 mA, +9.98 V; for $v_i = -10 \text{ V}$: 4.87 mA, 0.88 mA, 1.95 mA, 1.95 mA, -9.98 V; (c) for $v_i = +10 \text{ V}$: 0.38 mA, 4.87 mA, 100 mA, 0.02 mA, +9.86 V; for $v_i = -10 \text{ V}$: 4.87 mA, 0.38 mA, 0.02 mA, 100 mA, -9.86 V

11.8.2 Use of Compound Devices

To increase the current gain of the output-stage transistors, and thus reduce the required base current drive, the Darlington configuration shown in Fig. 11.31 is frequently used to replace the *nnp* transistor of the class AB stage. The Darlington configuration is equivalent to a single *nnp* transistor having $\beta \approx \beta_1\beta_2$, but almost twice the value of V_{BE} .

The Darlington configuration can be also used for *pnp* transistors, and this is indeed done in discrete-circuit design. In IC design, however, the lack of good-quality *pnp* transistors prompted the use of the alternative compound configuration shown in Fig. 11.32. This compound device is equivalent to a single *pnp* transistor having $\beta \approx \beta_1\beta_2$. When fabricated with standard IC technology, Q_1 is usually a lateral *pnp* having a low β ($\beta = 5 - 10$) and poor high-frequency response ($f_T \approx 5 \text{ MHz}$); see Appendix A and Appendix 7.A. The compound device, although it has a relatively high equivalent β , still suffers from a poor high-frequency response. It also suffers from another problem: The feedback loop formed by Q_1 and Q_2 is prone to high-frequency oscillations (with frequency near f_T of the *pnp* device, i.e., about 5 MHz). Methods exist for preventing such oscillations. The subject of feedback-amplifier stability was studied in Chapter 10.

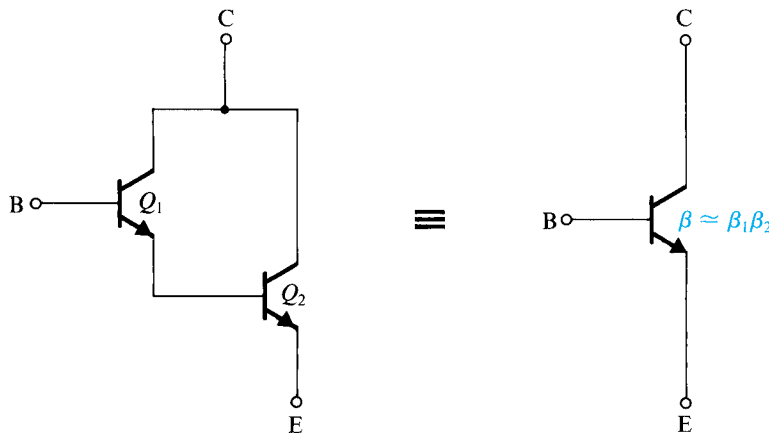


Figure 11.31 The Darlington configuration.

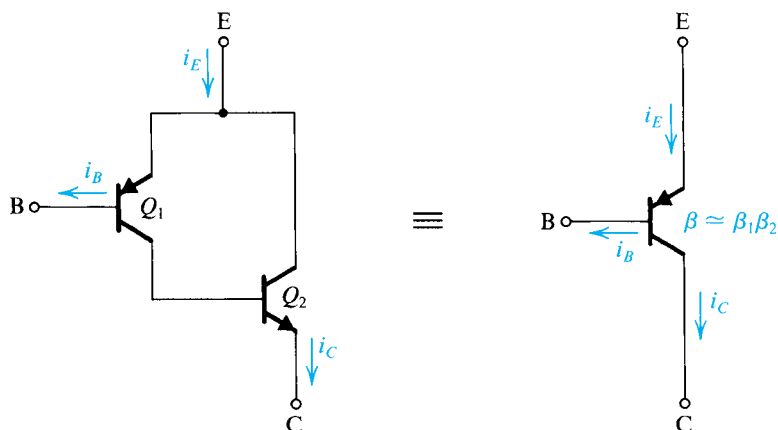


Figure 11.32 The compound-*pnp* configuration.

To illustrate the application of the Darlington configuration and of the compound *pnp*, we show in Fig. 11.33 an output stage utilizing both. Class AB biasing is achieved using a V_{BE} multiplier. Note that the Darlington *nnp* adds one more V_{BE} drop, and thus the V_{BE} multiplier is required to provide a bias voltage of about 2 V. The design of this class AB stage is investigated in Problem 11.43.

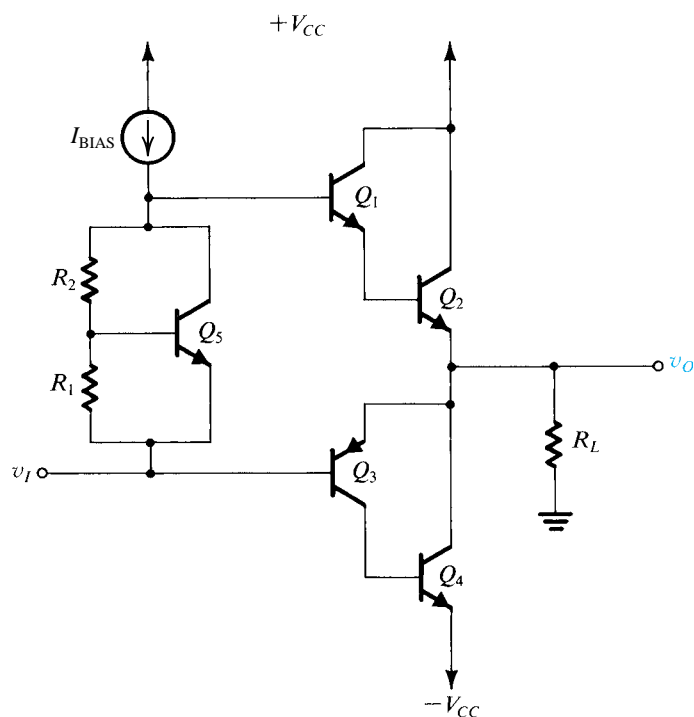


Figure 11.33 A class AB output stage utilizing a Darlington *nnp* and a compound *pnp*. Biasing is obtained using a V_{BE} multiplier.

EXERCISE

- 11.15** (a) Refer to Fig. 11.32. Show that, for the composite *pnp* transistor,

$$i_B \approx \frac{i_C}{\beta_N \beta_P}$$

and

$$i_E \approx i_C$$

Hence show that

$$i_C \approx \beta_N I_{SP} e^{v_{EB}/V_T}$$

and thus the transistor has an effective scale current

$$I_S = \beta_N I_{SP}$$

where I_{SP} is the saturation current of the *pnp* transistor Q_1 .

- (b) For $\beta_P = 20$, $\beta_N = 50$, $I_{SP} = 10^{-14}$ A, find the effective current gain of the compound device and its v_{EB} when $i_C = 100$ mA.

Ans. (b) 1000; 0.651 V

11.8.3 Short-Circuit Protection

Figure 11.34 shows a class AB output stage equipped with protection against the effect of short-circuiting the output while the stage is sourcing current. The large current that flows through Q_1 in the event of a short circuit will develop a voltage drop across R_{E1} of sufficient value to turn Q_5 on. The collector of Q_5 will then conduct most of the current I_{BIAS} , robbing Q_1 of its base drive. The current through Q_1 will thus be reduced to a safe operating level.

This method of short-circuit protection is effective in ensuring device safety, but it has the disadvantage that under normal operation about 0.5 V drop might appear across each R_E . This means that the voltage swing at the output will be reduced by that much, in each direction. On the other hand, the inclusion of emitter resistors provides the additional benefit of protecting the output transistors against thermal runaway.

EXERCISE

- D11.16** In the circuit of Fig. 11.34 let $I_{BIAS} = 2$ mA. Find the value of R_{E1} that causes Q_5 to turn on and absorb all 2 mA when the output current being sourced reaches 150 mA. For Q_5 , $I_S = 10^{-14}$ A. If the normal peak output current is 100 mA, find the voltage drop across R_{E1} and the collector current of Q_5 .

Ans. 4.3 Ω ; 430 mV; 0.3 μ A

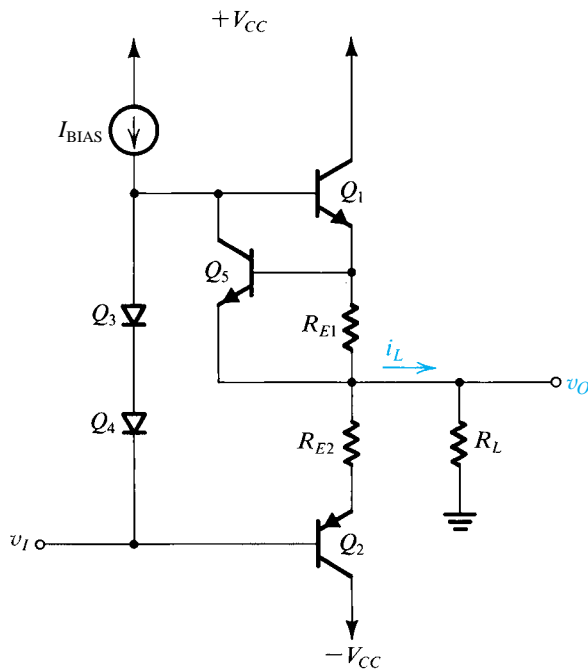


Figure 11.34 A class AB output stage with short-circuit protection. The protection circuit shown operates in the event of an output short circuit while v_o is positive.

11.8.4 Thermal Shutdown

In addition to short-circuit protection, most IC power amplifiers are usually equipped with a circuit that senses the temperature of the chip and turns on a transistor in the event that the temperature exceeds a safe preset value. The turned-on transistor is connected in such a way that it absorbs the bias current of the amplifier, thus virtually shutting down its operation.

Figure 11.35 shows a thermal-shutdown circuit. Here, transistor Q_2 is normally off. As the chip temperature rises, the combination of the positive temperature coefficient of zener diode Z_1 and the negative temperature coefficient of V_{BE1} causes the voltage at the emitter of Q_1 to rise. This in turn raises the voltage at the base of Q_2 to the point at which Q_2 turns on.

11.9 IC Power Amplifiers



A variety of IC power amplifiers are available. Most consist of a high-gain, small-signal amplifier followed by a class AB output stage. Some have overall negative feedback already applied, resulting in a fixed closed-loop voltage gain. Others do not have on-chip feedback and are, in effect, op amps with large output-power capability. In fact, the output current-driving capability of any general-purpose op amp can be increased by cascading it with a class B or class AB output stage and applying overall negative feedback. The additional output stage can be either a discrete circuit or a hybrid IC such as the buffer discussed in the preceding section. In the following we discuss some power-amplifier examples.

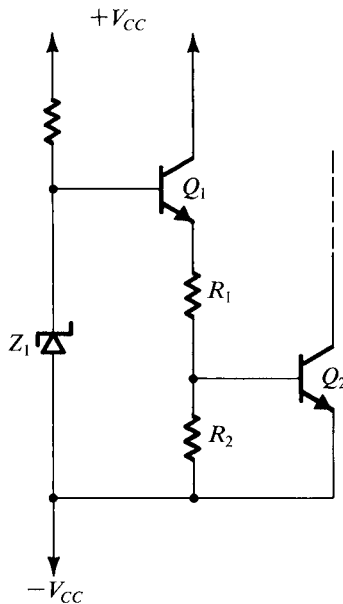


Figure 11.35 Thermal-shutdown circuit.

11.9.1 A Fixed-Gain IC Power Amplifier

Our first example is the LM380 (a product of National Semiconductor Corporation), which is a fixed-gain monolithic power amplifier. A simplified version of the internal circuit of the amplifier³ is shown in Fig. 11.36. The circuit consists of an input differential amplifier utilizing Q_1 and Q_2 as emitter followers for input buffering, and Q_3 and Q_4 as a differential pair with an emitter resistor R_3 . The two resistors R_4 and R_5 provide dc paths to ground for the base currents of Q_1 and Q_2 , thus enabling the input signal source to be capacitively coupled to either of the two input terminals.

The differential amplifier transistors Q_3 and Q_4 are biased by two separate currents: Q_3 is biased by a current from the dc supply V_S through the diode-connected transistor Q_{10} , and resistor R_1 ; Q_4 is biased by a dc current from the output terminal through R_2 . Under quiescent conditions (i.e., with no input signal applied) the two bias currents will be equal, and the current through and the voltage across R_3 will be zero. For the emitter current of Q_3 we can write

$$I_3 \approx \frac{V_S - V_{EB10} - V_{EB3} - V_{EB1}}{R_1}$$

where we have neglected the small dc voltage drop across R_4 . Assuming, for simplicity, all V_{EB} to be equal,

$$I_3 \approx \frac{V_S - 3V_{EB}}{R_1} \quad (11.76)$$

For the emitter current of Q_4 we have

$$I_4 = \frac{V_O - V_{EB4} - V_{EB2}}{R_2} \approx \frac{V_O - 2V_{EB}}{R_2} \quad (11.77)$$

³The main objective of showing this circuit is to point out some interesting design features. The circuit is *not* a detailed schematic diagram of what is actually on the chip.

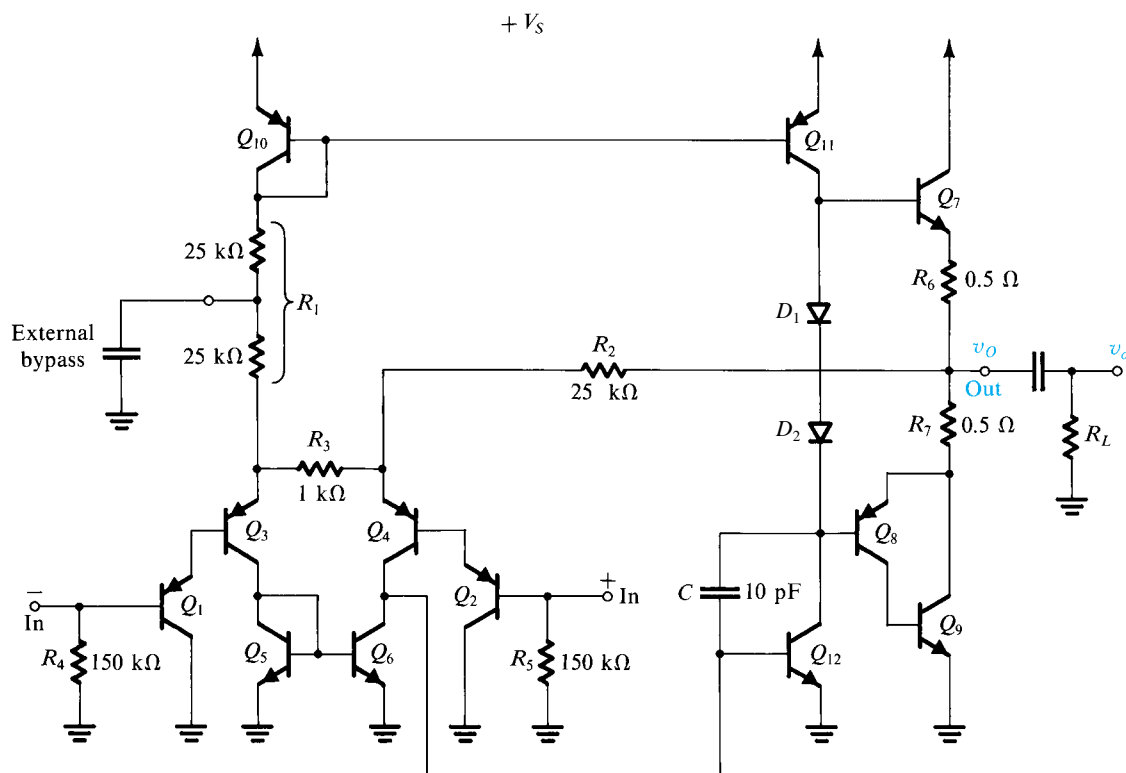


Figure 11.36 The simplified internal circuit of the LM380 IC power amplifier. (Courtesy National Semiconductor Corporation.)

where V_O is the dc voltage at the output, and we have neglected the small drop across R_5 . Equating I_3 and I_4 and using the fact that $R_1 = 2R_2$ results in

$$V_O = \frac{1}{2} V_S + \frac{1}{2} V_{EB} \quad (11.78)$$

Thus the output is biased at approximately half the power-supply voltage, as desired for maximum output voltage swing. An important feature is the dc feedback from the output to the emitter of Q_4 , through R_2 . This dc feedback acts to stabilize the output dc bias voltage at the value in Eq. (11.78). Qualitatively, the dc feedback functions as follows: If for some reason V_O increases, a corresponding current increment will flow through R_2 and into the emitter of Q_4 . Thus the collector current of Q_4 increases, resulting in a positive increment in the voltage at the base of Q_{12} . This, in turn, causes the collector current of Q_{12} to increase, thus bringing down the voltage at the base of Q_8 and hence V_O .

Continuing with the description of the circuit in Fig. 11.36, we observe that the differential amplifier (Q_3, Q_4) has a current mirror load composed of Q_5 and Q_6 (refer to Section 8.5 for a discussion of active loads). The single-ended output voltage signal of the first stage appears at the collector of Q_6 and thus is applied to the base of the second-stage common-emitter amplifier Q_{12} . Transistor Q_{12} is biased by the constant-current source Q_{11} , which also acts as its active load. In actual operation, however, the load of Q_{12} will be dominated by the reflected resistance due to R_L . Capacitor C provides frequency compensation (see Chapter 10).

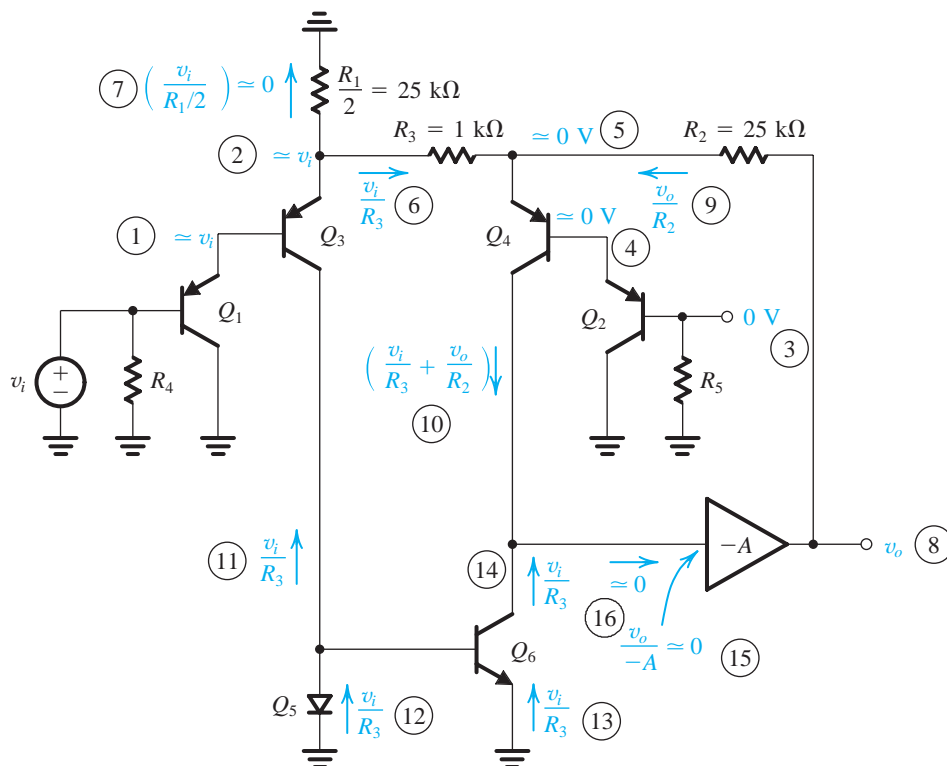


Figure 11.37 Small-signal analysis of the circuit in Fig. 11.36. The circled numbers indicate the order of the analysis steps.

The output stage is class AB, utilizing a compound *pnp* transistor (Q_8 and Q_9). Negative feedback is applied from the output to the emitter of Q_4 via resistor R_2 . To find the closed-loop gain consider the small-signal equivalent circuit shown in Fig. 11.37. Here, we have replaced the second-stage common-emitter amplifier and the output stage with an inverting amplifier block with gain A . We shall assume that the amplifier A has high gain and high input resistance, and thus the input signal current into A is negligibly small. Under this assumption, Fig. 11.37 shows the analysis details with an input signal v_i applied to the inverting input terminal. The order of the analysis steps is indicated by the circled numbers. Note that since the input differential amplifier has a relatively large resistance, R_3 , in the emitter circuit, most of the applied input voltage appears across R_3 . In other words, the signal voltages across the emitter–base junctions of Q_1 , Q_2 , Q_3 , and Q_4 are small in comparison to the voltage across R_3 . Accordingly, the voltage gain can be found by writing a node equation at the collector of Q_6 :

$$\frac{v_i}{R_3} + \frac{v_o}{R_2} + \frac{v_i}{R_3} = 0$$

which yields

$$\frac{v_o}{v_i} = -\frac{2R_2}{R_3} \approx -50 \text{ V/V}$$

EXERCISE

11.17 Denoting the total resistance between the collector of Q_6 and ground by R , show, using Fig. 11.37, that

$$\frac{v_o}{v_i} = \frac{-2R_2/R_3}{1 + (R_2/AR)}$$

which reduces to $(-2R_2/R_3)$ under the condition that $AR \gg R_2$.

As was demonstrated in Chapter 10, one of the advantages of negative feedback is the reduction of nonlinear distortion. This is the case in the circuit of the LM380.

The LM380 is designed to operate from a single supply V_S in the range of 12 V to 22 V. The selection of supply voltage depends on the value of R_L and the required output power P_L . The manufacturer supplies curves for the device power dissipation versus output power for a given load resistance and various supply voltages. One such set of curves for $R_L = 8 \Omega$ is shown in Fig. 11.38. Note the similarity to the class B power dissipation curve of Fig. 11.8. In fact, the reader can easily verify that the location and value of the peaks of the curves in Fig. 11.38 are accurately predicted by Eqs. (11.20) and (11.21), respectively (where $V_{CC} = \frac{1}{2}V_S$). The line labeled “3% distortion level” in Fig. 11.38 is the locus of the points on the various curves at which the distortion (THD) reaches 3%. A THD of 3% represents the onset of peak clipping due to output-transistor saturation.

The manufacturer also supplies curves for maximum power dissipation versus temperature (derating curves) similar to those discussed in Section 11.7 for discrete power transistors.

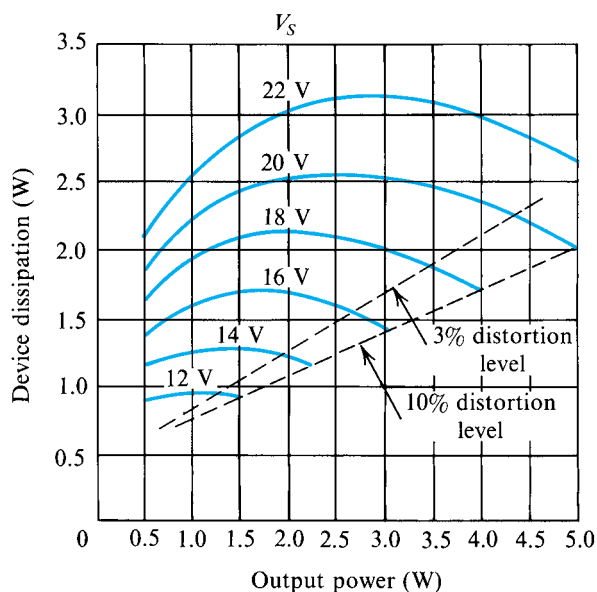


Figure 11.38 Power dissipation (P_D) versus output power (P_L) for the LM380 with $R_L = 8 \Omega$. (Courtesy National Semiconductor Corporation.)

EXERCISES

- 11.18** The manufacturer specifies that for ambient temperatures below 25°C the LM380 can dissipate a maximum of 3.6 W. This is obtained under the condition that its dual-in-line package be soldered onto a printed-circuit board in close thermal contact with 6 square inches of 2-ounce copper foil. Above $T_A = 25^\circ\text{C}$, the thermal resistance is $\theta_{JA} = 35^\circ\text{C/W}$. $T_{J\max}$ is specified to be 150°C . Find the maximum power dissipation possible if the ambient temperature is to be 50°C .

Ans. 2.9 W

- D11.19** It is required to use the LM380 to drive an $8\text{-}\Omega$ loudspeaker. Use the curves of Fig. 11.38 to determine the maximum power supply possible while limiting the maximum power dissipation to the 2.9 W determined in Exercise 11.18. If for this application a 3% THD is allowed, find P_L and the peak-to-peak output voltage.

Ans. 20 V; 4.2 W; 16.4 V

11.9.2 Power Op Amps

Figure 11.39 shows the general structure of a power op amp. It consists of a low-power op amp followed by a class AB buffer similar to that discussed in Section 11.8.1. The buffer consists of transistors Q_1 , Q_2 , Q_3 , and Q_4 , with bias resistors R_1 and R_2 and emitter degeneration resistors R_5 and R_6 . The buffer supplies the required load current until the current increases to the point that the voltage drop across R_3 (in the current-sourcing mode) becomes sufficiently large to turn Q_5 on. Transistor Q_5 then supplies the additional load current required. In the current-sinking mode, Q_4 supplies the load current until sufficient voltage develops across R_4 to turn Q_6 on. Then, Q_6 sinks the additional load current. Thus the stage formed by Q_5 and Q_6 acts as a **current booster**. The power op amp is intended to be used with negative feedback in the usual closed-loop configurations. A circuit based on the structure of Fig. 11.39 is commercially available from National Semiconductor as LH0101. This op amp is capable of providing a continuous output current of 2 A, and with appropriate heat sinking can provide 40 W of output power (Wong and Johnson, 1981). The LH0101 is fabricated using hybrid thick-film technology.

11.9.3 The Bridge Amplifier

We conclude this section with a discussion of a circuit configuration that is popular in high-power applications. This is the bridge-amplifier configuration shown in Fig. 11.40 utilizing two power op amps, A_1 and A_2 . While A_1 is connected in the noninverting configuration with a gain $K = 1 + (R_2/R_1)$, A_2 is connected as an inverting amplifier with a gain of equal magnitude $K = R_4/R_3$. The load R_L is floating and is connected between the output terminals of the two op amps.

If v_i is a sinusoid with amplitude \hat{V}_i , the voltage swing at the output of each op amp will be $\pm K\hat{V}_i$, and that across the load will be $\pm 2K\hat{V}_i$. Thus, with op amps operated from $\pm 15\text{-V}$ supplies and capable of providing, say a $\pm 12\text{-V}$ output swing, an output swing of $\pm 24\text{ V}$ can be obtained across the load of the bridge amplifier.

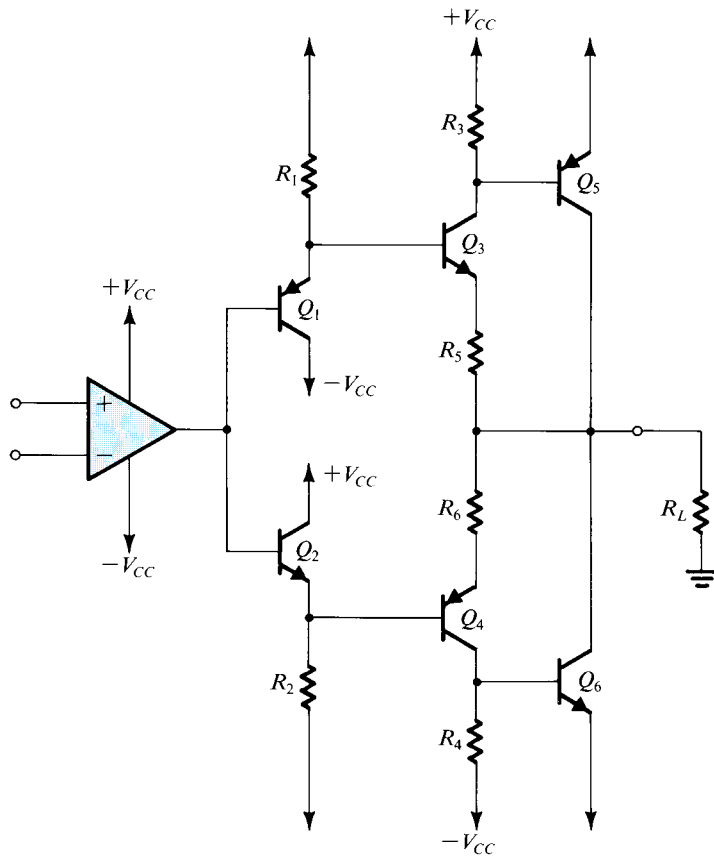


Figure 11.39 Structure of a power op amp. The circuit consists of an op amp followed by a class AB buffer similar to that discussed in Section 11.8.1. The output current capability of the buffer, consisting of Q_1 , Q_2 , Q_3 , and Q_4 , is further boosted by Q_5 and Q_6 .

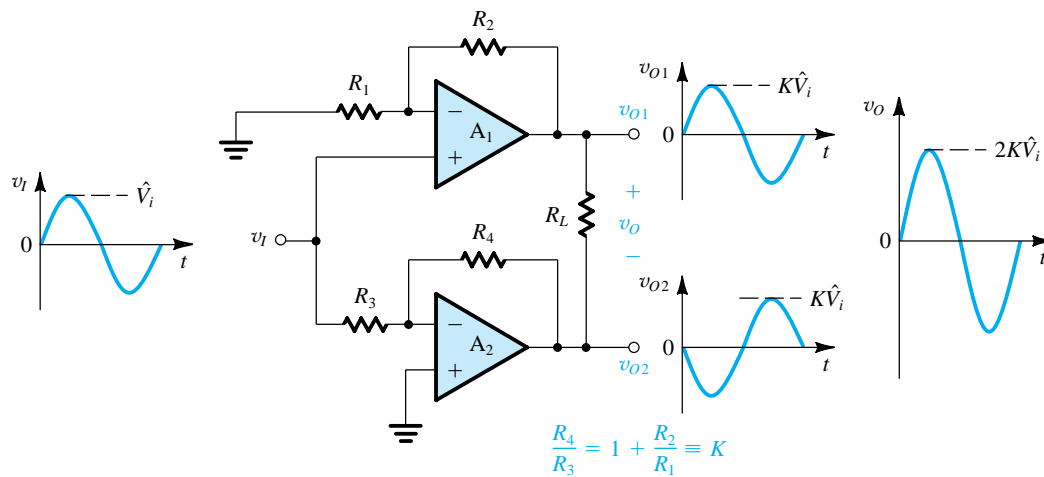


Figure 11.40 The bridge-amplifier configuration.

In designing bridge amplifiers, note should be taken of the fact that the peak current drawn from each op amp is $2K\hat{V}_i/R_L$. This effect can be taken into account by considering the load seen by each op amp (to ground) to be $R_L/2$.

EXERCISE

11.20 Consider the circuit of Fig. 11.40 with $R_1 = R_3 = 10\text{ k}\Omega$, $R_2 = 5\text{ k}\Omega$, $R_4 = 15\text{ k}\Omega$, and $R_L = 8\text{ }\Omega$. Find the voltage gain and the input resistance. The power supply used is $\pm 18\text{ V}$. If v_i is a 20-V peak-to-peak sine wave, what is the peak-to-peak output voltage? What is the peak load current? What is the load power?

Ans. 3 V/V; 10 k Ω ; 60 V; 3.75 A; 56.25 W

⊕ 11.10 MOS Power Transistors

In this section we consider the structure, characteristics, and application of a special type of MOSFET suitable for high-power applications.

11.10.1 Structure of the Power MOSFET

The MOSFET structure studied in Chapter 5 (Fig. 5.1) is not suitable for high-power applications. To appreciate this fact, recall that the drain current of an n -channel MOSFET operating in the saturation region is given by

$$i_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_t)^2 \quad (11.79)$$

It follows that to increase the current capability of the MOSFET, its width W should be made large and its channel length L should be made as small as possible. Unfortunately, however, reducing the channel length of the standard MOSFET structure results in a drastic reduction in its breakdown voltage. Specifically, the depletion region of the reverse-biased body-to-drain junction spreads into the short channel, resulting in breakdown at a relatively low voltage. Thus the resulting device would not be capable of handling the high voltages typical of power-transistor applications. For this reason, new structures had to be found for fabricating short-channel (1- to 2- μm) MOSFETs with high breakdown voltages.

At the present time the most popular structure for a power MOSFET is the **double-diffused** or **DMOS transistor** shown in Fig. 11.41. As indicated, the device is fabricated on a lightly doped n -type substrate with a heavily doped region at the bottom for the drain contact. Two diffusions⁴ are employed, one to form the p -type body region and another to form the n -type source region.

The DMOS device operates as follows. Application of a positive gate voltage, v_{GS} , greater than the threshold voltage V_t , induces a lateral n channel in the p -type body region underneath the gate oxide. The resulting channel is short; its length is denoted L in Fig. 11.41. Current is then conducted by electrons from the source moving through the resulting short channel to the substrate and then vertically down the substrate to the drain. This should be contrasted with the lateral current flow in the standard small-signal MOSFET structure (Chapter 5).

⁴See Appendix A for a description of the IC fabrication process.

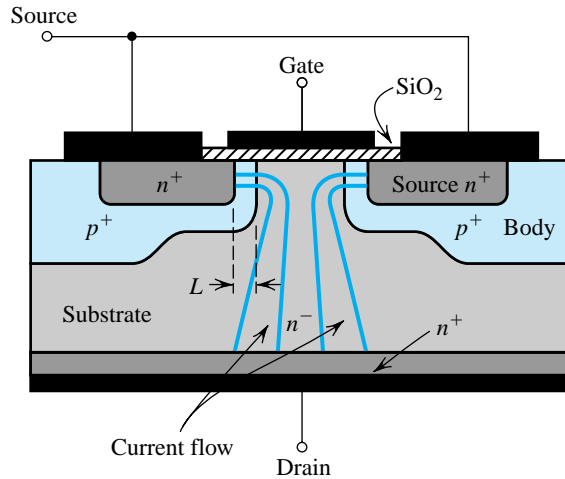


Figure 11.41 Double-diffused vertical MOS transistor (DMOS).

Even though the DMOS transistor has a short channel, its breakdown voltage can be very high (as high as 600 V). This is because the depletion region between the substrate and the body extends mostly in the lightly doped substrate and does not spread into the channel. The result is a MOS transistor that simultaneously has a high current capability (50 A is possible) as well as the high breakdown voltage just mentioned. Finally, we note that the vertical structure of the device provides efficient utilization of the silicon area.

An earlier structure used for power MOS transistors deserves mention. This is the V-groove MOS device [see Severns (1984)]. Although still in use, the **V-groove MOSFET** has lost application ground to the vertical DMOS structure of Fig. 11.41, except possibly for high-frequency applications. Because of space limitations, we shall not describe the V-groove MOSFET.

11.10.2 Characteristics of Power MOSFETs

In spite of their radically different structure, power MOSFETs exhibit characteristics that are quite similar to those of the small-signal MOSFETs studied in Chapter 5. Important differences exist, however, and these are discussed next.

Power MOSFETs have threshold voltages in the range of 2 V to 4 V. In saturation, the drain current is related to v_{GS} by the square-law characteristic of Eq. (11.80). However, as shown in Fig. 11.42, the i_D-v_{GS} characteristic becomes linear for larger values of v_{GS} . The linear portion of the characteristic occurs as a result of the high electric field along the short channel, causing the velocity of charge carriers to reach an upper limit, a phenomenon known as **velocity saturation**⁵. The linear i_D-v_{GS} relationship implies a constant g_m in the velocity-saturation region.

The i_D-v_{GS} characteristic shown in Fig. 11.42 includes a segment labeled “subthreshold.” Though of little significance for power devices, the subthreshold region of operation is of interest in very-low-power applications (see Section 5.1.9).

⁵Velocity saturation occurs also in standard MOSFET structures when the channel length is in the sub-micron range. We shall discuss velocity saturation in some detail in Section 13.5.

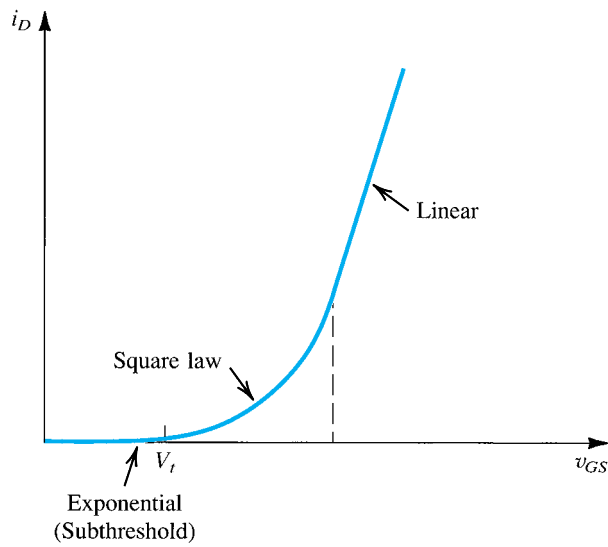


Figure 11.42 Typical i_D - v_{GS} characteristic for a power MOSFET.

11.10.3 Temperature Effects

Of considerable interest in the design of MOS power circuits is the variation of the MOSFET characteristics with temperature, illustrated in Fig. 11.43. Observe that there is a value of v_{GS} (in

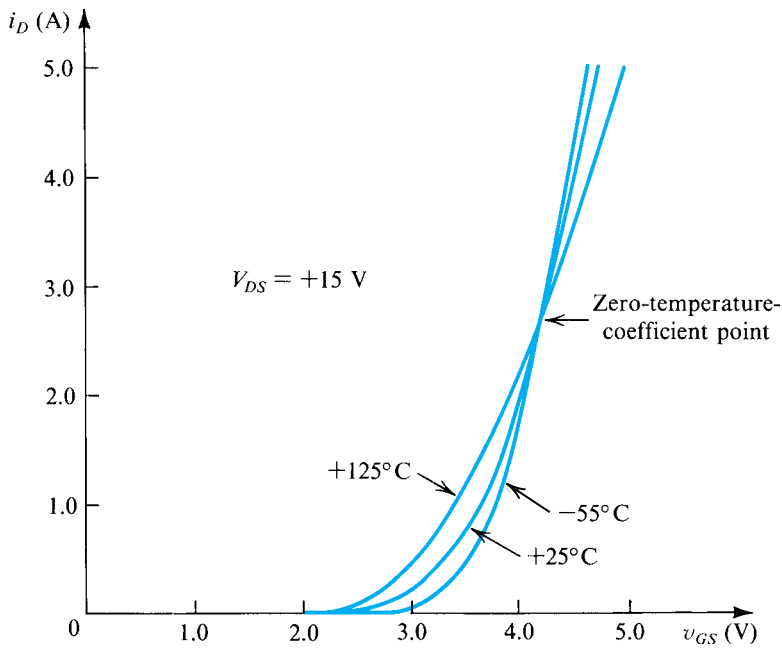


Figure 11.43 The i_D - v_{GS} characteristic curve of a power MOS transistor (IRF 630, Siliconix) at case temperatures of -55°C , $+25^\circ\text{C}$, and $+125^\circ\text{C}$. (Courtesy of Siliconix Inc.)

the range of 4 V to 6 V for most power MOSFETs) at which the temperature coefficient of i_D is zero. At higher values of v_{GS} , i_D exhibits a negative temperature coefficient. This is a significant property: It implies that a MOSFET operating beyond the zero-temperature-coefficient point does not suffer from the possibility of thermal runaway. This is *not* the case, however, at low currents (i.e., lower than the zero-temperature-coefficient point). In the (relatively) low-current region, the temperature coefficient of i_D is positive, and the power MOSFET can easily suffer thermal runaway (with unhappy consequences). Since class AB output stages are biased at low currents, means must be provided to guard against thermal runaway.

The reason for the positive temperature coefficient of i_D at low currents is that $v_{OV} = (v_{GS} - V_t)$ is relatively low, and the temperature dependence is dominated by the negative temperature coefficient of V_t (in the range of -3 mV/°C to -6 mV/°C) which causes v_{OV} to rise with temperature.

11.10.4 Comparison with BJTs

The power MOSFET does not suffer from second breakdown, which limits the safe operating area of BJTs. Also, power MOSFETs do not require the large dc base-drive currents of power BJTs. Note, however, that the driver stage in a MOS power amplifier should be capable of supplying sufficient current to charge and discharge the MOSFET's large and nonlinear input capacitance in the time allotted. Finally, the power MOSFET features, in general, a higher speed of operation than the power BJT. This makes MOS power transistors especially suited to switching applications—for instance, in motor-control circuits.

11.10.5 A Class AB Output Stage Utilizing Power MOSFETs

As an application of power MOSFETs, we show in Fig. 11.44 a class AB output stage utilizing a pair of complementary MOSFETs and employing BJTs for biasing and in the driver stage. The latter consists of complementary Darlington emitter followers formed by Q_1 through Q_4 and has the low output resistance necessary for driving the output MOSFETs at high speeds.

Of special interest in the circuit of Fig. 11.44 is the bias circuit utilizing two V_{BE} multipliers formed by Q_5 and Q_6 and their associated resistors. Transistor Q_6 is placed in direct thermal contact with the output transistors; this is achieved by simply mounting Q_6 on their common heat sink. Thus, by the appropriate choice of the V_{BE} multiplication factor of Q_6 , the bias voltage V_{GG} (between the gates of the output transistors) can be made to decrease with temperature at the same rate as that of the sum of the threshold voltages ($V_{tN} + |V_{tP}|$) of the output MOSFETs. In this way the overdrive voltages and hence the quiescent current of the output transistors can be stabilized against temperature variations.

Analytically, V_{GG} is given by

$$V_{GG} = \left(1 + \frac{R_3}{R_4}\right) V_{BE6} + \left(1 + \frac{R_1}{R_2}\right) V_{BE5} - 4V_{BE}$$

Since V_{BE6} is thermally coupled to the output devices while the other BJTs remain at constant temperature, we have

$$\frac{\partial V_{GG}}{\partial T} = \left(1 + \frac{R_3}{R_4}\right) \frac{\partial V_{BE6}}{\partial T}$$

which is the relationship needed to determine R_3/R_4 so that $\partial V_{GG}/\partial T = \partial(V_{tN} + |V_{tP}|)/\partial T$. The other V_{BE} multiplier is then adjusted to yield the value of V_{GG} required for the desired quiescent current in Q_N and Q_P .

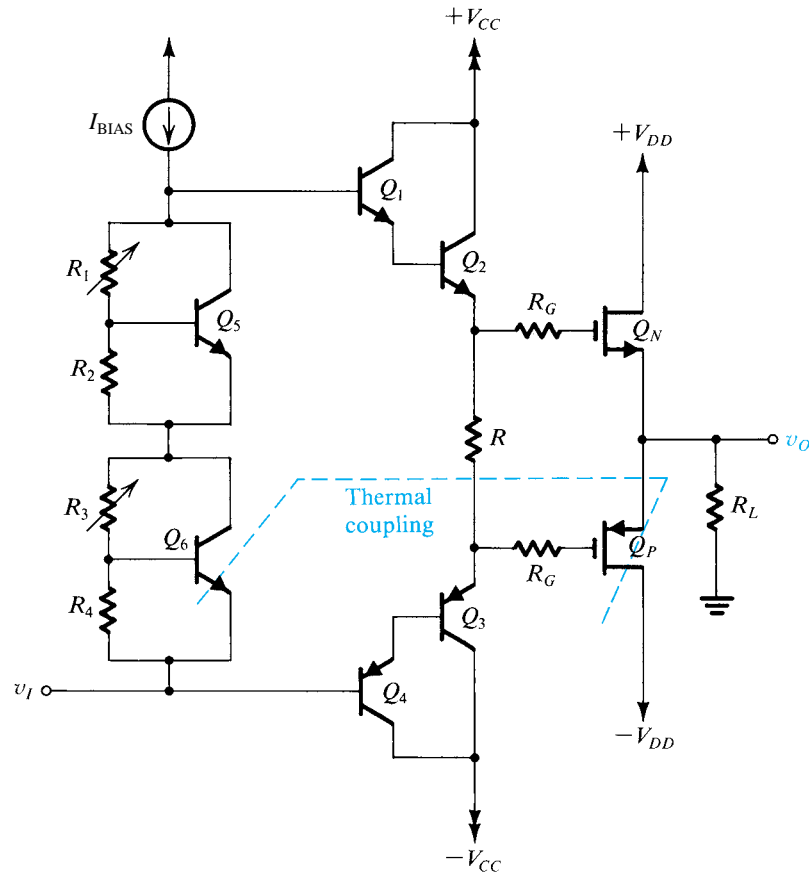


Figure 11.44 A class AB amplifier with MOS output transistors and BJT drivers. Resistor R_3 is adjusted to provide temperature compensation while R_1 is adjusted to yield the desired value of quiescent current in the output transistors. Resistors R_G are used to suppress parasitic oscillations at high frequencies. Typically, $R_G = 100\ \Omega$.

EXERCISES

11.21 For the circuit in Fig. 11.44, find the ratio R_3/R_4 that provides temperature stabilization of the quiescent current in Q_N and Q_P . Assume that $|V_t|$ changes at $-3\text{ mV}/^\circ\text{C}$ and that $\partial V_{BE}/\partial T = -2\text{ mV}/^\circ\text{C}$.
Ans. 2

11.22 For the circuit in Fig. 11.44 assume that the BJTs have a nominal V_{BE} of 0.7 V and that the MOSFETs have $|V_t| = 3\text{ V}$ and $\mu_n C_{ox}(W/L) = 2\text{ A/V}^2$. It is required to establish a quiescent current of 100 mA in the output stage and 20 mA in the driver stage. Find $|V_{GS}|$, V_{GG} , R , and R_1/R_2 . Use the value of R_3/R_4 found in Exercise 11.21. Assume that the MOSFETs are represented by their square-law i_D-v_{GS} characteristics.
Ans. 3.32 V ; 6.64 V ; $332\ \Omega$; 9.5

Summary

- Output stages are classified according to the transistor conduction angle: class A (360°), class AB (slightly more than 180°), class B (180°), and class C (less than 180°).
- The most common class A output stage is the emitter follower. It is biased at a current greater than the peak load current.
- The class A output stage dissipates its maximum power under quiescent conditions ($v_o = 0$). It achieves a maximum power-conversion efficiency of 25%.
- The class B stage is biased at zero current, and thus dissipates no power in quiescence.
- The class B stage can achieve a power conversion efficiency as high as 78.5%. It dissipates its maximum power for $\hat{V}_o = (2/\pi)V_{CC}$.
- The class B stage suffers from crossover distortion.
- The class AB output stage is biased at a small current; thus both transistors conduct for small input signals, and crossover distortion is virtually eliminated.
- Except for an additional small quiescent power dissipation, the power relationships of the class AB stage are similar to those in class B.
- To guard against the possibility of thermal runaway, the bias voltage of the class AB circuit is made to vary with temperature in the same manner as does V_{BE} of the output transistors.
- The classical CMOS class AB output stage suffers from reduced output signal-swing. This problem can be overcome by replacing the source-follower output transistors with a pair of complementary devices operating in the common-source configuration.
- The CMOS class AB output stage with common-source transistors allows the output voltage to swing to within an overdrive voltage from each of the two power

supplies. Utilizing error amplifiers in the feedback path of each of the output transistors reduces both the output resistance and gain error of the stage.

- To facilitate the removal of heat from the silicon chip, power devices are usually mounted on heat sinks. The maximum power that can be safely dissipated in the device is given by

$$P_{D\max} = \frac{T_{j\max} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

where $T_{j\max}$ and θ_{JC} are specified by the manufacturer, while θ_{CS} and θ_{SA} depend on the heat-sink design.

- Use of the Darlington configuration in the class AB output stage reduces the base-current drive requirement. In integrated circuits, the compound *pnp* configuration is commonly used.
- Output stages are usually equipped with circuitry that, in the event of a short circuit, can turn on and limit the base-current drive, and hence the emitter current, of the output transistors.
- IC power amplifiers consist of a small-signal voltage amplifier cascaded with a high-power output stage. Overall feedback is applied either on-chip or externally.
- The bridge amplifier configuration provides, across a floating load, a peak-to-peak output voltage which is twice that possible from a single amplifier with a grounded load.
- The DMOS transistor is a short-channel power device capable of both high-current and high-voltage operation.
- The drain current of a power MOSFET exhibits a positive temperature coefficient at low currents, and thus the device can suffer thermal runaway. At high currents the temperature coefficient of i_D is negative.

Computer Simulation Problems

SIM Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multism simulations for all the indicated problems can be found in the corresponding files on the disc. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

* difficult problem; ** more difficult; *** very challenging and/or time-consuming; D: design problem.

Section 11.2: Class A Output Stage

11.1 A class A emitter follower, biased using the circuit shown in Fig. 11.2, uses $V_{CC} = 5\text{ V}$, $R = R_L = 1\text{ k}\Omega$, with all transistors (including Q_3) identical. Assume $V_{BE} = 0.7\text{ V}$, $V_{CEsat} = 0.3\text{ V}$, and β to be very large. For linear operation, what are the upper and lower limits of output voltage, and the corresponding inputs? How do these values change if the emitter-base junction area of Q_3 is made twice as big as that of Q_2 ? Half as big?

11.2 A source-follower circuit using NMOS transistors is constructed following the pattern shown in Fig. 11.2. All three transistors used are identical, with $V_t = 1\text{ V}$ and $\mu_n C_{ox} W/L = 20\text{ mA/V}^2$; $V_{CC} = 5\text{ V}$, $R = R_L = 1\text{ k}\Omega$. For linear operation, what are the upper and lower limits of the output voltage, and the corresponding inputs?

D 11.3 Using the follower configuration shown in Fig. 11.2 with $\pm 9\text{-V}$ supplies, provide a design capable of $\pm 7\text{-V}$ outputs with a $1\text{-k}\Omega$ load, using the smallest possible total supply current. You are provided with four identical, high- β BJTs and a resistor of your choice.

D 11.4 An emitter follower using the circuit of Fig. 11.2, for which the output voltage range is $\pm 5\text{ V}$, is required using $V_{CC} = 10\text{ V}$. The circuit is to be designed such that the current variation in the emitter-follower transistor is no greater than a factor of 10, for load resistances as low as $100\ \Omega$. What is the value of R required? Find the incremental voltage gain of the resulting follower at $v_o = +5, 0$, and -5 V , with a $100\text{-}\Omega$ load. What is the percentage change in gain over this range of v_o ?

***11.5** Consider the operation of the follower circuit of Fig. 11.2 for which $R_L = V_{CC}/I$, when driven by a square wave such that the output ranges from $+V_{CC}$ to $-V_{CC}$ (ignoring V_{CEsat}). For this situation, sketch the equivalent of Fig. 11.4 for v_o , i_{C1} , and p_{D1} . Repeat for a square-wave output that has peak levels of $\pm V_{CC}/2$. What is the average power dissipation in Q_1 in each case? Compare these results to those for sine waves of peak amplitude V_{CC} and $V_{CC}/2$, respectively.

11.6 Consider the situation described in Problem 11.5. For square-wave outputs having peak-to-peak values of $2V_{CC}$ and V_{CC} , and for sine waves of the same peak-to-peak values, find the average power loss in the current-source transistor Q_2 .

11.7 Reconsider the situation described in Exercise 11.3 for variation in V_{CC} —specifically for $V_{CC} = 16\text{ V}$, 12 V , 10 V , and 8 V . Assume V_{CEsat} is nearly zero. What is the power-conversion efficiency in each case?

Section 11.3: Class B Output Stage

11.8 Consider the circuit of a complementary-BJT class B output stage. For what amplitude of input signal does the crossover distortion represent a 10% loss in peak amplitude?

11.9 Consider the feedback configuration with a class B output stage shown in Fig. 11.9. Let the amplifier gain $A_0 = 100\text{ V/V}$. Derive an expression for v_o versus v_i , assuming that $|V_{BE}| = 0.7\text{ V}$. Sketch the transfer characteristic v_o versus v_i , and compare it with that without feedback.

SIM 11.10 Consider the class B output stage, using enhancement MOSFETs, shown in Fig. P11.10. Let the devices have $|V_t| = 0.5\text{ V}$ and $\mu C_{ox} W/L = 2\text{ mA/V}^2$. With a 10-kHz sine-wave input of 5-V peak and a high value of load resistance, what peak output would you expect? What fraction of the sine-wave period does the crossover interval represent? For what value of load resistor is the peak output voltage reduced to half the input?

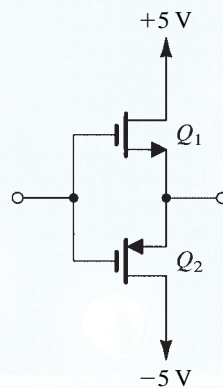


Figure P11.10

11.11 Consider the complementary-BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat} . For $\pm 10\text{-V}$ power supplies and a $100\text{-}\Omega$ load resistance, what is the maximum sine-wave output power available? What supply power corresponds? What is the power-conversion efficiency? For output signals of half this amplitude, find the output power, the supply power, and the power-conversion efficiency.

D 11.12 A class B output stage operates from $\pm 5\text{-V}$ supplies. Assuming relatively ideal transistors, what is the output voltage

for maximum power-conversion efficiency? What is the output voltage for maximum device dissipation? If each of the output devices is individually rated for 1-W dissipation, and a factor-of-2 safety margin is to be used, what is the smallest value of load resistance that can be tolerated, if operation is always at full output voltage? If operation is allowed at half the full output voltage, what is the smallest load permitted? What is the greatest possible output power available in each case?

D 11.13 A class B output stage is required to deliver an average power of 100 W into a 16- Ω load. The power supply should be 4 V greater than the corresponding peak sine-wave output voltage. Determine the power-supply voltage required (to the nearest volt in the appropriate direction), the peak current from each supply, the total supply power, and the power-conversion efficiency. Also, determine the maximum possible power dissipation in each transistor for a sine-wave input.

11.14 Consider the class B BJT output stage with a square-wave output voltage of amplitude \hat{V}_o across a load R_L and employing power supplies $\pm V_{SS}$. Neglecting the effects of finite V_{BE} and V_{CEsat} , determine the load power, the supply power, the power-conversion efficiency, the maximum attainable power-conversion efficiency and the corresponding value of \hat{V}_o , and the maximum available load power. Also find the value of \hat{V}_o at which the power dissipation in the transistors reaches its peak, and the corresponding value of power-conversion efficiency.

Section 11.4: Class AB Output Stage

D 11.15 Design the quiescent current of a class AB BJT output stage so that the incremental voltage gain for v_i in the vicinity of the origin is in excess of 0.98 V/V for loads larger than 100 Ω . Assume that the BJTs have V_{BE} of 0.7 V at a current of 100 mA and determine the value of V_{BB} required.

11.16 For the class AB output stage considered in Example 11.3, add two columns to the table of results as follows: the total input current drawn from v_i (i_I , mA); and the large-signal input resistance $R_{in} \equiv v_i/i_I$. Assume $\beta_N = \beta_P = \beta = 49$. Compare the values of R_{in} to the approximate value obtained using the resistance reflection rule, $R_{in} \approx \beta R_L$.

11.17 In this problem we investigate an important trade-off in the design of the class AB output stage of Fig. 11.11: Increasing the quiescent current I_Q reduces the nonlinearity of the transfer characteristic at the expense of increased quiescent power dissipation. As a measure of nonlinearity, we use the maximum deviation of the stage incremental gain, which occurs at $v_o = 0$, namely

$$\mathcal{E} = 1 - v_o/v_i|_{v_o=0}$$

(a) Show that \mathcal{E} is given by

$$\mathcal{E} = \frac{V_T/2I_Q}{R_L + (V_T/2I_Q)}$$

which for $2I_Q R_L \gg V_T$ can be approximated by

$$\mathcal{E} \approx V_T/2I_Q R_L$$

(b) If the stage is operated from power supplies of $\pm 2V_{CC}$, find the quiescent power dissipation, P_D .

(c) Show that for given V_{CC} and R_L , the product of the quiescent power dissipation and the gain error is a constant given by

$$\mathcal{E} P_D \approx V_T \left(\frac{V_{CC}}{R_L} \right)$$

(d) For $V_{CC} = 15$ V and $R_L = 100$ Ω , find the required values of P_D and I_Q if \mathcal{E} is to be 5%, 2%, and 1%.

***11.18** A class AB output stage, resembling that in Fig. 11.11 but utilizing a single supply of +10 V and biased at $V_I = 6$ V, is capacitively coupled to a 100- Ω load. For transistors for which $|V_{BE}| = 0.7$ V at 1 mA and for a bias voltage $V_{BB} = 1.4$ V, what quiescent current results? For a step change in output from 0 to -1 V, what input step is required? Assuming transistor saturation voltages of zero, find the largest possible positive-going and negative-going steps at the output.

Section 11.5: Biasing the Class AB Circuit

D 11.19 Consider the diode-biased class AB circuit of Fig. 11.14. For $I_{BIAS} = 100$ μ A, find the relative size (n) that should be used for the output devices (in comparison to the biasing devices) to ensure that an output resistance of 10 Ω or less is obtained in the quiescent state. Neglect the resistance of the biasing diodes.

D *11.20 A class AB output stage using a two-diode bias network as shown in Fig. 11.14 utilizes diodes having the same junction area as the output transistors. For $V_{CC} = 10$ V, $I_{BIAS} = 0.5$ mA, $R_L = 100$ Ω , $\beta_N = 50$, and $|V_{CEsat}| = 0$ V, what is the quiescent current? What are the largest possible positive and negative output signal levels? To achieve a positive peak output level equal to the negative peak level, what value of β_N is needed if I_{BIAS} is not changed? What value of I_{BIAS} is needed if β_N is held at 50? For this value, what does I_Q become?

****11.21** A class AB output stage using a two-diode bias network as shown in Fig. 11.14 utilizes diodes having the same junction area as the output transistors. At a room temperature of about 20°C the quiescent current is 1 mA and $|V_{BE}| = 0.6$ V. Through a manufacturing error, the thermal coupling between the output transistors and the biasing diode-connected transistors is omitted. After some output activity, the output devices heat up to 70°C while the biasing devices remain at 20°C. Thus, while the V_{BE} of each device remains unchanged, the quiescent current in the output devices increases. To calculate the new current value, recall that there are two effects: I_S increases by about 14%/°C and $V_T = kT/q$ changes, where $T = (273^\circ +$

temperature in °C), and $V_T = 25$ mV only at 20°C. However, you may assume that β_n remains almost constant. This assumption is based on the fact that β increases with temperature but decreases with current. What is the new value of I_Q ? If the power supply is ± 20 V, what additional power is dissipated? If thermal runaway occurs, and the temperature of the output transistors increases by 10°C for every watt of additional power dissipation, what additional temperature rise and current increase result?

D 11.22 Repeat Example 11.5 for the situation in which the peak positive output current is 200 mA. Use the same general approach to safety margins. What are the values of R_1 and R_2 you have chosen?

****11.23** A V_{BE} multiplier is designed with equal resistances for nominal operation at a terminal current of 1 mA, with half the current flowing in the bias network. The initial design is based on $\beta = \infty$ and $V_{BE} = 0.7$ V at 1 mA.

- Find the required resistor values and the terminal voltage.
- Find the terminal voltage that results when the terminal current increases to 2 mA. Assume $\beta = \infty$.
- Repeat (b) for the case the terminal current becomes 10 mA.
- Repeat (c) using the more realistic value of $\beta = 100$.

Section 11.6: CMOS Class AB Output Stages

D 11.24 (a) Show that for the class AB circuit in Fig. 11.17, the small-signal output resistance in the quiescent state is given by

$$R_{out} = \frac{1}{g_{mn} + g_{mp}}$$

which for matched devices becomes

$$R_{out} = \frac{1}{2g_m}$$

(b) For a circuit that utilizes MOSFETs with $|V_t| = 0.7$ V and $k'(W/L) = 200$ mA/V², find the voltage V_{GG} that results in $R_{out} = 10$ Ω .

D 11.25 (a) For the circuit in Fig. 11.17 in which Q_1 and Q_2 are matched, and Q_N and Q_P are matched, show that the small-signal voltage gain at the quiescent condition is given by

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + (2/g_m)}$$

where g_m is the transconductance of each of Q_N and Q_P and where channel-length modulation is neglected.

(b) For the case $I_{BIAS} = 0.1$ mA, $R_L = 1$ k Ω , $k_n = k_p = nk_1 = nk_2$, where $k = \mu C_{ox}(W/L)$, and $k_1 = 20$ mA/V², find the ratio n that results in an incremental gain of 0.98. Also find the quiescent current I_Q .

D 11.26 Design the circuit of Fig. 11.17 to operate at $I_{Q2} = 1$ mA with $I_{BIAS} = 0.1$ mA. Let $\mu_n C_{ox} = 250$ μ A/V²,

$\mu_p C_{ox} = 100$ μ A/V², $V_{tn} = -V_{tp} = 0.45$ V, and $V_{DD} = V_{SS} = 2.5$ V. Design so that Q_1 and Q_2 are matched and Q_N and Q_P are matched, and that in the quiescent state each operates at an overdrive voltage of 0.2 V.

- Specify the W/L ratio for each of the four transistors.
- In the quiescent state with $v_o = 0$, what must v_i be?
- If Q_N is required to supply a maximum load current of 10 mA, find the maximum allowable output voltage. Assume that the transistor supplying I_{BIAS} needs a minimum of 0.2 V to operate properly.

11.27 For the CMOS output stage of Fig. 11.19 with $I_Q = 3$ mA, $|V_{OV}| = 0.15$ V for each of Q_P and Q_N at the quiescent point, and $\mu = 5$, find the output resistance at the quiescent point.

11.28 (a) Show that for the CMOS output stage of Fig. 11.19,

$$|\text{Gain error}| = \frac{R_{out}}{R_L}$$

(b) For a stage that drives a load resistance of 100 Ω with a gain error of less than 5%, find the overdrive voltage at which Q_P and Q_N should be operated. Let $I_Q = 1$ mA and $\mu = 10$.

D 11.29 It is required to design the circuit of Fig. 11.19 to drive a load resistance of 50 Ω while exhibiting an output resistance, around the quiescent point, of 2.5 Ω . Operate Q_N and Q_P at $I_Q = 1.5$ mA and $|V_{OV}| = 0.15$ V. The technology utilized is specified to have $k'_n = 250$ μ A/V², $k'_p = 100$ μ A/V², $V_{tn} = -V_{tp} = 0.5$ V, and $V_{DD} = V_{SS} = 2.5$ V.

- Specify (W/L) for each of Q_N and Q_P .
- Specify the required value of μ .
- What is the expected error in the stage gain?
- In the quiescent state, what dc voltage must appear at the output of each of the error amplifiers?
- At what value of positive v_o will Q_P be supplying all the load current? Repeat for negative v_o and Q_N supplying all the load current.
- What is the linear range of v_o ?

Section 11.7: Power BJTs

D 11.30 A particular transistor having a thermal resistance $\theta_{JA} = 2^\circ\text{C/W}$ is operating at an ambient temperature of 30°C with a collector–emitter voltage of 20 V. If long life requires a maximum junction temperature of 130°C, what is the corresponding device power rating? What is the greatest average collector current that should be considered?

11.31 A particular transistor has a power rating at 25°C of 200 mW, and a maximum junction temperature of 150°C. What is its thermal resistance? What is its power rating when operated at an ambient temperature of 70°C? What is

its junction temperature when dissipating 100 mW at an ambient temperature of 50°C?

11.32 A power transistor operating at an ambient temperature of 50°C, and an average emitter current of 3 A, dissipates 30 W. If the thermal resistance of the transistor is known to be less than 3°C/W, what is the greatest junction temperature you would expect? If the transistor V_{BE} measured using a pulsed emitter current of 3 A at a junction temperature of 25°C is 0.80 V, what average V_{BE} would you expect under normal operating conditions? (Use a temperature coefficient of -2 mV/°C.)

11.33 For a particular application of the transistor specified in Example 11.7, extreme reliability is essential. To improve reliability, the maximum junction temperature is to be limited to 100°C. What are the consequences of this decision for the conditions specified?

11.34 A power transistor is specified to have a maximum junction temperature of 130°C. When the device is operated at this junction temperature with a heat sink, the case temperature is found to be 90°C. The case is attached to the heat sink with a bond having a thermal resistance $\theta_{CS} = 0.5^\circ\text{C/W}$ and the thermal resistance of the heat sink $\theta_{SA} = 0.1^\circ\text{C/W}$. If the ambient temperature is 30°C what is the power being dissipated in the device? What is the thermal resistance of the device, θ_{JC} , from junction to case?

11.35 A power transistor for which $T_{j\max} = 180^\circ\text{C}$ can dissipate 50 W at a case temperature of 50°C. If it is connected to a heat sink using an insulating washer for which the thermal resistance is 0.6°C/W , what heat-sink temperature is necessary to ensure safe operation at 30 W? For an ambient temperature of 39°C, what heat-sink thermal resistance is required? If, for a particular extruded-aluminum-finned heat sink, the thermal resistance in still air is 4.5°C/W per centimeter of length, how long a heat sink is needed?

Section 11.8: Variations on the Class AB Configuration

11.36 Use the results given in the answer to Exercise 11.14 to determine the input current of the circuit in Fig. 11.30 for $v_I = 0$ and ± 10 V with infinite and 100- Ω loads.

11.37 For the circuit in Fig. 11.30 when operated near $v_I = 0$ and fed with a signal source having zero resistance, show that the output resistance is given by

$$R_{\text{out}} = \frac{1}{2}[R_3 + r_{e3} + (R_1 \parallel r_{e1})/(\beta_3 + 1)]$$

Assume that the top and bottom halves of the circuit are perfectly matched.

D *11.38** Consider the circuit of Fig. 11.30 in which Q_1 and Q_2 are matched, and Q_3 and Q_4 are matched but have

three times the junction area of the others. For $V_{CC} = 10$ V, find values for resistors R_1 through R_4 which allow for a base current of at least 10 mA in Q_3 and Q_4 at $v_I = +5$ V (when a load demands it) with at most a 2-to-1 variation in currents in Q_1 and Q_2 , and a no-load quiescent current of 40 mA in Q_3 and Q_4 ; $\beta_{1,2} \geq 150$, and $\beta_{3,4} \geq 50$. For input voltages around 0 V, estimate the output resistance of the overall follower driven by a source having zero resistance. For an input voltage of +1 V and a load resistance of 2 Ω , what output voltage results? Q_1 and Q_2 have $|V_{BE}|$ of 0.7 V at a current of 10 mA.

11.39 Figure P11.39 shows a variant of the class AB circuit of Fig. 11.30. Assume that all four transistors are matched and have $\beta = 100$.

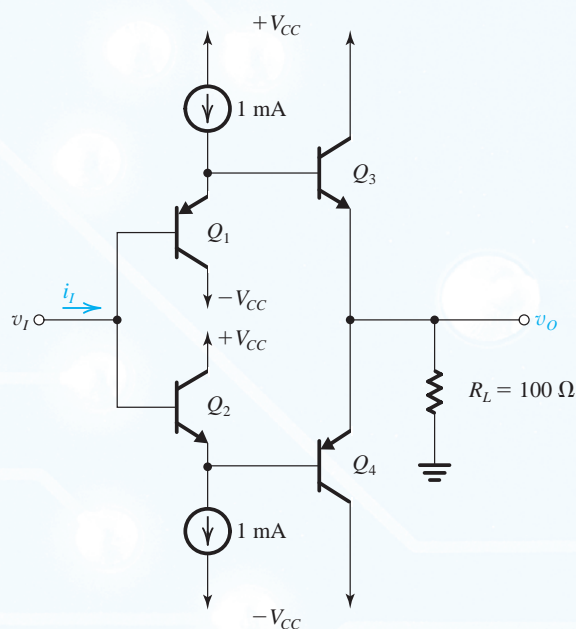


Figure P11.39

(a) For $v_I = 0$, find the quiescent current in Q_3 and Q_4 , the input current i_I , and the output voltage v_O .

(b) Since the circuit has perfect symmetry, the small-signal performance around $v_I = 0$ can be determined by considering either the top or bottom half of the circuit only. In this case, the load on the half-circuit must be $2R_L$, the input resistance found is $2R_{\text{in}}$, and the output resistance found is $2R_{\text{out}}$. Using this approach, find R_{in} , v_O/v_I , and R_{out} (assuming that the circuit is fed with a zero-resistance source).

11.40 For the Darlington configuration shown in Fig. 11.31, show that for $\beta_1 \gg 1$ and $\beta_2 \gg 1$:

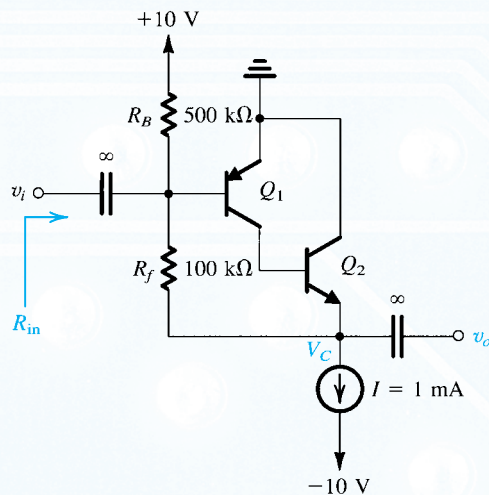
- The equivalent composite transistor has $\beta \approx \beta_1\beta_2$.
- If the composite transistor is operated at a current I_C , then Q_2 will be operating at a collector current approximately

(e) The composite transistor has an equivalent $g_m \approx \frac{1}{2}(I_C/V_T)$.

- Find the dc collector current for each of Q_1 and Q_2 .
- Find the small-signal current i_c that results from an input signal v_i , and hence find the voltage gain v_o/v_i .
- Find the input resistance R_{in} .

$$\frac{v_o}{v_i} \cong g_{m1}[r_{o1} \parallel \beta_N(r_{o2} \parallel R_f)]$$

D **11.43 Consider the compound-transistor class AB output stage shown in Fig. 11.33 in which Q_2 and Q_4 are matched transistors with $V_{BE} = 0.7$ V at 10 mA and $\beta = 100$, Q_1 and Q_5 have $V_{BE} = 0.7$ V at 1-mA currents and $\beta = 100$, and Q_3 has $V_{EB} = 0.7$ V at a 1-mA current and $\beta = 10$. Design the circuit for a quiescent current of 2 mA in Q_2 and Q_4 , I_{BIAS} that is 100 times the standby base current in Q_1 , and a current in Q_5 that is nine times that in the associated resistors. Find the values of the input voltage required to produce outputs of ± 10 V for a 1-k Ω load. Use V_{CC} of 15 V.



D 11.46 The circuit shown in Fig. P11.46 operates in a manner analogous to that in Fig. 11.35 to limit the output current from Q_3 in the event of a short circuit or other mishap. It has the advantage that the current-sensing resistor R does not appear directly at the output. Find the value of R that causes Q_5 to turn on and absorb all of $I_{\text{BIAS}} = 2 \text{ mA}$, when the current being sourced reaches 150 mA . For Q_5 ,

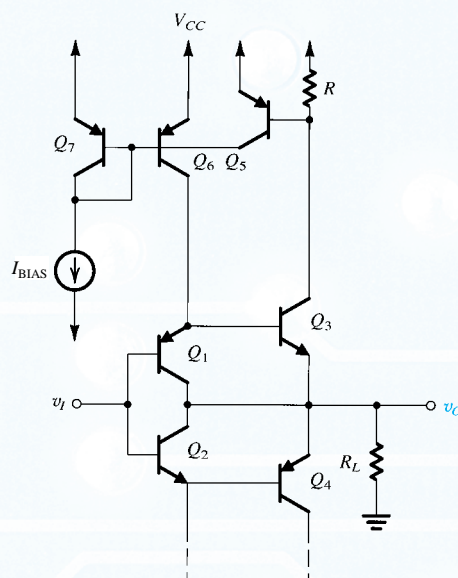


Figure P11.46

$I_S = 10^{-14}$ A. If the normal peak output current is 100 mA, find the voltage drop across R and the collector current in Q_5 .

D 11.47 Consider the thermal shutdown circuit shown in Fig. 11.35. At 25°C , Z_1 is a 6.8-V zener diode with a TC of $2\text{ mV}/^\circ\text{C}$, and Q_1 and Q_2 are BJTs that display V_{BE} of 0.7 V at a current of $100\text{ }\mu\text{A}$ and have a TC of $-2\text{ mV}/^\circ\text{C}$. Design the circuit so that at 125°C , a current of $100\text{ }\mu\text{A}$ flows in each of Q_1 and Q_2 . What is the current in Q_2 at 25°C ?

Section 11.9: IC Power Amplifiers

D 11.48 In the power-amplifier circuit of Fig. 11.36 two resistors are important in controlling the overall voltage gain. Which are they? Which controls the gain alone? Which affects both the dc output level and the gain? A new design is being considered in which the output dc level is approximately $\frac{1}{3}V_S$ (rather than approximately $\frac{1}{2}V_S$) with a gain of 50 (as before). What changes are needed?

11.49 Consider the front end of the circuit in Fig. 11.36. For $V_S = 20\text{ V}$, calculate approximate values for the bias currents in Q_1 through Q_6 . Assume $\beta_{npn} = 100$, $\beta_{pnp} = 20$, and $|V_{BE}| = 0.7\text{ V}$. Also find the dc voltage at the output.

11.50 It is required to use the LM380 power amplifier to drive an $8\text{-}\Omega$ loudspeaker while limiting the maximum possible device dissipation to 1.5 W . Use the graph of Fig. 11.38 to determine the maximum possible power-supply voltage that can be used. (Use only the given graphs; do not interpolate.) If the maximum allowed THD is to be 3% , what is the maximum possible load power? To deliver this power to the load what peak-to-peak output sinusoidal voltage is required?

D *11.51 Consider the power-op-amp output stage shown in Fig. 11.39. Using a $\pm 15\text{-V}$ supply, provide a design that provides an output of $\pm 11\text{ V}$ or more, with currents up to $\pm 20\text{ mA}$ provided primarily by Q_3 and Q_4 with a 10% contribution by Q_5 and Q_6 , and peak output currents of 1 A at full output ($+11\text{ V}$). As the basis of an initial design, use $\beta = 50$ and $|V_{BE}| = 0.7\text{ V}$ for all devices at all currents. Also use $R_5 = R_6 = 0$.

11.52 For the circuit in Fig. P11.52, assuming all transistors to have large β , show that $i_O = v_I/R$. [This voltage-to-current converter is an application of a versatile circuit building block known as the **current conveyor**; see Sedra and Roberts (1990)]. For $\beta = 100$, by what approximate percentage is i_O actually lower than this ideal value?

D 11.53 For the bridge amplifier of Fig. 11.40, let $R_1 = R_3 = 10\text{ k}\Omega$. Find R_2 and R_4 to obtain an overall gain of 10.

D 11.54 An alternative bridge amplifier configuration, with high input resistance, is shown in Fig. P11.54. (Note the similarity of this circuit to the front end of the instrumentation

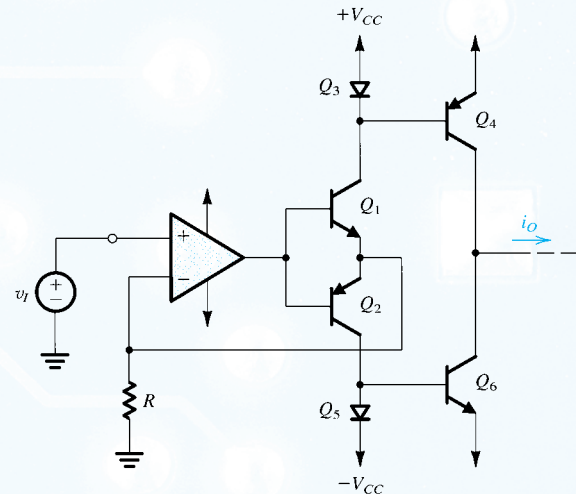


Figure P11.52

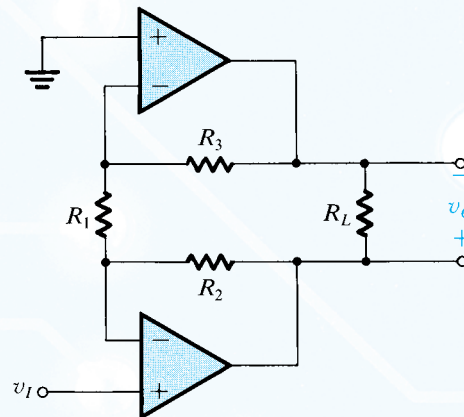


Figure P11.54

amplifier circuit shown in Fig. 2.20b.) What is the gain v_O/v_I ? For op amps (using $\pm 15\text{-V}$ supplies) that limit at $\pm 13\text{ V}$, what is the largest sine wave you can provide across R_L ? Using $1\text{ k}\Omega$ as the smallest resistor, find resistor values that make $v_O/v_I = 10\text{ V/V}$. Make sure that the signals at the outputs of the two amplifiers are complementary.

Section 11.10: MOS Power Transistors

D 11.55 Consider the design of the class AB amplifier of Fig. 11.44 under the following conditions: $|V_t| = 2\text{ V}$, $\mu C_{ox} W/L = 200\text{ mA/V}^2$, $|V_{BE}| = 0.7\text{ V}$, β is high, $I_{QN} = I_{QP} = I_R = 10\text{ mA}$, $I_{BIAS} = 100\text{ }\mu\text{A}$, $I_{Q5} = I_{Q6} = I_{BIAS}/2$, $R_2 = R_4$, the temperature coefficient of $V_{BE} = -2\text{ mV}/^\circ\text{C}$, and the temperature coefficient of $V_t = -3\text{ mV}/^\circ\text{C}$ in the low-current region. Find the values of R , R_1 , R_2 , R_3 , and R_4 . Assume Q_6 , Q_P , and Q_N to be thermally coupled. (R_G , used to suppress parasitic oscillation at high frequency, is usually $100\text{ }\Omega$ or so.)