14.3 TRANSISTOR–TRANSISTOR LOGIC (TTL OR T^{2}L)

For more than two decades (late 1960s to late 1980s) TTL enjoyed immense popularity. Indeed, the bulk of digital systems applications employing SSI and MSI packages were designed using TTL.

We shall begin this section with a study of the evolution of TTL from DTL. In this way we shall explain the function of each of the stages of the complete TTL gate circuit. Characteristics of standard TTL gates will be studied in Section 14.4. Standard TTL, however, has now been virtually replaced with more advanced forms of TTL that feature improved performance. These will be discussed in Section 14.5.

Evolution of TTL from DTL

The basic DTL gate circuit in discrete form was discussed in the previous section (see Fig. 14.6). The integrated-circuit form of the DTL gate is shown in Fig. 14.7 with only one input indicated. As a prelude to introducing TTL, we have drawn the input diode as a diode-connected transistor (Q_1), which corresponds to how diodes are made in IC form.

This circuit differs from the discrete DTL circuit of Fig. 14.6 in two important aspects. First, one of the steering diodes is replaced by the base–emitter junction of a transistor (Q_2) that is either cut off (when the input is low) or in the active mode (when the input is high). This is done to reduce the input current and thereby increase the fan-out capability of the gate. A detailed explanation of this point, however, is not relevant to our study of TTL. Second, the resistance R_B is returned to ground rather than to a negative supply, as was done in the earlier discrete circuit. An obvious advantage of this is the elimination of the additional power supply. The disadvantage, however, is that the reverse base current available to remove the excess charge stored in the base of Q_3 is rather small. We shall elaborate on this point below.

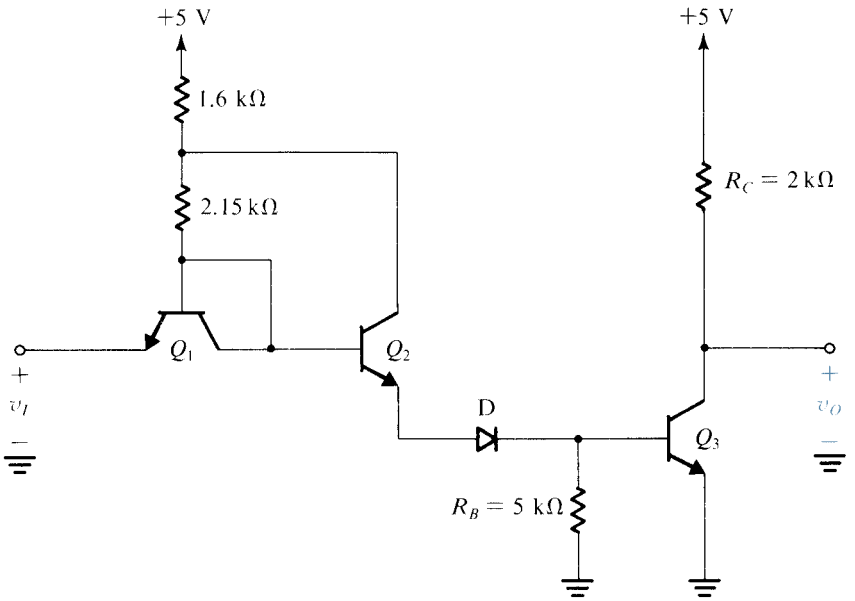

FIGURE 14.7 IC form of the DTL gate with the input diode shown as a diode-connected transistor (Q_1). Only one input terminal is shown.

EXERCISE

14.4 Consider the DTL gate circuit shown in Fig. 14.7 and assume that $\beta(Q_2) = \beta(Q_3) = 50$. (a) When $v_I = 0.2$ V, find the input current. (b) When $v_I = +5$ V, find the base current of Q_3.

Ans. (a) 1.1 mA; (b) 1.6 mA

Reasons for the Slow Response of DTL

The DTL gate has relatively good noise margins and reasonably good fan-out capability. Its response, however, is rather slow. There are two reasons for this: first, when the input goes low and Q_2 and D turn off, the charge stored in the base of Q_3 has to leak through R_B to ground. The initial value of the reverse base current that accomplishes this "base discharging" process is approximately 0.7 V/R_B, which is about 0.14 mA. Because this current is quite small in comparison to the forward base current, the time required for the removal of base charge is rather long, which contributes to lengthening the gate delay.

The second reason for the relatively slow response of DTL derives from the nature of the output circuit of the gate, which is simply a common-emitter transistor. Figure 14.8 shows the output transistor of a DTL gate driving a capacitive load C_L. The capacitance C_L represents the input capacitance of another gate and/or the wiring and parasitic capacitances that are inevitably present in any circuit. When Q_3 is turned on, its collector voltage cannot instantaneously fall because of the existence of C_L. Thus Q_3 will not immediately saturate but rather will operate in the active region. The collector of Q_3 will therefore act as a constant-current source and will sink a relatively large current (βI_B). This large current will rapidly discharge C_L. We thus see that the common-emitter output stage features a short turn-on time. However, turnoff is another matter.

Consider next the operation of the common-emitter output stage when Q_3 is turned off. The output voltage will not rise immediately to the high level (V_{CC}). Rather, C_L will charge up to V_{CC} through R_C. This is a rather slow process, and it results in lengthening the DTL gate delay (and similarly the RTL gate delay).

Having identified the two reasons for the slow response of DTL, we shall see in the following how these problems are remedied in TTL.

Input Circuit of the TTL Gate

Figure 14.9 shows a conceptual TTL gate with only one input terminal indicated. The most important feature to note is that the input diode has been replaced by a transistor. One can

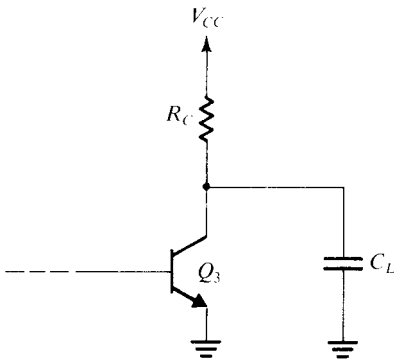

FIGURE 14.8 The output circuit of a DTL gate driving a capacitive load C_L.

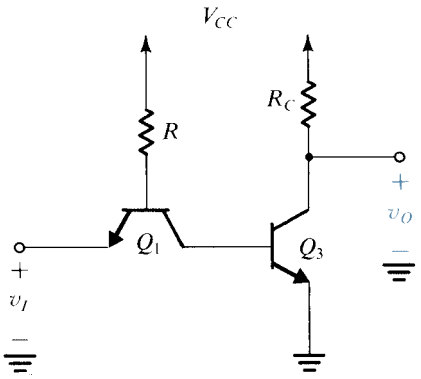

FIGURE 14.9 Conceptual form of TTL gate. Only one input terminal is shown.

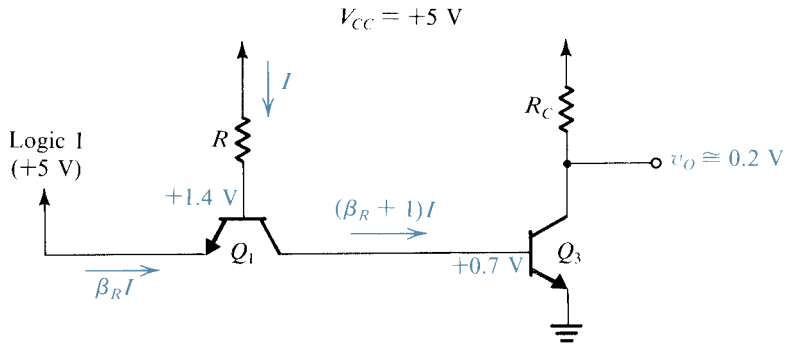

FIGURE 14.10 Analysis of the conceptual TTL gate when the input is high.

think of this simply as if the short circuit between base and collector of Q_1 in Fig. 14.7 has been removed.

To see how the conceptual TTL circuit of Fig. 14.9 works, let the input v_I be high (say, $v_I = V_{CC}$). In this case current will flow from V_{CC} through R, thus forward-biasing the base–collector junction of Q_1. Meanwhile, the base–emitter junction of Q_1 will be reverse-biased. Therefore Q_1 will be operating in the **inverse active mode**—that is, in the active mode but with the roles of emitter and collector interchanged. The voltages and currents will be as indicated in Fig. 14.10, where the current I can be calculated from

$$I = \frac{V_{CC} - 1.4}{R}$$

In actual TTL circuits Q_1 is designed to have a very low reverse β ($\beta_R \simeq 0.02$). Thus the gate input current will be very small, and the base current of Q_3 will be approximately equal to I. This current will be sufficient to drive Q_3 into saturation, and the output voltage will be low (0.1 to 0.2 V).

Next let the gate input voltage be brought down to the logic-0 level (say, $v_I \simeq 0.2$ V). The current I will then be diverted to the emitter of Q_1. The base–emitter junction of Q_1 will become forward-biased, and the base voltage of Q_1 will therefore drop to 0.9 V. Since Q_3 *was* in saturation, its base voltage will remain at +0.7 V pending the removal of the excess charge stored in the base region. Figure 14.11 indicates the various voltage and current values immediately after the input is lowered. We see that Q_1 will be operating in the normal

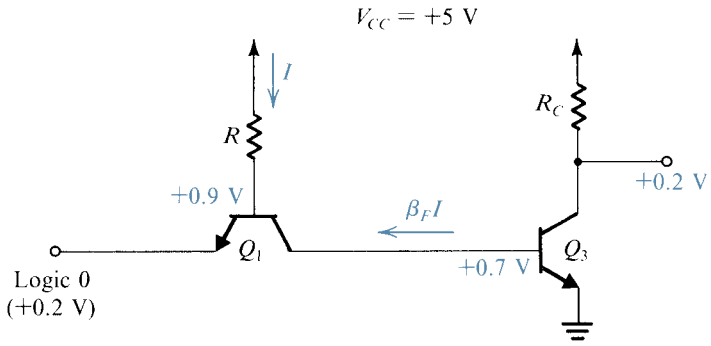

FIGURE 14.11 Voltage and current values in the conceptual TTL circuit immediately after the input voltage is lowered.

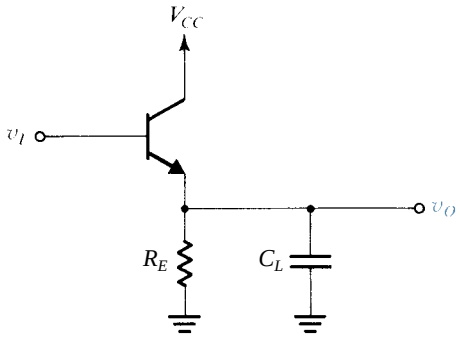

FIGURE 14.12 An emitter-follower output stage with capacitive load.

active mode[3] and its collector will carry a large current ($\beta_F I$). This large current rapidly discharges the base of Q_3 and drives it into cutoff. We thus see the action of Q_1 in speeding up the turn-off process.

As Q_3 turns off, the voltage at its base is reduced, and Q_1 enters the saturation mode. Eventually the collector current of Q_1 will become negligibly small, which implies that its V_{CEsat} will be approximately 0.1 V and the base of Q_3 will be at about 0.3 V, which keeps Q_3 in cutoff.

Output Circuit of the TTL Gate

The above discussion illustrates how one of the two problems that slow down the operation of DTL is solved in TTL. The second problem, the long rise time of the output waveform, is solved by modifying the output stage, as we shall now explain.

First, recall that the common-emitter output stage provides fast discharging of load capacitance but rather slow charging. The opposite is obtained in the emitter-follower output stage shown in Fig. 14.12. Here, as v_I goes high, the transistor turns on and provides a low output resistance (characteristic of emitter followers), which results in fast charging of C_L. On the other hand, when v_I goes low, the transistor turns off and C_L is then left to discharge slowly through R_E.

[3] Although the collector voltage of Q_1 is lower than its base voltage by 0.2 V, the collector–base junction will in effect be cut off and Q_1 will be operating in the active mode.

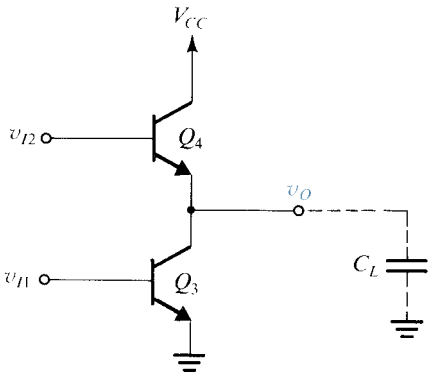

FIGURE 14.13 The totem-pole output stage.

It follows that an optimum output stage would be a combination of the common-emitter and the emitter-follower configurations. Such an output stage, shown in Fig. 14.13, has to be driven by two *complementary* signals v_{I1} and v_{I2}. When v_{I1} is high v_{I2} will be low, and in this case Q_3 will be on and saturated, and Q_4 will be off. The common-emitter transistor Q_3 will then provide the fast discharging of load capacitance and in steady state provide a low resistance (R_{CEsat}) to ground. Thus when the output is low, the gate can *sink* substantial amounts of current through the saturated transistor Q_3.

When v_{I1} is low and v_{I2} is high, Q_3 will be off and Q_4 will be conducting. The emitter follower Q_4 will then provide fast charging of load capacitance. It also provides the gate with a low output resistance in the high state and hence with the ability to *source* a substantial amount of load current.

Because of the appearance of the circuit in Fig. 14.13, with Q_4 stacked on top of Q_3, the circuit has been given the name **totem-pole output stage.** Also, because of the action of Q_4 in *pulling up* the output voltage to the high level, Q_4 is referred to as the **pull-up transistor.** Since the pulling up is achieved here by an active element (Q_4), the circuit is said to have an **active pull-up.** This is in contrast to the **passive pull-up** of RTL and DTL gates. Of course, the common-emitter transistor Q_3 provides the circuit with **active pull-down.** Finally, note that a special **driver circuit** is needed to generate the two complementary signals v_{I1} and v_{I2}.

EXAMPLE 14.1

We wish to analyze the circuit shown together with its driving waveforms in Fig. 14.14 to determine the waveform of the output signal v_O. Assume that Q_3 and Q_4 have $\beta = 50$.

Solution

Consider first the situation before v_{I1} goes high—that is, at time $t < 0$. In this case Q_3 is off and Q_4 is on, and the circuit can be simplified to that shown in Fig. 14.15. In this simplified circuit we have replaced the voltage divider (R_1, R_2) by its Thévenin equivalent. In the steady state, C_L will be charged to the output voltage v_O, whose value can be obtained as follows:

$$5 = 10 \times I_B + V_{BE} + I_E \times 0.5 + 2.5$$

Substituting $V_{BE} \simeq 0.7$ V and $I_B = I_E/(\beta + 1) = I_E/51$ gives $I_E = 2.59$ mA. Thus the output voltage v_O is given by

$$v_O = 2.5 + I_E \times 0.5 = 3.79 \text{ V}$$

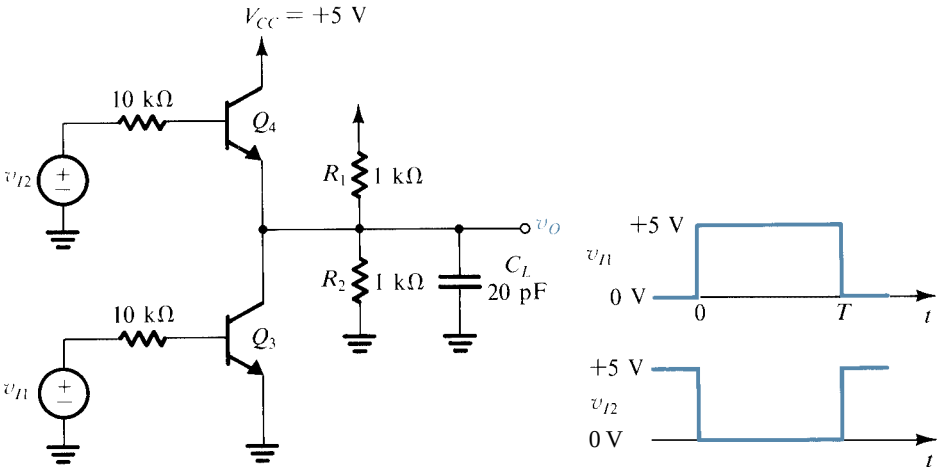

FIGURE 14.14 Circuit and input waveforms for Example 14.1.

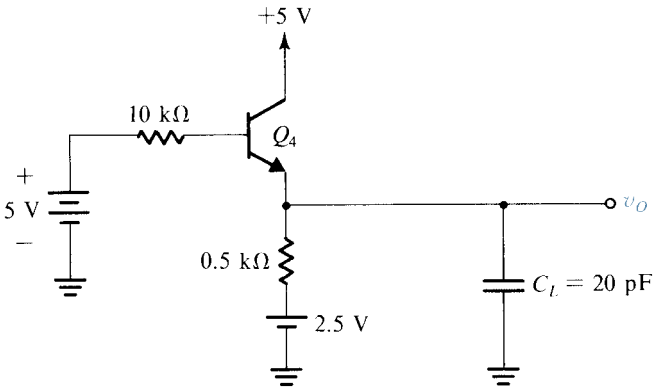

FIGURE 14.15 The circuit of Fig. 14.14 when Q_3 is off.

We next consider the circuit as v_{I1} goes high and v_{I2} goes low. Transistor Q_3 turns on and transistor Q_4 turns off, and the circuit simplifies to that shown in Fig. 14.16. Again we have used the Thévenin equivalent of the divider (R_1, R_2). We shall also assume that the switching times of the transistors are negligibly small. Thus at $t = 0+$ the base current of Q_3 becomes

$$I_B = \frac{5 - 0.7}{10} = 0.43 \text{ mA}$$

Since at $t = 0$ the collector voltage of Q_3 is 3.79 V, and since this value cannot change instantaneously because of C_L, we see that at $t = 0+$ transistor Q_3 will be in the active mode. The collector current of Q_3 will be βI_B, which is 21.5 mA, and the circuit will have the equivalent shown in Fig. 14.17(a). A simpler version of this equivalent circuit, obtained using Thévenin's theorem, is shown in Fig. 14.17(b).

The equivalent circuit of Fig. 14.17 applies as long as Q_3 remains in the active mode. This condition persists while C_L is being discharged and until v_O reaches about +0.3 V, at which time Q_3 enters saturation. This is illustrated by the waveform in Fig. 14.18. The time for the output

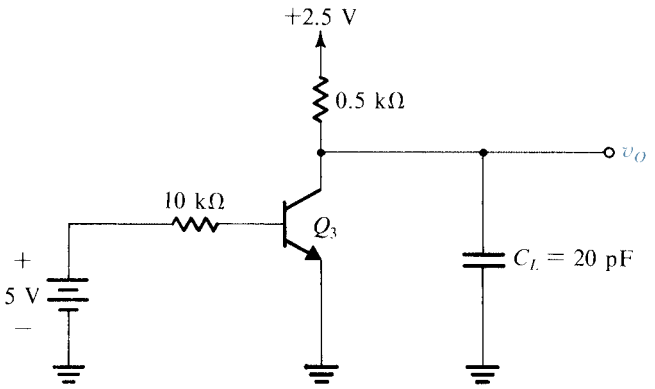

FIGURE 14.16 The circuit of Fig. 14.14 when Q_4 is off.

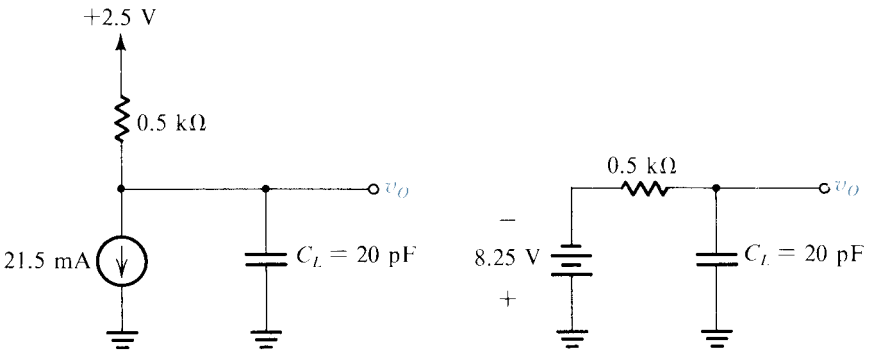

FIGURE 14.17 **(a)** Equivalent circuit for the circuit in Fig. 14.16 when Q_3 is in the active mode. **(b)** Simpler version of the circuit in (a) obtained using Thévenin's theorem.

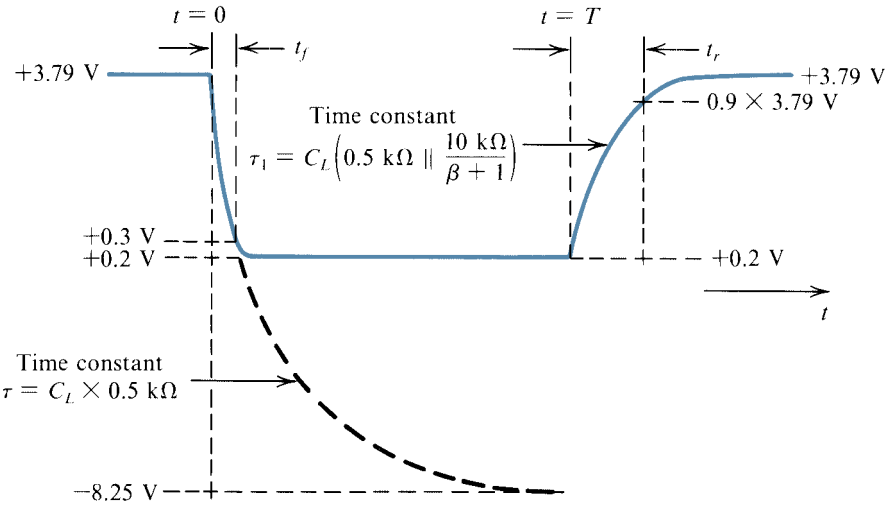

FIGURE 14.18 Details of the output voltage waveform for the circuit in Fig. 14.14.

voltage to fall from +3.79 V to +0.3 V, which can be considered the **fall time** t_f, can be obtained from

$$-8.25-(-8.25-3.79)e^{-t_f/\tau}=0.3$$

which results in

$$t_f \simeq 0.34\tau$$

where

$$\tau = C_L \times 0.5\ \text{k}\Omega = 10\ \text{ns}$$

Thus $t_f = 3.4$ ns.

After Q_3 enters saturation, the capacitor discharges further to the final steady-state value of V_{CEsat} (≃0.2 V). The transistor model that applies during this interval is more complex; since the interval in question is quite short, we shall not pursue the matter further.

Consider next the situation as v_{I1} goes low and v_{I2} goes high at $t = T$. Transistor Q_3 turns off as Q_4 turns on. We shall assume that this occurs immediately, and thus at $t = T+$ the circuit simplifies to that in Fig. 14.15. We have already analyzed this circuit in the steady state and thus know that eventually v_O will reach +3.79 V. Thus v_O rises exponentially from +0.2 V toward +3.79 V with a time constant of $C_L\{0.5\ \text{k}\Omega//[10\ \text{k}\Omega/(\beta+1)]\}$, where we have neglected the emitter resistance r_e. Denoting this time constant τ_1, we obtain $\tau_1 = 2.8$ ns. Defining the rise time t_r as the time for v_O to reach 90% of the final value, we obtain $3.79-(3.79-0.2)e^{-t_r/\tau_1} = 0.9\times 3.79$, which results in $t_r = 6.4$ ns. Figure 14.18 illustrates the details of the output voltage waveform.

The Complete Circuit of the TTL Gate

Figure 14.19 shows the complete TTL gate circuit. It consists of three stages: the input transistor Q_1, whose operation has already been explained, the driver stage Q_2, whose function is to generate the two complementary voltage signals required to drive the totem-pole circuit,

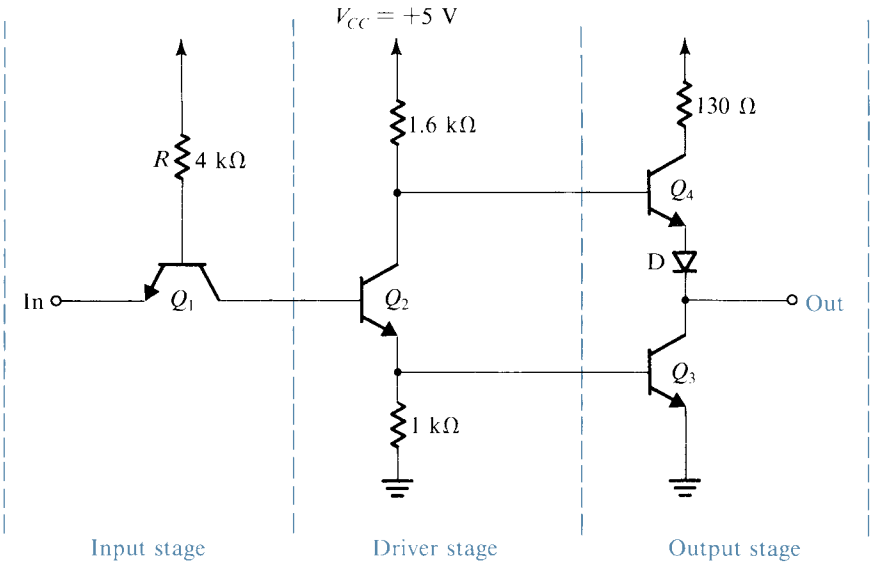

FIGURE 14.19 The complete TTL gate circuit with only one input terminal indicated.

which is the third (output) stage of the gate. The totem-pole circuit in the TTL gate has two additional components: the 130-Ω resistance in the collector circuit of Q_4 and the diode D in the emitter circuit of Q_4. The function of these two additional components will be explained shortly. Notice that the TTL gate is shown with only one input terminal indicated. Inclusion of additional input terminals will be considered in Section 14.4.

Because the driver stage Q_2 provides two complementary (that is, out-of-phase) signals, it is known as a **phase splitter.**

We shall now provide a detailed analysis of the TTL gate circuit in its two extreme states: one with the input high and one with the input low.

Analysis When the Input Is High

When the input is high (say, +5 V), the various voltages and currents of the TTL circuit will have the values indicated in Fig. 14.20. The analysis illustrated in Fig. 14.20 is quite straightforward, and the order of the steps followed is indicated by the circled numbers. As expected, the input transistor is operating in the inverse active mode, and the input current, called the **input high current** I_{IH}, is small; that is,

$$I_{IH} = \beta_R I \simeq 15\ \mu\text{A}$$

where we assume that $\beta_R \simeq 0.02$.

The collector current of Q_1 flows into the base of Q_2, and its value is sufficient to saturate the phase-splitter transistor Q_2. The latter supplies the base of Q_3 with sufficient current to drive it into saturation and lower its output voltage to V_{CEsat} (0.1 to 0.2 V). The voltage at the collector of Q_2 is $V_{BE3} + V_{CEsat}(Q_2)$, which is approximately +0.9 V. If diode D were not included, this voltage would be sufficient to turn Q_4 on, which is contrary to the proper operation of the totem-pole circuit. Including diode D ensures that both Q_4 and D remain off.

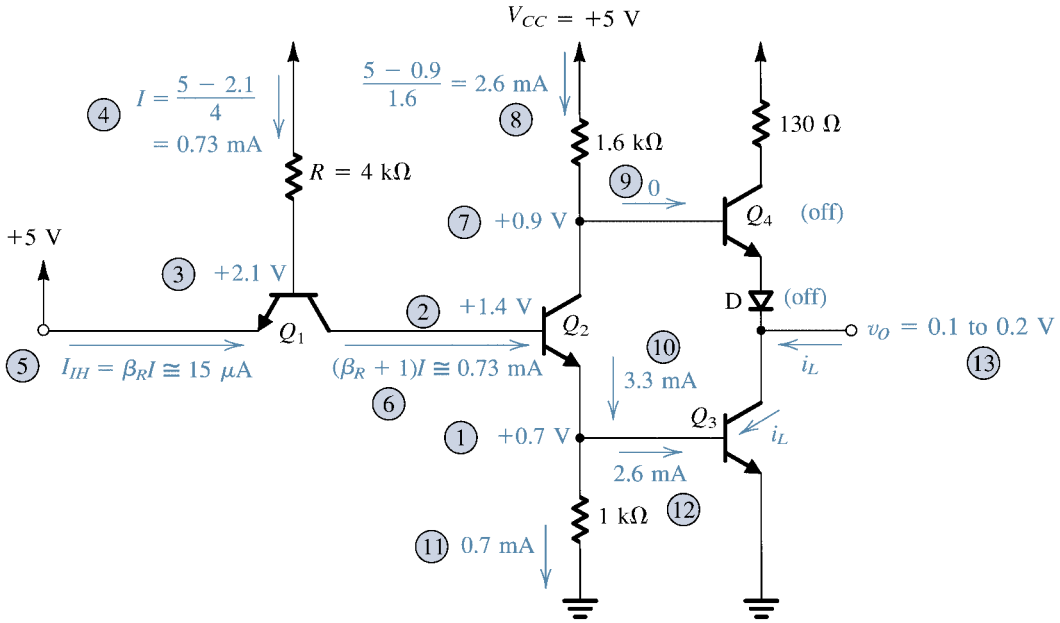

FIGURE 14.20 Analysis of the TTL gate with the input high. The circled numbers indicate the order of the analysis steps.

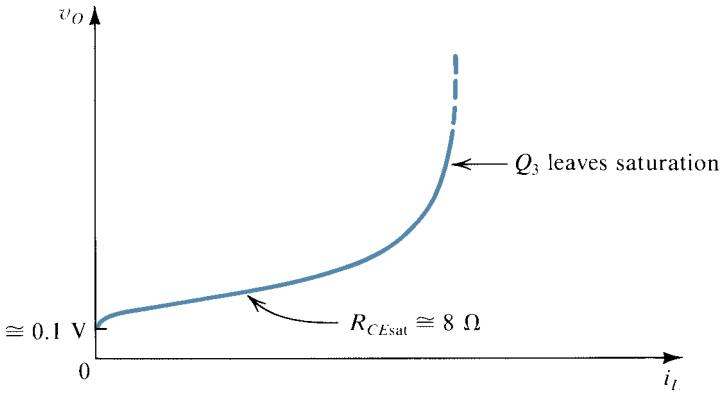

FIGURE 14.21 The v_O–i_L characteristic of the TTL gate when the output is low.

The saturated transistor Q_3 then establishes the low output voltage of the gate ($V_{CE\text{sat}}$) and provides a low impedance to ground.

In the low-output state the gate can sink a load current i_L, provided that the value of i_L does not exceed $\beta \times 2.6$ mA, which is the maximum collector current that Q_3 can sustain while remaining in saturation. Obviously the greater the value of i_L, the greater the output voltage will be. To maintain the logic-0 level below a certain specified limit, a corresponding limit has to be placed on the load current i_L. As will be seen shortly, it is this limit that determines the maximum fan-out of the TTL gate.

Figure 14.21 shows a sketch of the output voltage v_O versus the load current i_L of the TTL gate when the output is low. This is simply the v_{CE}–i_C characteristic curve of Q_3 measured with a base current of 2.6 mA. Note that at $i_L = 0$, v_O is the offset voltage, which is about 100 mV.

EXERCISE

14.5 Assume that the saturation portion of the v_O–i_L characteristic shown in Fig. 14.21 can be approximated by a straight line (of slope = 8 Ω) that intersects the v_O axis at 0.1 V. Find the maximum load current that the gate is allowed to sink if the logic-0 level is specified to be ≤0.3 V.

Ans. 25 mA

Analysis When the Input Is Low

Consider next the operation of the TTL gate when the input is at the logic-0 level (≃0.2 V). The analysis is illustrated in Fig. 14.22, from which we see that the base–emitter junction of Q_1 will be forward-biased and the base voltage will be approximately +0.9 V. Thus the current I can be found to be approximately 1 mA. Since 0.9 V is insufficient to forward-bias the series combination of the collector–base junction of Q_1 and the base–emitter junction of Q_2 (at least 1.2 V would be required), the latter will be off. Therefore the collector current of Q_1 will be almost zero and Q_1 will be saturated, with $V_{CE\text{sat}} \simeq 0.1$ V. Thus the base of Q_2 will be at approximately +0.3 V, which is indeed insufficient to turn Q_2 on.

The gate input current in the low state, called **input-low current** I_{IL}, is approximately equal to the current I ($\simeq 1$ mA) and flows out of the emitter of Q_1. If the TTL gate is driven

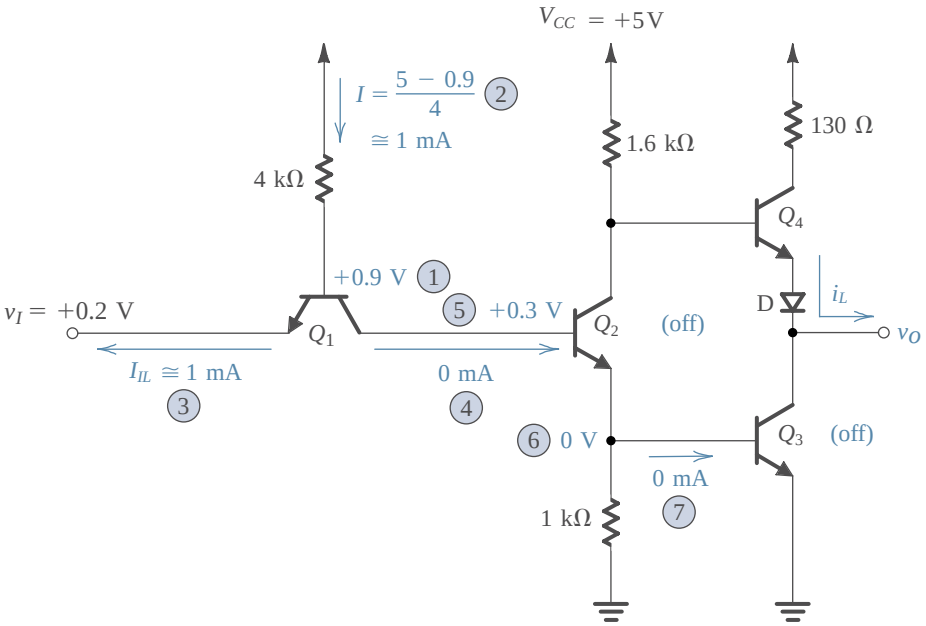

FIGURE 14.22 Analysis of the TTL gate when the input is low. The circled numbers indicate the order of the analysis steps.

by another TTL gate, the output transistor Q_3 of the driving gate should sink this current I_{IL}. Since the output current that a TTL gate can sink is limited to a certain maximum value, the maximum fan-out of the gate is directly determined by the value of I_{IL}.

EXERCISES

14.6 Consider the TTL gate analyzed in Exercise 14.5. Find its maximum allowable fan-out using the value of I_{IL} calculated above.

Ans. 25

14.7 Use Eq. (4.114) to find V_{CEsat} of transistor Q_1 when the input of the gate is low (0.2 V). Assume that $\beta_F = 50$ and $\beta_R = 0.02$.

Ans. 98 mV

Let us continue with our analysis of the TTL gate. When the input is low, we see that both Q_2 and Q_3 will be off. Transistor Q_4 will be on and will supply (source) the load current i_L. Depending on the value of i_L, Q_4 will be either in the active mode or in the saturation mode.

With the gate output terminal open, the current i_L will be very small (mostly leakage) and the two junctions (base–emitter junction of Q_4 and diode D) will be barely conducting. Assuming that each junction has a 0.65-V drop and neglecting the voltage drop across the 1.6-kΩ resistance, we find that the output voltage will be

$$v_O \simeq 5 - 0.65 - 0.65 = 3.7 \text{ V}$$

As i_L is increased, Q_4 and D conduct more heavily, but for a range of i_L, Q_4 remains in the active mode, and v_O is given by

$$v_O = V_{CC} - \frac{i_L}{\beta + 1} \times 1.6\ \text{k}\Omega - V_{BE4} - V_D \tag{14.4}$$

If we keep increasing i_L, a value will be reached at which Q_4 saturates. Then the output voltage becomes determined by the 130-Ω resistance according to the approximate relationship

$$v_O \simeq V_{CC} - i_L \times 130 - V_{CEsat}(Q_4) - V_D \tag{14.5}$$

Function of the 130-Ω Resistance

At this point the reason for including the 130-Ω resistance should be evident: It is simply to limit the current that flows through Q_4, especially in the event that the output terminal is accidentally short-circuited to ground. This resistance also limits the supply current in another circumstance, namely, when Q_4 turns on while Q_3 is still in saturation. To see how this occurs, consider the case where the gate input was high and then is suddenly brought down to the low level. Transistor Q_2 will turn off relatively fast because of the availability of a large reverse current supplied to its base terminal by the collector of Q_1. On the other hand, the base of Q_3 will have to discharge through the 1-kΩ resistance, and thus Q_3 will take some time to turn off. Meanwhile Q_4 will turn on, and a large current pulse will flow through the series combination of Q_4 and Q_3. Part of this current will serve the useful purpose of charging up any load capacitance to the logic-1 level. The magnitude of the current pulse will be limited by the 130-Ω resistance to about 30 mA.

The occurrence of these current pulses of short duration (called **current spikes**) raises another important issue. The current spikes have to be supplied by the V_{CC} source and, because of its finite source resistance, will result in voltage spikes (or "glitches") superimposed on V_{CC}. These voltage spikes could be coupled to other gates and flip-flops in the digital system and thus might produce false switching in other parts of the system. This effect, which might loosely be called **crosstalk,** is a problem in TTL systems. To reduce the size of the voltage spikes, capacitors (called bypass capacitors) should be connected between the supply rail and ground at frequent locations. These capacitors lower the impedance of the supply-voltage source and hence reduce the magnitude of the voltage spikes. Alternatively, one can think of the bypass capacitors as supplying the impulsive current spikes.

EXERCISES

14.8 Assuming that Q_4 has $\beta = 50$ and that at the verge of saturation $V_{CEsat} = 0.3$ V, find the value of i_L at which Q_4 saturates.

Ans. 4.16 mA

14.9 Assuming that at a current of 1 mA the voltage drops across the emitter–base junction of Q_4 and the diode D are each 0.7 V, find v_O when $i_L = 1$ mA and 10 mA. (Note the result of the previous exercise.)

Ans. 3.6 V; 2.7 V

14.10 Find the maximum current that can be sourced by a TTL gate while the output high level (V_{OH}) remains greater than the minimum guaranteed value of 2.4 V.

Ans. 12.3 mA; or, more accurately, taking the base current of Q_4 into account, 13.05 mA