5.11 THE JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

The **junction field-effect transistor,** or JFET, is perhaps the simplest transistor available. It has some important characteristics, notably a very high input resistance. Unfortunately, however (for the JFET), the MOSFET has an even higher input resistance. This, together with the many other advantages of MOS transistors, has made the JFET virtually obsolete. Currently, its applications are limited to discrete-circuit design, where it is used both as an amplifier and as a switch. Its integrated-circuit applications are limited to the design of the differential input stage of some operational amplifiers, where advantage is taken of its high input resistance (compared to the BJT). In this section, we briefly consider JFET operation and characteristics. Another important reason for including the JFET in the study of electronics is that it helps in understanding the operation of gallium arsenide devices, the subject of the next section.

Device Structure

As with other FET types, the JFET is available in two polarities: *n*-channel and *p*-channel. Fig. 5.69(a) shows a simplified structure of the *n*-channel JFET. It consists of a slab of *n*-type silicon with *p*-type regions diffused on its two sides. The *n* region is the channel, and the *p*-type regions are electrically connected together and form the gate. The device operation is based on reverse-biasing the *pn* junction between gate and channel. Indeed, it is the reverse bias on this junction that is used to control the channel width and hence the current flow from drain to source. The major role that this *pn* junction plays in the operation of this FET has given rise to its name: Junction Field-Effect Transistor (JFET).

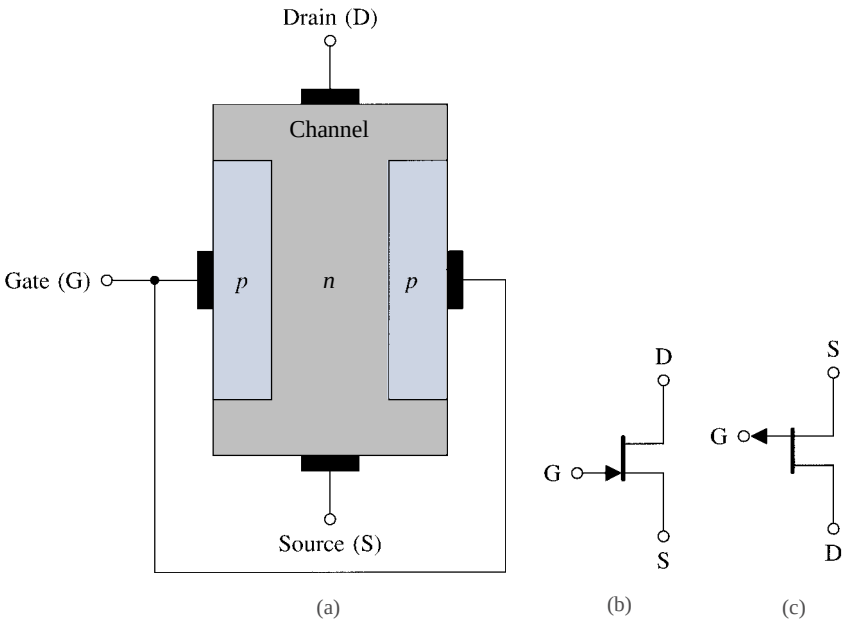


FIGURE 5.69 **(a)** Basic structure of *n*-channel JFET. This is a simplified structure utilized to explain device operation. **(b)** Circuit symbol for the *n*-channel JFET. **(c)** Circuit symbol for the *p*-channel JFET.

It should be obvious that a *p*-channel device can be fabricated by simply reversing all the semiconductor types, thus using *p*-type silicon for the channel and *n*-type silicon for the gate regions.

Figures 5.69(b) and (c) show the circuit symbols for JFETs of both polarities. Observe that the device polarity (*n*-channel or *p*-channel) is indicated by the direction of the arrowhead on the gate line. This arrowhead points in the forward direction of the gate–channel *pn* junction. Although the JFET is a symmetrical device whose source and drain can be interchanged, it is useful in circuit design to designate one of these two terminals as source and the other as drain. The circuit symbol achieves this designation by placing the gate closer to the source than to the drain.

Physical Operation

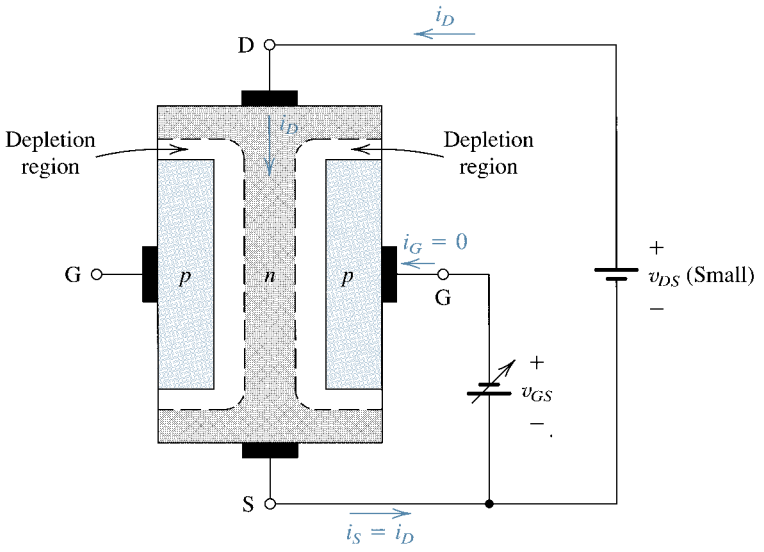
Consider an *n*-channel JFET and refer to Fig. 5.70(a). (Note that to simplify matters, we will not show the electrical connection between the gate terminals; it is assumed, however, that the two terminals labeled G are joined together.) With $v_{GS} = 0$, the application of a voltage v_{DS} causes current to flow from the drain to the source. When a negative v_{GS} is applied, the depletion region of the gate–channel junction widens and the channel becomes correspondingly narrower; thus the channel resistance increases and the current i_D (for a given v_{DS}) decreases. Because v_{DS} is small, the channel is almost of uniform width. The JFET is simply operating as a resistance whose value is controlled by v_{GS}. If we keep increasing v_{GS} in the negative direction, a value is reached at which the depletion region occupies the entire channel. At this value of v_{GS} the channel is completely depleted of charge carriers (electrons); the channel has in effect disappeared. This value of v_{GS} is therefore the threshold voltage of the device, V_t, which is obviously negative for an *n*-channel JFET. For JFETs the threshold voltage is called the **pinch-off voltage** and is denoted V_P.

Consider next the situation depicted in Fig. 5.70(b). Here v_{GS} is held constant at a value greater (that is, less negative) than V_P, and v_{DS} is increased. Since v_{DS} appears as a voltage drop across the length of the channel, the voltage increases as we move along the channel from source to drain. It follows that the reverse-bias voltage between gate and channel varies at different points along the channel and is highest at the drain end. Thus the channel acquires a tapered shape and the i_D–v_{DS} characteristic becomes nonlinear. When the reverse bias at the drain end, v_{GD}, falls below the pinch-off voltage V_P, the channel is pinched off at the drain end and the drain current saturates. The remainder of the description of JFET operation follows closely that given for the depletion MOSFET.

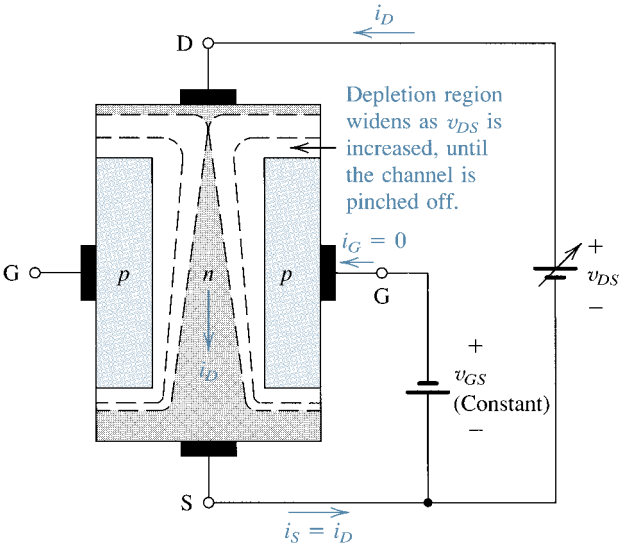
The description above clearly indicates that the JFET is a depletion-type device. Its characteristics should therefore be similar to those of the depletion-type MOSFET. This is true with a very important exception: While it is possible to operate the depletion-type MOSFET in the enhancement mode (by simply applying a positive v_{GS} if the device is *n* channel) this is impossible in the JFET case. If we attempt to apply a positive v_{GS}, the gate–channel *pn* junction becomes forward biased and the gate ceases to control the channel. Thus the maximum v_{GS} is limited to 0 V, though it is possible to go as high as 0.3 V or so since a *pn* junction remains essentially cut off at such a small forward voltage.

Current–Voltage Characteristics

The current–voltage characteristics of the JFET are identical to those of the depletion-mode MOSFET studied in Section 5.3 except that for the JFET the maximum v_{GS} allowed is



(a)



(b)

FIGURE 5.70 Physical operation of the *n*-channel JFET: **(a)** For small v_{DS} the channel is uniform and the device functions as a resistance whose value is controlled by v_{GS}. **(b)** Increasing v_{DS} causes the channel to acquire a tapered shape and eventually pinch-off occurs. Note that, though not shown, the two gate regions are electrically connected.

normally 0 V. Furthermore, the JFET is specified in terms of the pinch-off voltage V_P (equal to V_t of the MOSFET) and the *d*rain-to-source current with the gate *s*horted to the source, I_{DSS}, which corresponds to $\frac{1}{2}k_n'V_t^2$ for the MOSFET. With these substitutions, the *n*-channel JFET characteristics can be described as follows:

Cutoff: $v_{GS} \leq V_P$, $i_D = 0$

Triode region: $V_P \le v_{GS} \le 0$, $v_{DS} \le v_{GS} - V_P$

$$i_D = I_{DSS}\left[2\left(1 - \frac{v_{GS}}{V_P}\right)\left(\frac{v_{DS}}{-V_P}\right) - \left(\frac{v_{DS}}{V_P}\right)^2\right] \tag{5.116}$$

Saturation (pinch-off) region: $V_P \le v_{GS} \le 0$, $v_{DS} \ge v_{GS} - V_P$

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \tag{5.117}$$

where λ is the inverse of the Early voltage; $\lambda = 1/V_A$, and V_A and λ are positive for *n*-channel devices.

Recalling that for an *n*-channel device, V_P is negative, we see that operation in the pinch-off region is obtained when the drain voltage is greater than the gate voltage by at least $|V_P|$.

Since the gate–channel junction is always reverse-biased, only a leakage current flows through the gate terminal. From Chapter 3, we know that such a current is of the order of 10^{-9} A. Although i_G is very small, and is assumed zero in almost all applications, it should be noted that the gate current in a JFET is many orders of magnitude greater than the gate current in a MOSFET. Of course the latter is so tiny because of the insulated gate structure. Another complication arises in the JFET because of the strong dependence of gate leakage current on temperature—approximately doubling for every 10°C rise in temperature, just as in the case of a reverse-biased diode (see Chapter 3).

The *p*-Channel JFET

The current–voltage characteristics of the *p*-channel JFET are described by the same equations as the *n*-channel JFET. Note, however, that for the *p*-channel JFET, V_P is positive, $0 \le v_{GS} \le V_P$, v_{DS} is negative, λ and V_A are negative, and the current i_D flows out of the drain terminal. To operate the *p*-channel JFET in pinch-off, $v_{DS} \le v_{GS} - V_P$, which in words means that the drain voltage must be lower than the gate voltage by at least $|V_P|$. Otherwise, with $v_{DS} \ge v_{GS} - V_P$, the *p*-channel JFET operates in the triode region.

The JFET Small-Signal Model

The JFET small-signal model is identical to that of the MOSFET [see Fig. 5.34(b)]. Here, g_m is given by

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right)\left(1 - \frac{V_{GS}}{V_P}\right) \tag{5.118a}$$

or alternatively by

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right)\sqrt{\frac{I_D}{I_{DSS}}} \tag{5.118b}$$

where V_{GS} and I_D are the dc bias quantities, and

$$r_o = \frac{|V_A|}{I_D} \tag{5.119}$$

At high frequencies, the equivalent circuit of Fig. 5.67(c) applies with C_{gs} and C_{gd} being both depletion capacitances. Typically, $C_{gs} = 1$ to 3 pF, $C_{gd} = 0.1$ to 0.5 pF, and $f_T = 20$ to 100 MHz.

EXERCISES

In Exercises 5.43 to 5.46, let the *n*-channel JFET have $V_P = -4$ V and $I_{DSS} = 10$ mA, and unless otherwise specified assume that in pinch-off (saturation) the output resistance is infinite.

5.43 For $v_{GS} = -2$ V, find the minimum v_{DS} for the device to operate in pinch-off. Calculate i_D for $v_{GS} = -2$ V and $v_{DS} = 3$ V.

Ans. 2 V; 2.5 mA

5.44 For $v_{DS} = 3$ V, find the change in i_D corresponding to a change in v_{GS} from −2 to −1.6 V.

Ans. 1.1 mA

5.45 For small v_{DS}, calculate the value of r_{DS} at $v_{GS} = 0$ V and at $v_{GS} = -3$ V.

Ans. 200 Ω; 800 Ω

5.46 If $V_A = 100$ V, find the JFET output resistance r_o when operating in pinch-off at a current of 1 mA, 2.5 mA, and 10 mA.

Ans. 100 kΩ; 40 kΩ; 10 kΩ

D5.47 The JFET in the circuit of Fig. E5.47 has $V_P = -3$ V, $I_{DSS} = 9$ mA, and $\lambda = 0$. Find the values of all resistors so that $V_G = 5$ V, $I_D = 4$ mA, and $V_D = 11$ V. Design for 0.05 mA in the voltage divider.

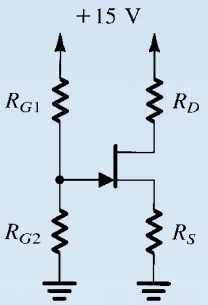


FIGURE E5.47

Ans. $R_{G1} = 200$ kΩ; $R_{G2} = 100$ kΩ; $R_S = 1.5$ kΩ; $R_D = 1$ kΩ

5.48 For the JFET circuit designed in Exercise 5.47, let an input signal v_i be capacitively coupled to the gate, a large bypass capacitor be connected between the source and ground, and the output signal v_o be taken from the drain through a large coupling capacitor. The resulting common-source amplifier is shown in Fig. E5.48. Calculate g_m and r_o (assuming $V_A = 100$ V). Also find R_i, $A_v \equiv (v_o/v_i)$, and R_o.

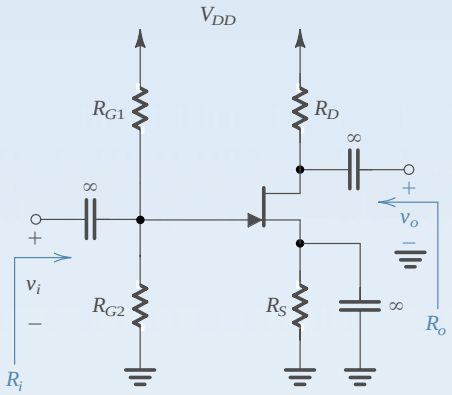


FIGURE E5.48

Ans. 4 mA/V; 25 kΩ; 66.7 kΩ; −3.8 V/V; 962 Ω