CHAPTER 14

Advanced MOS and Bipolar Logic Circuits

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IN THIS CHAPTER YOU WILL LEARN

1. That by replacing the pull-up network (PUN) of a CMOS logic gate by a single, permanently-on PMOS transistor, considerable savings in transistor count and silicon area can be achieved in gates with high fan-in. The resulting circuits are known as pseudo-NMOS.
2. That a useful and conceptually simple form of MOS logic circuits, known as pass-transistor logic (PTL), utilizes MOS transistors as series switches in the signal path from input to output.
3. That a very effective switch for both analog and digital applications, known as transmission gate, is formed by connecting an NMOS and a PMOS transistor in parallel.
4. That eliminating the pull-up network and placing two complementary switches, operated by a clock signal, in series with the pull-down network of a CMOS gate, results in an interesting and useful class of circuits known as dynamic logic.
5. How the BJT differential-pair configuration is used as a current switch to realize the fastest commercially available logic-circuit family: emitter-coupled logic (ECL).
6. How the MOSFET and the BJT are combined in BiCMOS circuits in ways that take advantage of the best attributes of each device.

Introduction

Standard CMOS logic, which we studied in Chapter 13, excels in almost every performance category: It is easy to design, has the maximum possible voltage swing, is robust from a noise-immunity standpoint, dissipates no static power, and can be designed to provide equal high-to-low and low-to-high propagation delays. Its main disadvantage is the requirement of two transistors for each additional gate input, which for gates with high fan-in can make the chip area large and increase the total capacitance and, correspondingly, the propagation delay and the dynamic power dissipation. For this reason designers of digital integrated circuits have been searching for forms of CMOS logic circuits that can be used to supplement standard CMOS. This chapter presents three such forms that reduce the required number of transistors but incur other costs. These forms are not intended to replace standard CMOS, but are rather to be used in special applications for special purposes.

Pseudo-NMOS logic, studied in Section 14.1, replaces the pull-up network (PUN) in a CMOS logic gate by a single permanently "on" PMOS transistor. The reduction in transistor count and silicon area comes at the expense of static power dissipation. As well, the output low level V_{OL} becomes dependent on the transistors' W/L ratios.

Pass-transistor logic (PTL), studied in Section 14.2, utilizes MOS transistors as switches in the series path from input to output. Though simple and attractive for special applications, PTL does not restore the signal level and thus requires the occasional use of standard CMOS inverters to avoid signal-level degradation, especially in long chains of switches.

The dynamic logic circuits studied in Section 14.3 dispense with the PUN and place two complementary switches in series with the PDN. The switches are operated by a clock, and the gate output is stored on the load capacitance. Here the reduction in transistor count is achieved at the expense of a more complex design that is less robust than static CMOS.

Although CMOS accounts for the vast majority of digital integrated circuits, there is a bipolar logic-circuit family that is still of some interest. This is emitter-coupled logic (ECL), which we study in Section 14.4. Finally, in Section 14.5 we show how the MOSFET and the BJT can be combined in ways that take advantage of the best properties of each, resulting in what are known as BiCMOS circuits.

14.1 Pseudo-NMOS Logic Circuits

14.1.1 The Pseudo-NMOS Inverter

Figure 14.1 shows a modified form of the CMOS inverter. Here, only Q_N is driven by the input voltage while the gate of Q_P is grounded, and Q_P acts as an active load for Q_N. Even before we examine the operation of this circuit in detail, an advantage over standard CMOS is obvious: Each input needs to be connected to the gate of only one transistor or, alternatively, only one additional transistor (an NMOS) will be needed for each additional gate input. Thus the area and delay penalties arising from increased fan-in in a standard CMOS will be reduced. This is indeed the motivation for exploring this modified inverter circuit.

The inverter circuit of Fig. 14.1(a) resembles other forms of NMOS logic that consist of a driver transistor (Q_N) and a load transistor (in this case, Q_P); hence the name pseudo-NMOS.

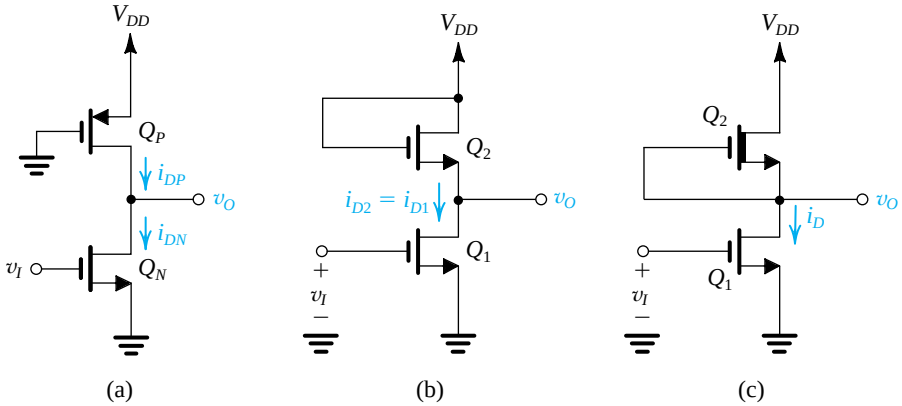

Figure 14.1 **(a)** The pseudo-NMOS logic inverter. **(b)** The enhancement-load (or saturated-load) NMOS inverter. **(c)** The depletion-load NMOS inverter.

For comparison purposes, we shall briefly mention two older forms of NMOS logic. The earliest form, popular in the mid-1970s, utilized an enhancement MOSFET for the load element, in a topology whose basic inverter is shown in Fig. 14.1(b). We studied this inverter circuit in Example 13.2, where we found that it suffers from a relatively small logic swing, small noise margins, and high static power dissipation. For these reasons, this logic-circuit technology is virtually obsolete. It was replaced in the late 1970s and early 1980s with depletion-load NMOS circuits, in which a depletion NMOS transistor (see Section 5.9.6) with its gate connected to its source is used as the load element. The topology of the basic depletion-load inverter is shown in Fig. 14.1(c).

It was initially expected that the depletion NMOS with $V_{GS} = 0$ would operate as a constant-current source and would thus provide an excellent load element.[1] However, it was quickly realized that the body effect in the depletion transistor causes its i–v characteristic to deviate considerably from that of a constant-current source. Nevertheless, depletion-load NMOS circuits feature significant improvements over their enhancement-load counterparts, enough to justify the extra processing step required to fabricate the depletion devices (namely, ion-implanting the channel). Although depletion-load NMOS has been virtually replaced by CMOS, one can still see some depletion-load circuits in specialized applications. We will not study depletion-load NMOS logic here (the interested reader can refer to the CD or the website of this book).

The pseudo-NMOS inverter that we are about to study is similar to depletion-load NMOS, but with rather improved characteristics. It also has the advantage of being directly compatible with standard CMOS circuits.

14.1.2 Static Characteristics

The static characteristics of the pseudo-NMOS inverter can be derived in a manner similar to that used for standard CMOS. Toward that end, we note that the drain currents of Q_N and Q_P are given by

$$i_{DN} = \tfrac{1}{2}k_n(v_I - V_t)^2, \quad \text{for } v_O \geq v_I - V_t \quad \text{(saturation)} \tag{14.1}$$

$$i_{DN} = k_n[(v_I - V_t)v_O - \tfrac{1}{2}v_O^2], \quad \text{for } v_O \leq v_I - V_t \quad \text{(triode)} \tag{14.2}$$

$$i_{DP} = \tfrac{1}{2}k_p(V_{DD} - V_t)^2, \quad \text{for } v_O \leq V_t \quad \text{(saturation)} \tag{14.3}$$

$$i_{DP} = k_p[(V_{DD} - V_t)(V_{DD} - v_O) - \tfrac{1}{2}(V_{DD} - v_O)^2], \quad \text{for } v_O \geq V_t \quad \text{(triode)} \tag{14.4}$$

where we have assumed that $V_{tn} = -V_{tp} = V_t$, and have used $k_n = k_n'(W/L)_n$ and $k_p = k_p'(W/L)_p$ to simplify matters.

To obtain the voltage-transfer characteristic of the inverter, we superimpose the load curve represented by Eqs. (14.3) and (14.4) on the i_D–v_{DS} characteristics of Q_N, which can be relabeled as i_{DN}–v_O and drawn for various values of $v_{GS} = v_I$. Such a graphical construction is shown in Fig. 14.2, where, to keep the diagram simple, we show the Q_N curves for only the two extreme values of v_I, namely, 0 and V_{DD}. Two observations follow:

[1] A constant-current load provides a capacitor-charging current that does not diminish as v_O rises toward V_{DD}, as is the case with a resistive load. Thus the value of t_{PLH} obtained with a current-source load is significantly lower than that obtained with a resistive load (see Problem 14.1). Of course, a resistive load, such as in the circuit studied in Example 13.1, is simply out of the question because of the very large silicon area it would occupy (equivalent to that of thousands of transistors!).

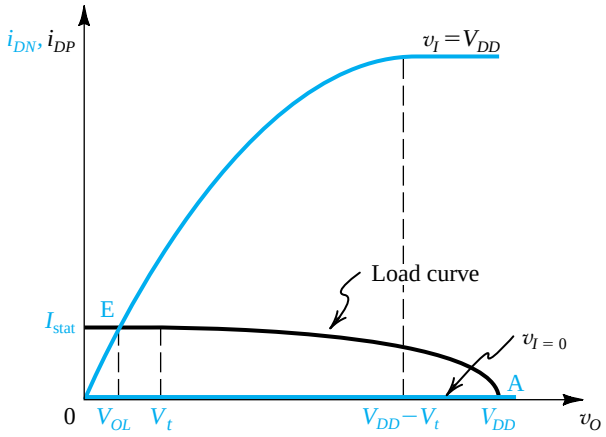

Figure 14.2 Graphical construction to determine the VTC of the inverter in Fig. 14.1(a).

1. The load curve represents a much lower saturation current (Eq. 14.3) than is represented by the corresponding curve for Q_N, namely, that for $v_I = V_{DD}$. This is a result of the fact that the pseudo-NMOS inverter is usually designed so that k_n is greater than k_p by a factor of 4 to 10. As we will show shortly, this inverter is of the so-called ratioed type,[2] and the ratio $r \equiv k_n/k_p$ determines all the breakpoints of the VTC, that is, V_{OL}, V_{IL}, V_{IH}, and so on, and thus determines the noise margins. Selection of a relatively high value for r reduces V_{OL} and widens the noise margins.
2. Although one tends to think of Q_P as acting as a constant-current source, it actually operates in saturation for only a small range of v_O, namely, $v_O \leq V_t$. For the remainder of the v_O range, Q_P operates in the triode region.

Consider first the two extreme cases of v_I: When $v_I = 0$, Q_N is cut off and Q_P is operating in the triode region, though with zero current and zero drain–source voltage. Thus the operating point is that labeled A in Fig. 14.2, where $v_O = V_{OH} = V_{DD}$, the static current is zero, and the static power dissipation is zero. When $v_I = V_{DD}$, the inverter will operate at the point labeled E in Fig. 14.2. Observe that unlike standard CMOS, here V_{OL} is not zero, an obvious disadvantage. Another disadvantage is that the gate conducts current (I_{stat}) in the low-output state, and thus there will be static power dissipation ($P_D = I_{stat} \times V_{DD}$).

14.1.3 Derivation of the VTC

Figure 14.3 shows the VTC of the pseudo-NMOS inverter. As indicated, it has four distinct regions, labeled I through IV, corresponding to the different combinations of possible modes of operation of Q_N and Q_P. The four regions, the corresponding transistor modes of operation, and the conditions that define the regions are listed in Table 14.1. We shall utilize the information in this table together with the device equations given in Eqs. (14.1) through (14.4) to derive expressions for the various segments of the VTC and in particular for the important parameters that characterize the static operation of the inverter.

[2]For the NMOS inverters such as that studied in Example 13.2, V_{OL} depends on the ratio of the transconductance parameters of the devices, that is, on the ratio $(k'(W/L))_{driver}/((k'(W/L))_{load}$. Such circuits are therefore known as *ratioed* logic circuits. Standard CMOS logic circuits do not have such a dependency and can therefore be called *ratioless*.

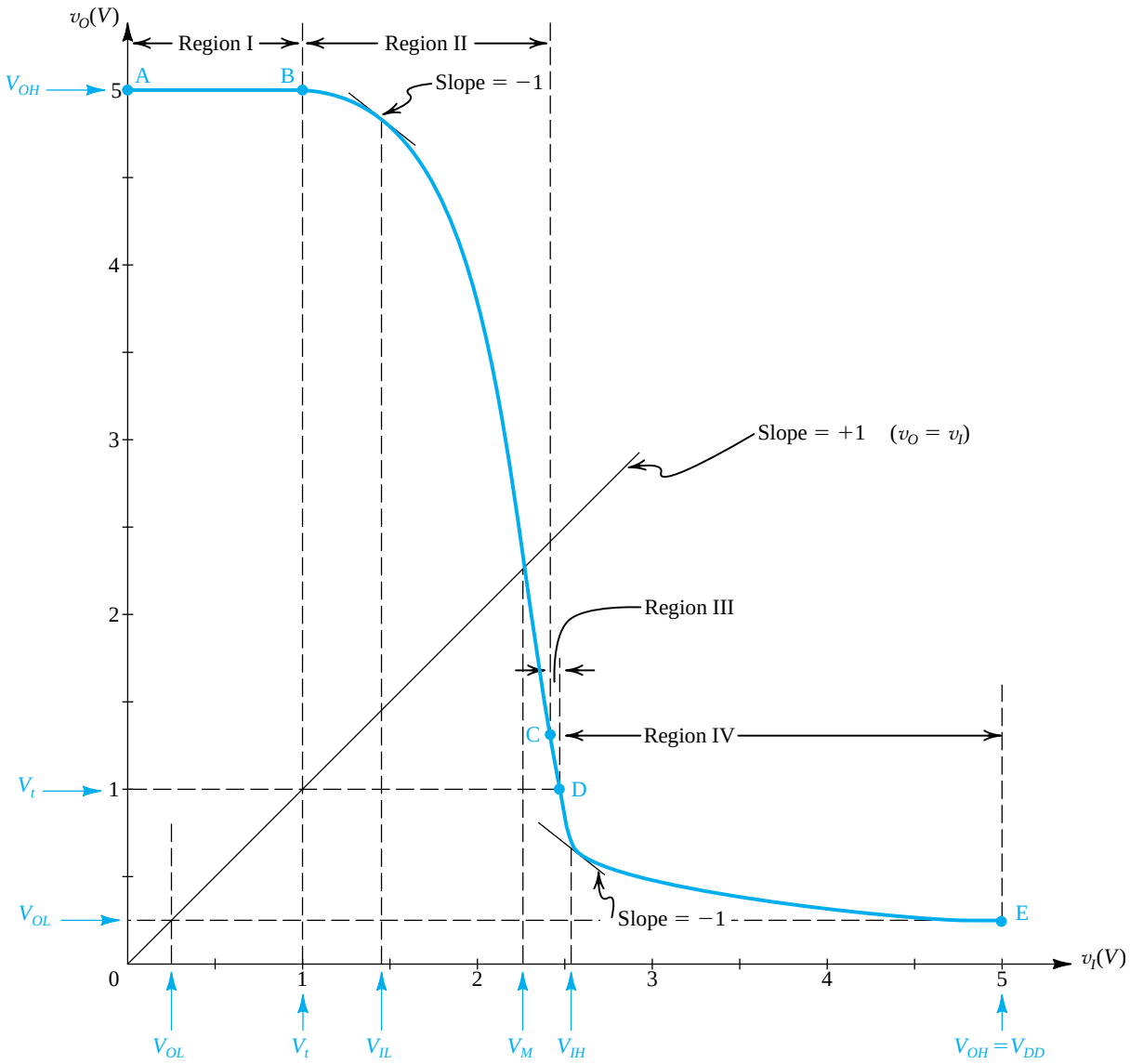

Figure 14.3 VTC for the pseudo-NMOS inverter. This curve is plotted for $V_{DD} = 5$ V, $V_{tn} = -V_{tp} = 1$ V, and $r = 9$.

Table 14.1 Regions of Operation of the Pseudo-NMOS Inverter

Region	Segment of VTC	Q_N	Q_P	Condition
I	AB	Cutoff	Triode	$v_I < V_t$
II	BC	Saturation	Triode	$v_O \geq v_I - V_t$
III	CD	Triode	Triode	$V_t \leq v_O \leq v_I - V_t$
IV	DE	Triode	Saturation	$v_O \leq V_t$

■ **Region I (segment AB):**

$$v_O = V_{OH} = V_{DD} \tag{14.5}$$

■ **Region II (segment BC):**
Equating i_{DN} from Eq. (14.1) and i_{DP} from Eq. (14.4) together with substituting $k_n = rk_p$, and with some manipulations, we obtain

$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2} \tag{14.6}$$

The value of V_{IL} can be obtained by differentiating this equation and substituting $\partial v_O / \partial v_I = -1$ and $v_I = V_{IL}$:

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}} \tag{14.7}$$

The threshold voltage V_M is by definition the value of v_I for which $v_O = v_I$,

$$V_M = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}} \tag{14.8}$$

Finally, the end of the region II segment (point C) can be found by substituting $v_O = v_I - V_t$ in Eq. (14.6), the condition for Q_N leaving saturation and entering the triode region.

■ **Region III (segment CD)**
This is a short segment that is not of great interest. Point D is characterized by $v_O = V_t$.

■ **Region IV (segment DE)**
Equating i_{DN} from Eq. (14.2) to i_{DP} from Eq. (14.3) and substituting $k_n = rk_p$ results in

$$v_O = (v_I - V_t) - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2} \tag{14.9}$$

The value of V_{IH} can be determined by differentiating this equation and setting $\partial v_O / \partial v_I = -1$ and $v_I = V_{IH}$,

$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t) \tag{14.10}$$

The value of V_{OL} can be found by substituting $v_I = V_{DD}$ into Eq. (14.9),

$$V_{OL} = (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}}\right] \tag{14.11}$$

The static current conducted by the inverter in the low-output state is found from Eq. (14.3) as

$$I_{\text{stat}} = \frac{1}{2}k_p(V_{DD} - V_t)^2 \tag{14.12}$$

Finally, we can use Eqs. (14.7) and (14.11) to determine NM_L and Eqs. (14.5) and (14.10) to determine NM_H:

$$NM_L = V_t - (V_{DD} - V_t)\left[1 - \sqrt{1 - \frac{1}{r}} - \frac{1}{\sqrt{r(r+1)}}\right] \tag{14.13}$$

$$NM_H = (V_{DD} - V_t)\left(1 - \frac{2}{\sqrt{3r}}\right) \tag{14.14}$$

As a final observation, we note that since V_{DD} and V_t are determined by the process technology, the only design parameter for controlling the values of V_{OL} and the noise margins is the ratio r.

14.1.4 Dynamic Operation

Analysis of the inverter transient response to determine t_{PLH} with the inverter loaded by a capacitance C is identical to that of the complementary CMOS inverter. The capacitance will be charged by the current i_{DP}; we can determine an estimate for t_{PLH} by using the average value of i_{DP} over the range $v_O = 0$ to $v_O = V_{DD}/2$. The result is:

$$t_{PLH} = \frac{\alpha_p C}{k_p V_{DD}} \tag{14.15}$$

where

$$\alpha_p = 2 \Big/ \left[\frac{7}{4} - 3\left(\frac{V_t}{V_{DD}}\right) + \left(\frac{V_t}{V_{DD}}\right)^2\right] \tag{14.16}$$

The case for the capacitor discharge is somewhat different because the current i_{DP} has to be subtracted from i_{DN} to determine the discharge current. The result is

$$t_{PHL} \simeq \frac{\alpha_n C}{k_n V_{DD}} \tag{14.17}$$

where

$$\alpha_n = 2 \Big/ \left[1 + \frac{3}{4}\left(1 - \frac{1}{r}\right) - \left(3 - \frac{1}{r}\right)\left(\frac{V_t}{V_{DD}}\right) + \left(\frac{V_t}{V_{DD}}\right)^2\right] \tag{14.18}$$

which, for a large value of r, reduces to

$$\alpha_n \simeq \alpha_p \tag{14.19}$$

Although these are similar formulas to those for the standard CMOS inverter, the pseudo-NMOS inverter has a special problem: Since k_p is r times smaller than k_n, t_{PLH} will be approximately r times larger than t_{PHL}. Thus the circuit exhibits an asymmetrical delay performance. Recall, however, that for gates with large fan-in, pseudo-NMOS requires fewer transistors and thus C can be smaller than in the corresponding standard CMOS gate.

14.1.5 Design

The design involves selecting the ratio r and the W/L for one of the transistors. The value of W/L for the other device can then be obtained using r. The design parameters of interest are V_{OL}, NM_L, NM_H, I_{stat}, P_D, t_{PLH}, and t_{PHL}. Important design considerations are as follows:

1. The ratio r determines all the breakpoints of the VTC; the larger the value of r, the lower V_{OL} is (Eq. 14.11) and the wider the noise margins are (Eqs. 14.13 and 14.14). However, a larger r increases the asymmetry in the dynamic response and, for a given $(W/L)_p$, makes the silicon area larger. Thus, selecting a value for r represents a compromise between noise margins on the one hand and silicon area and t_p on the other. Usually, r is selected in the range 4 to 10.

2. Once r has been determined, a value for $(W/L)_p$ or $(W/L)_n$ can be selected and the other determined. Here, one would select a small $(W/L)_n$ to keep the gate area small and thus obtain a small value for C. Similarly, a small $(W/L)_p$ keeps I_{stat} and P_D low. On the other hand, one would want to select larger W/L ratios to obtain low t_P and thus fast response. For usual (high-speed) applications, $(W/L)_p$ is selected so that I_{stat} is in the range of 50 µA to 100 µA, which for $V_{DD} = 1.8$ V results in P_D in the range of 90 µW to 180 µW.

14.1.6 Gate Circuits

Except for the load device, the pseudo-NMOS gate circuit is identical to the PDN of the complementary CMOS gate. Four-input, pseudo-NMOS NOR and NAND gates are shown in Fig. 14.4. Note that each requires five transistors compared to the eight used in standard CMOS. In pseudo-NMOS, NOR gates are preferred over NAND gates because the former do not utilize transistors in series and thus can be designed with minimum-size NMOS devices.

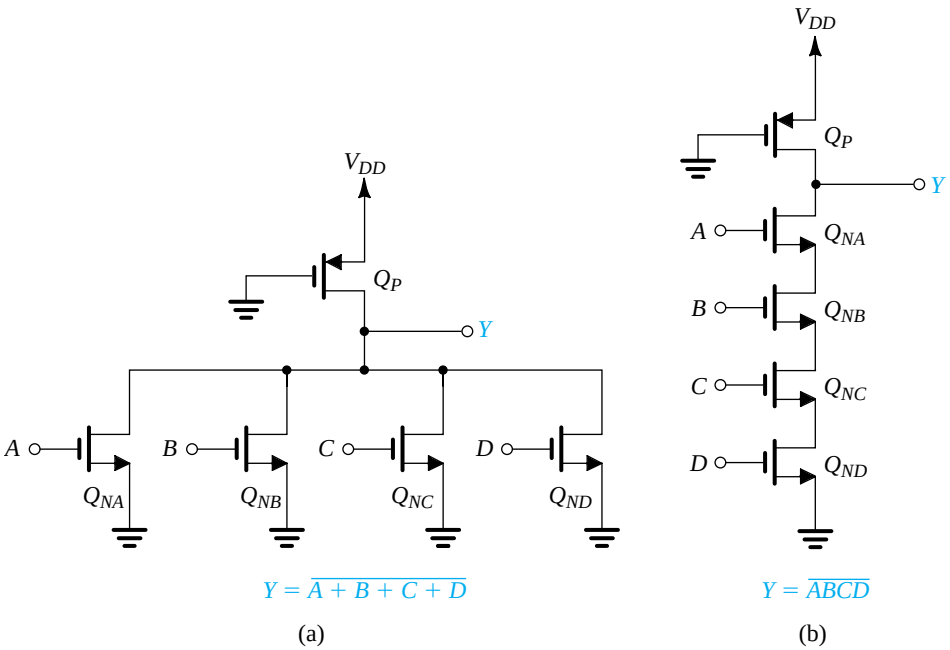

Figure 14.4 NOR and NAND gates of the pseudo-NMOS type.

14.1.7 Concluding Remarks

Pseudo-NMOS is particularly suited for applications in which the output remains high most of the time. In such applications, the static power dissipation can be reasonably low (since the gate dissipates static power only in the low-output state). Further, the output transitions that matter would presumably be high-to-low ones, where the propagation delay can be made as short as necessary. A particular application of this type can be found in the design of address decoders for memory chips (Section 15.4) and in read-only memories (Section 15.5).

Example 14.1

Consider a pseudo-NMOS inverter fabricated in a 0.25-μm CMOS technology for which $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.5$ V, and $V_{DD} = 2.5$ V. Let the W/L ratio of Q_N be (0.375 μm/0.25 μm) and $r = 9$. Find:

(a) V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, NM_H, and NM_L

(b) $(W/L)_p$

(c) I_{stat} and P_D

(d) t_{PLH}, t_{PHL}, and t_P, assuming a total capacitance at the inverter output of 7 fF

Solution

(a) $V_{OH} = V_{DD} = 2.5$ V

V_{OL} is determined from Eq. (14.11) as

$$V_{OL} = (2.5 - 0.5)\left[1 - \sqrt{1 - \frac{1}{9}}\right] = 0.11 \text{ V}$$

V_{IL} is determined from Eq. (14.7) as

$$V_{IL} = 0.5 + \frac{2.5 - 0.5}{\sqrt{9(9+1)}} = 0.71 \text{ V}$$

V_{IH} is determined from Eq. (14.10) as

$$V_{IH} = 0.5 + \frac{2}{\sqrt{3 \times 9}} \times (2.5 - 0.5) = 1.27 \text{ V}$$

V_M is determined from Eq. (14.8) as

$$V_M = 0.5 + \frac{2.5 - 0.5}{\sqrt{9+1}} = 1.13 \text{ V}$$

The noise margins can now be determined as

$$NM_H = V_{OH} - V_{IH} = 2.5 - 1.27 = 1.23 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.71 - 0.11 = 0.60 \text{ V}$$

Observe that the noise margins are not equal and that NM_L is rather low.

(b) The W/L ratio of Q_P can be found from

$$\frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = 9$$

$$\frac{115 \times \dfrac{0.375}{0.25}}{30(W/L)_p} = 9$$

Thus,

$$(W/L)_p = 0.64$$

Example 14.1 *continued*

(c) The dc current in the low-output state can be determined from Eq. (14.12) as

$$I_{\text{stat}} = \frac{1}{2} \times 30 \times 0.64(2.5 - 0.5)^2 = 38.4\ \mu\text{A}$$

The static power dissipation can now be found from

$$P_D = I_{\text{stat}} V_{DD}$$
$$= 38.4 \times 2.5 = 96\ \mu\text{W}$$

(d) The low-to-high propagation delay can be found by using Eqs. (14.15) and (14.16):

$$\alpha_p = 1.68$$

$$t_{PLH} = \frac{1.68 \times 7 \times 10^{-15}}{30 \times 10^{-6} \times 0.64 \times 2.5} = 0.25\ \text{ns}$$

The high-to-low propagation delay can be found by using Eqs. (14.17) and (14.18):

$$\alpha_n = 1.54$$

$$t_{PHL} = \frac{1.54 \times 7 \times 10^{-15}}{115 \times 10^{-6} \times \dfrac{0.375}{0.25} \times 2.5} = 0.03\ \text{ns}$$

Now, the propagation delay can be determined as

$$t_P = \frac{1}{2}(0.25 + 0.03) = 0.14\ \text{ns}$$

Although the propagation delay is considerably greater than that of a standard CMOS inverter, this is not an entirely fair comparison: Recall that the advantage of pseudo-NMOS occurs in gates with large fan-in, not in a single inverter.

EXERCISES

14.1 While keeping r unchanged, redesign the inverter circuit of Example 14.1 to lower its static power dissipation to half the value found. Find the W/L ratios for the new design. Also find t_{PLH}, t_{PHL}, and t_P, assuming that C remains unchanged. Would the noise margins change?
Ans. $(W/L)_n = 1.5$; $(W/L)_p = 0.32$; 0.5 ns; 0.03 ns; 0.27 ns; no

14.2 Redesign the inverter of Example 14.1 using $r = 4$. Find V_{OL} and the noise margins. If $(W/L)_n = 0.375\ \mu\text{m}/0.25\ \mu\text{m}$, find $(W/L)_p$, I_{stat}, P_D, t_{PLH}, t_{PHL}, and t_p. Assume $C = 7$ fF.
Ans. $V_{OL} = 0.27$ V; $NM_L = 0.68$ V; $NM_H = 0.85$ V; $(W/L)_p = 1.44$; $I_{\text{stat}} = 86.3\ \mu$A; $P_D = 0.22$ mW; $t_{PLH} = 0.11$ ns; $t_{PHL} = 0.03$ ns; $t_P = 0.07$ ns

14.2 Pass-Transistor Logic Circuits

A conceptually simple approach for implementing logic functions utilizes series and parallel combinations of switches that are controlled by input logic variables to connect the input

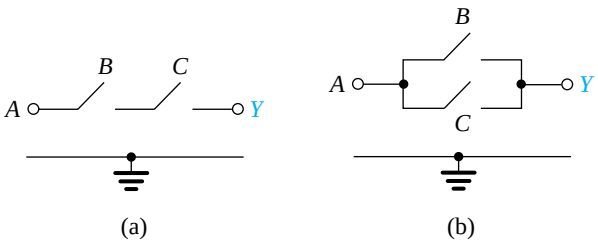

Figure 14.5 Conceptual pass-transistor logic gates. **(a)** Two switches, controlled by the input variables B and C, when connected in series in the path between the input node to which an input variable A is applied and the output node (with an implied load to ground) realize the function $Y = ABC$. **(b)** When the two switches are connected in parallel, the function realized is $Y = A(B + C)$.

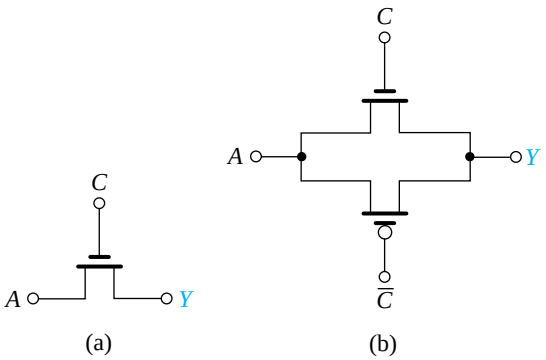

Figure 14.6 Two possible implementations of a voltage-controlled switch connecting nodes A and Y: **(a)** single NMOS transistor and **(b)** CMOS transmission gate.

and output nodes (see Fig. 14.5). Each of the switches can be implemented either by a single NMOS transistor (Fig. 14.6) or by a pair of complementary MOS transistors connected in what is known as the **CMOS transmission-gate** configuration (Fig. 14.6). The result is a simple form of logic circuit that is particularly suited for some special logic functions and is frequently used in conjunction with standard CMOS logic to implement such functions efficiently: that is, with a lower total number of transistors than is possible with CMOS alone.

Because this form of logic utilizes MOS transistors in the series path from input to output, to *pass* or block signal transmission, it is known as *pass-transistor logic* (PTL). As mentioned earlier, CMOS transmission gates are frequently employed to implement the switches, giving this logic-circuit form the alternative name, *transmission-gate logic*. The terms are used interchangeably independent of the actual implementation of the switches.

Though conceptually simple, pass-transistor logic circuits have to be designed with care. In the following, we shall study the basic principles of PTL circuit design and present examples of its application.

14.2.1 An Essential Design Requirement

An essential requirement in the design of PTL circuits is ensuring that *every circuit node has at all times a low-resistance path either to* V_{DD} *or to ground.* To appreciate this point,

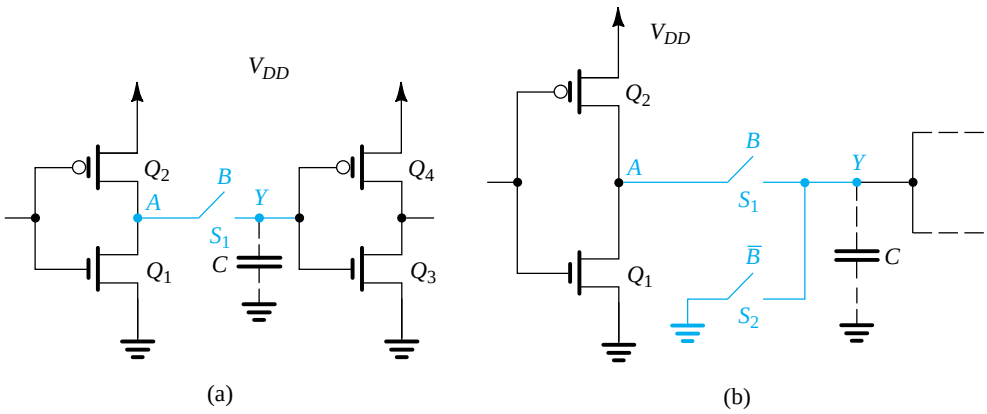

Figure 14.7 A basic design requirement of PTL circuits is that every node have, at all times, a low-resistance path to either ground or V_{DD}. Such a path does not exist in **(a)** when B is low and S_1 is open. It is provided in **(b)** through switch S_2.

consider the situation depicted in Fig. 14.7(a): A switch S_1 (usually part of a larger PTL network, not shown) is used to form the AND function of its controlling variable B and the variable A available at the output of a CMOS inverter. The output Y of the PTL circuit is shown connected to the input of another inverter. Now, if B is high, S_1 closes and $Y = A$. Node Y will then be connected either to V_{DD} (if A is high) through Q_2 or to ground (if A is low) through Q_1. But what happens when B goes low and S_1 opens? Node Y will now become a high-impedance node. If initially v_Y was zero, it will remain so. However, if initially v_Y was high at V_{DD}, this voltage will be maintained by the charge on the parasitic capacitance C, and Y will not be a logic 0 as required of the AND function.

The problem can be easily solved by establishing for node Y a low-resistance path that is activated when B goes low, as shown in Fig. 14.7(b). Here, another switch, S_2, controlled by $\overline{B}$, is connected between Y and ground. When B goes low, S_2 closes and establishes a low-resistance path between Y and ground. The voltage v_Y will then be 0 volts, the proper output of the AND function when B is zero.

14.2.2 Operation with NMOS Transistors as Switches

Implementing the switches in a PTL circuit with single NMOS transistors results in a simple circuit with small area and small node capacitances. These advantages, however, are obtained at the expense of serious shortcomings in both the static characteristics and the dynamic performance of the resulting circuits. To illustrate, consider the circuit shown in Fig. 14.8, where an NMOS transistor Q is used to implement a switch connecting an input node with voltage v_I and an output node. The total capacitance between the output node and ground is represented by capacitor C. The switch is shown in the closed state with the control signal applied to its gate being high at V_{DD}. We wish to analyze the operation of the circuit as the input voltage v_I goes high (to V_{DD}) at time $t = 0$. We assume that initially the output voltage v_O is zero and capacitor C is fully discharged.[3]

[3]Although the MOS transistor is symmetric and its drain and source are interchangeable, it is always useful to know which terminal is functioning as the source and which as the drain. The terminal with the higher voltage in an NMOS transistor is the drain. The opposite is true for the PMOS transistor.

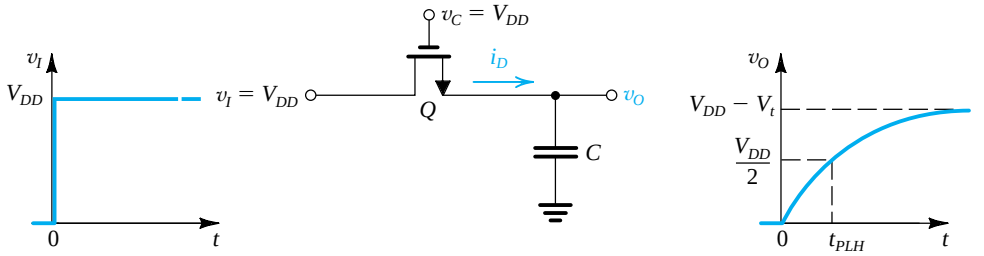

Figure 14.8 Operation of the NMOS transistor as a switch in the implementation of PTL circuits. This analysis is for the case with the switch closed (v_C is high) and the input going high ($v_I = V_{DD}$).

When v_I goes high, the transistor operates in the saturation mode and delivers a current i_D to charge the capacitor,

$$i_D = \frac{1}{2}k_n(V_{DD} - v_O - V_t)^2 \tag{14.20}$$

where $k_n = k_n'(W/L)$, and V_t is determined by the body effect since the source is at a voltage v_O relative to the body (which, though not shown, is connected to ground); thus (see Eq. 5. 107),

$$V_t = V_{t0} + \gamma\,(\sqrt{v_O + 2\phi_f} - \sqrt{2\phi_f}) \tag{14.21}$$

Thus, initially (at $t = 0$), $V_t = V_{t0}$ and the current i_D is relatively large. However, as C charges up and v_O rises, V_t increases (Eq. 14.21) and i_D decreases. The latter effect is due to both the increase in v_O and in V_t. It follows that the process of charging the capacitor will be relatively slow. More seriously, observe from Eq. (14.20) that i_D reduces to zero when v_O reaches ($V_{DD} - V_t$). Thus the high output voltage (V_{OH}) will *not* be equal to V_{DD}; rather, it will be lower by V_t, and to make matters worse, the value of V_t can be as high as 1.5 to 2 times V_{t0}!

In addition to reducing the gate noise immunity, the low value of V_{OH} (commonly referred to as a "poor 1") has another detrimental effect: Consider what happens when the output node is connected to the input of a standard CMOS inverter (as was the case in Fig. 14.7). The low value of V_{OH} can cause Q_P of the load inverter to conduct. Thus the inverter will have a finite static current and static power dissipation.

The propagation delay t_{PLH} of the PTL gate of Fig. 14.8 can be determined as the time for v_O to reach $V_{DD}/2$. This can be calculated using techniques similar to those employed in the analysis of the CMOS inverter in Section 13.3, as will be illustrated shortly in an example.

Figure 14.9 shows the NMOS switch circuit when v_I is brought down to 0 V. We assume that initially $v_O = V_{DD}$. Thus at $t = 0+$, the transistor conducts and operates in the saturation region,

$$i_D = \frac{1}{2}k_n(V_{DD} - V_t)^2 \tag{14.22}$$

where we note that since the source is now at 0 V (note that the drain and source have interchanged roles), there will be no body effect, and V_t remains constant at V_{t0}. As C discharges, v_O decreases and the transistor enters the triode region at $v_O = V_{DD} - V_t$. Nevertheless, the capacitor discharge continues until C is fully discharged and $v_O = 0$. Thus, the NMOS transistor provides $V_{OL} = 0$, or a "good 0." Again, the propagation delay t_{PHL} can be determined using usual techniques, as illustrated by the following example.

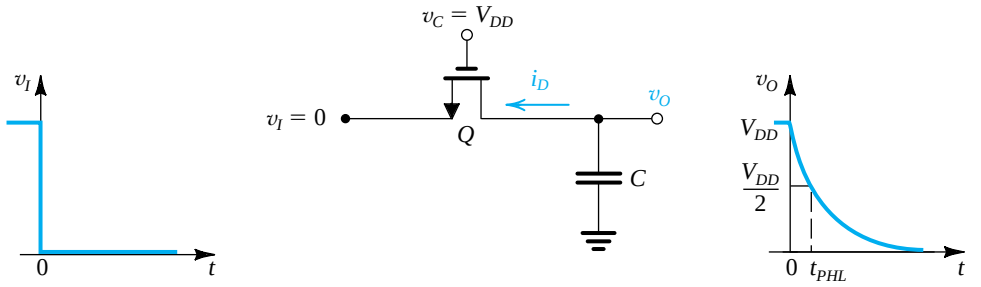

Figure 14.9 Operation of the NMOS switch as the input goes low ($v_I = 0$ V). Note that the drain of an NMOS transistor is always higher in voltage than the source; correspondingly, the drain and source terminals interchange roles in comparison to the circuit in Fig. 14.8.

Example 14.2

Consider the NMOS transistor switch in the circuits of Figs. 14.8 and 14.9 to be fabricated in a technology for which $\mu_n C_{ox} = 50\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 20\ \mu\text{A/V}^2$, $|V_{t0}| = 1$ V, $\gamma = 0.5\ \text{V}^{1/2}$, $2\phi_f = 0.6$ V, and $V_{DD} = 5$ V, where ϕ_f is a physical parameter. Let the transistor be of the minimum size for this technology, namely, 4 µm/2 µm, and assume that the total capacitance between the output node and ground is $C = 50$ fF.

(a) For the case with v_I high (Fig. 14.8), find V_{OH}.
(b) If the output feeds a CMOS inverter whose $(W/L)_p = 2.5\,(W/L)_n = 10\ \mu\text{m}/2\ \mu\text{m}$, find the static current of the inverter and its power dissipation when its input is at the value found in (a). Also find the inverter output voltage.
(c) Find t_{PLH}.
(d) For the case with v_I going low (Fig. 14.9), find t_{PHL}.
(e) Find t_P.

Solution

(a) Refer to Fig. 14.8. If V_{OH} is the value of v_O at which Q stops conducting,

$$V_{DD} - V_{OH} - V_t = 0$$

then,

$$V_{OH} = V_{DD} - V_t$$

where V_t is the value of the threshold voltage at a source–body reverse bias equal to V_{OH}. Using Eq. (14.21), we have

$$\begin{aligned} V_t &= V_{t0} + \gamma\,(\sqrt{V_{OH} + 2\phi_f} - \sqrt{2\phi_f}) \\ &= V_{t0} + \gamma\,(\sqrt{V_{DD} - V_t + 2\phi_f} - \sqrt{2\phi_f}) \end{aligned}$$

Substituting $V_{t0} = 1$, $\gamma = 0.5$, $V_{DD} = 5$, and $2\phi_f = 0.6$, we obtain a quadratic equation in V_t whose solution yields

$$V_t = 1.6\ \text{V}$$

Thus,

$$V_{OH} = 3.4\ \text{V}$$

Note that this represents a significant loss in signal amplitude.

(b) The load inverter will have an input signal of 3.4 V. Thus, its Q_P will conduct a current of

$$i_{DP} = \frac{1}{2} \times 20 \times \frac{10}{2}(5 - 3.4 - 1)^2 = 18 \ \mu\text{A}$$

where we have assumed Q_P to be operating in saturation, as we still expect v_O of the inverter to be close to 0. Thus, the static power dissipation of the inverter will be

$$P_D = V_{DD} i_{DP} = 5 \times 18 = 90 \ \mu\text{W}$$

The output voltage of the inverter can be found by noting that Q_N will be operating in the triode region. Equating its current to that of Q_P (i.e., 18 μA) enables us to determine the output voltage to be 0.08 V.

(c) To determine t_{PLH}, refer to Fig 14.8. We need to find the current i_D at $t = 0$ (where $v_O = 0$, $V_t = V_{t0} =$ 1 V) and at $t = t_{PLH}$ (where $v_O = 2.5$ V, V_t to be determined), as follows:

$$i_D(0) = \frac{1}{2} \times 50 \times \frac{4}{2} \times (5 - 1)^2 = 800 \ \mu\text{A}$$

$$V_t \ (\text{at } v_O = 2.5 \text{ V}) = 1 + 0.5(\sqrt{2.5 + 0.6} - \sqrt{0.6}) = 1.49 \text{ V}$$

$$i_D(t_{PLH}) = \frac{1}{2} \times 50 \times \frac{4}{2}(5 - 2.5 - 1.49)^2 = 50 \ \mu\text{A}$$

We can now compute the average discharge current as

$$i_D\big|_{\text{av}} = \frac{800 + 50}{2} = 425 \ \mu\text{A}$$

and t_{PLH} can be found as

$$t_{PLH} = \frac{C(V_{DD}/2)}{i_D\big|_{\text{av}}}$$

$$= \frac{50 \times 10^{-15} \times 2.5}{425 \times 10^{-6}} = 0.29 \text{ ns}$$

(d) Refer to the circuit in Fig. 14.9. Observe that, here, V_t remains constant at $V_{t0} = 1$ V. At $t = 0$, Q will be operating in saturation, and the drain current will be

$$i_D(0) = \frac{1}{2} \times 50 \times \frac{4}{2}(5 - 1)^2 = 800 \ \mu\text{A}$$

At $t = t_{PHL}$, Q will be operating in the triode region, and thus

$$i_D(t_{PHL}) = 50 \times \frac{4}{2}\left[(5 - 1) \times 2.5 - \frac{1}{2} \times 2.5^2\right]$$

$$= 690 \ \mu\text{A}$$

Thus, the average discharge current is given by

$$i_D\big|_{\text{av}} = \frac{1}{2}(800 + 690) = 740 \ \mu\text{A}$$

and t_{PHL} can be determined as

$$t_{PHL} = \frac{50 \times 10^{-15} \times 2.5}{740 \times 10^{-6}} = 0.17 \text{ ns}$$

(e) $t_P = \frac{1}{2}(t_{PLH} + t_{PHL}) = \frac{1}{2}(0.29 + 0.17) = 0.23$ ns

EXERCISE

14.3 Let the NMOS transistor switch in Fig. 14.8 be fabricated in a 0.18-μm CMOS process for which $V_{t0} = 0.5$ V, $\gamma = 0.3\ \text{V}^{1/2}$, $2\phi_f = 0.85$ V, and $V_{DD} = 1.8$ V. Find V_{OH}.

Ans. 1.15 V

14.2.3 Restoring the Value of V_{OH} to V_{DD}

Example 14.2 illustrates clearly the problem of signal-level loss and its deleterious effect on the operation of the succeeding CMOS inverter. Some rather ingenious techniques have been developed to restore the output level to V_{DD}. We shall briefly discuss two such techniques. One is circuit-based and the other is based on process technology.

The circuit-based approach is illustrated in Fig. 14.10. Here, Q_1 is a pass-transistor controlled by input B. The output node of the PTL network is connected to the input of a standard CMOS inverter formed by Q_N and Q_P. A PMOS transistor Q_R, whose gate is controlled by the output voltage of the inverter, v_{O2}, has been added to the circuit. Observe that in the event that the output of the PTL gate, v_{O1}, is low (at ground), v_{O2} will be high (at V_{DD}), and Q_R will be off. On the other hand, if v_{O1} is high but not quite equal to V_{DD}, the output of the inverter will be low (as it should be) and Q_R will turn on, supplying a current to charge C up to V_{DD}. This process will stop when $v_{O1} = V_{DD}$, that is, when the output voltage has been restored to its proper level. The "level-restoring" function performed by Q_R is frequently employed in MOS digital-circuit design. It should be noted that although the description of operation is relatively straight forward, the addition of Q_R closes a "positive-feedback" loop around the CMOS inverter, and thus operation is more involved than it appears, especially during transients. Selection of a W/L ratio for Q_R is also a somewhat involved process, although normally k_r is selected to be much lower than k_n (say a third or a fifth as large). Intuitively, this is appealing, for it implies that Q_R will not play a major role in circuit operation, apart from restoring the level of V_{OH} to V_{DD}, as explained above. Transistor Q_R is said to be a "weak PMOS transistor." See Problem 14.17.

The other technique for correcting for the loss of the high-output signal level (V_{OH}) is a technology-based solution. Specifically, recall that the loss in the value of V_{OH} is equal to V_{tn}. It follows that we can reduce the loss by using a lower value of V_{tn} for the NMOS switches, and we can eliminate the loss altogether by using devices for which $V_{tn} = 0$. These **zero-threshold devices** can be fabricated by using ion implantation to control the value of V_{tn} and are known as

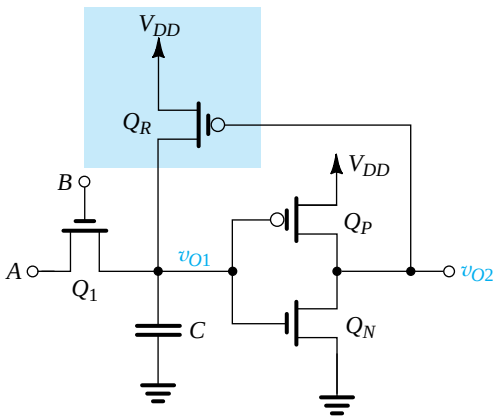

Figure 14.10 The use of transistor Q_R, connected in a feedback loop around the CMOS inverter, to restore the V_{OH} level, produced by Q_1, to V_{DD}.

natural devices. The problem of low-threshold devices, however, is the increased subthreshold conduction (Section 13.5.3) and the corresponding increase in static power dissipation.

14.2.4 The Use of CMOS Transmission Gates as Switches

Great improvements in static and dynamic performance are obtained when the switches are implemented with CMOS transmission gates. The transmission gate utilizes a pair of complementary transistors connected in parallel. It acts as an excellent switch, providing bidirectional current flow, and it exhibits an "on" resistance that remains almost constant for wide ranges of input voltage. These characteristics make the transmission gate not only an excellent switch in digital applications but also an excellent analog switch in such applications as data converters and switched-capacitor filters (Chapter 16).

Before we analyze the transmission gate circuit, it is useful to reflect on its origin. Recall that an NMOS transistor transmits the 0-V level to the output perfectly and thus produces a "good 0." It has difficulty, however, in passing the V_{DD} level, with the result that $V_{OH} = V_{DD} - V_t$ (a "poor 1"). It can be shown (see Problem 14.18) that a PMOS transistor does exactly the opposite; that is, it passes the V_{DD} level perfectly and thus produces a "good 1" but has trouble passing the 0-V level, thus producing a "poor 0." It is natural therefore to think that placing an NMOS and a PMOS transistor in parallel would produce good results in both the 0 and 1 cases.

Another way to describe the performance of the two transistor types is that the NMOS is good at pulling the output down to 0 V, while the PMOS is good at pulling the output up to V_{DD}. Interestingly, these are also the roles they play in the standard CMOS inverter.

Figure 14.11 shows the transmission gate together with its frequently used circuit symbol. The transmission gate is a bilateral switch that results in $v_Y = v_X$ when v_C is high (V_{DD}). In terms of logic variables, its function is described by

$$Y = X \quad \text{if} \quad C = 1$$

Figure 14.12(a) shows the transmission-gate switch in the "on" position with the input, v_I, rising to V_{DD} at $t = 0$. Assuming, as before, that initially the output voltage is zero, we see that Q_N will be operating in saturation and providing a charging current of

$$i_{DN} = \frac{1}{2}k_n(V_{DD} - v_O - V_{tn})^2 \tag{14.23}$$

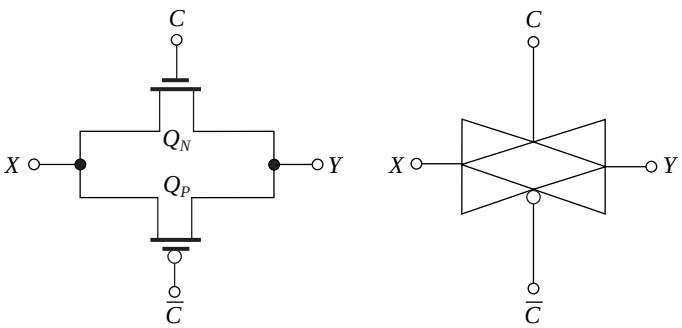

Figure 14.11 The CMOS transmission gate and its circuit symbol.

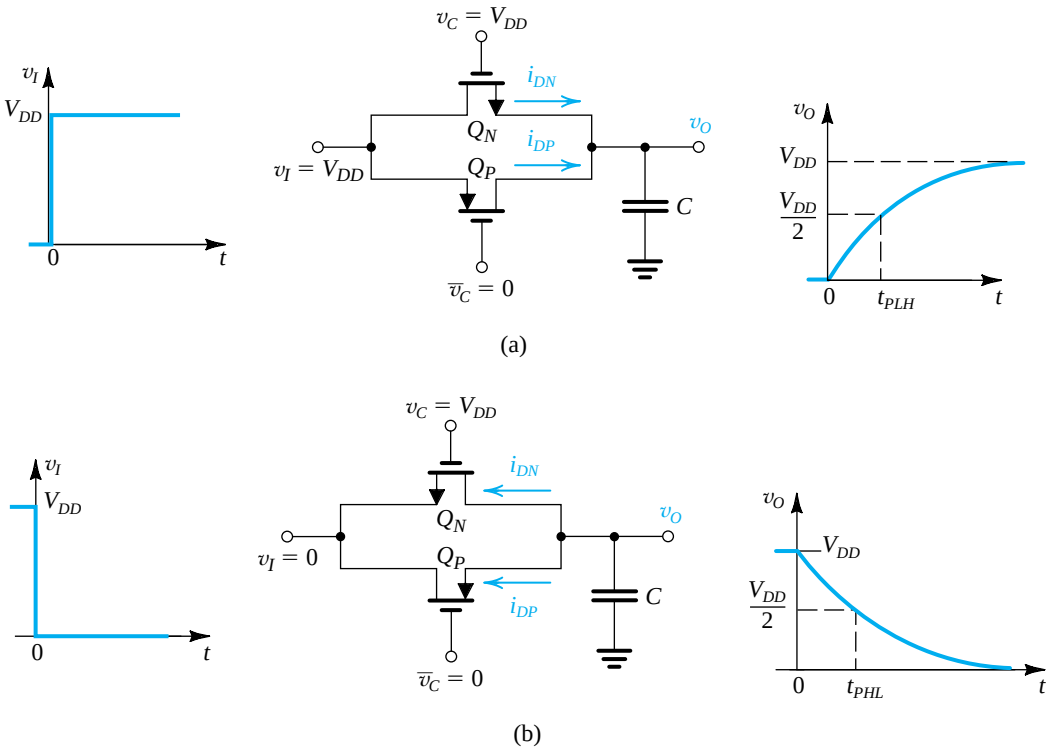

Figure 14.12 Operation of the transmission gate as a switch in PTL circuits with **(a)** v_I high and **(b)** v_I low.

where, as in the case of the single NMOS switch, V_{tn} is determined by the body effect,

$$V_{tn} = V_{t0} + \gamma(\sqrt{v_O + 2\phi_f} - \sqrt{2\phi_f}) \tag{14.24}$$

Transistor Q_N will conduct a diminishing current that reduces to zero at $v_O = V_{DD} - V_{tn}$. Observe, however, that Q_P operates with $V_{SG} = V_{DD}$ and is initially in saturation,

$$i_{DP} = \frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2 \tag{14.25}$$

where, since the body of Q_P is connected to V_{DD}, $|V_{tp}|$ remains constant at the value V_{t0}, assumed to be the same value as for the *n*-channel device. The total capacitor-charging current is the sum of i_{DN} and i_{DP}. Now, Q_P will enter the triode region at $v_O = |V_{tp}|$, but will continue to conduct until C is fully charged and $v_O = V_{OH} = V_{DD}$. Thus, the *p*-channel device will provide the gate with a "good 1." The value of t_{PLH} can be calculated using usual techniques, where we expect that as a result of the additional current available from the PMOS device, for the same value of C, t_{PLH} will be lower than in the case of the single NMOS switch. Note, however, that adding the PMOS transistor increases the value of C.

When v_I goes low, as shown in Fig. 14.12(b), Q_N and Q_P interchange roles. Analysis of the circuit in Fig. 14.12(b) will indicate that Q_P will cease conduction when v_O falls to $|V_{tp}|$, where $|V_{tp}|$ is given by

$$|V_{tp}| = V_{t0} + \gamma\left[\sqrt{V_{DD} - v_O + 2\phi_f} - \sqrt{2\phi_f}\right] \tag{14.26}$$

Transistor Q_N, however, continues to conduct until C is fully discharged and $v_O = V_{OL} = 0$ V, a "good 0."

We conclude that transmission gates provide far superior performance, both static and dynamic, than is possible with single NMOS switches. The price paid is increased circuit complexity, area, and capacitance.

EXERCISE

14.4 The transmission gate of Figs. 14.12(a) and 14.12(b) is fabricated in a CMOS process technology for which $k_n' = 50\ \mu A/V^2$, $k_p' = 20\ \mu A/V^2$, $V_{tn} = |V_{tp}|$, $V_{t0} = 1$ V, $\gamma = 0.5\ V^{1/2}$, $2\phi_f = 0.6$ V, and $V_{DD} = 5$ V. Let Q_N and Q_P be of the minimum size possible with this process technology, $(W/L)_n = (W/L)_p = 4\ \mu m/2\ \mu m$. The total capacitance at the output node is 70 fF. Utilize as many of the results of Example 14.2 as you need.

(a) What are the values of V_{OH} and V_{OL}?

(b) For the situation in Fig. 14.12(a), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PLH})$, $i_{DP}(t_{PLH})$, and t_{PLH}.

(c) For the situation depicted in Fig. 14.12(b), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PHL})$, $i_{DP}(t_{PHL})$, and t_{PHL}. At what value of v_O will Q_P turn off?

(d) Find t_P

Ans. (a) 5 V, 0 V; (b) 800 μA, 320 μA, 50 μA, 275 μA, 0.24 ns; (c) 800 μA, 320 μA, 688 μA, 20 μA, 0.19 ns, 1.6 V; (d) 0.22 ns

Equivalent Resistance of the Transmission Gate Although the transmission gate is capable of passing the full 1 and 0 levels to the load capacitance, it is not a perfect switch. In particular, the transmission gate has a finite "on" resistance. It is useful for us to obtain an estimate for this resistance. It can, for instance, be used together with the load capacitance as an alternative means to determining propagation delay. This approach is particularly useful in situations involving a network of inverters and transmission gates, as we shall shortly see.

To obtain an estimate of the resistance of the transmission gate, we shall consider the situation in Fig. 14.12(a), where the transmission gate is on and is passing a high input (V_{DD}) to the capacitor load. Transistor Q_N operates in saturation until the output voltage v_O reaches $(V_{DD} - V_{tn})$, at which time Q_N turns off; thus,

$$i_{DN} = \frac{1}{2}k_n(V_{DD} - V_{tn} - v_O)^2 \quad \text{for} \quad v_O \le V_{DD} - V_{tn} \tag{14.27}$$

$$i_{DN} = 0 \quad \text{for} \quad v_O \ge V_{DD} - V_{tn} \tag{14.28}$$

A gross estimate for the equivalent resistance of Q_N can be obtained by dividing the voltage across it, $(V_{DD} - v_O)$, by i_{DN}, and neglecting the body effect, that is, assuming V_{tn} remains constant; thus,

$$R_{Neq} = \frac{V_{DD} - v_O}{\frac{1}{2}k_n(V_{DD} - V_{tn} - v_O)^2} \quad \text{for} \quad v_O \le V_{DD} - V_{tn} \tag{14.29}$$

and

$$R_{Neq} = \infty \quad \text{for} \quad v_O \ge V_{DD} - V_{tn} \tag{14.30}$$

Transistor Q_P will operate in saturation until $v_O = |V_{tp}|$, after which it enters the triode region; thus,

$$i_{DP} = \frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2 \quad \text{for} \quad v_O \le |V_{tp}| \tag{14.31}$$

$$i_{DP} = k_p\left[(V_{DD} - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right] \quad \text{for} \quad v_O \ge |V_{tp}| \tag{14.32}$$

A gross estimate for the resistance of Q_P can be obtained by dividing the voltage across it, $(V_{DD} - v_O)$, by i_{DP}; thus,

$$R_{Peq} = \frac{V_{DD} - v_O}{\frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2} \quad \text{for} \quad v_O \le |V_{tp}| \tag{14.33}$$

$$R_{Peq} = \frac{1}{k_p\left[V_{DD} - |V_{tp}| - \frac{1}{2}(V_{DD} - v_O)\right]} \quad \text{for} \quad v_O \ge |V_{tp}| \tag{14.34}$$

Finally, the equivalent resistance R_{TG} of the transmission gate can be obtained as the parallel equivalent of R_{Neq} and R_{Peq},

$$R_{TG} = R_{Neq} \parallel R_{Peq} \tag{14.35}$$

Obviously, R_{TG} is a function of the output voltage v_O. As an example, we show in Fig. 14.13 a plot for R_{TG} for the transmission gate analyzed in Exercise 14.4. Observe that R_{TG} remains relatively constant over the full range of v_O. The average value of R_{TG} over the range $v_O = 0$ to $V_{DD}/2$ can be used to determine t_{PLH}, as illustrated in Exercise 14.5.

EXERCISE

14.5 For the transmission gate analyzed in Exercise 14.4, whose equivalent resistance for capacitor charging is plotted in Fig. 14.13, use the average resistance value over the range $v_O = 0$ V to 2.5 V to determine t_{PLH}. Compare the result to that obtained using average currents in Exercise 14.4. Note that from the graph, $R_{TG} = 4.5$ kΩ at $v_O = 0$ V, and $R_{TG} = 6.5$ kΩ at $v_O = 2.5$ V. Recall that $t_{PLH} = 0.69RC$.

Ans. $t_{PLH} = 0.27$ ns, very close to the value of 0.24 ns obtained in Exercise 14.4

The expression for R_{TG} derived above applies only to the case of capacitor charging. A similar analysis can be performed for the case of capacitor discharge illustrated in Fig. 14.12(b). The resulting value of R_{TG} is close to that obtained above (see Problem 14.21).

Similar to the empirical formulas for R_N and R_P of the CMOS inverter (Eqs. 13.70 and 13.71), there is a simple empirical formula for R_{TG} that applies for both capacitor charging and discharging and for all modern submicron technologies (see Hodges et al., 2004), namely,

$$R_{TG} \simeq \frac{12.5}{(W/L)_n}\ \text{k}\Omega \tag{14.36}$$

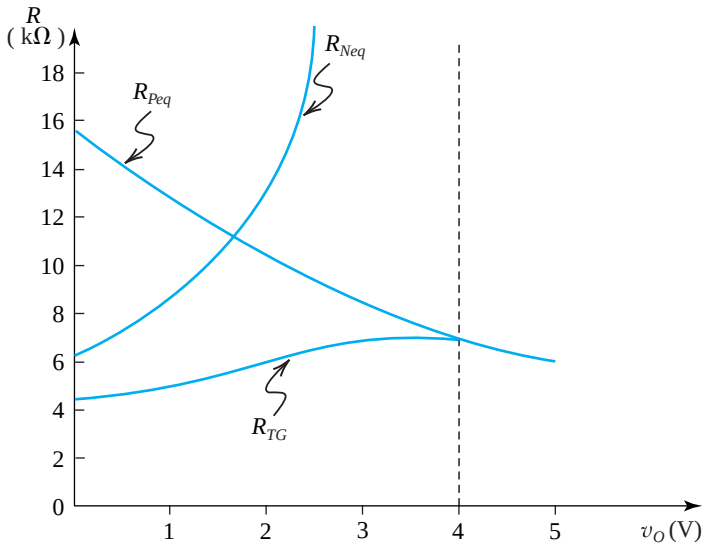

Figure 14.13 Plot of the equivalent resistances of the two transistors of the transmission gate in Fig. 14.12(a) and the overall resistance R_{TG} versus v_O. The data apply to the situation specified in Exercise 14.5.

EXERCISE

14.6 Use Eq. (14.36) to estimate the value of R_{TG} for a transmission gate fabricated in a 0.18-μm CMOS technology with $(W/L)_n = (W/L)_p = 1.5$.

Ans. 8.3 kΩ

Having an estimate of the resistance of the transmission gate enables us to calculate the propagation delay of a signal path containing one or more transmission gates. Figure 14.14(a) shows one such circuit. It consists of a transmission gate connecting the output of an inverter to the input of another. We are interested in finding the propagation delay from the input of the first inverter to the input of the second as we apply a negative going step to the input of the first inverter.

Fig. 14.14(b) shows the equivalent circuit where R_{P1} is the equivalent resistance of Q_{P1}, R_{TG} is the equivalent resistance of the transmission gate, C_{out1} is the output capacitance of the driver inverter, C_{TG1} and C_{TG2} are the capacitances introduced by the transmission gate at its input and output, respectively, and C_{in2} is the input capacitance of the load inverter. Observe that the circuit takes the form of an *RC* ladder network. A simple formula has been developed for calculating the delay of an arbitrarily long *RC* ladder network such as that shown in Fig. 14.15 having three sections. Known as the **Elmore delay formula**, it gives for the ladder in Fig. 14.15

$$t_P = 0.69[C_1R_1 + C_2(R_1 + R_2) + C_3(R_1 + R_2 + R_3)] \tag{14.37}$$

Applying the Elmore formula to the two-stage ladder in Fig. 14.14(b) gives

$$t_P = 0.69[(C_{\text{out1}} + C_{TG1})R_1 + (C_{\text{in2}} + C_{TG2})(R_1 + R_2)] \tag{14.38}$$

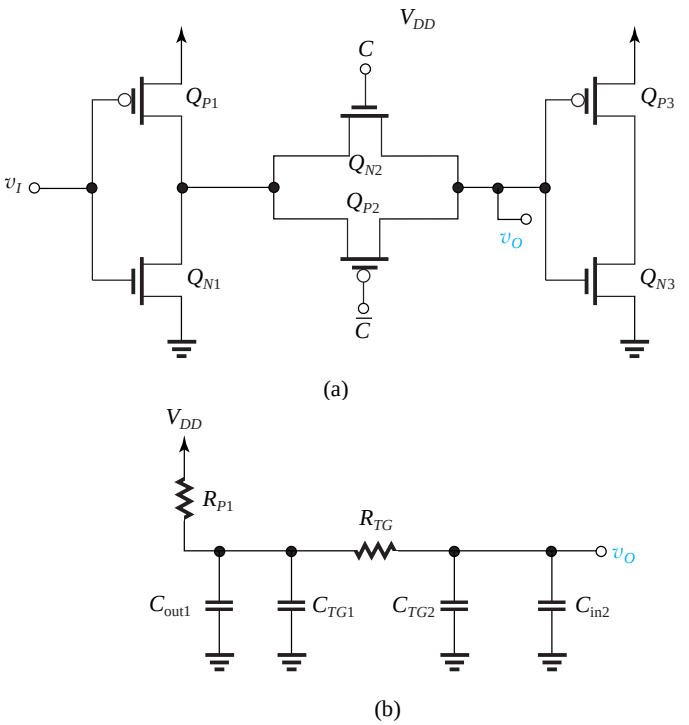

Figure 14.14 (**a**) A transmission gate connects the output of a CMOS inverter to the input of another. (**b**) Equivalent circuit for the purpose of analyzing the propagation delay of the circuit in (**a**).

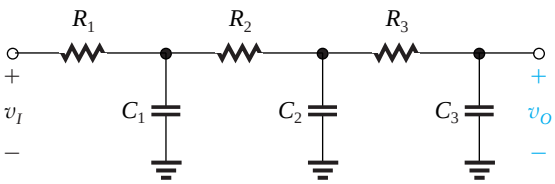

Figure 14.15 A three-section *RC* ladder network.

EXERCISE

14.7 The circuit in Fig. 14.14 is fabricated in a 0.13-µm CMOS technology; Q_P of the first inverter has $W/L = 2$, and both transistors of the transmission gate have $W/L = 1$. The capacitances have been estimated to be $C_{out1} = 10$ fF, $C_{TG1} = C_{TG2} = 5$ fF, and $C_{in2} = 10$ fF. Use the empirical formulas to obtain the values of R_{P1} and R_{TG}. Then, determine an estimate for t_P.

Ans. $R_{P1} = 15\ \text{k}\Omega$; $R_{TG} = 12.5\ \text{k}\Omega$; $t_P = 0.64$ ns

14.2.5 Pass-Transistor Logic Circuit Examples

We conclude this section by showing examples of PTL logic circuits. Figure 14.16 shows a PTL realization of a two-to-one multiplexer: Depending on the logic value of C, either A or B is connected to the output Y. The circuit realizes the Boolean function

$$Y = CA + \overline{C}B$$

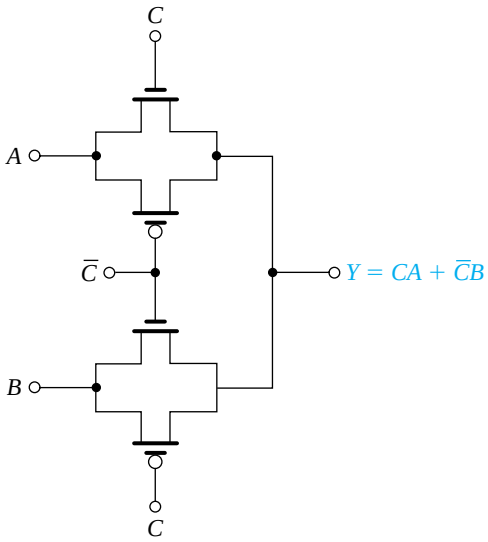

Figure 14.16 Realization of a two-to-one multiplexer using pass-transistor logic.

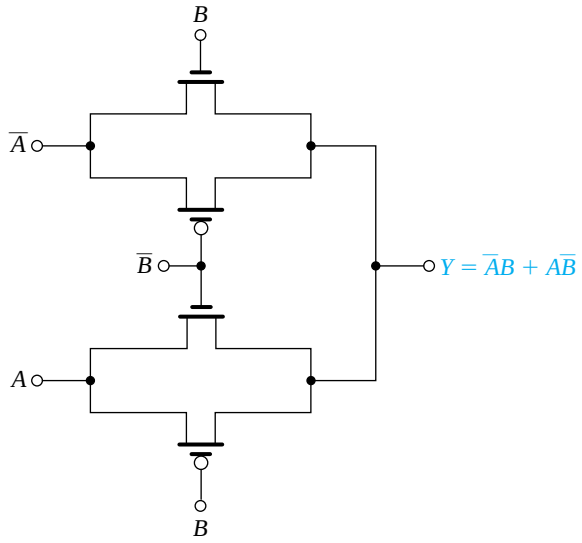

Figure 14.17 Realization of the XOR function using pass-transistor logic.

Our second example is an efficient realization of the exclusive-OR (XOR) function. The circuit, shown in Fig. 14.17, utilizes four transistors in the transmission gates and another four for the two inverters needed to generate the complements $\overline{A}$ and $\overline{B}$, for a total of eight transistors. Note that 12 transistors are needed in the realization with standard CMOS.

Our final PTL example is the circuit shown in Fig. 14.18. It uses NMOS switches with low or zero threshold. Observe that both the input variables and their complements are employed and that the circuit generates both the Boolean function and its complement. Thus this form of circuit is known as **complementary pass-transistor logic (CPL)**. The circuit consists of two identical networks of pass transistors with the corresponding transistor gates controlled by the same signal (B and $\overline{B}$). The inputs to the PTL, however, are complemented: A and B for the first network, and $\overline{A}$ and $\overline{B}$ for the second. The circuit shown realizes both the AND and NAND functions.

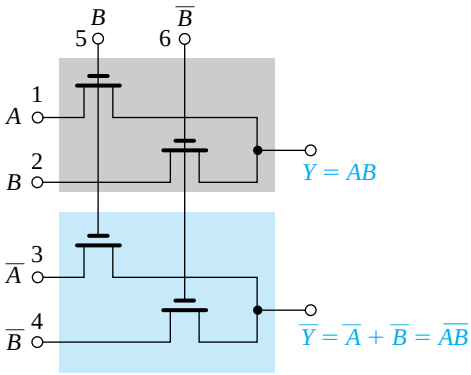

Figure 14.18 An example of a pass-transistor logic gate utilizing both the input variables and their complements. This type of circuit is therefore known as complementary pass-transistor logic, or CPL. Note that both the output function and its complement are generated.

EXERCISE

14.8 Consider the circuit in Fig. 14.8, and for each case, find Y and $\overline{Y}$. The input signals are changed as follows:

(a) The signals at terminals 5 and 6 are interchanged ($\overline{B}$ applied to 5 and B applied to 6). All the rest are the same.

(b) The signals at terminals 5 or 6 are interchanged as in (a), and the signals at 2 and 4 are changed to $\overline{A}$ and A, respectively. All the rest remain the same.

Ans. (a) $Y = A + B$, $\overline{Y} = \overline{A}\overline{B} = \overline{A + B}$ (i.e., OR–NOR); (b) $Y = A\overline{B} + \overline{A}B$, $\overline{Y} = \overline{A}\overline{B} + AB$ (i.e., XOR–XNOR)

14.2.6 A Final Remark

Although the use of zero-threshold devices solves the problem of the loss of signal levels when NMOS switches are used, the resulting circuits can be much more sensitive to noise and other effects, such as leakage currents resulting from subthreshold conduction.

14.3 Dynamic MOS Logic Circuits

The logic circuits that we have studied thus far are of the static type. In a static logic circuit, every node has, at all times, a low-resistance path to V_{DD} or ground. By the same token, the voltage of each node is well defined at all times, and no node is left floating. Static circuits do not need clocks (i.e., periodic timing signals) for their operation, although clocks may be present for other purposes. In contrast, the dynamic logic circuits we are about to discuss rely on the storage of signal voltages on parasitic capacitances at certain circuit nodes. Since charge will leak away with time, the circuits need to be *periodically refreshed;* thus the presence of a clock with a certain specified minimum frequency is essential.

To place dynamic logic circuit techniques into perspective, let's take stock of the various styles we have studied for logic circuits. Standard CMOS excels in nearly every performance category: It is easy to design, has the maximum possible logic swing, is robust from a noise-immunity standpoint, dissipates no static power, and can be designed to provide equal low-to-high and high-to-low propagation delays. Its main disadvantage is the requirement of two transistors for each additional gate input, which for high fan-in gates can make the chip

area large and increase the total capacitance and, correspondingly, the propagation delay and the dynamic power dissipation. Pseudo-NMOS reduces the number of required transistors at the expense of static power dissipation. Pass-transistor logic can result in simple small-area circuits but is limited to special applications and requires the use of CMOS inverters to restore signal levels, especially when the switches are simple NMOS transistors. The dynamic logic techniques studied in this section maintain the low device count of pseudo-NMOS while reducing the static power dissipation to zero. As will be seen, this is achieved at the expense of more complex, and less robust, design.

14.3.1 The Basic Principle

Figure 14.19(a) shows the basic dynamic logic gate. It consists of a pull-down network (PDN) that realizes the logic function in exactly the same way as the PDN of a standard CMOS gate or a pseudo-NMOS gate. Here, however, we have two switches in series that are periodically operated by the clock signal ϕ whose waveform is shown in Fig. 14.19(b). When ϕ is low, Q_p is turned on, and the circuit is said to be in the setup or **precharge phase**. When ϕ is high, Q_p is off and Q_e turns on, and the circuit is in the **evaluation phase**. Finally, note that C_L denotes the total capacitance between the output node and ground.

During precharge, Q_p conducts and charges capacitance C_L so that at the end of the precharge interval, the voltage at Y is equal to V_{DD}. Also during precharge, the inputs A, B, and C are allowed to change and settle to their proper values. Observe that because Q_e is off, no path to ground exists.

During the evaluation phase, Q_p is off and Q_e is turned on. Now, if the input combination is one that corresponds to a high output, the PDN does not conduct (just as in a standard

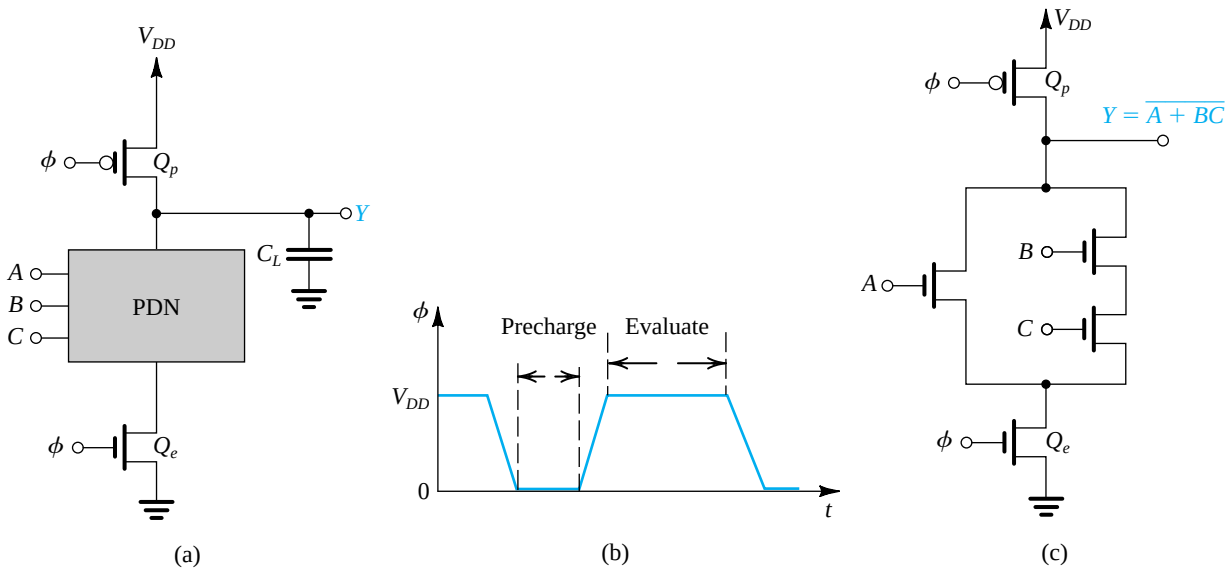

Figure 14.19 (**a**) Basic structure of dynamic-MOS logic circuits. (**b**) Waveform of the clock needed to operate the dynamic logic circuit. (**c**) An example circuit.

CMOS gate) and the output remains high at V_{DD}; thus $V_{OH} = V_{DD}$. Observe that no low-to-high propagation delay is required, thus $t_{PLH} = 0$. On the other hand, if the combination of inputs is one that corresponds to a low output, the appropriate NMOS transistors in the PDN will conduct and establish a path between the output node and ground through the "on" transistor Q_e. Thus C_L will be discharged through the PDN, and the voltage at the output node will reduce to $V_{OL} = 0$ V. The high-to-low propagation delay t_{PHL} can be calculated in exactly the same way as for a standard CMOS circuit, except that here we have an additional transistor, Q_e, in the series path to ground. Although this will increase the delay slightly, the increase will be more than offset by the reduced capacitance at the output node as a result of the absence of the PUN.

As an example, we show in Fig. 14.19(c) the circuit that realizes the function $Y = \overline{A + BC}$. Sizing of the PDN transistors often follows the same procedure employed in the design of static CMOS. For Q_p, we select a W/L ratio large enough to ensure that C_L will be fully charged during the precharge interval, but small enough so that the capacitance C_L will not be increased significantly. This is a ratioless form of MOS logic, where the output levels do not depend on the transistors' W/L ratios (unlike pseudo-NMOS, for instance).

Example 14.3

Consider the four-input, dynamic-logic NAND gate shown in Fig. 14.20(a). Assume that the gate is fabricated in a 0.18-μm CMOS technology for which $V_{DD} = 1.8$ V, $V_t = 0.5$ V, and $\mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu\text{A/V}^2$. To keep C_L small, NMOS devices with $W/L = 0.27\ \mu\text{m}/0.18\ \mu\text{m}$ are used (including transistor Q_e). The PMOS precharge transistor Q_p has $W/L = 0.54\ \mu\text{m}/0.18\ \mu\text{m}$. The total capacitance C_L is found to be 20 fF.

(a) Consider the precharge operation (Fig. 14.20b) with the gate of Q_p at 0 V, and assume that at $t = 0$, C_L is fully discharged. Calculate the rise time of the output voltage, defined as the time for v_Y to rise from 10% to 90% of the final voltage V_{DD}.

(b) For $A = B = C = D = 1$, find the value of t_{PHL}.

Solution

(a) From Fig. 14.20(a) we see that at $v_Y = 0.1V_{DD} = 0.18$ V, Q_p will be operating in the saturation region and i_D will be

$$i_D(0.1V_{DD}) = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)^2$$

$$= \frac{1}{2} \times 75 \times \frac{0.54}{0.18}(1.8 - 0.5)^2$$

$$= 190.1\ \mu\text{A}$$

At $v_Y = 0.9V_{DD} = 1.62$ V, Q_p will be operating in the triode region; thus,

$$i_D(0.9V_{DD}) = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \left[(V_{DD} - |V_{tp}|)(V_{DD} - 0.9V_{DD}) - \frac{1}{2}(V_{DD} - 0.9V_{DD})^2\right]$$

$$= 75 \times \frac{0.54}{0.18}\left[(1.8 - 0.5)(1.8 - 1.62) - \frac{1}{2}(1.8 - 1.62)^2\right]$$

$$= 49\ \mu\text{A}$$

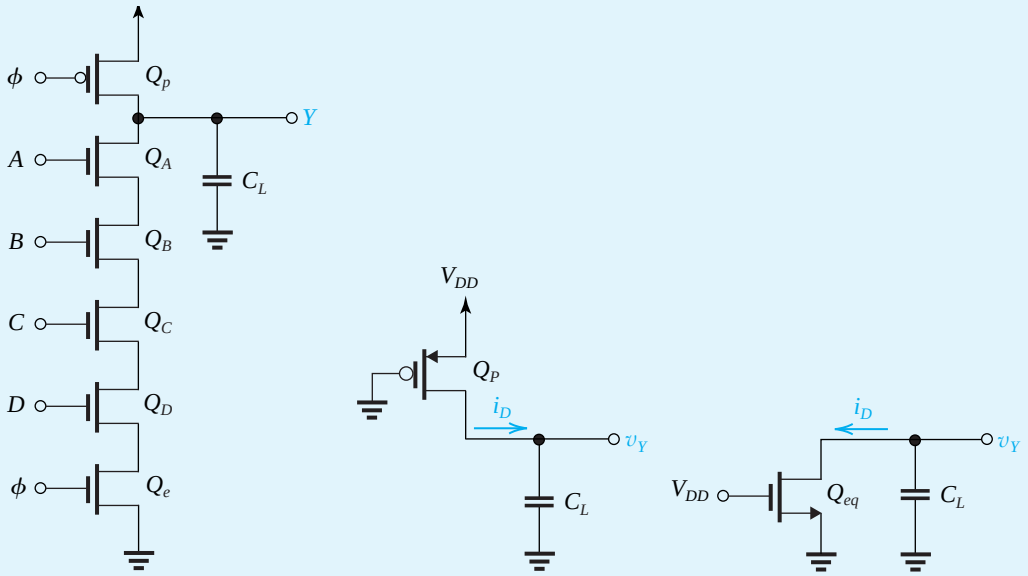

Figure 14.20 Circuits for Example 14.3.

Thus the average capacitor charging current is

$$I_{\text{av}} = \frac{1}{2}(190.1 + 49) = 119.6\ \mu\text{A}$$

The rise time t_r of v_Y can now be determined from

$$t_r = \frac{C\Delta v_Y}{I_{\text{av}}}$$

$$= \frac{C(0.9V_{DD} - 0.1V_{DD})}{I_{\text{av}}}$$

Thus,

$$t_r = \frac{20 \times 10^{-15} \times 0.8 \times 1.8}{119.6 \times 10^{-6}} = 0.19\ \text{ns}$$

(b) When $A = B = C = D = 1$, all the NMOS transistors will be conducting during the evaluation phase. Replacing the five identical transistors with an equivalent device Q_{eq} with $(W/L)_{\text{eq}} = \frac{1}{5}(W/L) = \frac{1}{5} \times 1.5 = 0.3$, we obtain the equivalent circuit for the capacitor discharge, shown in Fig. 14.20(c). At $v_Y = V_{DD}$, Q_{eq} will be operating in saturation; thus,

$$i_D(V_{DD}) = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)_{\text{eq}}(V_{DD} - V_t)^2$$

$$= \frac{1}{2} \times 300 \times 0.3(1.8 - 0.5)^2$$

$$= 76.1\ \mu\text{A}$$

Example 14.3 *continued*

At $v_Y = V_{DD}/2$, Q_{eq} will be operating in the triode region; thus,

$$i_D(V_{DD}/2) = (\mu_n C_{ox})\left(\frac{W}{L}\right)_{eq}\left[(V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

$$= 300 \times 0.3\left[(1.8 - 0.5)\left(\frac{1.8}{2}\right) - \frac{1}{2}\left(\frac{1.8}{2}\right)^2\right]$$

$$= 68.9\ \mu\text{A}$$

Thus the average capacitor-discharge current is

$$I_{av} = \frac{76.1 + 68.9}{2} = 72.5\ \mu\text{A}$$

and t_{PHL} can be found from

$$t_{PHL} = \frac{C(V_{DD} - V_{DD}/2)}{I_{av}}$$

$$= \frac{20 \times 10^{-15}(1.8 - 0.9)}{72.5 \times 10^{-6}} = 0.25\ \text{ns}$$

EXERCISE

14.9 In an attempt to reduce t_{PHL} of the NAND gate in Example 14.3, the designer doubles the value of W/L of each of the NMOS devices. If C increases to 30 fF, what is the new value if t_{PHL}?
Ans. 0.19 ns

14.3.2 Nonideal Effects

We now briefly consider various sources of nonideal operation of dynamic logic circuits.

Noise Margins Since, during the evaluation phase, the NMOS transistors begin to conduct for $v_I = V_{tn}$,

$$V_{IL} \simeq V_{IH} \simeq V_{tn}$$

and thus the noise margins will be

$$NM_L = V_{IL} - V_{OL} = V_{tn} - 0 = V_{tn}$$
$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{tn}$$

Thus the noise margins are far from equal, and NM_L is rather low. Although NM_H is high, other nonideal effects reduce its value, as we shall shortly see. At this time, however, observe that the output node is a high-impedance node and thus will be susceptible to noise pickup and other disturbances.

Output Voltage Decay Due to Leakage Effects In the absence of a path to ground through the PDN, the output voltage will ideally remain high at V_{DD}. This, however, is based

on the assumption that the charge on C_L will remain intact. In practice, there will be leakage current that will cause C_L to slowly discharge and v_Y to decay. The principal source of leakage is the reverse current of the reverse-biased junction between the drain diffusion of transistors connected to the output node and the substrate. Such currents can be in the range of 10^{-12} A to 10^{-15} A, and they increase rapidly with temperature (approximately doubling for every $10°C$ rise in temperature). Thus the circuit can malfunction if the clock is operating at a very low frequency and the output node is not "refreshed" periodically. This exact same point will be encountered when we study dynamic memory cells in Chapter 15.

Charge Sharing There is another and often more serious way for C_L to lose some of its charge and thus cause v_Y to fall significantly below V_{DD}. To see how this can happen, refer to Fig. 14.21(a), which shows only Q_1 and Q_2, the two top transistors of the PDN, together with the precharge transistor Q_p. Here, C_1 is the capacitance between the common node of Q_1 and Q_2 and ground. At the beginning of the evaluation phase, after Q_p has turned off and with C_L charged to V_{DD} (Fig. 14.21a), we assume that C_1 is initially discharged and that the inputs are such that at the gate of Q_1 we have a high signal, whereas at the gate of Q_2 the signal is low. We can easily see that Q_1 will turn on and its drain current, i_{D1}, will flow as indicated. Thus i_{D1} will discharge C_L and charge C_1. Although eventually i_{D1} will reduce to zero, C_L will have lost some of its charge, which will have been transferred to C_1. This phenomenon is known as charge sharing (see Problem 14.31).

We shall not pursue the problem of charge sharing any further here, except to point out a couple of the techniques usually employed to minimize its effect. One approach involves adding a *p*-channel device that continuously conducts a small current to replenish the charge lost by C_L, as shown in Fig. 14.21(b). This arrangement should remind us of pseudo-NMOS. Indeed, adding this transistor will cause the gate to dissipate static power. On the positive side, however, the added transistor will lower the impedance level of the output node and make it less susceptible to noise as well as solving the leakage and charge-sharing problems. Another approach to

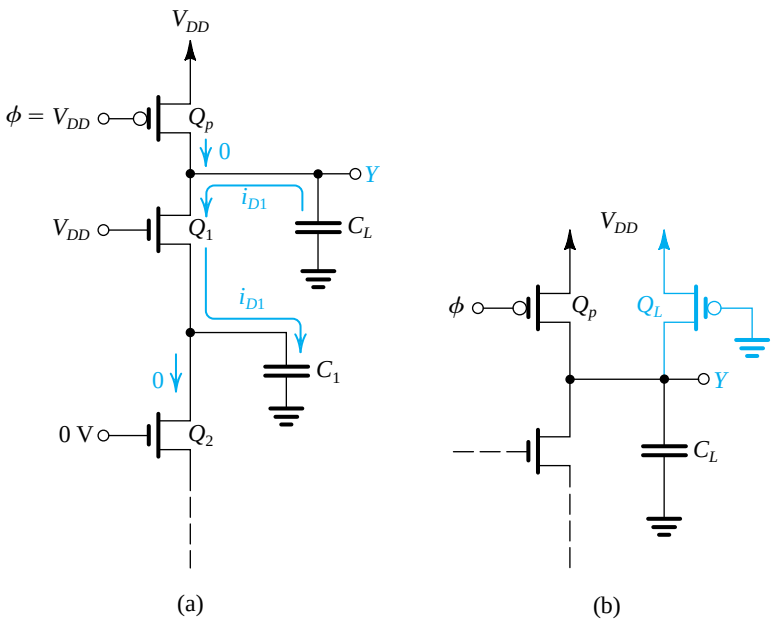

Figure 14.21 **(a)** Charge sharing. **(b)** Adding a permanently turned-on transistor Q_L solves the charge-sharing problem at the expense of static power dissipation.

solving the charge-sharing problem is to precharge the internal nodes: that is, to precharge capacitor C_1. The price paid in this case is increased circuit complexity and node capacitances.

Cascading Dynamic Logic Gates A serious problem arises if one attempts to cascade dynamic logic gates. Consider the situation depicted in Fig. 14.22, where two single-input dynamic gates are connected in cascade. During the precharge phase, C_{L1} and C_{L2} will be charged through Q_{p1} and Q_{p2}, respectively. Thus, at the end of the precharge interval, $v_{Y1} = V_{DD}$ and $v_{Y2} = V_{DD}$. Now consider what happens in the evaluation phase for the case of high input A. Obviously, the correct result will be Y_1 low ($v_{Y1} = 0$ V) and Y_2 high ($v_{Y2} = V_{DD}$). What happens, however, is somewhat different. As the evaluation phase begins, Q_1 turns on and C_{L1} begins to discharge. However, simultaneously, Q_2 turns on and C_{L2} also begins to discharge. Only when v_{Y1} drops below V_{tn} will Q_2 turn off. Unfortunately, however, by that time, C_{L2} will have lost a significant amount of its charge, and v_{Y2} will be less than the expected value of V_{DD}. (Here it is important to note that in dynamic logic, once charge has been lost, it cannot be recovered.) This problem is sufficiently serious to make simple cascading an impractical proposition. As usual, however, the ingenuity of circuit designers has come to the rescue, and a number of schemes have been proposed to make cascading possible in dynamic-logic circuits. We shall discuss one such scheme after considering Exercise 14.10.

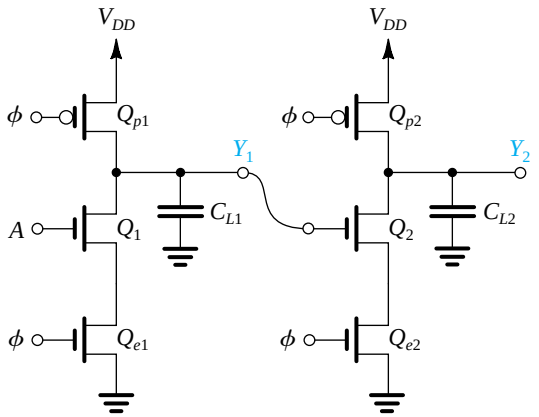

Figure 14.22 Two single-input dynamic logic gates connected in cascade. With the input A high, during the evaluation phase C_{L2} will partially discharge and the output at Y_2 will fall lower than V_{DD}, which can cause logic malfunction.

EXERCISE

14.10 To gain further insight into the cascading problem described above, let us determine the decrease in the output voltage v_{Y2} for the circuit in Fig. 14.22. Specifically, consider the circuit as the evaluation phase begins: At $t = 0$, $v_{Y1} = v_{Y2} = V_{DD}$ and $v_\phi = v_A = V_{DD}$. Transistors Q_{p1} and Q_{p2} are cut off and can be removed from the equivalent circuit. Furthermore, for the purpose of this approximate analysis, we can replace the series combination of Q_1 and Q_{e1} with a single device having an appropriate W/L, and similarly for the combination of Q_2 and Q_{e2}. The result is the approximate equivalent circuit in Fig. E14.10. We are interested in the operation of this circuit in the interval Δt

during which v_{Y1} falls from V_{DD} to V_t, at which time Q_{eq2} turns off and C_{L2} stops discharging. Assume that the process technology has the parameter values specified in Example 14.2; that for all NMOS transistors in the circuit of Fig. 14.22, $W/L = 4\ \mu m/2\ \mu m$ and $C_{L1} = C_{L2} = 40$ fF.

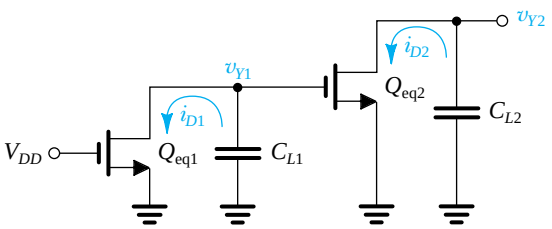

Figure E 14.10

(a) Find $(W/L)_{eq1}$ and $(W/L)_{eq2}$.

(b) Find the values of i_{D1} at $v_{Y1} = V_{DD}$ and at $v_{Y1} = V_t$. Hence determine an average value for i_{D1}.

(c) Use the average value of i_{D1} found in (b) to determine an estimate for the interval Δt.

(d) Find the average value of i_{D2} during Δt. To simplify matters, take the average to be the value of i_{D2} obtained when the gate voltage v_{Y1} is midway through its excursion (i.e., $v_{Y1} = 3$ V). (*Hint:* Q_{eq2} will remain in saturation.)

(e) Use the value of Δt found in (c) together with the average value of i_{D2} determined in (d) to find an estimate of the reduction in v_{Y2} during Δt. Hence determine the final value of v_{Y2}.

Ans. (a) 1, 1; (b) 400 µA and 175 µA, for an average value of 288 µA; (c) 0.56 ns; (d) 100 µA; (e) $\Delta v_{Y2} = 1.4$ V, thus v_{Y2} decreases to 3.6 V

14.3.3 Domino CMOS Logic

Domino CMOS logic is a form of dynamic logic that results in cascadable gates. Figure 14.23 shows the structure of the Domino CMOS logic gate. We observe that it is simply the basic dynamic logic gate of Fig. 14.19(a) with a static CMOS inverter connected to its output. Operation of the gate is straightforward. During precharge, X will be raised to V_{DD}, and the gate output Y will be at 0 V. During evaluation, depending on the combination of input variables, either X will remain high and thus the output Y will remain low ($t_{PHL} = 0$) or X will be brought down to 0 V and the output Y will rise to V_{DD} (t_{PLH} finite). Thus, during evaluation, the output either remains low or makes only one low-to-high transition.

To see why Domino CMOS gates can be cascaded, consider the situation in Fig. 14.24(a), where we show two Domino gates connected in cascade. For simplicity, we show single-input gates. At the end of precharge, X_1 will be at V_{DD}, Y_1 will be at 0 V, X_2 will be at V_{DD}, and Y_2 will be at 0 V. As in the preceding case, assume that A is high at the beginning of evaluation. Thus, as ϕ goes up, capacitor C_{L1} will begin discharging, pulling X_1 down. Meanwhile, the low input at the gate of Q_2 keeps Q_2 off, and C_{L2} remains fully charged. When v_{X1} falls below the threshold voltage of inverter I_1, Y_1 will go up, turning Q_2 on, which in turn begins to discharge C_{L2} and pulls X_2 low. Eventually, Y_2 rises to V_{DD}.

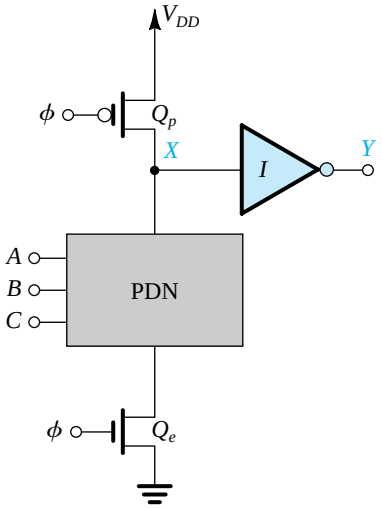

Figure 14.23 The Domino CMOS logic gate. The circuit consists of a dynamic-MOS logic gate with a static-CMOS inverter connected to the output. During evaluation, Y either will remain low (at 0 V) or will make one 0-to-1 transition (to V_{DD}).

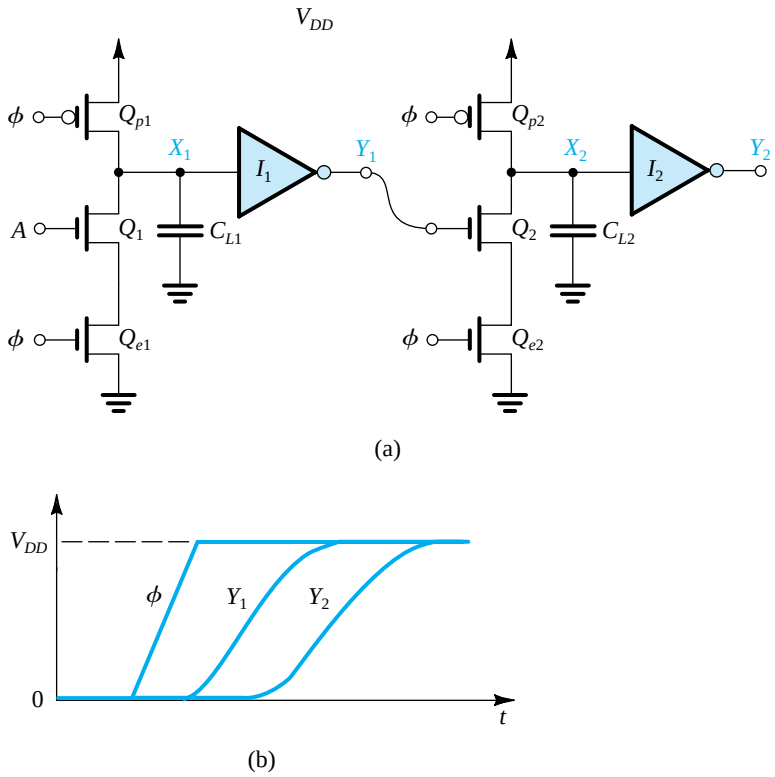

Figure 14.24 **(a)** Two single-input Domino CMOS logic gates connected in cascade. **(b)** Waveforms during the evaluation phase.

From this description, we see that because the output of the Domino gate is low at the beginning of evaluation, no premature capacitor discharge will occur in the subsequent gate in the cascade. As indicated in Fig. 14.24(b), output Y_1 will make a 0-to-1 transition t_{PLH}

seconds after the rising edge of the clock. Subsequently, output Y_2 makes a 0-to-1 transition after another t_{PLH} interval. The propagation of the rising edge through a cascade of gates resembles contiguously placed dominoes falling over, each toppling the next, which is the origin of the name Domino CMOS logic. Domino CMOS logic finds application in the design of address decoders in memory chips, for example.

14.3.4 Concluding Remarks

Dynamic logic presents many challenges to the circuit designer. Although it can provide considerable reduction in the chip-area requirement, as well as high-speed operation, and zero (or little) static-power dissipation, the circuits are prone to many nonideal effects, some of which have been discussed here. It should also be remembered that dynamic power dissipation is an important issue in dynamic logic. Another factor that should be considered is the "dead time" during precharge when the output of the circuit is not yet available.

14.4 Emitter-Coupled Logic (ECL)

Emitter-coupled logic (ECL) is the fastest logic circuit family available for conventional logic-system design.[4] High speed is achieved by operating all bipolar transistors out of saturation, thus avoiding storage-time delays, and by keeping the logic signal swings relatively small (about 0.8 V or less), thus reducing the time required to charge and discharge the various load and parasitic capacitances. Saturation in ECL is avoided by using the BJT differential pair as a current switch.[5] The BJT differential pair was studied in Chapter 8, and we urge the reader to review the introduction given in Section 8.3 before proceeding with the study of ECL.

14.4.1 The Basic Principle

Emitter-coupled logic is based on the use of the current-steering switch introduced in Section 13.1 (Fig 13.9). Such a switch can be most conveniently realized using the differential pair shown in Fig. 14.25. The pair is biased with a constant-current source I, and one side is connected to a reference voltage V_R. As shown in Section 8.3, the current I can be steered to either Q_1 or Q_2 under the control of the input signal v_I. Specifically, when v_I is greater than V_R by about $4V_T$ ($\simeq$100 mV), nearly all the current I is conducted by Q_1, and thus for $\alpha_1 \simeq 1$, $v_{O1} = V_{CC} - IR_C$. Simultaneously, the current through Q_2 will be nearly zero, and thus $v_{O2} = V_{CC}$. Conversely, when v_I is lower than V_R by about $4V_T$, most of the current I will flow through Q_2 and the current through Q_1 will be nearly zero. Thus $v_{O1} = V_{CC}$ and $v_{O2} = V_{CC} - IR_C$.

The preceding description suggests that as a logic element, the differential pair realizes an inversion function at v_{O1} and simultaneously provides the complementary output signal at v_{O2}. The output logic levels are $V_{OH} = V_{CC}$ and $V_{OL} = V_{CC} - IR_C$, and thus the output logic swing is IR_C. A number of additional remarks can be made concerning this circuit:

[4]Although higher speeds of operation can be obtained with gallium arsenide (GaAs) circuits, the latter are not available as off-the-shelf components for conventional digital system design. GaAs digital circuits are not covered in this book; however, a substantial amount of material on this subject can be found on the CD accompanying the book and on the website.

[5]This is in sharp contrast to the technique utilized in a nonsaturating variant of transistor-transistor logic (TTL) known as Schottky TTL. There, a Schottky diode is placed across the CBJ junction to shunt away some of the base current and, owing to the low voltage drop of the Schottky diode, the CBJ is prevented from becoming forward biased.

1. The differential nature of the circuit makes it less susceptible to picked-up noise. In particular, an interfering signal will tend to affect both sides of the differential pair similarly and thus will not result in current switching. This is the common-mode rejection property of the differential pair (see Section 8.3).
2. The current drawn from the power supply remains constant during switching. Thus, unlike CMOS (and TTL), no supply current spikes occur in ECL, eliminating an important source of noise in digital circuits. This is a definite advantage, especially since ECL is usually designed to operate with small signal swings and has correspondingly low noise margins.
3. The output signal levels are both referenced to V_{CC} and thus can be made particularly stable by operating the circuit with $V_{CC} = 0$: in other words, by utilizing a negative power supply and connecting the V_{CC} line to ground. In this case, $V_{OH} = 0$ and $V_{OL} = -IR_C$.
4. Some means must be provided to make the output signal levels compatible with those at the input so that one gate can drive another. As we shall see shortly, practical ECL gate circuits incorporate a level-shifting arrangement that serves to center the output signal levels on the value of V_R.
5. The availability of complementary outputs considerably simplifies logic design with ECL.

EXERCISE

14.11 For the circuit in Fig. 14.25, let $V_{CC} = 0$, $I = 4$ mA, $R_C = 220\ \Omega$, $V_R = -1.32$ V, and assume $\alpha \simeq 1$. Determine V_{OH} and V_{OL}. By how much should the output levels be shifted so that the values of V_{OH} and V_{OL} become centered on V_R? What will the shifted values of V_{OH} and V_{OL} be?
Ans. 0; –0.88 V; –0.88 V; –0.88 V, –1.76 V

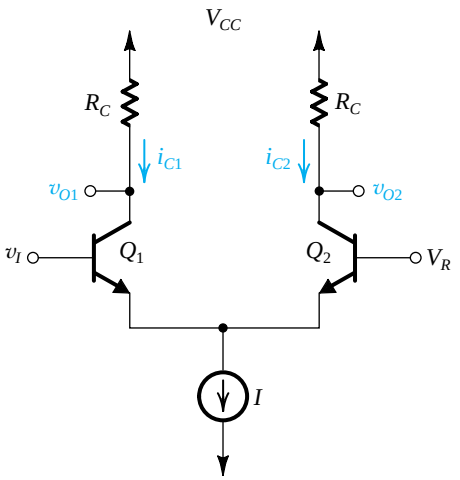

Figure 14.25 The basic element of ECL is the differential pair. Here, V_R is a reference voltage.

14.4.2 ECL Families

Currently there are two popular forms of commercially available ECL—namely, ECL 10 K and ECL 100K. The ECL 100K series features gate delays on the order of 0.75 ns and

dissipates about 40 mW/gate, for a delay–power product of 30 pJ. Although its power dissipation is relatively high, the 100K series provides the shortest available gate delay in small- and medium-scale integrated circuit packages.

The ECL 10 K series is slightly slower; it features a gate propagation delay of 2 ns and a power dissipation of 25 mW for a delay–power product of 50 pJ. Although the value of *PDP* is higher than that obtained in the 100K series, the 10K series is easier to use. This is because the rise and fall times of the pulse signals are deliberately made longer, thus reducing signal coupling, or cross talk, between adjacent signal lines. ECL 10K has an "edge speed" of about 3.5 ns, compared with the approximately 1 ns of ECL 100K. To give concreteness to our study of ECL, in the following we shall consider the popular ECL 10K in some detail. The same techniques, however, can be applied to other types of ECL.

In addition to its usage in SSI and MSI circuit packages, ECL is also employed in large-scale and VLSI applications. A variant of ECL known as **current-mode logic** (CML) is utilized in VLSI applications (see Treadway, 1989, and Wilson, 1990).

14.4.3 The Basic Gate Circuit

The basic gate circuit of the ECL 10K family is shown in Fig. 14.26. The circuit consists of three parts. The network composed of Q_1, D_1, D_2, R_1, R_2, and R_3 generates a reference voltage V_R whose value at room temperature is –1.32 V. As will be shown, the value of this reference voltage is made to change with temperature in a predetermined manner to keep the noise margins almost constant. Also, the reference voltage V_R is made relatively insensitive to variations in the power-supply voltage V_{EE}.

EXERCISE

14.12 Figure E14.12 shows the circuit that generates the reference voltage V_R. Assuming that the voltage drop across each of D_1, D_2, and the base–emitter junction of Q_1 is 0.75 V, calculate the value of V_R. Neglect the base current of Q_1.

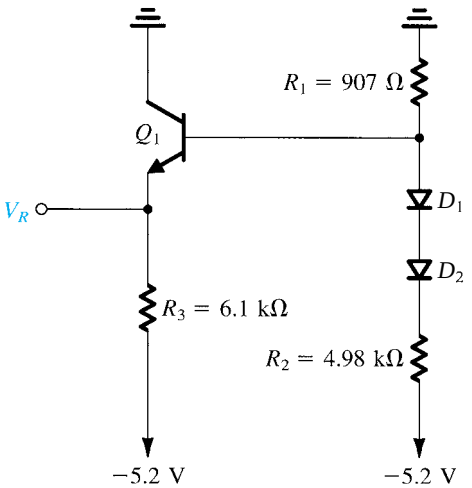

Figure E14.12

Ans. –1.32 V

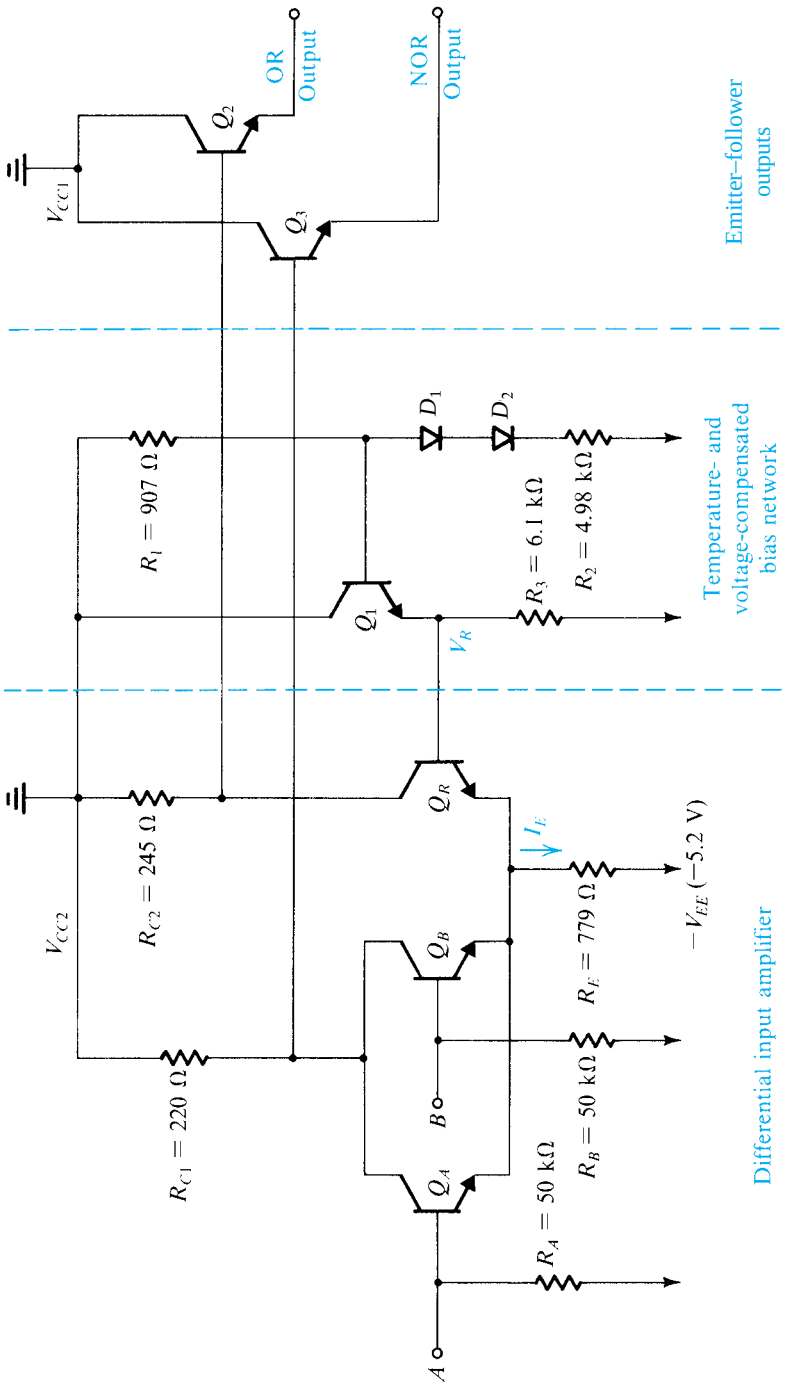

Figure 14.26 Basic circuit of the ECL 10K logic-gate family.

The second part, and the heart of the gate, is the differential amplifier formed by Q_R and either Q_A or Q_B. This differential amplifier is biased not by a constant-current source, as was done in the circuit of Fig. 14.25, but with a resistance R_E connected to the negative supply $-V_{EE}$. Nevertheless, we will shortly show that the current in R_E remains approximately constant over the normal range of operation of the gate. One side of the differential amplifier consists of the reference transistor Q_R, whose base is connected to the reference voltage V_R. The other side consists of a number of transistors (two in the case shown), connected in parallel, with separated bases, each connected to a gate input. If the voltages applied to A and B are at the logic-0 level, which, as we will soon find out, is about 0.4 V below V_R, both Q_A and Q_B, will be off and the current I_E in R_E will flow through the reference transistor Q_R. The resulting voltage drop across R_{C2} will cause the collector voltage of Q_R to be low.

On the other hand, when the voltage applied to A or B is at the logic-1 level, which, as we will show shortly, is about 0.4 V above V_R, transistor Q_A or Q_B, or both, will be on and Q_R will be off. Thus the current I_E will flow through Q_A or Q_B, or both, and an almost equal current will flow through R_{C1}. The resulting voltage drop across R_{C1} will cause the collector voltage to drop. Meanwhile, since Q_R is off, its collector voltage rises. We thus see that the voltage at the collector of Q_R will be high if A or B, or both, is high, and thus at the collector of Q_R, the OR logic function, $A + B$, is realized. On the other hand, the common collector of Q_A and Q_B will be high only when A and B are simultaneously low. Thus at the common collector of Q_A and Q_B, the logic function $\overline{A}\,\overline{B} = \overline{A + B}$ is realized. We therefore conclude that the two-input gate of Fig. 14.26 realizes the OR function and its complement, the NOR function. The availability of complementary outputs is an important advantage of ECL; it simplifies logic design and avoids the use of additional inverters with associated time delay.

It should be noted that the resistance connecting each of the gate input terminals to the negative supply enables the user to leave an unused input terminal open: An open input terminal will be *pulled down* to the negative supply voltage, and its associated transistor will be off.

EXERCISE

14.13 With input terminals A and B in Fig. 14.26 left open, find the current I_E through R_E. Also find the voltages at the collector of Q_R and at the common collector of the input transistors Q_A and Q_B. Use $V_R = -1.32$ V, V_{BE} of $Q_R \simeq 0.75$ V, and assume that β of Q_R is very high.
Ans. 4 mA; –1 V; 0 V

The third part of the ECL gate circuit is composed of the two emitter followers, Q_2 and Q_3. The emitter followers do not have on-chip loads, since in many applications of high-speed logic circuits the gate output drives a transmission line terminated at the other end, as indicated in Fig. 14.27. (More on this later in Section 14.4.6.)

The emitter followers have two purposes: First, they shift the level of the output signals by one V_{BE} drop. Thus, using the results of Exercise 14.13, we see that the output levels become approximately –1.75 V and –0.75 V. These shifted levels are centered approximately around the reference voltage ($V_R = -1.32$ V), which means that one gate can drive another. This compatibility of logic levels at input and output is an essential requirement in the design of gate circuits.

The second function of the output emitter followers is to provide the gate with low output resistances and with the large output currents required for charging load capacitances.

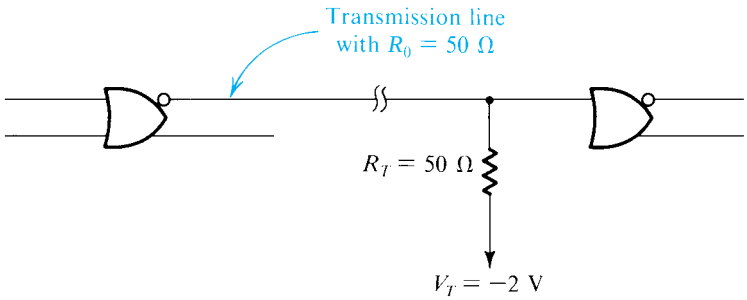

Figure 14.27 The proper way to connect high-speed logic gates such as ECL. Properly terminating the transmission line connecting the two gates eliminates the "ringing" that would otherwise corrupt the logic signals. (See Section 14.4.6.)

Since these large transient currents can cause spikes on the power-supply line, the collectors of the emitter followers are connected to a power-supply terminal V_{CC1} separate from that of the differential amplifier and the reference-voltage circuit, V_{CC2}. Here we note that the supply current of the differential amplifier and the reference circuit remains almost constant. The use of separate power-supply terminals prevents the coupling of power-supply spikes from the output circuit to the gate circuit and thus lessens the likelihood of false gate switching. Both V_{CC1} and V_{CC2} are of course connected to the same system ground, external to the chip.

14.4.4 Voltage-Transfer Characteristics

Having provided a qualitative description of the operation of the ECL gate, we shall now derive its voltage-transfer characteristics. This will be done under the conditions that the outputs are terminated in the manner indicated in Fig. 14.27. Assuming that the B input is low and thus Q_B is off, the circuit simplifies to that shown in Fig. 14.28. We wish to analyze this circuit to determine v_{OR} versus v_I and v_{NOR} versus v_I (where $v_I \equiv v_A$).

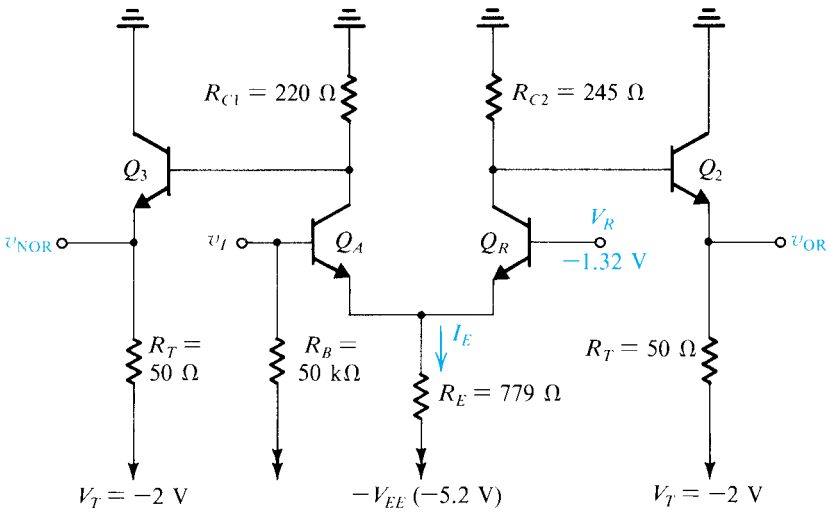

Figure 14.28 Simplified version of the ECL gate for the purpose of finding transfer characteristics.

In the analysis to follow we shall make use of the exponential i_C–v_{BE} characteristic of the BJT. Since the BJTs used in ECL circuits have small areas (in order to have small capacitances and hence high f_T), their scale currents I_S are small. We will therefore assume that at an emitter current of 1 mA, an ECL transistor has a V_{BE} drop of 0.75 V.

The OR Transfer Curve Figure 14.29 is a sketch of the OR transfer characteristic, v_{OR} versus v_I, with the parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH} indicated. However, to simplify the calculation of V_{IL} and V_{IH}, we shall use an alternative to the unity-gain definition. Specifically, we shall assume that at point x, transistor Q_A is conducting 1% of I_E while Q_R is conducting 99% of I_E. The reverse will be assumed for point y. Thus at point x we have

$$\frac{I_E|_{Q_R}}{I_E|_{Q_A}} = 99$$

Using the exponential i_E–v_{BE} relationship, we obtain

$$V_{BE}|_{Q_R} - V_{BE}|_{Q_A} = V_T \ln 99 = 115 \text{ mV}$$

which gives

$$V_{IL} = -1.32 - 0.115 = -1.435 \text{ V}$$

Assuming Q_A and Q_R to be matched, we can write

$$V_{IH} - V_R = V_R - V_{IL}$$

which can be used to find V_{IH} as

$$V_{IH} = -1.205 \text{ V}$$

To obtain V_{OL}, we note that Q_A is off and Q_R carries the entire current I_E, given by

$$I_E = \frac{V_R - V_{BE}|_{Q_R} + V_{EE}}{R_E}$$

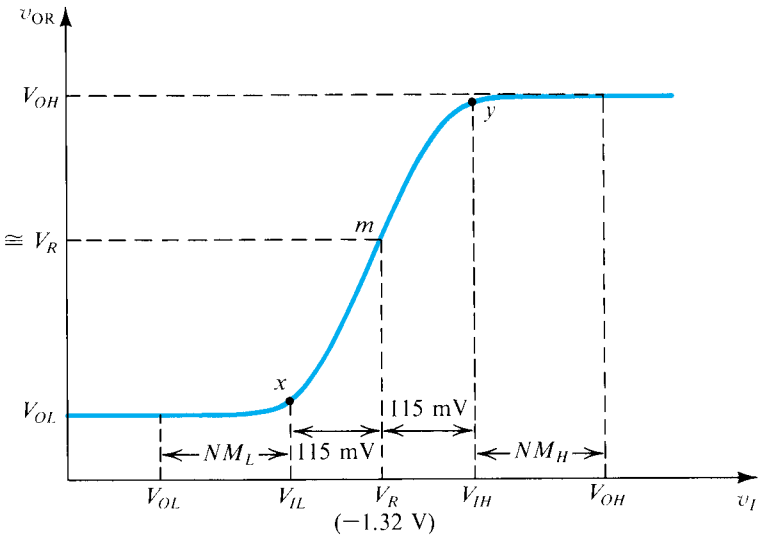

Figure 14.29 The OR transfer characteristic v_{OR} versus v_I, for the circuit in Fig. 14.28.

$$= \frac{-1.32 - 0.75 + 5.2}{0.779}$$
$$\simeq 4 \text{ mA}$$

(If we wish, we can iterate to determine a better estimate of $V_{BE}|_{Q_R}$ and hence of I_E.) Assuming that Q_R has a high β so that its $\alpha \simeq 1$, its collector current will be approximately 4 mA. If we neglect the base current of Q_2, we obtain for the collector voltage of Q_R

$$V_C|_{Q_R} \simeq -4 \times 0.245 = -0.98 \text{ V}$$

Thus a first approximation for the value of the output voltage V_{OL} is

$$V_{OL} = V_C|_{Q_R} - V_{BE}|_{Q_2}$$
$$\simeq -0.98 - 0.75 = -1.73 \text{ V}$$

We can use this value to find the emitter current of Q_2 and then iterate to determine a better estimate of its base–emitter voltage. The result is $V_{BE2} \simeq 0.79$ V and, correspondingly,

$$V_{OL} \simeq -1.77 \text{ V}$$

At this value of output voltage, Q_2 supplies a load current of about 4.6 mA.

To find the value of V_{OH} we assume that Q_R is completely cut off (because $v_I > V_{IH}$). Thus the circuit for determining V_{OH} simplifies to that in Fig. 14.30. Analysis of this circuit, assuming $\beta_2 = 100$, results in $V_{BE2} \simeq 0.83$ V, $I_{E2} = 22.4$ mA, and

$$V_{OH} \simeq -0.88 \text{ V}$$

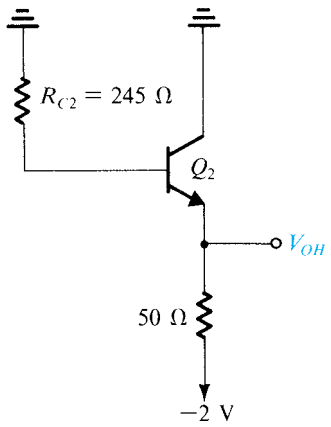

Figure 14.30 Circuit for determining V_{OH}.

EXERCISE

14.14 For the circuit in Fig. 14.28, determine the values of I_E obtained when $v_I = V_{IL}$, V_R, and V_{IH}. Also, find the value of v_{OR} corresponding to $v_I = V_R$. Assume that $v_{BE} = 0.75$ V at a current of 1 mA.
Ans. 3.97 mA; 4.00 mA; 4.12 mA; −1.31 V

Noise Margins The results of Exercise 14.14 indicate that the bias current I_E remains approximately constant. Also, the output voltage corresponding to $v_I = V_R$ is approximately equal to V_R. Notice further that this is also approximately the midpoint of the logic swing; specifically,

$$\frac{V_{OL} + V_{OH}}{2} = -1.325 \simeq V_R$$

Thus the output logic levels are centered around the midpoint of the input transition band. This is an ideal situation from the point of view of noise margins, and it is one of the reasons for selecting the rather arbitrary-looking numbers ($V_R = -1.32$ V and $V_{EE} = 5.2$ V) for reference and supply voltages.

The noise margins can now be evaluated as follows:

$$NM_H = V_{OH} - V_{IH}$$
$$= -0.88 - (-1.205) = 0.325 \text{ V}$$

$$NM_L = V_{IL} - V_{OL}$$
$$= -1.435 - (-1.77) = 0.335 \text{ V}$$

Note that these values are approximately equal.

The NOR Transfer Curve The NOR transfer characteristic, which is v_{NOR} versus v_I for the circuit in Fig. 14.28, is sketched in Fig. 14.31. The values of V_{IL} and V_{IH} are identical to those found earlier for the OR characteristic. To emphasize this, we have labeled the threshold points *x* and *y*, the same letters used in Fig. 14.29.

For $v_I < V_{IL}$, Q_A is off and the output voltage v_{NOR} can be found by analyzing the circuit composed of R_{C1}, Q_3, and its 50-Ω termination. Except that R_{C1} is slightly smaller than R_{C2}, this circuit is identical to that in Fig. 14.30. Thus the output voltage will be only slightly greater than the value V_{OH} found earlier. In the sketch of Fig. 14.31 we have assumed that the output voltage is approximately equal to V_{OH}.

For $v_I > V_{IH}$, Q_A is on and is conducting the entire bias current. The circuit then simplifies to that in Fig. 14.32. This circuit can be easily analyzed to obtain v_{NOR} versus v_I for the

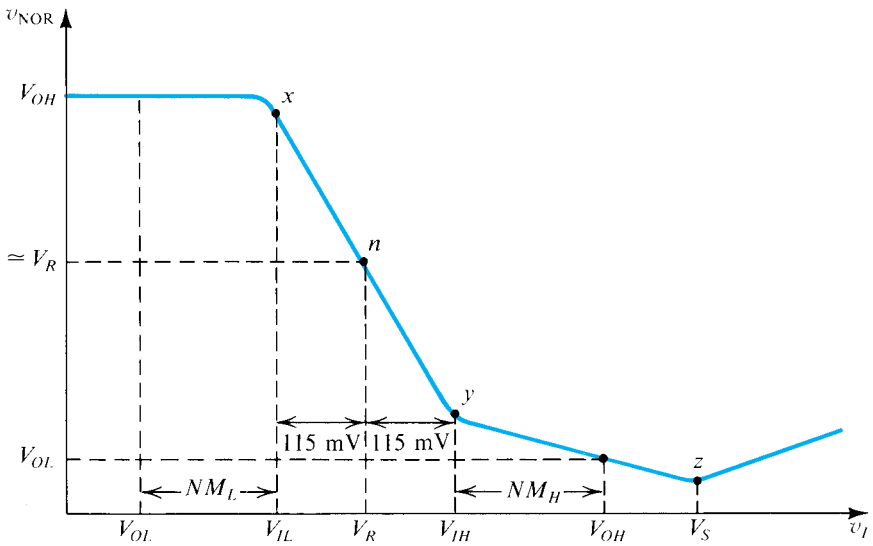

Figure 14.31 The NOR transfer characteristic, v_{NOR} versus v_I, for the circuit in Fig. 14.28.

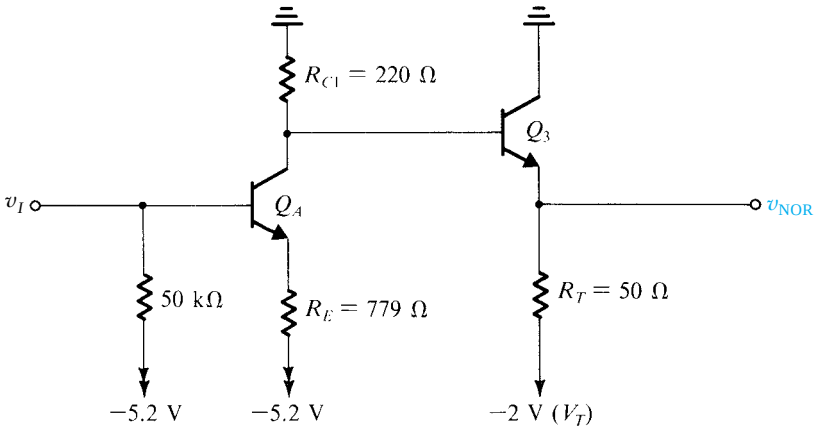

Figure 14.32 Circuit for finding v_{NOR} versus v_I for the range $v_I > V_{IH}$.

range $v_I \geq V_{IH}$. A number of observations are in order. First, note that $v_I = V_{IH}$ results in an output voltage slightly higher than V_{OL}. This is because R_{C1} is smaller than R_{C2}. In fact, R_{C1} is chosen lower in value than R_{C2} so that with v_I equal to the normal logic-1 value (i.e., V_{OH}, which is approximately –0.88 V), the output will be equal to the V_{OL} value found earlier for the OR output.

Second, note that as v_I exceeds V_{IH}, transistor Q_A operates in the active mode and the circuit of Fig. 14.32 can be analyzed to find the gain of this amplifier, which is the slope of the segment *yz* of the transfer characteristic. At point *z*, transistor Q_A saturates. Further increments in v_I (beyond the point $v_I = V_S$) cause the collector voltage and hence v_{NOR} to increase. The slope of the segment of the transfer characteristic beyond point *z*, however, is not unity, but is about 0.5, because as Q_A is driven deeper into saturation, a portion of the increment in v_I appears as an increment in the base–collector forward-bias voltage. The reader is urged to solve Exercise 14.15, which is concerned with the details of the NOR transfer characteristic.

EXERCISE

14.15 Consider the circuit in Fig. 14.32. (a) For $v_I = V_{IH} = -1.205$ V, find v_{NOR}. (b) For $v_I = V_{OH} = -0.88$ V, find v_{NOR}. (c) Find the slope of the transfer characteristic at the point $v_I = V_{OH} = -0.88$ V. (d) Find the value of v_I at which Q_A saturates (i.e., V_S). Assume that $V_{BE} = 0.75$ V at a current of 1 mA, $V_{CEsat} \simeq 0.3$ V, and $\beta = 100$.
Ans. (a) –1.70 V; (b) –1.79 V; (c) –0.24 V/V; (d) –0.58 V

Manufacturers' Specifications ECL manufacturers supply gate transfer characteristics of the form shown in Figs. 14.29 and 14.31. A manufacturer usually provides such curves measured at a number of temperatures. In addition, at each relevant temperature, worst-case values for the parameters V_{IL}, V_{IH}, V_{OL}, and V_{OH} are given. These worst-case values are specified with the inevitable component tolerances taken into account. As an example, Motorola specifies that for MECL 10,000 at 25°C, the following worst-case

values apply[6]

$$V_{IL\max} = -1.475 \text{ V} \qquad V_{IH\min} = -1.105 \text{ V}$$
$$V_{OL\max} = -1.630 \text{ V} \qquad V_{OH\min} = -0.980 \text{ V}$$

These values can be used to determine worst-case noise margins,

$$NM_L = 0.155 \text{ V} \qquad NM_H = 0.125 \text{ V}$$

which are about half the *typical* values previously calculated.

For additional information on MECL specifications the interested reader is referred to the Motorola (1988, 1989) publications listed in the bibliography in Appendix G.

14.4.5 Fan-Out

When the input signal to an ECL gate is low (V_{OL}), the input current is equal to the current that flows in the 50-kΩ pull-down resistor. Thus,

$$I_{IL} = \frac{-1.77 + 5.2}{50} \simeq 69 \text{ μA}$$

When the input is high (V_{OH}), the input current is greater because of the base current of the input transistor. Thus, assuming a transistor β of 100, we obtain

$$I_{IH} = \frac{-0.88 + 5.2}{50} + \frac{4}{101} \simeq 126 \text{ μA}$$

Both these current values are quite small, which, coupled with the very small output resistance of the ECL gate, ensures that little degradation of logic-signal levels results from the input currents of fan-out gates. It follows that the fan-out of ECL gates is not limited by logic-level considerations but rather by the degradation of the circuit speed (rise and fall times). This latter effect is due to the capacitance that each fan-out gate presents to the driving gate (approximately 3 pF). Thus while the *dc fan-out* can be as high as 90 and thus does not represent a design problem, the *ac fan-out* is limited by considerations of circuit speed to 10 or so.

14.4.6 Speed of Operation and Signal Transmission

The speed of operation of a logic family is measured by the delay of its basic gate and by the rise and fall times of the output waveforms. Typical values of these parameters for ECL have already been given. Here we should note that because the output circuit is an emitter follower, the rise time of the output signal is shorter than its fall time, since on the rising edge of the output pulse, the emitter follower functions and provides the output current required to charge up the load and parasitic capacitances. On the other hand, as the signal at the base of the emitter follower falls, the emitter follower cuts off, and the load capacitance discharges through the combination of load and pull-down resistances.

To take full advantage of the very high speed of operation possible with ECL, special attention should be paid to the method of interconnecting the various logic gates in a system. To appreciate this point, we shall briefly discuss the problem of signal transmission.

ECL deals with signals whose rise times may be 1 ns or even less, the time it takes for light to travel only 30 cm or so. For such signals, a wire and its environment become a relatively complex circuit element along which signals propagate with finite speed (perhaps half the speed of light—i.e., 15 cm/ns). Unless special care is taken, energy that reaches the end

[6]MECL is the trade name used by Motorola (now Freescale Semiconductors) for its ECL.

of such a wire is not absorbed but rather returns as a *reflection* to the transmitting end, where (without special care) it may be re-reflected. The result of this process of reflection is what can be observed as **ringing**, a damped oscillatory excursion of the signal about its final value.

Unfortunately, ECL is particularly sensitive to ringing because the signal levels are so small. Thus it is important that transmission of signals be well controlled, and surplus energy absorbed, to prevent reflections. The accepted technique is to limit the nature of connecting wires in some way. One way is to insist that they be very short, where "short" is taken to mean with respect to the signal rise time. The reason for this is that if the wire connection is so short that reflections return while the input is still rising, the result becomes only a somewhat slowed and "bumpy" rising edge.

If, however, the reflection returns *after* the rising edge, it produces not simply a modification of the initiating edge but an *independent second event.* This is clearly bad! Thus the time taken for a signal to go from one end of a line and back is restricted to less than the rise time of the driving signal by some factor—say, 5. Thus for a signal with a 1-ns rise time and for propagation at the speed of light (30 cm/ns), a double path of only 0.2-ns equivalent length, or 6 cm, would be allowed, representing in the limit a wire only 3 cm from end to end.

Such is the restriction on ECL 100K. However, ECL 10K has an intentionally slower rise time of about 3.5 ns. Using the same rules, wires can accordingly be as long as about 10 cm for ECL 10K.

If greater lengths are needed, then transmission lines must be used. These are simply wires in a controlled environment in which the distance to a ground reference plane or a second wire is highly controlled. Thus they might simply be twisted pairs of wires, one of which is grounded, or parallel ribbon wires, every second of which is grounded, or so-called microstrip lines on a printed-circuit board. The latter are simply copper strips of controlled geometry on one side of a thin printed-circuit board, the other side of which consists of a grounded plane.

Such transmission lines have a *characteristic impedance*, R_0, that ranges from a few tens of ohms to hundreds of ohms. Signals propagate on such lines somewhat more slowly than the speed of light, perhaps half as fast. When a transmission line is terminated at its receiving end in a resistance equal to its characteristic impedance, R_0, all the energy sent on the line is absorbed at the receiving end, and no reflections occur (since the termination acts as a limitless length of transmission line). Thus, signal integrity is maintained. Such transmission lines are said to be *properly terminated.* A properly terminated line appears at its sending end as a resistor of value R_0. The followers of ECL 10K with their open emitters and low output resistances (specified to be 7 Ω maximum) are ideally suited for driving transmission lines. ECL is also good as a line receiver. The simple gate with its high (50-kΩ) pull-down input resistor represents a very high resistance to the line. Thus a few such gates can be connected to a terminated line with little difficulty. Both these ideas are represented in Fig. 14.27.

14.4.7 Power Dissipation

Because of the differential-amplifier nature of ECL, the gate current remains approximately constant and is simply steered from one side of the gate to the other depending on the input logic signals. Thus, the supply current and hence the gate power dissipation of unterminated ECL remain relatively constant independent of the logic state of the gate. It follows that no voltage spikes are introduced on the supply line. Such spikes can be a dangerous source of noise in a digital system. It follows that in ECL the need for supply-line bypassing[7] is not as great as in, say, TTL. This is another advantage of ECL.

[7]Achieved by connecting capacitances to ground at frequent intervals along the power-supply line on a printed-circuit board.

At this juncture we should reiterate a point we made earlier, namely, that although an ECL gate would operate with $V_{EE} = 0$ and $V_{CC} = +5.2$ V, the selection of $V_{EE} = -5.2$ V and $V_{CC} = 0$ V is recommended, because in the circuit, all signal levels are referenced to V_{CC}, and ground is certainly an excellent reference.

EXERCISE

14.16 For the ECL gate in Fig. 14.26, calculate an approximate value for the power dissipated in the circuit under the condition that all inputs are low and that the emitters of the output followers are left open. Assume that the reference circuit supplies four identical gates, and hence only a quarter of the power dissipated in the reference circuit should be attributed to a single gate.
Ans. 22.4 mW

14.4.8 Thermal Effects

In our analysis of the ECL gate of Fig. 14.26, we found that at room temperature the reference voltage V_R is −1.32 V. We have also shown that the midpoint of the output logic swing is approximately equal to this voltage, which is an ideal situation in that it results in equal high and low noise margins. In Example 14.4, we shall derive expressions for the temperature coefficients of the reference voltage and of the output low and high voltages. In this way, it will be shown that the midpoint of the output logic swing varies with temperature at the same rate as the reference voltage. As a result, although the magnitudes of the high and low noise margins change with temperature, their values remain equal. This is an added advantage of ECL and provides a demonstration of the high degree of design optimization of this gate circuit.

Example 14.4

We wish to determine the temperature coefficient of the reference voltage V_R and of the midpoint between V_{OL} and V_{OH}.

Solution

To determine the temperature coefficient of V_R, consider the circuit in Fig. E14.12 and assume that the temperature changes by +1°C. Denoting the temperature coefficient of the diode and transistor voltage drops by δ, where $\delta \simeq -2$ mV/°C, we obtain the equivalent circuit shown in Fig. 14.33. In the latter circuit, the changes in device voltage drops are considered as signals, and hence the power supply is shown as a signal ground.

In the circuit of Fig. 14.33 we have two signal generators, and we wish to analyze the circuit to determine ΔV_R, the change in V_R. We shall do so using the principle of superposition.[8] Consider first the branch R_1, D_1, D_2, 2δ, and R_2, and neglect the signal base current of Q_1. The voltage signal at the base of Q_1 can be easily obtained from

[8]Although the circuit contains diodes and a transistor, which are nonlinear elements, we can use superposition because we are dealing with small changes in voltages and currents, and thus the diodes and the transistor are replaced by their linear small-signal models.

Example 14.4 *continued*

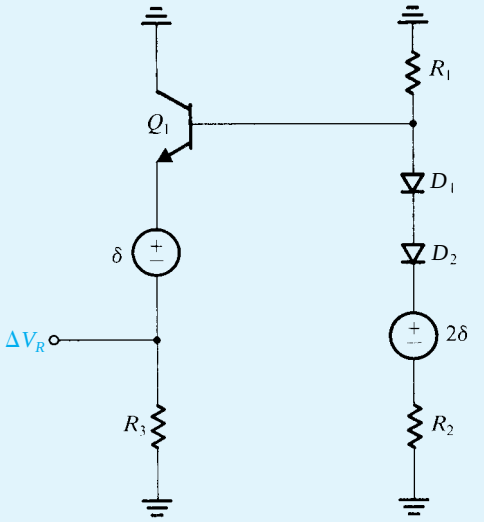

Figure 14.33 Equivalent circuit for determining the temperature coefficient of the reference voltage V_R.

$$v_{b1} = \frac{2\delta \times R_1}{R_1 + r_{d1} + r_{d2} + R_2}$$

where r_{d1} and r_{d2} denote the incremental resistances of diodes D_1 and D_2, respectively. The dc bias current through D_1 and D_2 is approximately 0.64 mA, and thus $r_{d1} = r_{d2} = 39.5\ \Omega$. Hence $v_{b1} \simeq 0.3\delta$. Since the gain of the emitter follower Q_1 is approximately unity, it follows that the component of ΔV_R due to the generator 2δ is approximately equal to v_{b1}; that is, $\Delta V_{R1} = 0.3\delta$.

Consider next the component of ΔV_R due to the generator δ. Reflection into the emitter circuit of the total resistance of the base circuit, $[R_1 \| (r_{d1} + r_{d2} + R_2)]$, by dividing it by $\beta + 1$ (with $\beta \simeq 100$) results in the following component of ΔV_R:

$$\Delta V_{R2} = -\frac{\delta \times R_3}{[R_B/(\beta+1)] + r_{e1} + R_3}$$

Here R_B denotes the total resistance in the base circuit, and r_{e1} denotes the emitter resistance of Q_1 ($\simeq 40\ \Omega$). This calculation yields $\Delta V_{R2} \simeq -\delta$. Adding this value to that due to the generator 2δ gives $\Delta V_R \simeq -0.7\delta$. Thus for $\delta = -2$ mV/°C, the temperature coefficient of V_R is +1.4 mV/°C.

We next consider the determination of the temperature coefficient of V_{OL}. The circuit on which to perform this analysis is shown in Fig. 14.34. Here we have three generators whose contributions can be considered separately and the resulting components of ΔV_{OL} summed. The result is

$$\Delta V_{OL} \simeq \Delta V_R \frac{-R_{C2}}{r_{eR} + R_E} \frac{R_T}{R_T + r_{e2}} - \delta \frac{-R_{C2}}{r_{eR} + R_E} \frac{R_T}{R_T + r_{e2}} - \delta \frac{R_T}{R_T + r_{e2} + R_{C2}/(\beta+1)}$$

Substituting the values given and those obtained throughout the analysis of this section, we find

$$\Delta V_{OL} \simeq -0.43\delta$$

The circuit for determining the temperature coefficient of V_{OH} is shown in Fig. 14.35, from which we obtain

$$\Delta V_{OH} = -\delta \frac{R_T}{R_T + r_{e2} + R_{C2}/(\beta+1)} = -0.93\delta$$

We now can obtain the variation of the midpoint of the logic swing as

$$\frac{\Delta V_{OL} + \Delta V_{OH}}{2} = -0.68\,\delta$$

which is approximately equal to that of the reference voltage $V_R(-0.7\,\delta)$.

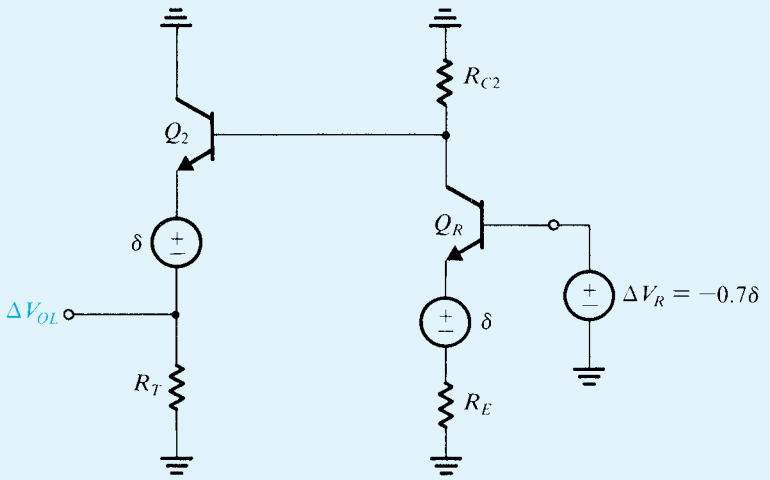

Figure 14.34 Equivalent circuit for determining the temperature coefficient of V_{OL}.

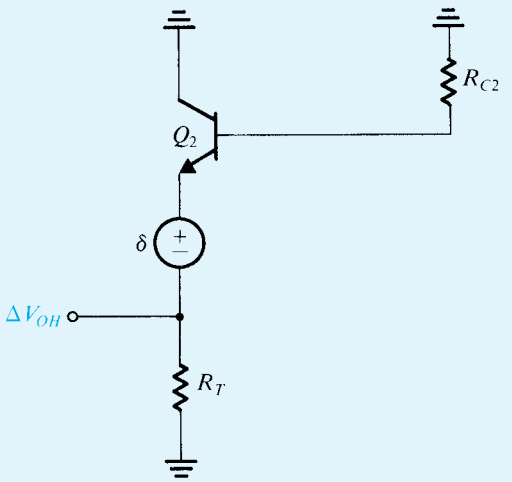

Figure 14.35 Equivalent circuit for determining the temperature coefficient of V_{OH}.

14.4.9 The Wired-OR Capability

The emitter–follower output stage of the ECL family allows an additional level of logic to be performed at very low cost by simply wiring the outputs of several gates in parallel. This is illustrated in Fig. 14.36, where the outputs of two gates are wired together. Note that the base–emitter diodes of the output followers realize an OR function: This **wired-OR** connection can be used to provide gates with high fan-in as well as to increase the flexibility of ECL in logic design.

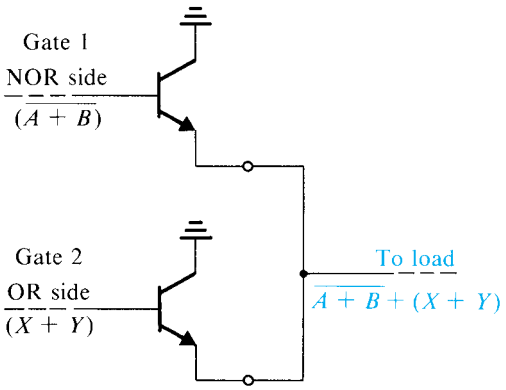

Figure 14.36 The wired-OR capability of ECL.

14.4.10 Final Remarks

We have chosen to study ECL by focusing on a commercially available circuit family. As has been demonstrated, a great deal of design optimization has been applied to create a very-high-performance family of SSI and MSI logic circuits. As already mentioned, ECL and some of its variants are also used in VLSI circuit design. Applications include very-high-speed processors such as those used in supercomputers, as well as high-speed and high-frequency communication systems. When employed in VLSI design, current–source biasing is almost always utilized. Further, a variety of circuit configurations are employed (see Rabaey, 1996).

⊕ 14.5 BiCMOS Digital Circuits

In this section, we provide an introduction to a VLSI circuit technology that is becoming increasingly popular, BiCMOS. As its name implies, BiCMOS technology combines *bi*polar and *CMOS* circuits on one IC chip. The aim is to combine the low-power, high-input impedance and wide noise margins of CMOS with the high current-driving capability of bipolar transistors. Specifically, CMOS, although a nearly ideal logic-circuit technology in many respects, has a limited current-driving capability. This is not a serious problem when the CMOS gate has to drive a few other CMOS gates. It becomes a serious issue, however, when relatively large capacitive loads (e.g., greater than 0.5 pF or so) are present. In such cases, one has to either resort to the use of elaborate CMOS buffer circuits or face the usually unacceptable consequence of long propagation delays. On the other hand, we know that by virtue of its much larger transconductance, the BJT is capable of large output currents. We have seen a practical illustration of that in the emitter–follower output stage of ECL.

Indeed, the high current-driving capability contributes to making ECL two to five times faster than CMOS (under equivalent conditions)—of course, at the expense of high power dissipation. In summary, then, BiCMOS seeks to combine the best of the CMOS and bipolar technologies to obtain a class of circuits that is particularly useful when output currents that are higher than possible with CMOS are needed. Furthermore, since BiCMOS technology is well suited for the implementation of high-performance analog circuits (see, e.g., Section 7.3.9), it makes possible the realization of both analog and digital functions on the same IC chip, making the "**system on a chip**" an attainable goal. The price paid is a more complex, and hence more expensive (than CMOS) processing technology.

14.5.1 The BiCMOS Inverter

A variety of BiCMOS inverter circuits have been proposed and are in use. All of these are based on the use of *npn* transistors to increase the output current available from a CMOS inverter. This can be most simply achieved by cascading each of the Q_N and Q_P devices of the CMOS inverter with an *npn* transistor, as shown in Fig. 14.37(a). Observe that this circuit can be thought of as utilizing the pair of complementary composite MOS-BJT devices shown in Fig. 14.37(b). These composite devices[9] retain the high input impedance of the MOS transistor while in effect multiplying its rather low g_m by the β of the BJT. It is also useful to observe that the output stage formed by Q_1 and Q_2 has what is known as the **totem-pole configuration** utilized by TTL.[10]

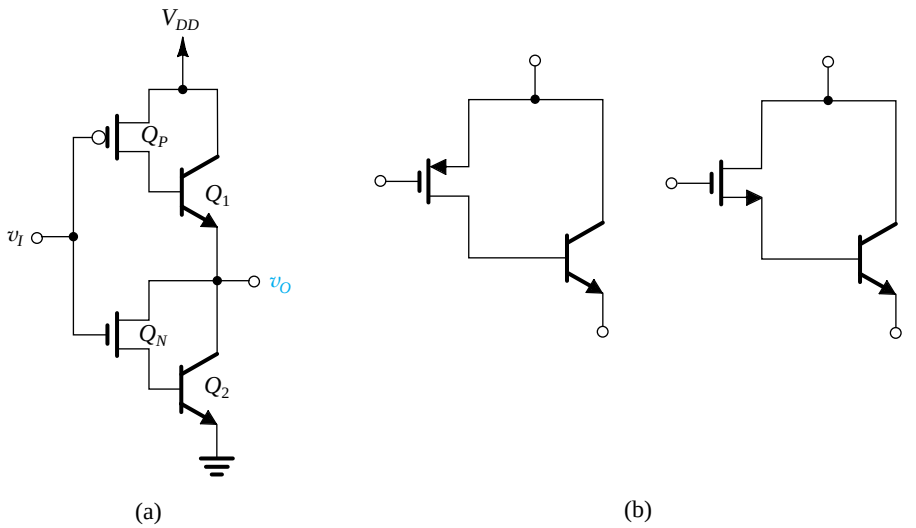

Figure 14.37 Development of the BiCMOS inverter circuit. **(a)** The basic concept is to use an additional bipolar transistor to increase the output current drive of each of Q_N and Q_P of the CMOS inverter. **(b)** The circuit in **(a)** can be thought of as utilizing these composite devices. **(c)** To reduce the turn-off times of Q_1 and Q_2, "bleeder resistors" R_1 and R_2 are added. **(d)** Implementation of the circuit in (**c**) using NMOS transistors to realize the resistors. **(e)** An improved version of the circuit in (**c**) obtained by connecting the lower end of R_1 to the output node.

[9]It is interesting to note that these composite devices were proposed as early as 1969 (see Lin et al., 1969).
[10]Refer to the CD accompanying this book or the book's website for a description of the basic TTL logic-gate circuit and its totem-pole output stage.

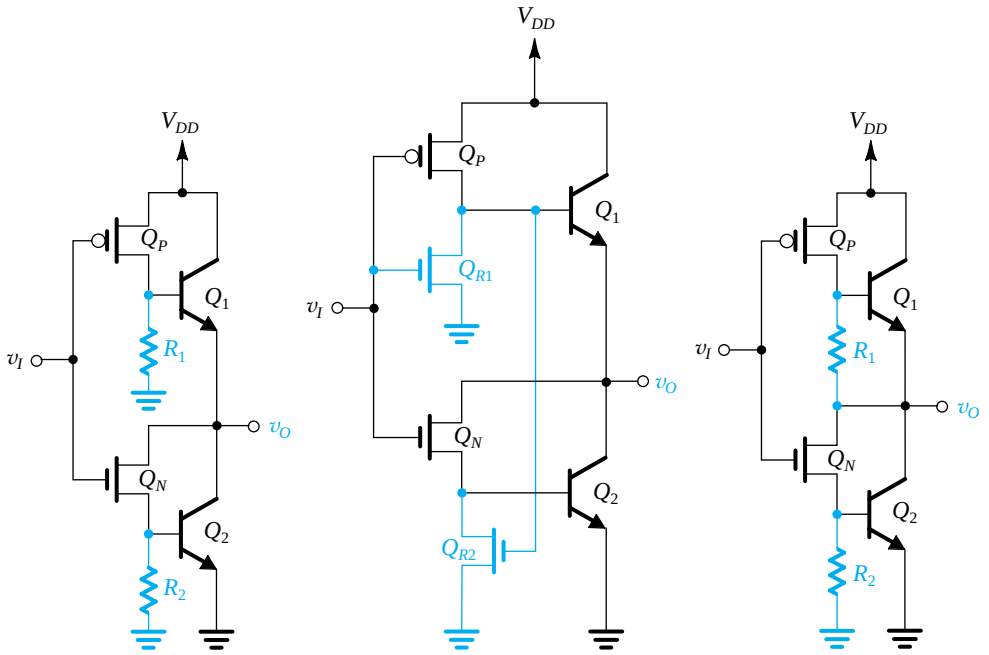

Figure 14.38 *continued*

The circuit of Fig. 14.37(a) operates as follows: When v_I is low, both Q_N and Q_2 are off while Q_P conducts and supplies Q_1 with base current, thus turning it on. Transistor Q_1 then provides a large output current to charge the load capacitance. The result is a very fast charging of the load capacitance and correspondingly a short low-to-high propagation delay, t_{PLH}. Transistor Q_1 turns off when v_O reaches a value of about $V_{DD} - V_{BE1}$, and thus the output high level is lower than V_{DD}, a disadvantage. When v_I goes high, Q_P and Q_1 turn off, and Q_N turns on, providing its drain current into the base of Q_2. Transistor Q_2 then turns on and provides a large output current that quickly discharges the load capacitance. Here again the result is a short high-to-low propagation delay, t_{PHL}. On the negative side, Q_2 turns off when v_O reaches a value of about V_{BE2}, and thus the output low level is greater than zero, a disadvantage.

Thus, while the circuit of Fig. 14.37(a) features large output currents and short propagation delays, it has the disadvantage of reduced logic swing and, correspondingly, reduced noise margins. There is also another and perhaps more serious disadvantage, namely, the relatively long turn-off delays of Q_1 and Q_2 arising from the absence of circuit paths along which the base charge can be removed. This problem can be solved by adding a resistor between the base of each of Q_1 and Q_2 and ground, as shown in Fig. 14.37(c). Now when either Q_1 or Q_2 is turned off, its stored base charge is removed to ground through R_1 or R_2, respectively. Resistor R_2 provides an additional benefit: With v_I high, and after Q_2 cuts off, v_O continues to fall below V_{BE2}, and the output node is pulled to ground through the series path of Q_N and R_2. Thus R_2 functions as a pull-down resistor. The Q_N–R_2 path, however, is a high-impedance one with the result that pulling v_O to ground is a rather slow process. Incorporating the resistor R_1, however, is disadvantageous from a static power-dissipation standpoint: When v_I is low, a dc path exists between V_{DD} and ground through the conducting Q_P and R_1. Finally, it should be noted that R_1 and R_2 take some of the drain currents of Q_P and Q_N away from the bases of Q_1 and Q_2 and thus slightly reduce the gate output current available to charge and discharge the load capacitance.

Figure 14.37(d) shows the way in which R_1 and R_2 are usually implemented. As indicated, NMOS devices Q_{R1} and Q_{R2} are used to realize R_1 and R_2. As an added innovation, these two transistors are made to conduct only when needed. Thus, Q_{R1} will conduct only when v_I rises, at which time its drain current constitutes a reverse base current for Q_1, speeding up its turn-off. Similarly, Q_{R2} will conduct only when v_I falls and Q_P conducts, pulling the gate of Q_{R2} high. The drain current of Q_{R2} then constitutes a reverse base current for Q_2, speeding up its turn-off.

As a final circuit for the BiCMOS inverter, we show the so-called *R*-circuit in Fig. 14.37(e). This circuit differs from that in Fig. 14.37(c) in only one respect: Rather than returning R_1 to ground, we have connected R_1 to the output node of the inverter. This simple change has two benefits. First, the problem of static power dissipation is now solved. Second, R_1 now functions as a pull-up resistor, pulling the output node voltage up to V_{DD} (through the conducting Q_P) after Q_1 has turned off. Thus, the *R* circuit in Fig. 14.37(e) does in fact have output levels very close to V_{DD} and ground.

As a final remark on the BiCMOS inverter, we note that the circuit is designed so that transistors Q_1 and Q_2 are never simultaneously conducting and neither is allowed to saturate. Unfortunately, sometimes the resistance of the collector region of the BJT in conjunction with large capacitive-charging currents causes saturation to occur. Specifically, at large output currents, the voltage developed across r_C (which can be of the order of 100 Ω) can lower the voltage at the intrinsic collector terminal and cause the CBJ to become forward biased. As the reader will recall, saturation is a harmful effect for two reasons: It limits the collector current to a value less than βI_B, and it slows down the transistor turn-off.

14.5.2 Dynamic Operation

A detailed analysis of the dynamic operation of the BiCMOS inverter circuit is a rather complex undertaking. Nevertheless, an estimate of its propagation delay can be obtained by considering only the time required to charge and discharge a load capacitance *C*. Such an approximation is justified when *C* is relatively large and thus its effect on inverter dynamics is dominant: in other words, when we are able to neglect the time required to charge the parasitic capacitances present at internal circuit nodes. Fortunately, this is usually the case in practice, for if the load capacitance is not large, one would use the simpler CMOS inverter. In fact, it has been shown (Embabi, Bellaouar, and Elmasry, 1993) that the speed advantage of BiCMOS (over CMOS) becomes evident only when the gate is required to drive a large fan-out or a large load capacitance. For instance, at a load capacitance of 50 fF to 100 fF, BiCMOS and CMOS typically feature equal delays. However, at a load capacitance of 1 pF, t_P of a BiCMOS inverter is 0.3 ns, whereas that of an otherwise comparable CMOS inverter is about 1 ns.

Finally, in Fig. 14.38, we show simplified equivalent circuits that can be employed in obtaining rough estimates of t_{PLH} and t_{PHL} of the *R*-type BiCMOS inverter (see Problem 14.49).

14.5.3 BiCMOS Logic Gates

In BiCMOS, the logic is performed by the CMOS part of the gate, with the bipolar portion simply functioning as an output stage. It follows that BiCMOS logic-gate circuits can be generated following the same approach used in CMOS. As an example, we show in Fig. 14.39 a BiCMOS two-input NAND gate.

As a final remark, we note that BiCMOS technology is applied in a variety of products including microprocessors, static RAMs, and gate arrays (see Alvarez, 1993).

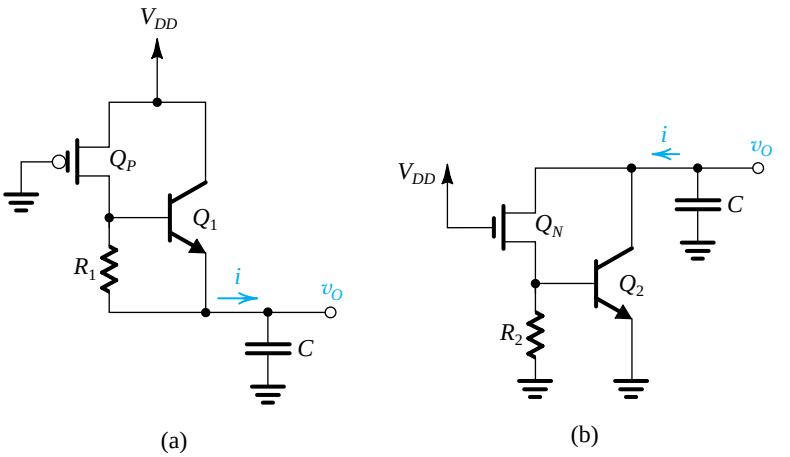

Figure 14.39 Equivalent circuits for charging and discharging a load capacitance C. Note that C includes all the capacitances present at the output node.

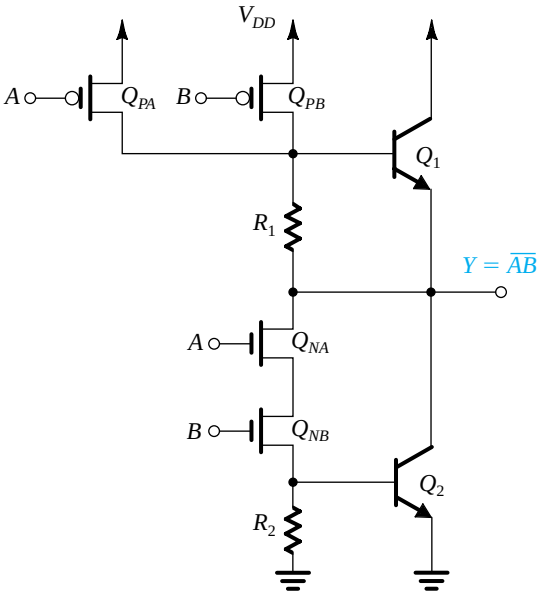

Figure 14.40 A BiCMOS two-input NAND gate.

EXERCISE

D14.17 The threshold voltage of the BiCMOS inverter of Fig. 14.37(e) is the value of v_I at which both Q_N and Q_P are conducting equal currents and operating in the saturation region. At this value of v_I, Q_2 will be on, causing the voltage at the source of Q_N to be approximately 0.7 V. It is required to design the circuit so that the threshold voltage is equal to $V_{DD}/2$. For $V_{DD} = 5$ V, $|V_t| = 0.6$ V, and assuming equal channel lengths for Q_N and Q_P and that $\mu_n \simeq 2.5\,\mu_p$, find the required ratio of widths, W_p/W_n.

Ans. 1

Summary

- Standard CMOS logic utilizes two transistors, an NMOS and a PMOS, for each input variable. Thus the circuit complexity, silicon area, and parasitic capacitance all increase with fan-in.
- To reduce the device count, two other forms of static CMOS, namely, pseudo-NMOS and pass-transistor logic (PTL), are employed in special applications as supplements to standard CMOS.
- Pseudo-NMOS utilizes the same PDN as in standard CMOS logic but replaces the PUN with a single PMOS transistor whose gate is grounded and thus is permanently on. Unlike standard CMOS, pseudo-NMOS is a ratioed form of logic in which V_{OL} is determined by the ratio r of k_n to k_p. Normally, r is selected in the range of 4 to 10 and its value determines the noise margins.
- Pseudo-NMOS has the disadvantage of dissipating static power when the output of the logic gate is low. Static power can be eliminated by turning the PMOS load on for only a brief interval, known as the precharge interval, to charge the capacitance at the output node to V_{DD}. Then the inputs are applied, and depending on the input combination, the output node either remains high or is discharged through the PDN. This is the essence of dynamic logic.
- Pass-transistor logic utilizes either single NMOS transistors or CMOS transmission gates to implement a network of switches that are controlled by the input logic variables. Switches implemented by single NMOS transistors, though simple, result in the reduction of V_{OH} from V_{DD} to $V_{DD} - V_t$.
- The CMOS transmission gate, composed of the parallel connection of an NMOS and a PMOS transistor, is a very effective switch in both analog and digital applications. It passes the entire input signal swing, 0 to V_{DD}. As well, it has an almost constant "on" resistance over the full output range.
- A particular form of dynamic logic circuits, known as Domino logic, allows the cascading of dynamic logic gates.
- Emitter-coupled logic (ECL) is the fastest commercially available logic-circuit family. It achieves its high speed of operation by avoiding transistor saturation and by utilizing small logic-signal swings.
- In ECL the input signals are used to steer a bias current between a reference transistor and an input transistor. The basic gate configuration is that of a differential amplifier.
- There are two popular commercially available ECL types: ECL 10K, having $t_p = 2$ ns, $P_D = 25$ mW, and $PDP = 50$ pJ; and ECL 100K, having $t_p = 0.75$ ns, $P_D = 40$ mW, and $PDP = 30$ pJ. ECL 10K is easier to use because the rise and fall times of its signals are deliberately made long (about 3.5 ns).
- Because of the very high operating speeds of ECL, care should be taken in connecting the output of one gate to the input of another. Transmission-line techniques are usually employed.
- The design of the ECL gate is optimized so that the noise margins are equal and remain equal as temperature changes.
- The ECL gate provides two complementary outputs, realizing the OR and NOR functions.
- The outputs of ECL gates can be wired together to realize the OR function of the individual output variables.
- BiCMOS combines the low-power and wide noise margins of CMOS with the high current-driving capability (and thus the short gate delays) of BJTs to obtain a technology that is capable of implementing very dense, low-power, high-speed VLSI circuits that can also include analog functions.

Problems involving design are marked with D throughout the text. As well, problems are marked with asterisks to describe their degree of difficulty. Difficult problems are marked with an asterisk (*); more difficult problems with two asterisks (**); and very challenging and/or time-consuming problems with three asterisks (***).

Section 14.1: Pseudo-NMOS Logic Circuits

14.1 The purpose of this problem is to compare the value of t_{PLH} obtained with a resistive load (see Fig. P14.1a) to that obtained with a current–source load (see Fig. P14.1b). For a fair comparison, let the current source $I = V_{DD}/R_D$, which is the initial current available to charge the capacitor in the case of a resistive load. Find t_{PLH} for each case, and hence the percentage reduction obtained when a current–source load is used.

D ***14.2** Design a pseudo-NMOS inverter that has equal capacitive charging and discharging currents at $v_O = V_{DD}/4$ for use in a system with $V_{DD} = 2.5$ V, $|V_t| = 0.5$ V, $k_n' = 115\ \mu A/V^2$, $k_p' = 30\mu A/V^2$, and $(W/L)_n = 1.5$. What are the values of $(W/L)_p$, V_{IL}, V_{IH}, V_M, V_{OH}, V_{OL}, NM_H, and NM_L?

14.3 Find t_{PLH}, t_{PHL}, and t_P for a pseudo-NMOS inverter fabricated in a 0.13-μm CMOS technology for which $V_{DD} = 1.2$ V, $V_t = 0.4$ V, and $\mu_n C_{ox} = 4\mu_p C_{ox} = 430\ \mu A/V^2$. Assume that the inverter has $r = 4$ and $(W/L)_n = 1$ and that the equivalent load capacitance is 10 fF.

***14.4** Use Eq. (14.13) to find the value of r for which NM_L is maximized. What is the corresponding value of NM_L for the case $V_{DD} = 2.5$ V and $V_t = 0.5$ V?

D 14.5 Design a pseudo-NMOS inverter that has $V_{OL} = 0.1$ V. Let $V_{DD} = 2.5$ V, $|V_t| = 0.5$ V, $k_n' = 4k_p' = 120\ \mu A/V^2$, and $(W/L)_p = 1$. What is the value of $(W/L)_n$? Calculate the values of NM_L and the static power dissipation.

14.6 For what value of r does NM_H of a pseudo-NMOS inverter become zero? Prepare a table of N_{MH} and N_{ML} versus r, for $r = 1$ to 16. Let $V_{DD} = 2.5$ V and $V_t = 0.5$ V.

14.7 For a pseudo-NMOS inverter, what value of r results in $NM_L = NM_H$? Let $V_{DD} = 2.5$ V and $|V_t| = 0.5$ V. What is the resulting margin?

D *14.8 It is required to design a minimum-area pseudo-NMOS inverter with equal high and low noise margins using a 2.5-V supply and devices for which $|V_t| = 0.5$ V, $k_n' = 4k_p' = 120\ \mu A/V^2$, and the minimum-size device has $(W/L) = 1$. Use $r = 3.2$ and show that $NM_L \simeq NM_H$. Specify the values of $(W/L)_n$ and $(W/L)_p$. What is the static power dissipated in this gate? What is the ratio of propagation delays for low-to-high and high-to-low transitions? For an equivalent load capacitance of 0.1 pF, find t_{PLH}, t_{PHL}, and t_P. At what frequency of operation would the static and dynamic power levels be equal? Is this speed of operation possible in view of the t_P value you found?

D 14.9 Sketch a pseudo-NMOS realization of the function $Y = \overline{A + B(C + D)}$.

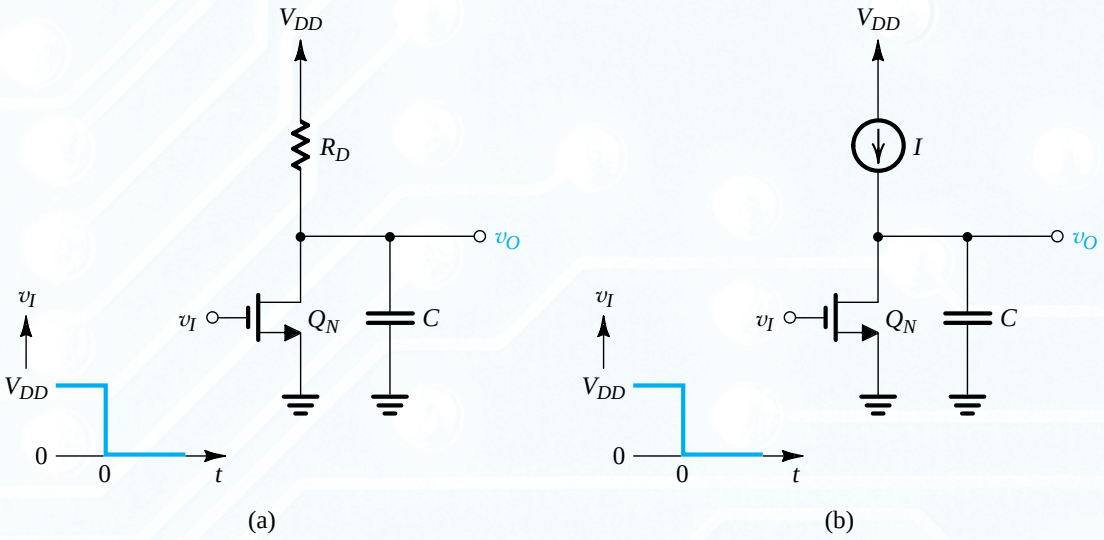

Figure P 14.1

D 14.10 Sketch a pseudo-NMOS realization of the exclusive-OR function $Y = A\bar{B} + \bar{A}B$.

D 14.11 Consider a four-input pseudo-NMOS NOR gate in which the NMOS devices have $(W/L)_n = 0.27\ \mu m/0.18\ \mu m$. It is required to find $(W/L)_p$ so that the worst-case value of V_{OL} is 0.1 V. Let $V_{DD} = 1.8$ V, $|V_t| = 0.5$ V, and $k_n' = 4k_p' = 300\ \mu A/V^2$. Assume that the minimum width possible is 0.2 µm.

14.12 This problem investigates the effect of velocity saturation (Section 13.5.2) on the operation of a pseudo-NMOS inverter fabricated in a 0.13-µm CMOS process for which, $V_{DD} = 1.2$ V, $V_t = 0.4$ V, $\mu_n C_{ox} = 4\mu_p C_{ox} = 430\ \mu A/V^2$, and $|V_{DSsatp}| = 0.6$ V. Consider the case with $v_I = V_{DD}$ and $v_O = V_{OL}$. Note that Q_P will be operating in the velocity-saturation region. Find its current I_{Dsat} and use it to determine V_{OL}.

Section 10.2: Pass-Transistor Logic Circuits

14.13 Consider the NMOS transistor switch in the circuits of Figs. 14.8 and 14.9 to be fabricated in a 0.18-µm CMOS technology for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu A/V^2$, $|V_{t0}| = 0.5$ V, $\gamma = 0.3\ V^{1/2}$, $2\phi_f = 0.85$ V, and $V_{DD} = 1.8$ V. Let the transistor have $W/L = 1.5$, and assume that the total capacitance between the output node and ground is $C = 10$ fF.

(a) For the case $v_I = V_{DD}$, find V_{OH}.
(b) If the output feeds a CMOS inverter having $(W/L)_p = 2(W/L)_n = 0.54\ \mu m/0.18\ \mu m$, find the static current of the inverter and its power dissipation when the inverter input is at the value found in (a). Also, find the inverter output voltage.
(c) Find t_{PLH}.
(d) For v_I going low (Fig. 14.9), find t_{PHL}.
(e) Find t_P.

***14.14** A designer, beginning to experiment with the idea of pass-transistor logic, seizes upon what he sees as two good ideas:

(a) that a string of minimum-size single MOS transistors can do complex logic functions, but
(b) that there must always be a path between output and a supply terminal.

Correspondingly, he first considers two circuits (shown in Fig. P14.14). For each, express Y as a function of A and B. In each case, what can be said about general operation? About the logic levels at Y? About node X? Do either of these circuits look familiar? If in each case the terminal connected to V_{DD} is instead connected to the output of a CMOS inverter whose input is connected to a signal C, what does the function Y become?

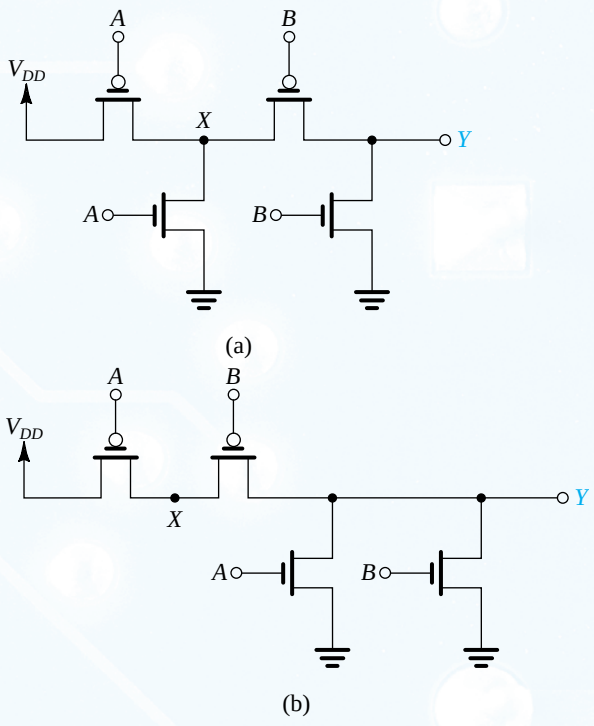

Figure P14.14

14.15 Consider the circuits in Fig. P14.14 with all PMOS transistors replaced with NMOS, and all NMOS by PMOS, and with ground and V_{DD} connections interchanged. What do the output functions Y become?

14.16 An NMOS pass-transistor switch with $W/L = 1.2\ \mu m/0.8\ \mu m$, used in a 3.3-V system for which $V_{t0} = 0.8$ V, $\gamma = 0.5\ V^{1/2}$, $2\phi_f = 0.6$ V, $\mu_n C_{ox} = 3\mu_p C_{ox} = 75\ \mu A/V^2$, drives a 100-fF load capacitance at the input of a matched standard CMOS inverter using $(W/L)_n = 1.2\ \mu m/0.8\ \mu m$. For the switch gate terminal at V_{DD}, evaluate the switch V_{OH} and V_{OL} for inputs at V_{DD} and 0 V, respectively. For this value of V_{OH}, what inverter static current results? Estimate t_{PLH} and t_{PHL} for this arrangement as measured from the input to the output of the switch itself.

D ***14.17 The purpose of this problem is to design the level-restoring circuit of Fig. 14.10 and gain insight into its operation. Assume that $k_n' = 3k_p' = 75\ \mu A/V^2$, $V_{DD} = 3.3$ V, $|V_{t0}| = 0.8$ V, $\gamma = 0.5\ V^{1/2}$ $2\phi_f = 0.6$ V, $(W/L)_1 = (W/L)_n = 1.2\ \mu m/0.8\ \mu m$, $(W/L)_p = 3.6\ \mu m\ /\ 0.8\ \mu m$, and $C = 20$ fF. Let $v_B = V_{DD}$.

(a) Consider first the situation with $v_A = V_{DD}$. Find the value of the voltage v_{O1} that causes v_{O2} to drop a threshold voltage

below V_{DD}; that is, to 2.5 V so that Q_R turns on. At this value of v_{O1}, find V_t of Q_1. What is the capacitor-charging current available at this time (i.e., just prior to Q_R turning on)? What is it at $v_{O1} = 0$? What is the average current available for charging C? Estimate the time t_{PLH} for v_{O1} to rise from 0 to the value at which Q_R turns on. Note that after Q_R turns on, v_{O1} rises to V_{DD}.
(b) Now, to determine a suitable W/L ratio for Q_R, consider the situation when v_A is brought down to 0 V and Q_1 conducts and begins to discharge C. The voltage v_{O1} will begin to drop. Meanwhile, v_{O2} is still low and Q_R is conducting. The current that Q_R conducts subtracts from the current of Q_1, reducing the current available to discharge C. Find the value of v_{O1} at which the inverter begins to switch. This is $V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$. Then, find the current that Q_1 conducts at this value of v_{O1}. Choose W/L for Q_R so that the maximum current it conducts is limited to one-half the value of the current in Q_1. What is the W/L you have chosen? Estimate t_{PHL} as the time for v_{O1} to drop from V_{DD} to V_{IH}.

14.18 Figure P14.18 shows a PMOS transistor operating as a switch in the on position.

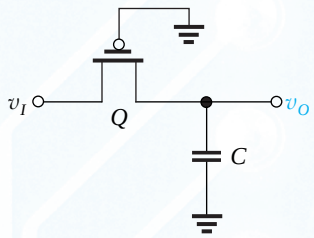

Figure P14.18

(a) If initially $v_O = 0$ and at $t = 0$, v_I is raised to V_{DD}, what is the final value V_{OH} reached at the output?
(b) If initially, $v_O = V_{DD}$ and at $t = 0$, v_I is lowered to 0 V, what is the final value V_{OL} reached at the output?
(c) For the situation in (a), find t_{PLH} for v_O to rise from 0 to $V_{DD}/2$. Let $k_p = 225\ \mu A/V^2$, $V_{DD} = 1.8$ V, and $|V_{tp}| = 0.5$ V.

14.19 The transmission gate in Fig. 14.12(a) and 14.12(b) is fabricated in a CMOS process technology for which $k_n' = 4k_p' = 300\ \mu A/V^2$, $|V_{t0}| = 0.5$ V, $\gamma = 0.3\ V^{1/2}$, $2\phi_f = 0.85$ V, and $V_{DD} = 1.8$ V. Let Q_N and Q_P have $(W/L)_n = (W/L)_p = 1.5$. The total capacitance at the output node is 15 fF.

(a) What are the values of V_{OH} and V_{OL}?
(b) For the situation in Fig. 14.12(a), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PLH})$, $i_{DP}(t_{PLH})$, and t_{PLH}.
(c) For the situation depicted in Fig. 14.12(b), find $i_{DN}(0)$, $i_{DP}(0)$, $i_{DN}(t_{PHL})$, $i_{DP}(t_{PHL})$, and t_{PHL}. At what value of v_O will Q_P turn off?
(d) Find t_P.

14.20 For the transmission gate specified in Problem 14.19, find R_{TG} at $v_O = 0$ and 0.9 V. Use the average of those values to determine t_{PLH} for the situation in which $C = 15$ fF.

***14.21** Refer to the situation in Fig. 14.12(b). Derive expressions for R_{Neq}, R_{Peq}, and R_{TG} following the approach used in Section 14.2.4 for the capacitor-charging case. Evaluate the value of R_{TG} for $v_O = V_{DD}$ and $v_O = V_{DD}/2$ for the process technology specified in Problem 14.19. Find the average value of R_{TG} and use it to determine t_{PHL} for the case $C = 15$ fF.

14.22 A transmission gate for which $(W/L)_n = (W/L)_p = 1.5$ is fabricated in a 0.18-μm CMOS technology and used in a circuit for which $C = 10$ fF. Use Eq. (14.36) to obtain an estimate of R_{TG} and hence of the propagation delay t_P.

14.23 Figure P14.23 shows a chain of transmission gates. This situation often occurs in circuits such as adders and multiplexers. Consider the case when all the transmission gates are turned on and a step voltage V_{DD} is applied to the input. The propagation delay t_P can be determined from the Elmore delay formula as follows:

$$t_P = 0.69 \sum_{k=0}^{n} kCR_{TG}$$

where R_{TG} is the resistance of each transmission gate, C is the capacitance between each node and ground, and n is the

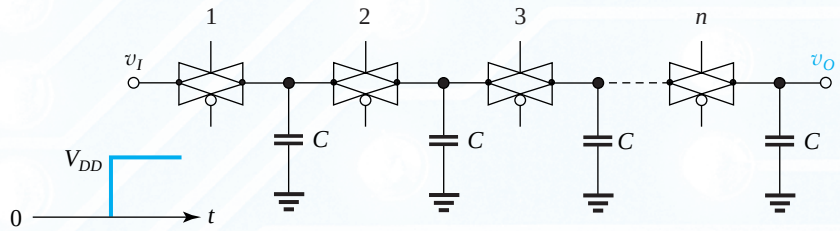

Figure P14.23

number of transmission gates in the chain. Note that the sum of the series in this formula is given by

$$t_P = 0.69CR_{TG}\,\frac{n(n+1)}{2}$$

Now evaluate t_P for the case of 16 transmission gates with $R_{TG} = 10\ \text{k}\Omega$ and $C = 10$ fF.

D 14.24 (a) Use the idea embodied in the exclusive-OR realization in Fig. 14.17 to realize $\overline{Y} = AB + \overline{A}\,\overline{B}$. That is, find a realization for $\overline{Y}$ using two transmission gates.

(b) Now combine the circuit obtained in (a) with the circuit in Fig. 14.17 to obtain a realization of the function $Z = \overline{Y}C + Y\overline{C}$, where C is a third input. Sketch the complete 12-transistor circuit realization of Z. Note that Z is a three-input exclusive-OR.

D *14.25 Using the idea presented in Fig. 14.18, sketch a CPL circuit whose outputs are $Y = A\overline{B} + \overline{A}B$ and $\overline{Y} = AB + \overline{A}\,\overline{B}$.

D 14.26 Extend the CPL idea in Fig. 14.18 to three variables to form $Z = ABC$ and $\overline{Z} = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$.

Section 14.3: Dynamic MOS Logic Circuits

D 14.27 Based on the basic dynamic logic circuit of Fig. 14.19, sketch complete circuits for NOT, NAND, and NOR gates, the latter two with two inputs, and a circuit for which $\overline{Y} = AB + CD$.

14.28 In this and the following problem, we investigate the dynamic operation of a two-input NAND gate realized in the dynamic logic form and fabricated in a CMOS process technology for which $k_n' = 3k_p' = 75\ \mu\text{A/V}^2$, $V_{tn} = -V_{tp} = 0.8$ V, and $V_{DD} = 3$ V. To keep C_L small, minimum-size NMOS devices are used for which $W/L = 1.2\ \mu\text{m}/0.8\ \mu\text{m}$ (this includes Q_e). The PMOS precharge transistor Q_p has $2.4\ \mu\text{m}/0.8\ \mu\text{m}$. The capacitance C_L is found to be 30 fF. Consider the precharge operation with the gate of Q_p at 0 V, and assume that at $t = 0$, C_L is fully discharged. We wish to calculate the rise time of the output voltage, defined as the time for v_Y to rise from 10% to 90% of the final value of 3 V. Find the current at $v_Y = 0.3$ V and the current at $v_Y = 2.7$ V, then compute an approximate value for t_r, $t_r = C_L(2.7 - 0.3)/I_{\text{av}}$, where I_{av} is the average value of the two currents.

14.29 For the gate specified in Problem 14.28, evaluate the high-to-low propagation delay, t_{PHL}. To obtain an approximate value of t_{PHL}, replace the three series NMOS transistors with an equivalent device and find the average discharge current.

14.30 The leakage current in a dynamic-logic gate causes the capacitor C_L to discharge during the evaluation phase, even if the PDN is not conducting. For $C_L = 15$ fF, and $I_{\text{leakage}} = 10^{-12}$ A, find the longest allowable evaluate time if the decay in output voltage is to be limited to 0.2 V. If the precharge interval is much shorter than the maximum allowable evaluate time, find the minimum clocking frequency required.

***14.31** In this problem, we wish to calculate the reduction in the output voltage of a dynamic-logic gate as a result of charge redistribution. Refer to the circuit in Fig. 14.21(a), and assume that at $t = 0-$, $v_Y = V_{DD}$, and $v_{C1} = 0$. At $t = 0$, ϕ goes high and Q_p turns off, and simultaneously the voltage at the gate of Q_1 goes high (to V_{DD}), turning Q_1 on. Transistor Q_1 will remain conducting until either the voltage at its source (v_{C1}) reaches $V_{DD} - V_{tn}$ or until $v_Y = v_{C1}$, whichever comes first. In both cases, the final value of v_Y can be found using charge conservation; that is, by equating the charge gained by C_1 to the charge lost by C_L.

(a) Convince yourself that the first situation obtains when $|\Delta v_Y| \le V_{tn}$.
(b) For each of the two situations, derive an expression for Δv_Y.
(c) Find an expression for the maximum ratio (C_1/C_L) for which $|\Delta v_Y| \le V_{tn}$.
(d) For $V_{tn} = 1$ V, $V_{DD} = 5$ V, $C_L = 30$ fF, and neglecting the body effect in Q_1, find the drop in voltage at the output in the two cases: (a) $C_1 = 5$ fF and (b) $C_1 = 10$ fF.

14.32 Solve the problem in Exercise 14.10 symbolically (rather than numerically). Refer to Fig E14.10 and assume Q_{eq1} and Q_{eq2} to be identical with threshold voltages $V_{tn} = 0.2V_{DD}$ and transconductance parameters k_n. Also, let $C_{L1} = C_{L2}$. Derive an expression for the drop in the output voltage, Δv_{Y2}.

14.33 For the four-input dynamic-logic NAND gate analyzed in Example 14.3, estimate the maximum clocking frequency allowed.

Section 14.4: Emitter-Coupled Logic (ECL)

D 14.34 For the ECL circuit in Fig. P14.34, the transistors exhibit V_{BE} of 0.75 V at an emitter current I and have very high β.

(a) Find V_{OH} and V_{OL}.
(b) For the input at B that is sufficiently negative for Q_B to be cut off, what voltage at A causes a current of $I/2$ to flow in Q_R?
(c) Repeat (b) for a current in Q_R of $0.99I$.
(d) Repeat (c) for a current in Q_R of $0.01I$.
(e) Use the results of (c) and (d) to specify V_{IL} and V_{IH}.
(f) Find NM_H and NM_L.
(g) Find the value of IR that makes the noise margins equal to the width of the transition region, $V_{IH} - V_{IL}$.

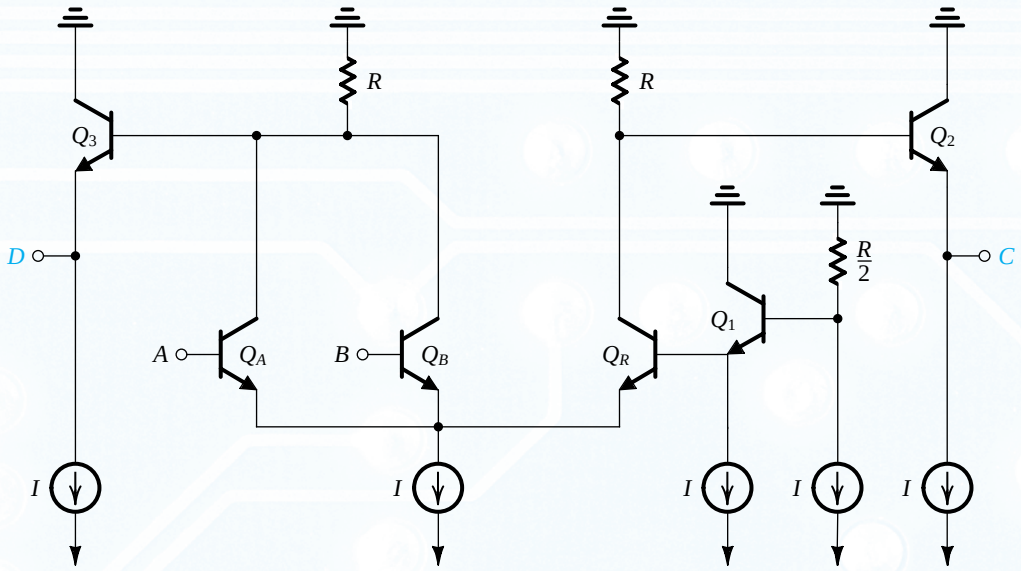

Figure P14.34

(h) Using the *IR* value obtained in (g), give numerical values for V_{OH}, V_{OL}, V_{IH}, V_{IL}, and V_R for this ECL gate.

***14.35** Three logic inverters are connected in a ring. Specifications for this family of gates indicate a typical propagation delay of 3 ns for high-to-low output transitions and 7 ns for low-to-high transitions. Assume that for some reason the input to one of the gates undergoes a low-to-high transition. By sketching the waveforms at the outputs of the three gates and keeping track of their relative positions, show that the circuit functions as an oscillator. What is the frequency of oscillation of this ring oscillator? In each cycle, how long is the output high? low?

***14.36** Following the idea of a ring oscillator introduced in Problem 14.35, consider an implementation using a ring of five ECL 100K inverters. Assume that the inverters have linearly rising and falling edges (and thus the waveforms are trapezoidal in shape). Let the 0 to 100% rise and fall times be equal to 1 ns. Also, let the propagation delay (for both transitions) be equal to 1 ns. Provide a labeled sketch of the five output signals, taking care that relevant phase information is provided. What is the frequency of oscillation?

D ***14.37** Using the logic and circuit flexibility of ECL indicated by Figs. 14.26 and 14.36, sketch an ECL logic circuit that realizes the exclusive OR function, $Y = \bar{A}B + A\bar{B}$. Give a logic diagram (as opposed to a circuit diagram).

***14.38** For the circuit in Fig. 14.28 whose transfer characteristic is shown in Fig. 14.29, calculate the incremental voltage gain from input to the OR output at points *x*, *m*, and *y* of the transfer characteristic. Assume $\beta = 100$. Use the results of Exercise 14.14, and let the output at *x* be –1.77 V and that at *y* be –0.88 V. (*Hint*: Recall that *x* and *y* are defined by a 1%, 99% current split.)

14.39 For the circuit in Fig. 14.28 whose transfer characteristic is shown in Fig. 14.29, find V_{IL} and V_{IH} if *x* and *y* are defined as the points at which

(a) 90% of the current I_E is switched.
(b) 99.9% of the current I_E is switched.

14.40 For the symmetrically loaded circuit of Fig. 14.28 and for typical output signal levels ($V_{OH} = -0.88$ V and $V_{OL} = -1.77$ V), calculate the power lost in both load resistors R_T and both output followers. What then is the total power dissipation of a single ECL gate, including its symmetrical output terminations?

14.41 Considering the circuit of Fig. 14.30, what is the value of β of Q_2, for which the high noise margin (NM_H) is reduced by 50%?

***14.42** Consider an ECL gate whose inverting output is terminated in a 50-Ω resistance connected to a –2-V supply. Let the total load capacitance be denoted *C*. As the input of

the gate rises, the output emitter follower cuts off and the load capacitance C discharges through the 50-Ω load (until the emitter follower conducts again). Find the value of C that will result in a discharge time of 1 ns. Assume that the two output levels are –0.88 V and –1.77 V.

14.43 For signals whose rise and fall times are 3.5 ns, what length of unterminated gate-to-gate wire interconnect can be used if a ratio of rise time to return time of 5 to 1 is required? Assume the environment of the wire to be such that the signal propagates at two-thirds the speed of light (which is 30 cm/ns).

***14.44** For the circuit in Fig. P14.44, let the levels of the inputs A, B, C, and D be 0 and +5 V. For all inputs low at 0 V, what is the voltage at E? If A and C are raised to +5 V, what is the voltage at E? Assume $|V_{BE}| = 0.7$ V and $\beta = 50$. Express E as a logic function of A, B, C, and D.

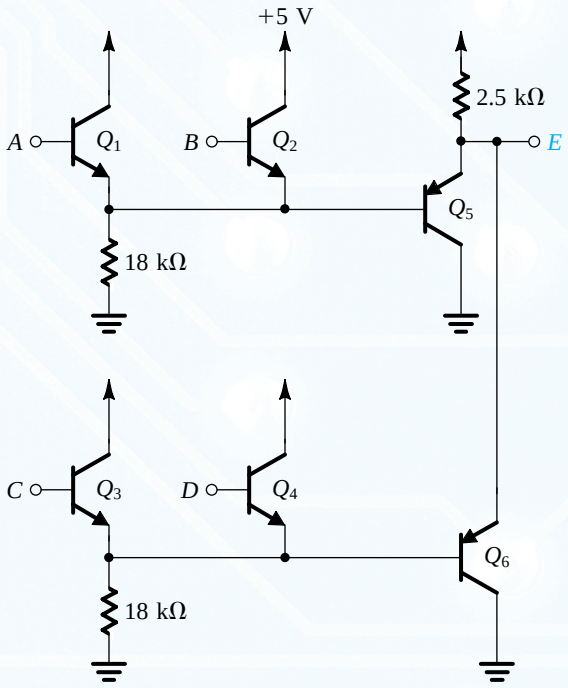

Figure P14.44

Section 14.5: BiCMOS Digital Circuits

14.45 Consider the conceptual BiCMOS circuit of Fig. 14.37(a), for the conditions that $V_{DD} = 5$ V, $|V_t| = 1$ V, $V_{BE} = 0.7$ V, $\beta = 100$, $k_n' = 2.5k_p' = 100\ \mu A/V^2$, and $(W/L)_n = 2\ \mu m/1\ \mu m$. For $v_I = v_O = V_{DD}/2$, find $(W/L)_p$ so that $I_{EQ_1} = I_{EQ_2}$. What is this totem-pole transient current?

14.46 Consider the conceptual BiCMOS circuit of Fig. 14.37(a) for the conditions stated in Problem 14.45. What is the threshold voltage of the inverter if both Q_N and Q_P have $W/L = 2\ \mu m/1\ \mu m$? What totem-pole current flows at v_I equal to the threshold voltage?

D *14.47 Consider the choice of values for R_1 and R_2 in the circuit of Fig. 14.37(c). An important consideration in making this choice is that the loss of base drive current will be limited. This loss becomes particularly acute when the current through Q_N and Q_P becomes small. This in turn happens near the end of the output signal swing when the associated MOS device is deeply in triode operation (say at $|v_{DS}| = |V_t|/3$). Determine values for R_1 and R_2 so that the loss in base current is limited to 50%. What is the ratio R_1/R_2? Repeat for a 20% loss in base drive.

***14.48** For the circuit of Fig. 14.37(a) with parameters as in Problem 14.45 and with $(W/L)_p = (W/L)_n$, estimate the propagation delays t_{PLH}, t_{PHL} and t_P obtained for a load capacitance of 2 pF. Assume that the internal node capacitances do not contribute much to this result. Use average values for the charging and discharging currents.

***14.49** Repeat Problem 14.48 for the circuit in Fig. 14.37(e), assuming that $R_1 = R_2 = 5$ kΩ.

D 14.50 Consider the dynamic response of the NAND gate of Fig. 14.39 with a large external capacitive load. If the worst-case response is to be identical to that of the inverter of Fig. 14.37(e), how must the W/L ratios of Q_{NA}, Q_{NB}, Q_N, Q_{PA}, Q_{PB}, and Q_P be related?

D 14.51 Sketch the circuit of a BiCMOS two-input NOR gate. If, when loaded with a large capacitance, the gate is to have worst-case delays equal to the corresponding values of the inverter of Fig. 14.37(e), find W/L of each transistor in terms of $(W/L)_n$ and $(W/L)_p$.