

## CHAPTER 2

# Operational Amplifiers

Introduction	53	2.6 DC Imperfections	88
2.1 The Ideal Op Amp	54	2.7 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance	97
2.2 The Inverting Configuration	58	2.8 Large-Signal Operation of Op Amps	102
2.3 The Noninverting Configuration	67	Summary	107
2.4 Difference Amplifiers	71	Problems	108
2.5 Integrators and Differentiators	80		

## IN THIS CHAPTER YOU WILL LEARN

1. The terminal characteristics of the ideal op amp.
2. How to analyze circuits containing op amps, resistors, and capacitors.
3. How to use op amps to design amplifiers having precise characteristics.
4. How to design more sophisticated op-amp circuits, including summing amplifiers, instrumentation amplifiers, integrators, and differentiators.
5. Important nonideal characteristics of op amps and how these limit the performance of basic op-amp circuits.

---

## Introduction

Having learned basic amplifier concepts and terminology, we are now ready to undertake the study of a circuit building block of universal importance: The operational amplifier (op amp). Op amps have been in use for a long time, their initial applications being primarily in the areas of analog computation and sophisticated instrumentation. Early op amps were constructed from discrete components (vacuum tubes and then transistors, and resistors), and their cost was prohibitively high (tens of dollars). In the mid-1960s the first integrated-circuit (IC) op amp was produced. This unit (the  $\mu\text{A}$  709) was made up of a relatively large number of transistors and resistors all on the same silicon chip. Although its characteristics were poor (by today's standards) and its price was still quite high, its appearance signaled a new era in electronic circuit design. Electronics engineers started using op amps in large quantities, which caused their price to drop dramatically. They also demanded better-quality op amps. Semiconductor manufacturers responded quickly, and within the span of a few years, high-quality op amps became available at extremely low prices (tens of cents) from a large number of suppliers.

One of the reasons for the popularity of the op amp is its versatility. As we will shortly see, one can do almost anything with op amps! Equally important is the fact that the IC op amp has characteristics that closely approach the assumed ideal. This implies that it is quite easy to design circuits using the IC op amp. Also, op-amp circuits work at performance levels that are quite close to those predicted theoretically. It is for this reason that we are studying op amps at this early stage. It is expected that by the end of this chapter the reader should be able to design nontrivial circuits successfully using op amps.

As already implied, an IC op amp is made up of a large number (tens or more) of transistors, resistors, and (usually) one capacitor connected in a rather complex circuit. Since

we have not yet studied transistor circuits, the circuit inside the op amp will not be discussed in this chapter. Rather, we will treat the op amp as a circuit building block and study its terminal characteristics and its applications. This approach is quite satisfactory in many op-amp applications. Nevertheless, for the more difficult and demanding applications it is quite useful to know what is inside the op-amp package. This topic will be studied in Chapter 12. More advanced applications of op amps will appear in later chapters.

## 2.1 The Ideal Op Amp

### 2.1.1 The Op-Amp Terminals

From a signal point of view the op amp has three terminals: two input terminals and one output terminal. Figure 2.1 shows the symbol we shall use to represent the op amp. Terminals 1 and 2 are input terminals, and terminal 3 is the output terminal. As explained in Section 1.4, amplifiers require dc power to operate. Most IC op amps require two dc power supplies, as shown in Fig. 2.2. Two terminals, 4 and 5, are brought out of the op-amp package and connected to a positive voltage  $V_{CC}$  and a negative voltage  $-V_{EE}$ , respectively. In Fig. 2.2(b) we explicitly show the two dc power supplies as batteries with a common ground. It is interesting to note that the reference grounding point in op-amp circuits is just the common terminal of the two power supplies; that is, no terminal of the op-amp package is physically connected to ground. In what follows we will not, for simplicity, explicitly show the op-amp power supplies.

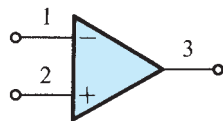


Figure 2.1 Circuit symbol for the op amp.

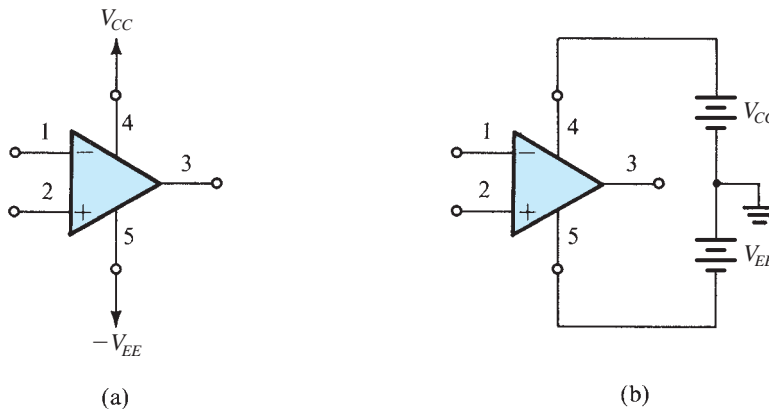


Figure 2.2 The op amp shown connected to dc power supplies.

In addition to the three signal terminals and the two power-supply terminals, an op amp may have other terminals for specific purposes. These other terminals can include terminals for frequency compensation and terminals for offset nulling; both functions will be explained in later sections.

### EXERCISE

**2.1** What is the minimum number of terminals required by a single op amp? What is the minimum number of terminals required on an integrated-circuit package containing four op amps (called a quad op amp)?

**Ans.** 5; 14

## 2.1.2 Function and Characteristics of the Ideal Op Amp

We now consider the circuit function of the op amp. The op amp is designed to sense the difference between the voltage signals applied at its two input terminals (i.e., the quantity  $v_2 - v_1$ ), multiply this by a number  $A$ , and cause the resulting voltage  $A(v_2 - v_1)$  to appear at output terminal 3. Thus  $v_3 = A(v_2 - v_1)$ . Here it should be emphasized that when we talk about the voltage at a terminal we mean the voltage between that terminal and ground; thus  $v_1$  means the voltage applied between terminal 1 and ground.

The ideal op amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current into terminal 2 are both zero. In other words, *the input impedance of an ideal op amp is supposed to be infinite*.

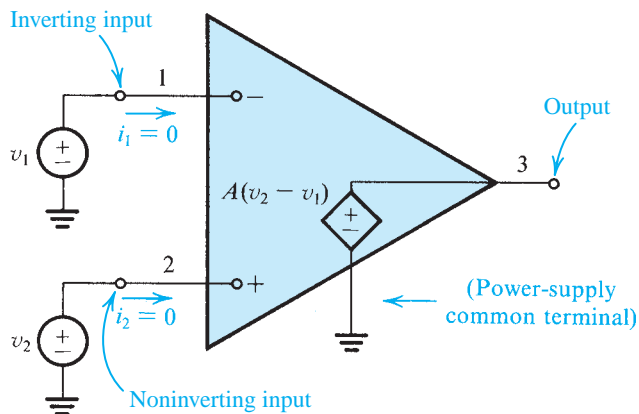
How about the output terminal 3? This terminal is supposed to act as the output terminal of an ideal voltage source. That is, the voltage between terminal 3 and ground will always be equal to  $A(v_2 - v_1)$ , independent of the current that may be drawn from terminal 3 into a load impedance. In other words, *the output impedance of an ideal op amp is supposed to be zero*.

Putting together all of the above, we arrive at the equivalent circuit model shown in Fig. 2.3. Note that the output is in phase with (has the same sign as)  $v_2$  and is out of phase with (has the opposite sign of)  $v_1$ . For this reason, input terminal 1 is called the **inverting input terminal** and is distinguished by a “−” sign, while input terminal 2 is called the **noninverting input terminal** and is distinguished by a “+” sign.

As can be seen from the above description, the op amp responds only to the *difference* signal  $v_2 - v_1$  and hence ignores any signal *common* to both inputs. That is, if  $v_1 = v_2 = 1$  V, then the output will (ideally) be zero. We call this property **common-mode rejection**, and we conclude that an ideal op amp has zero common-mode gain or, equivalently, infinite common-mode rejection. We will have more to say about this point later. For the time being note that the op amp is a **differential-input, single-ended-output** amplifier, with the latter term referring to the fact that the output appears between terminal 3 and ground.<sup>1</sup>

<sup>1</sup>Some op amps are designed to have differential outputs. This topic will not be discussed in this book. Rather, we confine ourselves here to single-ended-output op amps, which constitute the vast majority of commercially available op amps.





**Figure 2.3** Equivalent circuit of the ideal op amp.

Furthermore, gain  $A$  is called the **differential gain**, for obvious reasons. Perhaps not so obvious is another name that we will attach to  $A$ : the **open-loop gain**. The reason for this name will become obvious later on when we “close the loop” around the op amp and define another gain, the closed-loop gain.

An important characteristic of op amps is that they are **direct-coupled** or **dc amplifiers**, where dc stands for direct-coupled (it could equally well stand for direct current, since a direct-coupled amplifier is one that amplifies signals whose frequency is as low as zero). The fact that op amps are direct-coupled devices will allow us to use them in many important applications. Unfortunately, though, the direct-coupling property can cause some serious practical problems, as will be discussed in a later section.

How about bandwidth? The ideal op amp has a gain  $A$  that remains constant down to zero frequency and up to infinite frequency. That is, ideal op amps will amplify signals of any frequency with equal gain, and are thus said to have *infinite bandwidth*.

We have discussed all of the properties of the ideal op amp except for one, which in fact is the most important. This has to do with the value of  $A$ . *The ideal op amp should have a gain  $A$  whose value is very large and ideally infinite.* One may justifiably ask: If the gain  $A$  is infinite, how are we going to use the op amp? The answer is very simple: In almost all applications the op amp will *not* be used alone in a so-called open-loop configuration. Rather, we will use other components to apply feedback to close the loop around the op amp, as will be illustrated in detail in Section 2.2.

For future reference, Table 2.1 lists the characteristics of the ideal op amp.

**Table 2.1** Characteristics of the Ideal Op Amp

1. Infinite input impedance
2. Zero output impedance
3. Zero common-mode gain or, equivalently, infinite common-mode rejection
4. Infinite open-loop gain  $A$
5. Infinite bandwidth

### 2.1.3 Differential and Common-Mode Signals

The differential input signal  $v_{ld}$  is simply the difference between the two input signals  $v_1$  and  $v_2$ ; that is,

$$v_{ld} = v_2 - v_1 \quad (2.1) \quad \text{!}$$

The common-mode input signal  $v_{lcm}$  is the average of the two input signals  $v_1$  and  $v_2$ ; namely,

$$v_{lcm} = \frac{1}{2}(v_1 + v_2) \quad (2.2) \quad \text{!}$$

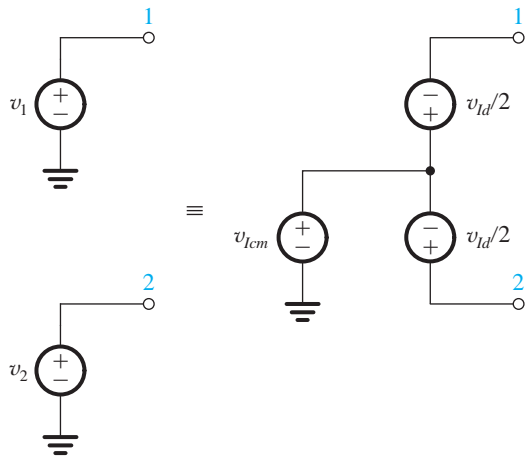
Equations (2.1) and (2.2) can be used to express the input signals  $v_1$  and  $v_2$  in terms of their differential and common-mode components as follows:

$$v_1 = v_{lcm} - v_{ld}/2 \quad (2.3)$$

and

$$v_2 = v_{lcm} + v_{ld}/2 \quad (2.4)$$

These equations can in turn lead to the pictorial representation in Fig. 2.4.



**Figure 2.4** Representation of the signal sources  $v_1$  and  $v_2$  in terms of their differential and common-mode components.

## EXERCISES

**2.2** Consider an op amp that is ideal except that its open-loop gain  $A = 10^3$ . The op amp is used in a feedback circuit, and the voltages appearing at two of its three signal terminals are measured. In each of the following cases, use the measured values to find the expected value of the voltage at the third terminal. Also give the differential and common-mode input signals in each case. (a)  $v_2 = 0$  V and  $v_3 = 2$  V; (b)  $v_2 = +5$  V and  $v_3 = -10$  V; (c)  $v_1 = 1.002$  V and  $v_2 = 0.998$  V; (d)  $v_1 = -3.6$  V and  $v_3 = -3.6$  V.

**Ans.** (a)  $v_1 = -0.002$  V,  $v_{ld} = 2$  mV,  $v_{lcm} = -1$  mV; (b)  $v_1 = +5.01$  V,  $v_{ld} = -10$  mV,  $v_{lcm} = 5.005 \approx 5$  V; (c)  $v_3 = -4$  V,  $v_{ld} = -4$  mV,  $v_{lcm} = 1$  V; (d)  $v_2 = -3.6036$  V,  $v_{ld} = -3.6$  mV,  $v_{lcm} \approx -3.6$  V

**2.3** The internal circuit of a particular op amp can be modeled by the circuit shown in Fig. E2.3. Express  $v_3$  as a function of  $v_1$  and  $v_2$ . For the case  $G_m = 10 \text{ mA/V}$ ,  $R = 10 \text{ k}\Omega$ , and  $\mu = 100$ , find the value of the open-loop gain  $A$ .

**Ans.**  $v_3 = \mu G_m R (v_2 - v_1)$ ;  $A = 10,000 \text{ V/V}$  or  $80 \text{ dB}$

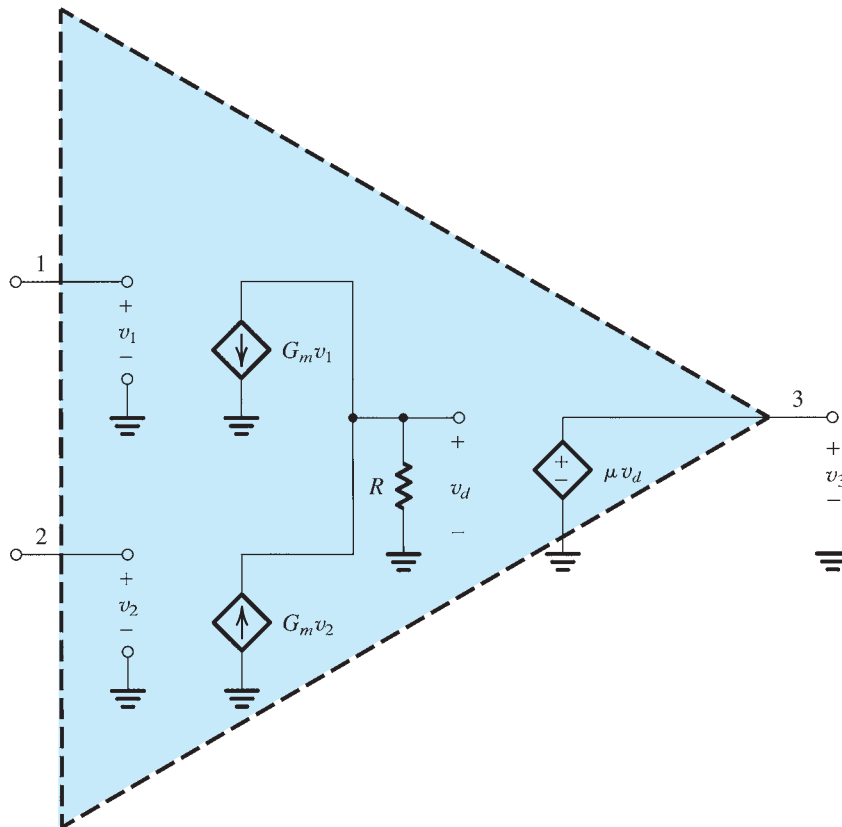
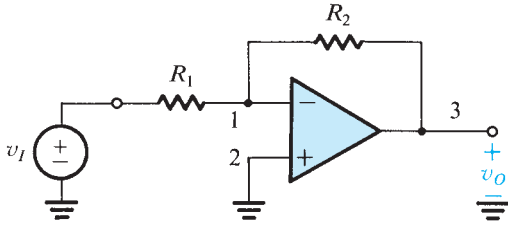


Figure E2.3

## 2.2 The Inverting Configuration

As mentioned above, op amps are not used alone; rather, the op amp is connected to passive components in a feedback circuit. There are two such basic circuit configurations employing an op amp and two resistors: the inverting configuration, which is studied in this section, and the noninverting configuration, which we shall study in the next section.

Figure 2.5 shows the inverting configuration. It consists of one op amp and two resistors  $R_1$  and  $R_2$ . Resistor  $R_2$  is connected from the output terminal of the op amp, terminal 3, *back* to the *inverting* or *negative* input terminal, terminal 1. We speak of  $R_2$  as applying **negative feedback**; if  $R_2$  were connected between terminals 3 and 2 we would have called this **positive feedback**. Note also that  $R_2$  *closes the loop* around the op amp. In addition to adding  $R_2$ , we have grounded terminal 2 and connected a resistor  $R_1$  between terminal 1 and an input signal source with a voltage  $v_i$ . The output of the overall circuit is taken at terminal 3 (i.e., between terminal 3 and



**Figure 2.5** The inverting closed-loop configuration.

ground). Terminal 3 is, of course, a convenient point from which to take the output, since the impedance level there is ideally zero. Thus the voltage  $v_o$  will not depend on the value of the current that might be supplied to a load impedance connected between terminal 3 and ground.

### 2.2.1 The Closed-Loop Gain

We now wish to analyze the circuit in Fig. 2.5 to determine the **closed-loop gain**  $G$ , defined as

$$G \equiv \frac{v_o}{v_I}$$

We will do so assuming the op amp to be ideal. Figure 2.6(a) shows the equivalent circuit, and the analysis proceeds as follows: The gain  $A$  is very large (ideally infinite). If we assume that the circuit is “working” and producing a finite output voltage at terminal 3, then the voltage between the op-amp input terminals should be negligibly small and ideally zero. Specifically, if we call the output voltage  $v_o$ , then, by definition,

$$v_2 - v_1 = \frac{v_o}{A} = 0$$

It follows that the voltage at the inverting input terminal ( $v_1$ ) is given by  $v_1 = v_2$ . That is, because the gain  $A$  approaches infinity, the voltage  $v_1$  approaches and ideally equals  $v_2$ . We speak of this as the two input terminals “tracking each other in potential.” We also speak of a “virtual short circuit” that exists between the two input terminals. Here the word *virtual* should be emphasized, and one should *not* make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A **virtual short circuit** means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain  $A$ . But terminal 2 happens to be connected to ground; thus  $v_2 = 0$  and  $v_1 = 0$ . We speak of terminal 1 as being a **virtual ground**—that is, having zero voltage but not physically connected to ground.

Now that we have determined  $v_1$  we are in a position to apply Ohm’s law and find the current  $i_1$  through  $R_1$  (see Fig. 2.6) as follows:

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

Where will this current go? It cannot go into the op amp, since the ideal op amp has an infinite input impedance and hence draws zero current. It follows that  $i_1$  will have to flow through  $R_2$  to the low-impedance terminal 3. We can then apply Ohm’s law to  $R_2$  and determine  $v_o$ ; that is,

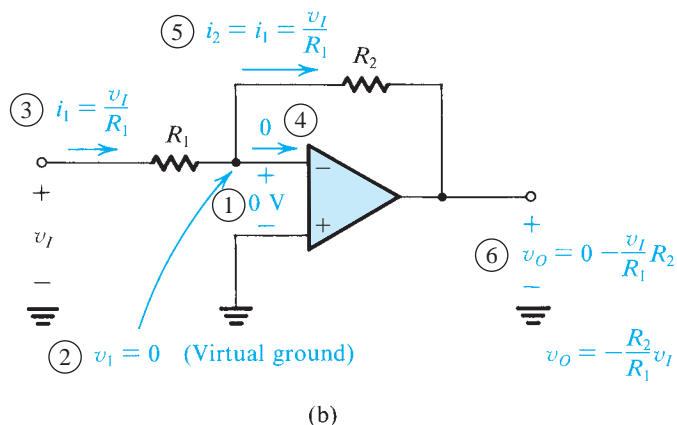
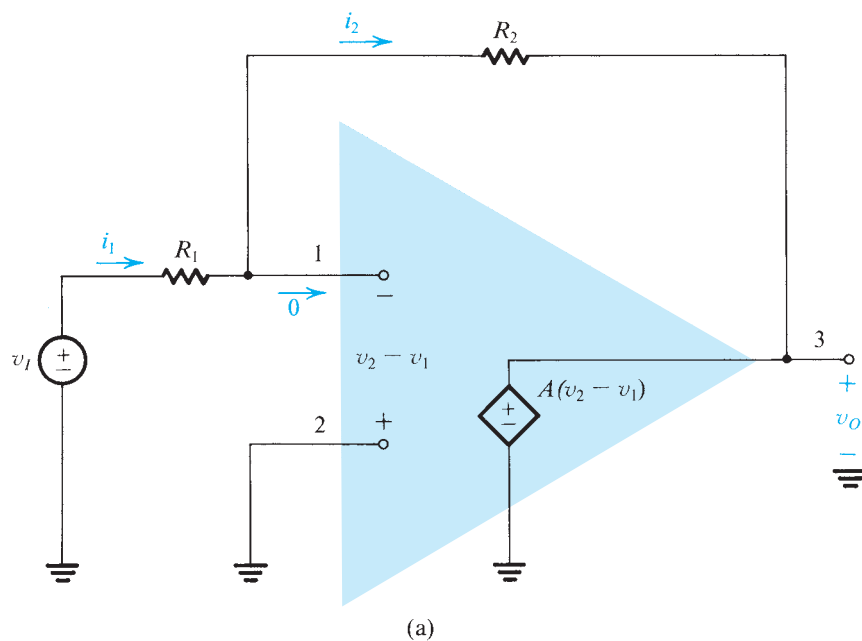
$$\begin{aligned} v_o &= v_1 - i_1 R_2 \\ &= 0 - \frac{v_I}{R_1} R_2 \end{aligned}$$

Thus,

$$\frac{v_o}{v_I} = -\frac{R_2}{R_1}$$







**Figure 2.6** Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.

which is the required closed-loop gain. Figure 2.6(b) illustrates these steps and indicates by the circled numbers the order in which the analysis is performed.

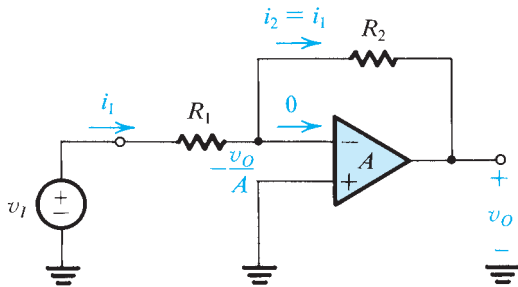
We thus see that the closed-loop gain is simply the ratio of the two resistances  $R_2$  and  $R_1$ . The minus sign means that the closed-loop amplifier provides signal inversion. Thus if  $R_2/R_1 = 10$  and we apply at the input ( $v_I$ ) a sine-wave signal of 1 V peak-to-peak, then the output  $v_O$  will be a sine wave of 10 V peak-to-peak and phase-shifted  $180^\circ$  with respect to the input sine wave. Because of the minus sign associated with the closed-loop gain, this configuration is called the **inverting configuration**.

The fact that the closed-loop gain depends entirely on external passive components (resistors  $R_1$  and  $R_2$ ) is very significant. It means that we can make the closed-loop gain as accurate as we want by selecting passive components of appropriate accuracy. It also means that the closed-loop gain is (ideally) independent of the op-amp gain. This is a dramatic illustration of negative feedback: We started out with an amplifier having very large gain  $A$ , and through applying negative feedback we have obtained a closed-loop gain  $R_2/R_1$  that is much smaller than  $A$  but is stable and predictable. That is, we are trading gain for accuracy.

### 2.2.2 Effect of Finite Open-Loop Gain

The points just made are more clearly illustrated by deriving an expression for the closed-loop gain under the assumption that the op-amp open-loop gain  $A$  is finite. Figure 2.7 shows the analysis. If we denote the output voltage  $v_o$ , then the voltage between the two input terminals of the op amp will be  $v_o/A$ . Since the positive input terminal is grounded, the voltage at the negative input terminal must be  $-v_o/A$ . The current  $i_1$  through  $R_1$  can now be found from

$$i_1 = \frac{v_I - (-v_o/A)}{R_1} = \frac{v_I + v_o/A}{R_1}$$



**Figure 2.7** Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.

The infinite input impedance of the op amp forces the current  $i_1$  to flow entirely through  $R_2$ . The output voltage  $v_o$  can thus be determined from

$$\begin{aligned} v_o &= -\frac{v_o}{A} - i_1 R_2 \\ &= -\frac{v_o}{A} - \left( \frac{v_I + v_o/A}{R_1} \right) R_2 \end{aligned}$$

Collecting terms, the closed-loop gain  $G$  is found as

$$G \equiv \frac{v_o}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.5)$$

We note that as  $A$  approaches  $\infty$ ,  $G$  approaches the ideal value of  $-R_2/R_1$ . Also, from Fig. 2.7 we see that as  $A$  approaches  $\infty$ , the voltage at the inverting input terminal approaches zero. This is the virtual-ground assumption we used in our earlier analysis when the op amp was

assumed to be ideal. Finally, note that Eq. (2.5) in fact indicates that to minimize the dependence of the closed-loop gain  $G$  on the value of the open-loop gain  $A$ , we should make

$$1 + \frac{R_2}{R_1} \ll A$$

### Example 2.1

Consider the inverting configuration with  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$ .

- Find the closed-loop gain for the cases  $A = 10^3$ ,  $10^4$ , and  $10^5$ . In each case determine the percentage error in the magnitude of  $G$  relative to the ideal value of  $R_2/R_1$  (obtained with  $A = \infty$ ). Also determine the voltage  $v_i$  that appears at the inverting input terminal when  $v_i = 0.1 \text{ V}$ .
- If the open-loop gain  $A$  changes from 100,000 to 50,000 (i.e., drops by 50%), what is the corresponding percentage change in the magnitude of the closed-loop gain  $G$ ?

#### Solution

- Substituting the given values in Eq. (2.5), we obtain the values given in the following table, where the percentage error  $\varepsilon$  is defined as

$$\varepsilon \equiv \frac{|G| - (R_2/R_1)}{(R_2/R_1)} \times 100$$

The values of  $v_i$  are obtained from  $v_i = -v_o/A = Gv_i/A$  with  $v_i = 0.1 \text{ V}$ .

$A$	$ G $	$\varepsilon$	$v_i$
$10^3$	90.83	-9.17%	-9.08 mV
$10^4$	99.00	-1.00%	-0.99 mV
$10^5$	99.90	-0.10%	-0.10 mV

- Using Eq. (2.5), we find that for  $A = 50,000$ ,  $|G| = 99.80$ . Thus a -50% change in the open-loop gain results in a change of only -0.1% in the closed-loop gain!

### 2.2.3 Input and Output Resistances

Assuming an ideal op amp with infinite open-loop gain, the input resistance of the closed-loop inverting amplifier of Fig. 2.5 is simply equal to  $R_1$ . This can be seen from Fig. 2.6(b), where



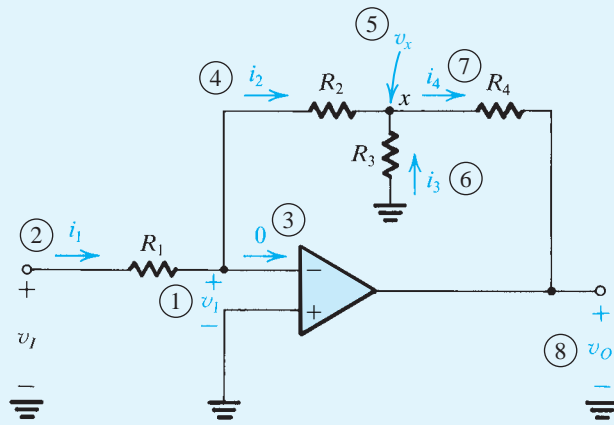
$$R_i \equiv \frac{v_i}{i_1} = \frac{v_i}{v_i/R_1} = R_1$$

Now recall that in Section 1.5 we learned that the amplifier input resistance forms a voltage divider with the resistance of the source that feeds the amplifier. Thus, to avoid the loss of signal strength, voltage amplifiers are required to have high input resistance. In the case of the inverting op-amp configuration we are studying, to make  $R_i$  high we should select a high value for  $R_1$ . However, if the required gain  $R_2/R_1$  is also high, then  $R_2$  could become impractically large (e.g., greater than a few megohms). We may conclude that the inverting configuration suffers from a low input resistance. A solution to this problem is discussed in Example 2.2 below.

Since the output of the inverting configuration is taken at the terminals of the ideal voltage source  $A(v_2 - v_1)$  (see Fig. 2.6a), it follows that the output resistance of the closed-loop amplifier is zero.

### Example 2.2

Assuming the op amp to be ideal, derive an expression for the closed-loop gain  $v_O/v_I$  of the circuit shown in Fig. 2.8. Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of 1 M $\Omega$ . Assume that for practical reasons it is required not to use resistors greater than 1 M $\Omega$ . Compare your design with that based on the inverting configuration of Fig. 2.5.



**Figure 2.8** Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

### Solution

The analysis begins at the inverting input terminal of the op amp, where the voltage is

$$v_1 = \frac{-v_O}{A} = \frac{-v_O}{\infty} = 0$$

Here we have assumed that the circuit is “working” and producing a finite output voltage  $v_O$ . Knowing  $v_1$ , we can determine the current  $i_1$  as follows:

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

Since zero current flows into the inverting input terminal, all of  $i_1$  will flow through  $R_2$ , and thus

$$i_2 = i_1 = \frac{v_I}{R_1}$$

Now we can determine the voltage at node  $x$ :

$$v_x = v_1 - i_2 R_2 = 0 - \frac{v_I}{R_1} R_2 = -\frac{R_2}{R_1} v_I$$

**Example 2.2** *continued*

This in turn enables us to find the current  $i_3$ :

$$i_3 = \frac{0 - v_x}{R_3} = \frac{R_2}{R_1 R_3} v_I$$

Next, a node equation at  $x$  yields  $i_4$ :

$$i_4 = i_2 + i_3 = \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I$$

Finally, we can determine  $v_o$  from

$$\begin{aligned} v_o &= v_x - i_4 R_4 \\ &= -\frac{R_2}{R_1} v_I - \left( \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I \right) R_4 \end{aligned}$$

Thus the voltage gain is given by

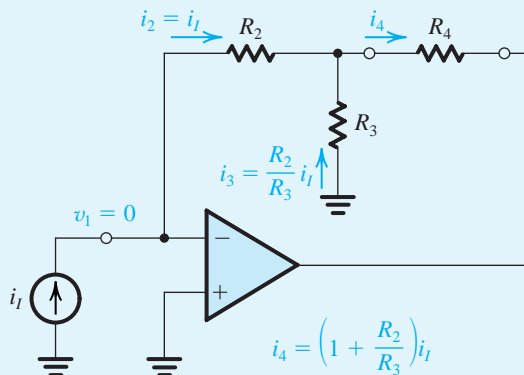
$$\frac{v_o}{v_I} = - \left[ \frac{R_2}{R_1} + \frac{R_4}{R_1} \left( 1 + \frac{R_2}{R_3} \right) \right]$$

which can be written in the form

$$\frac{v_o}{v_I} = - \frac{R_2}{R_1} \left( 1 + \frac{R_4}{R_2} + \frac{R_4}{R_3} \right)$$

Now, since an input resistance of  $1 \text{ M}\Omega$  is required, we select  $R_1 = 1 \text{ M}\Omega$ . Then, with the limitation of using resistors no greater than  $1 \text{ M}\Omega$ , the maximum value possible for the first factor in the gain expression is 1 and is obtained by selecting  $R_2 = 1 \text{ M}\Omega$ . To obtain a gain of  $-100$ ,  $R_3$  and  $R_4$  must be selected so that the second factor in the gain expression is 100. If we select the maximum allowed (in this example) value of  $1 \text{ M}\Omega$  for  $R_4$ , then the required value of  $R_3$  can be calculated to be  $10.2 \text{ k}\Omega$ . Thus this circuit utilizes three  $1\text{-M}\Omega$  resistors and a  $10.2\text{-k}\Omega$  resistor. In comparison, if the inverting configuration were used with  $R_1 = 1 \text{ M}\Omega$  we would have required a feedback resistor of  $100 \text{ M}\Omega$ , an impractically large value!

Before leaving this example it is insightful to inquire into the mechanism by which the circuit is able to realize a large voltage gain without using large resistances in the feedback path. Toward that end, observe that because of the virtual ground at the inverting input terminal of the op amp,  $R_2$  and  $R_3$  are in effect in parallel. Thus, by making  $R_3$  lower than  $R_2$  by, say, a factor  $k$  (i.e., where  $k > 1$ ),  $R_3$  is forced to carry a current  $k$ -times that in  $R_2$ . Thus, while  $i_2 = i_1$ ,  $i_3 = k i_1$  and  $i_4 = (k + 1) i_1$ . It is the current multiplication by a factor of  $(k + 1)$  that enables a large voltage drop to develop across  $R_4$  and hence a large  $v_o$  without using a large value for  $R_4$ . Notice also that the current through  $R_4$  is independent of the value of  $R_4$ . It follows that the circuit can be used as a current amplifier as shown in Fig. 2.9.



**Figure 2.9** A current amplifier based on the circuit of Fig. 2.8. The amplifier delivers its output current to  $R_4$ . It has a current gain of  $(1 + R_2/R_3)$ , a zero input resistance, and an infinite output resistance. The load ( $R_4$ ), however, must be floating (i.e., neither of its two terminals can be connected to ground).

## EXERCISES

**D2.4** Use the circuit of Fig. 2.5 to design an inverting amplifier having a gain of  $-10$  and an input resistance of  $100\text{ k}\Omega$ . Give the values of  $R_1$  and  $R_2$ .

**Ans.**  $R_1 = 100\text{ k}\Omega$ ;  $R_2 = 1\text{ M}\Omega$

**2.5** The circuit shown in Fig. E2.5(a) can be used to implement a transresistance amplifier (see Table 1.1 in Section 1.5). Find the value of the input resistance  $R_i$ , the transresistance  $R_m$ , and the output resistance  $R_o$  of the transresistance amplifier. If the signal source shown in Fig. E2.5(b) is connected to the input of the transresistance amplifier, find its output voltage.

**Ans.**  $R_i = 0$ ;  $R_m = -10\text{ k}\Omega$ ;  $R_o = 0$ ;  $v_o = -5\text{ V}$

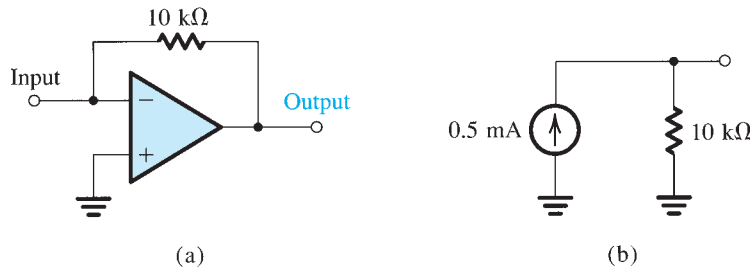


Figure E2.5

**2.6** For the circuit in Fig. E2.6 determine the values of  $v_1$ ,  $i_1$ ,  $i_2$ ,  $v_o$ ,  $i_L$ , and  $i_o$ . Also determine the voltage gain  $v_o/v_1$ , current gain  $i_L/i_1$ , and power gain  $P_o/P_I$ .

**Ans.**  $0\text{ V}$ ;  $1\text{ mA}$ ;  $1\text{ mA}$ ;  $-10\text{ V}$ ;  $-10\text{ mA}$ ;  $-11\text{ mA}$ ;  $-10\text{ V/V}$  (20 dB),  $-10\text{ A/A}$  (20 dB);  $100\text{ W/W}$  (20 dB)

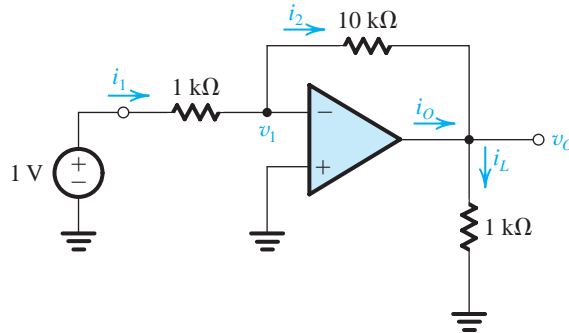


Figure E2.6

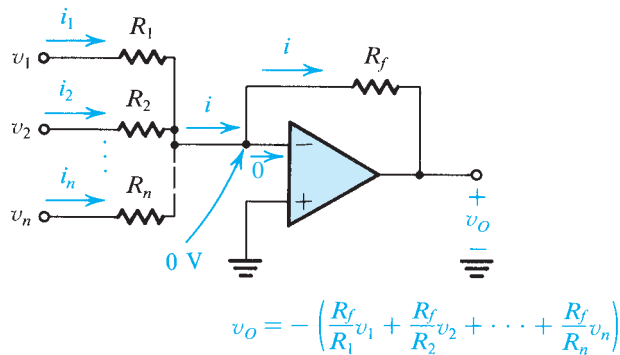
### 2.2.4 An Important Application—The Weighted Summer

A very important application of the inverting configuration is the weighted-summer circuit shown in Fig. 2.10. Here we have a resistance  $R_f$  in the negative-feedback path (as before); but we have a number of input signals  $v_1, v_2, \dots, v_n$  each applied to a corresponding resistor  $R_1, R_2, \dots, R_n$ , which are connected to the inverting terminal of the op amp. From our previous discussion, the ideal op amp will have a virtual ground appearing



at its negative input terminal. Ohm's law then tells us that the currents  $i_1, i_2, \dots, i_n$  are given by

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_2}{R_2}, \quad \dots, \quad i_n = \frac{v_n}{R_n}$$



**Figure 2.10** A weighted summer.

All these currents sum together to produce the current  $i$ ; that is,

$$i = i_1 + i_2 + \dots + i_n \quad (2.6)$$

will be forced to flow through  $R_f$  (since no current flows into the input terminals of an ideal op amp). The output voltage  $v_O$  may now be determined by another application of Ohm's law,

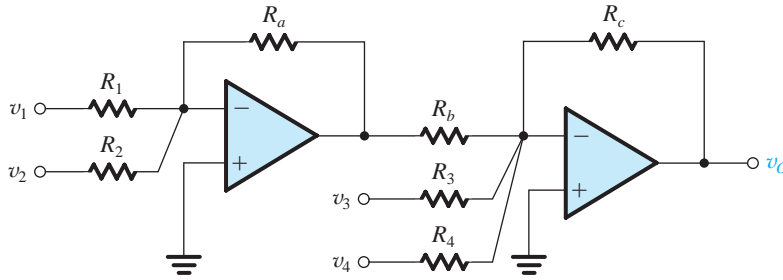
$$v_O = 0 - iR_f = -iR_f$$

Thus,

$$v_O = - \left( \frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \dots + \frac{R_f}{R_n} v_n \right) \quad (2.7)$$

That is, the output voltage is a weighted sum of the input signals  $v_1, v_2, \dots, v_n$ . This circuit is therefore called a **weighted summer**. Note that each summing coefficient may be independently adjusted by adjusting the corresponding “feed-in” resistor ( $R_1$  to  $R_n$ ). This nice property, which greatly simplifies circuit adjustment, is a direct consequence of the virtual ground that exists at the inverting op-amp terminal. As the reader will soon come to appreciate, virtual grounds are extremely “handy.” In the weighted summer of Fig. 2.10 all the summing coefficients must be of the same sign. The need occasionally arises for summing signals with opposite signs. Such a function can be implemented, however, using two op amps as shown in Fig. 2.11. Assuming ideal op amps, it can be easily shown that the output voltage is given by

$$v_O = v_1 \left( \frac{R_a}{R_1} \right) \left( \frac{R_c}{R_b} \right) + v_2 \left( \frac{R_a}{R_2} \right) \left( \frac{R_c}{R_b} \right) - v_3 \left( \frac{R_c}{R_3} \right) - v_4 \left( \frac{R_c}{R_4} \right) \quad (2.8)$$



**Figure 2.11** A weighted summer capable of implementing summing coefficients of both signs.

## EXERCISES

**D2.7** Design an inverting op-amp circuit to form the weighted sum  $v_o$  of two inputs  $v_1$  and  $v_2$ . It is required that  $v_o = -(v_1 + 5v_2)$ . Choose values for  $R_1$ ,  $R_2$ , and  $R_f$  so that for a maximum output voltage of 10 V the current in the feedback resistor will not exceed 1 mA.

**Ans.** A possible choice:  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ , and  $R_f = 10 \text{ k}\Omega$

**D2.8** Use the idea presented in Fig. 2.11 to design a weighted summer that provides

$$v_o = 2v_1 + v_2 - 4v_3$$

**Ans.** A possible choice:  $R_1 = 5 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_a = 10 \text{ k}\Omega$ ,  $R_b = 10 \text{ k}\Omega$ ,  $R_3 = 2.5 \text{ k}\Omega$ ,  $R_c = 10 \text{ k}\Omega$ .

## 2.3 The Noninverting Configuration

The second closed-loop configuration we shall study is shown in Fig. 2.12. Here the input signal  $v_i$  is applied directly to the positive input terminal of the op amp while one terminal of  $R_1$  is connected to ground.

### 2.3.1 The Closed-Loop Gain

Analysis of the noninverting circuit to determine its closed-loop gain ( $v_o/v_i$ ) is illustrated in Fig. 2.13. Again the order of the steps in the analysis is indicated by circled numbers. Assuming that the op amp is ideal with infinite gain, a virtual short circuit exists between its two input terminals. Hence the difference input signal is

$$v_{Id} = \frac{v_o}{A} = 0 \quad \text{for } A = \infty$$

Thus the voltage at the inverting input terminal will be equal to that at the noninverting input terminal, which is the applied voltage  $v_i$ . The current through  $R_1$  can then be determined as  $v_i/R_1$ . Because of the infinite input impedance of the op amp, this current will flow through  $R_2$ , as shown in Fig. 2.13. Now the output voltage can be determined from

$$v_o = v_i + \left(\frac{v_i}{R_1}\right)R_2$$

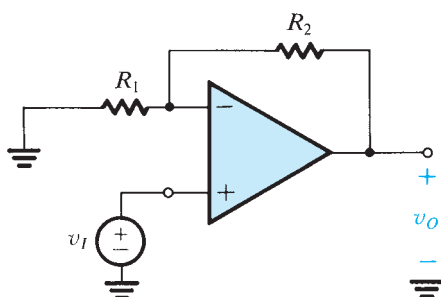


Figure 2.12 The noninverting configuration.

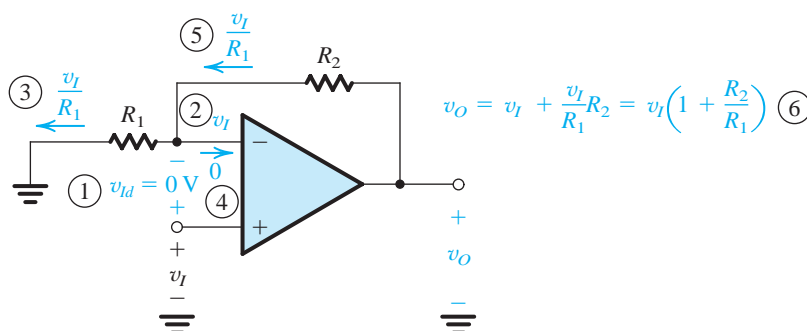


Figure 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

which yields

1

$$\frac{v_O}{v_I} = 1 + \frac{R_2}{R_1} \quad (2.9)$$

Further insight into the operation of the noninverting configuration can be obtained by considering the following: Since the current into the op-amp inverting input is zero, the circuit composed of  $R_1$  and  $R_2$  acts in effect as a voltage divider feeding a fraction of the output voltage back to the inverting input terminal of the op amp; that is,

$$v_1 = v_O \left( \frac{R_1}{R_1 + R_2} \right) \quad (2.10)$$

Then the infinite op-amp gain and the resulting virtual short circuit between the two input terminals of the op amp forces this voltage to be equal to that applied at the positive input terminal; thus,

$$v_O \left( \frac{R_1}{R_1 + R_2} \right) = v_I$$

which yields the gain expression given in Eq. (2.9).

This is an appropriate point to reflect further on the action of the negative feedback present in the noninverting circuit of Fig. 2.12. Let  $v_I$  increase. Such a change in  $v_I$  will cause  $v_{id}$  to increase, and  $v_O$  will correspondingly increase as a result of the high (ideally infinite) gain of the op amp. However, a fraction of the increase in  $v_O$  will be fed back to the inverting input terminal of the op amp through the  $(R_1, R_2)$  voltage divider. The result of this feedback will be to counteract the increase in  $v_{id}$ , driving  $v_{id}$  back to zero, albeit at a higher value of  $v_O$  that corresponds to the increased value of  $v_I$ . This *degenerative* action of negative feedback gives it the alternative name **degenerative feedback**. Finally, note that the argument above applies equally well if  $v_I$  decreases. A formal and detailed study of feedback is presented in Chapter 10.

### 2.3.2 Effect of Finite Open-Loop Gain

As we have done for the inverting configuration, we now consider the effect of the finite op-amp open-loop gain  $A$  on the gain of the noninverting configuration. Assuming the op amp to be ideal except for having a finite open-loop gain  $A$ , it can be shown that the closed-loop gain of the noninverting amplifier circuit of Fig. 2.12 is given by

$$G \equiv \frac{v_o}{v_i} = \frac{1 + (R_2/R_1)}{1 + \frac{1 + (R_2/R_1)}{A}} \quad (2.11)$$

Observe that the denominator is identical to that for the case of the inverting configuration (Eq. 2.5). This is no coincidence; it is a result of the fact that both the inverting and the noninverting configurations have the same feedback loop, which can be readily seen if the input signal source is eliminated (i.e., short-circuited). The numerators, however, are different, for the numerator gives the ideal or nominal closed-loop gain ( $-R_2/R_1$  for the inverting configuration, and  $1 + R_2/R_1$  for the noninverting configuration). Finally, we note (with reassurance) that the gain expression in Eq. (2.11) reduces to the ideal value for  $A = \infty$ . In fact, it approximates the ideal value for

$$A \gg 1 + \frac{R_2}{R_1}$$

This is the same condition as in the inverting configuration, except that here the quantity on the right-hand side is the nominal closed-loop gain. The expressions for the actual and ideal values of the closed-loop gain  $G$  in Eqs. (2.11) and (2.9), respectively, can be used to determine the percentage error in  $G$  resulting from the finite op-amp gain  $A$  as

$$\text{Percent gain error} = -\frac{1 + (R_2/R_1)}{A + 1 + (R_2/R_1)} \times 100 \quad (2.12)$$

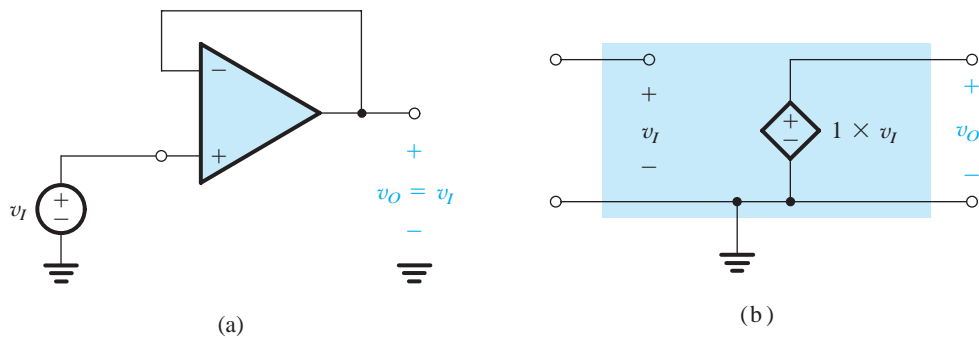
Thus, as an example, if an op amp with an open-loop gain of 1000 is used to design a noninverting amplifier with a nominal closed-loop gain of 10, we would expect the closed-loop gain to be about 1% below the nominal value.

### 2.3.3 Input and Output Resistance

The gain of the noninverting configuration is positive—hence the name *noninverting*. The input impedance of this closed-loop amplifier is ideally infinite, since no current flows into the positive input terminal of the op amp. The output of the noninverting amplifier is taken at the terminals of the ideal voltage source  $A(v_2 - v_1)$  (see the op-amp equivalent circuit in Fig. 2.3), thus the output resistance of the noninverting configuration is zero.

### 2.3.4 The Voltage Follower

The property of high input impedance is a very desirable feature of the noninverting configuration. It enables using this circuit as a buffer amplifier to connect a source with a high impedance to a low-impedance load. We have discussed the need for buffer amplifiers in Section 1.5. In many applications the buffer amplifier is not required to provide any voltage gain; rather, it is used mainly as an impedance transformer or a power amplifier. In such cases we may make  $R_2 = 0$  and  $R_1 = \infty$  to obtain the **unity-gain amplifier** shown in Fig. 2.14(a). This circuit is commonly referred to as a **voltage follower**, since the output “follows” the input. In the ideal case,  $v_o = v_i$ ,  $R_{in} = \infty$ ,  $R_{out} = 0$ , and the follower has the equivalent circuit shown in Fig. 2.14(b).



**Figure 2.14** (a) The unity-gain buffer or follower amplifier. (b) Its equivalent circuit model.

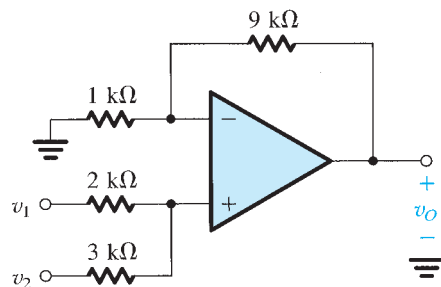
Since in the voltage-follower circuit the entire output is fed back to the inverting input, the circuit is said to have 100% negative feedback. The infinite gain of the op amp then acts to make  $v_{id} = 0$  and hence  $v_O = v_I$ . Observe that the circuit is elegant in its simplicity!

Since the noninverting configuration has a gain greater than or equal to unity, depending on the choice of  $R_2/R_1$ , some prefer to call it “a follower with gain.”

## EXERCISES

**2.9** Use the superposition principle to find the output voltage of the circuit shown in Fig. E2.9.

**Ans.**  $v_O = 6v_1 + 4v_2$



**Figure E2.9**

**2.10** If in the circuit of Fig. E2.9 the 1-kΩ resistor is disconnected from ground and connected to a third signal source  $v_3$ , use superposition to determine  $v_O$  in terms of  $v_1$ ,  $v_2$ , and  $v_3$ .

**Ans.**  $v_O = 6v_1 + 4v_2 - 9v_3$

**D2.11** Design a noninverting amplifier with a gain of 2. At the maximum output voltage of 10 V the current in the voltage divider is to be 10 μA.

**Ans.**  $R_1 = R_2 = 0.5 \text{ M}\Omega$

**2.12** (a) Show that if the op amp in the circuit of Fig. 2.12 has a finite open-loop gain  $A$ , then the closed-loop gain is given by Eq. (2.11). (b) For  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 9 \text{ k}\Omega$  find the percentage deviation  $\varepsilon$  of the closed-loop gain from the ideal value of  $(1 + R_2/R_1)$  for the cases  $A = 10^3$ ,  $10^4$ , and  $10^5$ . For  $v_I = 1 \text{ V}$ , find in each case the voltage between the two input terminals of the op amp.

**Ans.**  $\varepsilon = -1\%$ ,  $-0.1\%$ ,  $-0.01\%$ ;  $v_2 - v_1 = 9.9 \text{ mV}$ ,  $1 \text{ mV}$ ,  $0.1 \text{ mV}$

**2.13** For the circuit in Fig. E2.13 find the values of  $i_p$ ,  $v_1$ ,  $i_1$ ,  $i_2$ ,  $v_o$ ,  $i_L$ , and  $i_o$ . Also find the voltage gain  $v_o/v_1$ , the current gain  $i_L/i_1$ , and the power gain  $P_L/P_I$ .

**Ans.** 0; 1 V; 1 mA; 1 mA; 10 V; 10 mA; 11 mA; 10 V/V (20 dB);  $\infty$ ;  $\infty$

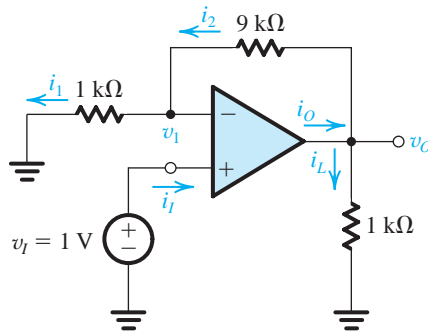


Figure E2.13

**2.14** It is required to connect a transducer having an open-circuit voltage of 1 V and a source resistance of 1 M $\Omega$  to a load of 1-k $\Omega$  resistance. Find the load voltage if the connection is done (a) directly and (b) through a unity-gain voltage follower.

**Ans.** (a) 1 mV; (b) 1 V

## 2.4 Difference Amplifiers

Having studied the two basic configurations of op-amp circuits together with some of their direct applications, we are now ready to consider a somewhat more involved but very important application. Specifically, we shall study the use of op amps to design difference or differential amplifiers.<sup>2</sup> A difference amplifier is one that responds to the difference between the two signals applied at its input and ideally rejects signals that are common to the two inputs. The representation of signals in terms of their differential and common-mode components was given in Fig. 2.4. It is repeated here in Fig. 2.15 with slightly different symbols to serve as the input signals for the difference amplifiers we are about to design. Although ideally the difference amplifier will amplify only the differential input signal  $v_{Id}$  and reject completely the common-mode input signal  $v_{Icm}$ , practical circuits will have an output voltage  $v_o$  given by

$$v_o = A_d v_{Id} + A_{cm} v_{Icm} \quad (2.13)$$

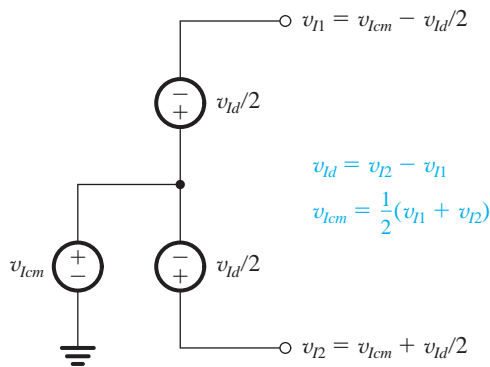
where  $A_d$  denotes the amplifier differential gain and  $A_{cm}$  denotes its common-mode gain (ideally zero). The efficacy of a differential amplifier is measured by the degree of its rejection of common-mode signals in preference to differential signals. This is usually quantified by a measure known as the **common-mode rejection ratio (CMRR)**, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right| \quad (2.14)$$



<sup>2</sup>The terms *difference* and *differential* are usually used to describe somewhat different amplifier types. For our purposes at this point, the distinction is not sufficiently significant. We will be more precise near the end of this section.





**Figure 2.15** Representing the input signals to a differential amplifier in terms of their differential and common-mode components.

The need for difference amplifiers arises frequently in the design of electronic systems, especially those employed in instrumentation. As a common example, consider a transducer providing a small (e.g., 1 mV) signal between its two output terminals while each of the two wires leading from the transducer terminals to the measuring instrument may have a large interference signal (e.g., 1 V) relative to the circuit ground. The instrument front end obviously needs a difference amplifier.

Before we proceed any further we should address a question that the reader might have: The op amp is itself a difference amplifier; why not just use an op amp? The answer is that the very high (ideally infinite) gain of the op amp makes it impossible to use by itself. Rather, as we did before, we have to devise an appropriate feedback network to connect to the op amp to create a circuit whose closed-loop gain is finite, predictable, and stable.

### 2.4.1 A Single-Op-Amp Difference Amplifier

Our first attempt at designing a difference amplifier is motivated by the observation that the gain of the noninverting amplifier configuration is positive,  $(1 + R_2/R_1)$ , while that of the inverting configuration is negative,  $(-R_2/R_1)$ . Combining the two configurations together is then a step in the right direction—namely, getting the difference between two input signals. Of course, we have to make the two gain magnitudes equal in order to reject common-mode signals. This, however, can be easily achieved by attenuating the positive input signal to reduce the gain of the positive path from  $(1 + R_2/R_1)$  to  $(R_2/R_1)$ . The resulting circuit would then look like that shown in Fig. 2.16, where the attenuation in the positive input path is achieved by the voltage divider  $(R_3, R_4)$ . The proper ratio of this voltage divider can be determined from

$$\frac{R_4}{R_4 + R_3} \left( 1 + \frac{R_2}{R_1} \right) = \frac{R_2}{R_1}$$

which can be put in the form

$$\frac{R_4}{R_4 + R_3} = \frac{R_2}{R_2 + R_1}$$

This condition is satisfied by selecting

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \quad (2.15)$$

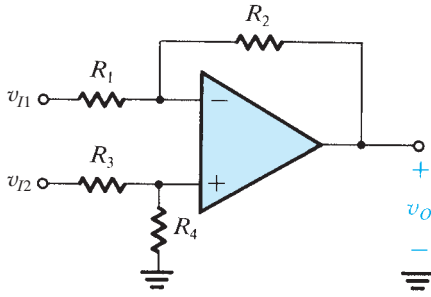


Figure 2.16 A difference amplifier.

This completes our work. However, we have perhaps proceeded a little too fast! Let's step back and verify that the circuit in Fig. 2.16 with  $R_3$  and  $R_4$  selected according to Eq. (2.15) does in fact function as a difference amplifier. Specifically, we wish to determine the output voltage  $v_o$  in terms of  $v_{I1}$  and  $v_{I2}$ . Toward that end, we observe that the circuit is linear, and thus we can use superposition.

To apply superposition, we first reduce  $v_{I2}$  to zero—that is, ground the terminal to which  $v_{I2}$  is applied—and then find the corresponding output voltage, which will be due entirely to  $v_{I1}$ . We denote this output voltage  $v_{O1}$ . Its value may be found from the circuit in Fig. 2.17(a), which we recognize as that of the inverting configuration. The existence of  $R_3$  and  $R_4$  does not affect the gain expression, since no current flows through either of them. Thus,

$$v_{O1} = -\frac{R_2}{R_1} v_{I1}$$

Next, we reduce  $v_{I1}$  to zero and evaluate the corresponding output voltage  $v_{O2}$ . The circuit will now take the form shown in Fig. 2.17(b), which we recognize as the noninverting configuration with an additional voltage divider, made up of  $R_3$  and  $R_4$ , connected to the input  $v_{I2}$ . The output voltage  $v_{O2}$  is therefore given by

$$v_{O2} = v_{I2} \frac{R_4}{R_3 + R_4} \left( 1 + \frac{R_2}{R_1} \right) = \frac{R_2}{R_1} v_{I2}$$

where we have utilized Eq. (2.15).

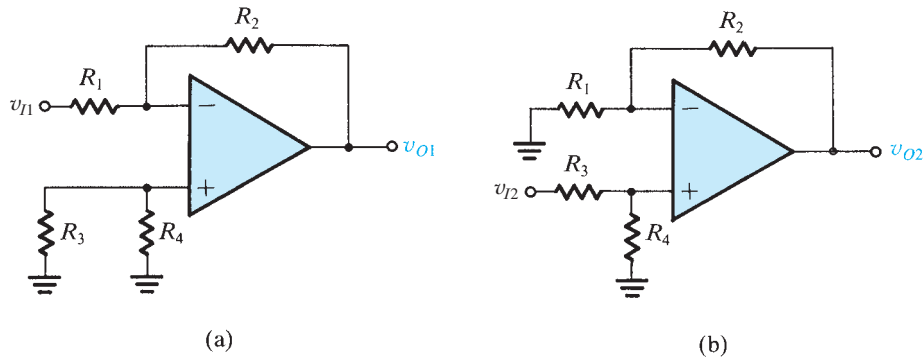
The superposition principle tells us that the output voltage  $v_o$  is equal to the sum of  $v_{O1}$  and  $v_{O2}$ . Thus we have

$$v_o = \frac{R_2}{R_1} (v_{I2} - v_{I1}) = \frac{R_2}{R_1} v_{Id} \quad (2.16) \quad \text{!}$$

Thus, as expected, the circuit acts as a difference amplifier with a differential gain  $A_d$  of

$$A_d = \frac{R_2}{R_1} \quad (2.17) \quad \text{!}$$

Of course this is predicated on the op amp being ideal and furthermore on the selection of  $R_3$  and  $R_4$  so that their ratio matches that of  $R_1$  and  $R_2$  (Eq. 2.15). To make this matching requirement a little easier to satisfy, we usually select



**Figure 2.17** Application of superposition to the analysis of the circuit of Fig. 2.16.

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

Let's next consider the circuit with only a common-mode signal applied at the input, as shown in Fig. 2.18. The figure also shows some of the analysis steps. Thus,

$$\begin{aligned} i_1 &= \frac{1}{R_1} \left[ v_{Icm} - \frac{R_4}{R_4 + R_3} v_{Icm} \right] \\ &= v_{Icm} \frac{R_3}{R_4 + R_3} \frac{1}{R_1} \end{aligned} \quad (2.18)$$

The output voltage can now be found from

$$v_O = \frac{R_4}{R_4 + R_3} v_{Icm} - i_2 R_2$$

Substituting  $i_2 = i_1$  and for  $i_1$  from Eq. (2.18),

$$\begin{aligned} v_O &= \frac{R_4}{R_4 + R_3} v_{Icm} - \frac{R_2}{R_1} \frac{R_3}{R_4 + R_3} v_{Icm} \\ &= \frac{R_4}{R_4 + R_3} \left( 1 - \frac{R_2}{R_1} \frac{R_3}{R_4} \right) v_{Icm} \end{aligned}$$

Thus,

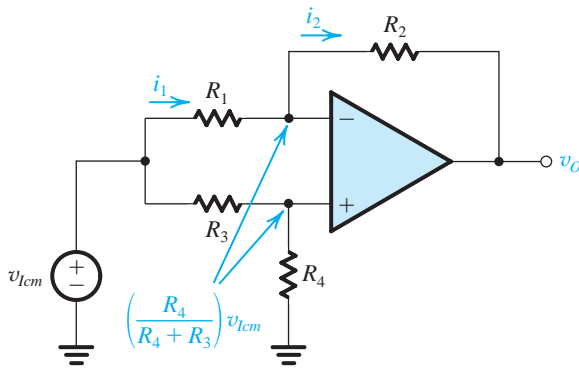
$$A_{cm} \equiv \frac{v_O}{v_{Icm}} = \left( \frac{R_4}{R_4 + R_3} \right) \left( 1 - \frac{R_2}{R_1} \frac{R_3}{R_4} \right) \quad (2.19)$$

For the design with the resistor ratios selected according to Eq. (2.15), we obtain

$$A_{cm} = 0$$

as expected. Note, however, that any mismatch in the resistance ratios can make  $A_{cm}$  nonzero, and hence CMRR finite.

In addition to rejecting common-mode signals, a difference amplifier is usually required to have a high input resistance. To find the input resistance between the two input terminals



**Figure 2.18** Analysis of the difference amplifier to determine its common-mode gain  $A_{cm} \equiv v_O / v_{Icm}$ .

(i.e., the resistance seen by  $v_{Id}$ ), called the **differential input resistance**  $R_{id}$ , consider Fig. 2.19. Here we have assumed that the resistors are selected so that

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

Now

$$R_{id} \equiv \frac{v_{Id}}{i_I}$$

Since the two input terminals of the op amp track each other in potential, we may write a loop equation and obtain

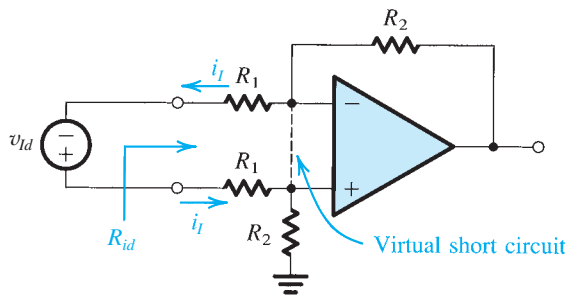
$$v_{Id} = R_1 i_I + 0 + R_1 i_I$$

Thus,

$$R_{id} = 2R_1 \quad (2.20)$$



Note that if the amplifier is required to have a large differential gain ( $R_2/R_1$ ), then  $R_1$  of necessity will be relatively small and the input resistance will be correspondingly low, a drawback of this circuit. Another drawback of the circuit is that it is not easy to vary the differential gain of the amplifier. Both of these drawbacks are overcome in the instrumentation amplifier discussed next.



**Figure 2.19** Finding the input resistance of the difference amplifier for the case  $R_3 = R_1$  and  $R_4 = R_2$ .

## EXERCISES

**2.15** Consider the difference-amplifier circuit of Fig. 2.16 for the case  $R_1 = R_3 = 2 \text{ k}\Omega$  and  $R_2 = R_4 = 200 \text{ k}\Omega$ . (a) Find the value of the differential gain  $A_d$ . (b) Find the value of the differential input resistance  $R_{id}$  and the output resistance  $R_o$ . (c) If the resistors have 1% tolerance (i.e., each can be within  $\pm 1\%$  of its nominal value), use Eq. (2.19) to find the worst-case common-mode gain  $A_{cm}$  and hence the corresponding value of CMRR.

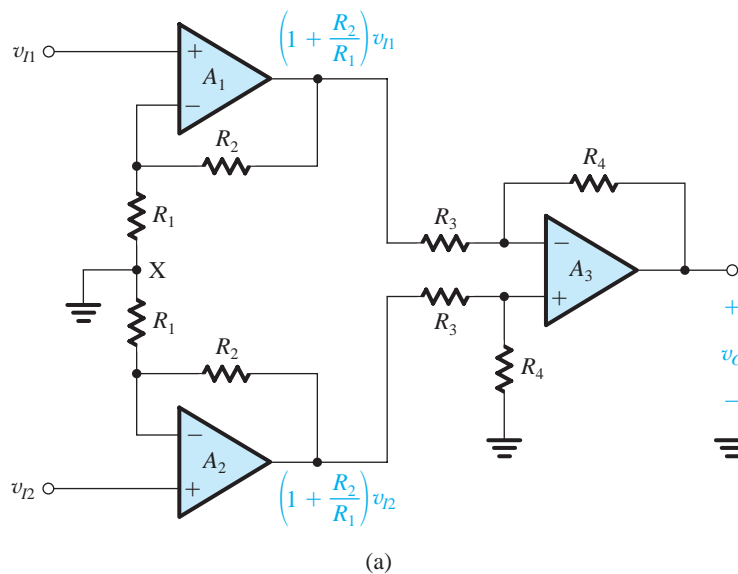
**Ans.** (a) 100 V/V (40 dB); (b) 4 k $\Omega$ , 0  $\Omega$ ; (c) 0.04 V/V, 68 dB

**D2.16** Find values for the resistances in the circuit of Fig. 2.16 so that the circuit behaves as a difference amplifier with an input resistance of 20 k $\Omega$  and a gain of 10.

**Ans.**  $R_1 = R_3 = 10 \text{ k}\Omega$ ;  $R_2 = R_4 = 100 \text{ k}\Omega$

### 2.4.2 A Superior Circuit—The Instrumentation Amplifier

The low-input-resistance problem of the difference amplifier of Fig. 2.16 can be solved by using voltage followers to buffer the two input terminals; that is, a voltage follower of the type in Fig. 2.14 is connected between each input terminal and the corresponding input terminal of the difference amplifier. However, if we are going to use two additional op amps, we should ask the question: Can we get more from them than just impedance buffering? An obvious answer would be that we should try to get some voltage gain. It is especially interesting that we can achieve this without compromising the high input resistance simply by using followers with gain rather than unity-gain followers. Achieving some or indeed the bulk of the required gain in this new first stage of the



**Figure 2.20** A popular circuit for an instrumentation amplifier. (a) Initial approach to the circuit (b) The circuit in (a) with the connection between node X and ground removed and the two resistors  $R_1$  and  $R_1$  lumped together. This simple wiring change dramatically improves performance. (c) Analysis of the circuit in (b) assuming ideal op amps.

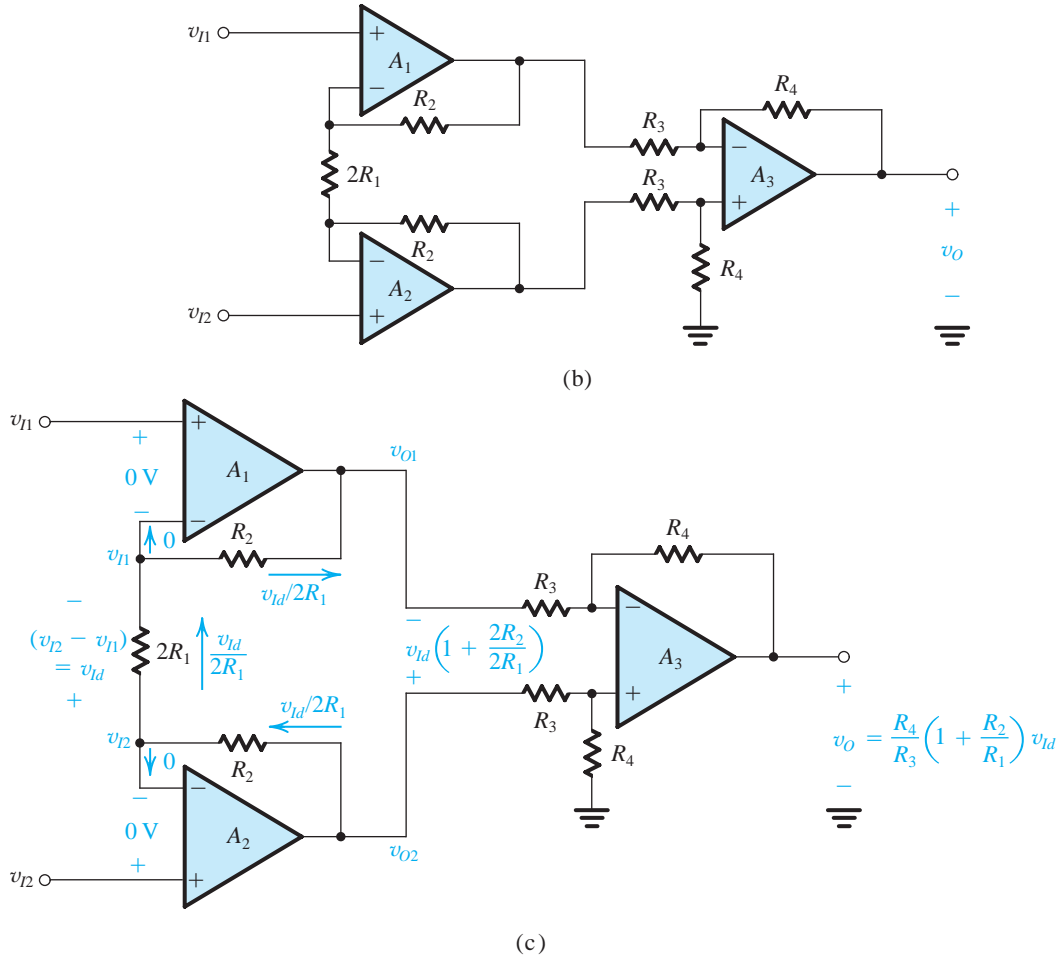


Figure 2.20 (Continued)

difference amplifier eases the burden on the difference amplifier in the second stage, leaving it to its main task of implementing the differencing function and thus rejecting common-mode signals.

The resulting circuit is shown in Fig. 2.20(a). It consists of two stages in cascade. The first stage is formed by op amps  $A_1$  and  $A_2$  and their associated resistors, and the second stage is the by-now-familiar difference amplifier formed by op amp  $A_3$  and its four associated resistors. Observe that as we set out to do, each of  $A_1$  and  $A_2$  is connected in the noninverting configuration and thus realizes a gain of  $(1 + R_2/R_1)$ . It follows that each of  $v_{i1}$  and  $v_{i2}$  is amplified by this factor, and the resulting amplified signals appear at the outputs of  $A_1$  and  $A_2$ , respectively.

The difference amplifier in the second stage operates on the difference signal  $(1 + R_2/R_1)(v_{i2} - v_{i1}) = (1 + R_2/R_1)v_{id}$  and provides at its output

$$v_O = \frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right) v_{id}$$

Thus the differential gain realized is

$$A_d = \left( \frac{R_4}{R_3} \right) \left( 1 + \frac{R_2}{R_1} \right) \quad (2.21)$$



The common-mode gain will be zero because of the differencing action of the second-stage amplifier.

The circuit in Fig. 2.20(a) has the advantage of very high (ideally infinite) input resistance and high differential gain. Also, provided  $A_1$  and  $A_2$  and their corresponding resistors are matched, the two signal paths are symmetric—a definite advantage in the design of a differential amplifier. The circuit, however, has three major disadvantages:

1. The input common-mode signal  $v_{icm}$  is amplified in the first stage by a gain equal to that experienced by the differential signal  $v_{id}$ . This is a very serious issue, for it could result in the signals at the outputs of  $A_1$  and  $A_3$  being of such large magnitudes that the op amps saturate (more on op-amp saturation in Section 2.8). But even if the op amps do not saturate, the difference amplifier of the second stage will now have to deal with much larger common-mode signals, with the result that the CMRR of the overall amplifier will inevitably be reduced.
2. The two amplifier channels in the first stage have to be perfectly matched, otherwise a spurious signal may appear between their two outputs. Such a signal would get amplified by the difference amplifier in the second stage.
3. To vary the differential gain  $A_d$ , two resistors have to be varied simultaneously, say the two resistors labeled  $R_1$ . At each gain setting the two resistors have to be perfectly matched: a difficult task.

All three problems can be solved with a very simple wiring change: Simply disconnect the node between the two resistors labeled  $R_1$ , node X, from ground. The circuit with this small but functionally profound change is redrawn in Fig. 2.20(b), where we have lumped the two resistors ( $R_1$  and  $R_1$ ) together into a single resistor ( $2R_1$ ).

Analysis of the circuit in Fig. 2.20(b), assuming ideal op amps, is straightforward, as is illustrated in Fig. 2.20(c). The key point is that the virtual short circuits at the inputs of op amps  $A_1$  and  $A_2$  cause the input voltages  $v_{i1}$  and  $v_{i2}$  to appear at the two terminals of resistor ( $2R_1$ ). Thus the differential input voltage  $v_{i2} - v_{i1} \equiv v_{id}$  appears across  $2R_1$  and causes a current  $i = v_{id}/2R_1$  to flow through  $2R_1$  and the two resistors labeled  $R_2$ . This current in turn produces a voltage difference between the output terminals of  $A_1$  and  $A_2$  given by

$$v_{O2} - v_{O1} = \left(1 + \frac{2R_2}{2R_1}\right) v_{id}$$

The difference amplifier formed by op amp  $A_3$  and its associated resistors senses the voltage difference ( $v_{O2} - v_{O1}$ ) and provides a proportional output voltage  $v_O$ :

$$\begin{aligned} v_O &= \frac{R_4}{R_3}(v_{O2} - v_{O1}) \\ &= \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right) v_{id} \end{aligned}$$

Thus the overall differential voltage-gain is given by

$$\text{①} \quad A_d \equiv \frac{v_O}{v_{id}} = \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right) \quad (2.22)$$

Observe that proper differential operation does *not* depend on the matching of the two resistors labeled  $R_2$ . Indeed, if one of the two is of different value, say  $R'_2$ , the expression for  $A_d$  becomes

$$A_d = \frac{R_4}{R_3} \left(1 + \frac{R_2 + R'_2}{2R_1}\right) \quad (2.23)$$

Consider next what happens when the two input terminals are connected together to a common-mode input voltage  $v_{lcm}$ . It is easy to see that an equal voltage appears at the negative input terminals of  $A_1$  and  $A_2$ , causing the current through  $2R_1$  to be zero. Thus there will be no current flowing in the  $R_2$  resistors, and the voltages at the output terminals of  $A_1$  and  $A_2$  will be equal to the input (i.e.,  $v_{lcm}$ ). Thus the first stage no longer amplifies  $v_{lcm}$ ; it simply propagates  $v_{lcm}$  to its two output terminals, where they are subtracted to produce a zero common-mode output by  $A_3$ . The difference amplifier in the second stage, however, now has a much improved situation at its input: The difference signal has been amplified by  $(1 + R_2/R_1)$  while the common-mode voltage remained unchanged.

Finally, we observe from the expression in Eq. (2.22) that the gain can be varied by changing only one resistor,  $2R_1$ . We conclude that this is an excellent differential amplifier circuit and is widely employed as an instrumentation amplifier; that is, as the input amplifier used in a variety of electronic instruments.

### Example 2.3

Design the instrumentation amplifier circuit in Fig. 2.20(b) to provide a gain that can be varied over the range of 2 to 1000 utilizing a 100-k $\Omega$  variable resistance (a potentiometer, or “pot” for short).

#### Solution

It is usually preferable to obtain all the required gain in the first stage, leaving the second stage to perform the task of taking the difference between the outputs of the first stage and thereby rejecting the common-mode signal. In other words, the second stage is usually designed for a gain of 1. Adopting this approach, we select all the second-stage resistors to be equal to a practically convenient value, say 10 k $\Omega$ . The problem then reduces to designing the first stage to realize a gain adjustable over the range of 2 to 1000. Implementing  $2R_1$  as the series combination of a fixed resistor  $R_{1f}$  and the variable resistor  $R_{1v}$  obtained using the 100-k $\Omega$  pot (Fig. 2.21), we can write

$$1 + \frac{2R_2}{R_{1f} + R_{1v}} = 2 \text{ to } 1000$$

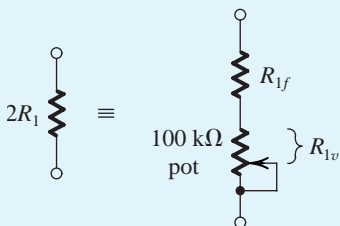
Thus,

$$1 + \frac{2R_2}{R_{1f}} = 1000$$

and

$$1 + \frac{2R_2}{R_{1f} + 100 \text{ k}\Omega} = 2$$

These two equations yield  $R_{1f} = 100.2 \text{ }\Omega$  and  $R_2 = 50.050 \text{ k}\Omega$ . Other practical values may be selected; for instance,  $R_{1f} = 100 \text{ }\Omega$  and  $R_2 = 49.9 \text{ k}\Omega$  (both values are available as standard 1%-tolerance metal-film resistors; see Appendix H) results in a gain covering approximately the required range.



**Figure 2.21** To make the gain of the circuit in Fig. 2.20(b) variable,  $2R_1$  is implemented as the series combination of a fixed resistor  $R_{1f}$  and a variable resistor  $R_{1v}$ . Resistor  $R_{1f}$  ensures that the maximum available gain is limited.

## EXERCISE

**2.17** Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of +5 V (dc) and a differential input signal of 10-mV-peak sine wave. Let  $(2R_1) = 1 \text{ k}\Omega$ ,  $R_2 = 0.5 \text{ M}\Omega$ , and  $R_3 = R_4 = 10 \text{ k}\Omega$ . Find the voltage at every node in the circuit.

**Ans.**  $v_{i1} = 5 - 0.005 \sin \omega t$ ;  $v_{i2} = 5 + 0.005 \sin \omega t$ ;  $v_- (\text{op amp } A_1) = 5 - 0.005 \sin \omega t$ ;  $v_- (\text{op amp } A_2) = 5 + 0.005 \sin \omega t$ ;  $v_{o1} = 5 - 5.005 \sin \omega t$ ;  $v_{o2} = 5 + 5.005 \sin \omega t$ ;  $v_- (A_3) = v_+ (A_3) = 2.5 + 2.5025 \sin \omega t$ ;  $v_o = 10.01 \sin \omega t$  (all in volts)

## 2.5 Integrators and Differentiators

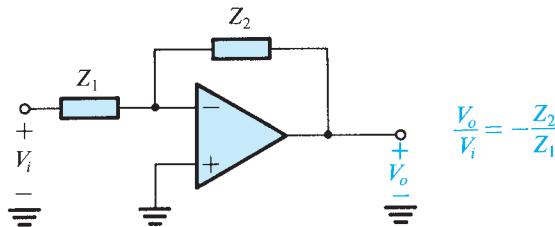
The op-amp circuit applications we have studied thus far utilized resistors in the op-amp feedback path and in connecting the signal source to the circuit, that is, in the feed-in path. As a result, circuit operation has been (ideally) independent of frequency. By allowing the use of capacitors together with resistors in the feedback and feed-in paths of op-amp circuits, we open the door to a very wide range of useful and exciting applications of the op amp. We begin our study of op-amp- $RC$  circuits by considering two basic applications, namely, signal integrators and differentiators.

### 2.5.1 The Inverting Configuration with General Impedances

To begin with, consider the inverting closed-loop configuration with impedances  $Z_1(s)$  and  $Z_2(s)$  replacing resistors  $R_1$  and  $R_2$ , respectively. The resulting circuit is shown in Fig. 2.22 and, for an ideal op amp, has the closed-loop gain or, more appropriately, the closed-loop transfer function

$$\text{①} \quad \frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} \quad (2.24)$$

As explained in Section 1.6, replacing  $s$  by  $j\omega$  provides the transfer function for physical frequencies  $\omega$ , that is, the transmission magnitude and phase for a sinusoidal input signal of frequency  $\omega$ .



**Figure 2.22** The inverting configuration with general impedances in the feedback and the feed-in paths.

### Example 2.4

For the circuit in Fig. 2.23, derive an expression for the transfer function  $V_o(s)/V_i(s)$ . Show that the transfer function is that of a low-pass STC circuit. By expressing the transfer function in the standard form shown in Table 1.2 on page 34, find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz, and an input resistance of 1 k $\Omega$ . At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency?

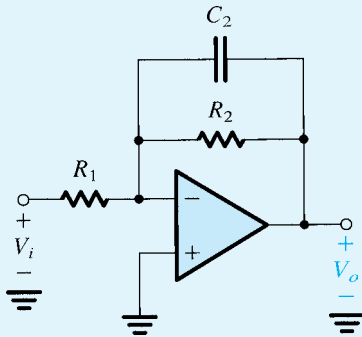


Figure 2.23 Circuit for Example 2.4.

### Solution

To obtain the transfer function of the circuit in Fig. 2.23, we substitute in Eq. (2.24),  $Z_1 = R_1$  and  $Z_2 = R_2 \parallel (1/sC_2)$ . Since  $Z_2$  is the parallel connection of two components, it is more convenient to work in terms of  $Y_2$ ; that is, we use the following alternative form of the transfer function:

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{Z_1(s)Y_2(s)}$$

and substitute  $Z_1 = R_1$  and  $Y_2(s) = (1/R_2) + sC_2$  to obtain

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{\frac{R_1}{R_2} + sC_2R_1}$$

This transfer function is of first order, has a finite dc gain (at  $s = 0$ ,  $V_o/V_i = -R_2/R_1$ ), and has zero gain at infinite frequency. Thus it is the transfer function of a low-pass STC network and can be expressed in the standard form of Table 1.2 as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + sC_2R_2}$$

from which we find the dc gain  $K$  to be

$$K = -\frac{R_2}{R_1}$$

**Example 2.4** *continued*

and the 3-dB frequency  $\omega_0$  as

$$\omega_0 = \frac{1}{C_2 R_2}$$

We could have found all this from the circuit in Fig. 2.23 by inspection. Specifically, note that the capacitor behaves as an open circuit at dc; thus at dc the gain is simply  $(-R_2/R_1)$ . Furthermore, because there is a virtual ground at the inverting input terminal, the resistance seen by the capacitor is  $R_2$ , and thus the time constant of the STC network is  $C_2 R_2$ .

Now to obtain a dc gain of 40 dB, that is, 100 V/V, we select  $R_2/R_1 = 100$ . For an input resistance of 1 k $\Omega$ , we select  $R_1 = 1$  k $\Omega$ , and thus  $R_2 = 100$  k $\Omega$ . Finally, for a 3-dB frequency  $f_0 = 1$  kHz, we select  $C_2$  from

$$2\pi \times 1 \times 10^3 = \frac{1}{C_2 \times 100 \times 10^3}$$

which yields  $C_2 = 1.59$  nF.

The circuit has gain and phase Bode plots of the standard form in Fig. 1.23. As the gain falls off at the rate of  $-20$  dB/decade, it will reach 0 dB in two decades, that is, at  $f = 100f_0 = 100$  kHz. As Fig. 1.23(b) indicates, at such a frequency which is much greater than  $f_0$ , the phase is approximately  $-90^\circ$ . To this, however, we must add the  $180^\circ$  arising from the inverting nature of the amplifier (i.e., the negative sign in the transfer function expression). Thus at 100 kHz, the total phase shift will be  $-270^\circ$  or, equivalently,  $+90^\circ$ .

## 2.5.2 The Inverting Integrator

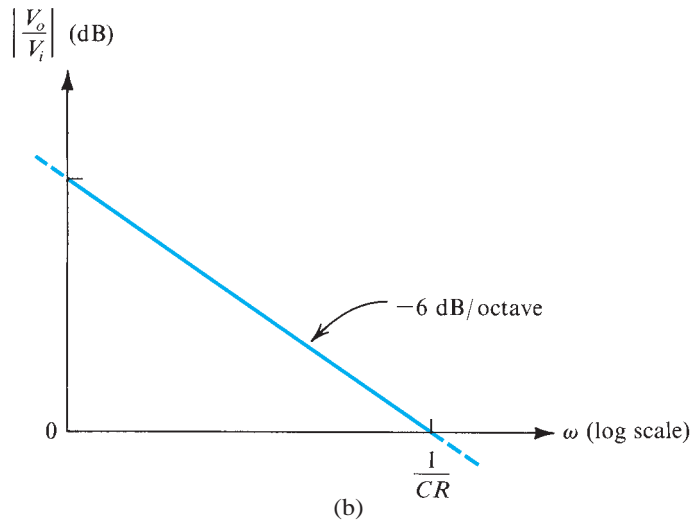
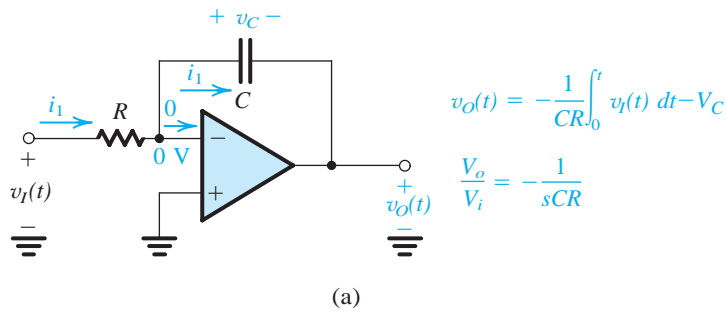
By placing a capacitor in the feedback path (i.e., in place of  $Z_2$  in Fig. 2.22) and a resistor at the input (in place of  $Z_1$ ), we obtain the circuit of Fig. 2.24(a). We shall now show that this circuit realizes the mathematical operation of integration. Let the input be a time-varying function  $v_i(t)$ . The virtual ground at the inverting op-amp input causes  $v_i(t)$  to appear in effect across  $R$ , and thus the current  $i_1(t)$  will be  $v_i(t)/R$ . This current flows through the capacitor  $C$ , causing charge to accumulate on  $C$ . If we assume that the circuit begins operation at time  $t = 0$ , then at an arbitrary time  $t$  the current  $i_1(t)$  will have deposited on  $C$  a charge equal to  $\int_0^t i_1(t) dt$ . Thus the capacitor voltage  $v_C(t)$  will change by  $\frac{1}{C} \int_0^t i_1(t) dt$ . If the initial voltage on  $C$  (at  $t = 0$ ) is denoted  $V_C$ , then

$$v_C(t) = V_C + \frac{1}{C} \int_0^t i_1(t) dt$$

Now the output voltage  $v_o(t) = -v_C(t)$ ; thus,

$$\text{①} \quad v_o(t) = -\frac{1}{CR} \int_0^t v_i(t) dt - V_C \quad (2.25)$$

Thus the circuit provides an output voltage that is proportional to the time integral of the input, with  $V_C$  being the initial condition of integration and  $CR$  the **integrator time constant**. Note that, as expected, there is a negative sign attached to the output voltage, and thus this



**Figure 2.24** (a) The Miller or inverting integrator. (b) Frequency response of the integrator.

integrator circuit is said to be an **inverting integrator**. It is also known as a **Miller integrator** after an early worker in this field.

The operation of the integrator circuit can be described alternatively in the frequency domain by substituting  $Z_1(s) = R$  and  $Z_2(s) = 1/sC$  in Eq. (2.24) to obtain the transfer function

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR} \quad (2.26) \quad \text{1}$$

For physical frequencies,  $s = j\omega$  and

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR} \quad (2.27) \quad \text{1}$$

Thus the integrator transfer function has magnitude

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega CR} \quad (2.28) \quad \text{1}$$



and phase

1

$$\phi = +90^\circ \quad (2.29)$$

The Bode plot for the integrator magnitude response can be obtained by noting from Eq. (2.28) that as  $\omega$  doubles (increases by an octave) the magnitude is halved (decreased by 6 dB). Thus the Bode plot is a straight line of slope  $-6$  dB/octave (or, equivalently,  $-20$  dB/decade). This line (shown in Fig. 2.24b) intercepts the 0-dB line at the frequency that makes  $|V_o/V_i| = 1$ , which from Eq. (2.28) is

1

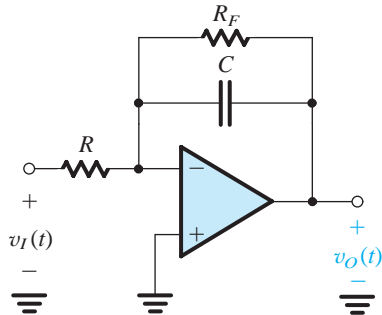
$$\omega_{int} = \frac{1}{CR} \quad (2.30)$$

The frequency  $\omega_{int}$  is known as the **integrator frequency** and is simply the inverse of the integrator time constant.

Comparison of the frequency response of the integrator to that of an STC low-pass network indicates that the integrator behaves as a low-pass filter with a corner frequency of zero. Observe also that at  $\omega = 0$ , the magnitude of the integrator transfer function is infinite. This indicates that at dc the op amp is operating with an open loop. This should also be obvious from the integrator circuit itself. Reference to Fig. 2.24(a) shows that the feedback element is a capacitor, and thus at dc, where the capacitor behaves as an open circuit, there is no negative feedback! This is a very significant observation and one that indicates a source of problems with the integrator circuit: Any tiny dc component in the input signal will theoretically produce an infinite output. Of course, no infinite output voltage results in practice; rather, the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply ( $L_+$  or  $L_-$ ), depending on the polarity of the input dc signal.

The dc problem of the integrator circuit can be alleviated by connecting a resistor  $R_F$  across the integrator capacitor  $C$ , as shown in Fig. 2.25 and thus the gain at dc will be  $-R_F/R$  rather than infinite. Such a resistor provides a dc feedback path. Unfortunately, however, the integration is no longer ideal, and the lower the value of  $R_F$ , the less ideal the integrator circuit becomes. This is because  $R_F$  causes the frequency of the integrator pole to move from its ideal location at  $\omega = 0$  to one determined by the corner frequency of the STC network ( $R_F$ ,  $C$ ). Specifically, the integrator transfer function becomes

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_F/R}{1 + sCR_F}$$



**Figure 2.25** The Miller integrator with a large resistance  $R_F$  connected in parallel with  $C$  in order to provide negative feedback and hence finite gain at dc.

as opposed to the ideal function of  $-1/sCR$ . The lower the value we select for  $R_F$ , the higher the corner frequency ( $1/CR_F$ ) will be and the more nonideal the integrator becomes. Thus selecting a value for  $R_F$  presents the designer with a trade-off between dc performance and signal performance. The effect of  $R_F$  on integrator performance is investigated further in the Example 2.5.

### Example 2.5

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let  $R = 10\text{ k}\Omega$  and  $C = 10\text{ nF}$ . If the integrator capacitor is shunted by a  $1\text{-M}\Omega$  resistor, how will the response be modified? The op amp is specified to saturate at  $\pm 13\text{ V}$ .

#### Solution

In response to a 1-V, 1-ms input pulse, the integrator output will be

$$v_O(t) = -\frac{1}{CR} \int_0^t 1 dt, \quad 0 \leq t \leq 1\text{ ms}$$

where we have assumed that the initial voltage on the integrator capacitor is 0. For  $C = 10\text{ nF}$  and  $R = 10\text{ k}\Omega$ ,  $CR = 0.1\text{ ms}$ , and

$$v_O(t) = -10t, \quad 0 \leq t \leq 1\text{ ms}$$

which is the linear ramp shown in Fig. 2.26(b). It reaches a magnitude of  $-10\text{ V}$  at  $t = 1\text{ ms}$  and remains constant thereafter.

That the output is a linear ramp should also be obvious from the fact that the 1-V input pulse produces a constant current through the capacitor of  $1\text{ V}/10\text{ k}\Omega = 0.1\text{ mA}$ . This constant current  $I = 0.1\text{ mA}$  supplies the capacitor with a charge  $It$ , and thus the capacitor voltage changes linearly as  $(It/C)$ , resulting in  $v_O = -(I/C)t$ . It is worth remembering that charging a capacitor with a constant current produces a linear voltage across it.

Next consider the situation with resistor  $R_F = 1\text{ M}\Omega$  connected across  $C$ . As before, the 1-V pulse will provide a constant current  $I = 0.1\text{ mA}$ . Now, however, this current is supplied to an STC network composed of  $R_F$  in parallel with  $C$ . Thus, the output will be an exponential heading toward  $-100\text{ V}$  with a time constant of  $CR_F = 10 \times 10^{-9} \times 1 \times 10^6 = 10\text{ ms}$ ,

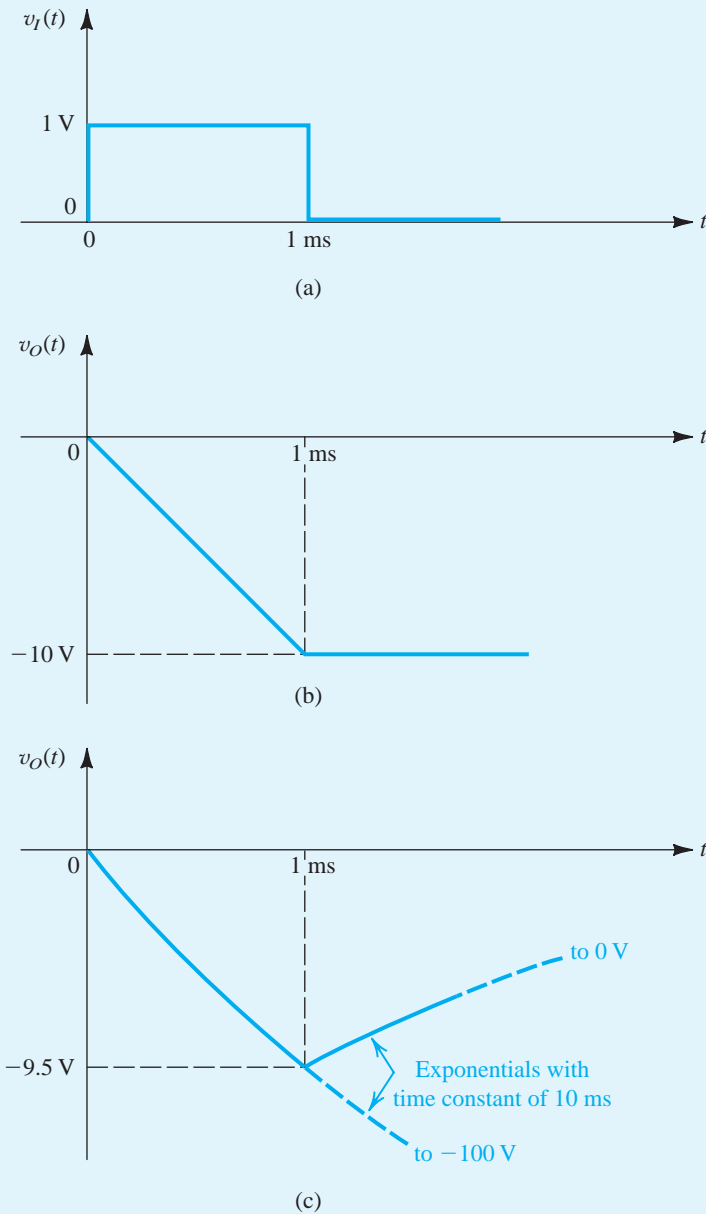
$$v_O(t) = -100(1 - e^{-t/10}), \quad 0 \leq t \leq 1\text{ ms}$$

Of course, the exponential will be interrupted at the end of the pulse, that is, at  $t = 1\text{ ms}$ , and the output will reach the value

$$v_O(1\text{ ms}) = -100(1 - e^{-1/10}) = -9.5\text{ V}$$

The output waveform is shown in Fig. 2.26(c), from which we see that including  $R_F$  causes the ramp to be slightly rounded such that the output reaches only  $-9.5\text{ V}$ ,  $0.5\text{ V}$  short of the ideal value of  $-10\text{ V}$ . Furthermore, for  $t > 1\text{ ms}$ , the capacitor discharges through  $R_F$  with the relatively long time-constant of  $10\text{ ms}$ . Finally, we note that op amp saturation, specified to occur at  $\pm 13\text{ V}$ , has no effect on the operation of this circuit.

## Example 2.5 continued



**Figure 2.26** Waveforms for Example 2.5: (a) Input pulse. (b) Output linear ramp of ideal integrator with time constant of 0.1 ms. (c) Output exponential ramp with resistor  $R_f$  connected across integrator capacitor.

The preceding example hints at an important application of integrators, namely, their use in providing triangular waveforms in response to square-wave inputs. This application is explored in Exercise 2.18. Integrators have many other applications, including their use in the design of filters (Chapter 16).

### 2.5.3 The Op-Amp Differentiator

Interchanging the location of the capacitor and the resistor of the integrator circuit results in the circuit in Fig. 2.27(a), which performs the mathematical function of differentiation. To see how this comes about, let the input be the time-varying function  $v_I(t)$ , and note that the virtual ground at the inverting input terminal of the op amp causes  $v_I(t)$  to appear in effect across the capacitor  $C$ . Thus the current through  $C$  will be  $C(dv_I/dt)$ , and this current flows through the feedback resistor  $R$  providing at the op-amp output a voltage  $v_O(t)$ ,

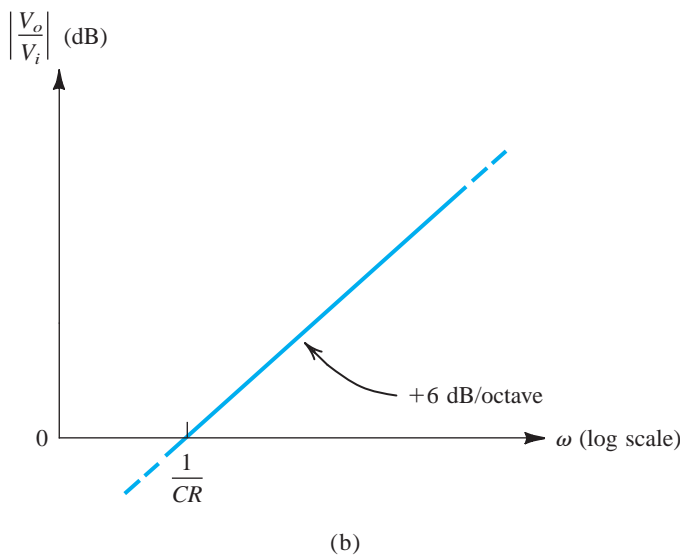
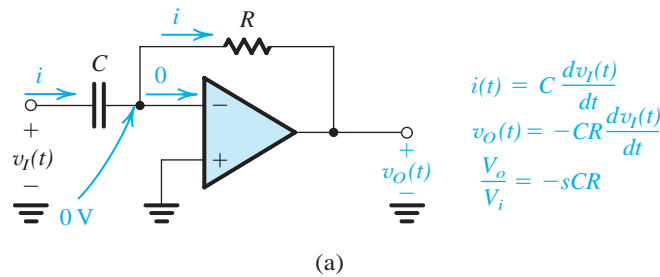
$$v_O(t) = -CR \frac{dv_I(t)}{dt} \quad (2.31) \quad \text{①}$$

The frequency-domain transfer function of the differentiator circuit can be found by substituting in Eq. (2.24),  $Z_1(s) = 1/sC$  and  $Z_2(s) = R$  to obtain

$$\frac{V_o(s)}{V_i(s)} = -sCR \quad (2.32) \quad \text{①}$$

which for physical frequencies  $s = j\omega$  yields

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR \quad (2.33) \quad \text{①}$$



**Figure 2.27** (a) A differentiator. (b) Frequency response of a differentiator with a time-constant  $CR$ .

Thus the transfer function has magnitude

$$\mathbf{1} \quad \left| \frac{V_o}{V_i} \right| = \omega CR \quad (2.34)$$

and phase

$$\mathbf{1} \quad \phi = -90^\circ \quad (2.35)$$

The Bode plot of the magnitude response can be found from Eq. (2.34) by noting that for an octave increase in  $\omega$ , the magnitude doubles (increases by 6 dB). Thus the plot is simply a straight line of slope +6 dB/octave (or, equivalently, +20 dB/decade) intersecting the 0-dB line (where  $|V_o/V_i| = 1$ ) at  $\omega = 1/CR$ , where  $CR$  is the **differentiator time-constant** [see Fig. 2.27(b)].

The frequency response of the differentiator can be thought of as that of an STC highpass filter with a corner frequency at infinity (refer to Fig. 1.24). Finally, we should note that the very nature of a differentiator circuit causes it to be a “noise magnifier.” This is due to the spike introduced at the output every time there is a sharp change in  $v_i(t)$ ; such a change could be interference coupled electromagnetically (“picked up”) from adjacent signal sources. For this reason and because they suffer from stability problems (Chapter 10), differentiator circuits are generally avoided in practice. When the circuit of Fig. 2.27(a) is used, it is usually necessary to connect a small-valued resistor in series with the capacitor. This modification, unfortunately, turns the circuit into a nonideal differentiator.

## EXERCISES

- 2.18** Consider a symmetrical square wave of 20-V peak-to-peak, 0 average, and 2-ms period applied to a Miller integrator. Find the value of the time constant  $CR$  such that the triangular waveform at the output has a 20-V peak-to-peak amplitude.

**Ans.** 0.5 ms

- D2.19** Use an ideal op amp to design an inverting integrator with an input resistance of 10 k $\Omega$  and an integration time constant of  $10^{-3}$  s. What is the gain magnitude and phase angle of this circuit at 10 rad/s and at 1 rad/s? What is the frequency at which the gain magnitude is unity?

**Ans.**  $R = 10$  k $\Omega$ ,  $C = 0.1$   $\mu$ F; at  $\omega = 10$  rad/s:  $|V_o/V_i| = 100$  V/V and  $\phi = +90^\circ$ ; at  $\omega = 1$  rad/s:  $|V_o/V_i| = 1,000$  V/V and  $\phi = +90^\circ$ ; 1000 rad/s

- D2.20** Design a differentiator to have a time constant of  $10^{-2}$  s and an input capacitance of 0.01  $\mu$ F. What is the gain magnitude and phase of this circuit at 10 rad/s, and at  $10^3$  rad/s? In order to limit the high-frequency gain of the differentiator circuit to 100, a resistor is added in series with the capacitor. Find the required resistor value.

**Ans.**  $C = 0.01$   $\mu$ F;  $R = 1$  M $\Omega$ ; at  $\omega = 10$  rad/s:  $|V_o/V_i| = 0.1$  V/V and  $\phi = -90^\circ$ ; at  $\omega = 1000$  rad/s:  $|V_o/V_i| = 10$  V/V and  $\phi = -90^\circ$ ; 10 k $\Omega$

## 2.6 DC Imperfections

Thus far we have considered the op amp to be ideal. The only exception has been a brief discussion of the effect of the op-amp finite gain  $A$  on the closed-loop gain of the inverting and noninverting configurations. Although in many applications the assumption of an ideal op

amp is not a bad one, a circuit designer has to be thoroughly familiar with the characteristics of practical op amps and the effects of such characteristics on the performance of op-amp circuits. Only then will the designer be able to use the op amp intelligently, especially if the application at hand is not a straightforward one. The nonideal properties of op amps will, of course, limit the range of operation of the circuits analyzed in the previous examples.

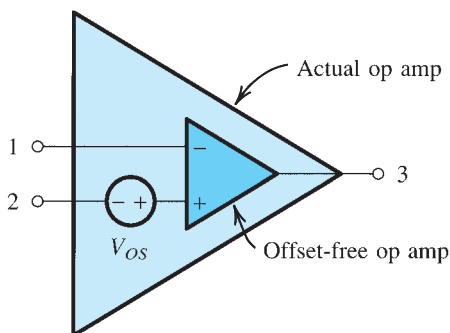
In this and the two sections that follow, we consider some of the important nonideal properties of the op amp.<sup>3</sup> We do this by treating one nonideality at a time, beginning in this section with the dc problems to which op amps are susceptible.

### 2.6.1 Offset Voltage

Because op amps are direct-coupled devices with large gains at dc, they are prone to dc problems. The first such problem is the dc offset voltage. To understand this problem consider the following *conceptual* experiment: If the two input terminals of the op amp are tied together and connected to ground, it will be found that despite the fact that  $v_{id} = 0$ , a finite dc voltage exists at the output. In fact, if the op amp has a high dc gain, the output will be at either the positive or negative saturation level. The op-amp output can be brought back to its ideal value of 0 V by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op amp. This external source balances out the input offset voltage of the op amp. It follows that the **input offset voltage** ( $V_{OS}$ ) must be of equal magnitude and of opposite polarity to the voltage we applied externally.

The input offset voltage arises as a result of the unavoidable mismatches present in the input differential stage inside the op amp. In later chapters (in particular Chapters 8 and 12) we shall study this topic in detail. Here, however, our concern is to investigate the effect of  $V_{OS}$  on the operation of closed-loop op-amp circuits. Toward that end, we note that general-purpose op amps exhibit  $V_{OS}$  in the range of 1 mV to 5 mV. Also, the value of  $V_{OS}$  depends on temperature. The op-amp data sheets usually specify typical and maximum values for  $V_{OS}$  at room temperature as well as the temperature coefficient of  $V_{OS}$  (usually in  $\mu\text{V}/^\circ\text{C}$ ). They do not, however, specify the polarity of  $V_{OS}$  because the component mismatches that give rise to  $V_{OS}$  are obviously not known a priori; different units of the same op-amp type may exhibit either a positive or a negative  $V_{OS}$ .

To analyze the effect of  $V_{OS}$  on the operation of op-amp circuits, we need a circuit model for the op amp with input offset voltage. Such a model is shown in Fig. 2.28. It consists of a



**Figure 2.28** Circuit model for an op amp with input offset voltage  $V_{OS}$ .

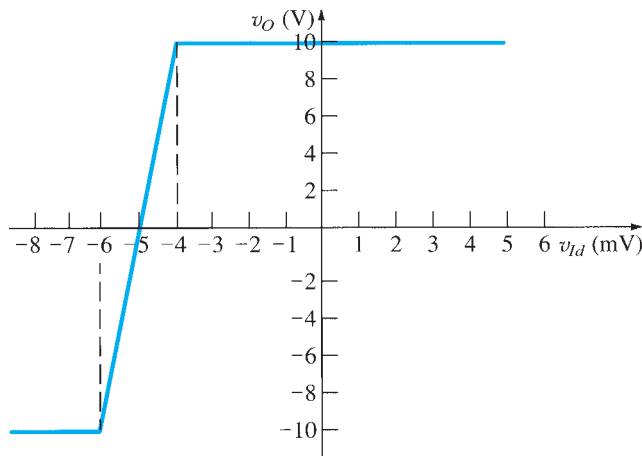
<sup>3</sup>We should note that real op amps have nonideal effects additional to those discussed in this chapter. These include finite (nonzero) common-mode gain or, equivalently, noninfinite CMRR, noninfinite input resistance, and nonzero output resistance. The effect of these, however, on the performance of most of the closed-loop circuits studied here is not very significant, and their study will be postponed to later chapters (in particular Chapters 8, 9, and 12).

dc source of value  $V_{os}$  placed in series with the positive input lead of an offset-free op amp. The justification for this model follows from the description above.

## EXERCISE

**2.21** Use the model of Fig. 2.28 to sketch the transfer characteristic  $v_o$  versus  $v_{id}$  ( $v_o \equiv v_3$  and  $v_{id} \equiv v_2 - v_1$ ) of an op amp having an open-loop dc gain  $A_0 = 10^4$  V/V, output saturation levels of  $\pm 10$  V, and  $V_{os}$  of +5 mV.

**Ans.** See Fig. E2.21. Observe that true to its name, the input offset voltage causes an offset in the voltage-transfer characteristic; rather than passing through the origin it is now shifted to the left by  $V_{os}$ .



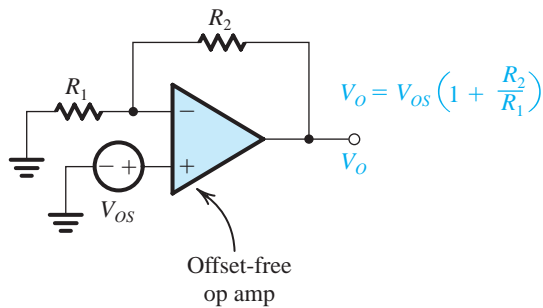
**Figure E2.21** Transfer characteristic of an op amp with  $V_{os} = 5$  mV.

Analysis of op-amp circuits to determine the effect of the op-amp  $V_{os}$  on their performance is straightforward: The input voltage signal source is short-circuited and the op amp is replaced with the model of Fig. 2.28. (Eliminating the input signal, done to simplify matters, is based on the principle of superposition.) Following this procedure, we find that both the inverting and the noninverting amplifier configurations result in the same circuit, that shown in Fig. 2.29, from which the output dc voltage due to  $V_{os}$  is found to be

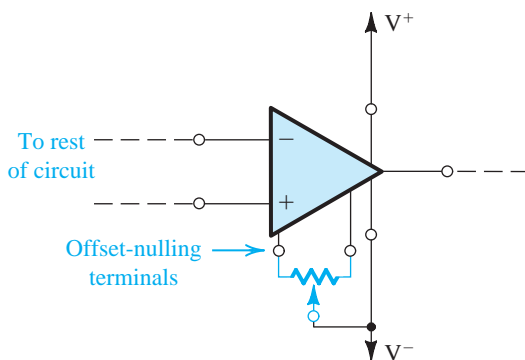
**1**

$$V_o = V_{os} \left[ 1 + \frac{R_2}{R_1} \right] \quad (2.36)$$

This output dc voltage can have a large magnitude. For instance, a noninverting amplifier with a closed-loop gain of 1000, when constructed from an op amp with a 5-mV input offset voltage, will have a dc output voltage of +5 V or -5 V (depending on the polarity of  $V_{os}$ ) rather than the ideal value of 0 V. Now, when an input signal is applied to the



**Figure 2.29** Evaluating the output dc offset voltage due to  $V_{Os}$  in a closed-loop amplifier.



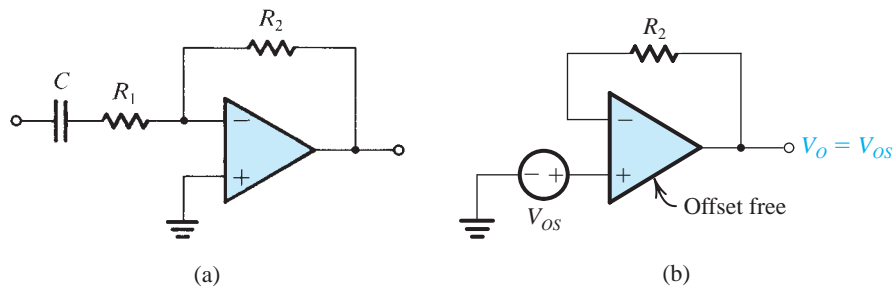
**Figure 2.30** The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

amplifier, the corresponding signal output will be superimposed on the 5-V dc. Obviously then, the allowable signal swing at the output will be reduced. Even worse, if the signal to be amplified is dc, we would not know whether the output is due to  $V_{Os}$  or to the signal!

Some op amps are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output dc voltage due to  $V_{Os}$ . Figure 2.30 shows such an arrangement that is typically used with general-purpose op amps. A potentiometer is connected between the offset-nulling terminals with the wiper of the potentiometer connected to the op-amp negative supply. Moving the potentiometer wiper introduces an imbalance that counteracts the asymmetry present in the internal op-amp circuitry and that gives rise to  $V_{Os}$ . We shall return to this point in the context of our study of the internal circuitry of op amps in Chapter 12. It should be noted, however, that even though the dc output offset can be trimmed to zero, the problem remains of the variation (or drift) of  $V_{Os}$  with temperature.

One way to overcome the dc offset problem is by capacitively coupling the amplifier. This, however, will be possible only in applications where the closed-loop amplifier is not required to amplify dc or very-low-frequency signals. Figure 2.31(a) shows a capacitively coupled amplifier. Because of its infinite impedance at dc, the coupling capacitor will cause the gain to be zero at dc. As a result the equivalent circuit for determining the dc output





**Figure 2.31** (a) A capacitively coupled inverting amplifier. (b) The equivalent circuit for determining its dc output offset voltage  $V_O$ .

voltage resulting from the op-amp input offset voltage  $V_{OS}$  will be that shown in Fig. 2.31(b). Thus  $V_{OS}$  sees in effect a unity-gain voltage follower, and the dc output voltage  $V_O$  will be equal to  $V_{OS}$  rather than  $V_{OS}(1 + R_2/R_1)$ , which is the case without the coupling capacitor. As far as input signals are concerned, the coupling capacitor  $C$  forms together with  $R_1$  an STC high-pass circuit with a corner frequency of  $\omega_0 = 1/CR_1$ . Thus the gain of the capacitively coupled amplifier will fall off at the low-frequency end [from a magnitude of  $(1 + R_2/R_1)$  at high frequencies] and will be 3 dB down at  $\omega_0$ .

## EXERCISES

**2.22** Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of  $\pm 10$  V. (a) What is (approximately) the peak sine-wave input signal that can be applied without output clipping? (b) If the effect of  $V_{OS}$  is nulled at room temperature ( $25^\circ\text{C}$ ), how large an input can one now apply if: (i) the circuit is to operate at a constant temperature? (ii) the circuit is to operate at a temperature in the range  $0^\circ\text{C}$  to  $75^\circ\text{C}$  and the temperature coefficient of  $V_{OS}$  is  $10\ \mu\text{V}/^\circ\text{C}$ ?

**Ans.** (a) 7 mV; (b) 10 mV, 9.5 mV

**2.23** Consider the same amplifier as in Exercise 2.22—that is, an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of  $\pm 10$  V—except here let the amplifier be capacitively coupled as in Fig. 2.31(a). (a) What is the dc offset voltage at the output, and what (approximately) is the peak sine-wave signal that can be applied at the input without output clipping? Is there a need for offset trimming? (b) If  $R_1 = 1\ \text{k}\Omega$  and  $R_2 = 1\ \text{M}\Omega$ , find the value of the coupling capacitor  $C_1$  that will ensure that the gain will be greater than 57 dB down to 100 Hz.

**Ans.** (a) 3 mV, 10 mV, no need for offset trimming; (b)  $1.6\ \mu\text{F}$

### 2.6.2 Input Bias and Offset Currents

The second dc problem encountered in op amps is illustrated in Fig. 2.32. In order for the op amp to operate, its two input terminals have to be supplied with dc currents, termed the **input bias currents**.<sup>4</sup> In Fig. 2.32 these two currents are represented by two current sources,  $I_{B1}$  and  $I_{B2}$ , connected to the two input terminals. It should be emphasized that the input bias currents are independent of the fact that a real op amp has finite (though large) input resistance (not shown in Fig. 2.32). The op-amp manufacturer usually specifies the average value of  $I_{B1}$  and  $I_{B2}$  as well as their expected difference. The average value  $I_B$  is called the **input bias current**,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

and the difference is called the **input offset current** and is given by

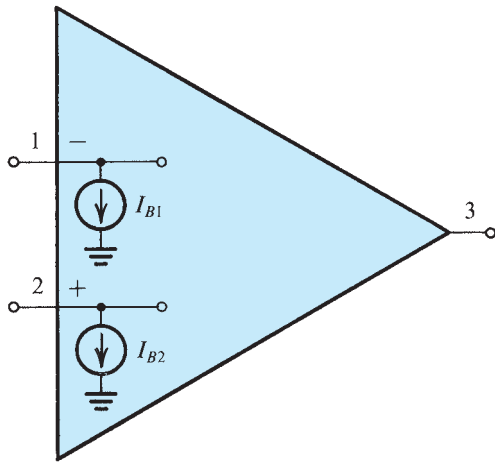
$$I_{OS} = |I_{B1} - I_{B2}|$$

Typical values for general-purpose op amps that use bipolar transistors are  $I_B = 100$  nA and  $I_{OS} = 10$  nA.

We now wish to find the dc output voltage of the closed-loop amplifier due to the input bias currents. To do this we ground the signal source and obtain the circuit shown in Fig. 2.33 for both the inverting and noninverting configurations. As shown in Fig. 2.33, the output dc voltage is given by

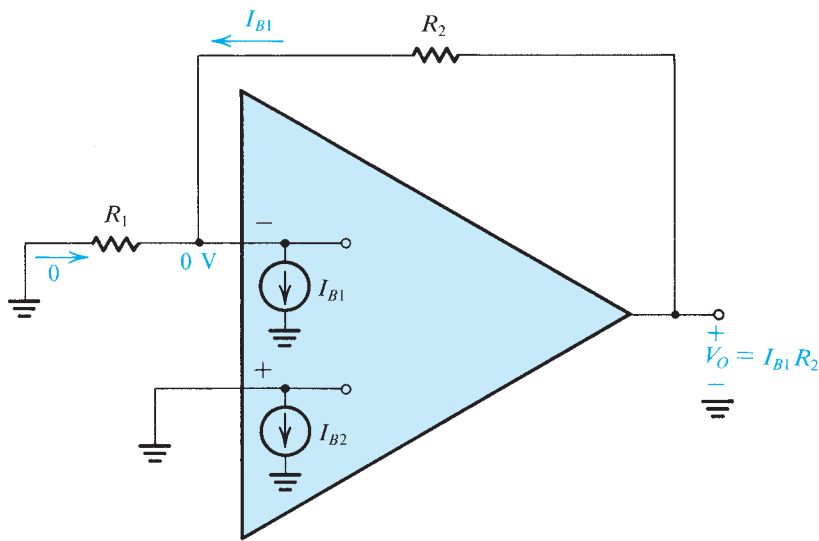
$$V_O = I_{B1}R_2 \approx I_B R_2 \quad (2.37)$$

This obviously places an upper limit on the value of  $R_2$ . Fortunately, however, a technique exists for reducing the value of the output dc voltage due to the input bias currents. The method consists of introducing a resistance  $R_3$  in series with the noninverting input lead, as

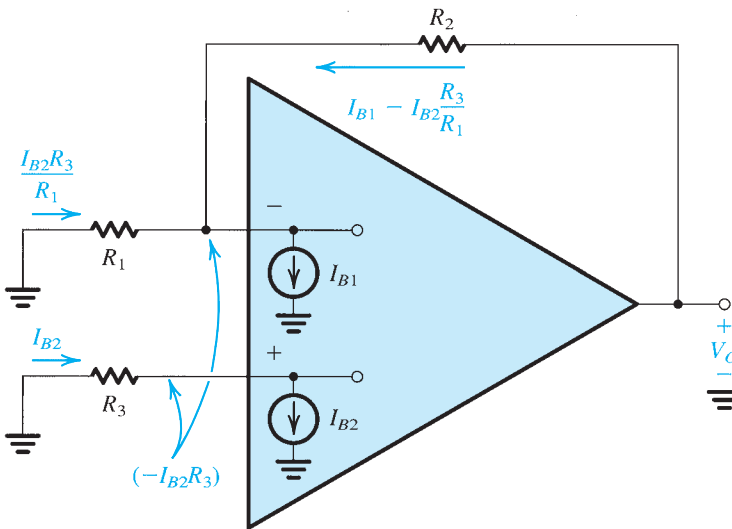


**Figure 2.32** The op-amp input bias currents represented by two current sources  $I_{B1}$  and  $I_{B2}$ .

<sup>4</sup>This is the case for op amps constructed using bipolar junction transistors (BJTs). Those using MOSFETs in the first (input) stage do not draw an appreciable input bias current; nevertheless, the input terminals should have continuous dc paths to ground. More on this in later chapters.



**Figure 2.33** Analysis of the closed-loop amplifier, taking into account the input bias currents.



**Figure 2.34** Reducing the effect of the input bias currents by introducing a resistor  $R_3$ .

shown in Fig. 2.34. From a signal point of view,  $R_3$  has a negligible effect (ideally no effect). The appropriate value for  $R_3$  can be determined by analyzing the circuit in Fig. 2.34, where analysis details are shown, and the output voltage is given by

$$V_O = -I_{B2}R_3 + R_2(I_{B1} - I_{B2}R_3/R_1) \quad (2.38)$$

Consider first the case  $I_{B1} = I_{B2} = I_B$ , which results in

$$V_O = I_B[R_2 - R_3(1 + R_2/R_1)]$$

Thus we can reduce  $V_o$  to zero by selecting  $R_3$  such that

$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1 R_2}{R_1 + R_2} \quad (2.39)$$

That is,  $R_3$  should be made equal to the parallel equivalent of  $R_1$  and  $R_2$ .

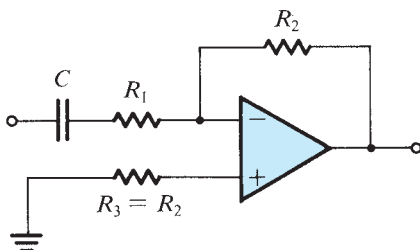
Having selected  $R_3$  as above, let us evaluate the effect of a finite offset current  $I_{OS}$ . Let  $I_{B1} = I_B + I_{OS}/2$  and  $I_{B2} = I_B - I_{OS}/2$ , and substitute in Eq. (2.38). The result is

$$V_o = I_{OS} R_2 \quad (2.40)$$

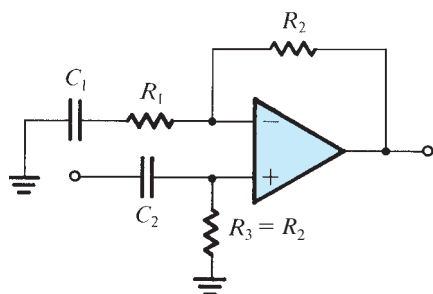


which is usually about an order of magnitude smaller than the value obtained without  $R_3$  (Eq. 2.37). We conclude that to minimize the effect of the input bias currents, one should *place in the positive lead a resistance equal to the equivalent dc resistance seen by the inverting terminal*. We emphasize the word *dc* in the last statement; note that if the amplifier is ac-coupled, we should select  $R_3 = R_2$ , as shown in Fig. 2.35.

While we are on the subject of ac-coupled amplifiers, we should note that one must always provide a continuous dc path between each of the input terminals of the op amp and ground. This is the case no matter how small  $I_B$  is. For this reason the ac-coupled noninverting amplifier of Fig. 2.36 will *not* work without the resistance  $R_3$  to ground. Unfortunately, including  $R_3$  lowers considerably the input resistance of the closed-loop amplifier.



**Figure 2.35** In an ac-coupled amplifier the dc resistance seen by the inverting terminal is  $R_2$ ; hence  $R_3$  is chosen equal to  $R_2$ .



**Figure 2.36** Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor  $R_3$ .

## EXERCISE

**2.24** Consider an inverting amplifier circuit designed using an op amp and two resistors,  $R_1 = 10 \text{ k}\Omega$  and  $R_2 = 1 \text{ M}\Omega$ . If the op amp is specified to have an input bias current of  $100 \text{ nA}$  and an input offset current of  $10 \text{ nA}$ , find the output dc offset voltage resulting and the value of a resistor  $R_3$  to be placed in series with the positive input lead in order to minimize the output offset voltage. What is the new value of  $V_o$ ?

**Ans.**  $0.1 \text{ V}$ ;  $9.9 \text{ k}\Omega$  ( $\approx 10 \text{ k}\Omega$ );  $0.01 \text{ V}$

### 2.6.3 Effect of $V_{OS}$ and $I_{OS}$ on the Operation of the Inverting Integrator

Our discussion of the inverting integrator circuit in Section 2.5.2 mentioned the susceptibility of this circuit to saturation in the presence of small dc voltages or currents. It behooves us therefore to consider the effect of the op-amp dc offsets on its operation. As will be seen, these effects can be quite dramatic.

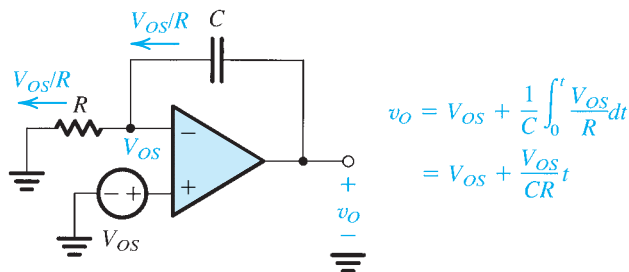
To see the effect of the input dc offset voltage  $V_{OS}$ , consider the integrator circuit in Fig. 2.38, where for simplicity we have short-circuited the input signal source. Analysis of the circuit is straightforward and is shown in Fig. 2.37. Assuming for simplicity that at time  $t = 0$  the voltage across the capacitor is zero, the output voltage as a function of time is given by

**I**

$$v_o = V_{OS} + \frac{V_{OS}}{CR} t \quad (2.41)$$

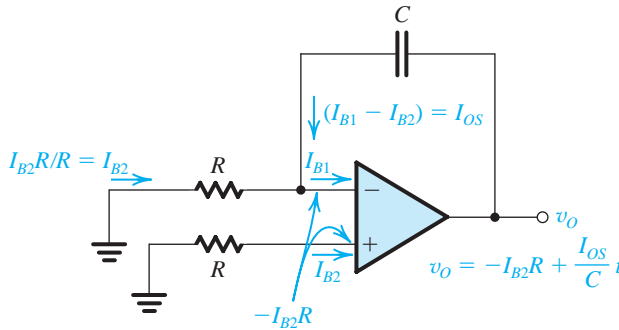
Thus  $v_o$  increases linearly with time until the op amp saturates—clearly an unacceptable situation! As should be expected, the dc input offset current  $I_{OS}$  produces a similar problem. Figure 2.38 illustrates the situation. Observe that we have added a resistance  $R$  in the op-amp positive-input lead in order to keep the input bias current  $I_b$  from flowing through  $C$ . Nevertheless, the offset current  $I_{OS}$  will flow through  $C$  and cause  $v_o$  to ramp linearly with time until the op amp saturates.

As mentioned in Section 2.5.2 the dc problem of the integrator circuit can be alleviated by connecting a resistor  $R_f$  across the integrator capacitor  $C$ , as shown in Fig. 2.25.



**Figure 2.37** Determining the effect of the op-amp input offset voltage  $V_{OS}$  on the Miller integrator circuit. Note that since the output rises with time, the op amp eventually saturates.

Such a resistor provides a dc path through which the dc currents ( $V_{OS}/R$ ) and  $I_{OS}$  can flow, with the result that  $v_o$  will now have a dc component  $[V_{OS}(1 + R_F/R) + I_{OS}R_F]$  instead of rising linearly. To keep the dc offset at the output small, one would select a low value for  $R_F$ . Unfortunately, however, the lower the value of  $R_F$ , the less ideal the integrator circuit becomes.



**Figure 2.38** Effect of the op-amp input bias and offset currents on the performance of the Miller integrator circuit.

## EXERCISE

**2.25** Consider a Miller integrator with a time constant of 1 ms and an input resistance of 10 k $\Omega$ . Let the op amp have  $V_{OS} = 2$  mV and output saturation voltages of  $\pm 12$  V. (a) Assuming that when the power supply is turned on the capacitor voltage is zero, how long does it take for the amplifier to saturate? (b) Select the largest possible value for a feedback resistor  $R_F$  so that at least  $\pm 10$  V of output signal swing remains available. What is the corner frequency of the resulting STC network?

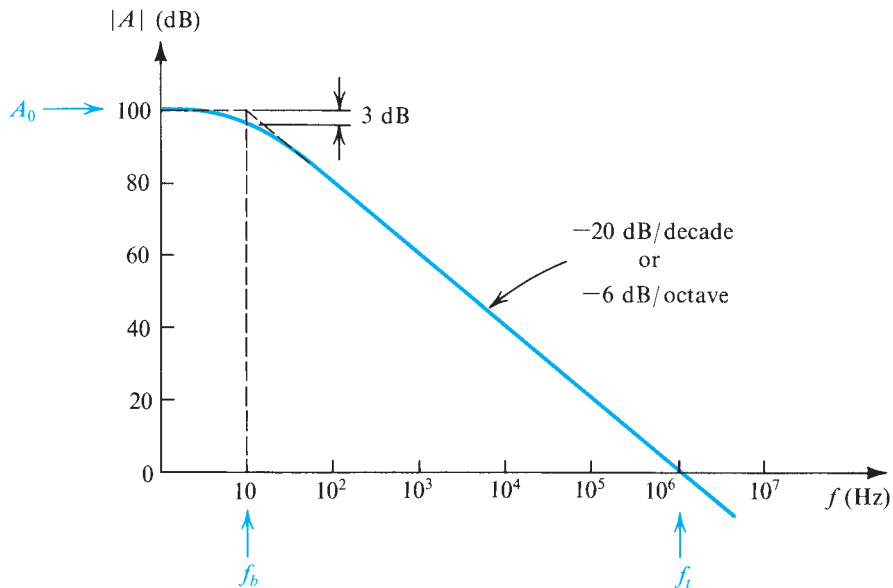
**Ans.** (a) 6 s; (b) 10 M $\Omega$ , 0.16 Hz

## 2.7 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

### 2.7.1 Frequency Dependence of the Open-Loop Gain

The differential open-loop gain  $A$  of an op amp is not infinite; rather, it is finite and decreases with frequency. Figure 2.39 shows a plot for  $|A|$ , with the numbers typical of some commercially available general-purpose op amps (such as the popular 741-type op amp, available from many semiconductor manufacturers; its internal circuit is studied in Chapter 12).

Note that although the gain is quite high at dc and low frequencies, it starts to fall off at a rather low frequency (10 Hz in our example). The uniform  $-20$ -dB/decade gain rolloff shown is typical of **internally compensated** op amps. These are units that have a network (usually a single capacitor) included within the same IC chip whose function is to cause the op-amp gain to have the single-time-constant (STC) low-pass response shown. This



**Figure 2.39** Open-loop gain of a typical general-purpose internally compensated op amp.

process of modifying the open-loop gain is termed **frequency compensation**, and its purpose is to ensure that op-amp circuits will be stable (as opposed to oscillatory). The subject of stability of op-amp circuits—or, more generally, of feedback amplifiers—will be studied in Chapter 10.

By analogy to the response of low-pass STC circuits (see Section 1.6 and, for more detail, Appendix E), the gain  $A(s)$  of an internally compensated op amp may be expressed as

$$\text{①} \quad A(s) = \frac{A_0}{1 + s/\omega_b} \quad (2.42)$$

which for physical frequencies,  $s = j\omega$ , becomes

$$\text{①} \quad A(j\omega) = \frac{A_0}{1 + j\omega/\omega_b} \quad (2.43)$$

where  $A_0$  denotes the dc gain and  $\omega_b$  is the 3-dB frequency (corner frequency or “break” frequency). For the example shown in Fig. 2.39,  $A_0 = 10^5$  and  $\omega_b = 2\pi \times 10$  rad/s. For frequencies  $\omega \gg \omega_b$  (about 10 times and higher) Eq. (2.43) may be approximated by

$$A(j\omega) \approx \frac{A_0\omega_b}{j\omega} \quad (2.44)$$

Thus,

$$|A(j\omega)| = \frac{A_0\omega_b}{\omega} \quad (2.45)$$

from which it can be seen that the gain  $|A|$  reaches unity (0 dB) at a frequency denoted by  $\omega_i$  and given by

$$\text{①} \quad \omega_i = A_0\omega_b \quad (2.46)$$

Substituting in Eq. (2.44) gives

$$A(j\omega) \approx \frac{\omega_t}{j\omega} \quad (2.47) \quad \text{!}$$

The frequency  $f_t = \omega_t/2\pi$  is usually specified on the data sheets of commercially available op amps and is known as the **unity-gain bandwidth**.<sup>5</sup> Also note that for  $\omega \gg \omega_b$  the open-loop gain in Eq. (2.42) becomes

$$A(s) \approx \frac{\omega_t}{s} \quad (2.48) \quad \text{!}$$

The gain magnitude can be obtained from Eq. (2.47) as

$$|A(j\omega)| \approx \frac{\omega_t}{\omega} = \frac{f_t}{f} \quad (2.49) \quad \text{!}$$

Thus if  $f_t$  is known ( $10^6$  Hz in our example), one can easily determine the magnitude of the op-amp gain at a given frequency  $f$ . Furthermore, observe that this relationship correlates with the Bode plot in Fig. 2.39. Specifically, for  $f \gg f_b$ , doubling  $f$  (an octave increase) results in halving the gain (a 6-dB reduction). Similarly, increasing  $f$  by a factor of 10 (a decade increase) results in reducing  $|A|$  by a factor of 10 (20 dB).

As a matter of practical importance, we note that the production spread in the value of  $f_t$  between op-amp units of the same type is usually much smaller than that observed for  $A_0$  and  $f_b$ . For this reason  $f_t$  is preferred as a specification parameter. Finally, it should be mentioned that an op amp having this uniform  $-6\text{-dB/octave}$  (or equivalently  $-20\text{-dB/decade}$ ) gain rolloff is said to have a **single-pole model**. Also, since this single pole *dominates* the amplifier frequency response, it is called a *dominant pole*. For more on poles (and zeros), the reader may wish to consult Appendix F.

## EXERCISE

**2.26** An internally compensated op amp is specified to have an open-loop dc gain of 106 dB and a unity-gain bandwidth of 3 MHz. Find  $f_b$  and the open-loop gain (in dB) at  $f_b$ , 300 Hz, 3 kHz, 12 kHz, and 60 kHz.

**Ans.** 15 Hz; 103 dB; 80 dB; 60 dB; 48 dB; 34 dB

## 2.7.2 Frequency Response of Closed-Loop Amplifiers

We next consider the effect of limited op-amp gain and bandwidth on the closed-loop transfer functions of the two basic configurations: the inverting circuit of Fig. 2.5 and the noninverting circuit of Fig. 2.12. The closed-loop gain of the inverting amplifier, assuming a finite op-amp open-loop gain  $A$ , was derived in Section 2.2 and given in Eq. (2.5), which we repeat here as

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.50) \quad \text{!}$$

<sup>5</sup>Since  $f_t$  is the product of the dc gain  $A_0$  and the 3-dB bandwidth  $f_b$  (where  $f_b = \omega_b/2\pi$ ), it is also known as the **gain-bandwidth product** (GB). The reader is cautioned, however, that in some amplifiers, the unity-gain frequency and the gain-bandwidth product are *not* equal.



Substituting for  $A$  from Eq. (2.42) and using Eq. (2.46) gives

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + \frac{1}{A_0} \left(1 + \frac{R_2}{R_1}\right) + \frac{s}{\omega_t/(1 + R_2/R_1)}} \quad (2.51)$$

For  $A_0 \gg 1 + R_2/R_1$ , which is usually the case,

$$\frac{V_o(s)}{V_i(s)} \approx \frac{-R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}} \quad (2.52)$$

which is of the same form as that for a low-pass STC network (see Table 1.2, page 34). Thus the inverting amplifier has an STC low-pass response with a dc gain of magnitude equal to  $R_2/R_1$ . The closed-loop gain rolls off at a uniform  $-20$ -dB/decade slope with a corner frequency (3-dB frequency) given by

$$\omega_{3\text{dB}} = \frac{\omega_t}{1 + R_2/R_1} \quad (2.53)$$

Similarly, analysis of the noninverting amplifier of Fig. 2.12, assuming a finite open-loop gain  $A$ , yields the closed-loop transfer function

$$\frac{V_o}{V_i} = \frac{1 + R_2/R_1}{1 + (1 + R_2/R_1)/A} \quad (2.54)$$

Substituting for  $A$  from Eq. (2.42) and making the approximation  $A_0 \gg 1 + R_2/R_1$  results in

$$\frac{V_o(s)}{V_i(s)} \approx \frac{1 + R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}} \quad (2.55)$$

Thus the noninverting amplifier has an STC low-pass response with a dc gain of  $(1 + R_2/R_1)$  and a 3-dB frequency given also by Eq. (2.53).

## Example 2.6

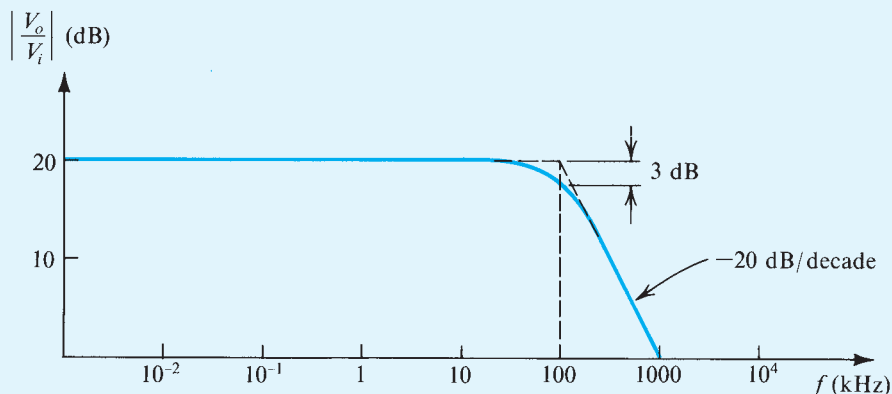
Consider an op amp with  $f_t = 1$  MHz. Find the 3-dB frequency of closed-loop amplifiers with nominal gains of +1000, +100, +10, +1, -1, -10, -100, and -1000. Sketch the magnitude frequency response for the amplifiers with closed-loop gains of +10 and -10.

### Solution

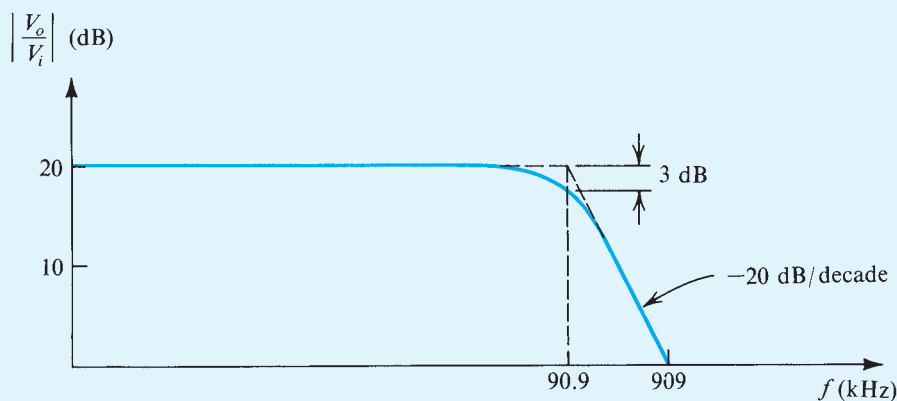
We use Eq. (2.53) to obtain the results given in the following table.

Closed-Loop Gain	$R_2/R_1$	$f_{3\text{dB}} = f_t / (1 + R_2/R_1)$
+1000	999	1 kHz
+100	99	10 kHz
+10	9	100 kHz
+1	0	1 MHz
-1	1	0.5 MHz
-10	10	90.9 kHz
-100	100	9.9 kHz
-1000	1000	$\approx 1$ kHz

Figure 2.40 shows the frequency response for the amplifier whose nominal dc gain is +10 (20 dB), and Fig. 2.41 shows the frequency response for the  $-10$  (also 20 dB) case. An interesting observation follows from the table above: The unity-gain inverting amplifier has a 3-dB frequency of  $f_i/2$  as compared to  $f_i$  for the unity-gain noninverting amplifier (the unity-gain voltage follower).



**Figure 2.40** Frequency response of an amplifier with a nominal gain of +10 V/V.



**Figure 2.41** Frequency response of an amplifier with a nominal gain of  $-10$  V/V.

The table in Example 2.6 above clearly illustrates the trade-off between gain and bandwidth: For a given op amp, the lower the closed-loop gain required, the wider the bandwidth achieved. Indeed, the noninverting configuration exhibits a constant **gain–bandwidth product** equal to  $f_i$  of the op amp. An interpretation of these results in terms of feedback theory will be given in Chapter 10.

## EXERCISES

**2.27** An internally compensated op amp has a dc open-loop gain of  $10^6$  V/V and an ac open-loop gain of 40 dB at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, its gain–bandwidth product, and its expected gain at 1 kHz.

**Ans.** 1 Hz; 1 MHz; 1 MHz; 60 dB

**2.28** An op amp having a 106-dB gain at dc and a single-pole frequency response with  $f_t = 2$  MHz is used to design a noninverting amplifier with nominal dc gain of 100. Find the 3-dB frequency of the closed-loop gain.

**Ans.** 20 kHz

## 2.8 Large-Signal Operation of Op Amps

In this section, we study the limitations on the performance of op-amp circuits when large output signals are present.

### 2.8.1 Output Voltage Saturation

Similar to all other amplifiers, op amps operate linearly over a limited range of output voltages. Specifically, the op-amp output saturates in the manner shown in Fig. 1.14 with  $L_+$  and  $L_-$  within 1 V or so of the positive and negative power supplies, respectively. Thus, an op amp that is operating from  $\pm 15$ -V supplies will saturate when the output voltage reaches about +13 V in the positive direction and –13 V in the negative direction. For this particular op amp the **rated output voltage** is said to be  $\pm 13$  V. To avoid clipping off the peaks of the output waveform, and the resulting waveform distortion, the input signal must be kept correspondingly small.

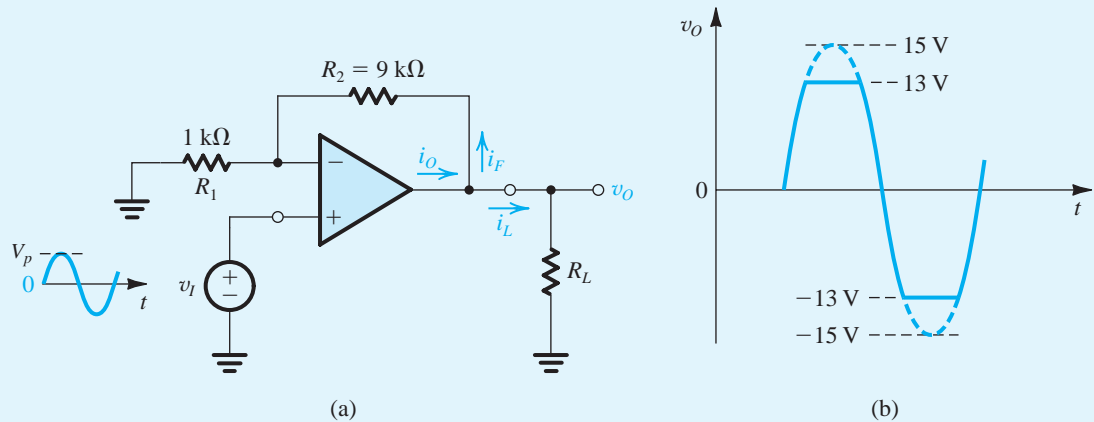
### 2.8.2 Output Current Limits

Another limitation on the operation of op amps is that their output current is limited to a specified maximum. For instance, the popular 741 op amp is specified to have a maximum output current of  $\pm 20$  mA. Thus, in designing closed-loop circuits utilizing the 741, the designer has to ensure that under no condition will the op amp be required to supply an output current, in either direction, exceeding 20 mA. This, of course, has to include both the current in the feedback circuit as well as the current supplied to a load resistor. If the circuit requires a larger current, the op-amp output voltage will saturate at the level corresponding to the maximum allowed output current.

### Example 2.7

Consider the noninverting amplifier circuit shown in Fig. 2.42. As shown, the circuit is designed for a nominal gain  $(1 + R_2/R_1) = 10$  V/V. It is fed with a low-frequency sine-wave signal of peak voltage  $V_p$  and is connected to a load resistor  $R_L$ . The op amp is specified to have output saturation voltages of  $\pm 13$  V and output current limits of  $\pm 20$  mA.

- For  $V_p = 1$  V and  $R_L = 1$  k $\Omega$ , specify the signal resulting at the output of the amplifier.
- For  $V_p = 1.5$  V and  $R_L = 1$  k $\Omega$ , specify the signal resulting at the output of the amplifier.
- For  $R_L = 1$  k $\Omega$ , what is the maximum value of  $V_p$  for which an undistorted sine-wave output is obtained?
- For  $V_p = 1$  V, what is the lowest value of  $R_L$  for which an undistorted sine-wave output is obtained?



**Figure 2.42** (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at  $\pm 13$ -V output voltage and has  $\pm 20$ -mA output current limits. (b) When the input sine wave has a peak of 1.5 V, the output is clipped off at  $\pm 13$  V.

### Solution

- For  $V_p = 1$  V and  $R_L = 1$  k $\Omega$ , the output will be a sine wave with peak value of 10 V. This is lower than output saturation levels of  $\pm 13$  V, and thus the amplifier is not limited that way. Also, when the output is at its peak (10 V), the current in the load will be  $10 \text{ V} / 1 \text{ k}\Omega = 10 \text{ mA}$ , and the current in the feedback network will be  $10 \text{ V} / (9 + 1) \text{ k}\Omega = 1 \text{ mA}$ , for a total op-amp output current of 11 mA, well under its limit of 20 mA.
- Now if  $V_p$  is increased to 1.5 V, ideally the output would be a sine wave of 15-V peak. The op amp, however, will saturate at  $\pm 13$  V, thus clipping the sine-wave output at these levels. Let's next check on the op-amp output current: At 13-V output and  $R_L = 1$  k $\Omega$ ,  $i_L = 13 \text{ mA}$  and  $i_F = 1.3 \text{ mA}$ ; thus  $i_o = 14.3 \text{ mA}$ , again under the 20-mA limit. Thus the output will be a sine wave with its peaks clipped off at  $\pm 13$  V, as shown in Fig. 2.42(b).

**Example 2.7** *continued*

- (c) For  $R_L = 1 \text{ k}\Omega$ , the maximum value of  $V_p$  for undistorted sine-wave output is 1.3 V. The output will be a 13-V peak sine wave, and the op-amp output current at the peaks will be 14.3 mA.
- (d) For  $V_p = 1 \text{ V}$  and  $R_L$  reduced, the lowest value possible for  $R_L$  while the output is remaining an undistorted sine wave of 10-V peak can be found from

$$i_{O\max} = 20 \text{ mA} = \frac{10 \text{ V}}{R_{L\min}} + \frac{10 \text{ V}}{9 \text{ k}\Omega + 1 \text{ k}\Omega}$$

which results in

$$R_{L\min} = 526 \text{ }\Omega$$

### 2.8.3 Slew Rate

Another phenomenon that can cause nonlinear distortion when large output signals are present is slew-rate limiting. The name refers to the fact that there is a specific *maximum rate of change* possible at the output of a real op amp. This maximum is known as the **slew rate** (SR) of the op amp and is defined as



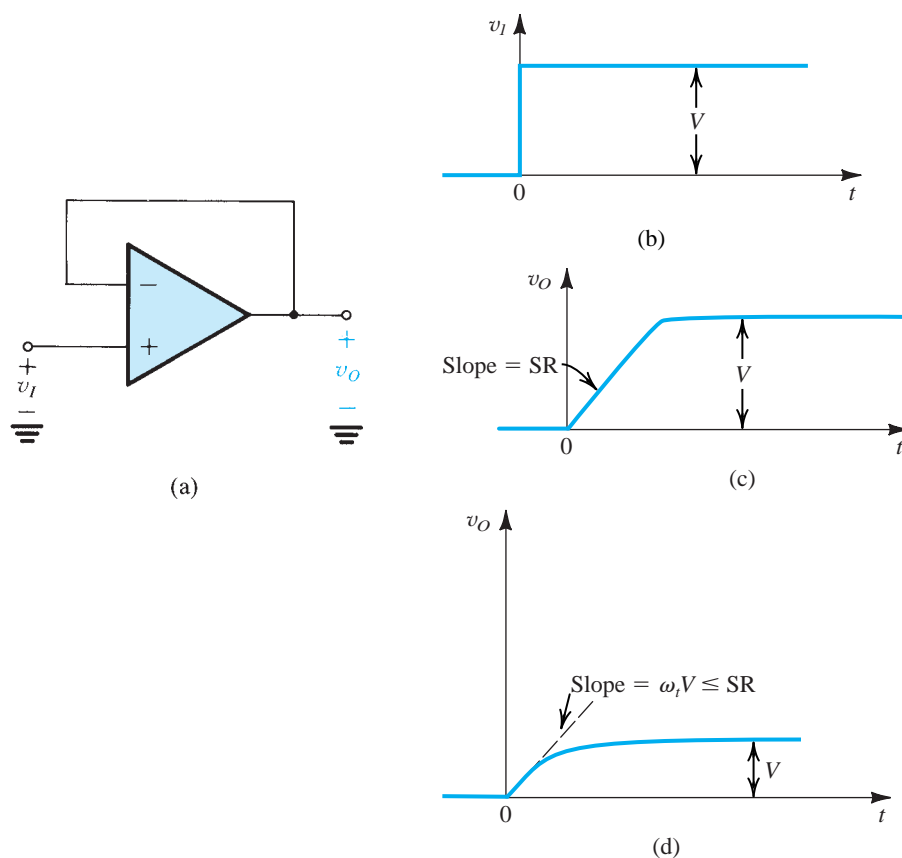
$$\text{SR} = \left. \frac{dv_o}{dt} \right|_{\max} \quad (2.56)$$

and is usually specified on the op-amp data sheet in units of V/ $\mu$ s. It follows that if the input signal applied to an op-amp circuit is such that it demands an output response that is faster than the specified value of SR, the op amp will not comply. Rather, its output will change at the maximum possible rate, which is equal to its SR. As an example, consider an op amp connected in the unity-gain voltage-follower configuration shown in Fig. 2.43(a), and let the input signal be the step voltage shown in Fig. 2.43(b). The output of the op amp will not be able to rise instantaneously to the ideal value  $V$ ; rather, the output will be the linear ramp of slope equal to SR, shown in Fig. 2.43(c). The amplifier is then said to be **slewing**, and its output is **slew-rate limited**.

In order to understand the origin of the slew-rate phenomenon, we need to know about the internal circuit of the op amp, and we will study it in Chapter 12. For the time being, however, it is sufficient to know about the phenomenon and to note that it is distinct from the finite op-amp bandwidth that limits the frequency response of the closed-loop amplifiers, studied in the previous section. The limited bandwidth is a linear phenomenon and does not result in a change in the shape of an input sinusoid; that is, it does not lead to nonlinear distortion. The slew-rate limitation, on the other hand, can cause nonlinear distortion to an input sinusoidal signal when its frequency and amplitude are such that the corresponding ideal output would require  $v_o$  to change at a rate greater than SR. This is the origin of another related op-amp specification, its full-power bandwidth, to be explained later.

Before leaving the example in Fig. 2.43, however, we should point out that if the step input voltage  $V$  is sufficiently small, the output can be the exponentially rising ramp shown in Fig. 2.43(d). Such an output would be expected from the follower if the only limitation on its dynamic performance were the finite op-amp bandwidth. Specifically, the transfer function of the follower can be found by substituting  $R_1 = \infty$  and  $R_2 = 0$  in Eq. (2.55) to obtain

$$\frac{V_o}{V_i} = \frac{1}{1 + s/\omega_t} \quad (2.57)$$



**Figure 2.43** (a) Unity-gain follower. (b) Input step waveform. (c) Linearly rising output waveform obtained when the amplifier is slew-rate limited. (d) Exponentially rising output waveform obtained when  $V$  is sufficiently small so that the initial slope ( $\omega_t V$ ) is smaller than or equal to  $SR$ .

which is a low-pass STC response with a time constant  $1/\omega_t$ . Its step response would therefore be (see Appendix E)

$$v_O(t) = V(1 - e^{-\omega_t t}) \quad (2.58)$$

The initial slope of this exponentially rising function is ( $\omega_t V$ ). Thus, as long as  $V$  is sufficiently small so that  $\omega_t V \leq SR$ , the output will be as in Fig. 2.43(d).

## EXERCISE

**2.29** An op amp that has a slew rate of  $1 \text{ V}/\mu\text{s}$  and a unity-gain bandwidth  $f_t$  of  $1 \text{ MHz}$  is connected in the unity-gain follower configuration. Find the largest possible input voltage step for which the output waveform will still be given by the exponential ramp of Eq. (2.58). For this input voltage, what is the 10% to 90% rise time of the output waveform? If an input step 10 times as large is applied, find the 10% to 90% rise time of the output waveform.

**Ans.**  $0.16 \text{ V}$ ;  $0.35 \mu\text{s}$ ;  $1.28 \mu\text{s}$

### 2.8.4 Full-Power Bandwidth

Op-amp slew-rate limiting can cause nonlinear distortion in sinusoidal waveforms. Consider once more the unity-gain follower with a sine-wave input given by

$$v_i = \hat{V}_i \sin \omega t$$

The rate of change of this waveform is given by

$$\frac{dv_i}{dt} = \omega \hat{V}_i \cos \omega t$$

with a maximum value of  $\omega \hat{V}_i$ . This maximum occurs at the zero crossings of the input sinusoid. Now if  $\omega \hat{V}_i$  exceeds the slew rate of the op amp, the output waveform will be distorted in the manner shown in Fig. 2.44. Observe that the output cannot keep up with the large rate of change of the sinusoid at its zero crossings, and the op amp slews.

The op-amp data sheets usually specify a frequency  $f_M$  called the **full-power bandwidth**. It is the frequency at which an output sinusoid with amplitude equal to the rated output voltage of the op amp begins to show distortion due to slew-rate limiting. If we denote the rated output voltage  $V_{o\max}$ , then  $f_M$  is related to SR as follows:

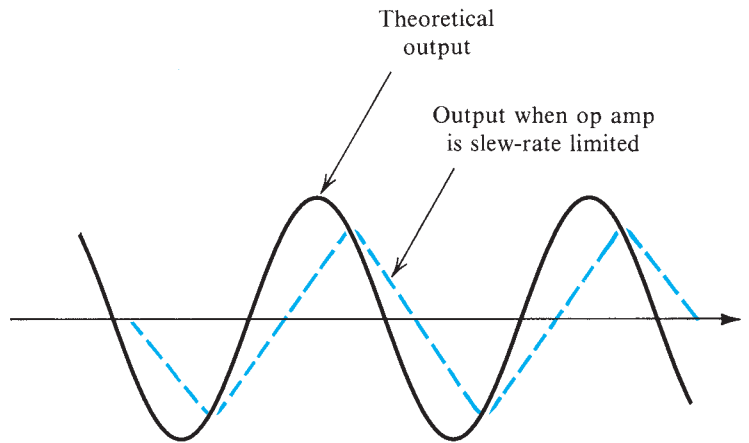
$$\omega_M V_{o\max} = \text{SR}$$

Thus,

$$\text{I} \quad f_M = \frac{\text{SR}}{2\pi V_{o\max}} \quad (2.59)$$

It should be obvious that output sinusoids of amplitudes smaller than  $V_{o\max}$  will show slew-rate distortion at frequencies higher than  $\omega_M$ . In fact, at a frequency  $\omega$  higher than  $\omega_M$ , the maximum amplitude of the undistorted output sinusoid is given by

$$\text{I} \quad V_o = V_{o\max} \left( \frac{\omega_M}{\omega} \right) \quad (2.60)$$



**Figure 2.44** Effect of slew-rate limiting on output sinusoidal waveforms.

## EXERCISE

**2.30** An op amp has a rated output voltage of  $\pm 10$  V and a slew rate of  $1$  V/ $\mu$ s. What is its full-power bandwidth? If an input sinusoid with frequency  $f = 5f_M$  is applied to a unity-gain follower constructed using this op amp, what is the maximum possible amplitude that can be accommodated at the output without incurring SR distortion?

**Ans.** 15.9 kHz; 2 V (peak)

## Summary

- The IC op amp is a versatile circuit building block. It is easy to apply, and the performance of op-amp circuits closely matches theoretical predictions.
- The op-amp terminals are the inverting input terminal (1), the noninverting input terminal (2), the output terminal (3), the positive-supply terminal (4) to be connected to the positive power supply ( $V_{CC}$ ), and the negative-supply terminal (5) to be connected to the negative supply ( $-V_{EE}$ ). The common terminal of the two supplies is the circuit ground.
- The ideal op amp responds only to the difference input signal, that is,  $(v_2 - v_1)$ ; providing at the output, between terminal 3 and ground, a signal  $A(v_2 - v_1)$ , where  $A$ , the open-loop gain, is very large ( $10^4$  to  $10^6$ ) and ideally infinite; and has an infinite input resistance and a zero output resistance. (See Table 3.1.)
- Negative feedback is applied to an op amp by connecting a passive component between its output terminal and its inverting (negative) input terminal. Negative feedback causes the voltage between the two input terminals to become very small and ideally zero. Correspondingly, a virtual short circuit is said to exist between the two input terminals. If the positive input terminal is connected to ground, a virtual ground appears on the negative input terminal.
- The two most important assumptions in the analysis of op-amp circuits, presuming negative feedback exists and the op amps are ideal, are as follows: the two input terminals of the op amp are at the same voltage, and zero current flows into the op-amp input terminals.
- With negative feedback applied and the loop closed, the closed-loop gain is almost entirely determined by external components: For the inverting configuration,  $V_o/V_i = -R_2/R_1$ ; and for the noninverting configuration,  $V_o/V_i = 1 + R_2/R_1$ .
- The noninverting closed-loop configuration features a very high input resistance. A special case is the unity-gain follower, frequently employed as a buffer amplifier to connect a high-resistance source to a low-resistance load.
- The difference amplifier of Fig. 2.16 is designed with  $R_4/R_3 = R_2/R_1$ , resulting in  $v_o = (R_2/R_1)(v_{I2} - v_{I1})$ .
- The instrumentation amplifier of Fig. 2.20(b) is a very popular circuit. It provides  $v_o = (1 + R_2/R_1)(R_4/R_3)(v_{I2} - v_{I1})$ . It is usually designed with  $R_3 = R_4$ , and  $R_1$  and  $R_2$  selected to provide the required gain. If an adjustable gain is needed, part of  $R_1$  can be made variable.
- The inverting Miller integrator of Fig. 2.24 is a popular circuit, frequently employed in analog signal-processing functions such as filters (Chapter 16) and oscillators (Chapter 17).
- The input offset voltage,  $V_{OS}$ , is the magnitude of dc voltage that when applied between the op amp input terminals, with appropriate polarity, reduces the dc offset voltage at the output to zero.
- The effect of  $V_{OS}$  on performance can be evaluated by including in the analysis a dc source  $V_{OS}$  in series with the op-amp positive input lead. For both the inverting and the noninverting configurations,  $V_{OS}$  results in a dc offset voltage at the output of  $V_{OS}(1 + R_2/R_1)$ .
- Capacitively coupling an op amp reduces the dc offset voltage at the output considerably.
- The average of the two dc currents,  $I_{B1}$  and  $I_{B2}$ , that flow in the input terminals of the op amp, is called the input bias current,  $I_B$ . In a closed-loop amplifier,  $I_B$  gives rise to a dc offset voltage at the output of magnitude  $I_B R_2$ . This voltage can be reduced to  $I_{OS} R_2$  by connecting a resistance in series with the positive input terminal equal to the total dc resistance seen by the negative input terminal.  $I_{OS}$  is the input offset current; that is,  $I_{OS} = |I_{B1} - I_{B2}|$ .



- Connecting a large resistance in parallel with the capacitor of an op-amp inverting integrator prevents op-amp saturation (due to the effect of  $V_{OS}$  and  $I_B$ ).
- For most internally compensated op amps, the open-loop gain falls off with frequency at a rate of  $-20$  dB/decade, reaching unity at a frequency  $f_t$  (the unity-gain bandwidth). Frequency  $f_t$  is also known as the gain–bandwidth product of the op amp:  $f_t = A_0 f_b$ , where  $A_0$  is the dc gain, and  $f_b$  is the 3-dB frequency of the open-loop gain. At any frequency  $f$  ( $f \gg f_b$ ), the op-amp gain  $|A| \approx f_t/f$ .
- For both the inverting and the noninverting closed-loop configurations, the 3-dB frequency is equal to  $f_t/(1 + R_2/R_1)$ .
- The maximum rate at which the op-amp output voltage can change is called the slew rate. The slew rate, SR, is usually specified in V/ $\mu$ s. Op-amp slewing can result in nonlinear distortion of output signal waveforms.
- The full-power bandwidth,  $f_M$ , is the maximum frequency at which an output sinusoid with an amplitude equal to the op-amp rated output voltage ( $V_{Omax}$ ) can be produced without distortion:  $f_M = SR/2\pi V_{Omax}$ .

## PROBLEMS

### Computer Simulation Problems

**SIM** Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multism simulations for all the indicated problems can be found in the corresponding files on the disc. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption. \* difficult problem; \*\* more difficult; \*\*\* very challenging and/or time-consuming; D: design problem.

### Section 2.1: The Ideal Op Amp

**2.1** What is the minimum number of pins required for a so-called dual-op-amp IC package, one containing two op amps? What is the number of pins required for a so-called quad-op-amp package, one containing four op-amps?

**2.2** The circuit of Fig. P2.2 uses an op amp that is ideal except for having a finite gain  $A$ . Measurements indicate  $v_o = 4.0$  V when  $v_i = 2.0$  V. What is the op-amp gain  $A$ ?

**2.3** Measurement of a circuit incorporating what is thought to be an ideal op amp shows the voltage at the op-amp output to be  $-2.000$  V and that at the negative input to be  $-1.000$  V. For the amplifier to be ideal, what would you expect the voltage at the positive input to be? If the measured voltage at the positive input is  $-1.010$  V, what is likely to be the actual gain of the amplifier?

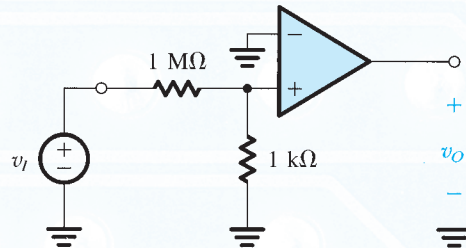


Figure P2.2

**2.4** A set of experiments is run on an op amp that is ideal except for having a finite gain  $A$ . The results are tabulated below. Are the results consistent? If not, are they reasonable, in view of the possibility of experimental error? What do they show the gain to be? Using this value, predict values of the measurements that were accidentally omitted (the blank entries).

Experiment #	$v_1$	$v_2$	$v_o$
1	0.00	0.00	0.00
2	1.00	1.00	0.00
3		1.00	1.00
4	1.00	1.10	10.1
5	2.01	2.00	-0.99
6	1.99	2.00	1.00
7	5.10		-5.10

**2.5** Refer to Exercise 2.3. This problem explores an alternative internal structure for the op amp. In particular, we wish to model the internal structure of a particular op amp using two transconductance amplifiers and one transresistance amplifier. Suggest an appropriate topology. For equal transconductances  $G_m$  and a transresistance  $R_m$ , find an expression for the open-loop gain  $A$ . For  $G_m = 10 \text{ mA/V}$  and  $R_m = 2 \times 10^6 \Omega$ , what value of  $A$  results?

**2.6** The two wires leading from the output terminals of a transducer pick up an interference signal that is a 60-Hz, 1-V sinusoid. The output signal of the transducer is sinusoidal of 10-mV amplitude and 1000-Hz frequency. Give expressions for  $v_{cm}$ ,  $v_d$ , and the total signal between each wire and the system ground.

**2.7** Nonideal (i.e., real) operational amplifiers respond to both the differential and common-mode components of their input signals (refer to Fig. 2.4 for signal representation). Thus the output voltage of the op amp can be expressed as

$$v_o = A_d v_{id} + A_{cm} v_{icm}$$

where  $A_d$  is the differential gain (referred to simply as  $A$  in the text) and  $A_{cm}$  is the common-mode gain (assumed to be zero in the text). The op amp's effectiveness in rejecting common-mode signals is measured by its CMRR, defined as

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Consider an op amp whose internal structure is of the type shown in Fig. E2.3 except for a mismatch  $\Delta G_m$  between the transconductances of the two channels; that is,

$$G_{m1} = G_m - \frac{1}{2} \Delta G_m$$

$$G_{m2} = G_m + \frac{1}{2} \Delta G_m$$

Find expressions for  $A_d$ ,  $A_{cm}$ , and CMRR. If  $A_d$  is 80 dB and the two transconductances are matched to within 0.1% of each other, calculate  $A_{cm}$  and CMRR.

## Section 2.2: The Inverting Configuration

**2.8** Assuming ideal op amps, find the voltage gain  $v_o/v_i$  and input resistance  $R_{in}$  of each of the circuits in Fig. P2.8.

**2.9** A particular inverting circuit uses an ideal op amp and two 10-k $\Omega$  resistors. What closed-loop gain would you expect? If a dc voltage of +1.00 V is applied at the input, what output result? If the 10-k $\Omega$  resistors are said to be "1% resistors," having values somewhere in the range  $(1 \pm 0.01)$  times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 1.00 V?

**2.10** You are provided with an ideal op amp and three 10-k $\Omega$  resistors. Using series and parallel resistor combinations, how many different inverting-amplifier circuit topologies are possible? What is the largest (noninfinite) available voltage

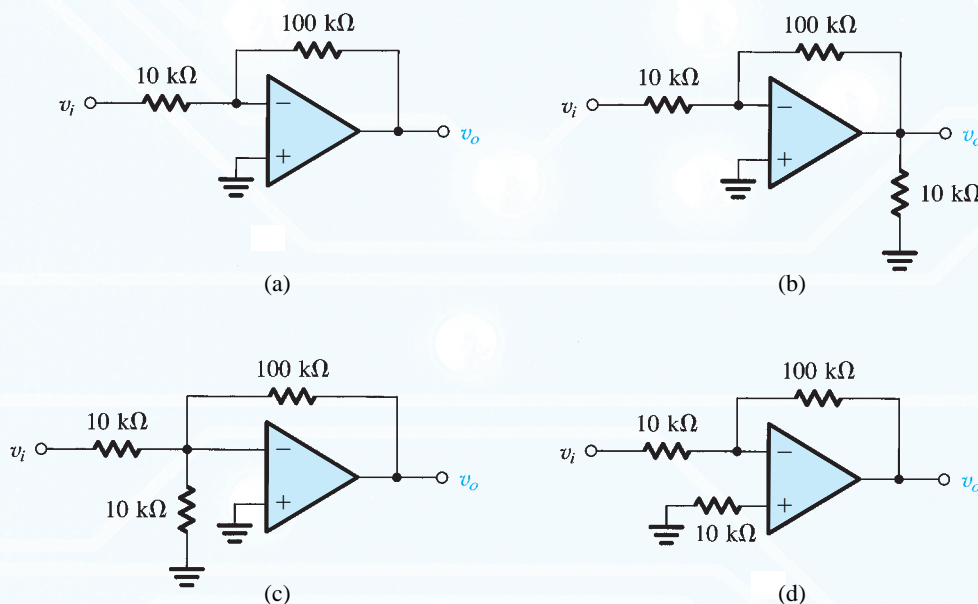


Figure P2.8



## 110 Chapter 2 Operational Amplifiers

gain? What is the smallest (nonzero) available gain? What are the input resistances in these two cases?

**SIM 2.11** For ideal op amps operating with the following feedback networks in the inverting configuration, what closed-loop gain results?

- (a)  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$
- (b)  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 100 \text{ k}\Omega$
- (c)  $R_1 = 10 \text{ k}\Omega$ ,  $R_2 = 1 \text{ k}\Omega$
- (d)  $R_1 = 100 \text{ k}\Omega$ ,  $R_2 = 10 \text{ M}\Omega$
- (e)  $R_1 = 100 \text{ k}\Omega$ ,  $R_2 = 1 \text{ M}\Omega$

**D 2.12** Given an ideal op amp, what are the values of the resistors  $R_1$  and  $R_2$  to be used to design amplifiers with the closed-loop gains listed below? In your designs, use at least one  $10\text{-k}\Omega$  resistor and another equal or larger resistor.

- (a)  $-1 \text{ V/V}$
- (b)  $-2 \text{ V/V}$
- (c)  $-0.5 \text{ V/V}$
- (d)  $-100 \text{ V/V}$

**D 2.13** Design an inverting op-amp circuit for which the gain is  $-4 \text{ V/V}$  and the total resistance used is  $100 \text{ k}\Omega$ .

**D 2.14** Using the circuit of Fig. 2.5 and assuming an ideal op amp, design an inverting amplifier with a gain of  $26 \text{ dB}$  having the largest possible input resistance under the constraint of having to use resistors no larger than  $1 \text{ M}\Omega$ . What is the input resistance of your design?

**2.15** An ideal op amp is connected as shown in Fig. 2.5 with  $R_1 = 10 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$ . A symmetrical square-wave signal with levels of  $0 \text{ V}$  and  $1 \text{ V}$  is applied at the input. Sketch and clearly label the waveform of the resulting output voltage. What is its average value? What is its highest value? What is its lowest value?

**2.16** For the circuit in Fig. P2.16, assuming an ideal op amp, find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

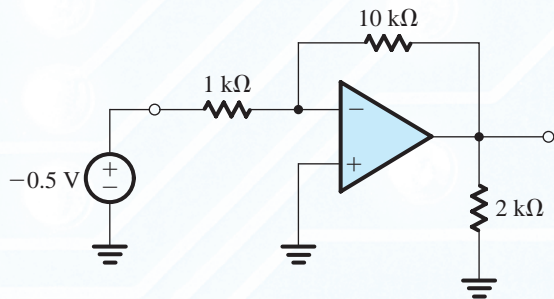


Figure P2.16

**2.17** An inverting op-amp circuit is fabricated with the resistors  $R_1$  and  $R_2$  having  $x\%$  tolerance (i.e., the value of each resistance can deviate from the nominal value by as much as  $\pm x\%$ ). What is the tolerance on the realized closed-loop gain? Assume the op amp to be ideal. If the nominal closed-loop gain is  $-100 \text{ V/V}$  and  $x = 1$ , what is the range of gain values expected from such a circuit?

**2.18** An ideal op amp with  $5\text{-k}\Omega$  and  $15\text{-k}\Omega$  resistors is used to create a  $+5\text{-V}$  supply from a  $-15\text{-V}$  reference. Sketch the circuit. What are the voltages at the ends of the  $5\text{-k}\Omega$  resistor? If these resistors are so-called  $1\%$  resistors, whose actual values are the range bounded by the nominal value  $\pm 1\%$ , what are the limits of the output voltage produced? If the  $-15\text{-V}$  supply can also vary by  $\pm 1\%$ , what is the range of the output voltages that might be found?

**2.19** An inverting op-amp circuit for which the required gain is  $-50 \text{ V/V}$  uses an op amp whose open-loop gain is only  $300 \text{ V/V}$ . If the larger resistor used is  $100 \text{ k}\Omega$ , to what must the smaller be adjusted? With what resistor must a  $2\text{-k}\Omega$  resistor connected to the input be shunted to achieve this goal? (Note that a resistor  $R_a$  is said to be shunted by resistor  $R_b$  when  $R_b$  is placed in parallel with  $R_a$ .)

**D 2.20** (a) Design an inverting amplifier with a closed-loop gain of  $-100 \text{ V/V}$  and an input resistance of  $1 \text{ k}\Omega$ .

(b) If the op amp is known to have an open-loop gain of  $2000 \text{ V/V}$ , what do you expect the closed-loop gain of your circuit to be (assuming the resistors have precise values)?

(c) Give the value of a resistor you can place in parallel (shunt) with  $R_1$  to restore the closed-loop gain to its nominal value. Use the closest standard  $1\%$  resistor value (see Appendix H).

**2.21** An op amp with an open-loop gain of  $2000 \text{ V/V}$  is used in the inverting configuration. If in this application the output voltage ranges from  $-10 \text{ V}$  to  $+10 \text{ V}$ , what is the maximum voltage by which the “virtual ground node” departs from its ideal value?

**2.22** The circuit in Fig. P2.22 is frequently used to provide an output voltage  $v_o$  proportional to an input signal current  $i_i$ .

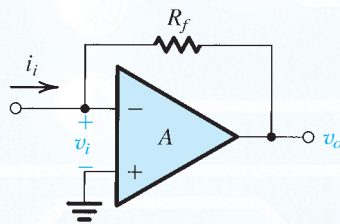


Figure P2.22

Derive expressions for the transresistance  $R_m \equiv v_o/i_i$  and the input resistance  $R_i \equiv v_i/i_i$  for the following cases:

- (a)  $A$  is infinite.
- (b)  $A$  is finite.

**2.23** Show that for the inverting amplifier if the op-amp gain is  $A$ , the input resistance is given by

$$R_{in} = R_1 + \frac{R_2}{A + 1}$$

**\*2.24** For an inverting amplifier with nominal closed-loop gain  $R_2/R_1$ , find the minimum value that the op-amp open-loop gain  $A$  must have (in terms of  $R_2/R_1$ ) so that the gain error is limited to 0.1%, 1%, and 10%. In each case find the value of a resistor  $R_{ia}$  such that when it is placed in shunt with  $R_i$ , the gain is restored to its nominal value.

**\*2.25** Figure P2.25 shows an op amp that is ideal except for having a finite open-loop gain and is used to realize an inverting amplifier whose gain has a nominal magnitude  $G = R_2/R_1$ . To compensate for the gain reduction due to the finite  $A$ , a resistor  $R_c$  is shunted across  $R_1$ . Show that perfect compensation is achieved when  $R_c$  is selected according to

$$\frac{R_c}{R_1} = \frac{A - G}{1 + G}$$

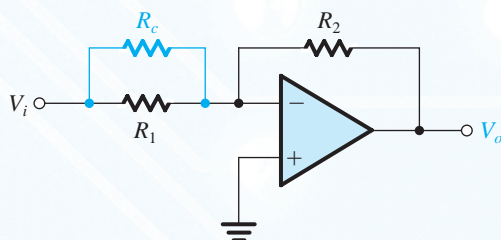


Figure P2.25

**\*D 2.26** (a) Use Eq. (2.5) to obtain the amplifier open-loop gain  $A$  required to realize a specified closed-loop gain ( $G_{\text{nominal}} = -R_2/R_1$ ) within a specified gain error  $\varepsilon$ ,

$$\varepsilon \equiv \left| \frac{G - G_{\text{nominal}}}{G_{\text{nominal}}} \right|$$

(b) Design an inverting amplifier for a nominal closed-loop gain of  $-100$ , an input resistance of  $2 \text{ k}\Omega$ , and a gain error of  $\leq 10\%$ . Specify  $R_1$ ,  $R_2$ , and the minimum  $A$  required.

**\*2.27** (a) Use Eq. (2.5) to show that a reduction  $\Delta A$  in the op-amp gain  $A$  gives rise to a reduction  $\Delta|G|$  in the magnitude of the closed-loop gain  $G$  with  $\Delta|G|$  and  $\Delta A$  related by

$$\frac{\Delta|G|/|G|}{\Delta A/A} = \frac{1 + R_2/R_1}{A}$$

(b) If in a closed-loop amplifier with a nominal gain (i.e.,  $R_2/R_1$ ) of  $100$ ,  $A$  decreases by  $50\%$ , what is the minimum nominal  $A$  required to limit the percentage change in  $|G|$  to  $0.5\%$ ?

**2.28** Consider the circuit in Fig. 2.8 with  $R_1 = R_2 = R_4 = 1 \text{ M}\Omega$ , and assume the op amp to be ideal. Find values for  $R_3$  to obtain the following gains:

- (a)  $-200 \text{ V/V}$
- (b)  $-20 \text{ V/V}$
- (c)  $-2 \text{ V/V}$

**D 2.29** An inverting op-amp circuit using an ideal op amp must be designed to have a gain of  $-1000 \text{ V/V}$  using resistors no larger than  $100 \text{ k}\Omega$ .

- (a) For the simple two-resistor circuit, what input resistance would result?
- (b) If the circuit in Fig. 2.8 is used with three resistors of maximum value, what input resistance results? What is the value of the smallest resistor needed?

**2.30** The inverting circuit with the T network in the feedback is redrawn in Fig. P2.30 in a way that emphasizes the observation that  $R_2$  and  $R_3$  in effect are in parallel (because the ideal op amp forces a virtual ground at the inverting input terminal). Use this observation to derive an expression for the gain ( $v_o/v_i$ ) by first finding ( $v_x/v_i$ ) and ( $v_o/v_x$ ). For the latter use the voltage-divider rule applied to  $R_4$  and ( $R_2 \parallel R_3$ ).

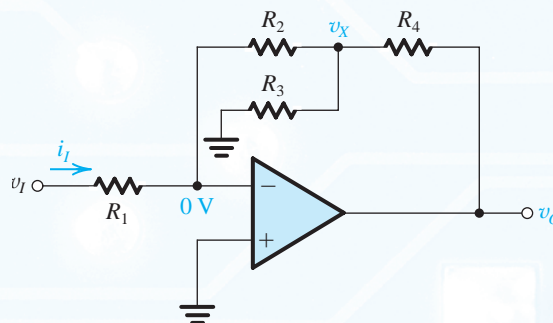


Figure P2.30

**\*2.31** The circuit in Fig. P2.31 can be considered to be an extension of the circuit in Fig. 2.8.

- (a) Find the resistances looking into node 1,  $R_1$ ; node 2,  $R_2$ ; node 3,  $R_3$ ; and node 4,  $R_4$ .
- (b) Find the currents  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_4$ , in terms of the input current  $I$ .
- (c) Find the voltages at nodes 1, 2, 3, and 4, that is,  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  in terms of ( $IR$ ).



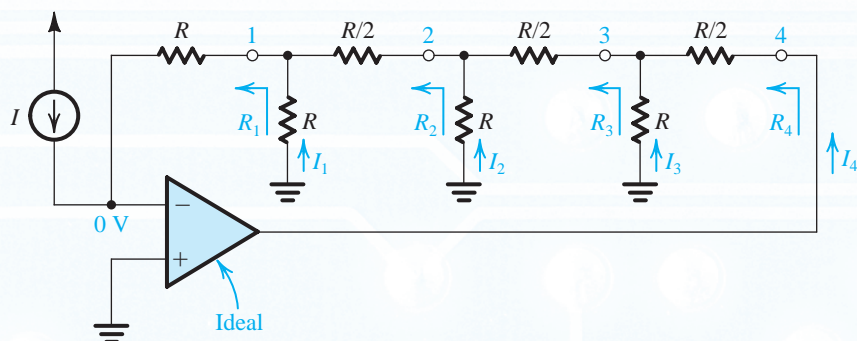


Figure P2.31

**2.32** The circuit in Fig. P2.32 utilizes an ideal op amp.

- Find  $I_1$ ,  $I_2$ ,  $I_3$ ,  $I_L$ , and  $V_x$ .
- If  $V_o$  is not to be lower than  $-13$  V, find the maximum allowed value for  $R_L$ .
- If  $R_L$  is varied in the range  $100\ \Omega$  to  $1\text{ k}\Omega$ , what is the corresponding change in  $I_L$  and in  $V_o$ ?

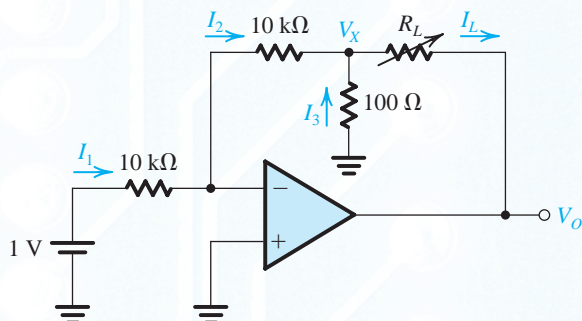


Figure P2.32

**2.33** Use the circuit in Fig. P2.32 as an inspiration to design a circuit that supplies a constant current  $I$  of  $3.1\text{ mA}$  to a variable resistance  $R_L$ . Assume the availability of a  $1.5\text{ V}$  battery and design so that the current drawn from the battery is  $0.1\text{ mA}$ . For the smallest resistance in the circuit, use  $500\ \Omega$ . If the op amp saturates at  $\pm 12\text{ V}$ , what is the maximum value that  $R_L$  can have while the current-source supplying it operates properly?

**D 2.34** Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.34 to implement a current amplifier with gain  $i_L/i_I = 10\text{ A/A}$ .

- Find the required value for  $R$ .
- What are the input and the output resistance of this current amplifier?

- If  $R_L = 1\text{ k}\Omega$  and the op amp operates in an ideal manner as long as  $v_o$  is in the range  $\pm 12\text{ V}$ , what range of  $i_I$  is possible?
- If the amplifier is fed with a current source having a current of  $0.2\text{ mA}$  and a source resistance of  $10\text{ k}\Omega$ , find  $i_L$ .

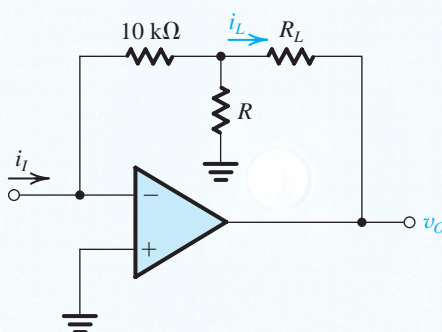


Figure P2.34

**D 2.35** Design the circuit shown in Fig. P2.35 to have an input resistance of  $100\text{ k}\Omega$  and a gain that can be varied

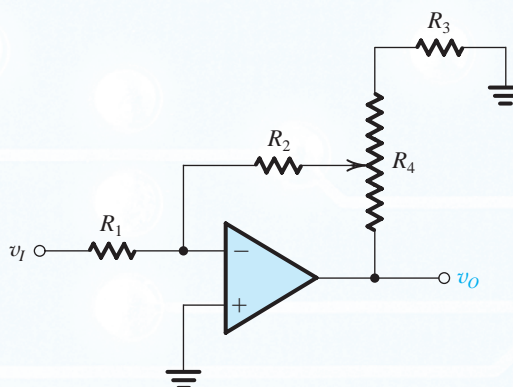


Figure P2.35

from  $-1$  V/V to  $-10$  V/V using the  $10\text{-k}\Omega$  potentiometer  $R_1$ . What voltage gain results when the potentiometer is set exactly at its middle value?

**2.36** A weighted summer circuit using an ideal op amp has three inputs using  $100\text{-k}\Omega$  resistors and a feedback resistor of  $50\text{ k}\Omega$ . A signal  $v_1$  is connected to two of the inputs while a signal  $v_2$  is connected to the third. Express  $v_o$  in terms of  $v_1$  and  $v_2$ . If  $v_1 = 2$  V and  $v_2 = -2$  V, what is  $v_o$ ?

**D 2.37** Design an op amp circuit to provide an output  $v_o = -[2v_1 + (v_2/2)]$ . Choose relatively low values of resistors but ones for which the input current (from each input signal source) does not exceed  $0.1$  mA for  $1\text{-V}$  input signals.

**D 2.38** Use the scheme illustrated in Fig. 2.10 to design an op-amp circuit with inputs  $v_1$ ,  $v_2$ , and  $v_3$ , whose output is  $v_o = -(2v_1 + 4v_2 + 8v_3)$  using small resistors but no smaller than  $10\text{ k}\Omega$ .

**D 2.39** An ideal op amp is connected in the weighted summer configuration of Fig. 2.10. The feedback resistor  $R_f = 10\text{ k}\Omega$ , and six  $10\text{-k}\Omega$  resistors are connected to the inverting input terminal of the op amp. Show, by sketching the various circuit configurations, how this basic circuit can be used to implement the following functions:

- (a)  $v_o = -(v_1 + 2v_2 + 3v_3)$
- (b)  $v_o = -(v_1 + v_2 + 2v_3 + 2v_4)$
- (c)  $v_o = -(v_1 + 5v_2)$
- (d)  $v_o = -6v_1$

In each case find the input resistance seen by each of the signal sources supplying  $v_1$ ,  $v_2$ ,  $v_3$ , and  $v_4$ . Suggest at least two additional summing functions that you can realize with this circuit. How would you realize a summing coefficient that is  $0.5$ ?

**D 2.40** Give a circuit, complete with component values, for a weighted summer that shifts the dc level of a sine-wave signal of  $3 \sin(\omega t)$  V from zero to  $-3$  V. Assume that in addition to the sine-wave signal you have a dc reference voltage of  $1.5$  V available. Sketch the output signal waveform.

**D 2.41** Use two ideal op amps and resistors to implement the summing function

$$v_o = v_1 + 2v_2 - 3v_3 - 4v_4$$

**D \*2.42** In an instrumentation system, there is a need to take the difference between two signals, one of  $v_1 = 2 \sin(2\pi \times 60t) + 0.01 \sin(2\pi \times 1000t)$  volts and another of  $v_2 = 2 \sin(2\pi \times 60t) - 0.01 \sin(2\pi \times 1000t)$  volts. Draw a circuit that finds the required difference using two op amps and mainly  $100\text{-k}\Omega$  resistors. Since it is desirable to amplify the  $1000\text{-Hz}$  component in the process, arrange to provide an overall gain of  $100$  as well. The op amps

available are ideal except that their output voltage swing is limited to  $\pm 10$  V.

**\*2.43** Figure P2.43 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word  $a_3a_2a_1a_0$ , where  $a_0$ ,  $a_1$ ,  $a_2$ , and  $a_3$  take the values of  $0$  or  $1$ , and it provides an analog output voltage  $v_o$  proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if  $a_2$  is  $0$  then switch  $S_2$  connects the  $20\text{-k}\Omega$  resistor to ground, while if  $a_2$  is  $1$  then  $S_2$  connects the  $20\text{-k}\Omega$  resistor to the  $+5\text{-V}$  power supply. Show that  $v_o$  is given by

$$v_o = -\frac{R_f}{16}[2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3]$$

where  $R_f$  is in kilohms. Find the value of  $R_f$  so that  $v_o$  ranges from  $0$  to  $-12$  volts.

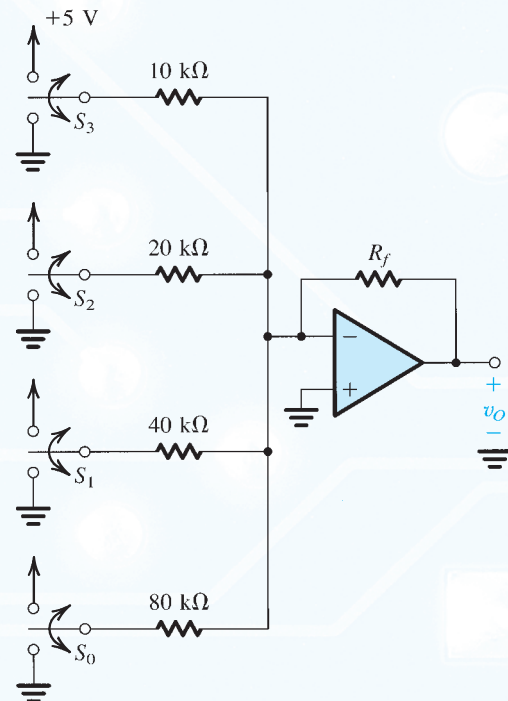


Figure P2.43

### Section 2.3: The Noninverting Configuration

**D 2.44** Given an ideal op amp to implement designs for the following closed-loop gains, what values of resistors ( $R_1$ ,  $R_2$ ) should be used? Where possible, use at least one  $10\text{-k}\Omega$  resistor as the smallest resistor in your design.



- (a) +1 V/V  
(b) +2 V/V  
(c) +11 V/V  
(d) +100 V/V

**D 2.45** Design a circuit based on the topology of the non-inverting amplifier to obtain a gain of +1.5 V/V, using only 10-k $\Omega$  resistors. Note that there are two possibilities. Which of these can be easily converted to have a gain of either +1.0 V/V or +2.0 V/V simply by short-circuiting a single resistor in each case?

**D 2.46** Figure P2.46 shows a circuit for an analog voltmeter of very high input resistance that uses an inexpensive moving-coil meter. The voltmeter measures the voltage  $V$  applied between the op amp's positive-input terminal and ground. Assuming that the moving coil produces full-scale deflection when the current passing through it is 100  $\mu$ A, find the value of  $R$  such that full-scale reading is obtained when  $V$  is +10 V. Does the meter resistance shown affect the voltmeter calibration?

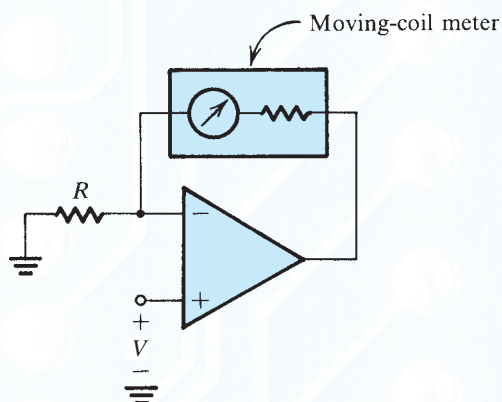


Figure P2.46

**D \*2.47** (a) Use superposition to show that the output of the circuit in Fig. P2.47 is given by

$$v_O = -\left[\frac{R_f}{R_{N1}}v_{N1} + \frac{R_f}{R_{N2}}v_{N2} + \cdots + \frac{R_f}{R_{Nn}}v_{Nn}\right] + \left[1 + \frac{R_f}{R_N}\right]\left[\frac{R_p}{R_{P1}}v_{P1} + \frac{R_p}{R_{P2}}v_{P2} + \cdots + \frac{R_p}{R_{Pn}}v_{Pn}\right]$$

where  $R_N = R_{N1} \parallel R_{N2} \parallel \cdots \parallel R_{Nn}$  and

$$R_p = R_{P1} \parallel R_{P2} \parallel \cdots \parallel R_{Pn} \parallel R_{P0}$$

(b) Design a circuit to obtain

$$v_O = -3v_{N1} + v_{P1} + 2v_{P2}$$

The smallest resistor used should be 10 k $\Omega$ .

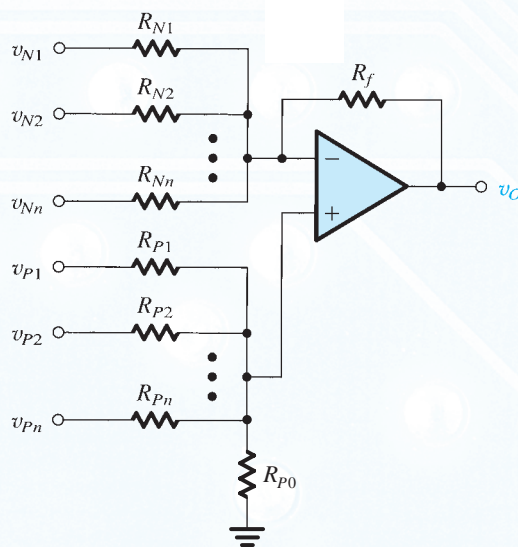


Figure P2.47

**D 2.48** Design a circuit, using one ideal op amp, whose output is  $v_O = v_1 + 3v_2 - 2(v_3 + 3v_4)$ . (Hint: Use a structure similar to that shown in general form in Fig. P2.47.)

**2.49** Derive an expression for the voltage gain,  $v_O/v_I$ , of the circuit in Fig. P2.49.

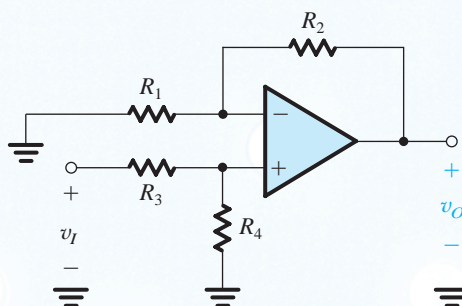


Figure P2.49

**2.50** For the circuit in Fig. P2.50, use superposition to find  $v_O$  in terms of the input voltages  $v_1$  and  $v_2$ . Assume an ideal op amp. For

$$v_1 = 10 \sin(2\pi \times 60t) - 0.1 \sin(2\pi \times 1000t), \text{ volts}$$

$$v_2 = 10 \sin(2\pi \times 60t) + 0.1 \sin(2\pi \times 1000t), \text{ volts}$$

find  $v_O$ .

**D 2.51** The circuit shown in Fig. P2.51 utilizes a 10-k $\Omega$  potentiometer to realize an adjustable-gain amplifier. Derive an expression for the gain as a function of the potentiometer

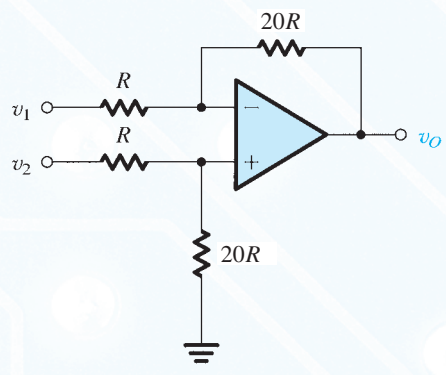


Figure P2.50

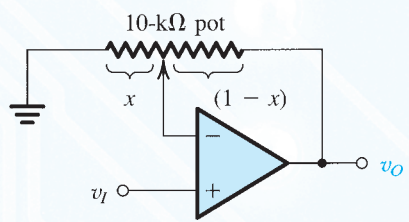


Figure P2.51

setting  $x$ . Assume the op amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range can be 1 to 11 V/V. What should the resistor value be?

**D 2.52** Given the availability of resistors of value 1 k $\Omega$  and 10 k $\Omega$  only, design a circuit based on the noninverting configuration to realize a gain of +10 V/V.

**2.53** It is required to connect a 10-V source with a source resistance of 100 k $\Omega$  to a 1-k $\Omega$  load. Find the voltage that will appear across the load if:

- (a) The source is connected directly to the load.
- (b) A unity-gain op-amp buffer is inserted between the source and the load.

In each case find the load current and the current supplied by the source. Where does the load current come from in case (b)?

**2.54** Derive an expression for the gain of the voltage follower of Fig. 2.14, assuming the op amp to be ideal except for having a finite gain  $A$ . Calculate the value of the closed-loop gain for  $A = 1000$ , 100, and 10. In each case find the percentage error in gain magnitude from the nominal value of unity.

**2.55** Complete the following table for feedback amplifiers created using one ideal op amp. Note that  $R_{in}$  signifies input resistance and  $R_1$  and  $R_2$  are feedback-network resistors as labelled in the inverting and noninverting configurations.

Case	Gain	$R_{in}$	$R_1$	$R_2$
a	−10 V/V	10 k $\Omega$		
b	−1 V/V		100 k $\Omega$	
c	−2 V/V			100 k $\Omega$
d	+1 V/V	$\infty$		
e	+2 V/V		10 k $\Omega$	
f	+11 V/V			100 k $\Omega$
g	−0.5 V/V	10 k $\Omega$		

**D 2.56** A noninverting op-amp circuit with nominal gain of 10 V/V uses an op amp with open-loop gain of 50 V/V and a lowest-value resistor of 10 k $\Omega$ . What closed-loop gain actually results? With what value resistor can which resistor be shunted to achieve the nominal gain? If in the manufacturing process, an op amp of gain 100 V/V were used, what closed-loop gain would result in each case (the uncompensated one, and the compensated one)?

**2.57** Use Eq. (2.11) to show that if the reduction in the closed-loop gain  $G$  from the nominal value  $G_0 = 1 + R_2/R_1$  is to be kept less than  $x\%$  of  $G_0$ , then the open-loop gain of the op amp must exceed  $G_0$  by at least a factor  $F = (100/x) - 1 \approx 100/x$ . Find the required  $F$  for  $x = 0.01$ , 0.1, 1, and 10. Utilize these results to find for each value of  $x$  the minimum required open-loop gain to obtain closed-loop gains of 1, 10,  $10^2$ ,  $10^3$ , and  $10^4$  V/V.

**2.58** For each of the following combinations of op-amp open-loop gain  $A$  and nominal closed-loop gain  $G_0$ , calculate the actual closed-loop gain  $G$  that is achieved. Also, calculate the percentage by which  $|G|$  falls short of the nominal gain magnitude  $|G_0|$ .

Case	$G_0$ (V/V)	$A$ (V/V)
a	−1	10
b	+1	10
c	−1	100
d	+10	10
e	−10	100
f	−10	1000
g	+1	2



**2.59** Figure P2.59 shows a circuit that provides an output voltage  $v_o$  whose value can be varied by turning the wiper of the 100-k $\Omega$  potentiometer. Find the range over which  $v_o$  can be varied. If the potentiometer is a “20-turn” device, find the change in  $v_o$  corresponding to each turn of the pot.

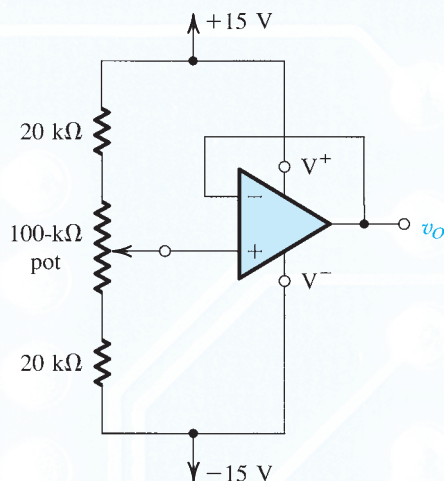


Figure P2.59

## Section 2.4: Difference Amplifiers

**2.60** Find the voltage gain  $v_o/v_{id}$  for the difference amplifier of Fig. 2.16 for the case  $R_1 = R_3 = 10\text{ k}\Omega$  and  $R_2 = R_4 = 100\text{ k}\Omega$ . What is the differential input resistance  $R_{id}$ ? If the two key resistance ratios ( $R_2/R_1$ ) and ( $R_4/R_3$ ) are different from each other by 1%, what do you expect the common-mode gain  $A_{cm}$  to be? Also, find the CMRR in this case. Neglect the effect of the ratio mismatch on the value of  $A_d$ .

**D 2.61** Using the difference amplifier configuration of Fig. 2.16 and assuming an ideal op amp, design the circuit to provide the following differential gains. In each case, the differential input resistance should be 20 k $\Omega$ .

- 1 V/V
- 2 V/V
- 100 V/V
- 0.5 V/V

**2.62** For the circuit shown in Fig. P2.62, express  $v_o$  as a function of  $v_1$  and  $v_2$ . What is the input resistance seen by  $v_1$  alone? By  $v_2$  alone? By a source connected between the two input terminals? By a source connected to both input terminals simultaneously?

**2.63** Consider the difference amplifier of Fig. 2.16 with the two input terminals connected together to an input

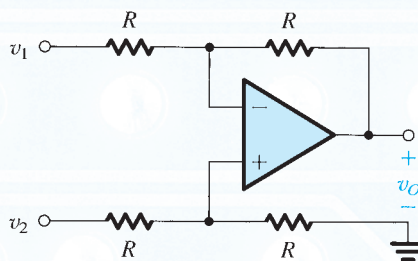


Figure P2.62

common-mode signal source. For  $R_2/R_1 = R_4/R_3$ , show that the input common-mode resistance is  $(R_3 + R_4) \parallel (R_1 + R_2)$ .

**2.64** Consider the circuit of Fig. 2.16, and let each of the  $v_{i1}$  and  $v_{i2}$  signal sources have a series resistance  $R_s$ . What condition must apply in addition to the condition in Eq. (2.15) in order for the amplifier to function as an ideal difference amplifier?

**\*2.65** For the difference amplifier shown in Fig. P2.62, let all the resistors be  $10\text{ k}\Omega \pm x\%$ . Find an expression for the worst-case common-mode gain that results. Evaluate this for  $x = 0.1, 1$ , and  $5$ . Also, evaluate the resulting CMRR in each case. Neglect the effect of resistor tolerances on  $A_d$ .

**2.66** For the difference amplifier of Fig. 2.16, show that if each resistor has a tolerance of  $\pm 100\text{ } \epsilon\%$  (i.e., for, say, a 5% resistor,  $\epsilon = 0.05$ ) then the worst-case CMRR is given approximately by

$$\text{CMRR} \approx 20 \log \left[ \frac{K+1}{4\epsilon} \right]$$

where  $K$  is the nominal (ideal) value of the ratios ( $R_2/R_1$ ) and ( $R_4/R_3$ ). Calculate the value of worst-case CMRR for an amplifier designed to have a differential gain of ideally 100 V/V, assuming that the op amp is ideal and that 1% resistors are used.

**D \*2.67** Design the difference amplifier circuit of Fig. 2.16 to realize a differential gain of 100, a differential input resistance of 20 k $\Omega$ , and a minimum CMRR of 80 dB. Assume the op amp to be ideal. Specify both the resistor values and their required tolerance (e.g., better than  $x\%$ ).

**\*2.68** (a) Find  $A_d$  and  $A_{cm}$  for the difference amplifier circuit shown in Fig. P2.68.

(b) If the op amp is specified to operate properly as long as the common-mode voltage at its positive and negative inputs falls in the range  $\pm 2.5\text{ V}$ , what is the corresponding limitation on the range of the input common-mode signal  $v_{icm}$ ? (This is known as the **common-mode range** of the differential amplifier.)

(c) The circuit is modified by connecting a 10-k $\Omega$  resistor between node A and ground, and another 10-k $\Omega$  resistor between node B and ground. What will now be the values of  $A_d$ ,  $A_{cm}$ , and the input common-mode range?

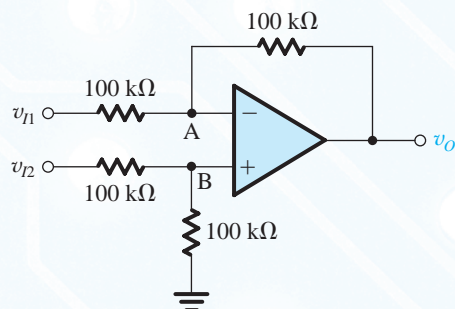


Figure P2.68

**\*\*2.69** To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. P2.69 employs positive feedback, in addition to the negative feedback provided by the resistor  $R$  connected from the output to the negative input of the op amp. Specifically, a voltage divider ( $R_5$ ,  $R_6$ ) connected across the output feeds a fraction  $\beta$  of the output, that is, a voltage  $\beta v_O$ , back to the positive-input terminal of the op amp through a resistor  $R$ . Assume that  $R_5$  and  $R_6$  are much smaller than  $R$  so that the current through  $R$  is much lower than the current in the voltage divider, with the result that  $\beta \approx R_6 / (R_5 + R_6)$ . Show that the differential gain is given by

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{1}{1 - \beta}$$

(Hint: Use superposition.)

Design the circuit to obtain a differential gain of 10 V/V and differential input resistance of 2 M $\Omega$ . Select values for  $R$ ,  $R_5$ , and  $R_6$ , such that  $(R_5 + R_6) \leq R/100$ .

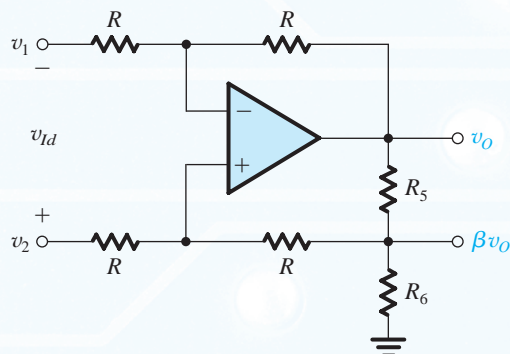


Figure P2.69

**\*2.70** Figure P2.70 shows a modified version of the difference amplifier. The modified circuit includes a resistor  $R_G$ , which can be used to vary the gain. Show that the differential voltage gain is given by

$$\frac{v_O}{v_{Id}} = -2 \frac{R_2}{R_1} \left[ 1 + \frac{R_2}{R_G} \right]$$

(Hint: The virtual short circuit at the op-amp input causes the current through the  $R_1$  resistors to be  $v_{Id}/2R_1$ .)

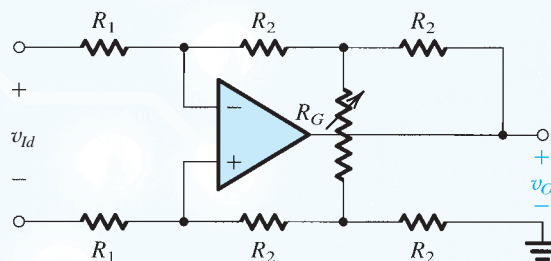


Figure P2.70

**D \*2.71** The circuit shown in Fig. P2.71 is a representation of a versatile, commercially available IC, the INA105, manufactured by Burr-Brown and known as a differential amplifier module. It consists of an op amp and precision, laser-trimmed, metal-film resistors. The circuit can be configured for a variety of applications by the appropriate connection of terminals A, B, C, D, and O.

(a) Show how the circuit can be used to implement a difference amplifier of unity gain.

(b) Show how the circuit can be used to implement single-ended amplifiers with gains:

- (i)  $-1$  V/V
- (ii)  $+1$  V/V
- (iii)  $+2$  V/V
- (iv)  $+1/2$  V/V

Avoid leaving a terminal open-circuited, for such a terminal may act as an “antenna,” picking up interference and noise

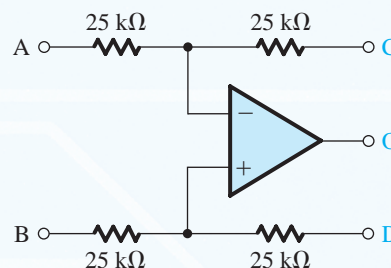


Figure P2.71



through capacitive coupling. Rather, find a convenient node to connect such a terminal in a redundant way. When more than one circuit implementation is possible, comment on the relative merits of each, taking into account such considerations as dependence on component matching and input resistance.

**2.72** Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of +2 V (dc) and a differential input signal of 80-mV peak sine wave. Let  $2R_1 = 2\text{ k}\Omega$ ,  $R_2 = 50\text{ k}\Omega$ ,  $R_3 = R_4 = 10\text{ k}\Omega$ . Find the voltage at every node in the circuit.

**2.73** (a) Consider the instrumentation amplifier circuit of Fig. 2.20(a). If the op amps are ideal except that their outputs saturate at  $\pm 14\text{ V}$ , in the manner shown in Fig. 1.14, find the maximum allowed input common-mode signal for the case  $R_1 = 1\text{ k}\Omega$  and  $R_2 = 100\text{ k}\Omega$ .

(b) Repeat (a) for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

**2.74** (a) Expressing  $v_{i1}$  and  $v_{i2}$  in terms of differential and common-mode components, find  $v_{o1}$  and  $v_{o2}$  in the circuit in Fig. 2.20(a) and hence find their differential component  $v_{o2} - v_{o1}$  and their common-mode component  $\frac{1}{2}(v_{o1} + v_{o2})$ . Now find the differential gain and the common-mode gain of the first stage of this instrumentation amplifier and hence the CMRR.

(b) Repeat for the circuit in Fig. 2.20(b), and comment on the difference between the two circuits.

**\*2.75** For an instrumentation amplifier of the type shown in Fig. 2.20(b), a designer proposes to make  $R_2 = R_3 = R_4 = 100\text{ k}\Omega$ , and  $2R_1 = 10\text{ k}\Omega$ . For ideal components, what difference-mode gain, common-mode gain, and CMRR result? Reevaluate the worst-case values for these for the situation in which all resistors are specified as  $\pm 1\%$  units. Repeat the latter analysis for the case in which  $2R_1$  is reduced to  $1\text{ k}\Omega$ . What do you conclude about the effect of the gain of the first stage on CMRR? (Hint: Eq. (2.19) can be used to evaluate  $A_{cm}$  of the second stage.)

**D 2.76** Design the instrumentation-amplifier circuit of Fig. 2.20(b) to realize a differential gain, variable in the range 1 to 100, utilizing a 100-k $\Omega$  pot as variable resistor. (Hint: Design the second stage for a gain of 0.5.)

**SIM \*2.77** The circuit shown in Fig. P2.77 is intended to supply a voltage to floating loads (those for which both terminals are ungrounded) while making greatest possible use of the available power supply.

(a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1-V peak-to-peak sine wave applied at A. Also sketch  $v_o$ .

(b) What is the voltage gain  $v_o/v_i$ ?

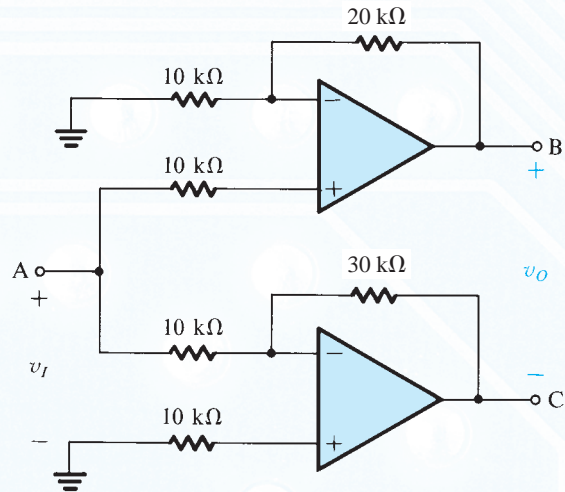


Figure P2.77

(c) Assuming that the op amps operate from  $\pm 15\text{-V}$  power supplies and that their output saturates at  $\pm 14\text{ V}$  (in the manner shown in Fig. 1.14), what is the largest sine-wave output that can be accommodated? Specify both its peak-to-peak and rms values.

**\*2.78** The two circuits in Fig. P2.78 are intended to function as voltage-to-current converters; that is, they supply the load impedance  $Z_L$  with a current proportional to  $v_i$  and independent of the value of  $Z_L$ . Show that this is indeed the case, and find for each circuit  $i_o$  as a function of  $v_i$ . Comment on the differences between the two circuits.

## Section 2.5: Integrators and Differentiators

**2.79** A Miller integrator incorporates an ideal op amp, a resistor  $R$  of  $100\text{ k}\Omega$ , and a capacitor  $C$  of  $1\text{ nF}$ . A sine-wave signal is applied to its input.

(a) At what frequency (in Hz) are the input and output signals equal in amplitude?

(b) At that frequency, how does the phase of the output sine wave relate to that of the input?

(c) If the frequency is lowered by a factor of 10 from that found in (a), by what factor does the output voltage change, and in what direction (smaller or larger)?

(d) What is the phase relation between the input and output in situation (c)?

**D 2.80** Design a Miller integrator with a time constant of  $0.1\text{ s}$  and an input resistance of  $100\text{ k}\Omega$ . A dc voltage of  $-1\text{ V}$  is applied at the input at time 0, at which moment  $v_o = -10\text{ V}$ . How long does it take the output to reach  $0\text{ V}$ ?  $+10\text{ V}$ ?

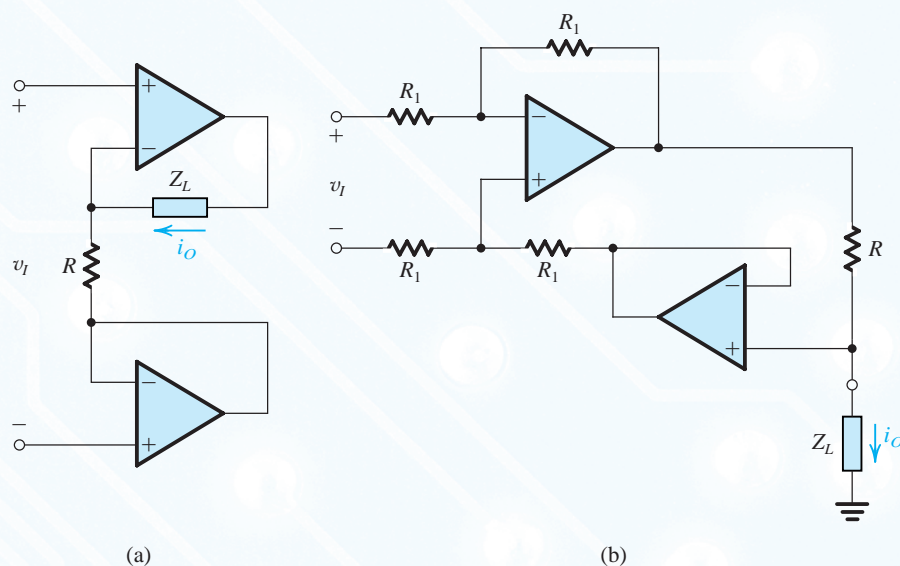


Figure P2.78

**2.81** An op-amp-based inverting integrator is measured at 1 kHz to have a voltage gain of  $-100$  V/V. At what frequency is its gain reduced to  $-1$  V/V? What is the integrator time constant?

**D 2.82** Design a Miller integrator that has a unity-gain frequency of 1 krad/s and an input resistance of  $100$  k $\Omega$ . Sketch the output you would expect for the situation in which, with output initially at 0 V, a 2-V, 2-ms pulse is applied to the input. Characterize the output that results when a sine wave  $2 \sin 1000t$  is applied to the input.

**D 2.83** Design a Miller integrator whose input resistance is  $20$  k $\Omega$  and unity-gain frequency is 10 kHz. What components are needed? For long-term stability, a feedback resistor is introduced across the capacitor, limits the dc gain to 40 dB. What is its value? What is the associated lower 3-dB frequency? Sketch and label the output that results with a 0.1-ms, 1-V positive-input pulse (initially at 0 V) with (a) no dc stabilization (but with the output initially at 0 V) and (b) the feedback resistor connected.

**\*2.84** A Miller integrator whose input and output voltages are initially zero and whose time constant is 1 ms is driven by the signal shown in Fig. P2.84. Sketch and label the output waveform that results. Indicate what happens if the input levels are  $\pm 2$  V, with the time constant the same (1 ms) and with the time constant raised to 2 ms.

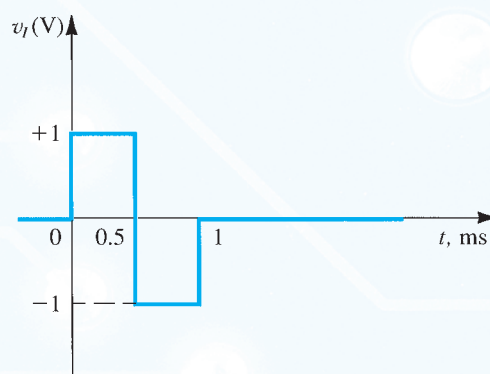


Figure P2.84

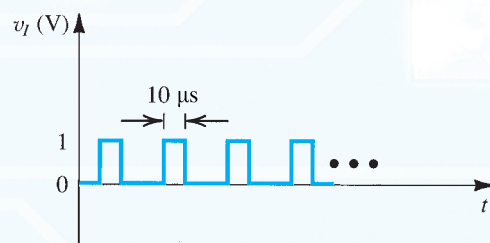


Figure P2.85

**2.85** Consider a Miller integrator having a time constant of 1 ms and an output that is initially zero, when fed with a string of pulses of  $10$ - $\mu$ s duration and 1-V amplitude rising from 0 V (see Fig. P2.85). Sketch and label the output wave

form resulting. How many pulses are required for an output voltage change of 1 V?



**D 2.86** Figure P2.86 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order, low-pass active filter. Derive the transfer function and show that the dc gain is  $(-R_2/R_1)$  and the 3-dB frequency  $\omega_0 = 1/CR_2$ . Design the circuit to obtain an input resistance of  $10\text{ k}\Omega$ , a dc gain of 20 dB, and a 3-dB frequency of 10 kHz. At what frequency does the magnitude of the transfer function reduce to unity?

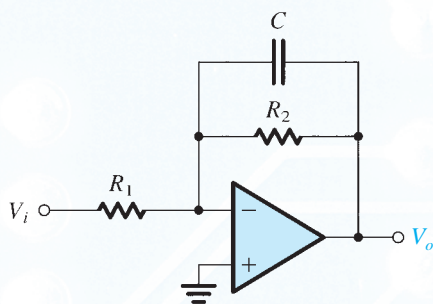


Figure P2.86

**2.87** Show that a Miller integrator implemented with an op amp with open-loop gain  $A_0$  has a low-pass STC transfer function. What is the pole frequency of the STC function? How does this compare with the pole frequency of the ideal integrator? If an ideal Miller integrator is fed with a  $-1\text{-V}$  pulse signal with a width  $T = CR$ , what will the output voltage be at  $t = T$ ? Assume that at  $t = 0$ ,  $v_o = 0$ . Repeat for an integrator with an op amp having  $A_0 = 1000$ .

**2.88** A differentiator utilizes an ideal op amp, a  $10\text{-k}\Omega$  resistor, and a  $0.01\text{-}\mu\text{F}$  capacitor. What is the frequency  $f_0$  (in Hz) at which its input and output sine-wave signals have equal magnitude? What is the output signal for a  $1\text{-V}$  peak-to-peak sine-wave input with frequency equal to  $10f_0$ ?

**2.89** An op-amp differentiator with  $1\text{-ms}$  time constant is driven by the rate-controlled step shown in Fig. P2.89. Assuming  $v_o$  to be zero initially, sketch and label its waveform.

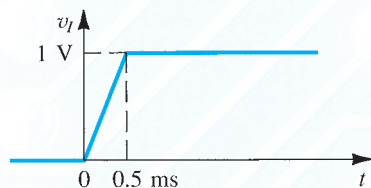


Figure P2.89

**2.90** An op-amp differentiator, employing the circuit shown in Fig. 2.27(a), has  $R = 10\text{ k}\Omega$  and  $C = 0.1\text{ }\mu\text{F}$ . When a triangle wave of  $\pm 1\text{-V}$  peak amplitude at  $1\text{ kHz}$  is applied to the input, what form of output results? What is its frequency? What is its peak amplitude? What is its average value? What value of  $R$  is needed to cause the output to have a  $10\text{-V}$  peak amplitude?

**2.91** Use an ideal op amp to design a differentiation circuit for which the time constant is  $10^{-3}\text{ s}$  using a  $10\text{-nF}$  capacitor. What are the gains and phase shifts found for this circuit at one-tenth and 10 times the unity-gain frequency? A series input resistor is added to limit the gain magnitude at high frequencies to  $100\text{ V/V}$ . What is the associated 3-dB frequency? What gain and phase shift result at 10 times the unity-gain frequency?

**D 2.92** Figure P2.92 shows a circuit that performs the high-pass, single-time-constant function. Such a circuit is known as a first-order high-pass active filter. Derive the transfer function and show that the high-frequency gain is  $(-R_2/R_1)$  and the 3-dB frequency  $\omega_0 = 1/CR_1$ . Design the circuit to obtain a high-frequency input resistance of  $10\text{ k}\Omega$ , a high-frequency gain of 40 dB, and a 3-dB frequency of 500 Hz. At what frequency does the magnitude of the transfer function reduce to unity?

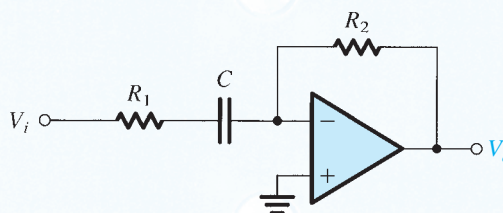


Figure P2.92

**D \*\*2.93** Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1 + (\omega_1/j\omega)][1 + j(\omega/\omega_2)]}$$

where  $\omega_1 = 1/C_1R_1$  and  $\omega_2 = 1/C_2R_2$ . Assuming that the circuit is designed such that  $\omega_2 \gg \omega_1$ , find approximate expressions for the transfer function in the following frequency regions:

- $\omega \ll \omega_1$
- $\omega_1 \ll \omega \ll \omega_2$
- $\omega \gg \omega_2$

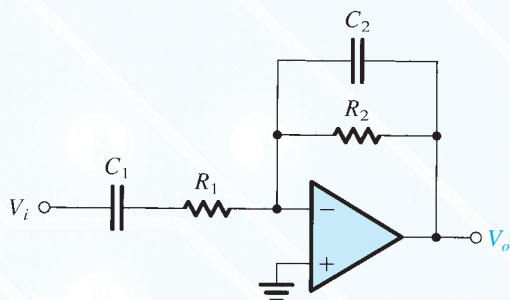


Figure P2.93

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle frequency range,” a low-frequency 3-dB point at 100 Hz, a high-frequency 3-dB point at 100 kHz, and an input resistance (at  $\omega \gg \omega_i$ ) of 1 k $\Omega$ .

## Section 2.6: DC Imperfections

**2.94** An op amp wired in the inverting configuration with the input grounded, having  $R_2 = 100$  k $\Omega$  and  $R_1 = 1$  k $\Omega$ , has an output dc voltage of  $-0.4$  V. If the input bias current is known to be very small, find the input offset voltage.

**2.95** A noninverting amplifier with a gain of 200 uses an op amp having an input offset voltage of  $\pm 2$  mV. Find the output when the input is  $0.01 \sin \omega t$ , volts.

**2.96** A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 5 mV and output saturation levels of  $\pm 13$  V. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? If the amplifier is capacitively coupled in the manner indicated in Fig. 2.36, what would the maximum possible amplitude be?

**2.97** An op amp connected in a closed-loop inverting configuration having a gain of 1000 V/V and using relatively small-valued resistors is measured with input grounded to have a dc output voltage of  $-1.4$  V. What is its input offset voltage? Prepare an offset-voltage-source sketch resembling that in Fig. 2.28. Be careful of polarities.

**2.98** A particular inverting amplifier with nominal gain of  $-100$  V/V uses an imperfect op amp in conjunction with 100-k $\Omega$  and 10-M $\Omega$  resistors. The output voltage is found to be  $+9.31$  V when measured with the input open and  $+9.09$  V with the input grounded.

- What is the bias current of this amplifier? In what direction does it flow?
- Estimate the value of the input offset voltage.
- A 10-M $\Omega$  resistor is connected between the positive-input terminal and ground. With the input left floating (disconnected), the output dc voltage is measured to be  $-0.8$  V. Estimate the input offset current.

**D \*2.99** A noninverting amplifier with a gain of  $+10$  V/V using 100 k $\Omega$  as the feedback resistor operates from a 5-k $\Omega$  source. For an amplifier offset voltage of 0 mV, but with a bias current of 1  $\mu$ A and an offset current of 0.1  $\mu$ A, what range of outputs would you expect? Indicate where you would add an additional resistor to compensate for the bias currents. What does the range of possible outputs then become? A designer wishes to use this amplifier with a 15-k $\Omega$  source. In order to compensate for the bias current in this case, what resistor would you use? And where?

**D 2.100** The circuit of Fig. 2.36 is used to create an ac-coupled noninverting amplifier with a gain of 200 V/V using resistors no larger than 100 k $\Omega$ . What values of  $R_1$ ,  $R_2$ , and  $R_3$  should be used? For a break frequency due to  $C_1$  at 100 Hz, and that due to  $C_2$  at 10 Hz, what values of  $C_1$  and  $C_2$  are needed?

**\*2.101** Consider the difference amplifier circuit in Fig. 2.16. Let  $R_1 = R_3 = 10$  k $\Omega$  and  $R_2 = R_4 = 1$  M $\Omega$ . If the op amp has  $V_{os} = 4$  mV,  $I_B = 0.5$   $\mu$ A, and  $I_{OS} = 0.1$   $\mu$ A, find the worst-case (largest) dc offset voltage at the output.

**\*2.102** The circuit shown in Fig. P2.102 uses an op amp having a  $\pm 4$ -mV offset. What is its output offset voltage? What does the output offset become with the input ac coupled through a capacitor  $C$ ? If, instead, a large capacitor is placed in series with 1-k $\Omega$  resistor, what does the output offset become?

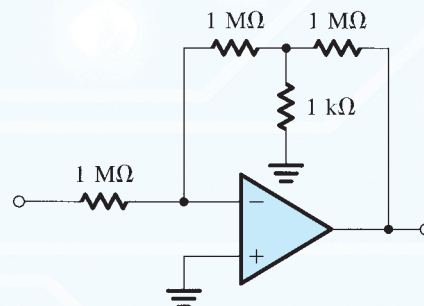


Figure P2.102

**2.103** Using offset-nulling facilities provided for the op amp, a closed-loop amplifier with gain of  $+1000$  is adjusted



at 25°C to produce zero output with the input grounded. If the input offset-voltage drift of the op amp is specified to be 10  $\mu\text{V}/^\circ\text{C}$ , what output would you expect at 0°C and at 75°C? While nothing can be said separately about the polarity of the output offset at either 0 or 75°C, what would you expect their relative polarities to be?

**2.104** An op amp is connected in a closed loop with gain of +100 utilizing a feedback resistor of 1 M $\Omega$ .

- If the input bias current is 100 nA, what output voltage results with the input grounded?
- If the input offset voltage is  $\pm 1$  mV and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded?
- If bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)?
- With bias-current compensation as in (c) in place what is the largest dc voltage at the output due to the combined effect of offset voltage and offset current?

**\*2.105** An op amp intended for operation with a closed-loop gain of  $-100$  V/V uses resistors of 10 k $\Omega$  and 1 M $\Omega$  with a bias-current-compensation resistor  $R_3$ . What should the value of  $R_3$  be? With input grounded, the output offset voltage is found to be +0.21 V. Estimate the input offset current assuming zero input offset voltage. If the input offset voltage can be as large as 1 mV of unknown polarity, what range of offset current is possible?

**2.106** A Miller integrator with  $R = 10$  k $\Omega$  and  $C = 10$  nF is implemented by using an op amp with  $V_{OS} = 3$  mV,  $I_B = 0.1$   $\mu\text{A}$ , and  $I_{OS} = 10$  nA. To provide a finite dc gain, a 1-M $\Omega$  resistor is connected across the capacitor.

- To compensate for the effect of  $I_B$ , a resistor is connected in series with the positive-input terminal of the op amp. What should its value be?
- With the resistor of (a) in place, find the worst-case dc output voltage of the integrator when the input is grounded.

## Section 2.7: Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

**2.107** The data in the following table apply to internally compensated op amps. Fill in the blank entries.

$A_0$	$f_b$ (Hz)	$f_t$ (Hz)
$10^5$	$10^2$	
$10^6$		$10^6$
	$10^3$	$10^8$
	$10^{-1}$	$10^6$
$2 \times 10^5$	10	

**2.108** A measurement of the open-loop gain of an internally compensated op amp at very low frequencies shows it to be 92 dB; at 100 kHz, this shows it is 40 dB. Estimate values for  $A_0$ ,  $f_b$ , and  $f_t$ .

**2.109** Measurements of the open-loop gain of a compensated op amp intended for high-frequency operation indicate that the gain is  $5.1 \times 10^3$  at 100 kHz and  $8.3 \times 10^3$  at 10 kHz. Estimate its 3-dB frequency, its unity-gain frequency, and its dc gain.

**2.110** Measurements made on the internally compensated amplifiers listed below provide the dc gain and the frequency at which the gain has dropped by 20 dB. For each, what are the 3 dB and unity-gain frequencies?

- $3 \times 10^5$  V/V and  $6 \times 10^2$  Hz
- $50 \times 10^5$  V/V and 10 Hz
- 1500 V/V and 0.1 MHz
- 100 V/V and 0.1 GHz
- 25 V/mV and 25 kHz

**2.111** An inverting amplifier with nominal gain of  $-20$  V/V employs an op amp having a dc gain of  $10^4$  and a unity-gain frequency of  $10^6$  Hz. What is the 3-dB frequency  $f_{3dB}$  of the closed-loop amplifier? What is its gain at  $0.1 f_{3dB}$  and at  $10 f_{3dB}$ ?

**2.112** A particular op amp, characterized by a gain-bandwidth product of 10 MHz, is operated with a closed-loop gain of +100 V/V. What 3-dB bandwidth results? At what frequency does the closed-loop amplifier exhibit a  $-6^\circ$  phase shift? A  $-84^\circ$  phase shift?

**2.113** Find the  $f_t$  required for internally compensated op amps to be used in the implementation of closed-loop amplifiers with the following nominal dc gains and 3-dB bandwidths:

- $-100$  V/V; 100 kHz
- $+100$  V/V; 100 kHz
- $+2$  V/V; 10 MHz
- $-2$  V/V; 10 MHz
- $-1000$  V/V; 20 kHz
- $+1$  V/V; 1 MHz
- $-1$  V/V; 1 MHz

**2.114** A noninverting op-amp circuit with a gain of 96 V/V is found to have a 3-dB frequency of 8 kHz. For a particular system application, a bandwidth of 24 kHz is required. What is the highest gain available under these conditions?

**2.115** Consider a unity-gain follower utilizing an internally compensated op amp with  $f_t = 1$  MHz. What is the 3-dB frequency of the follower? At what frequency is the gain of the follower 1% below its low-frequency magnitude? If the input to the follower is a 1-V step, find the 10% to 90% rise time of the output voltage. (Note: The step response of STC low-pass networks is discussed in Appendix E.)



**D \*2.116** It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied at the input, it is required that the output be within 1% of its final value of 1 V in at most 100 ns. What must the  $f_i$  of the op amp be? (Note: The step response of STC low-pass networks is discussed in Appendix E.)

**D \*2.117** This problem illustrates the use of cascaded closed-loop amplifiers to obtain an overall bandwidth greater than can be achieved using a single-stage amplifier with the same overall gain.

(a) Show that cascading two identical amplifier stages, each having a low-pass STC frequency response with a 3-dB frequency  $f_i$ , results in an overall amplifier with a 3-dB frequency given by

$$f_{3\text{dB}} = \sqrt{\sqrt{2} - 1} f_i$$

(b) It is required to design a noninverting amplifier with a dc gain of 40 dB utilizing a single internally compensated op amp with  $f_i = 1$  MHz. What is the 3-dB frequency obtained?

(c) Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 dB. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (b) above.

**D \*\*2.118** A designer, wanting to achieve a stable gain of 100 V/V at 5 MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an  $f_i$  of 40 MHz. How many such amplifiers connected in a cascade of identical noninverting stages would she need to achieve her goal? What is the 3-dB frequency of each stage she can use? What is the overall 3-dB frequency?

**2.119** Consider the use of an op amp with a unity-gain frequency  $f_i$  in the realization of:

- An inverting amplifier with dc gain of magnitude  $K$ .
- A noninverting amplifier with a dc gain of  $K$ .

In each case find the 3-dB frequency and the gain-bandwidth product ( $\text{GBP} \equiv |\text{Gain}| \times f_{3\text{dB}}$ ). Comment on the results.

**\*2.120** Consider an inverting summer with two inputs  $V_1$  and  $V_2$  and with  $V_o = -(V_1 + 2V_2)$ . Find the 3-dB frequency of each of the gain functions  $V_o/V_1$  and  $V_o/V_2$  in terms of the op amp  $f_i$ . (Hint: In each case, the other input to the summer can be set to zero—an application of superposition.)

## Section 2.8: Large-Signal Operation of Op Amps

**2.121** A particular op amp using  $\pm 15$ -V supplies operates linearly for outputs in the range  $-12$  V to  $+12$  V. If used in

an inverting amplifier configuration of gain  $-100$ , what is the rms value of the largest possible sine wave that can be applied at the input without output clipping?

**2.122** Consider an op amp connected in the inverting configuration to realize a closed-loop gain of  $-100$  V/V utilizing resistors of  $1$  k $\Omega$  and  $100$  k $\Omega$ . A load resistance  $R_L$  is connected from the output to ground, and a low-frequency sine-wave signal of peak amplitude  $V_p$  is applied to the input. Let the op amp be ideal except that its output voltage saturates at  $\pm 10$  V and its output current is limited to the range  $\pm 20$  mA.

- For  $R_L = 1$  k $\Omega$ , what is the maximum possible value of  $V_p$  while an undistorted output sinusoid is obtained?
- Repeat (a) for  $R_L = 100$   $\Omega$ .
- If it is desired to obtain an output sinusoid of 10-V peak amplitude, what minimum value of  $R_L$  is allowed?

**2.123** An op amp having a slew rate of  $10$  V/ $\mu$ s is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 5 V. What is the shortest pulse that can be used while ensuring full-amplitude output? For such a pulse, describe the output resulting.

**2.124** For operation with 10-V output pulses with the requirement that the sum of the rise and fall times represent only 20% of the pulse width (at half amplitude), what is the slew-rate requirement for an op amp to handle pulses  $2$   $\mu$ s wide? (Note: The rise and fall times of a pulse signal are usually measured between the 10%- and 90%-height points.)

**2.125** What is the highest frequency of a triangle wave of 20-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is  $10$  V/ $\mu$ s? For a sine wave of the same frequency, what is the maximum amplitude of output signal that remains undistorted?

**2.126** For an amplifier having a slew rate of  $60$  V/ $\mu$ s, what is the highest frequency at which a 20-V peak-to-peak sine wave can be produced at the output?

**D \*2.127** In designing with op amps one has to check the limitations on the voltage and frequency ranges of operation of the closed-loop amplifier, imposed by the op-amp finite bandwidth ( $f_i$ ), slew rate (SR), and output saturation ( $V_{\text{omax}}$ ). This problem illustrates the point by considering the use of an op amp with  $f_i = 2$  MHz,  $\text{SR} = 1$  V/ $\mu$ s, and  $V_{\text{omax}} = 10$  V in the design of a noninverting amplifier with a nominal gain of 10. Assume a sine-wave input with peak amplitude  $V_i$ .

- If  $V_i = 0.5$  V, what is the maximum frequency before the output distorts?
- If  $f = 20$  kHz, what is the maximum value of  $V_i$  before the output distorts?
- If  $V_i = 50$  mV, what is the useful frequency range of operation?
- If  $f = 5$  kHz, what is the useful input voltage range?