that is *enabled* (by raising its third-state input terminal). All other gates will be in the third state and thus will have no control of the bus.

14.5 TTL FAMILIES WITH IMPROVED PERFORMANCE

The standard TTL circuits studied in the two previous sections were introduced in the mid-1960s. Since then, several improved versions have been developed. In this section we shall discuss some of these improved TTL subfamilies. As will be seen the improvements are in two directions: increasing speed and reducing power dissipation.

The speed of the standard TTL gate of Fig. 14.24 is limited by two mechanisms: first, transistors Q_1, Q_2, and Q_3 saturate, and hence we have to contend with their finite storage time. Although Q_2 is discharged reasonably quickly because of the active mode of operation of Q_1, as already explained, this is not true for Q_3, whose base charge has to leak out through the 1-kΩ resistance in its base circuit. Second, the resistances in the circuit, together with the various transistor and wiring capacitances, form relatively long time constants, which contribute to lengthening the gate delay.

It follows that there are two approaches to speeding up the operation of TTL. The first is to prevent transistor saturation and the second is to reduce the values of all resistances. Both approaches are utilized in the Schottky TTL circuit family.

Schottky TTL

In Schottky TTL, transistors are prevented from saturation by connecting a low-voltage-drop diode between base and collector, as shown in Fig. 14.27. These diodes, formed as a metal-to-semiconductor junction, are called Schottky diodes and have a forward voltage drop of about 0.5 V. We have briefly discussed Schottky diodes in Section 3.9. Schottky diodes[4] are easily fabricated and do not increase chip area. In fact, the Schottky TTL fabrication process has been designed to yield transistors with smaller areas and thus higher β and f_T than those produced by the standard TTL process. Figure 14.27 also shows the symbol used to represent the combination of a transistor and a Schottky diode, referred to as a Schottky transistor.

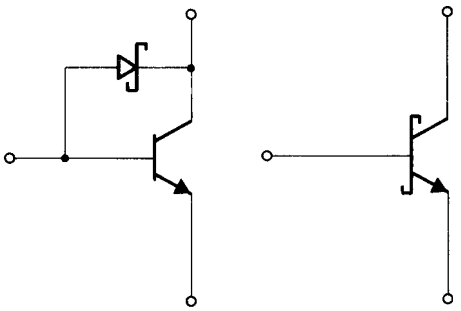


FIGURE 14.27 **(a)** A transistor with a Schottky diode clamp. **(b)** Circuit symbol for the connection in (a), known as a Schottky transistor.

[4] Note that silicon Schottky diodes exhibit voltage drops of about 0.5 V, whereas GaAs Schottky diodes (Section 5.12) exhibit voltage drops of about 0.7 V.

9.7 DATA CONVERTERS—AN INTRODUCTION

In this section we begin the study of another group of analog IC circuits of great importance; namely, data converters.

9.7.1 Digital Processing of Signals

Most physical signals, such as those obtained at transducer outputs, exist in analog form. Some of the processing required on these signals is most conveniently performed in an analog fashion. For instance, in instrumentation systems it is quite common to use a high-input-impedance, high-gain, high-CMRR differential amplifier right at the output of the transducer. This is usually followed by a filter whose purpose is to eliminate interference. However, further signal processing is usually required, which can range from simply obtaining a measurement of signal strength to performing some algebraic manipulations on this and related signals to obtain the value of a particular system parameter of interest, as is usually the case in systems intended to provide a complex control function. Another example of signal processing can be found in the common need for transmission of signals to a remote receiver.

Many such forms of signal processing can be performed by analog means. In earlier chapters we encountered circuits for implementing a number of such tasks. However, an attractive alternative exists: It is to convert, following some initial analog processing, the signal from analog to digital form and then use economical, accurate, and convenient digital ICs to perform **digital signal processing.** Such processing can in its simplest form provide us with a measure of the signal strength as an easy-to-read number (consider, e.g., the digital voltmeter). In more involved cases the digital signal processor can perform a variety of arithmetic and logic operations that implement a **filtering algorithm.** The resulting **digital filter** does many of the same tasks that an analog filter performs—namely, eliminate interference and noise. Yet another example of digital signal processing is found in digital communications systems, where signals are transmitted as a sequence of binary pulses, with the obvious advantage that corruption of the amplitudes of these pulses by noise is, to a large extent, of no consequence.

Once digital signal processing has been performed, we might be content to display the result in digital form, such as a printed list of numbers. Alternatively, we might require an analog output. Such is the case in a telecommunications system, where the usual output may be audible speech. If such an analog output is desired, then obviously we need to convert the digital signal back to an analog form.

It is not our purpose here to study the techniques of digital signal processing. Rather, we shall examine the interface circuits between the analog and digital domains. Specifically, we shall study the basic techniques and circuits employed to convert an analog signal to digital form **(analog-to-digital** or simply **A/D conversion)** and those used to convert a digital signal to analog form **(digital-to-analog** or simply **D/A conversion).** Digital circuits are studied in Chapters 10 and 11.

9.7.2 Sampling of Analog Signals

The principle underlying digital signal processing is that of **sampling** the analog signal. Figure 9.36 illustrates in a conceptual form the process of obtaining samples of an analog signal. The switch shown closes periodically under the control of a periodic pulse signal (clock). The closure time of the switch, τ, is relatively short, and the samples obtained are

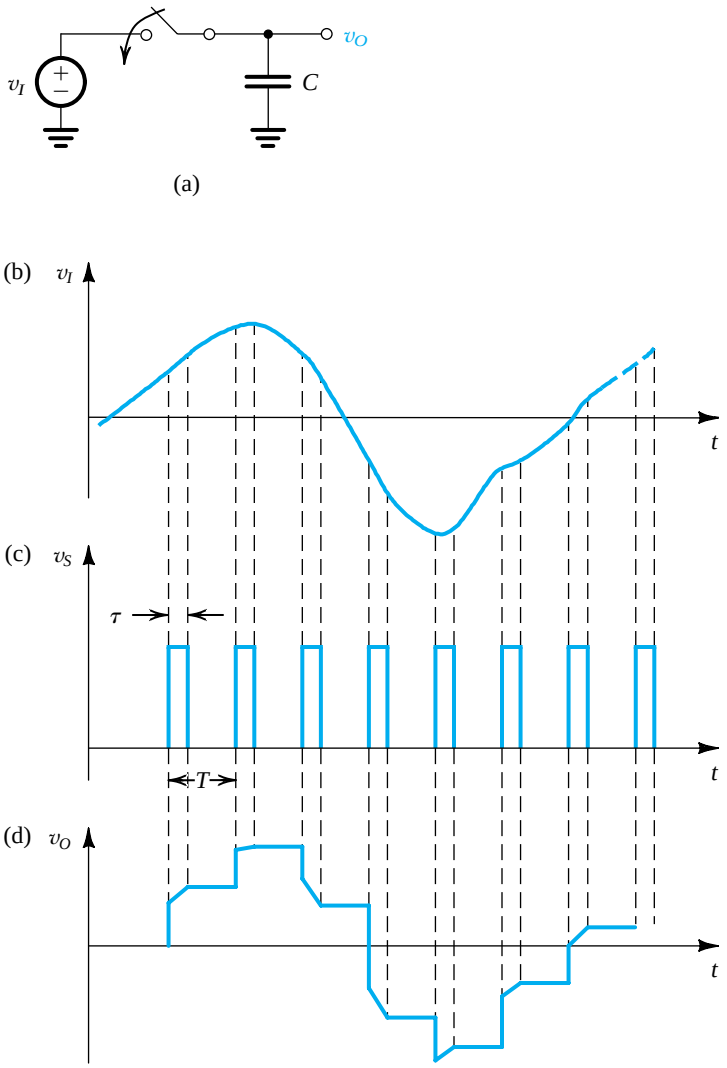


FIGURE 9.36 The process of periodically sampling an analog signal. **(a)** Sample-and-hold (S/H) circuit. The switch closes for a small part (τ seconds) of every clock period (T). **(b)** Input signal waveform. **(c)** Sampling signal (control signal for the switch). **(d)** Output signal (to be fed to A/D converter).

stored (held) on the capacitor. The circuit of Fig. 9.36 is known as a **sample-and-hold (S/H) circuit.** As indicated, the S/H circuit consists of an analog switch that can be implemented by a MOSFET transmission gate (Section 10.5), a storage capacitor, and (not shown) a buffer amplifier.

Between the sampling intervals—that is, during the *hold* intervals—the voltage level on the capacitor represents the signal samples we are after. Each of these voltage levels is then fed to the input of an A/D converter, which provides an N-bit binary number proportional to the value of signal sample.

The fact that we can do our processing on a limited number of samples of an analog signal while ignoring the analog-signal details between samples is based on the Shannon's sampling theorem [see Lathi (1965)].

9.7.3 Signal Quantization

Consider an analog signal whose values range from 0 to +10 V. Let us assume that we wish to convert this signal to digital form and that the required output is a 4-bit digital signal.[4] We know that a 4-bit binary number can represent 16 different values, 0 to 15; it follows that the *resolution* of our conversion will be 10 V/15 = $\frac{2}{3}$ V. Thus an analog signal of 0 V will be represented by 0000, $\frac{2}{3}$ V will be represented by 0001, 6 V will be represented by 1001, and 10 V will be represented by 1111.

All these sample numbers are multiples of the basic increment ($\frac{2}{3}$ V). A question now arises regarding the conversion of numbers that fall between these successive incremental levels. For instance, consider the case of a 6.2-V analog level. This falls between 18/3 and 20/3. However, since it is closer to 18/3 we treat it as if it were 6 V and *code* it as 1001. This process is called **quantization.** Obviously errors are inherent in this process; such errors are called quantization errors. Using more bits to represent (encode or, simply, code) an analog signal reduces quantization errors but requires more complex circuitry.

9.7.4 The A/D and D/A Converters as Functional Blocks

Figure 9.37 depicts the functional block representations of A/D and D/A converters. As indicated, the **A/D converter** (also called an **ADC**) accepts an analog sample v_A and produces an N-bit **digital word.** Conversely, the **D/A converter** (also called a **DAC**) accepts an n-bit digital word and produces an analog sample. The output samples of the D/A converter are often fed to a sample-and-hold circuit. At the output of the S/H circuit a staircase waveform, such as that in Fig. 9.38, is obtained. The staircase waveform can then be smoothed by a

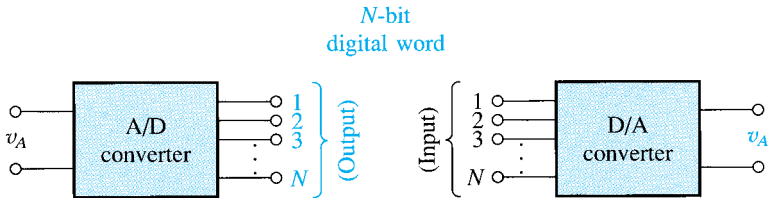


FIGURE 9.37 The A/D and D/A converters as circuit blocks.

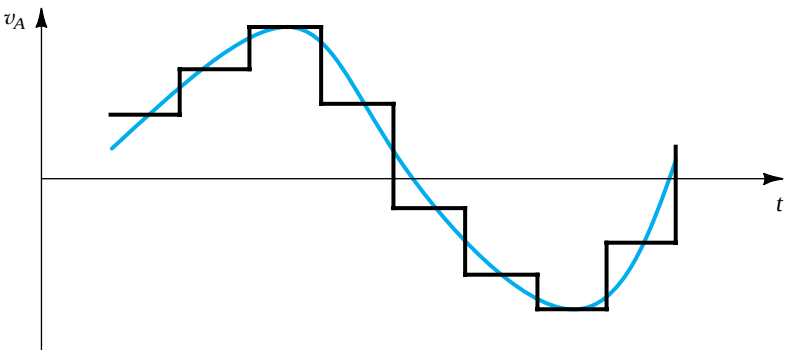


FIGURE 9.38 The analog samples at the output of a D/A converter are usually fed to a sample-and-hold circuit to obtain the staircase waveform shown. This waveform can then be filtered to obtain the smooth waveform, shown in color. The time delay usually introduced by the filter is not shown.

[4] *Bit* stands for *b*inary dig*it*.

low-pass filter, giving rise to the smooth curve shown in color in Fig. 9.38. In this way an analog output signal is reconstructed. Finally, note that the quantization error of an A/D converter is equivalent to $\pm\frac{1}{2}$ least significant bit (b_N).

EXERCISE

9.31 An analog signal in the range 0 to +10 V is to be converted to an 8-bit digital signal. What is the resolution of the conversion in volts? What is the digital representation of an input of 6 V? What is the representation of an input of 6.2 V? What is the error made in the quantization of 6.2 V in absolute terms and as a percentage of the input? As a percentage of full scale? What is the largest possible quantization error as a percentage of full scale?

Ans. 0.0392 V; 10011001; 10011110; –0.0064 V; –0.1%; –0.064%; 0.196%

9.8 D/A CONVERTER CIRCUITS

9.8.1 Basic Circuit Using Binary-Weighted Resistors

Figure 9.39 shows a simple circuit for an N-bit D/A converter. The circuit consists of a reference voltage V_{REF}, N binary-weighted resistors R, $2R$, $4R$, $8R$, . . . , $2^{N-1}R$, N single-pole double-throw switches S_1, S_2, . . . , S_N, and an op amp together with its feedback resistance $R_f = R/2$.

The switches are controlled by an N-bit digital input word D,

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N} \tag{9.109}$$

where b_1, b_2, and so on are bit coefficients that are either 1 or 0. Note that the bit b_N is the **least significant bit (LSB)** and b_1 is the **most significant bit (MSB).** In the circuit in Fig. 9.39, b_1 controls switch S_1, b_2 controls S_2, and so on. When b_i is 0, switch S_i is in position 1, and when b_i is 1 switch S_i is in position 2.

Since position 1 of all switches is ground and position 2 is virtual ground, the current through each resistor remains constant. Each switch simply controls where its corresponding current goes: to ground (when the corresponding bit is 0) or to virtual ground (when the corresponding bit is 1). The currents flowing into the virtual ground add up, and the sum flows

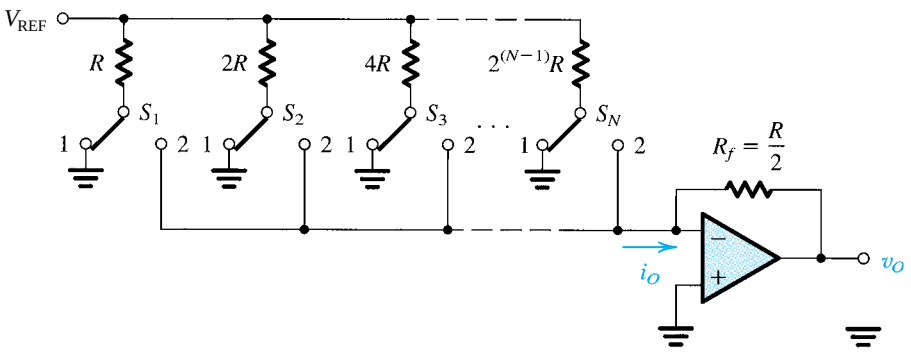


FIGURE 9.39 An N-bit D/A converter using a binary-weighted resistive ladder network.

through the feedback resistance R_f. The total current i_O is therefore given by

$$i_O = \frac{V_{REF}}{R}b_1 + \frac{V_{REF}}{2R}b_2 + \cdots + \frac{V_{REF}}{2^{N-1}R}b_N$$
$$= \frac{2V_{REF}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

Thus,

$$i_O = \frac{2V_{REF}}{R}D \tag{9.110}$$

and the output voltage v_O is given by

$$v_O = -i_O R_f = -V_{REF}D \tag{9.111}$$

which is directly proportional to the digital word D, as desired.

It should be noted that the accuracy of the DAC depends critically on (1) the accuracy of V_{REF}, (2) the precision of the binary-weighted resistors, and (3) the perfection of the switches. Regarding the third point, we should emphasize that these switches handle analog signals; thus their perfection is of considerable interest. While the offset voltage and the finite on resistance are not of critical significance in a digital switch, these parameters are of immense importance in *analog switches*. The use of MOSFETs to implement analog switches will be discussed in Chapter 10. Also, we shall shortly see that in practical circuit implementations of the DAC, the binary-weighted currents are generated by current sources. In this case the analog switch can be realized using the differential-pair circuit, as will be shown shortly.

A disadvantage of the binary-weighted resistor network is that for a large number of bits ($N > 4$) the spread between the smallest and largest resistances becomes quite large. This implies difficulties in maintaining accuracy in resistor values. A more convenient scheme exists utilizing a resistive network called the *R*-2*R* ladder.

9.8.2 *R*-2*R* Ladders

Figure 9.40 shows the basic arrangement of a DAC using an *R*-2*R* ladder. Because of the small spread in resistance values, this network is usually preferred to the binary-weighted scheme discussed earlier, especially for $N > 4$. Operation of the *R*-2*R* ladder is straightforward. First, it can be shown, by starting from the right and working toward the left, that the

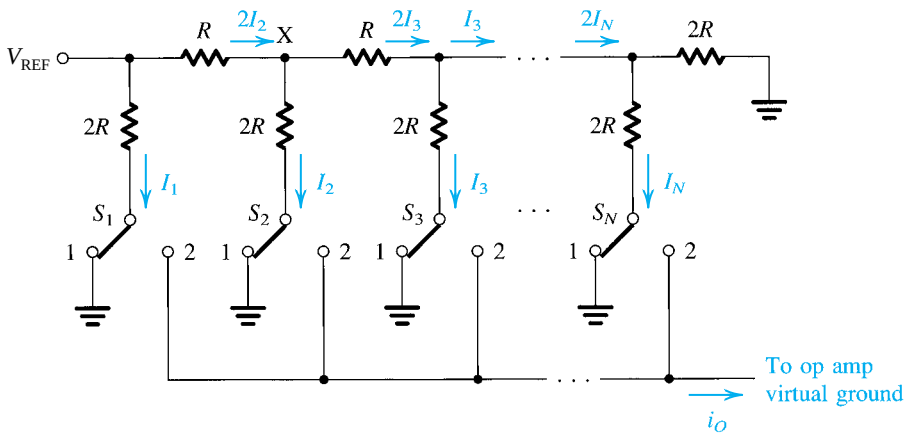


FIGURE 9.40 The basic circuit configuration of a DAC utilizing an *R*-2*R* ladder network.

resistance to the right of each ladder node, such as that labeled X, is equal to $2R$. Thus the current flowing to the right, away from each node, is equal to the current flowing downward to ground, and twice that current flows into the node from the left side. It follows that

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1}I_N \tag{9.112}$$

Thus, as in the binary-weighted resistive network, the currents controlled by the switches are binary weighted. The output current i_O will therefore be given by

$$i_O = \frac{V_{\text{REF}}}{R}D \tag{9.113}$$

9.8.3 A Practical Circuit Implementation

A practical circuit implementation of the DAC utilizing an R-$2R$ ladder is shown in Fig. 9.41. The circuit utilizes BJTs to generate binary-weighted constant currents $I_1, I_2, \ldots, I_N$, which are switched between ground and virtual ground of an output summing op amp (not shown). We shall first show that the currents I_1 to I_N are indeed binary-weighted, with I_1 corresponding to the MSB and I_N corresponding to the LSB of the DAC.

Starting at the two rightmost transistors, Q_N and Q_t, we see that if they are matched, their emitter currents will be equal and are denoted (I_N/α). Transistor Q_t is included to provide proper termination of the R-$2R$ network. The voltage between the base line of the BJTs and node N will be

$$V_N = V_{BE_N} + \left(\frac{I_N}{\alpha}\right)(2R)$$

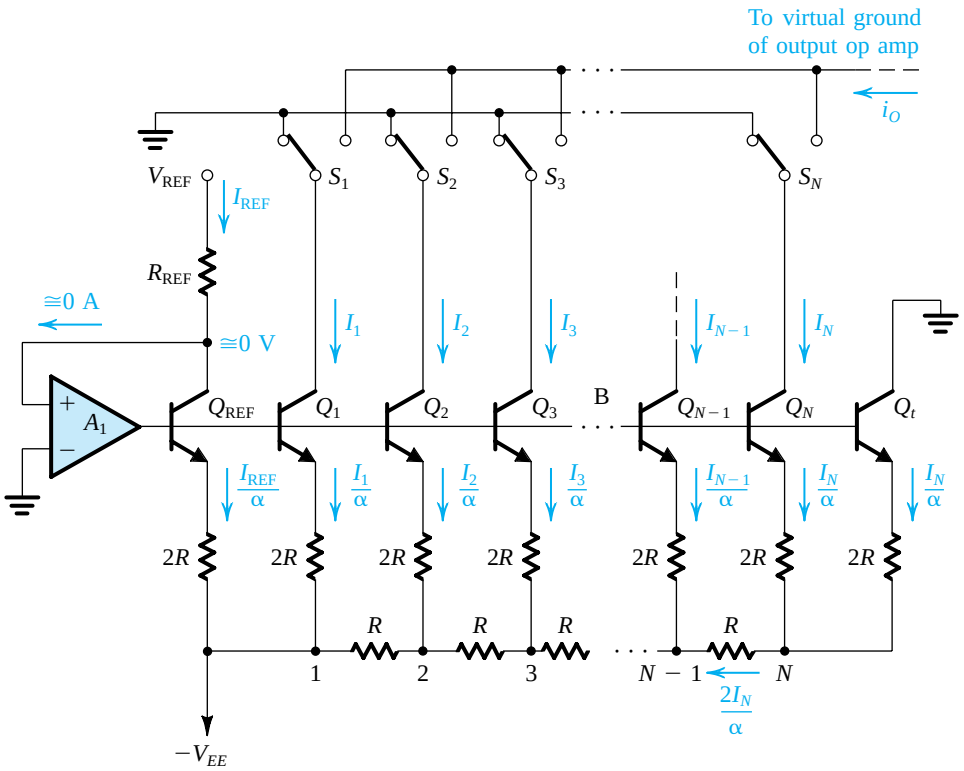


FIGURE 9.41 A practical circuit implementation of a DAC utilizing an R-$2R$ ladder network.

where V_{BE_N} is the base–emitter voltage of Q_N. Since the current flowing through the resistor R connected to node N is $(2I_N/\alpha)$, the voltage between node B and node $(N-1)$ will be

$$V_{N-1} = V_N + \left(\frac{2I_N}{\alpha}\right)R = V_{BE_N} + \frac{4I_N}{\alpha}R$$

Assuming, for the moment, that $V_{BE_{N-1}} = V_{BE_N}$, we see that a voltage of $(4I_N/\alpha)R$ appears across the resistance $2R$ in the emitter of Q_{N-1}. Thus Q_{N-1} will have an emitter current of $(2I_N/\alpha)$ and a collector current of $(2I_N)$, twice the current in Q_N. The two transistors will have equal V_{BE} drops if their junction areas are scaled in the same proportion as their currents, which is usually done in practice.

Proceeding in the manner above we can show that

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1}I_N \tag{9.114}$$

under the assumption that the EBJ areas of Q_1 to Q_N are scaled in a binary-weighted fashion.

Next consider op amp A_1, which, together with the reference transistor Q_{REF}, forms a negative-feedback loop. (Convince yourself that the feedback is indeed negative.) A virtual ground appears at the collector of Q_{REF} forcing it to conduct a collector current $I_{\text{REF}} = V_{\text{REF}}/R_{\text{REF}}$ independent of whatever imperfections Q_{REF} might have. Now, if Q_{REF} and Q_1 are matched, their collector currents will be equal,

$$I_1 = I_{\text{REF}}$$

Thus, the binary-weighted currents are directly related to the reference current, independent of the exact values of V_{BE} and α. Also observe that op amp A_1 supplies the base currents of all the BJTs.

9.8.4 Current Switches

Each of the single-pole double-throw switches in the DAC circuit of Fig. 9.41 can be implemented by a circuit such as that shown in Fig. 9.42 for switch S_m. Here I_m denotes the current flowing in the collector of the mth-bit transistor. The circuit is a differential pair with the

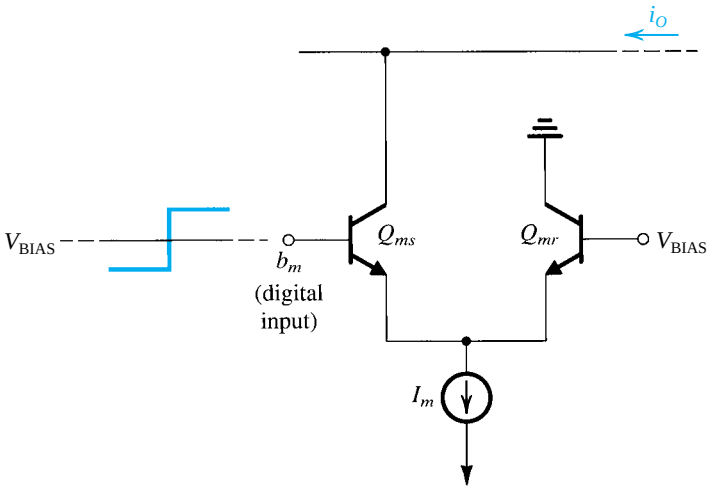


FIGURE 9.42 Circuit implementation of switch S_m in the DAC of Fig. 9.41. In a BiCMOS technology, Q_{ms} and Q_{mr} can be implemented using MOSFETs, thus avoiding the inaccuracy caused by the base current of BJTs.

base of the reference transistor Q_{mr} connected to a suitable dc voltage V_{BIAS}, and the digital signal representing the mth bit b_m applied to the base of the other transistor Q_{ms}. If the voltage representing b_m is higher than V_{BIAS} by a few hundred millivolts, Q_{ms} will turn on and Q_{mr} will turn off. The bit current I_m will flow through Q_{ms} and onto the output summing line. On the other hand, when b_m is low, Q_{ms} will be off and I_m will flow through Q_{mr} to ground.

The current switch of Fig. 9.42 is simple and features high-speed operation. It suffers, however, from the fact that part of the current I_m flows through the base of Q_{ms} and thus does not appear on the output summing line. More elaborate circuits for current switches can be found in Grebene (1984). Also, in a BiCMOS technology the differential-pair transistors Q_{ms} and Q_{mr} can be replaced with MOSFETs, thus eliminating the base current problem.

EXERCISES

9.32 What is the maximum resistor ratio required by a 12-bit D/A converter utilizing a binary-weighted resistor network?

Ans. 2048

9.33 If the input bias current of an op amp, used as the output summer in a 10-bit DAC, is to be no more than that equivalent to $\frac{1}{4}$ LSB, what is the maximum current required to flow in R_f for an op amp whose bias current is as great as 0.5 μA?

Ans. 2.046 mA

9.9 A/D CONVERTER CIRCUITS

There exist a number of A/D conversion techniques varying in complexity and speed. We shall discuss four different approaches: two simple, but slow, schemes, one complex (in terms of the amount of circuitry required) but extremely fast method, and, finally, a method particularly suited for MOS implementation.

9.9.1 The Feedback-Type Converter

Figure 9.43 shows a simple A/D converter that employs a comparator, an up/down counter, and a D/A converter. The comparator circuit provides an output that assumes one of two

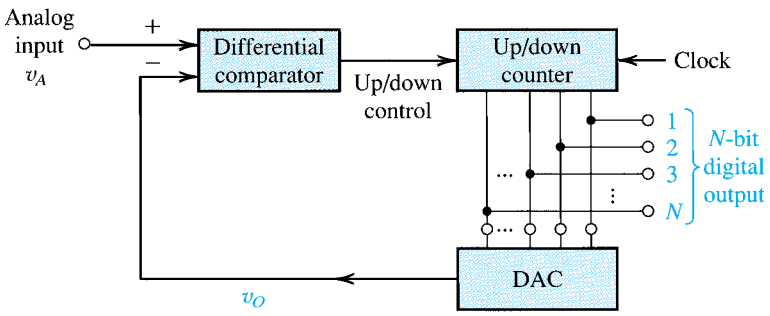


FIGURE 9.43 A simple feedback-type A/D converter.

distinct values: positive when the difference input signal is positive, and negative when the difference input signal is negative. We shall study comparator circuits in Chapter 13. An up/down counter is simply a counter that can count either up or down depending on the binary level applied at its up/down control terminal. Because the A/D converter of Fig. 9.43 employs a DAC in its feedback loop it is usually called a feedback-type A/D converter. It operates as follows: With a 0 count in the counter, the D/A converter output, v_O, will be zero and the output of the comparator will be high, instructing the counter to count the clock pulses in the up direction. As the count increases, the output of the DAC rises. The process continues until the DAC output reaches the value of the analog input signal, at which point the comparator switches and stops the counter. The counter output will then be the digital equivalent of the input analog voltage.

Operation of the converter of Fig. 9.43 is slow if it starts from zero. This converter however, tracks incremental changes in the input signal quite rapidly.

9.9.2 The Dual-Slope A/D Converter

A very popular high-resolution (12- to 14-bit) (but slow) A/D conversion scheme is illustrated in Fig. 9.44. To see how it operates, refer to Fig. 9.44 and assume that the analog input signal v_A is negative. Prior to the start of the conversion cycle, switch S_2 is closed, thus discharging capacitor C and setting $v_1 = 0$. The conversion cycle begins with opening S_2 and connecting the integrator input through switch S_1 to the analog input signal. Since v_A is negative, a current $I = v_A/R$ will flow through R in the direction away from the integrator. Thus v_1 rises linearly with a slope of $I/C = v_A/RC$, as indicated in Fig. 9.44(b). Simultaneously, the counter is enabled and it counts the pulses from a fixed-frequency clock. This phase of the conversion process continues for a fixed duration T_1. It ends when the counter has accumulated a fixed count denoted n_{REF}. Usually, for an N-bit converter, $n_{\text{REF}} = 2^N$. Denoting the peak voltage at the output of the integrator as V_{PEAK}, we can write with reference to Fig. 9.44(b)

$$\frac{V_{\text{PEAK}}}{T_1} = \frac{v_A}{RC} \tag{9.115}$$

At the end of this phase, the counter is reset to zero.

Phase II of the conversion begins at $t = T_1$ by connecting the integrator input through switch S_1 to the positive reference voltage V_{REF}. The current into the integrator reverses direction and is equal to V_{REF}/R. Thus v_1 decreases linearly with a slope of (V_{REF}/RC). Simultaneously the counter is enabled and it counts the pulses from the fixed-frequency clock. When v_1 reaches zero volts, the comparator signals the control logic to stop the counter. Denoting the duration of phase II by T_2, we can write, by reference to Fig. 9.44(b),

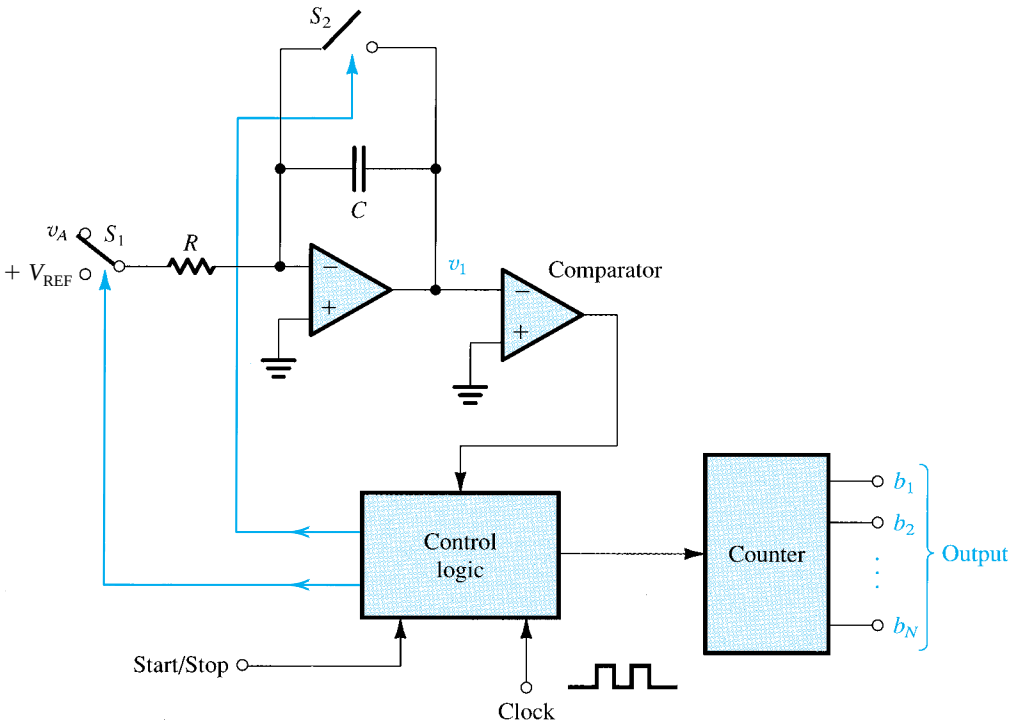
$$\frac{V_{\text{PEAK}}}{T_2} = \frac{V_{\text{REF}}}{RC} \tag{9.116}$$

Equations (9.115) and (9.116) can be combined to yield

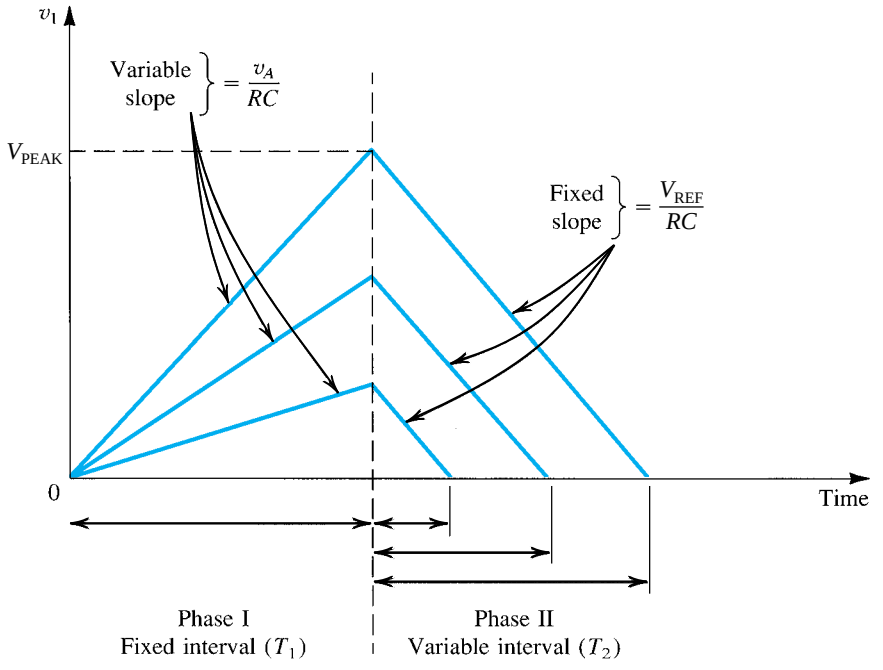
$$T_2 = T_1\left(\frac{v_A}{V_{\text{REF}}}\right) \tag{9.117}$$

Since the counter reading, n_{REF}, at the end of T_1 is proportional to T_1 and the reading, n, at the end of T_2 is proportional to T_2, we have

$$n = n_{\text{REF}}\left(\frac{v_A}{V_{\text{REF}}}\right) \tag{9.118}$$



(a)



(b)

FIGURE 9.44 The dual-slope A/D conversion method. Note that v_A is assumed to be negative.

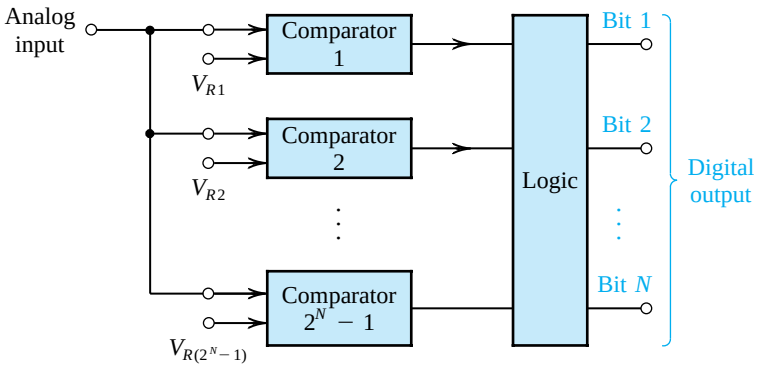


FIGURE 9.45 Parallel, simultaneous, or flash A/D conversion.

Thus the content of the counter,[5] n, at the end of the conversion process is the digital equivalent of v_A.

The dual-slope converter features high accuracy, since its performance is independent of the exact values of R and C. There exist many commercial implementations of the dual-slope method, some of which utilize CMOS technology.

9.9.3 The Parallel or Flash Converter

The fastest A/D conversion scheme is the simultaneous, parallel, or flash conversion process illustrated in Fig. 9.45. Conceptually, flash conversion is very simple. It utilizes $2^N - 1$ comparators to compare the input signal level with each of the $2^N - 1$ possible quantization levels. The outputs of the comparators are processed by an encoding-logic block to provide the N bits of the output digital word. Note that a complete conversion can be obtained within one clock cycle.

Although flash conversion is very fast, the price paid is a rather complex circuit implementation. Variations on the basic technique have been successfully employed in the design of IC converters.

9.9.4 The Charge-Redistribution Converter

The last A/D conversion technique that we shall discuss is particularly suited for CMOS implementation. As shown in Fig. 9.46, the circuit utilizes a binary-weighted capacitor array, a voltage comparator, and analog switches; control logic (not shown in Fig. 9.46) is also required. The circuit shown is for a 5-bit converter; capacitor C_T serves the purpose of terminating the capacitor array, making the total capacitance equal to the desired value of $2C$.

Operation of the converter can be divided into three distinct phases, as illustrated in Fig. 9.46. In the sample phase (Fig. 9.46a) switch S_B is closed, thus connecting the top plate of all capacitors to ground and setting v_O to zero. Meanwhile, switch S_A is connected to the analog input voltage v_A. Thus the voltage v_A appears across the total capacitance of $2C$, resulting in a stored charge of $2Cv_A$. Thus, during this phase, a sample of v_A is taken and a proportional amount of charge is stored on the capacitor array.

[5] Note that n is *not* a continuous function of v_A, as might be inferred from Eq. (9.118). Rather, n takes on discrete values corresponding to one of the 2^N quantized levels of v_A.

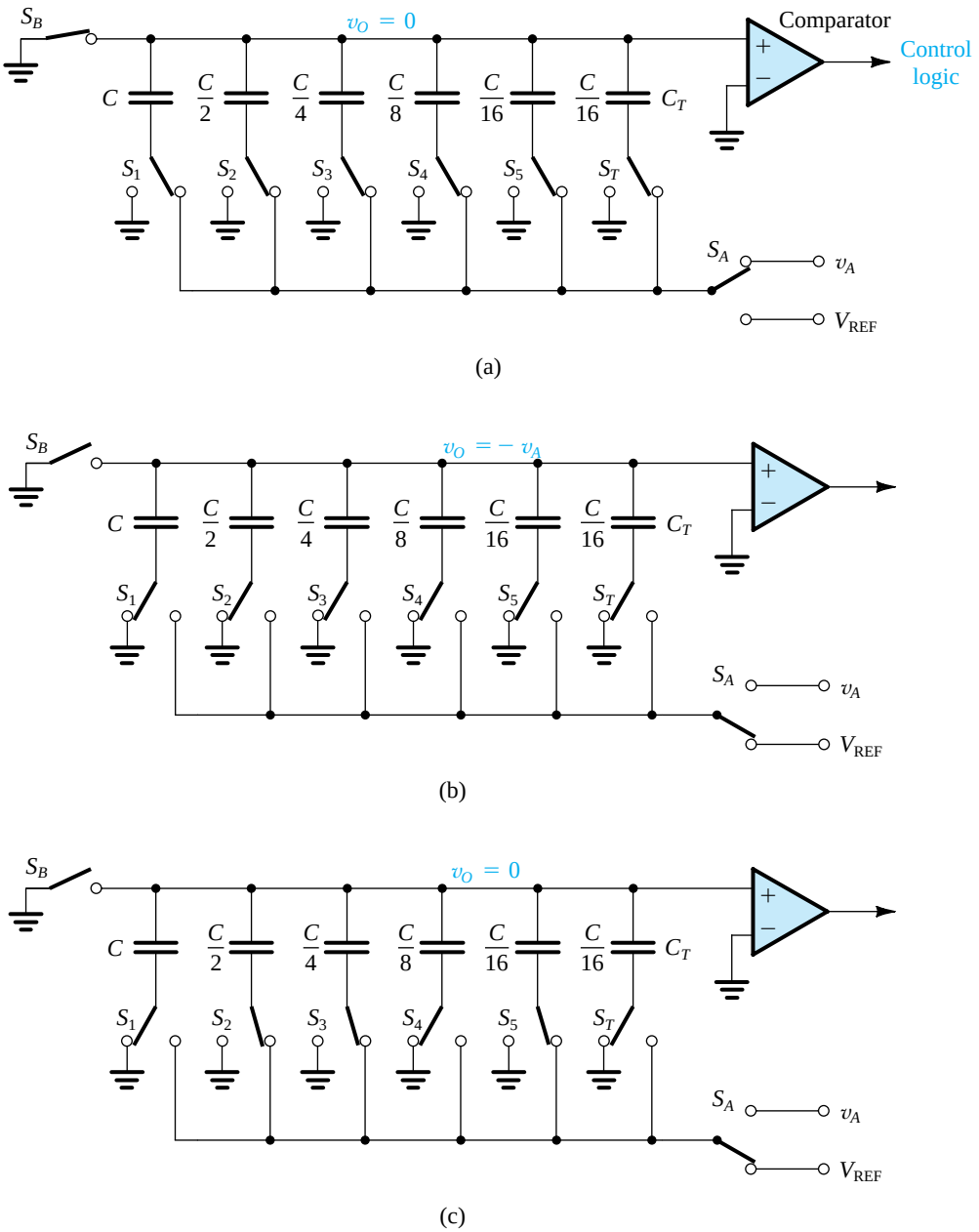


FIGURE 9.46 Charge-redistribution A/D converter suitable for CMOS implementation: **(a)** sample phase, **(b)** hold phase, and **(c)** charge-redistribution phase.

During the hold phase (Fig. 9.46b), switch S_B is opened and switches S_1 to S_5, and S_T are thrown to the ground side. Thus the top plate of the capacitor array is open-circuited while their bottom plates are connected to ground. Since no discharge path has been provided, the capacitor charges must remain constant, with the total equal to $2Cv_A$. It follows that the voltage at the top plate must become $-v_A$. Finally, note that during the hold phase, S_A is connected to V_{REF} in preparation for the charge-redistribution phase.