of Q_2 is loaded with a current-source load (as before), the output signal developed is fed back to the drain of Q_1 via the source follower Q_3. The small-signal analysis of the circuit is illustrated in Fig. 6.45(b) where the current sources I and $I/2$ have been assumed ideal and thus replaced with open circuits. To determine the voltage gain, we have grounded the gate terminal of Q_2 and applied the differential input signal v_i to the gate of Q_1. The analysis proceeds along the following steps:

1. From the output node we see that $i_{d2} = 0$.
2. From the sources node, since $i_{d2} = 0$, we find that $i_{d1} = 0$.
3. From the node at the drain of Q_1, since $i_{d1} = 0$, we find that $i_{d3} = 0$.
4. Writing for each transistor

$$i_d = g_m v_{gs} + v_{ds} / r_o = 0$$

we obtain three equations in the three unknowns v_{d1}, v_s, and v_o. The solution yields

$$\frac{v_o}{v_i} = g_{m1} r_{o1} \Big/ \left[\frac{g_{m1} r_{o1} + 1}{g_{m2} r_{o2} + 1} - \frac{g_{m3} r_{o3}}{g_{m3} r_{o3} + 1} \right] \tag{6.139}$$

If all three transistors have the same geometry and are operating at equal dc currents, their g_m and r_o values will be equal and the expression in Eq. (6.139) reduces to

$$\frac{v_o}{v_i} \simeq (g_m r_o)^2 \tag{6.140}$$

Thus application of positive feedback through follower Q_3 enables one to obtain a gain equal to the square of that naturally available from a single stage!

EXERCISE

6.26 Using the device data given in Table 5.2, find the gain of the differential amplifier circuit of Fig. 6.45(a) for $I = 10$ mA and $W_1 = W_2 = W_3 = 100$ μm.

Ans. 784 V/V

14.8 GALLIUM-ARSENIDE DIGITAL CIRCUITS

We conclude our study of digital-circuit families with a discussion of logic circuits implemented using the emerging technology of gallium arsenide. An introduction to this technology and its two basic devices, the MESFET and the Schottky-barrier diode (SBD), was given in Section 5.12. We urge the reader to review Section 5.12 before proceeding with the study of this section.

The major advantage that GaAs technology offers is a higher speed of operation than currently achievable using silicon devices. Gate delays of 10 to 100 ps have been reported for GaAs circuits. The disadvantages are a relatively high power dissipation per gate (1 to 10 mW); relatively small voltage swings and, correspondingly, narrow noise margins; low packing density, mostly as a result of the high-power dissipation per gate; and low manufacturing yield. The present state of affairs is that a few specialized manufacturers produce SSI, MSI, and some LSI digital circuits performing relatively specialized functions, with a cost per gate considerably higher than that of silicon digital ICs. Nevertheless, the very high

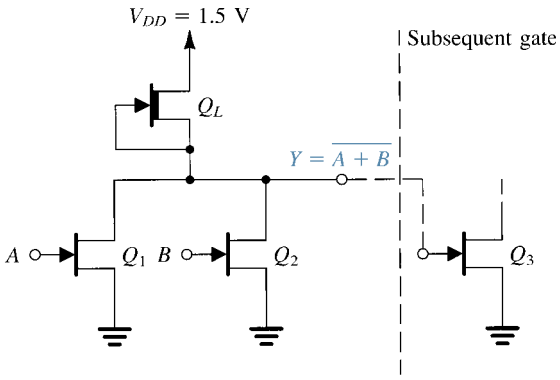

FIGURE 14.47 A DCFL GaAs gate implementing a two-input NOR function. The gate is shown driving the input transistor Q_3 of another gate.

speeds of operation achievable in GaAs circuits make it a worthwhile technology whose applications will possibly grow.

Unlike the CMOS logic circuits that we have studied in Chapter 13, and the bipolar logic families that we have studied in earlier sections of this chapter, there are no standard GaAs logic-circuit families. The lack of standards extends not only to the topology of the basic gates but also to the power-supply voltages used. In the following we present examples of the most popular GaAs logic gate circuits.

Direct-Coupled FET Logic (DCFL)

Direct-coupled FET logic (DCFL) is the simplest form of GaAs digital logic circuits. The basic gate is shown in Fig. 14.47. The gate utilizes enhancement MESFETs, Q_1 and Q_2, for the input switching transistors, and a depletion MESFET for the load transistor Q_L. The gate closely resembles the now obsolete depletion-load MOSFET circuit. The GaAs circuit of Fig. 14.47 implements a two-input NOR function.

To see how the MESFET circuit of Fig. 14.47 operates, ignore input B and consider the basic inverter formed by Q_1 and Q_L. When the input voltage applied to node A, v_I, is lower than the threshold voltage of the enhancement MESFET Q_1, denoted V_{tE}, transistor Q_1 will be off. Recall that V_{tE} is positive and for GaAs MESFETs is typically 0.1 to 0.3 V. Now if the gate output Y is open circuited, the output voltage will be very close to V_{DD}. In practice, however, the gate will be driving another gate, as indicated in Fig. 14.47, where Q_3 is the input transistor of the subsequent gate. In such a case, current will flow from V_{DD} through Q_L and into the gate terminal of Q_3. Recalling that the gate to source of a GaAs MESFET is a Schottky-barrier diode that exhibits a voltage drop of about 0.7 V when conducting, we see that the gate conduction of Q_3 will clamp the output high voltage (V_{OH}) to about 0.7 V. This is in sharp contrast to the MOSFET case, where no gate conduction takes place.

Figure 14.48 shows the DCFL inverter under study with the input of the subsequent gate represented by a Schottky diode Q_3. With $v_I < V_{tE}$, $i_1 = 0$ and i_L flows through Q_3 resulting in $v_O = V_{OH} \simeq 0.7$ V. Since V_{DD} is usually low (1.2 to 1.5 V) and the threshold voltage of Q_L, V_{tD}, is typically –0.7 to –1 V, Q_L will be operating in the triode region. (To simplify matters, we shall ignore in this discussion the early-saturation effect exhibited by GaAs MESFETs.)

As v_I is increased above V_{tE}, Q_1 turns on and conducts a current denoted i_1. Initially, Q_1 will be in the saturation region. Current i_1 subtracts from i_L, thus reducing the current in Q_3. The voltage across Q_3, v_O, decreases slightly. However, for the present discussion we shall assume that v_O will remain close to 0.7 V as long as Q_3 is conducting. This will continue until v_I reaches the value that results in $i_1 = i_L$. At this point, Q_3 ceases conduction

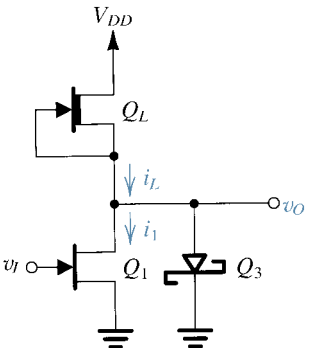

FIGURE 14.48 The DCFL gate with the input of the subsequent gate represented by a Schottky diode Q_3.

and can be ignored altogether. Further increase in v_I results in i_1 increasing, v_O decreasing, and $i_L = i_1$. When $(V_{DD} - v_O)$ exceeds $|V_{tD}|$, Q_L saturates; and when v_O falls below v_I by V_{tE}, Q_1 enters the triode region. Eventually, when $v_I = V_{OH} = 0.7$ V, $v_O = V_{OL}$, which is typically 0.1 to 0.2 V.

From the description above we see that the output voltage swing of the DCFL gate is limited by gate conduction to a value less than 0.7 V (typically 0.5 V or so). Further details on the operation of the DCFL gate are illustrated by the following example.

EXAMPLE 14.3

Consider a DCFL gate fabricated in a GaAs technology for which $L = 1$ μm, $V_{tD} = -1$ V, $V_{tE} = 0.2$ V, β (for 1-μm width) $= 10^{-4}$ A/V^2, and $\lambda = 0.1$ V^{-1}. Let the widths of the input MESFETs be 50 μm, and let the width of the load MESFET be 6 μm. $V_{DD} = 1.5$ V. Using a constant-voltage-drop model for the gate-source Schottky diode with $V_D = 0.7$ V, and neglecting the early-saturation effect of GaAs MESFETs (that is, using Eqs. 5.120 to describe MESFET operation), find V_{OH}, V_{OL}, V_{IH}, NM_H, NM_L, the static power dissipation, and the propagation delay for a total equivalent capacitance at the gate output of 30 fF.

Solution

From the description above of the operation of the DCFL gate we found that $V_{OH} = 0.7$ V. To obtain V_{OL}, we consider the inverter in the circuit of Fig. 14.48 and let $v_I = V_{OH} = 0.7$ V. Since we expect $v_O = V_{OL}$ to be small, we assume Q_1 to be in the triode region and Q_L to be in saturation. (Q_3 is of course off.) Equating i_1 and i_L gives the equation

$$\beta_1[2(0.7 - 0.2)V_{OL} - V_{OL}^2](1 + 0.1V_{OL}) = \beta_L[0 - (-1)]^2[1 + 0.1(1.5 - V_{OL})]$$

To simplify matters, we neglect the terms $0.1V_{OL}$ and substitute $\beta_L/\beta_1 = W_L/W_1 = 6/50$ to obtain a quadratic equation in V_{OL} whose solution gives $V_{OL} \simeq 0.17$ V.

Toward obtaining the value of V_{IL} we shall first find the value of v_I at which $i_1 = i_L$, the diode Q_3 turns off, and v_O begins to decrease. Since at this point $v_O = 0.7$ V, we assume that Q_1 is in saturation. Transistor Q_L has a v_{DS} of 0.8 V, which is less than $|V_{tD}|$ and is thus in the triode region. Equating i_1 and i_L gives

$$\beta_1(v_I - 0.2)^2(1 + 0.1 \times 0.7) = \beta_L[2(1)(1.5 - 0.7) - (1.5 - 0.7)^2][1 + 0.1(1.5 - 0.7)]$$

Substituting $\beta_L/\beta_1 = W_L/W_1 = 6/50$ and solving the resulting equation yields $v_I = 0.54$ V. Figure 14.49 shows a sketch of the transfer characteristic of the inverter. The slope dv_O/dv_I at

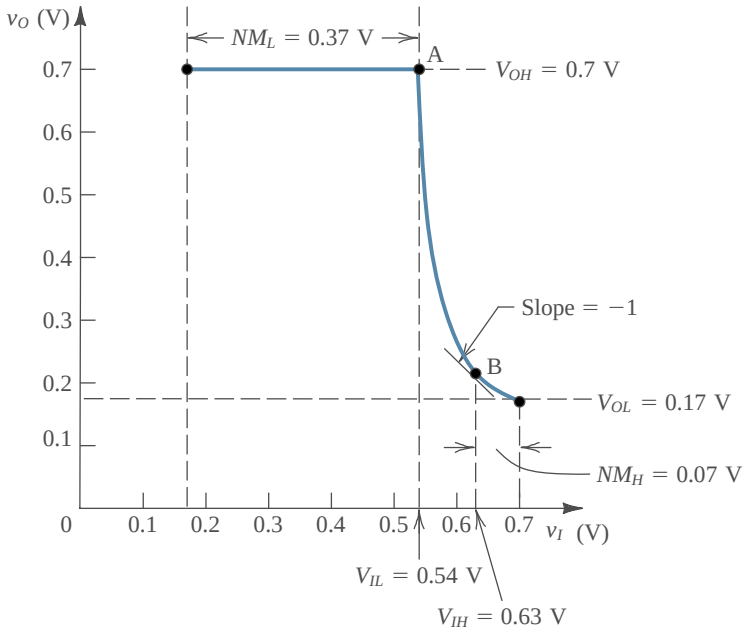

FIGURE 14.49 Transfer characteristic of the DCFL inverter of Fig. 14.48.

point A can be found to be −14.2 V/V. We shall consider point A as the point at which the inverter begins to switch from the high-output state; thus $V_{IL} \simeq 0.54$ V.

To obtain V_{IH}, we find the co-ordinates of point B at which $dv_O/dv_I = -1$. This can be done using a procedure similar to that employed for the MOSFET inverters and assuming Q_1 to be in the triode region and Q_L to be in saturation. Neglecting terms in $0.1v_O$, the result is $V_{IH} \simeq 0.63$ V. The noise margins can now be found as

$$NM_H \equiv V_{OH} - V_{IH} = 0.7 - 0.63 = 0.07 \text{ V}$$

$$NM_L \equiv V_{IL} - V_{OL} = 0.54 - 0.17 = 0.37 \text{ V}$$

The static power dissipation is determined by finding the supply current I_{DD} in the output-high and the output-low cases. When the output is high (at 0.7 V), Q_L is in the triode region and the supply current is

$$I_{DD} = \beta_L[2(0+1)(1.5-0.7) - (1.5-0.7)^2][1 + 0.1(1.5-0.7)]$$

Substituting $\beta_L = 10^{-4} \times W_L = 0.6$ mA/V^2 results in

$$I_{DD} = 0.61 \text{ mA}$$

When the output is low (at 0.17 V), Q_L is in saturation and the supply current is

$$I_{DD} = \beta_L(0+1)^2[1 + 0.1(1.5-0.17)] = 0.68 \text{ mA}$$

Thus the average supply current is

$$I_{DD} = \tfrac{1}{2}(0.61 + 0.68) = 0.645 \text{ mA}$$

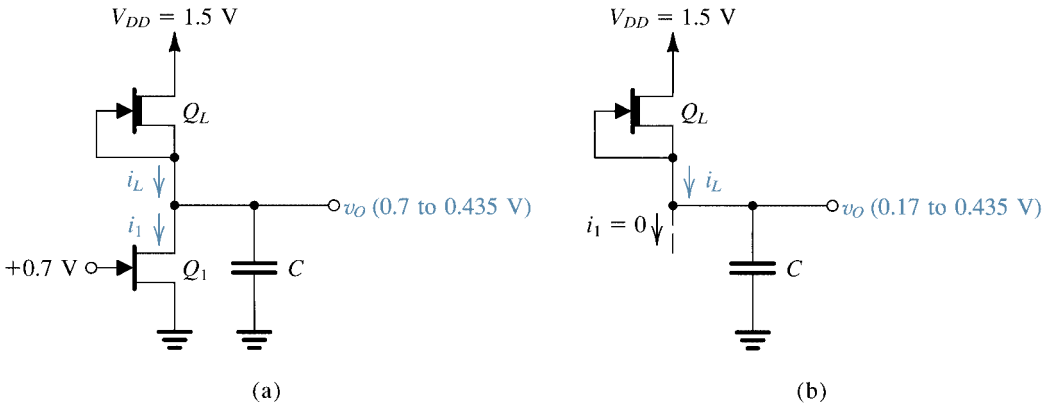

FIGURE 14.50 Circuits for calculating the propagation delays of the DCFL inverter: **(a)** t_{PHL}; **(b)** t_{PLH}.

and the static power dissipation is

$$P_D = 0.645 \times 1.5 \simeq 1 \text{ mW}$$

The propagation delay t_{PHL} is the time for the output voltage of the inverter to decrease from $V_{OH} = 0.7$ V to $\frac{1}{2}(V_{OH} + V_{OL}) = 0.435$ V. During this time v_I is at the high level of 0.7 V, and the capacitance C (assumed to be 30 fempto Farads [fF]) is discharged by $(i_1 - i_L)$; refer to Fig. 14.50(a). The average discharge current is found by calculating i_1 and i_L at the beginning and at the end of the discharge interval. The result is that i_1 changes from 1.34 mA to 1.28 mA and i_L changes from 0.61 mA to 0.66 mA. Thus the discharge current $(i_1 - i_L)$ changes from 0.73 mA to 0.62 mA for an average value of 0.675 mA. Thus

$$t_{PHL} = \frac{C\Delta V}{I} = \frac{30 \times 10^{-15}(0.7 - 0.435)}{0.675 \times 10^{-3}} = 11.8 \text{ ps}$$

To determine t_{PLH} we refer to the circuit in Fig. 14.50(b) and note that during t_{PLH}, v_O changes from $V_{OL} = 0.17$ V to $\frac{1}{2}(V_{OH} + V_{OL}) = 0.435$ V. The charging current is the average value of i_L, which changes from 0.8 mA to 0.66 mA. Thus $i_{L|\text{average}} = 0.73$ mA and

$$t_{PLH} = \frac{30 \times 10^{-15} \times (0.435 - 0.17)}{0.73 \times 10^{-3}} = 10.9 \text{ ps}$$

The propagation delay of the DCFL gate can now be found as

$$t_P = \tfrac{1}{2}(t_{PHL} + t_{PLH}) = 11.4 \text{ ps}$$

As a final remark, we note that the analysis above was done using simplified device models; our objective is to show how the circuit works rather than to find accurate performance measures. These can be obtained using SPICE simulation with more elaborate models [see Roberts and Sedra (1997)].

Logic Gates Using Depletion MESFETs

The DCFL circuits studied above require both enhancement and depletion devices and thus are somewhat difficult to fabricate. Also, owing to the fact that the voltage swings and noise margins are rather small, very careful control of the value of V_{tE} is required in fabrication. As an alternative, we now present circuits that utilize depletion devices only.

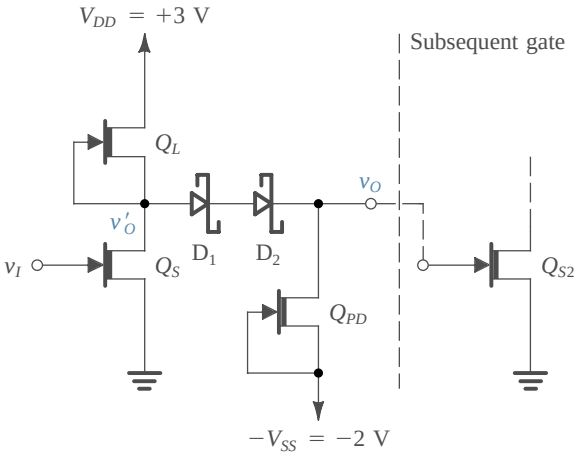

FIGURE 14.51 An inverter circuit utilizing depletion-mode devices only. Schottky diodes are employed to shift the output logic levels to values compatible with the input levels required to turn the depletion MESFET Q_S on and off. This circuit is known as FET logic (FL).

Figure 14.51 shows the basic inverter circuit of a family of GaAs logic circuits known at FET logic (FL). The heart of the FL inverter is formed by the switching transistor Q_S and its load Q_L—both depletion-type MESFETs. Since the threshold voltage of a depletion MESFET, V_{tD}, is negative, a negative voltage $<V_{tD}$ is needed to turn Q_S off. On the other hand the output low voltage at the drain of Q_S will always be positive. It follows that the logic levels at the drain of Q_S are not compatible with the levels required at the gate input. The incompatibility problem is solved by simply shifting the level of the voltage v'_O down by two diode drops, that is, by approximately 1.4 V. This level shifting is accomplished by the two Schottky diodes D_1 and D_2. The depletion transistor Q_{PD} provides a constant-current bias for D_1 and D_2. To ensure that Q_{PD} operates in the saturation region at all times, its source is connected to a negative supply $-V_{SS}$, and the value of V_{SS} is selected to be equal to or greater than the lowest level of $v_O(V_{OL})$ plus the magnitude of the threshold voltage, $|V_{tD}|$. Transistor Q_{PD} also supplies the current required to discharge a load capacitance when the output voltage of the gate goes low, hence the name "pull-down" transistor and the subscript *PD*.

To see how the inverter of Fig. 14.51 operates, refer to its transfer characteristic, shown in Fig. 14.52. The circuit is usually designed using MESFETs having equal channel lengths (typically 1 μm) and having widths $W_S = W_L = 2W_{PD}$. The transfer characteristic shown is for the case $V_{tD} = -0.9$ V. For v_I lower than V_{tD}, Q_S will be off and Q_L will operate in saturation, supplying a constant current I_L to D_1 and D_2. Transistor Q_{PD} will also operate in saturation with a constant current $I_{PD} = \frac{1}{2}I_L$. The difference between the two currents will flow through the gate terminal of the input transistor of the next gate in the chain, Q_{S2}. Thus the input Schottky diode of Q_{S2} clamps the output voltage v_O to approximately 0.7 V, which is the output high level, V_{OH}. (Note that for this discussion we shall neglect the finite output resistance in saturation.)

As v_I is raised above V_{tD}, Q_S turns on. Since its drain is at +2.1 V, Q_S will operate in the saturation region and will take away some of the current supplied by Q_L. Thus the current flowing into the gate of Q_{S2} decreases by an equal amount. If we keep increasing v_I, a value is reached for which the current in Q_S equals $\frac{1}{2}I_L$, thus leaving no current to flow through the gate of Q_{S2}. This corresponds to the point labeled A on the transfer characteristic. A further slight increase in v_I will cause the voltage v'_O to fall to the point B where Q_S enters the triode region. The segment AB of the transfer curve represents the high-gain region of operation, having a slope equal to $-g_{ms}R$ where R denotes the total equivalent resistance at the drain node. Note that this segment is shown as vertical in Fig. 14.52 because we are neglecting the output resistance in saturation.

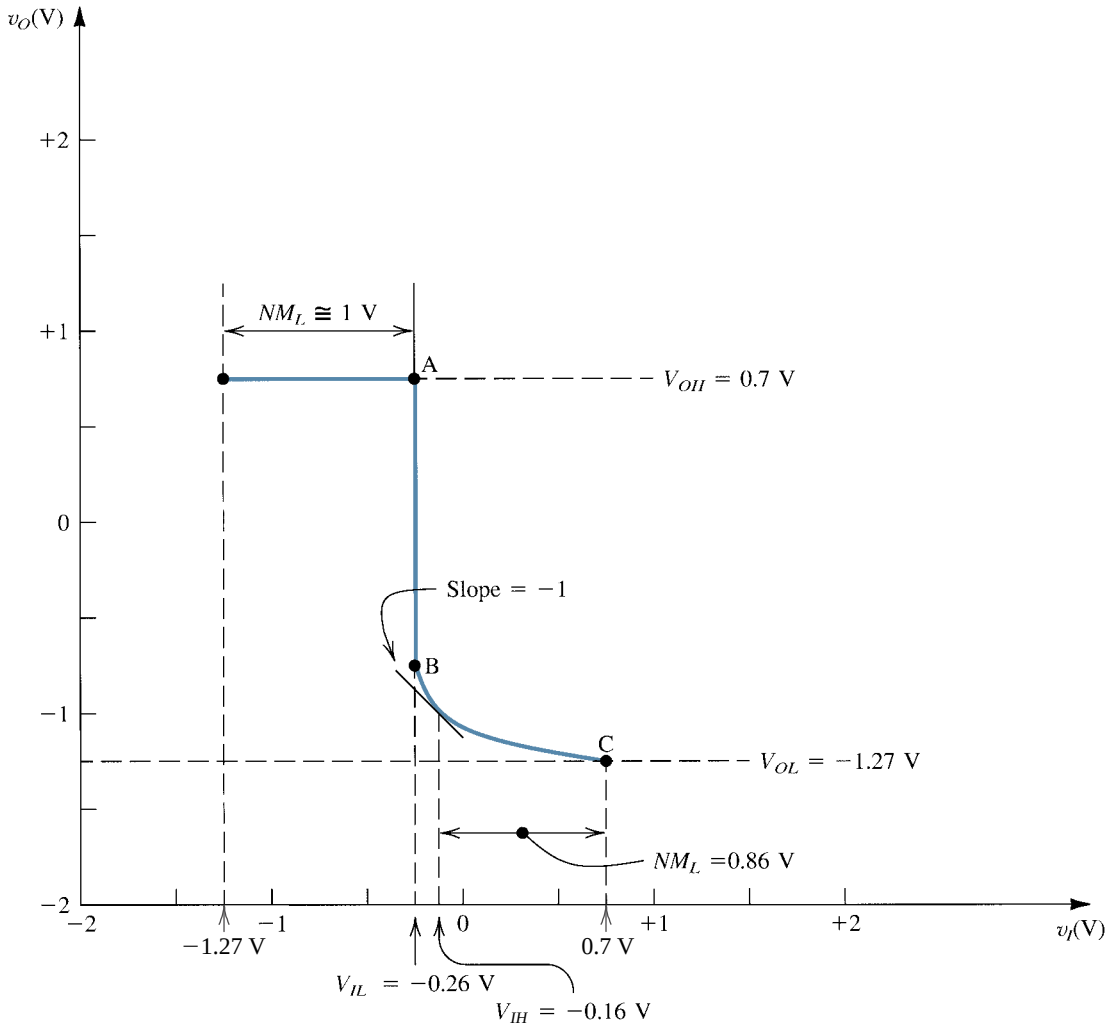

FIGURE 14.52 Transfer characteristic of the FL inverter of Fig. 14.51.

The segment BC of the transfer curve corresponds to Q_S operating in the triode region. Here Q_L and Q_{PD} continue to operate in saturation and D_1 and D_2 remain conducting. Finally, for $v_I = V_{OH} = 0.7$ V, $v_O = V_{OL}$, which for the case $V_{tD} = -0.9$ V can be found to be –1.3 V.

EXERCISE

14.30 Verify that the co-ordinates of points A, B, and C of the transfer characteristic are as indicated in Fig. 14.52. Let $V_{tD} = -0.9$ V and $\lambda = 0$.

As indicated in Fig. 14.52, the FL inverter exhibits much higher noise margins than those for the DCFL circuit. The FL inverter, however, requires two power supplies.

The FL inverter can be used to construct a NOR gate by simply adding transistors with drain and source connected in parallel with those of Q_S.

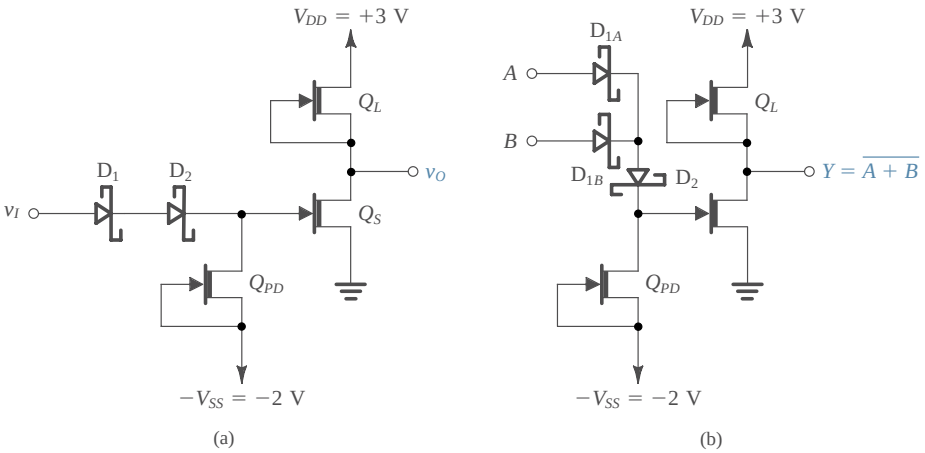

FIGURE 14.53 **(a)** An SDFL inverter. **(b)** An SDFL NOR gate.

Schottky Diode FET Logic (SDFL)

If the diode level-shifting network of the FL inverter is connected at the input side of the gate, rather than at the output side, we obtain the circuit shown in Fig. 14.53(a). This inverter operates in much the same manner as the FL inverter. The modified circuit, however, has a very interesting feature: The NOR function can be implemented by simply connecting additional diodes, as shown in Fig. 14.53(b). This logic form is known as Schottky diode FET logic (SDFL). SDFL permits higher packing density than other forms of MESFET logic because only an additional diode, rather than an additional transistor, is required for each additional input, and diodes require much smaller areas than transistors.

Buffered FET Logic (BFL)

Another variation on the basic FL inverter of Fig. 14.51 is possible. A source follower can be inserted between the drain of Q_S and the diode level-shifting network. The resulting gate, shown for the case of a two-input NOR, is depicted in Fig. 14.54. This form of GaAs logic circuit is known as buffered FET logic (BFL). The source-follower transistor Q_{SF} increases the output current-driving capability, thus decreasing the low-to-high propagation time. FL, BFL, and SDFL feature propagation delays of the order of 100 ps and power dissipation of the order of 10 mW/gate.

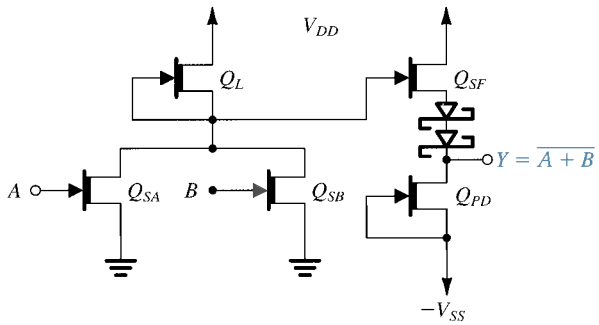

FIGURE 14.54 A BFL two-input NOR gate. The gate is formed by inserting a source-follower transistor Q_{SF} between the inverting stage and the level-shifting stage.