CHAPTER 7

Building Blocks of Integrated-Circuit Amplifiers

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IN THIS CHAPTER YOU WILL LEARN

1. The basic integrated-circuit (IC) design philosophy and how it differs from that for discrete-circuit design.
2. The basic gain cells of IC amplifiers, namely, the CS and CE amplifiers with current-source loads.
3. How to increase the gain realized in the basic gain cells by employing the principle of cascoding.
4. Analysis and design of the cascode amplifier and the cascode current source in both their MOS and bipolar forms.
5. How current sources are used to bias IC amplifiers and how the reference current generated in one location is replicated at various other locations on the IC chip by using current mirrors.
6. Some ingenious analog circuit design techniques that result in current mirrors with vastly improved characteristics.
7. How to pair transistors to realize amplifiers with characteristics superior to those obtained from a single-transistor stage.

Introduction

Having studied the two major transistor types, the MOSFET and the BJT, and their basic discrete-circuit amplifier configurations, we are now ready to begin the study of integrated-circuit (IC) amplifiers. This chapter is devoted to the design of the basic building blocks of IC amplifiers.

We begin with a brief section on the design philosophy of integrated circuits and how it differs from that of discrete circuits. Throughout this chapter, MOS and bipolar circuits are presented side by side, which allows a certain economy in presentation and, more importantly, provides an opportunity to compare and contrast the two circuit types. Toward that end, Appendix 7.A provides a comprehensive comparison of the attributes of the two transistor types. This should serve both as a condensed review and as a guide to very interesting similarities and differences between the two devices. Appendix 7.A can be consulted at any time during the study of this or any of the remaining chapters of the book.

The heart of this chapter is the material in Sections 7.2 to 7.4. In Section 7.2 we present the basic gain cell of IC amplifiers, namely, the current-source-loaded common-source (common-emitter) amplifier. We then ask the question of how to increase its gain. This leads naturally and seamlessly to the principle of cascoding and its application in amplifier

design: namely, the cascode amplifier and the cascode current source, which are very important building blocks of IC amplifiers.

Section 7.4 is devoted to IC biasing and the study of another key IC building block, the current mirror. We study a collection of current-mirror circuits with improved performance in Section 7.5, for their significance and usefulness, but also because they embody ideas that illustrate the beauty and power of analog circuit design. The chapter concludes with the presentation in Section 7.6 of an interesting and useful collection of amplifier configurations, each utilizing a pair of transistors.

7.1 IC Design Philosophy

Integrated-circuit fabrication technology (Appendix A) imposes constraints on—and provides opportunities to—the circuit designer. Thus, while chip-area considerations dictate that large- and even moderate-value resistors are to be avoided, constant-current sources are readily available. Large capacitors, such as those we used in Sections 5.8 and 6.8 for signal coupling and bypass, are not available to be used, except perhaps as components external to the IC chip. Even then, the number of such capacitors has to be kept to a minimum; otherwise the number of chip terminals increases, and hence the cost. Very small capacitors, in the picofarad and fraction-of-a-picofarad range, however, are easy to fabricate in IC MOS technology and can be combined with MOS amplifiers and MOS switches to realize a wide range of signal processing functions, both analog (Chapter 16) and digital (Chapter 14).

As a general rule, in designing IC MOS circuits, one should strive to realize as many of the functions required as possible using MOS transistors only and, when needed, small MOS capacitors. MOS transistors can be sized; that is, their W and L values can be selected to fit a wide range of design requirements. Also, arrays of transistors can be matched (or, more generally, made to have desired size ratios) to realize such useful circuit building blocks as current mirrors.

At this juncture, it is useful to mention that to pack a larger number of devices on the same IC chip, the trend has been to reduce the device dimensions. By 2009, CMOS process technologies capable of producing devices with a 45-nm minimum channel length were in use. Such small devices need to operate with dc voltage supplies close to 1 V. While low-voltage operation can help to reduce power dissipation, it poses a host of challenges to the circuit designer. For instance, such MOS transistors must be operated with overdrive voltages of only 0.1 V to 0.2 V. In our study of MOS amplifiers, we will make frequent comments on such issues.

The MOS-amplifier circuits that we shall study will be designed almost entirely using MOSFETs of both polarities—that is, NMOS and PMOS—as are readily available in CMOS technology. As mentioned earlier, CMOS is currently the most widely used IC technology for both analog and digital as well as combined analog and digital (or mixed-signal) applications. Nevertheless, bipolar integrated circuits still offer many exciting opportunities to the analog design engineer. This is especially the case for general-purpose circuit packages, such as high-quality op amps that are intended for assembly on printed-circuit (pc) boards (as opposed to being part of a system-on-chip). As well, bipolar circuits can provide much higher output currents and are favored for certain applications, such as in the automotive industry, for their high reliability under severe environmental conditions. Finally, bipolar circuits can be combined with CMOS in innovative and exciting ways in what is known as BiCMOS technology.

7.2 The Basic Gain Cell

7.2.1 The CS and CE Amplifiers with Current-Source Loads

The basic gain cell in an IC amplifier is a common-source (CS) or common-emitter (CE) transistor loaded with a constant-current source, as shown in Fig. 7.1(a) and (b). These circuits are similar to the CS and CE amplifiers studied in Sections 5.6 and 6.6, except that here we have replaced the resistances R_D and R_C with constant-current sources. This is done for two reasons: First, as mentioned in Section 7.1, it is difficult in IC technology to implement resistances with reasonably precise values; rather, it is much easier to use current sources, which are implemented using transistors, as we shall see shortly. Second, by using a constant-current source we are in effect operating the CS and CE amplifiers with a very high (ideally infinite) load resistance; thus we can obtain a much higher gain than if a finite R_D or R_C is used. The circuits in Fig. 7.1(a) and (b) are said to be **current-source loaded** or **active loaded**.

Before we consider the small-signal analysis of the active-loaded CS and CE amplifiers, a word on their dc bias is in order. Obviously, in each circuit Q_1 is biased at $I_D = I$ and $I_C = I$. But what determines the dc voltages at the drain (collector) and at the gate (base)? Usually, these gain cells will be part of larger circuits in which negative feedback is utilized to fix the values of V_{DS} and V_{GS} (V_{CE} and V_{BE}). We shall be discussing dc biasing later in this chapter. As well, in the next chapter we will begin to see complete IC amplifiers including biasing. For the time being, however, we shall assume that the MOS transistor in Fig. 7.1(a) is biased to operate in the saturation region and that the BJT in Fig. 7.1(b) is biased to operate in the active region. We will often refer to both the MOSFET and the BJT as operating in the "active region."

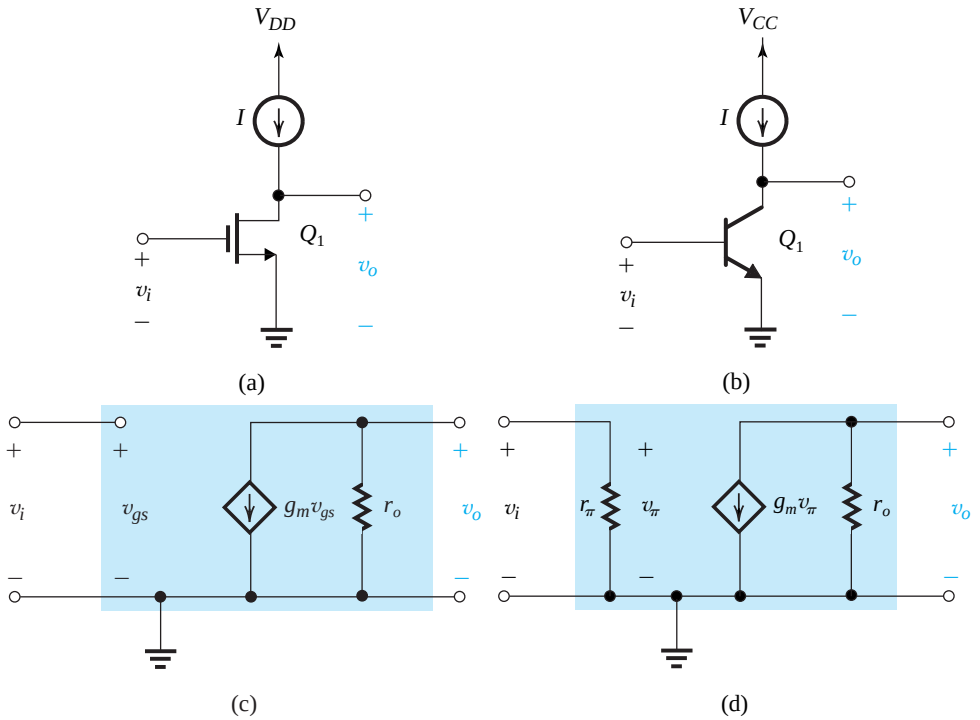


Figure 7.1 The basic gain cells of IC amplifiers: **(a)** current-source- or active-loaded common-source amplifier; **(b)** current-source- or active-loaded common-emitter amplifier; **(c)** small-signal equivalent circuit of **(a)**; and **(d)** small-signal equivalent circuit of **(b)**.

Small-signal analysis of the current-source-loaded CS and CE amplifiers can be performed by utilizing their equivalent-circuit models, shown respectively in Fig. 7.1(c) and (d). Observe that since the current-source load is assumed to be ideal, it is represented in the models by an infinite resistance. Practical current sources will have finite output resistance, as we shall see shortly. For the time being, however, note that the CS and CE amplifiers of Fig. 7.1 are in effect operating in an open-circuit fashion. The only resistance between their output node and ground is the output resistance of the transistor itself, r_o. Thus the voltage gain obtained in these circuits is the maximum possible for a CS or a CE amplifier.

From Fig. 7.1(c) we obtain for the active-loaded CS amplifier:

$$R_{\text{in}} = \infty \tag{7.1}$$

$$A_{vo} = -g_m r_o \tag{7.2}$$

$$R_o = r_o \tag{7.3}$$

Similarly, from Fig. 7.1(d) we obtain for the active-loaded CE amplifier:

$$R_{\text{in}} = r_\pi \tag{7.4}$$

$$A_{vo} = -g_m r_o \tag{7.5}$$

$$R_o = r_o \tag{7.6}$$

Thus both circuits realize a voltage gain of magnitude $g_m r_o$. Since this is the maximum gain obtainable in a CS or CE amplifier, we refer to it as the **intrinsic gain** and give it the symbol A_0. Furthermore, it is useful to examine the nature of A_0 in a little more detail.

7.2.2 The Intrinsic Gain

For the BJT, we can derive a formula for the intrinsic gain $A_{vo} = g_m r_o$ by using the following formulas for g_m and r_o:

$$g_m = \frac{I_C}{V_T} \tag{7.7}$$

$$r_o = \frac{V_A}{I_C} \tag{7.8}$$

The result is

$$A_0 = g_m r_o = \frac{V_A}{V_T} \tag{7.9}$$

Thus A_0 is simply the ratio of the Early voltage V_A, which is a technology-determined parameter, and the thermal voltage V_T, which is a physical parameter (approximately 0.025 V at room temperature). The value of V_A ranges from 5 V to 35 V for modern IC fabrication processes to 100 V to 130 V for the older, so-called high-voltage processes (see chapter appendix, Section 7.A.1). As a result, the value of A_0 will be in the range of 200 V/V to 5000 V/V, with the lower values characteristic of modern small-feature-size devices. It is important to note that for a given bipolar-transistor fabrication process, A_0 is independent of the transistor junction area and of its bias current. This is not the case for the MOSFET, as we shall now see.

Recall from our study of the MOSFET g_m in Section 5.5, that there are three possible expressions for g_m. Two of these are particularly useful for our purposes here:

$$g_m = \frac{I_D}{V_{OV}/2} \tag{7.10}$$

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)}\ \sqrt{I_D} \tag{7.11}$$

For the MOSFET r_o we have

$$r_o = \frac{V_A}{I_D} = \frac{V_A' L}{I_D} \tag{7.12}$$

where V_A is the Early voltage and V_A' is the technology-dependent component of the Early voltage. Utilizing each of the g_m expressions together with the expression for r_o, we obtain for A_0,

$$A_0 = \frac{V_A}{V_{OV}/2} \tag{7.13}$$

which can be expressed in the alternate forms

$$A_0 = \frac{2V_A' L}{V_{OV}} \tag{7.14}$$

and

$$A_0 = \frac{V_A' \sqrt{2(\mu_n C_{ox})(WL)}}{\sqrt{I_D}} \tag{7.15}$$

The expression in Eq. (7.13) is the one most directly comparable to that of the BJT (Eq. 7.9). Here, however, we note the following:

1. The quantity in the denominator is $V_{OV}/2$, which is a design parameter. Although the value of V_{OV} that designers use for modern submicron technologies has been steadily decreasing, it is still about 0.15 V to 0.3 V. Thus $V_{OV}/2$ is 0.075 V to 0.15 V, which is 3 to 6 times higher than V_T. Furthermore, there are reasons for selecting higher values for V_{OV} (to be discussed in later chapters).
2. The numerator quantity is both process dependent (through V_A') and device dependent (through L), and its value has been steadily decreasing with the scaling down of the technology (see Appendix 7.A).
3. From Eq. (7.14) we see that for a given technology (i.e., a given value of V_A') the intrinsic gain A_0 can be increased by using a longer MOSFET and operating it at a lower V_{OV}. As usual, however, there are design trade-offs. For instance, we will see in Chapter 9 that increasing L and lowering V_{OV} result, independently, in decreasing the amplifier bandwidth.

As a result, the intrinsic gain realized in a MOSFET fabricated in a modern short-channel technology is only 20 V/V to 40 V/V, an order of magnitude lower than that for a BJT.

The alternative expression for the MOSFET A_0 given in Eq. (7.15) reveals a very interesting fact: For a given process technology (V_A' and $\mu_n C_{ox}$) and a given device (W and L), the intrinsic gain is inversely proportional to $\sqrt{I_D}$. This is illustrated in Fig. 7.2, which shows a typical plot for A_0 versus the bias current I_D. The plot confirms that the gain increases as the bias current is lowered. The gain, however, levels off at very low currents. This is because the MOSFET enters the **subthreshold region** of operation (Section 5.1.9), where it becomes very much like a BJT with an exponential current–voltage characteristic. The intrinsic gain then becomes constant, just like that of a BJT. Note, however, that although higher gain is obtained at lower values of I_D, the price paid is a lower g_m (Eq. 7.11), and less ability to drive capacitive loads and thus a decrease in bandwidth. This point will be studied in Chapter 9.

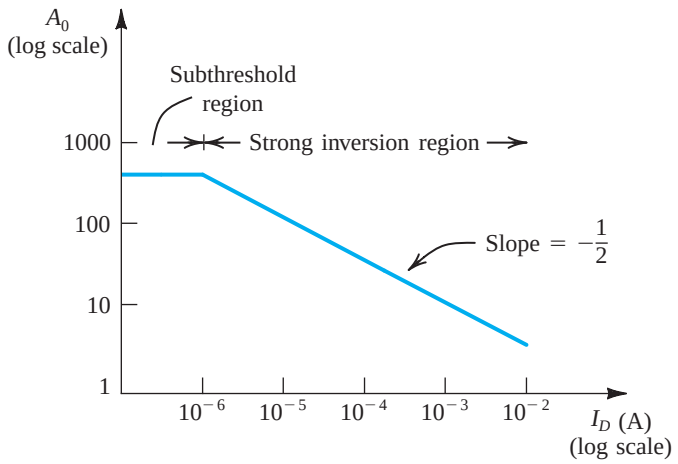


Figure 7.2 The intrinsic gain of the MOSFET versus bias current I_D. Outside the subthreshold region, this is a plot of $A_0 = V_A'\sqrt{2\mu_n C_{ox} WL/I_D}$ for the case: $\mu_n C_{ox} = 20\ \mu A/V^2$, $V_A' = 20\ V/\mu m$, $L = 2\ \mu m$, and $W = 20\ \mu m$.

Example 7.1

We wish to compare the values of g_m, R_{in}, R_o, and A_0 for a CS amplifier that is designed using an NMOS transistor with $L = 0.4\ \mu m$ and $W = 4\ \mu m$ and fabricated in a 0.25-μm technology specified to have $\mu_n C_{ox} = 267\ \mu A/V^2$ and $V_A' = 10\ V/\mu m$, with those for a CE amplifier designed using a BJT fabricated in a process with $\beta = 100$ and $V_A = 10\ V$. Assume that both devices are operating at a drain (collector) current of 100 μA.

Solution

For simplicity, we shall neglect the Early effect in the MOSFET in determining V_{OV}; thus,

$$I_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}^2$$

$$100 = \frac{1}{2} \times 267 \times \left(\frac{4}{0.4}\right)V_{OV}^2$$

resulting in

$$V_{OV} = 0.27\ V$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 0.1}{0.27} = 0.74\ mA/V$$

$$R_{in} = \infty$$

$$r_o = \frac{V_A' L}{I_D} = \frac{10 \times 0.4}{0.1} = 40\ k\Omega$$

$$R_o = r_o = 40\ k\Omega$$

$$A_0 = g_m r_o = 0.74 \times 40 = 29.6\ V/V$$

For the CE amplifier we have

$$g_m = \frac{I_C}{V_T} = \frac{0.1\text{ mA}}{0.025\text{ V}} = 4\text{ mA/V}$$

$$R_{in} = r_\pi = \frac{\beta}{g_m} = \frac{100}{4} = 25\text{ k}\Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{10}{0.1} = 100\text{ k}\Omega$$

$$R_o = r_o = 100\text{ k}\Omega$$

$$A_0 = g_m r_o = 4 \times 100 = 400\text{ V/V}$$

EXERCISE

7.1 A CS amplifier utilizes an NMOS transistor with $L = 0.36\ \mu m$ and $W/L = 10$; it was fabricated in a 0.18-μm CMOS process for which $\mu_n C_{ox} = 387\ \mu A/V^2$ and $V_A' = 5\ V/\mu m$. Find the values of g_m and A_0 obtained at $I_D = 10\ \mu A$, 100 μA, and 1 mA.
Ans. 0.28 mA/V, 50 V/V; 0.88 mA/V, 15.8 V/V; 2.78 mA/V, 5 V/V

7.2.3 Effect of the Output Resistance of the Current-Source Load

The current-source load of the CS amplifier in Fig. 7.1(a) can be implemented using a PMOS transistor biased in the saturation region to provide the required current I, as shown in Fig. 7.3(a). We can use the large-signal MOSFET model (Section 5.2, Fig. 5.15) to model Q_2 as shown in Fig. 7.3(b), where

$$I = \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)_2 [V_{DD} - V_G - |V_{tp}|]^2 \tag{7.16}$$

and

$$r_{o2} = \frac{|V_{A2}|}{I} \tag{7.17}$$

Thus the current-source load no longer has an infinite resistance; rather, it has a finite output resistance r_{o2}. This resistance will in effect appear in parallel with r_{o1}, as shown in the amplifier equivalent-circuit model in Fig. 7.3(c), from which we obtain

$$A_v \equiv \frac{v_o}{v_i} = -g_{m1}(r_{o1} \| r_{o2}) \tag{7.18}$$

Thus, not surprisingly, the finite output resistance of the current-source load reduces the magnitude of the voltage gain from $(g_{m1}r_{o1})$ to $g_{m1}(r_{o1} \| r_{o2})$. This reduction can be substantial. For instance, if Q_2 has an Early voltage equal to that of Q_1, $r_{o2} = r_{o1}$ and the gain is reduced by half,

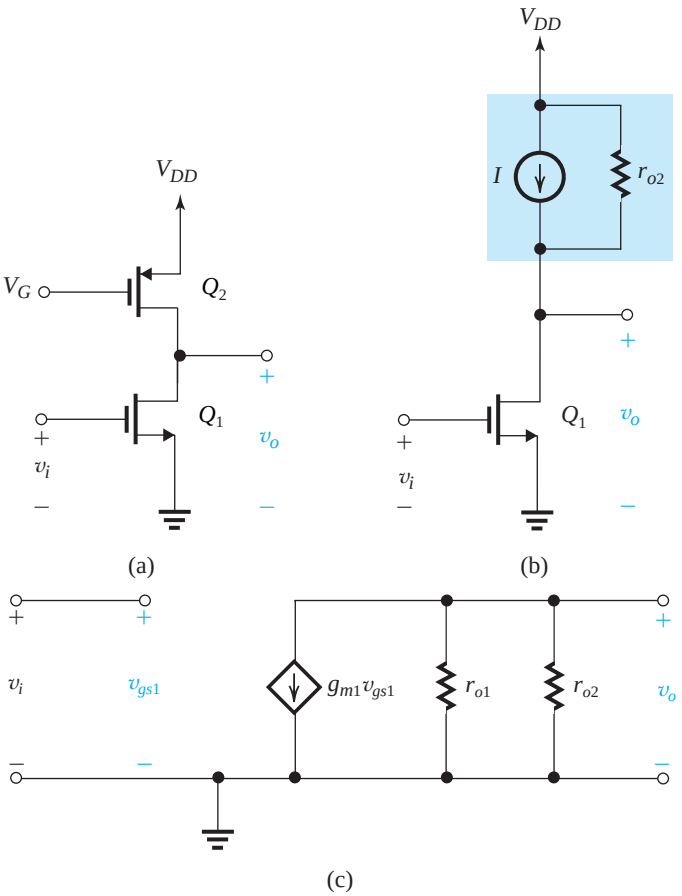


Figure 7.3 **(a)** The CS amplifier with the current-source load implemented with a *p*-channel MOSFET Q_2; **(b)** the circuit with Q_2 replaced with its large-signal model; and **(c)** small-signal equivalent circuit of the amplifier.

$$A_v = -\frac{1}{2} g_m r_o \tag{7.18′}$$

Finally, we note that a similar development can be used for the bipolar case.

Example 7.2

A practical circuit implementation of the common-source amplifier is shown in Fig. 7.4(a). Here the current-source transistor Q_2 is the output transistor of a current mirror formed by Q_2 and Q_3 and fed with a reference current I_{REF}. Current mirrors were briefly introduced in Section 5.7.4 and will be studied more extensively in Sections 7.4 and 7.5. For the time being, assume that Q_2 and Q_3 are matched. Also assume that I_{REF} is a stable, well-predicted current that is generated with a special circuit on the chip. To be able to clearly see the region of v_I over which the circuit operates as an almost-linear amplifier, determine the voltage transfer characteristic (VTC), that is, v_O versus v_I.

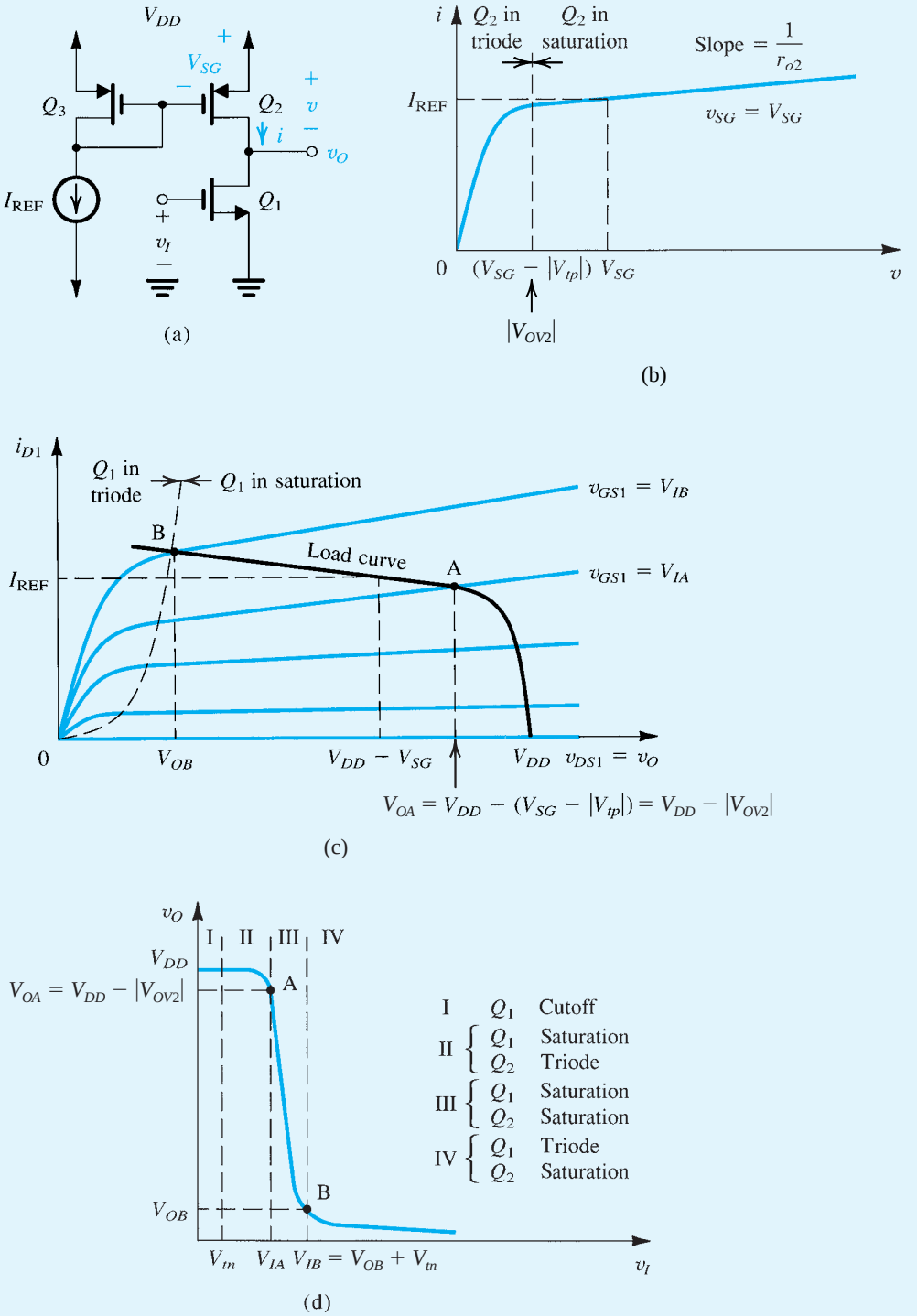


Figure 7.4 Practical implementation of the common-source amplifier: **(a)** circuit; **(b)** i–v characteristic of the active-load Q_2; **(c)** graphical construction to determine the transfer characteristic; **(d)** transfer characteristic.

Example 7.2 *continued*

Solution

First we concern ourselves with the current mirror, with the objective of determining the $i-v$ characteristic of the current source Q_2. Toward that end, we note that the current I_{REF} flows through the diode-connected transistor Q_3 and thus determines V_{SG} of Q_3, which is in turn applied between the source and the gate of Q_2. Thus, the $i-v$ characteristic of the current source Q_2 will be the i_D-v_{SD} characteristic curve of Q_2 obtained for $v_{SG} = V_{SG}$. This is shown in Fig. 7.4(b), where we note that i will be equal to I_{REF} at one point only, namely, at $v_{SD2} = V_{SG}$, this being the only point at which the two matched transistors Q_2 and Q_3 have identical operating conditions. We also observe the effect of channel-length modulation in Q_2 (the Early effect), which is modeled by the finite output resistance r_{o2}. Finally, note that Q_2 operates as a current source when v is equal to or greater than $|V_{OV2}| = V_{SG} - |V_{tp}|$. This in turn is obtained when $v_O \leq V_{DD} - |V_{OV2}|$. This is the maximum permitted value of the output voltage v_O.

Now, with the $i-v$ characteristic of the current-source load Q_2 in hand, we can proceed to determine v_O versus v_I. Figure 7.4(c) shows a graphical construction for doing this. It is based on the graphical analysis method employed in Section 5.4.5 except that here the load line is not a straight line but is the $i-v$ characteristic curve of Q_2 shifted along the v_O axis by V_{DD} volts and "flipped around." The reason for this is that

$$v_O = V_{DD} - v$$

The term V_{DD} necessitates the shift, and the minus sign of v gives rise to the "flipping around" of the load curve.

The graphical construction of Fig. 7.4(c) can be used to determine v_O for every value of v_I, point by point: The value of v_I determines the particular characteristic curve of Q_1 on which the operating point lies. The operating point will be at the intersection of this particular graph and the load curve. The horizontal coordinate of the operating point then gives the value of v_O.

Proceeding in the manner just explained, we obtain the VTC shown in Fig. 7.4(d). As indicated, it has four distinct segments, labeled I, II, III, and IV. Each segment is obtained for one of the four combinations of the modes of operation of Q_1 and Q_2, which are also indicated in the diagram. Note that we have labeled two important break points on the transfer characteristic (A and B) in correspondence with the intersection points (A and B) in Fig. 7.4(c). We urge the reader to carefully study the transfer characteristic and its various details.

Not surprisingly, segment III is the one of interest for amplifier operation. Observe that in region III the transfer curve is almost linear and is very steep, indicating large voltage gain. In region III both the amplifying transistor Q_1 and the load transistor Q_2 are operating in saturation. The end points of region III are A and B: At A, defined by $v_O = V_{DD} - |V_{OV2}|$, Q_2 enters the triode region, and at B, defined by $v_O = v_I - V_{tn}$, Q_1 enters the triode region. When the amplifier is biased at a point in region III, the small-signal voltage gain can be determined as we have done in Fig. 7.3(c). The question remains as to how we are going to guarantee that the dc component of v_I will have such a value that will result in operation in region III. That is why overall negative feedback is needed, as will be demonstrated later.

Before leaving this example it is useful to reiterate that the upper limit of the amplifier region (i.e., point A) is defined by $V_{OA} = V_{DD} - |V_{OV2}|$ and the lower limit (i.e., point B) is defined by $V_{OB} = V_{OV1}$, where V_{OV1} can be approximately determined by assuming that $I_{D1} \simeq I_{\text{REF}}$. A more precise value for V_{OB} can be obtained by taking into account the Early effect in both Q_1 and Q_2, as will be demonstrated in the next example.

Example 7.3

Consider the CMOS common-source amplifier in Fig. 7.4(a) for the case $V_{DD} = 3$ V, $V_{tn} = |V_{tp}| = 0.6$ V, $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$, and $\mu_p C_{ox} = 65\ \mu\text{A/V}^2$. For all transistors, $L = 0.4\ \mu$m and $W = 4\ \mu$m. Also, $V_{An} = 20$ V, $|V_{Ap}| = 10$ V, and $I_{\text{REF}} = 100\ \mu$A. Find the small-signal voltage gain. Also, find the coordinates of the extremities of the amplifier region of the transfer characteristic—that is, points A and B.

Solution

$$g_{m1} = \sqrt{2k_n'\left(\frac{W}{L}\right)_1 I_{\text{REF}}}$$

$$= \sqrt{2 \times 200 \times \frac{4}{0.4} \times 100} = 0.63\ \text{mA/V}$$

$$r_{o1} = \frac{V_{An}}{I_{D1}} = \frac{20\ \text{V}}{0.1\ \text{mA}} = 200\ \text{k}\Omega$$

$$r_{o2} = \frac{|V_{Ap}|}{I_{D2}} = \frac{10\ \text{V}}{0.1\ \text{mA}} = 100\ \text{k}\Omega$$

Thus,

$$A_v = -g_{m1}(r_{o1} \parallel r_{o2})$$

$$= -0.63(\text{mA/V}) \times (200 \parallel 100)(\text{k}\Omega) = -42\ \text{V/V}$$

Approximate values for the extremities of the amplifier region of the transfer characteristic (region III) can be determined as follows: Neglecting the Early effect, all three transistors are carrying equal currents I_{REF}, and thus we can determine the overdrive voltages at which they are operating. Transistors Q_2 and Q_3 will have equal overdrive voltages, $|V_{OV3}|$, determined from

$$I_{D3} = I_{\text{REF}} \simeq \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)_3 |V_{OV3}|^2$$

Substituting, $I_{\text{REF}} = 100\ \mu$A, $\mu_p C_{ox} = 65\ \mu\text{A/V}^2$, $(W/L)_3 = 4/0.4 = 10$ results in

$$|V_{OV3}| = 0.55\ \text{V}$$

Thus,

$$V_{OA} = V_{DD} - |V_{OV3}| = 2.45\ \text{V}$$

Next we determine $|V_{OV1}|$ from

$$I_{D1} \simeq I_{\text{REF}} \simeq \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)_1 V_{OV1}^2$$

Substituting, $I_{\text{REF}} = 100\ \mu$A, $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$, $(W/L)_1 = 4/0.4 = 10$ results in

$$V_{OV1} = 0.32\ \text{V}$$

Thus, $V_{OB} = V_{OV1} = 0.32$ V.

More precise values for V_{OA} and V_{OB} can be determined by taking the Early effect in all transistors into account as follows.

Example 7.3 *continued*

First, we determine V_{SG} of Q_2 and Q_3 corresponding to $I_{D3} = I_{REF} = 100\ \mu A$ using

$$I_{D3} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_3(V_{SG} - |V_{tp}|)^2\left(1 + \frac{V_{SD}}{|V_{Ap}|}\right)$$

Thus,

$$100 = \frac{1}{2} \times 65\left(\frac{4}{0.4}\right)|V_{OV3}|^2\left(1 + \frac{0.6 + |V_{OV3}|}{10}\right) \tag{7.19}$$

where $|V_{OV3}|$ is the magnitude of the overdrive voltage at which Q_3 and Q_2 are operating, and we have used the fact that, for Q_3, $V_{SD} = V_{SG}$. Equation (7.19) can be manipulated to the form

$$0.29 = |V_{OV3}|^2(1 + 0.09|V_{OV3}|)$$

which by a trial-and-error process yields

$$|V_{OV3}| = 0.53\ V$$

Thus,

$$V_{SG} = 0.6 + 0.53 = 1.13\ V$$

and

$$V_{OA} = V_{DD} - V_{OV3} = 2.47\ V$$

To find the corresponding value of v_I, V_{IA}, we derive an expression for v_O versus v_I in region III. Noting that in region III, Q_1 and Q_2 are in saturation and obviously conduct equal currents, we can write

$$i_{D1} = i_{D2}$$

$$\frac{1}{2}k_n'\left(\frac{W}{L}\right)_1(v_I - V_{tn})^2\left(1 + \frac{v_O}{|V_{An}|}\right) = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_2(V_{SG} - |V_{tp}|)^2\left(1 + \frac{V_{DD} - v_O}{|V_{Ap}|}\right)$$

Substituting numerical values, we obtain

$$8.55(v_I - 0.6)^2 = \frac{1 - 0.08v_O}{1 + 0.05v_O} \simeq (1 - 0.13v_O)$$

which can be manipulated to the form

$$v_O = 7.69 - 65.77(v_I - 0.6)^2 \tag{7.20}$$

This is the equation of segment III of the transfer characteristic. Although it includes v_I^2, the reader should not be alarmed: Because region III is very narrow, v_I changes very little, and the characteristic is nearly linear. Substituting $v_O = 2.47\ V$ gives the corresponding value of v_I; that is, $V_{IA} = 0.88\ V$. To determine the coordinates of B, we note that they are related by $V_{OB} = V_{IB} - V_{tn}$. Substituting in Eq. (7.20) and solving gives $V_{IB} = 0.93\ V$ and $V_{OB} = 0.33\ V$. The width of the amplifier region is therefore

$$\Delta v_I = V_{IB} - V_{IA} = 0.05\ V$$

and the corresponding output range is

$$\Delta v_O = V_{OB} - V_{OA} = -2.14\ V$$

Thus, the "large-signal" voltage gain is

$$\frac{\Delta v_O}{\Delta v_I} = -\frac{2.14}{0.05} = -42.8\ V/V$$

which is very close to the small-signal value of –42, indicating that segment III of the transfer characteristic is quite linear.

EXERCISES

7.2 A CMOS common-source amplifier such as that in Fig. 7.4(a), fabricated in a 0.18-μm technology, has $W/L = 7.2\ \mu m/0.36\ \mu m$ for all transistors, $k_n' = 387\ \mu A/V^2$, $k_p' = 86\ \mu A/V^2$, $I_{REF} = 100\ \mu A$, $V_{An}' = 5\ V/\mu m$, and $|V_{Ap}'| = 6\ V/\mu m$. Find g_{m1}, r_{o1}, r_{o2}, and the voltage gain.
Ans. 1.25 mA/V; 18 kΩ; 21.6 kΩ; −12.3 V/V

7.3 Consider the active-loaded CE amplifier when the constant-current source I is implemented with a *pnp* transistor. Let $I = 0.1$ mA, $|V_A| = 50$ V (for both the *npn* and the *pnp* transistors), and $\beta = 100$. Find R_{in}, r_o (for each transistor), g_m, A_0, and the amplifier voltage gain.
Ans. 25 kΩ; 0.5 MΩ; 4 mA/V; 2000 V/V; −1000 V/V

7.2.4 Increasing the Gain of the Basic Cell

We conclude this section by considering a question: How can we increase the voltage gain obtained from the basic gain cell? The answer lies in finding a way to raise the level of the output resistance of both the amplifying transistor and the load transistor. That is, we seek a circuit that passes the current $g_m v_i$ provided by the amplifying transistor right through, but increases the resistance from r_o to a much larger value. This requirement is illustrated in Fig. 7.5. Figure 7.5(a) shows the CS amplifying transistor Q_1 together with its output equivalent circuit. Note that for the time being we are not showing the load device. In Fig. 7.5(b) we have inserted a shaded box between the drain of Q_1 and a new output terminal labeled d_2. Here again we are not showing the load to which d_2 will be connected. Our "black box" takes in the output current of Q_1 and passes it to the output; thus at its output we have the equivalent circuit shown, consisting of the same controlled source $g_{m1} v_i$ but with the output resistance increased by a factor K.

Now, what does the black box really do? Since it passes the current but *raises* the resistance level, it is a **current buffer**. It is the dual of the voltage buffer (the source and emitter followers), which passes the *voltage* but *lowers* the resistance level.

Now searching our repertoire of transistor amplifier configurations studied in Sections 5.6 and 6.6, the only candidate for implementing this current-buffering action is the common-gate (or common-base in bipolar) amplifier. Indeed, recall that the CG and CB circuits have a unity current gain. What we have not yet investigated, however, is their resistance transformation property. We shall do this in the next section.

Two important final comments:

1. It is not sufficient to raise the output resistance of the amplifying transistor only. We also need to raise the output resistance of the current-source load. Obviously, we can use a current buffer to do this also.
2. Placing a CG (or a CB) circuit on top of the CS (or CE) amplifying transistor to implement the current-buffering action is called **cascoding**. We will explain the origin of this name shortly.

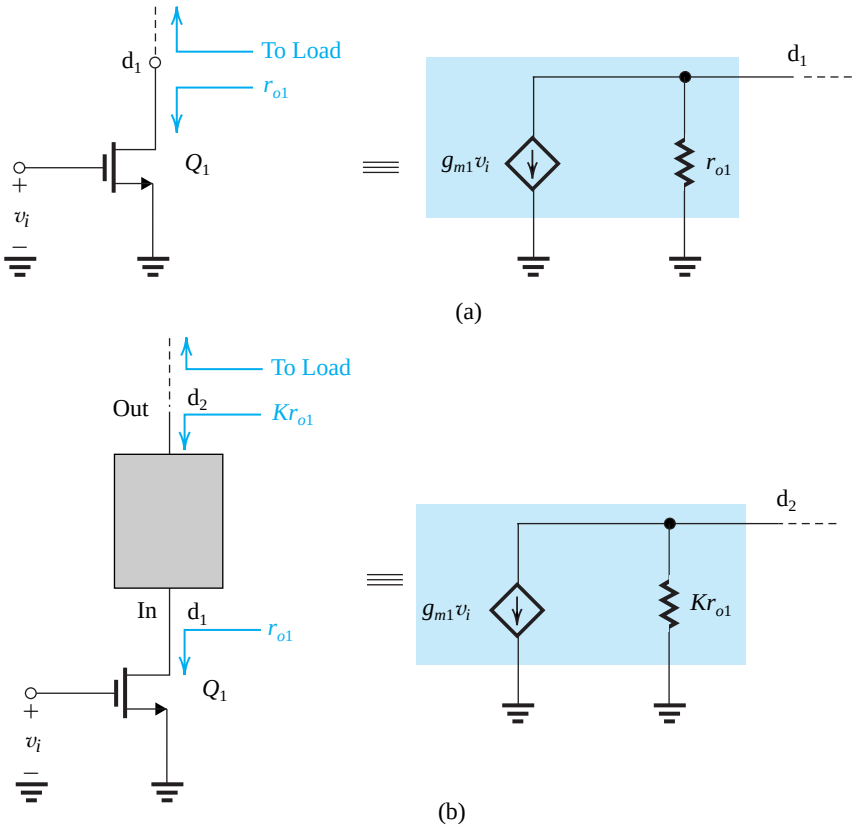


Figure 7.5 To increase the voltage gain realized in the basic gain cell shown in **(a)**, a functional block, shown as a black box in **(b)**, is connected between d_1 and the load. This new block is required to pass the current $g_{m1}v_i$ right through but raise the resistance level by a factor K. The functional block is a current buffer.

7.3 The Cascode Amplifier

7.3.1 Cascoding

Cascoding refers to the use of a transistor connected in the common-gate (or the common-base) configuration to provide **current buffering** for the output of a common-source (or a common-emitter) amplifying transistor. Figure 7.6 illustrates the technique for the MOS case. Here the CS transistor Q_1 is the amplifying transistor and Q_2, connected in the CG configuration with a dc bias voltage V_{G2} (signal ground) at its gate, is the cascode transistor.[1] A similar arrangement applies for the bipolar case and will be considered later.

We will show in the following that the equivalent circuit at the output of the cascode amplifier is that shown in Fig. 7.6. Thus, the cascode transistor passes the current $g_{m1}v_i$ to the output node while raising the resistance level by a factor K. We will derive an expression for K.

[1]The name *cascode* is a carryover from the days of vacuum tubes and is a shortened version of "*casc*aded cath*ode*"; in the tube version, the anode of the amplifying tube (corresponding to the drain of Q_1) feeds the cathode of the cascode tube (corresponding to the source of Q_2).

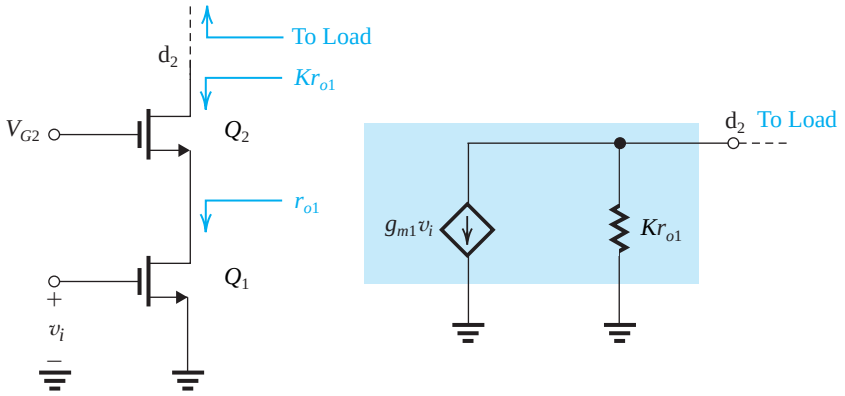


Figure 7.6 The current-buffering action of Fig. 7.5(a) is implemented using a transistor Q_2 connected in the CG configuration. Here V_{G2} is a dc bias voltage. The output equivalent circuit indicates that the CG transistor passes the current $g_{m1}v_i$ through but raises the resistance level by a factor K. Transistor Q_2 is called a cascode transistor.

7.3.2 The MOS Cascode

Figure 7.7(a) shows the MOS cascode amplifier without a load circuit and with the gate of Q_2 connected to signal ground. Thus this circuit is for the purpose of small-signal calculations only. Our objective is to determine the parameters G_m and R_o of the equivalent circuit shown in Fig. 7.7(b), which we shall use to represent the output of the cascode amplifier. Toward that end, observe that if node d_2 of the equivalent circuit is short-circuited to ground, the current flowing through the short circuit will be equal to $G_m v_i$. It follows that we can determine G_m by short-circuiting (from a signal point of view) the output of the cascode amplifier to ground, as shown in Fig. 7.7(c), determine i_o, and then

$$G_m = \frac{i_o}{v_i}$$

Now, replacing Q_1 and Q_2 in the circuit of Fig. 7.7(c) with their small-signal models results in the circuit in Fig. 7.7(d), which we shall analyze to determine i_o in terms of v_i.

Observe that the voltage at the (d_1, s_2) node is equal to $-v_{gs2}$. Writing a node equation for that node, we have

$$g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{o1}} + \frac{v_{gs2}}{r_{o2}} = g_{m1}v_i$$

Thus,

$$\left(g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right)v_{gs2} = g_{m1}v_i$$

Since $g_{m2} \gg (1/r_{o1}),\ 1/r_{o2}$,

$$g_{m2}v_{gs2} \simeq g_{m1}v_i \tag{7.21}$$

In other words, the current of the controlled source of Q_2 is equal to that of the controlled source of Q_1. Next, we write an equation for the d_2 node,

$$i_o = g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{o2}}$$

$$= \left(g_{m2} + \frac{1}{r_{o2}}\right)v_{gs2}$$

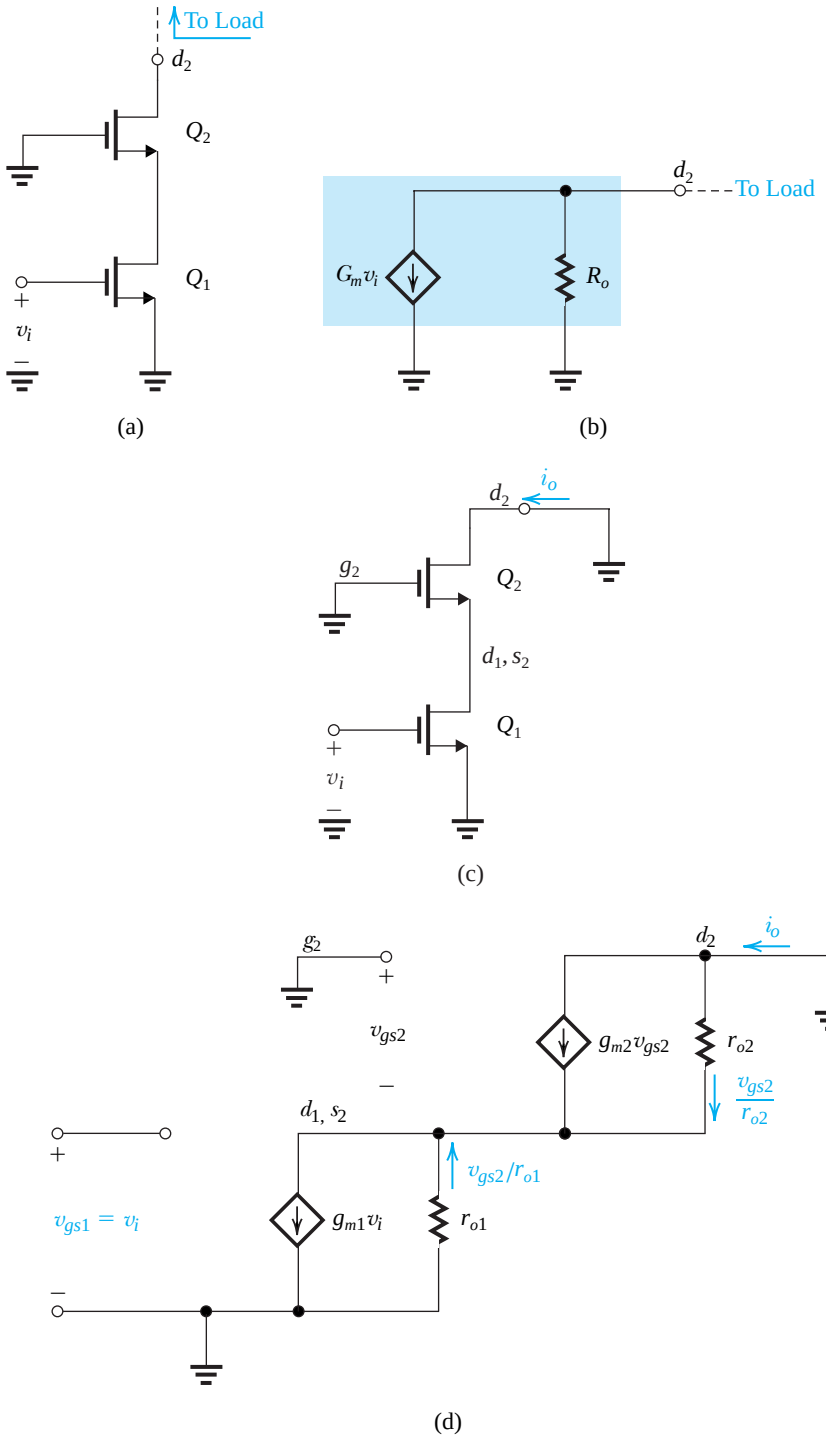


Figure 7.7 (**a**) A MOS cascode amplifier prepared for small-signal calculations; (**b**) output equivalent circuit of the amplifier in (**a**); (**c**) the cascode amplifier with the output short-circuited to determine $G_m \equiv i_o v_i$; (**d**) equivalent circuit of the situation in (**c**).

Thus,

$$i_o \simeq g_{m2} v_{gs2}$$

Using Eq. (7.21) results in

$$i_o = g_{m1} v_i$$

Thus,

$$G_m = \frac{i_o}{v_i} = g_{m1} \tag{7.22}$$

which is the result we have anticipated.

Next we need to determine R_o. For this purpose we set v_i to zero, which results in Q_1 simply reduced to its output resistance r_{o1}, which appears in the source circuit of Q_2, as shown in Fig. 7.8(a). Now, replacing Q_2 with its hybrid-π model and applying a test voltage v_x to the output node results in the equivalent circuit shown in Fig. 7.8(b). The output resistance R_o can be obtained as

$$R_o \equiv \frac{v_x}{i_x}$$

Analysis of the circuit is greatly simplified by noting that the current exiting the source node of Q_2 is equal to i_x. Thus, the voltage at the source node, which is $-v_{gs2}$, can be expressed in terms of i_x as

$$-v_{gs2} = i_x r_{o1} \tag{7.23}$$

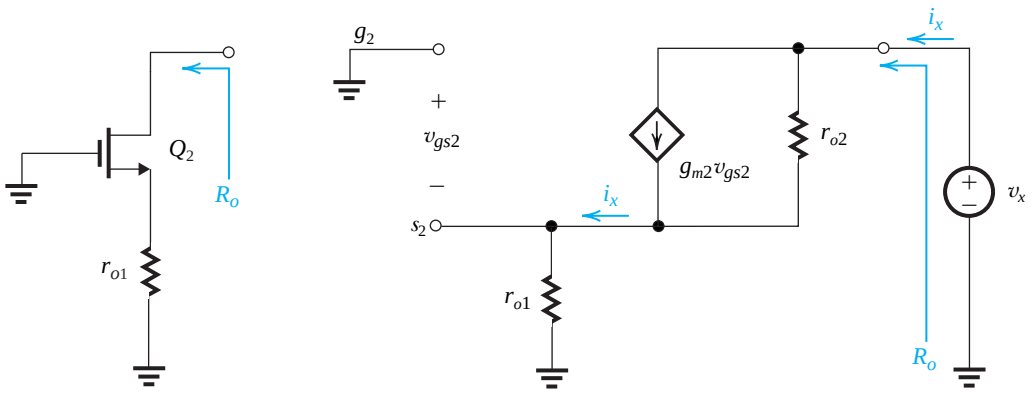
Next we express v_x as the sum of the voltages across r_{o2} and r_{o1} as

$$v_x = (i_x - g_{m2} v_{gs2})\, r_{o2} + i_x r_{o1}$$

Substituting for v_{gs2} from Eq. (7.23) results in

$$v_x = i_x(r_{o1} + r_{o2} + g_{m2} r_{o2} r_{o1})$$

Thus, $R_o \equiv v_x / i_x$ is given by



(a) (b)

Figure 7.8 Determining the output resistance of the MOS cascode amplifier.

$$R_o = r_{o1} + r_{o2} + g_{m2} r_{o2} r_{o1} \tag{7.24}$$

In this expression the last term will dominate, thus

$$R_o \simeq (g_{m2} r_{o2}) r_{o1} \tag{7.25}$$

This expression has a simple and elegant interpretation: The CG transistor Q_2 raises the output resistance of the amplifier by the factor $(g_{m2} r_{o2})$, which is its intrinsic gain. At the same time, the CG transistor simply passes the current $(g_{m1} v_i)$ to the output node. Thus the CG or cascode transistor very effectively realizes the objectives we set for the current buffer (refer to Figs. 7.5 and 7.6) with $K = A_{02} = g_{m2} r_{o2}$.

Voltage Gain If the cascode amplifier is loaded with an ideal constant-current source as shown in Fig. 7.9(a), the voltage gain realized can be found from the equivalent circuit in Fig. 7.9(b) as

$$A_{vo} = \frac{v_o}{v_i} = -g_{m1} R_o$$

Thus,

$$A_{vo} = -(g_{m1} r_{o1})\,(g_{m2} r_{o2}) \tag{7.26}$$

For the case $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$,

$$\begin{aligned} A_{vo} &= -(g_m r_o)^2 \\ &= -A_0^2 \end{aligned} \tag{7.27}$$

Thus cascoding results in increasing the gain magnitude from A_0 to A_0^2.

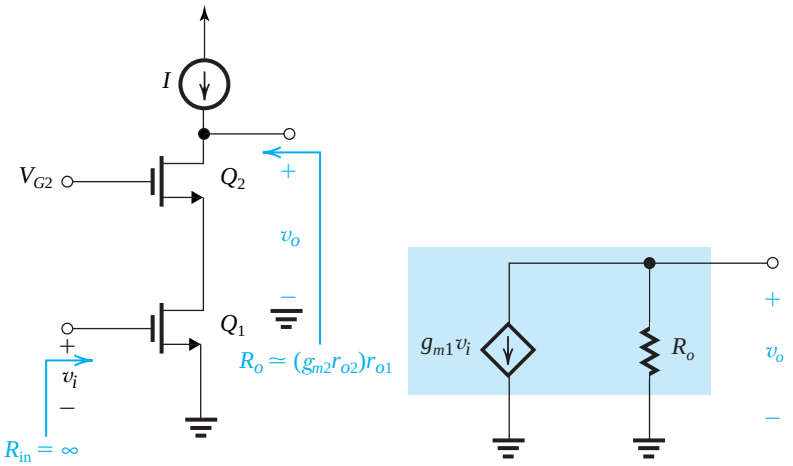


Figure 7.9 **(a)** A MOS cascode amplifier with an ideal current-source load; **(b)** equivalent circuit representation of the cascode output.

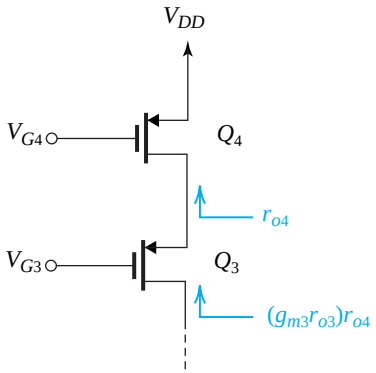


Figure 7.10 Employing a cascode transistor Q_3 to raise the output resistance of the current source Q_4.

Cascoding can also be employed to raise the output resistance of the current-source load as shown in Fig. 7.10. Here Q_4 is the current-source transistor, and Q_3 is the CG cascode transistor. Voltages V_{G3} and V_{G4} are dc bias voltages. The cascode transistor Q_3 multiplies the output resistance of Q_4, r_{o4} by $(g_{m3}r_{o3})$ to provide an output resistance for the cascode current source of

$$R_o = (g_{m3}r_{o3})r_{o4} \tag{7.28}$$

Combining a cascode amplifier with a cascode current source results in the circuit of Fig. 7.11(a). The equivalent circuit at the output side is shown in Fig. 7.11(b), from which the

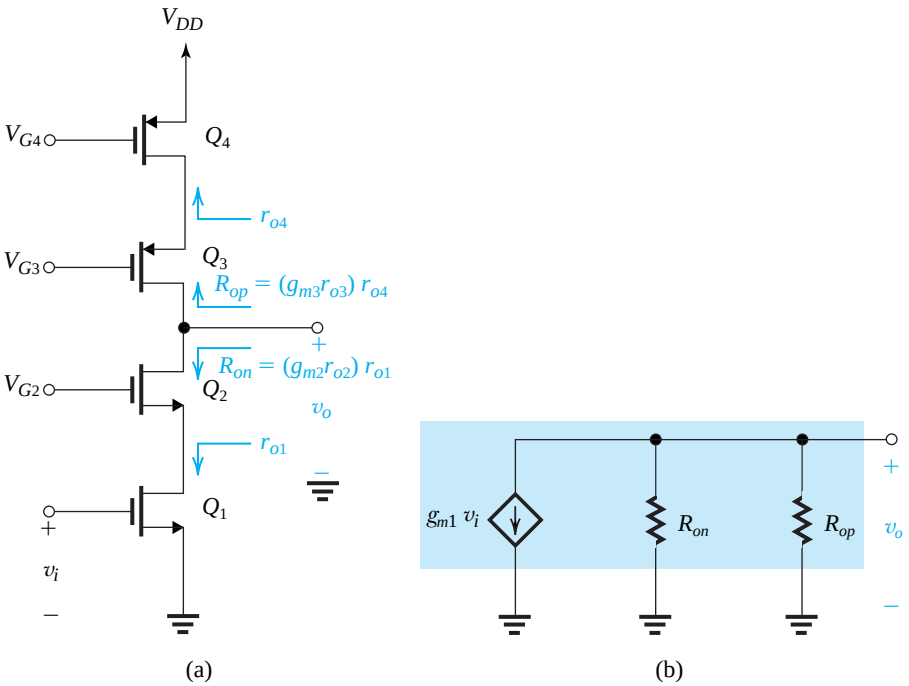


Figure 7.11 A cascode amplifier with a cascode current-source load.

voltage gain can be easily found as

$$A_v = \frac{v_o}{v_i} = -g_{m1}[R_{on} \| R_{op}]$$

Thus,

$$A_v = -g_{m1}\{[(g_{m2}r_{o2})r_{o1}] \| [(g_{m3}r_{o3})r_{o4}]\} \tag{7.29}$$

For the case in which all transistors are identical,

$$A_v = -\frac{1}{2}(g_m r_o)^2 = -\frac{1}{2}A_0^2 \tag{7.30}$$

By comparison to the gain expression in Eq. (7.18′), we see that using the cascode configuration for both the amplifying transistor and the current-source load transistor results in an increase in the magnitude of gain by a factor equal to A_0.

Example 7.4

It is required to design the cascode current-source of Fig. 7.10 to provide a current of 100 μA and an output resistance of 500 kΩ. Assume the availability of a 0.18-μm CMOS technology for which $V_{DD} = 1.8$ V, $V_{tp} = -0.5$ V, $\mu_p C_{ox} = 90$ μA/V^2 and $V_A' = -5$ V/μm. Use $|V_{OV}| = 0.3$ V and determine L and W/L for each transistor, and the values of the bias voltages V_{G3} and V_{G4}.

Solution

The output resistance R_o is given by

$$R_o = (g_{m3}r_{o3})r_{o4}$$

Assuming Q_3 and Q_4 are identical,

$$R_o = (g_m r_o)r_o = \frac{|V_A|}{|V_{OV}|/2} \times \frac{|V_A|}{I_D}$$

Using $|V_{OV}| = 0.3$ V, we write

$$500\ \text{k}\Omega = \frac{|V_A|}{0.15} \times \frac{|V_A|}{0.1\ \text{mA}}$$

Thus we require

$$|V_A| = 2.74\ \text{V}$$

Now, since $|V_A| = |V_A'|L$ we need to use a channel length of

$$L = \frac{2.74}{5} = 0.55\ \mu\text{m}$$

which is about three times the minimum channel length. With $|V_t| = 0.5$ V and $|V_{OV}| = 0.3$ V,

$$V_{SG4} = 0.5 + 0.3 = 0.8\ \text{V}$$

and thus,

$$V_{G4} = 1.8 - 0.8 = 1.0 \text{ V}$$

To allow for the largest possible signal swing at the output terminal, we shall use the minimum required voltage across Q_4, namely, $|V_{OV}|$ or 0.3 V. Thus,

$$V_{D4} = 1.8 - 0.3 = 1.5 \text{ V}$$

Since the two transistors are identical and are carrying equal currents,

$$V_{SG3} = V_{SG4} = 0.8 \text{ V}$$

Thus,

$$V_{G3} = 1.5 - 0.8 = +0.7 \text{ V}$$

We note that the maximum voltage allowed at the output terminal of the current source will be constrained by the need to allow a minimum voltage of $|V_{OV}|$ across Q_3; thus,

$$v_{D3\max} = 1.5 - 0.3 = +1.2 \text{ V}$$

To determine the required W/L ratios of Q_3 and Q_4, we use

$$I_D = \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)|V_{OV}|^2\left(1 + \frac{V_{SD}}{|V_A|}\right)$$

$$100 = \frac{1}{2} \times 90 \times \left(\frac{W}{L}\right) \times 0.3^2\left(1 + \frac{0.3}{2.74}\right)$$

which yields

$$\frac{W}{L} = 22.3$$

EXERCISES

D7.4 If in Example 7.4, L of each of Q_3 and Q_4 is halved while W/L is changed to allow I_D and V_{OV} to remain unchanged, find the new values of R_o and W/L. [*Hint*: In computing the required (W/L), note that $|V_A|$ has changed.]
Ans. 125 kΩ; 20.3

7.5 Consider the cascode amplifier of Fig. 7.11 with the dc component at the input, $V_I = 0.7$ V, $V_{G2} = 1.0$ V, $V_{G3} = 0.8$ V, $V_{G4} = 1.1$ V, and $V_{DD} = 1.8$ V. If all devices are matched (i.e., if $k_{n1} = k_{n2} = k_{p3} = k_{p4}$), and have equal $|V_t|$ of 0.5 V, what is the overdrive voltage at which the four transistors are operating? What is the allowable voltage range at the output?
Ans. 0.2 V; 0.5 V to 1.3 V

7.6 The cascode amplifier in Fig. 7.11 is operated at a current of 0.2 mA with all devices operating at $|V_{OV}| = 0.2$ V. All devices have $|V_A| = 2$ V. Find g_{m1}, the output resistance of the amplifier, R_{on}, and the output resistance of the current source, R_{op}. Also find the overall output resistance and the voltage gain realized.
Ans. 2 mA/V; 200 kΩ, 200 kΩ; 100 kΩ; –200 V/V

7.3.3 Distribution of Voltage Gain in a Cascode Amplifier

It is often useful to know how much of the overall voltage gain of a cascode amplifier is realized in each of its two stages: the CS stage Q_1, and the CG stage Q_2. For this purpose, consider the cascode amplifier shown in Fig. 7.12(a). Here, for generality we have included a load resistance R_L, which represents the output resistance of the current-source load plus any additional resistance that may be connected to the output node. Recalling that the cascode amplifier output can be represented with the equivalent circuit of Fig. 7.7(b), where $G_m = g_{m1}$ and $R_o = (g_{m2}r_{o2})r_{o1}$, the voltage gain A_v of the amplifier in Fig. 7.12(a) can be found as

$$A_v = -g_{m1}(R_o \parallel R_L)$$

Thus,

$$A_v = -g_{m1}(g_{m2}r_{o2}r_{o1} \parallel R_L) \tag{7.31}$$

The overall gain A_v can be expressed as the product of the voltage gains of Q_1 and Q_2 as

$$A_v = A_{v1}A_{v2} = \left(\frac{v_{o1}}{v_i}\right)\left(\frac{v_o}{v_{o1}}\right) \tag{7.32}$$

To obtain $A_{v1} \equiv v_{o1}/v_i$ we need to find the total resistance between the drain of Q_1 and ground. Referring to Fig. 7.12(b) and denoting this resistance R_{d1}, we can express A_{v1} as

$$A_{v1} = \frac{v_{o1}}{v_i} = -g_{m1}R_{d1} \tag{7.33}$$

Observe that R_{d1} is the parallel equivalent of r_{o1} and R_{in2}, where R_{in2} is the input resistance of the CG transistor Q_2. We shall now derive an expression[2] for R_{in2}. For this purpose, refer to the equivalent circuit of Q_2 with its load resistance R_L, shown in Fig. 7.12(c). Observe that the voltage at the source of Q_2 is $-v_{gs2}$, thus R_{in2} can be found from

$$R_{\text{in2}} = \frac{-v_{gs2}}{i}$$

where i is the current flowing into the source of Q_2. Now this is the same current that flows out of the drain of Q_2 and into R_L. Summing the currents at the source node, we see that the current through r_{o2} is $i + g_{m2}v_{gs2}$. We can now express the voltage at the source node, $-v_{gs2}$, as the sum of the voltage drops across r_{o2} and R_L to obtain

$$-v_{gs2} = (i + g_{m2}v_{gs2})r_{o2} + iR_L$$

which can be rearranged to obtain

$$R_{\text{in2}} \equiv -v_{gs2}/i$$

$$R_{\text{in2}} = \frac{R_L + r_{o2}}{1 + g_{m2}r_{o2}} \tag{7.34}$$

This is a useful expression because it provides the input resistance of a CG amplifier loaded in a resistance R_L. Since $g_{m2}r_{o2} \gg 1$, we can simplify R_{in2} as follows:

$$R_{\text{in2}} \simeq \frac{R_L}{g_{m2}r_{o2}} + \frac{1}{g_{m2}} \tag{7.35}$$

[2]The reader should not jump to the conclusion that R_{in2} is equal to $1/g_{m2}$; this is the case when we neglect r_{o2}. As will be seen very shortly, R_{in2} can be vastly different from $1/g_{m2}$.

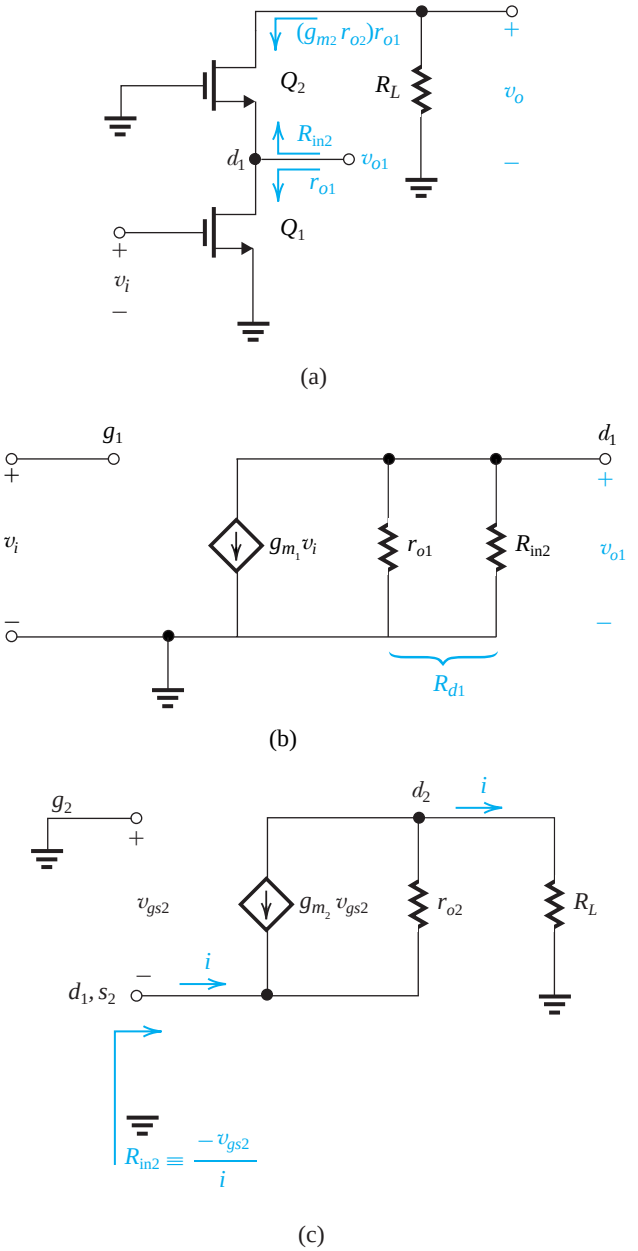


Figure 7.12 **(a)** The cascode amplifier with a load resistance R_L. Only signal quantities are shown. **(b)** Determining v_{o1}. **(c)** Determining R_{in2}.

This is a very interesting result. First, it shows that if r_{o2} is infinite, as was assumed in our analysis of the discrete CG amplifier in Section 5.6.5, then R_{in2} reduces to $1/g_{m2}$, verifying the result we found there. If r_{o2} cannot be neglected, as is always the case in IC amplifiers, we see that the input resistance depends on the value of R_L in an interesting fashion: The load resistance R_L is divided by the factor $(g_{m2}r_{o2})$. This is of course the "flip side" of the impedance transformation action of the CG. For emphasis and future reference, we illustrate the impedance transformation properties of the CG circuit in Fig. 7.13.

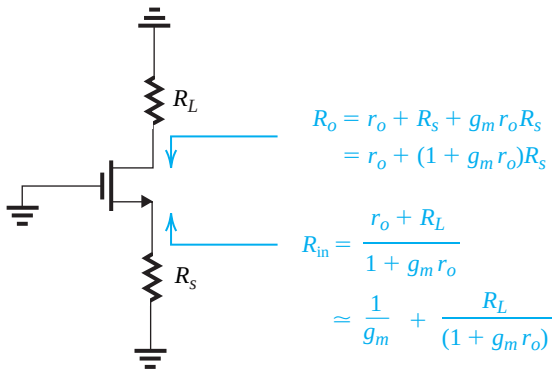


Figure 7.13 The impedance-transformation properties of the common-gate amplifier. Depending on the values of R_s and R_L, we can sometimes write $R_{in} \simeq R_L/(g_m r_o)$ and $R_o \simeq (g_m r_o)R_s$. However, such approximations are not always justified.

Going back to the cascode amplifier in Fig. 7.12(a), having found the value of R_{in2} we can now obtain R_{d1} as

$$R_{d1} = r_{o1} \parallel R_{in2} \tag{7.36}$$

and A_{v1} as

$$A_{v1} = -g_{m1}R_{d1} = -g_{m1}(r_{o1} \parallel R_{in2}) \tag{7.37}$$

Finally, we can obtain A_{v2} by dividing the total gain A_v given by Eq. (7.31) by A_{v1}. To provide insight into the effect of the value of R_L on the overall gain of the cascode as well as on how this gain is distributed among the two stages of the cascode amplifier, we provide in Table 7.1 approximate values for the case $r_{o1} = r_{o2} = r_o$ and for four different values of R_L: (1) $R_L = \infty$, obtained with an ideal current-source load; (2) $R_L = (g_m r_o)r_o$, obtained with a cascode current-source load; (3) $R_L = r_o$, obtained with a simple current-source load; and (4) for completeness, $R_L = 0$, that is, a signal short circuit at the output.

Table 7.1 Gain Distribution in the MOS Cascode Amplifier for Various Values of R_L

Case	R_L	R_{in2}	R_{d1}	A_{v1}	A_{v2}	A_v
1	∞	∞	r_o	$-g_m r_o$	$g_m r_o$	$-(g_m r_o)^2$
2	$(g_m r_o)r_o$	r_o	$r_o/2$	$-\frac{1}{2}(g_m r_o)$	$g_m r_o$	$-\frac{1}{2}(g_m r_o)^2$
3	r_o	$\frac{2}{g_m}$	$\frac{2}{g_m}$	-2	$\frac{1}{2}(g_m r_o)$	$-(g_m r_o)$
4	0	$\frac{1}{g_m}$	$\frac{1}{g_m}$	-1	0	0

Observe that while case 1 represents an idealized situation, it is useful in that it provides the theoretical maximum voltage gain achievable in a MOS cascode amplifier. Case 2, which assumes a cascode current-source load with an output resistance equal to that of the cascode amplifier, provides a realistic estimate of the gain achieved if one aims to maximize the realized gain. In certain situations, however, that is not our objective. This point is important, for as we shall see in Chapter 9, there is an entirely different application of the cascode amplifier: namely, to obtain wideband amplification by extending the upper 3-dB frequency f_H. As will be seen, for such an application one opts for the situation represented by case 3, where the gain achieved in the CS amplifier is only –2 V/V, and of course the overall gain is now only $-(g_m r_o)$. However, as will be seen in Chapter 9, this trade-off of the overall gain to obtain extended bandwidth is in some cases a good bargain!

EXERCISES

7.7 The common-gate transistor in Fig. 7.13 is biased at a drain current of 0.25 mA and is operating with an overdrive voltage $V_{OV} = 0.25$ V. The transistor has an Early voltage V_A of 5 V.
(a) Find R_{in} for $R_L = \infty$, 1 MΩ, 100 kΩ, 20 kΩ, and 0.
(b) Find R_o for $R_s = 0$, 1 kΩ, 10 kΩ, 20 kΩ, and 100 kΩ.
Ans. (a) ∞, 25.5 kΩ, 3 kΩ, 1 kΩ, 0.5 kΩ; (b) 20 kΩ, 61 kΩ, 430 kΩ, 840 kΩ, 4.12 MΩ

7.8 Consider a cascode amplifier for which the CS and CG transistors are identical and are biased to operate at $I_D = 0.1$ mA with $V_{OV} = 0.2$ V. Also let $V_A = 2$ V. Find A_{v1}, A_{v2}, and A_v for two cases: (a) $R_L = 20$ kΩ and (b) $R_L = 400$ kΩ.
Ans. (a) –1.82 V/V, 10.5 V/V, –19.0 V/V; (b) –10.2 V/V, 19.6 V/V, –200 V/V

7.3.4 The Output Resistance of a Source-Degenerated CS Amplifier

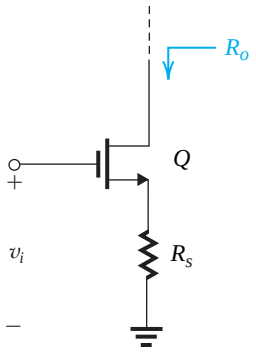
In Section 5.6.4 we discussed some of the benefits that are obtained when a resistance R_s is included in the source lead of a CS amplifier, as in Fig. 7.14(a). Such a resistance is referred to as a source-degeneration resistance because of its action in reducing the effective transconductance of the CS stage to $g_m/(1 + g_m R_s)$, that is, by a factor $(1 + g_m R_s)$. This also is the factor by which we increase a number of performance parameters such as linearity and bandwidth (as will be seen in Chapter 9). At this juncture we simply wish to point out that the expression we derived for the output resistance of the cascode amplifier applies directly to the case of a source-degenerated CS amplifier. This is because when we determine R_o, we ground the input terminal, making transistor Q appear as a CG transistor. Thus R_o is given by

$$R_o = R_s + r_o + g_m r_o R_s \tag{7.38}$$

Since $g_m r_o \gg 1$, the first term on the right-hand side will be much lower than the third and can be neglected, resulting in

$$R_o \simeq (1 + g_m R_s) r_o \tag{7.39}$$

Thus source degeneration increases the output resistance of the CS amplifier from r_o to $(1 + g_m R_s) r_o$, again by the same factor $(1 + g_m R_s)$. In Chapter 10, we will find that R_s introduces negative (degenerative) feedback of an amount $(1 + g_m R_s)$.



$$R_o = R_s + r_o + g_m r_o R_s$$
$$\simeq (1 + g_m R_s)\, r_o$$

Figure 7.14 The output resistance expression of the cascode can be used to find the output resistance of a source-degenerated common-source amplifier. Here, a useful interpretation of the result is that R_s increases the output resistance by the factor $(1 + g_m R_s)$.

EXERCISE

7.9 Given that source degeneration reduces the transconductance of a CS amplifier from g_m to approximately $g_m/(1 + g_m R_s)$ and increases its output resistance by approximately the same factor, what happens to the open-circuit voltage gain A_{vo}? Now, find an expression for A_v when a load resistance R_L is connected to the output.

Ans. A_{vo} remains constant at $g_m r_o$:

$$A_v = (g_m r_o)\frac{R_L}{R_L + (1 + g_m R_s) r_o} \tag{7.40}$$

7.3.5 Double Cascoding

If a still higher output resistance and correspondingly higher gain are required, it is possible to add another level of cascoding, as illustrated in Fig. 7.15. Observe that Q_3 is the second cascode transistor, and it raises the output resistance by $(g_{m3} r_{o3})$. For the case of identical transistors, the output resistance will be $(g_m r_o)^2 r_o$ and the voltage gain, assuming an ideal current-source load, will be $(g_m r_o)^3$ or A_0^3. Of course, we have to generate another dc bias voltage for the second cascode transistor, Q_3.

A drawback of double cascoding is that an additional transistor is now stacked between the power-supply rails. Furthermore, to realize the advantage of double cascoding, the current-source load will also need to use double cascoding with an additional transistor. Since for proper operation each transistor needs a certain minimum v_{DS} (at least equal to V_{OV}), and recalling that modern MOS technology utilizes power supplies in the range of 1 V to 2 V, we see that there is a limit on the number of transistors in a cascode stack.

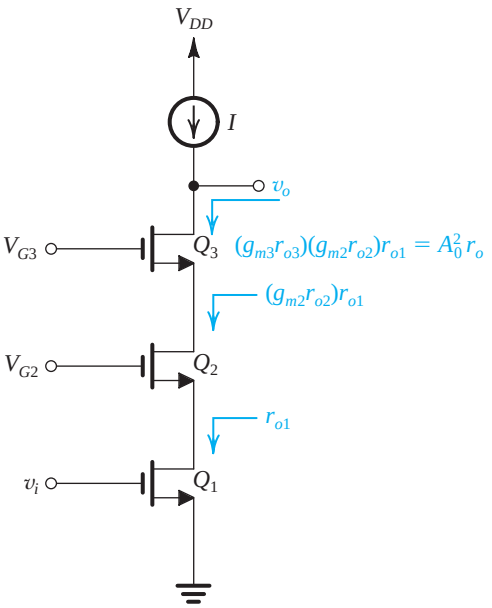


Figure 7.15 Double cascoding.

7.3.6 The Folded Cascode

To avoid the problem of stacking a large number of transistors across a low-voltage power supply, one can use a PMOS transistor for the cascode device, as shown in Fig. 7.16. Here, as before, the NMOS transistor Q_1 is operating in the CS configuration, but the CG stage is implemented using the PMOS transistor Q_2. An additional current source I_2 is needed to bias Q_2 and provide it with its active load. Note that Q_1 is now operating at a bias current of $(I_1 - I_2)$. Finally, a dc voltage V_{G2} is needed to provide an appropriate dc level for the gate of the cascode transistor Q_2. Its value has to be selected so that Q_2 and Q_1 operate in the saturation region.

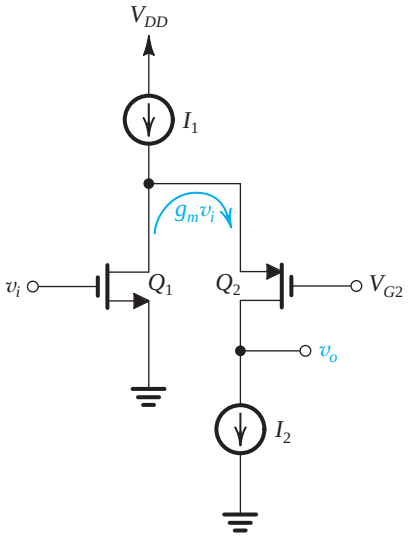


Figure 7.16 The folded cascode.

The small-signal operation of the circuit in Fig. 7.16 is similar to that of the NMOS cascode. The difference here is that the signal current $g_m v_i$ is *folded down* and made to flow into the source terminal of Q_2, which gives the circuit the name **folded cascode**.[3] The folded cascode is a very popular building block in CMOS amplifiers.

EXERCISE

7.10 Consider the folded-cascode amplifier of Fig. 7.16 for the following case: $V_{DD} = 1.8$ V, $k_p' = 1/4k_n'$, and $V_{tn} = -V_{tp} = 0.5$ V. To operate Q_1 and Q_2 at equal bias currents I, $I_1 = 2I$ and $I_2 = I$. While current source I_1 is implemented using the simple circuit studied in Section 7.2, current source I_2 is realized using a cascoded circuit (i.e., the NMOS version of the circuit in Fig. 7.10). The transistor W/L ratios are selected so that each operates at an overdrive voltage of 0.2 V.

(a) What must the relationship of $(W/L)_2$ to $(W/L)_1$ be?

(b) What is the minimum dc voltage required across current source I_1 for proper operation? Now, if a 0.1-V peak-to-peak signal swing is to be allowed at the drain of Q_1, what is the highest dc bias voltage that can be used at that node?

(c) What is the value of V_{SG} of Q_2, and hence what is the largest value to which V_{G2} can be set?

(d) What is the minimum dc voltage required across current-source I_2 for proper operation?

(e) Given the results of (c) and (d), what is the allowable range of signal swing at the output?

Ans. (a) $(W/L)_2 = 4\,(W/L)_1$; (b) 0.2 V, 1.55 V; (c) 0.7 V, 0.85 V; (d) 0.4 V; (e) 0.4 V to 1.35 V

7.3.7 The BJT Cascode

Figure 7.17(a) shows the BJT cascode amplifier with an ideal current-source load. Voltage V_{B2} is a dc bias voltage for the CB cascode transistor Q_2. The circuit is very similar to the MOS cascode, and the small-signal analysis will follow in a parallel fashion. Our objective then is to determine the parameters G_m and R_o of the equivalent circuit of Fig. 7.17(b), which we shall use to represent the output of the cascode amplifier formed by Q_1 and Q_2.

As in the case of the MOS cascode, G_m is the short-circuit transconductance and can be determined from the circuit in Fig. 7.17(c). Here we show the cascode amplifier prepared for small-signal analysis with the output short-circuited to ground. The transconductance G_m can be determined as

$$G_m = \frac{i_o}{v_i}$$

Replacing Q_1 and Q_2 with their hybrid-π equivalent-circuit models gives rise to the circuit in Fig. 7.17(d). Analysis of this circuit is straightforward and proceeds as follows: The voltage at the node (c_1, e_2) is seen to be $-v_{\pi 2}$. Thus we can write a node equation for (c_1, e_2) as

$$g_{m2} v_{\pi 2} + \frac{v_{\pi 2}}{r_{o1}} + \frac{v_{\pi 2}}{r_{o2}} + \frac{v_{\pi 2}}{r_{\pi 2}} = g_{m1} v_i$$

[3]The circuit itself can be thought of as having been folded. In this same vein, the regular cascode is sometimes referred to as a **telescopic cascode** because the stacking of transistors resembles the extension of a telescope.

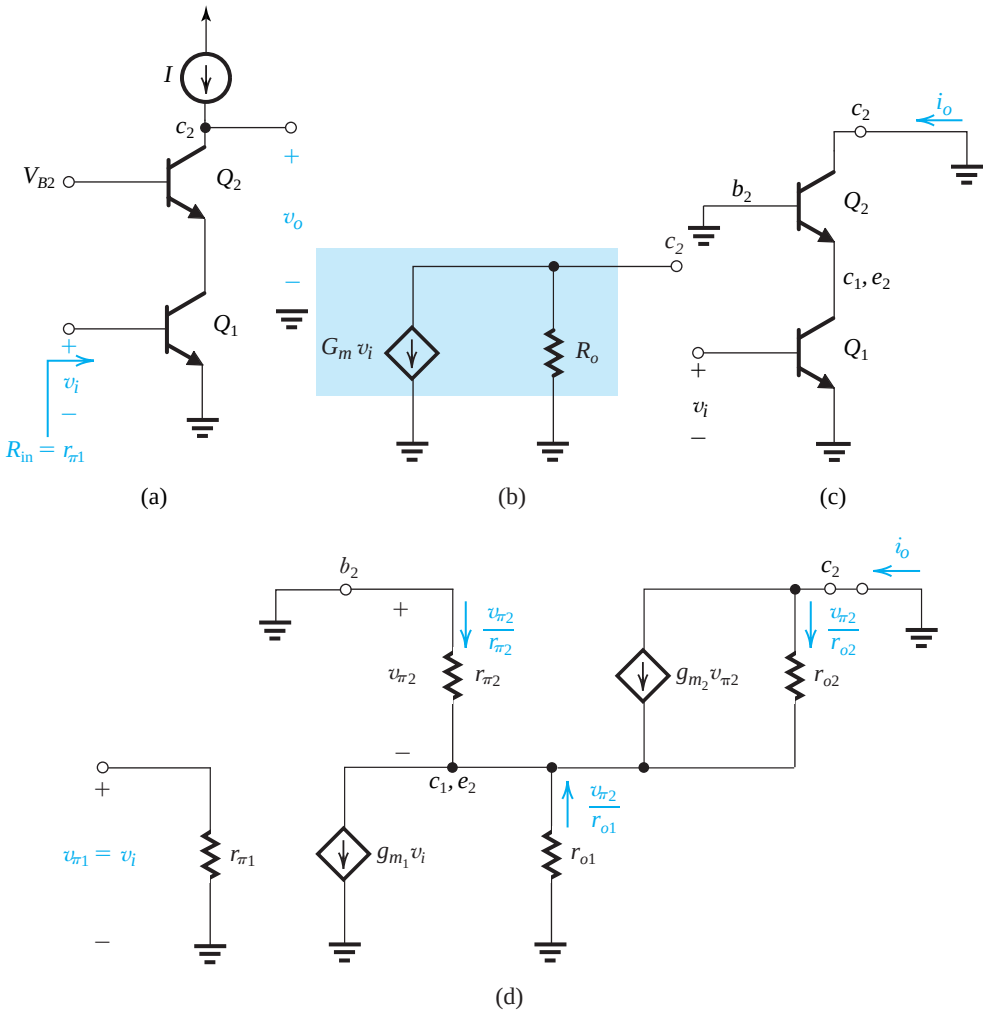


Figure 7.17 **(a)** A BJT cascode amplifier with an ideal current-source load; **(b)** small-signal equivalent-circuit representation of the output of the cascode amplifier; **(c)** the cascode amplifier with the output short-circuited to ground, and **(d)** equivalent circuit representation of **(c)**.

Since $g_{m2} \gg (1/r_{\pi 2})$, $1/r_{o1}$ and $1/r_{o2}$, we can neglect all the terms beyond the first on the left-hand side to obtain

$$g_{m2} v_{\pi 2} \simeq g_{m1} v_i \tag{7.41}$$

Next, we write a node equation at c_2,

$$i_o = g_{m2} v_{\pi 2} + \frac{v_{\pi 2}}{r_{o2}}$$

and again neglect the second term on the right-hand side to obtain

$$i_o \simeq g_{m2} v_{\pi 2}$$

Using Eq. (7.41) results in

$$i_o = g_{m1} v_i$$

Thus,

$$G_m = g_{m1}$$

which is the result we have anticipated and is identical to that for the MOS case.

To obtain R_o, we set $v_i = 0$, which results in Q_1 being reduced to its output resistance r_{o1}, which appears in the emitter lead of Q_2 as shown in Fig. 7.18(a). Here we have applied a test voltage v_x and will determine R_o as

$$R_o = \frac{v_x}{i_x}$$

Replacing Q_2 with its hybrid-π model results in the circuit of Fig. 7.18(b). Before embarking on the analysis, it is very useful to observe first that the current flowing into the emitter node must be equal to i_x. Second, note that r_{o1} and $r_{\pi 2}$ appear in parallel. Thus the voltage at the emitter node, $-v_{\pi 2}$, can be found as

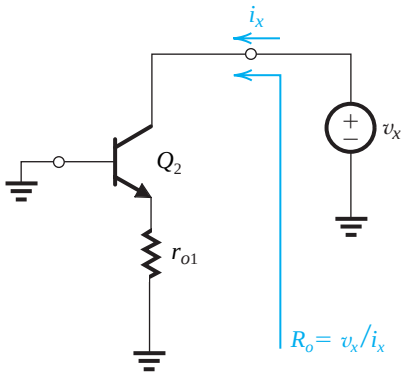
$$-v_{\pi 2} = i_x(r_{o1} \| r_{\pi 2}) \tag{7.42}$$

Next we write a loop equation around the $c_2 - e_2 -$ ground loop as

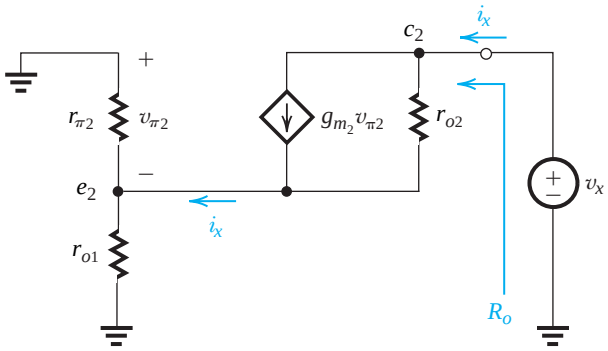
$$v_x = (i_x - g_{m2}v_{\pi 2})r_{o2} + i_x(r_{o1} \| r_{\pi 2})$$

Substituting for $v_{\pi 2}$ from Eq. (7.42) and collecting terms, we find $R_o = v_x/i_x$ as

$$R_o = r_{o2} + (r_{o1} \| r_{\pi 2}) + (g_{m2}r_{o2})(r_{o1} \| r_{\pi 2}) \tag{7.43}$$



(a)



(b)

Figure 7.18 Determining the output resistant R_o of the BJT cascode amplifier.

which can be written as

$$R_o = r_{o2} + (g_{m2}r_{o2} + 1)(r_{o1} \parallel r_{\pi 2})$$

$$\simeq r_{o2} + (g_{m2}r_{o2})(r_{o1} \parallel r_{\pi 2}) \tag{7.44}$$

Since $g_{m2}(r_{o1} \parallel r_{\pi 2}) \gg 1$, we can neglect the first term on the right-hand side of Eq. (7.44),

$$R_o \simeq (g_{m2}r_{o2})(r_{o1} \parallel r_{\pi 2}) \tag{7.45}$$

This result is similar but certainly *not identical* to that for the MOS cascode. Here, because of the finite β of the BJT, we have $r_{\pi 2}$ appearing in parallel with r_{o1}. This poses a very significant constraint on R_o of the BJT cascode. Specifically, because $(r_{o1} \parallel r_{\pi 2})$ will always be lower than $r_{\pi 2}$, it follows that the maximum possible value of R_o is

$$R_o|_{\max} = g_{m2}r_{o2}r_{\pi 2}$$

$$= (g_{m2}r_{\pi 2})r_{o2} = \beta_2 r_{o2} \tag{7.46}$$

Thus the maximum output resistance realizable by cascoding is $\beta_2 r_{o2}$. This means that unlike the MOS case, double cascoding with a BJT would not be useful.

Having determined G_m and R_o, we can now find the open-circuit voltage gain of the bipolar cascode as

$$A_{vo} = \frac{v_o}{v_i} = -G_m R_o$$

Thus,

$$A_{vo} = -g_{m1}(g_{m2}r_{o2})(r_{o1} \parallel r_{\pi 2}) \tag{7.47}$$

For the case $g_{m1} = g_{m2}$, $r_{o1} = r_{o2}$,

$$A_{vo} = -(g_m r_o)[g_m(r_o \parallel r_\pi)] \tag{7.48}$$

which will be less than $(g_m r_o)^2$ in magnitude. In fact, the maximum possible gain magnitude is obtained when $r_o \gg r_\pi$ and is given by

$$|A_{vo}|_{\max} = \beta g_m r_o = \beta A_0 \tag{7.49}$$

Finally, we note that to be able to realize gains approaching this level, the current-source load must also be cascoded. Figure 7.19 shows a cascode BJT amplifier with a cascode current-source load.

EXERCISES

7.11 Find an expression for the maximum voltage gain achieved in the amplifier of Fig. 7.19.
Ans. $|A_{v\max}| = g_{m1}(\beta_2 r_{o2} \parallel \beta_3 r_{o3})$

7.12 Consider the BJT cascode amplifier of Fig. 7.19 when biased at a current of 0.2 mA. Assuming that *npn* transistors have $\beta = 100$ and $V_A = 5$ V and that *pnp* transistors have $\beta = 50$ and $|V_A| = 4$ V, find R_{on}, R_{op}, and A_v. Also use the result of Exercise 7.11 to determine the maximum achievable gain.
Ans. 1.67 MΩ; 0.762 MΩ; –4186 V/V; –5714 V/V

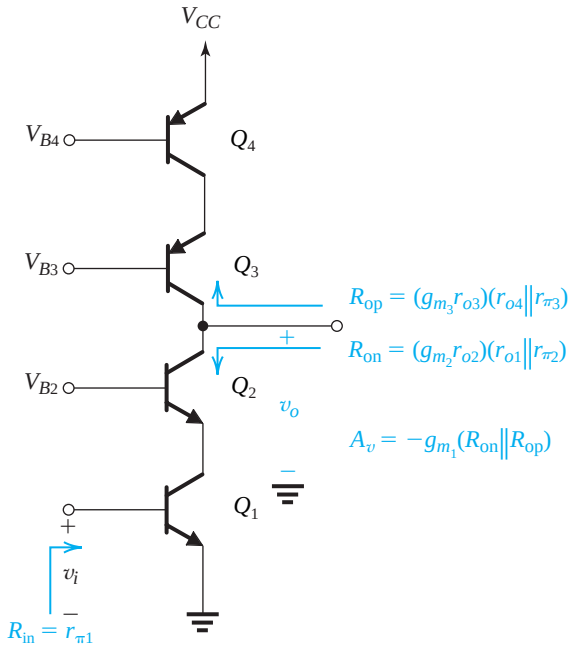


Figure 7.19 A BJT cascode amplifier with a cascode current source.

7.3.8 The Output Resistance of an Emitter-Degenerated CE Amplifier

As we have done in the MOS case, we shall adapt the expression for R_o derived for the BJT cascode (Eq. 7.43) for the case of a CE amplifier with a resistance R_e connected in its emitter, as shown in Fig. 7.20(a). The output resistance is obtained from Eq. (7.43) by replacing r_{o2} with r_o, g_{m2} by g_m, $r_{\pi 2}$ by r_π, and r_{o1} by R_e:

$$R_o = r_o + (R_e \| r_\pi) + (g_m r_o)(R_e \| r_\pi) \tag{7.50}$$

Since $g_m r_o \gg 1$, we can neglect the second term relative to the third; thus,

$$R_o \simeq r_o + g_m r_o (R_e \| r_\pi)$$

That is,

$$R_o = [1 + g_m (R_e \| r_\pi)] r_o \tag{7.51}$$

Thus, emitter degeneration multiplies the transistor output resistance r_o by the factor $[1 + g_m(R_e \| r_\pi)]$.

Finally, for completeness and future reference we show in Fig. 7.20(b) the BJT equivalent of Fig. 7.13. Here both R_{in} and R_o of a grounded-base BJT are shown. Note that we have not provided the derivation of R_{in}.

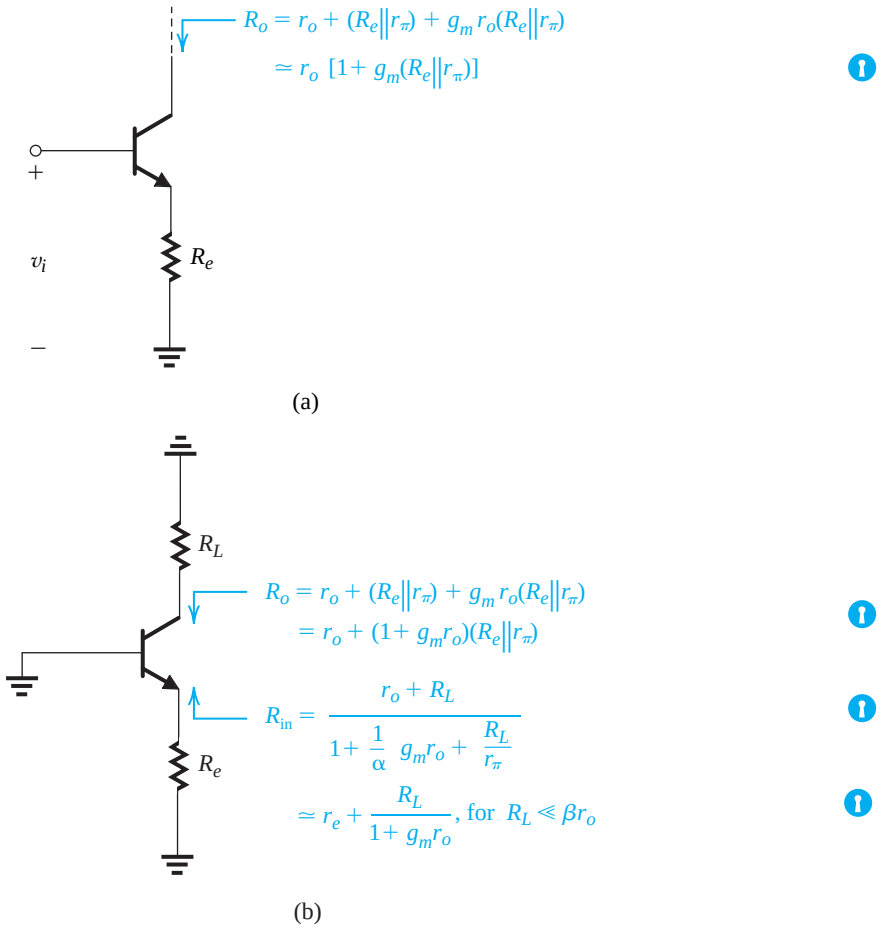


Figure 7.20 **(a)** Output resistance of a CE amplifier with emitter degeneration; **(b)** The impedance transformation properties of the CB amplifier. Note that for $\beta = \infty$, these formulas reduce to those for the MOSFET case (Fig. 7.13).

EXERCISE

7.13 Find the output resistance of a CE amplifier biased at $I_C = 1$ mA and having a resistance of 500 Ω connected in its emitter. Let $\beta = 100$ and $V_A = 10$ V. What is the value of the output resistance without degeneration.?

Ans. 177 kΩ; 10 kΩ

7.3.9 BiCMOS Cascodes

Certain advanced CMOS technologies allow the fabrication of bipolar transistors, thus permitting the circuit designer to combine MOS and bipolar transistors in circuits that take advantage of the unique features of each. The resulting technology is called BiCMOS, and the circuits are referred to as BiCMOS circuits.

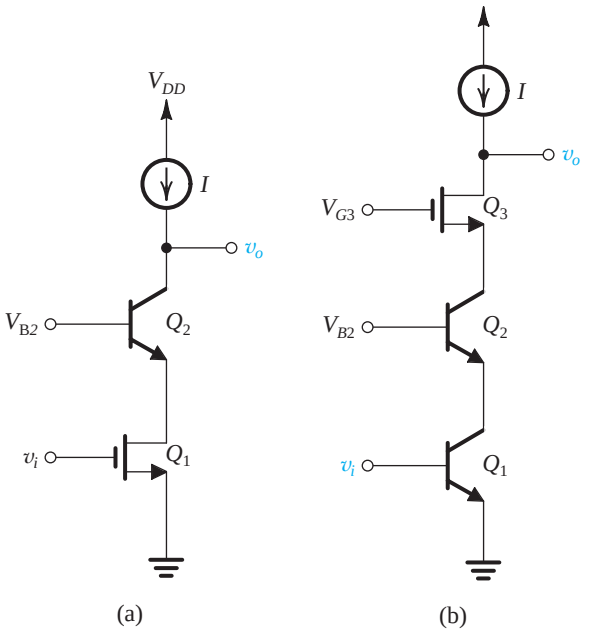


Figure 7.21 BiCMOS cascodes.

Figure 7.21 shows two possible BiCMOS cascode amplifiers. The circuit in Fig. 7.21(a) uses a MOS transistor for the amplifying device and a BJT for the cascode device. This circuit has the advantage of an infinite input resistance compared with an input resistance of r_π, obtained in the all-bipolar case. As well, the use of a bipolar transistor for the cascode stage can result in an increased output resistance as compared to the all-MOS case [because β of the bipolar transistor is usually higher than $(g_m r_o)$ of the MOSFET].

The circuit of Fig. 7.21(b) uses a MOS transistor Q_3 to implement double cascoding. Recall that double cascoding is not possible with BJT circuits alone.

EXERCISE

7.14 For $I = 100\ \mu A$, find G_m, R_o, and A_{vo} of the BiCMOS amplifiers in Fig. 7.21. Let $V_A = 5$ V (for both MOS and bipolar transistors), $\beta = 100$, $\mu_n C_{ox} = 200\ \mu A/V^2$, and $W/L = 25$.
Ans. (a) 1 mA/V, 3.33 MΩ, -3.33×10^3 V/V; (b) 4 mA/V, 167 MΩ, -668×10^3 V/V

7.4 IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits

Biasing in integrated-circuit design is based on the use of constant-current sources. On an IC chip with a number of amplifier stages, a constant dc current (called a **reference current**) is generated at one location and is then replicated at various other locations for biasing the

various amplifier stages through a process known as **current steering**. This approach has the advantage that the effort expended on generating a predictable and stable reference current, usually utilizing a precision resistor external to the chip or a special circuit on the chip, need not be repeated for every amplifier stage. Furthermore, the bias currents of the various stages track each other in case of changes in power-supply voltage or in temperature.

In this section we study circuit building blocks and techniques employed in the bias design of IC amplifiers. These current-source circuits are also utilized as amplifier load elements, as we have seen in Sections 7.2 and 7.3.

7.4.1 The Basic MOSFET Current Source

Figure 7.22 shows the circuit of a simple MOS constant-current source. The heart of the circuit is transistor Q_1, the drain of which is shorted to its gate,[4] thereby forcing it to operate in the saturation mode with

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1 (V_{GS} - V_{tn})^2 \tag{7.52}$$

where we have neglected channel-length modulation. The drain current of Q_1 is supplied by V_{DD} through resistor R, which in most cases would be outside the IC chip. Since the gate currents are zero,

$$I_{D1} = I_{\text{REF}} = \frac{V_{DD} - V_{GS}}{R} \tag{7.53}$$

where the current through R is considered to be the reference current of the current source and is denoted I_{REF}. Equations (7.52) and (7.53) can be used to determine the value required for R.

Now consider transistor Q_2: It has the same V_{GS} as Q_1; thus, if we assume that it is operating in saturation, its drain current, which is the output current I_O of the current source, will be

$$I_O = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2 \tag{7.54}$$

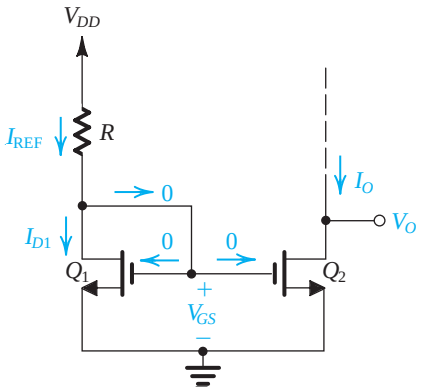


Figure 7.22 Circuit for a basic MOSFET constant-current source. For proper operation, the output terminal, that is, the drain of Q_2, must be connected to a circuit that ensures that Q_2 operates in saturation.

[4]Such a transistor is said to be *diode connected*.

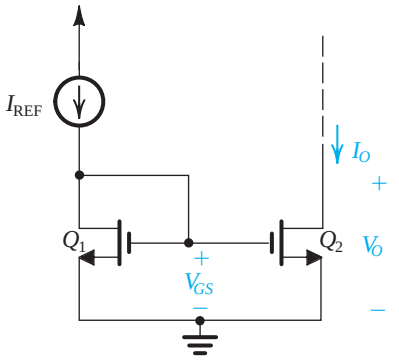


Figure 7.23 Basic MOSFET current mirror.

where we have neglected channel-length modulation. Equations (7.52) and (7.54) enable us to relate the output current I_O to the reference current I_{REF} as follows:

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \tag{7.55}$$

This is a simple and attractive relationship: The special connection of Q_1 and Q_2 provides an output current I_O that is related to the reference current I_{REF} by the aspect ratios of the transistors. In other words, the relationship between I_O and I_{REF} is solely determined by the geometries of the transistors. In the special case of identical transistors, $I_O = I_{REF}$, and the circuit simply replicates or mirrors the reference current in the output terminal. This has given the circuit composed of Q_1 and Q_2 the name **current mirror**, a name that is used irrespective of the ratio of device dimensions.

Figure 7.23 depicts the current-mirror circuit with the input reference current shown as being supplied by a current source for both simplicity and generality. The **current gain** or **current transfer ratio** of the current mirror is given by Eq. (7.55).

Effect of V_O on I_O In the description above for the operation of the current source of Fig. 7.22, we assumed Q_2 to be operating in saturation. This is essential if Q_2 is to supply a constant-current output. To ensure that Q_2 is saturated, the circuit to which the drain of Q_2 is to be connected must establish a drain voltage V_O that satisfies the relationship

$$V_O \geq V_{GS} - V_{tn} \tag{7.56}$$

or, equivalently, in terms of the overdrive voltage V_{OV} of Q_1 and Q_2,

$$V_O \geq V_{OV} \tag{7.57}$$

In other words, the current source will operate properly with an output voltage V_O as low as V_{OV}, which is a few tenths of a volt.

Although thus far neglected, channel-length modulation can have a significant effect on the operation of the current source. Consider, for simplicity, the case of identical devices Q_1 and Q_2. The drain current of Q_2, I_O, will equal the current in Q_1, I_{REF}, at the value of V_O that causes the two devices to have the same V_{DS}, that is, at $V_O = V_{GS}$. As V_O is increased above this value, I_O will increase according to the incremental output resistance r_{o2} of Q_2. This is illustrated in Fig. 7.24, which shows I_O versus V_O. Observe that since Q_2 is operating at a constant V_{GS} (determined by passing I_{REF} through the matched device Q_1), the

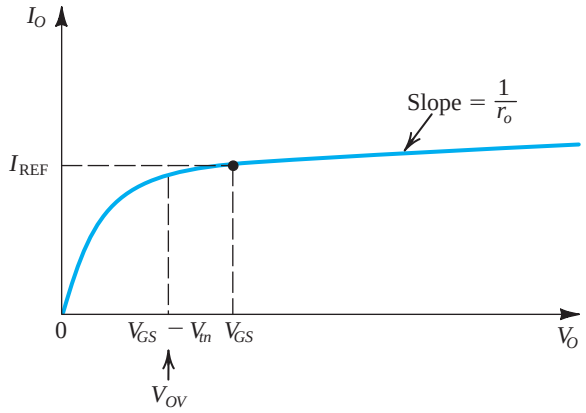


Figure 7.24 Output characteristic of the current source in Fig. 7.22 and the current mirror of Fig. 7.23 for the case of Q_2 matched to Q_1.

curve in Fig. 7.24 is simply the i_D–v_{DS} characteristic curve of Q_2 for v_{GS} equal to the particular value V_{GS}.

In summary, the current source of Fig. 7.22 and the current mirror of Fig. 7.23 have a finite output resistance R_o,

$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O} \tag{7.58}$$

where I_O is given by Eq. (7.54) and V_{A2} is the Early voltage of Q_2. Also, recall that for a given process technology, V_A is proportional to the transistor channel length; thus, to obtain high output-resistance values, current sources are usually designed using transistors with relatively long channels. Finally, note that we can express the current I_O as

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} \left(1 + \frac{V_O - V_{GS}}{V_{A2}}\right) \tag{7.59}$$

Example 7.5

Given $V_{DD} = 3$ V and using $I_{REF} = 100$ μA, design the circuit of Fig. 7.22 to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 μm, channel widths of 10 μm, $V_t = 0.7$ V, and $k_n' = 200$ μA/V^2. What is the lowest possible value of V_O? Assuming that for this process technology, the Early voltage $V_A' = 20$ V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a +1-V change in V_O.

Solution

$$I_{D1} = I_{REF} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 V_{OV}^2$$

$$100 = \frac{1}{2} \times 200 \times 10 V_{OV}^2$$

Thus,

$$V_{OV} = 0.316 \text{ V}$$

Example 7.5 *continued*

and

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.316 \simeq 1 \text{ V}$$

$$R = \frac{V_{DD} - V_{GS}}{I_{\text{REF}}} = \frac{3 - 1}{0.1 \text{ mA}} = 20 \text{ k}\Omega$$

$$V_{O\min} = V_{OV} \simeq 0.3 \text{ V}$$

For the transistors used, $L = 1$ μm. Thus,

$$V_A = 20 \times 1 = 20 \text{ V}$$

$$r_{o2} = \frac{20 \text{ V}}{100 \text{ μA}} = 0.2 \text{ M}\Omega$$

The output current will be 100 μA at $V_O = V_{GS} = 1$ V. If V_O changes by +1 V, the corresponding change in I_O will be

$$\Delta I_O = \frac{\Delta V_O}{r_{o2}} = \frac{1 \text{ V}}{0.2 \text{ M}\Omega} = 5 \text{ μA}$$

EXERCISE

D7.15 In the current source of Example 7.5, it is required to reduce the change in output current, ΔI_O, corresponding to a change in output voltage, ΔV_O, of 1 V to 1% of I_O. What should the dimensions of Q_1 and Q_2 be changed to? Assume that Q_1 and Q_2 are to remain matched.
Ans. $L = 5$ μm; $W = 50$ μm

7.4.2 MOS Current-Steering Circuits

As mentioned earlier, once a constant current has been generated, it can be replicated to provide dc bias or load currents for the various amplifier stages in an IC. Current mirrors can obviously be used to implement this current-steering function. Figure 7.25 shows a simple current-steering circuit. Here Q_1 together with R determine the reference current I_{REF}. Transistors Q_1, Q_2, and Q_3 form a two-output current mirror,

$$I_2 = I_{\text{REF}} \frac{(W/L)_2}{(W/L)_1} \tag{7.60}$$

$$I_3 = I_{\text{REF}} \frac{(W/L)_3}{(W/L)_1} \tag{7.61}$$

To ensure operation in the saturation region, the voltages at the drains of Q_2 and Q_3 are constrained as follows:

$$V_{D2},\ V_{D3} \geq -V_{SS} + V_{GS1} - V_{tn} \tag{7.62}$$

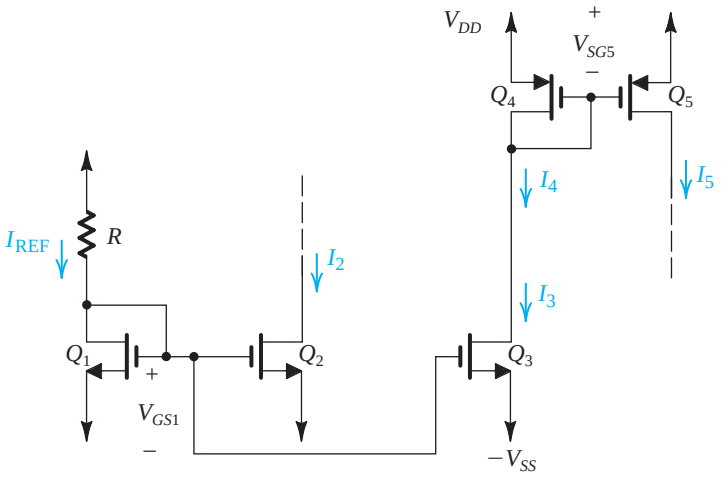


Figure 7.25 A current-steering circuit.

or, equivalently,

$$V_{D2},\ V_{D3} \geq -V_{SS} + V_{OV1} \tag{7.63}$$

where V_{OV1} is the overdrive voltage at which Q_1, Q_2, and Q_3 are operating. In other words, the drains of Q_2 and Q_3 will have to remain higher than $-V_{SS}$ by at least the overdrive voltage, which is usually a few tenths of a volt.

Continuing our discussion of the circuit in Fig. 7.25, we see that current I_3 is fed to the input side of a current mirror formed by PMOS transistors Q_4 and Q_5. This mirror provides

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4} \tag{7.64}$$

where $I_4 = I_3$. To keep Q_5 in saturation, its drain voltage should be

$$V_{D5} \leq V_{DD} - |V_{OV5}| \tag{7.65}$$

where V_{OV5} is the overdrive voltage at which Q_5 is operating.

The constant current I_2 generated in the circuit of Fig. 7.25 can be used to bias a source-follower amplifier such as that implemented by transistor Q_6 in Fig. 7.26(a). Similarly, the constant current I_5 can be used as the load for a common-source amplifier such as that implemented with transistor Q_7 in Fig. 7.26(b).

Finally, an important point to note is that in the circuit of Fig. 7.25, while Q_2 *pulls* its current I_2 from a circuit (not shown in Fig. 7.25), Q_5 *pushes* its current I_5 into a circuit (not shown in Fig. 7.25). Thus Q_5 is appropriately called a **current source**, whereas Q_2 should more properly be called a **current sink**. In an IC, both current sources and current sinks are usually needed. The difference between a current source and a current sink is further illustrated in Fig. 7.27, where $V_{CS\,\min}$ denotes the minimum voltage needed across the current source (or sink) for its proper operation.

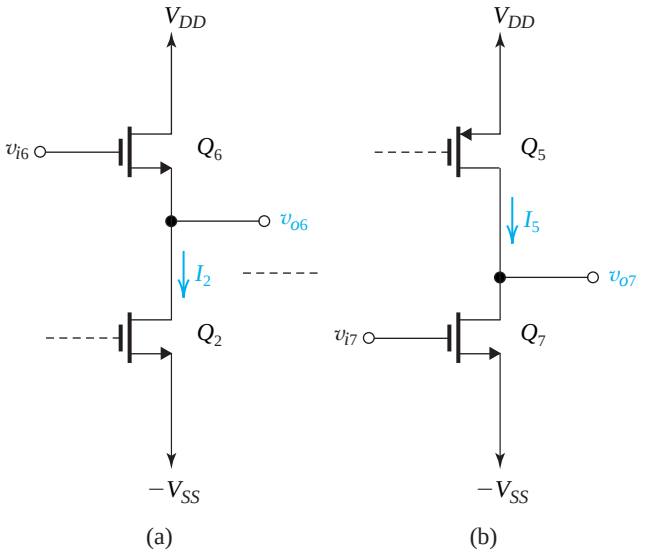


Figure 7.26 Application of the constant currents I_2 and I_5 generated in the current-steering circuit of Fig. 7.25. Constant-current I_2 is the bias current for the source follower Q_6, and constant-current I_5 is the load current for the common-source amplier Q_7.

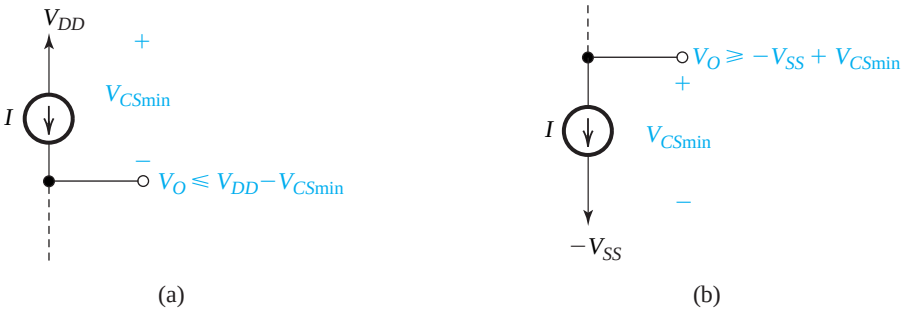


Figure 7.27 (**a**) A current source; and (**b**) a current sink.

EXERCISE

D 7.16 For the circuit of Fig. 7.25, let $V_{DD} = V_{SS} = 1.5$ V, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, all channel lengths = 1 μm, $k_n' = 200\ \mu A/V^2$, $k_p' = 80\ \mu A/V^2$, and $\lambda = 0$. For $I_{REF} = 10\ \mu A$, find the widths of all transistors to obtain $I_2 = 60\ \mu A$, $I_3 = 20\ \mu A$, and $I_5 = 80\ \mu A$. It is further required that the voltage at the drain of Q_2 be allowed to go down to within 0.2 V of the negative supply and that the voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply.

Ans. $W_1 = 2.5\ \mu m$; $W_2 = 15\ \mu m$; $W_3 = 5\ \mu m$; $W_4 = 12.5\ \mu m$; $W_5 = 50\ \mu m$

7.4.3 BJT Circuits

The basic BJT current mirror is shown in Fig. 7.28. It works in a fashion very similar to that of the MOS mirror. However, there are two important differences: First, the nonzero base current of the BJT (or, equivalently, the finite β) causes an error in the current transfer ratio

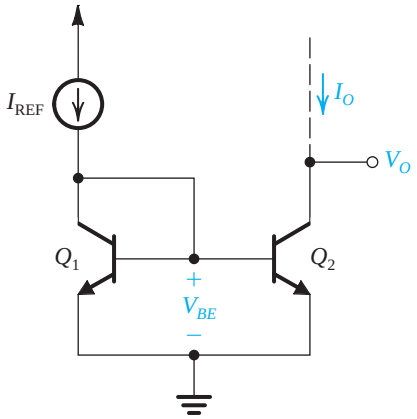


Figure 7.28 The basic BJT current mirror.

of the bipolar mirror. Second, the current transfer ratio is determined by the relative areas of the emitter–base junctions of Q_1 and Q_2.

Let us first consider the case of β sufficiently high that we can neglect the base currents. The reference current I_{REF} is passed through the diode-connected transistor Q_1 and thus establishes a corresponding voltage V_{BE}, which in turn is applied between base and emitter of Q_2. Now, if Q_2 is matched to Q_1 or, more specifically, if the EBJ area of Q_2 is the same as that of Q_1, and thus Q_2 has the same scale current I_S as Q_1, then the collector current of Q_2 will be equal to that of Q_1; that is,

$$I_O = I_{REF} \tag{7.66}$$

For this to happen, however, Q_2 must be operating in the active mode, which in turn is achieved as long as the collector voltage V_O is 0.3 V or so higher than that of the emitter.

To obtain a current transfer ratio other than unity, say m, we simply arrange that the area of the EBJ of Q_2 is m times that of Q_1. In this case,

$$I_O = mI_{REF} \tag{7.67}$$

In general, the current transfer ratio is given by

$$\frac{I_O}{I_{REF}} = \frac{I_{S2}}{I_{S1}} = \frac{\text{Area of EBJ of } Q_2}{\text{Area of EBJ of } Q_1} \tag{7.68}$$

Alternatively, if the area ratio m is an integer, one can think of Q_2 as equivalent to m transistors, each matched to Q_1 and connected in parallel.

Next we consider the effect of finite transistor β on the current transfer ratio. The analysis for the case in which the current transfer ratio is nominally unity—that is, for the case in which Q_2 is matched to Q_1—is illustrated in Fig. 7.29. The key point here is that since Q_1 and Q_2 are matched and have the same V_{BE}, their collector currents will be equal. The rest of the analysis is straightforward. A node equation at the collector of Q_1 yields

$$I_{REF} = I_C + 2I_C/\beta = I_C\left(1 + \frac{2}{\beta}\right)$$

Finally, since $I_O = I_C$, the current transfer ratio can be found as

$$\frac{I_O}{I_{REF}} = \frac{I_C}{I_C\left(1 + \frac{2}{\beta}\right)} = \frac{1}{1 + \frac{2}{\beta}} \tag{7.69}$$

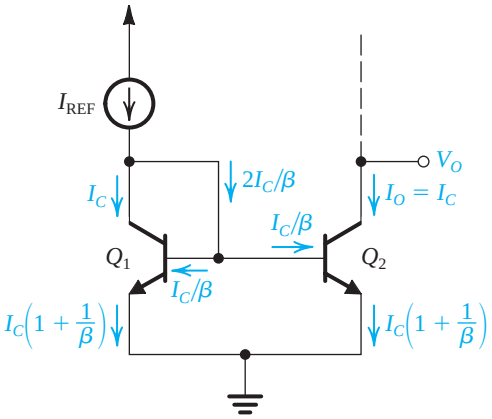


Figure 7.29 Analysis of the current mirror taking into account the finite β of the BJTs.

Note that as β approaches ∞, I_O/I_{REF} approaches the nominal value of unity. For typical values of β, however, the error in the current transfer ratio can be significant. For instance, $\beta = 100$ results in a 2% error in the current transfer ratio. Furthermore, the error due to the finite β increases as the nominal current transfer ratio is increased. The reader is encouraged to show that for a mirror with a nominal current transfer ratio m—that is, one in which $I_{S2} = mI_{S1}$—the actual current transfer ratio is given by

$$\frac{I_O}{I_{REF}} = \frac{m}{1+\dfrac{m+1}{\beta}} \tag{7.70}$$

In common with the MOS current mirror, the BJT mirror has a finite output resistance R_o,

$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O} \tag{7.71}$$

where V_{A2} and r_{o2} are the Early voltage and the output resistance, respectively, of Q_2. Thus, even if we neglect the error due to finite β, the output current I_O will be at its nominal value only when Q_2 has the same V_{CE} as Q_1, namely at $V_O = V_{BE}$. As V_O is increased, I_O will correspondingly increase. Taking both the finite β and the finite R_o into account, we can express the output current of a BJT mirror with a nominal current transfer ratio m as

$$I_O = I_{REF}\left(\frac{m}{1+\dfrac{m+1}{\beta}}\right)\left(1+\frac{V_O - V_{BE}}{V_{A2}}\right) \tag{7.72}$$

where we note that the error term due to the Early effect is expressed in a form that shows that it reduces to zero for $V_O = V_{BE}$.

EXERCISE

7.17 Consider a BJT current mirror with a nominal current transfer ratio of unity. Let the transistors have $I_S = 10^{-15}$ A, $\beta = 100$, and $V_A = 100$ V. For $I_{REF} = 1$ mA, find I_O when $V_O = 5$ V. Also, find the output resistance.

Ans. 1.02 mA; 100 kΩ

A Simple Current Source In a manner analogous to that in the MOS case, the basic BJT current mirror can be used to implement a simple current source, as shown in Fig. 7.30. Here the reference current is

$$I_{\text{REF}} = \frac{V_{CC} - V_{BE}}{R} \tag{7.73}$$

where V_{BE} is the base–emitter voltage corresponding to the desired value of I_{REF}. The output current I_O is given by

$$I_O = \frac{I_{\text{REF}}}{1 + (2/\beta)} \left(1 + \frac{V_O - V_{BE}}{V_A}\right) \tag{7.74}$$

The output resistance of this current source is r_o of Q_2,

$$R_o \ (= r_{o2}) \simeq \frac{V_A}{I_O} \simeq \frac{V_A}{I_{\text{REF}}} \tag{7.75}$$

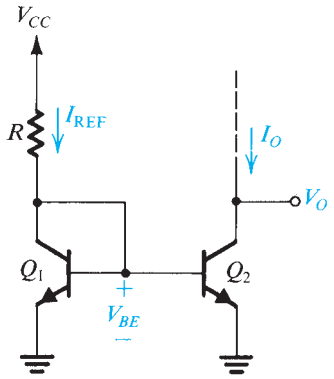


Figure 7.30 A simple BJT current source.

EXERCISE

D7.18 Assuming the availability of BJTs with scale currents $I_S = 10^{-15}$ A, $\beta = 100$, and $V_A = 50$ V, design the current-source circuit of Fig. 7.30 to provide an output current $I_O = 0.5$ mA at $V_O = 2$ V. The power supply $V_{CC} = 5$ V. Give the values of I_{REF}, R, and $V_{O\text{min}}$. Also, find I_O at $V_O = 5$ V.

Ans. 0.497 mA; 8.71 kΩ; 0.3 V; 0.53 mA

Current Steering To generate bias currents for different amplifier stages in an IC, the current-steering approach described for MOS circuits can be applied in the bipolar case. As an example, consider the circuit shown in Fig. 7.31. The dc reference current I_{REF} is gener-

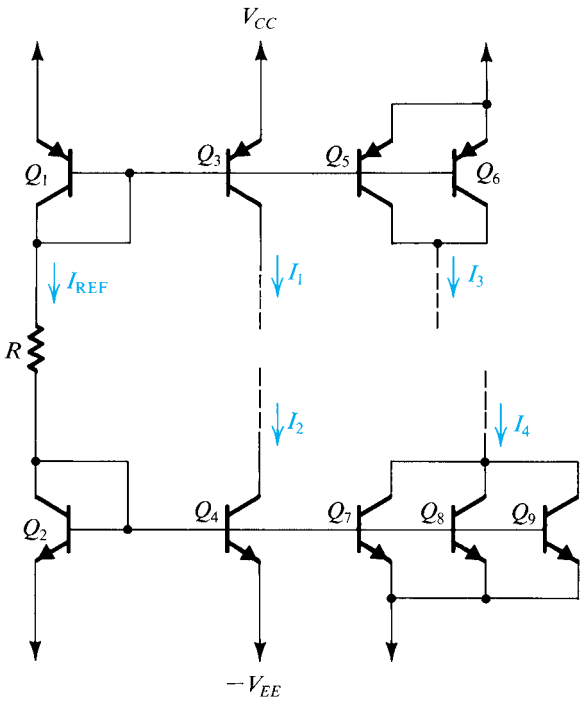


Figure 7.31 Generation of a number of constant currents of various magnitudes.

ated in the branch that consists of the diode-connected transistor Q_1, resistor R, and the diode-connected transistor Q_2:

$$I_{\text{REF}} = \frac{V_{CC} + V_{EE} - V_{EB1} - V_{BE2}}{R} \tag{7.76}$$

Now, for simplicity, assume that all the transistors have high β and thus that the base currents are negligibly small. We will also neglect the Early effect. The diode-connected transistor Q_1 forms a current mirror with Q_3; thus Q_3 will supply a constant current I equal to I_{REF}. Transistor Q_3 can supply this current to any load as long as the voltage that develops at the collector does not exceed $(V_{CC} - 0.3\text{ V})$; otherwise Q_3 would enter the saturation region.

To generate a dc current twice the value of I_{REF}, two transistors, Q_5 and Q_6, each of which is matched to Q_1, are connected in parallel, and the combination forms a mirror with Q_1. Thus $I_3 = 2I_{\text{REF}}$. Note that the parallel combination of Q_5 and Q_6 is equivalent to a transistor with an EBJ area double that of Q_1, which is precisely what is done when this circuit is fabricated in IC form.

Transistor Q_4 forms a mirror with Q_2; thus Q_4 provides a constant current I_2 equal to I_{REF}. Note that while Q_3 *sources* its current to parts of the circuit whose voltage should not exceed $(V_{CC} - 0.3\text{ V})$, Q_4 *sinks* its current from parts of the circuit whose voltage should not decrease below $-V_{EE} + 0.3$ V. Finally, to generate a current three times I_{REF}, three transistors, Q_7, Q_8, and Q_9, each of which is matched to Q_2, are connected in parallel, and the combination is placed in a mirror configuration with Q_2. Again, in an IC implementation, Q_7, Q_8, and Q_9 would be replaced with a transistor having a junction area three times that of Q_2.

EXERCISE

7.19 Figure E7.19 shows an N-output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \cdots = I_N = \frac{I_{\text{REF}}}{1 + (N+1)/\beta}$$

For $\beta = 100$, find the maximum number of outputs for an error not exceeding 10%.

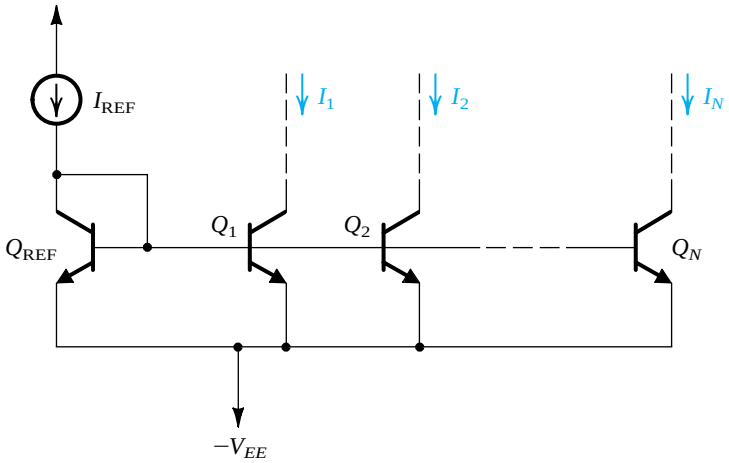


Figure E7.19

Ans. 9

7.5 Current-Mirror Circuits with Improved Performance

As we have seen throughout this chapter, current sources play a major role in the design of IC amplifiers: The constant-current source is used both in biasing and as active load. Simple forms of both MOS and bipolar current sources and, more generally, current mirrors were studied in Section 7.4. The need to improve the characteristics of the simple sources and mirrors has already been demonstrated. Specifically, two performance parameters need to be addressed: the *accuracy of the current transfer ratio of the mirror* and the *output resistance of the current source*.

The reader will recall from Section 7.4 that the accuracy of the current transfer ratio suffers particularly from the finite β of the BJT. The output resistance, which in the simple circuits is limited to r_o of the MOSFET and the BJT, also reduces accuracy and, much more seriously, severely limits the gain available from cascode amplifiers (Section 7.3). In this section we study MOS and bipolar current mirrors with more accurate current transfer ratios and higher output resistances.

7.5.1 Cascode MOS Mirrors

The use of cascoding in the design of current sources was presented in Section 7.3. Figure 7.32 shows the basic cascode current mirror. Observe that in addition to the diode-connected transistor Q_1, which forms the basic mirror Q_1–Q_2, another diode-connected transistor, Q_4, is used to provide a suitable bias voltage for the gate of the cascode transistor Q_3. To determine the output resistance of the cascode mirror at the drain of Q_3, we assume that the voltages across Q_1 and Q_4 are constant, and thus the signal voltages at the gates of Q_2 and Q_3 will be zero. Thus R_o will be that of the cascode current source formed by Q_2 and Q_3,

$$R_o \simeq g_{m3} r_{o3} r_{o2} \tag{7.77}$$

Thus, as expected, cascoding raises the output resistance of the current source by the factor $(g_{m3}r_{o3})$, which is the intrinsic gain of the cascode transistor.

A drawback of the cascode current mirror is that it consumes a relatively large portion of the steadily shrinking supply voltage V_{DD}. While the simple MOS mirror operates properly with a voltage as low as V_{OV} across its output transistor, the cascode circuit of Fig. 7.32 requires a minimum voltage of $V_t + 2V_{OV}$. This is because the gate of Q_3 is at $2V_{GS} = 2V_t + 2V_{OV}$. Thus the minimum voltage required across the output of the cascode mirror is 1 V or so. This obviously limits the signal swing at the output of the mirror (i.e., at the output of the amplifier that utilizes this current source as a load). In Chapter 12 we shall study a wide-swing cascode mirror.

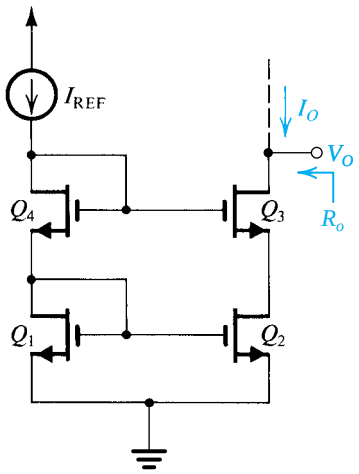


Figure 7.32 A cascode MOS current mirror.

EXERCISE

7.20 For a cascode MOS mirror utilizing devices with $V_t = 0.5$ V, $\mu_n C_{ox} = 387\ \mu\text{A/V}^2$, $V_A' = 5$ V/μm, $W/L = 3.6\ \mu\text{m}/0.36\ \mu\text{m}$, and $I_{REF} = 100\ \mu\text{A}$, find the minimum voltage required at the output and the output resistance.

Ans. 0.95 V; 285 kΩ

7.5.2 A Bipolar Mirror with Base-Current Compensation

Figure 7.33 shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of the simple current mirror. The reduced dependence on β is achieved by including transistor Q_3, the emitter of which supplies the base currents of Q_1 and Q_2. The sum of the base currents is then divided by $(\beta_3 + 1)$, resulting in a much smaller error current that has to be supplied by I_{REF}. Detailed analysis is shown on the circuit diagram; it is based on the assumption that Q_1 and Q_2 are matched and thus have equal collector currents, I_C. A node equation at the node labeled x gives

$$I_{REF} = I_C\left[1 + \frac{2}{\beta(\beta+1)}\right]$$

Since

$$I_O = I_C$$

the current transfer ratio of the mirror will be

$$\frac{I_O}{I_{REF}} = \frac{1}{1 + 2/(\beta^2 + \beta)} \simeq \frac{1}{1 + 2/\beta^2} \tag{7.78}$$

which means that the error due to finite β has been reduced from $2/\beta$ in the simple mirror to $2/\beta^2$, a tremendous improvement. Unfortunately, however, the output resistance remains approximately equal to that of the simple mirror, namely r_o. Finally, note that if a reference current I_{REF} is not available, we simply connect node x to the power supply, V_{CC} through a resistance R. The result is a reference current given by

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R} \tag{7.79}$$

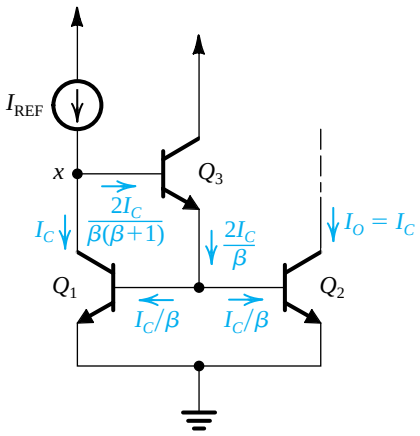


Figure 7.33 A current mirror with base-current compensation.

7.5.3 The Wilson Current Mirror

A simple but ingenious modification of the basic bipolar mirror results in both reducing the β dependence and increasing the output resistance. The resulting circuit, known as the **Wilson**

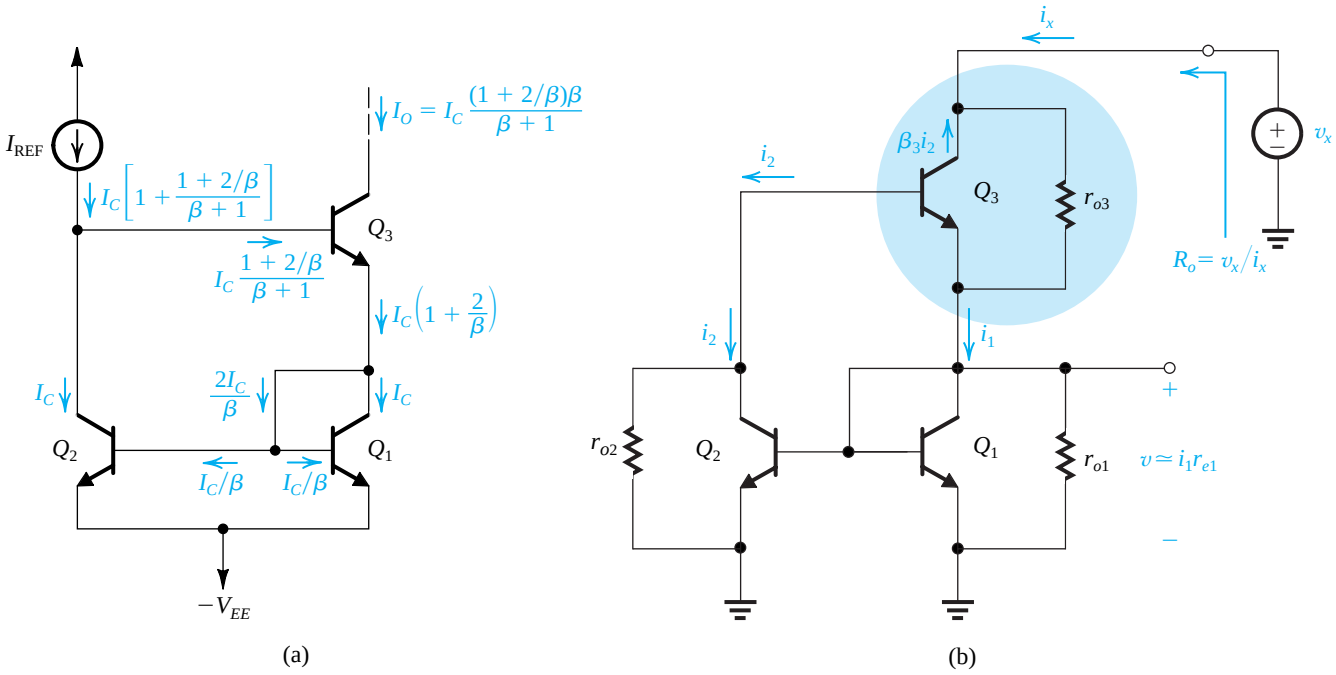


Figure 7.34 The Wilson bipolar current mirror: **(a)** circuit showing analysis to determine the current transfer ratio; **(b)** determining the output resistance.

mirror after its inventor George Wilson, an IC design engineer working for Tektronix, is shown in Fig. 7.34(a). The analysis to determine the effect of finite β on the current transfer ratio is shown in Fig. 7.34(a), from which we can write

$$\frac{I_O}{I_{REF}} = \frac{I_C\left(1 + \frac{2}{\beta}\right)\beta/(\beta+1)}{I_C\left[1 + \left(1 + \frac{2}{\beta}\right)/(\beta+1)\right]}$$

$$= \frac{\beta+2}{\beta+1+\frac{\beta+2}{\beta}} = \frac{\beta+2}{\beta+2+\frac{2}{\beta}}$$

$$= \frac{1}{1+\frac{2}{\beta(\beta+2)}}$$

$$\simeq \frac{1}{1+2/\beta^2} \tag{7.80}$$

This analysis assumes that Q_1 and Q_2 conduct equal collector currents. There is, however, a slight problem with this assumption: The collector-to-emitter voltages of Q_1 and Q_2 are not equal, which introduces a current offset or a systematic error. The problem can be solved

by adding a diode-connected transistor in series with the collector of Q_2, as we shall shortly show for the MOS version.

To determine the output resistance of the Wilson mirror, we set $I_{\text{REF}} = 0$ and apply a test voltage v_x to the output node, as shown in Fig. 7.34(b). Our purpose is to determine the current i_x and hence R_o as

$$R_o = v_x / i_x$$

Rather than replacing each transistor with its hybrid-π model, we shall do the analysis directly on the circuit diagram. For this purpose, we have "pulled r_o out" of each transistor and shown it separately.

Observe that transistor Q_3, viewed as a supernode (highlighted in color), has a current i_x entering it and two currents i_1 and i_2 exiting it; thus,

$$i_1 + i_2 = i_x$$

Next note that the action of current mirror $Q_1 - Q_2$ forces i_2 to be approximately equal to i_1; thus,

$$i_2 \simeq i_1 = i_x/2$$

Current i_2 flows into the base of Q_3 and thus gives rise to a collector current $\beta_3 i_2$ in the direction indicated. We are now in a position to write a node equation at the collector of Q_3 and thus determine the current through r_{o2} as $i_x + \beta_3 i_2 = i_x + \beta_3(i_x/2) = i_x(\beta_3/2 + 1)$. Finally, we can express the voltage between the collector of Q_3 and ground as the sum of the voltage drop across r_{o3} and the voltage v across Q_1,

$$\begin{aligned} v_x &= i_x\left(\frac{\beta_3}{2} + 1\right) r_{o3} + i_1 r_{e1} \\ &= i_x\left(\frac{\beta_3}{2} + 1\right) r_{o3} + \left(\frac{i_x}{2}\right) r_{e1} \end{aligned}$$

Since $r_o \gg r_e$ and $\beta_3 \gg 2$,

$$v_x \simeq i_x\left(\frac{\beta_3}{2}\right) r_{o3}$$

and

$$R_o = \beta_3 r_{o3}/2 \tag{7.81}$$

Thus the Wilson current mirror has an output resistance $(\frac{1}{2}\beta_3)$ times higher than that of Q_3 alone. This is a result of the negative feedback obtained by feeding the collector current of Q_2 (i_2) back to the base of Q_3. As can be seen from the above analysis, this feedback results in increasing the current through r_{o3} to approximately $\frac{1}{2}\beta_3 i_x$, and thus the voltage across r_{o3} and the output resistance increase by the same factor, $\frac{1}{2}\beta_3$. Finally, note that the factor $\frac{1}{2}$ is because only half of i_x is mirrored back to the base of Q_3.

The Wilson mirror is preferred over the cascode circuit because the latter has the same dependence on β as the simple mirror. However, like the cascode mirror, the Wilson mirror requires an additional V_{BE} drop for its operation; that is, for proper operation we must allow for 1 V or so across the Wilson mirror output.

EXERCISE

7.21 For $\beta = 100$ and $r_o = 100\ \text{k}\Omega$, contrast the Wilson mirror and the simple mirror by evaluating the transfer-ratio error due to finite β, and the output resistance.
Ans. Transfer-ratio error: 0.02% for Wilson as opposed to 2% for the simple circuit; $R_o = 5\ \text{M}\Omega$ for Wilson compared to 100 kΩ for the simple circuit

7.5.4 The Wilson MOS Mirror

Figure 7.35(a) shows the MOS version of the Wilson mirror. Obviously there is no β error to reduce here, and the advantage of the MOS Wilson lies in its enhanced output resistance.

To determine the output resistance of the Wilson MOS mirror, we set $I_{\text{REF}} = 0$, and apply a test voltage v_x to the output node, as shown in Fig. 7.35(b). Our purpose is to determine the current i_x and hence R_o as

$$R_o = v_x / i_x$$

Rather than replacing each transistor with its hybrid-π, equivalent-circuit model, we shall perform the analysis directly on the circuit. For this purpose, we have "pulled r_o out" of each transistor and shown it separately.

Observe that the current i_x that enters the drain of Q_3 must exit at its source. Thus the current that feeds the input side of the Q_1–Q_2 mirror is equal to i_x. Most of this current will flow in the drain proper of Q_1 (i.e., only a very small fraction flows through r_{o1}) and will give rise to a voltage $v \simeq i_x / g_{m1}$, where $1/g_{m1}$ is the approximate resistance of the diode-connected transistor Q_1. The current-mirror action of (Q_1, Q_2) forces a current equal to i_x to flow through the drain proper of Q_2. Now, since the current in the drain of Q_2 is forced (by the connection to the gate of Q_3) to be zero, all of i_x must flow through r_{o2}, resulting in a voltage $-i_x r_{o2}$. This is the voltage fed back to the gate of Q_3. The drain current of Q_3 can now be found as

$$\begin{aligned} i_{d3} &= g_{m3} v_{gs3} \\ &= g_{m3}(v_{g3} - v_{s3}) \\ &= g_{m3}(-i_x r_{o2} - i_x / g_{m1}) \\ &\simeq -(g_{m3} r_{o2}) i_x \end{aligned}$$

A node equation at the drain of Q_3 gives the current through r_{o3} as $(i_x - i_{d3}) = i_x + g_{m3} r_{o2} i_x \simeq g_{m3} r_{o2} i_x$. Finally, we can express v_x as the sum of the voltage drop across r_{o3} and the voltage v across Q_1,

$$\begin{aligned} v_x &= g_{m3} r_{o2} i_x r_{o3} + v \\ &= (g_{m3} r_{o3} r_{o2}) i_x + (i_x / g_{m1}) \\ &\simeq g_{m3} r_{o3} r_{o2} i_x \end{aligned}$$

and obtain

$$R_o = \frac{v_x}{i_x} = (g_{m3} r_{o3}) r_{o2} \tag{7.82}$$

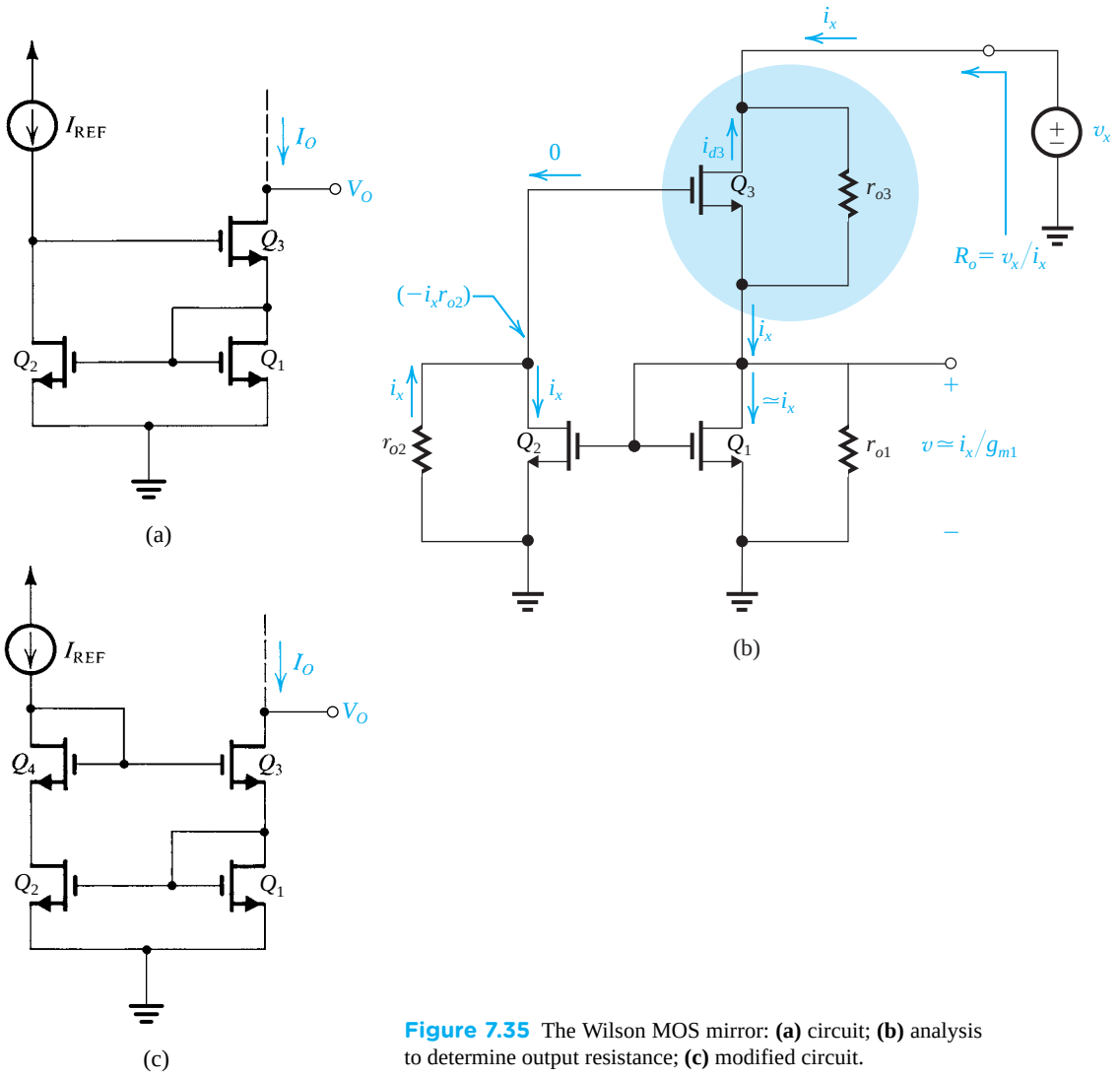


Figure 7.35 The Wilson MOS mirror: **(a)** circuit; **(b)** analysis to determine output resistance; **(c)** modified circuit.

Thus, the Wilson MOS mirror exhibits an increase of output resistance by a factor $(g_{m3}r_{o3})$, an identical result to that achieved in the cascode mirror. Here the increase in R_o, as demonstrated in the analysis above, is a result of the negative feedback obtained by connecting the drain of Q_2 to the gate of Q_3. Finally, to balance the two branches of the mirror and thus avoid the systematic current error resulting from the difference in V_{DS} between Q_1 and Q_2, the circuit can be modified as shown in Fig. 7.35(c).

7.5.5 The Widlar Current Source[5]

Our final current-source circuit, known as the **Widlar current source**, is shown in Fig. 7.36. It differs from the basic current mirror circuit in an important way: A resistor R_E is included in

[5]Named after Robert Widlar, a pioneer in analog IC design.

the emitter lead of Q_2. Neglecting base currents we can write

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \tag{7.83}$$

and

$$V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right) \tag{7.84}$$

where we have assumed that Q_1 and Q_2 are matched devices. Combining Eqs. (7.83) and (7.84) gives

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \tag{7.85}$$

But from the circuit we see that

$$V_{BE1} = V_{BE2} + I_O R_E \tag{7.86}$$

Thus,

$$I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \tag{7.87}$$

The design and advantages of the Widlar current source are illustrated in the following example.

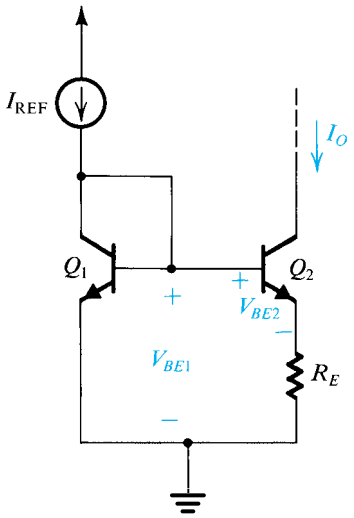


Figure 7.36 The Widlar current source.

Example 7.6

The two circuits for generating a constant current I_O = 10 μA shown in Fig. 7.37 operate from a 10-V supply. Determine the values of the required resistors, assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting the effect of finite β.

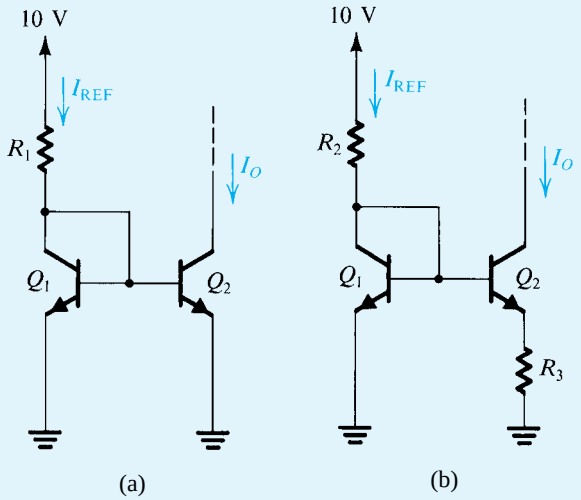


Figure 7.37 Circuits for Example 7.6.

Solution

For the basic current-source circuit in Fig. 7.37(a) we choose a value for R_1 to result in $I_{REF} = 10\ \mu A$. At this current, the voltage drop across Q_1 will be

$$V_{BE1} = 0.7 + V_T \ln\left(\frac{10\ \mu A}{1\ mA}\right) = 0.58\ V$$

Thus,

$$R_1 = \frac{10 - 0.58}{0.01} = 942\ k\Omega$$

For the Widlar circuit in Fig. 7.37(b) we must first decide on a suitable value for I_{REF}. If we select $I_{REF} = 1$ mA, then $V_{BE1} = 0.7$ V and R_2 is given by

$$R_2 = \frac{10 - 0.7}{1} = 9.3\ k\Omega$$

The value of R_3 can be determined using Eq. (7.87) as follows:

$$10 \times 10^{-6} R_3 = 0.025 \ln\left(\frac{1\ mA}{10\ \mu A}\right)$$

$$R_3 = 11.5\ k\Omega$$

From the above example we observe that using the Widlar circuit allows the generation of a small constant current using relatively small resistors. This is an important advantage that results in considerable savings in chip area. In fact the circuit of Fig. 7.37(a), requiring a 942-kΩ resistance, is totally impractical for implementation in IC form because of the very-high value of resistor R_1.

Another important characteristic of the Widlar current source is that its output resistance is high. The increase in the output resistance, above that achieved in the basic current source, is due to the emitter-degeneration resistance R_E. To determine the output resistance of Q_2, we assume that since the base of Q_2 is connected to ground via the small resistance r_e of Q_1, the incremental voltage at the base will be small. Thus we can use the formula in Eq. (7.51) and adapt it for our purposes here as follows:

$$R_{\text{out}} \simeq [1 + g_m(R_E \parallel r_\pi)]r_o \tag{7.88}$$

Thus the output resistance is increased above r_o by a factor that can be significant.

EXERCISE

7.22 Find the output resistance of each of the two current sources designed in Example 7.6. Let $V_A = 100$ V and $\beta = 100$.
Ans. 10 MΩ; 54 MΩ

7.6 Some Useful Transistor Pairings

The cascode configuration studied in Section 7.3 combines CS and CG MOS transistors (CE and CB bipolar transistors) to great advantage. The key to the superior performance of the resulting combination is that the transistor pairing is done in a way that maximizes the advantages and minimizes the shortcomings of each of the two individual configurations. In this section we present a number of other such transistor pairings. In each case the transistor pair can be thought of as a compound device; thus the resulting amplifier may be considered as a single stage.

7.6.1 The CC–CE, CD–CS, and CD–CE Configurations

Figure 7.38(a) shows an amplifier formed by cascading a common-collector (emitter follower) transistor Q_1 with a common-emitter transistor Q_2. This circuit has two main advantages over the CE amplifier. First, the emitter follower increases the input resistance by a factor equal to $(\beta_1 + 1)$. As a result, the overall voltage gain is increased, especially if the resistance of the signal source is large. Second, it will be shown in Chapter 9 that the CC–CE amplifier can exhibit much wider bandwidth than that obtained with the CE amplifier.

The MOS counterpart of the CC–CE amplifier, namely, the CD–CS configuration, is shown in Fig. 7.38(b). Here, since the CS amplifier alone has an infinite input resistance, the sole purpose for adding the source-follower stage is to increase the amplifier bandwidth, as will be seen in Chapter 9. Finally, Fig. 7.38(c) shows the BiCMOS version of this circuit type. Compared to the bipolar circuit in Fig. 7.38(a), the BiCMOS circuit has an infinite input resistance. Compared to the MOS circuit in Fig. 7.38(b), the BiCMOS circuit typically has a higher g_{m2}.

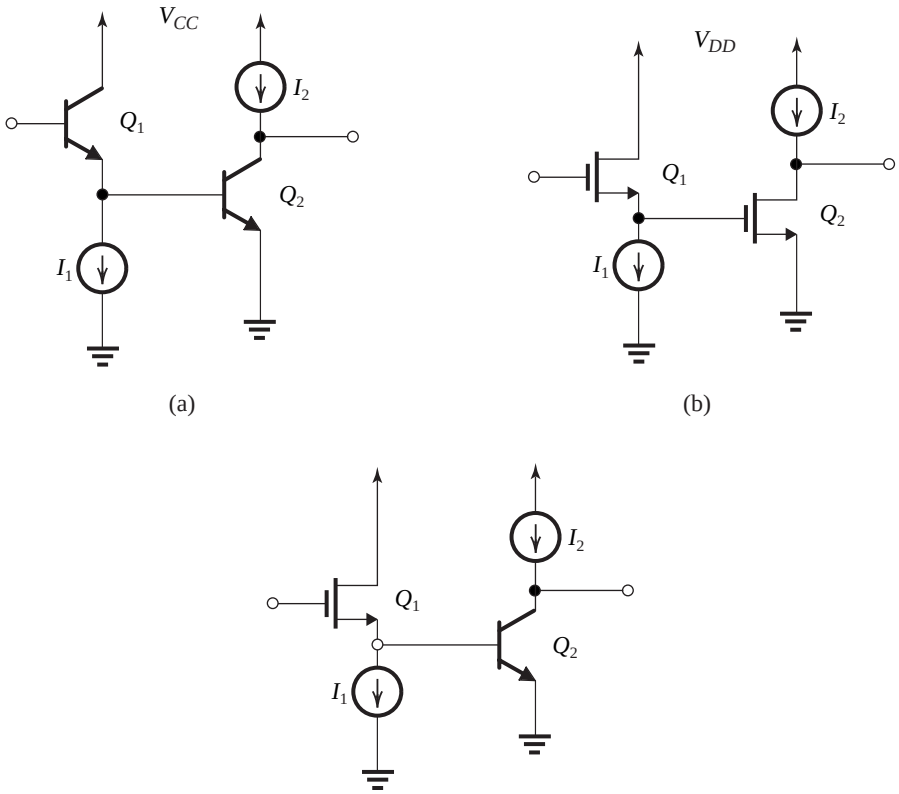


Figure 7.38 (**a**) CC–CE amplifier; (**b**) CD–CS amplifier; (**c**) CD–CE amplifier.

Example 7.7

For the CC–CE amplifier in Fig. 7.38(a) let $I_1 = I_2 = 1$ mA and assume identical transistors with $\beta = 100$. Find the input resistance R_{in} and the overall voltage gain obtained when the amplifier is fed with a signal source having $R_{sig} = 4\ \text{k}\Omega$ and loaded with a resistance $R_L = 4\ \text{k}\Omega$. Compare the results with those obtained with a common-emitter amplifier operating under the same conditions. Ignore r_o.

Solution

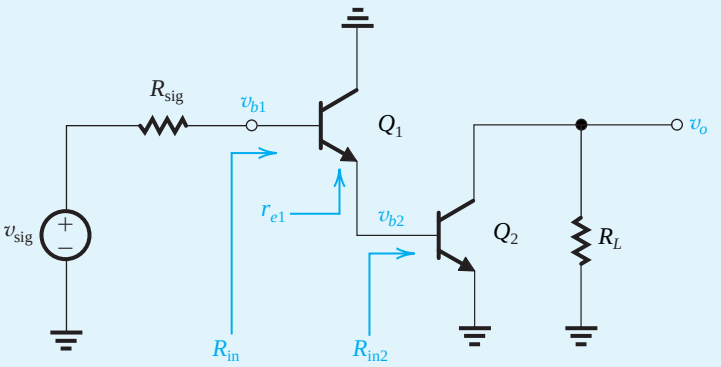
At an emitter current of 1 mA, Q_1 and Q_2 have

$$g_m = 40\ \text{mA/V}$$

$$r_e = 25\ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40} = 2.5\ \text{k}\Omega$$

Example 7.7 *continued*



(c)

Figure 7.39 Circuit for Example 7.7.

Referring to Fig. 7.39 we can find

$$R_{in2} = r_{\pi 2} = 2.5\ \text{k}\Omega$$

$$R_{in} = (\beta_1 + 1)\ (r_{e1} + R_{in2})$$

$$= 101\,(0.025 + 2.5) = 255\ \text{k}\Omega$$

$$\frac{v_{b1}}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{255}{255 + 4} = 0.98\ \text{V/V}$$

$$\frac{v_{b2}}{v_{b1}} = \frac{R_{in2}}{R_{in2} + r_{e1}} = \frac{2.5}{2.5 + 0.025} = 0.99\ \text{V/V}$$

$$\frac{v_o}{v_{b2}} = -g_{m2} R_L = -40 \times 4 = -160\ \text{V/V}$$

Thus,

$$G_v = \frac{v_o}{v_{sig}} = -160 \times 0.99 \times 0.98 = -155\ \text{V/V}$$

For comparison, a CE amplifier operating under the same conditions will have

$$R_{in} = r_\pi = 2.5\ \text{k}\Omega$$

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}}(-g_m R_L)$$

$$= \frac{2.5}{2.5 + 4}(-40 \times 4)$$

$$= -61.5\ \text{V/V}$$

EXERCISE

7.23 Repeat Example 7.7 for the CD–CE configuration of Fig. 7.38(c). Let $I_1 = I_2 = 1$ mA, $\beta_2 = 100$, and $k_{n1} = 8$ mA/V^2; neglect r_o of both transistors. Find R_{in} and G_v when $R_{sig} = 4$ kΩ (as in Example 7.7) and $R_{sig} = 400$ kΩ. What would G_v of the CC–CE amplifier in Example 7.7 become for $R_{sig} = 400$ kΩ?

Ans. $R_{in} = \infty$; $G_v = -145.5$ V/V, independent of R_{sig}; -61.7 V/V

7.6.2 The Darlington Configuration[6]

Figure 7.40(a) shows a popular BJT circuit known as the **Darlington configuration**. It can be thought of as a variation of the CC–CE circuit with the collector of Q_1 connected to that of Q_2. Alternatively, the **Darlington pair** can be thought of as a composite transistor with $\beta = \beta_1\beta_2$. It can therefore be used to implement a high-performance voltage follower, as illustrated in Fig. 7.40(b). Note that in this application the circuit can be considered as the cascade connection of two common-collector transistors (i.e., a CC–CC configuration).

Since the transistor β depends on the dc bias current, it is possible that Q_1 will be operating at a very low β, rendering the β-multiplication effect of the Darlington pair rather ineffective. A simple solution to this problem is to provide a bias current for Q_1, as shown in Fig. 7.40(c).

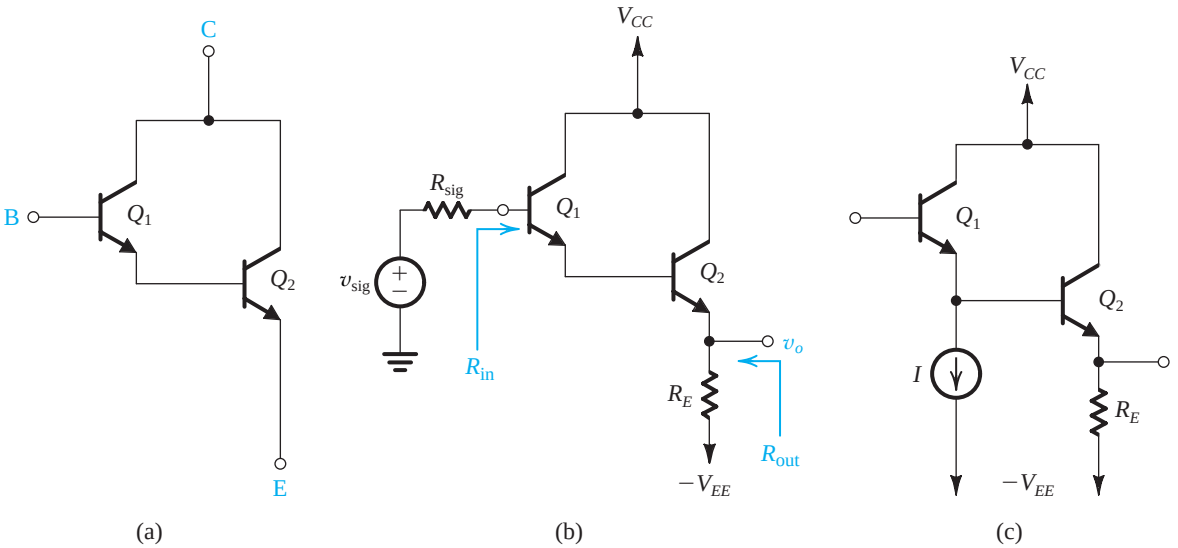


Figure 7.40 **(a)** The Darlington configuration; **(b)** voltage follower using the Darlington configuration; **(c)** the Darlington follower with a bias current I supplied to Q_1 to ensure that its β remains high.

[6]Named after Sidney Darlington, a pioneer in filter design and transistor circuit design.

EXERCISE

7.24 For the Darlington voltage follower in Fig. 7.40(b), show that:

$$R_{\text{in}} = (\beta_1 + 1)[r_{e1} + (\beta_2 + 1)(r_{e2} + R_E)]$$

$$R_{\text{out}} = R_E \| \left[r_{e2} + \frac{r_{e1} + [R_{\text{sig}}/(\beta_1 + 1)]}{\beta_2 + 1} \right]$$

$$\frac{v_o}{v_{\text{sig}}} = \frac{R_E}{R_E + r_{e2} + [r_{e1} + R_{\text{sig}}/(\beta_1 + 1)]/(\beta_2 + 1)}$$

Evaluate R_{in}, R_{out}, and v_o/v_{sig} for the case $I_{E2} = 5$ mA, $\beta_1 = \beta_2 = 100$, $R_E = 1$ kΩ, and $R_{\text{sig}} = 100$ kΩ.

Ans. 10.3 MΩ; 20 Ω; 0.98 V/V

7.6.3 The CC–CB and CD–CG Configurations

Cascading an emitter follower with a common-base amplifier, as shown in Fig. 7.41(a), results in a circuit with a low-frequency gain approximately equal to that of the CB but with the problem of the low input resistance of the CB solved by the buffering action of the CC stage. It will be shown in Chapter 9 that this circuit exhibits wider bandwidth than that obtained with a CE amplifier of the same gain. Note that the biasing current sources shown in Fig. 7.41(a) ensure that each of Q_1 and Q_2 is operating at a bias current I. We are not

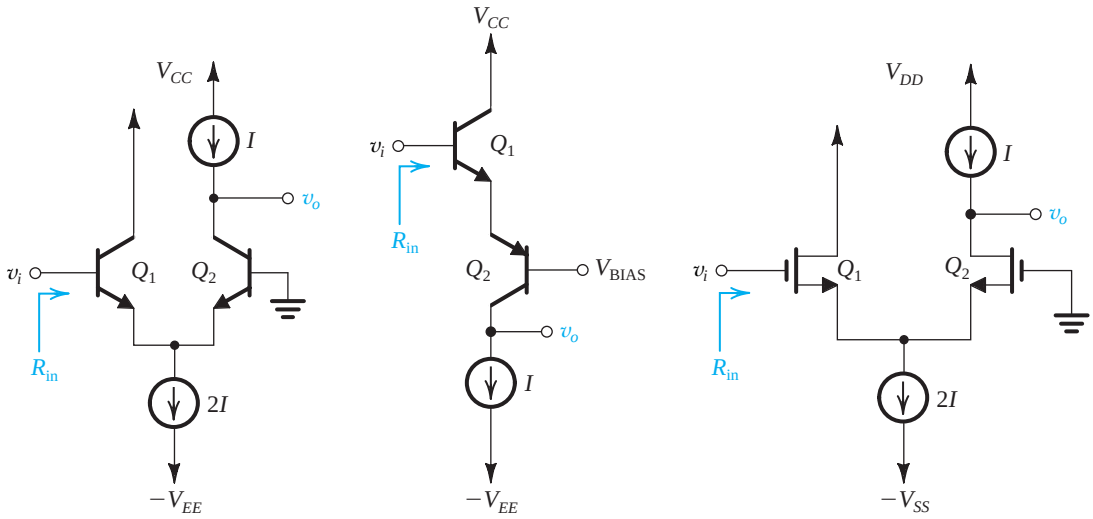


Figure 7.41 **(a)** A CC–CB amplifier. (**b**) Another version of the CC–CB circuit with Q_2 implemented using a *pnp* transistor. (**c**) The MOSFET version of the circuit in (**a**).

showing, however, how the dc voltage at the base of Q_1 is set or the circuit that determines the dc voltage at the collector of Q_2. Both issues are usually looked after in the larger circuit of which the CC–CB amplifier is a part.

An interesting version of the CC–CB configuration is shown in Fig. 7.41(b). Here the CB stage is implemented with a *pnp* transistor. Although only one current source is now needed, observe that we also need to establish an appropriate bias voltage at the base of Q_2. This circuit is part of the internal circuit of the popular 741 op amp, which will be studied in Chapter 12.

The MOSFET version of the circuit in Fig. 7.41(a) is the CD–CG amplifier shown in Fig. 7.41(c).

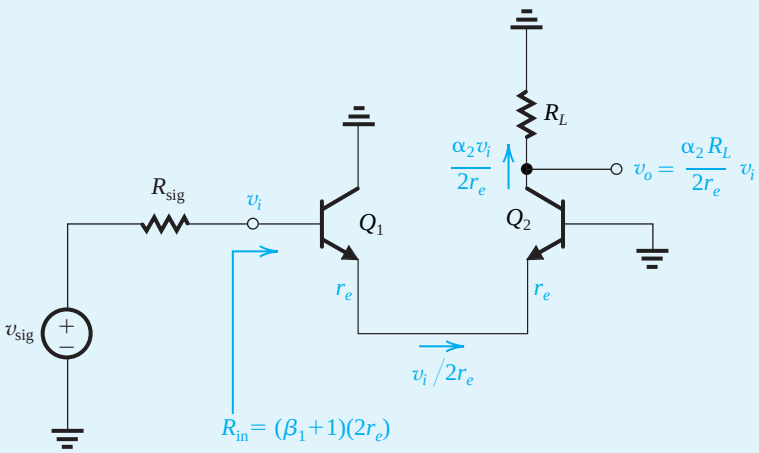
Example 7.8

For the CC–CB amplifiers in Fig. 7.41(a) and (b), find R_{in}, v_o/v_i, and v_o/v_{sig} when each amplifier is fed with a signal source having a resistance R_{sig}, and a load resistance R_L is connected at the output. For simplicity, neglect r_o.

Solution

The analysis of both circuits is illustrated in Fig. 7.42. Observe that both amplifiers have the same R_{in} and v_o/v_i. The overall voltage gain v_o/v_{sig} can be found as

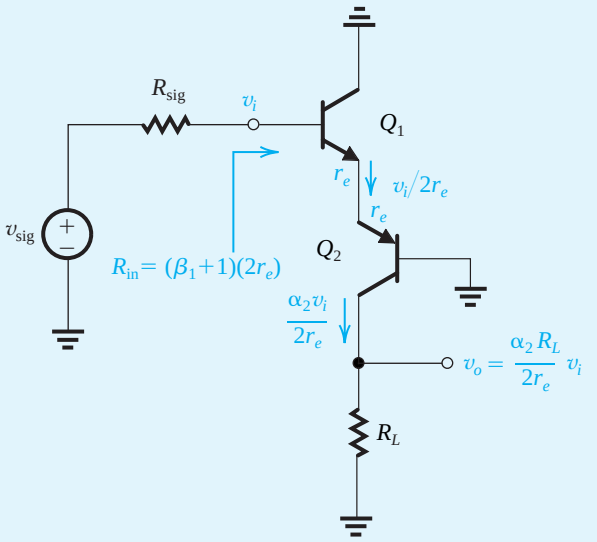
$$\frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} \frac{\alpha_2 R_L}{2r_e}$$



(a)

Figure 7.42 Circuits for Example 7.8. (*continued on following page*)

Example 7.8 *continued*



(b)

Figure 7.42 (*continued*)

EXERCISES

7.25 For the amplifiers in Example 7.8 find R_{in}, v_o/v_i, and v_o/v_{sig} for the case $I = 1$ mA, $\beta = 100$. $R_L = R_{sig} = 5$ kΩ.

Ans. 5.05 kΩ; 100 V/V; 50 V/V

D7.26 (a) Neglecting r_{o1}, show that the voltage gain v_o/v_i of the CD–CG amplifier shown earlier in Fig. 7.4(c) is given by

$$\frac{v_o}{v_i} = \frac{IR_L}{V_{OV}}$$

where R_L is a load resistance connected at the output and V_{OV} is the overdrive voltage at which each of Q_1 and Q_2 is operating.
(b) For $I = 0.1$ mA and $R_L = 20$ kΩ, find W/L for each of Q_1 and Q_2 to obtain a gain of 10 V/V. Assume $k'_n = 200$ μA/V^2.

Ans. (b) $W/L = 25$

Summary

- Integrated-circuit fabrication technology offers the circuit designer many exciting opportunities, the most important of which is the large number of inexpensive small-area MOS transistors. An overriding concern for IC designers, however, is the minimization of chip area or "silicon real estate." As a result, large-valued resistors and capacitors are virtually absent.
- The basic gain cell of IC amplifiers is the CS (CE) amplifier with a current-source load. For an ideal current-source load (i.e., one with infinite output resistance), the transistor operates in an open-circuit fashion and thus provides the maximum gain possible, $A_{vo} = -g_m r_o = -A_0$.
- The intrinsic gain A_0 is given by $A_0 = V_A/V_T$ for a BJT and $A_0 = V_A/(V_{OV}/2)$ for a MOSFET. For a BJT, A_0 is constant independent of bias current and device dimensions. For a MOSFET, A_0 is inversely proportional to $\sqrt{I_D}$ (see Eq. 7.15).
- Simple current-source loads reduce the gain realized in the basic gain cell because of their finite output resistance (usually comparable to the value of r_o of the amplifying transistor).
- To raise the output resistance of the CS or CE transistor, we stack a CG or CB transistor on top. This is cascoding. The CG or CB transistor in the cascode passes the current $g_{m1}v_i$ provided by the CS or CE transistor to the output but increases the resistance at the output from r_{o1} to $(g_{m2}r_{o2})r_{o1}$ in the MOS case [$g_{m2}(r_{o1} \parallel r_{\pi 2})r_{o2}$ in the bipolar case]. The maximum output resistance achieved in the bipolar case is $\beta_2 r_{o2}$.
- A MOS cascode amplifier operating with an ideal current-source load achieves a gain of $(g_m r_o)^2 = A_0^2$.
- To realize the full advantage of cascoding, the load current-source must also be cascoded, in which case a gain as high as $\frac{1}{2}A_0^2$ can be obtained.
- Double cascoding is possible in the MOS case only. However, the large number of transistors in the stack between the power-supply rails results in the disadvantage of a severely limited output-signal swing. The folded-cascode configuration helps resolve this issue.
- A CS amplifier with a resistance R_s in its source lead has an output resistance $R_o \simeq (1 + g_m R_s)r_o$. The corresponding formula for the BJT case is $R_o = [1 + g_m(R_e \parallel r_\pi)]r_o$.
- Biasing in integrated circuits utilizes current sources. As well, current sources are used as load devices. Typically an accurate and stable reference current is generated and then replicated to provide bias currents for the various amplifier stages on the chip. The heart of the current-steering circuitry utilized to perform this function is the current mirror.
- The MOS current mirror has a current transfer ratio of $(W/L)_2/(W/L)_1$. For a bipolar mirror, the ratio is I_{S2}/I_{S1}.
- Bipolar mirrors suffer from the finite β, which reduces the accuracy of the current transfer ratio.
- Both bipolar and MOS mirrors of the basic type have a finite output resistance equal to r_o of the output device. Also, for proper operation, a voltage of at least 0.3 V is required across the output transistor of a simple bipolar mirror ($|V_{OV}|$ for the MOS case).
- Cascoding can be applied to current mirrors to increase their output resistances. An alternative that also solves the β problem in the bipolar case is the Wilson circuit. The MOS Wilson mirror has an output resistance of $(g_m r_o)r_o$, and the BJT version has an output resistance of $\frac{1}{2}\beta r_o$. Both the cascode and Wilson mirrors require at least 1 V or so for proper operation.
- The Widlar current source provides an area-efficient way to implement a low-valued constant-current source that also has a high output resistance.
- Preceding the CE (CS) transistor with an emitter follower (a source follower) results in increased input resistance in the BJT case and wider bandwidth in both the BJT and MOS cases.
- Preceding the CB (CG) transistor with an emitter follower (a source follower) solves the low-input-resistance problem of the CB and CG configurations.
- The Darlington configuration results in an equivalent BJT with a current gain approaching β^2.

Appendix 7.A Comparison of the MOSFET and the BJT

In this appendix we present a comparison of the characteristics of the two major electronic devices: the MOSFET and the BJT. To facilitate this comparison, typical values for the important parameters of the two devices are first presented. We also discuss the design parameters available with each of the two devices, such as I_C in the BJT, and I_D and V_{OV} in the MOSFET, and the trade-offs encountered in deciding on suitable values for these.

7.A.1 Typical Values of MOSFET Parameters

Typical values for the important parameters of NMOS and PMOS transistors fabricated in a number of CMOS processes are shown in Table 7.A.1. Each process is characterized by the minimum allowed channel length, $L_{\min}$; thus, for example, in a 0.18-μm process, the smallest transistor has a channel length $L = 0.18$ μm. The technologies presented in Table 7.A.1 are in descending order of channel length, with that having the shortest channel length being the most modern. Although the 0.8-μm process is now obsolete, its data are included to show trends in the values of various parameters. It should also be mentioned that although Table 7.A.1 stops at the 0.13-μm process, by 2009 there were 90-, 65-, and 45-nm processes available, and processes down to 22 nm were in various stages of development. The 0.18-μm and the 0.13-μm processes, however, remained popular in the design of analog ICs. The most recently announced digital ICs utilize 65-nm and 45-nm processes and pack as many as 2.3 billion transistors onto one chip. An important caution is in order regarding the data presented in Table 7.A.1: These data do *not* pertain to any particular commercially available process. Accordingly, these generic data are not intended for use in an actual IC design; rather, they show trends and, as we shall see, help to illustrate design trade-offs as well as enable us to work out design examples and problems with parameter values that are as realistic as possible.

As indicated in Table 7.A.1, the trend has been to reduce the minimum allowable channel length. This trend has been motivated by the desire to pack more transistors on a chip as well as to operate at higher speeds or, in analog terms, over wider bandwidths.

Observe that the oxide thickness, t_{ox}, scales down with the channel length, reaching 2.7 nm for the 0.13-μm process. (The 65-nm process, not shown in Table 7.A.1, has an oxide thickness of 1.2 nm.) Since the oxide capacitance C_{ox} is inversely proportional to t_{ox},

Table 7.A.1 Typical Values of CMOS Device Parameters

	0.8 μm		0.5 μm		0.25 μm		0.18 μm		0.13 μm	
Parameter	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
t_{ox} (nm)	15	15	9	9	6	6	4	4	2.7	2.7
C_{ox} (fF/μm^2)	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8
μ (cm^2/V·s)	550	250	500	180	460	160	450	100	400	100
μC_{ox} (μA/V^2)	127	58	190	68	267	93	387	86	511	128
V_{t0} (V)	0.7	–0.7	0.7	–0.8	0.5	–0.6	0.5	–0.5	0.4	–0.4
V_{DD} (V)	5	5	3.3	3.3	2.5	2.5	1.8	1.8	1.3	1.3
$\lvert V_A' \rvert$ (V/μm)	25	20	20	10	5	6	5	6	5	6
C_{ov} (fF/μm)	0.2	0.2	0.4	0.4	0.3	0.3	0.37	0.33	0.36	0.33

we see that C_{ox} increases as the technology scales down. The surface mobility μ decreases as the technology minimum-feature size is decreased, and μ_p decreases faster than μ_n. As a result, the ratio of μ_p to μ_n has been decreasing with each generation of technology, falling from about 0.5 for older technologies to 0.2 or so for the newer ones. Despite the reduction of μ_n and μ_p, the transconductance parameters $k_n' = \mu_n C_{ox}$ and $k_p' = \mu_p C_{ox}$ have been steadily increasing. As a result, modern short-channel devices achieve required levels of bias currents at lower overdrive voltages. As well, they achieve higher transconductance, a major advantage.

Although the magnitudes of the threshold voltages V_{tn} and V_{tp} have been decreasing with $L_{\min}$ from about 0.7–0.8 V to 0.3–0.4 V, the reduction has not been as large as that of the power supply V_{DD}. The latter has been reduced dramatically, from 5 V for older technologies to 1.3 V for the 0.13-μm process (and approaching 1 V for the 45-nm process). This reduction has been necessitated by the need to keep the electric fields in the smaller devices from reaching very high values. Another reason for reducing V_{DD} is to keep power dissipation as low as possible given that the IC chip now has a much larger number of transistors.[7]

The fact that in modern short-channel CMOS processes $|V_t|$ has become a much larger proportion of the power-supply voltage poses a serious challenge to the circuit design engineer. Recalling that $|V_{GS}| = |V_t| + |V_{OV}|$, where V_{OV} is the overdrive voltage, to keep $|V_{GS}|$ reasonably small, $|V_{OV}|$ for modern technologies is usually in the range of 0.1 V to 0.2 V. To appreciate this point further, recall that to operate a MOSFET in the saturation region, $|V_{DS}|$ must exceed $|V_{OV}|$; thus, to be able to have a number of devices stacked between the power-supply rails in a regime in which V_{DD} is only 1.8 V or lower, we need to keep $|V_{OV}|$ as low as possible. We will shortly see, however, that operating at a low $|V_{OV}|$ has some drawbacks.

Another significant though undesirable feature of modern deep submicron ($L_{\min} < 0.25$ μm) CMOS technologies is that the channel-length modulation effect is very pronounced. As a result, V_A' has decreased to about 5 V/μm, which combined with the decreasing values of L has caused the Early voltage $V_A = V_A' L$ to become very small. Correspondingly, short-channel MOSFETs exhibit low output resistances.

When we study the MOSFET high-frequency[8] equivalent-circuit model in Section 9.2 and the high-frequency response of the common-source amplifier in Section 9.3, we will learn that two major MOSFET capacitances are C_{gs} and C_{gd}. While C_{gs} has an overlap component,[9] C_{gd} is entirely an overlap capacitance. Both C_{gd} and the overlap component of C_{gs} are almost equal and are denoted C_{ov}. The last line of Table 7.A.1 provides the value of C_{ov} per micron of gate width. Although the normalized C_{ov} has been staying more or less constant with the reduction in $L_{\min}$, we will shortly see that the shorter devices exhibit much higher operating speeds and wider amplifier bandwidths than the longer devices. Specifically, we will, for example, see that f_T for a 0.25-μm NMOS transistor can be as high as 10 GHz.

[7]Chip power dissipation is a very serious issue, with some ICs dissipating as much as 100 W. As a result, an important current area of research concerns what is termed "power-aware design."

[8]For completeness, this appendix includes material on the high-frequency models and operation of both the MOSFET and the BJT. These topics are covered in Chapter 9. The reader can easily skip the appendix paragraphs dealing with these topics until Chapter 9 has been studied.

[9]Overlap capacitances result because the gate electrode overlaps the source and drain diffusions (Fig. 5.1).

7.A.2 Typical Values of IC BJT Parameters

Table 7.A.2 provides typical values for the major parameters that characterize integrated-circuit bipolar transistors. Data are provided for devices fabricated in two different processes: the standard, old process, known as the "high-voltage process," and an advanced, modern process, referred to as a "low-voltage process." For each process we show the parameters of the standard *npn* transistor and those of a special type of *pnp* transistor known as a **lateral *pnp*** (as opposed to **vertical**, as in the *npn* case) (see Appendix A). In this regard we should mention that a major drawback of standard bipolar integrated-circuit fabrication processes has been the lack of *pnp* transistors of a quality equal to that of the *npn* devices. Rather, there are a number of *pnp* implementations for which the lateral *pnp* is the most economical to fabricate. Unfortunately, however, as should be evident from Table 7.A.2, the lateral *pnp* has characteristics that are much inferior to those of the vertical *npn*. Note in particular the lower value of β and the much larger value of the forward transit time τ_F that determines the emitter–base diffusion capacitance C_{de} and, hence, the transistor speed of operation. The data in Table 7.A.2 can be used to show that the unity-gain frequency of the lateral *pnp* is 2 orders of magnitude lower than that of the *npn* transistor fabricated in the same process. Another important difference between the lateral *pnp* and the corresponding *npn* transistor is the value of collector current at which their β values reach their maximums: For the high-voltage process, for example, this current is in the tens of microamperes range for the *pnp* and in the milliampere range for the *npn*. On the positive side, the problem of the lack of high-quality *pnp* transistors has spurred analog circuit designers to come up with highly innovative circuit topologies that either minimize the use of *pnp* transistors or minimize the dependence of circuit performance on that of the *pnp*. We shall encounter some of these ingenious circuits later in this book.

The dramatic reduction in device size achieved in the advanced low-voltage process should be evident from Table 7.A.2. As a result, the scale current I_S also has been reduced by about three orders of magnitude. Here we should note that the base width, W_B, achieved in the advanced process is on the order of 0.1 μm, as compared to a few microns in the standard high-voltage process. Note also the dramatic increase in speed; for the low-voltage *npn* transistor, $\tau_F = 10$ ps as opposed to 0.35 ns in the high-voltage process. As a result, f_T for the modern *npn* transistor is 10 GHz to 25 GHz, as compared to the 400 MHz to 600 MHz achieved in the high-voltage process. Although the Early voltage, V_A, for the modern process is lower than its value in the old high-voltage process, it is still reasonably high at 35 V. Another feature of the advanced process—and one that is not obvious from Table 7.A.2—is that β for the *npn*

Table 7.A.2 Typical Parameter Values for BJTs*

	Standard High-Voltage Process		Advanced Low-Voltage Process	
Parameter	*npn*	Lateral *pnp*	*npn*	Lateral *pnp*
A_E (μm^2)	500	900	2	2
I_S (A)	5×10^{-15}	2×10^{-15}	6×10^{-18}	6×10^{-18}
β_0 (A/A)	200	50	100	50
V_A (V)	130	50	35	30
V_{CEO} (V)	50	60	8	18
τ_F	0.35 ns	30 ns	10 ps	650 ps
C_{je0}	1 pF	0.3 pF	5 fF	14 fF
$C_{\mu 0}$	0.3 pF	1 pF	5 fF	15 fF
r_x (Ω)	200	300	400	200

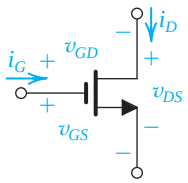
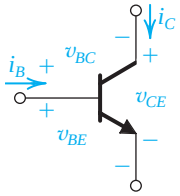
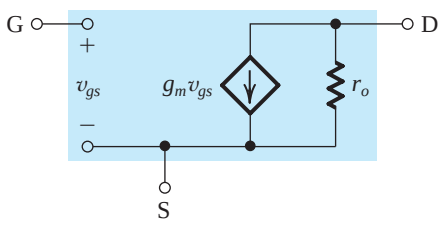
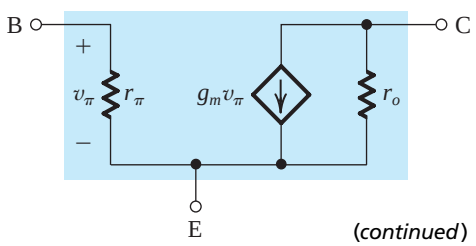
*Adapted from Gray et al. (2001); see Appendix F.

peaks at a collector current of 50 μA or so. Finally, note that as the name implies, *npn* transistors fabricated in the low-voltage process break down at collector–emitter voltages of 8 V, versus 50 V or so for the high-voltage process. Thus, while circuits designed with the standard high-voltage process utilize power supplies of ±15 V (e.g., in commercially available op amps of the 741 type), the total power-supply voltage utilized with modern bipolar devices is 5 V (or even 2.5 V to achieve compatibility with some of the submicron CMOS processes).

7.A.3 Comparison of Important Characteristics

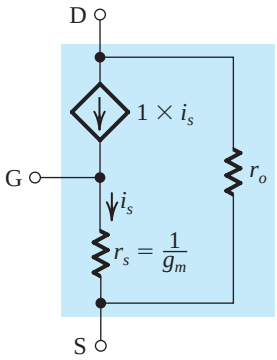
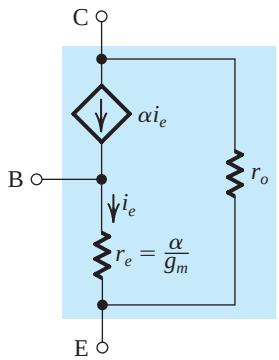
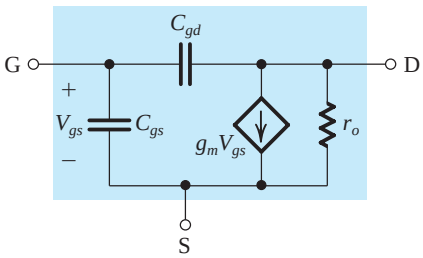
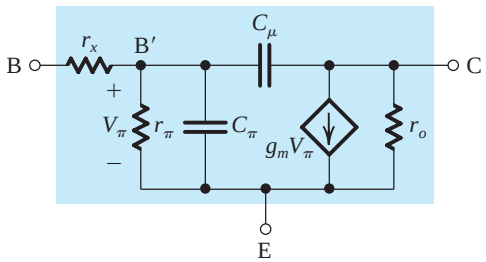
Table 7.A.3 provides a compilation of the important characteristics of the NMOS and the *npn* transistors. The material is presented in a manner that facilitates comparison. In the following, we comment on the various items in Table 7.A.3. As well, a number of numerical examples and exercises are provided to illustrate how the wealth of information in Table 7.A.3 can be put to use. Before proceeding, note that the PMOS and the *pnp* transistors can be compared in a similar way.

Table 7.A.3 Comparison of the MOSFET and the BJT

	NMOS	*npn*
Circuit Symbol		
To Operate in the Active Mode, Two Conditions Have to Be Satisfied	(1) *Induce a channel*: $v_{GS} \geq V_t$, $V_t = 0.3 - 0.5$ V Let $v_{GS} = V_t + v_{OV}$ (2) *Pinch-off channel at drain*: $v_{GD} < V_t$ or equivalently, $v_{DS} \geq V_{OV}$, $V_{OV} = 0.1 - 0.3$ V	(1) *Forward-bias EBJ*: $v_{BE} \geq V_{BEon}$, $V_{BEon} \simeq 0.5$ V (2) *Reverse-bias CBJ*: $v_{BC} < V_{BCon}$, $V_{BCon} \simeq 0.4$ V or equivalently, $v_{CE} \geq 0.3$ V
Current–Voltage Characteristics in the Active Region	$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2\left(1 + \frac{v_{DS}}{V_A}\right)$ $= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2\left(1 + \frac{v_{DS}}{V_A}\right)$ $i_G = 0$	$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$ $i_B = i_C/\beta$
Low-Frequency, Hybrid-π Model		

(*continued*)

Table 7.A.3 *continued*

	NMOS	*npn*
Low-Frequency T Model		
Transconductance g_m	$g_m = I_D/(V_{OV}/2)$ $g_m = (\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}$ $g_m = \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right)I_D}$	$g_m = I_C/V_T$
Output Resistance r_o	$r_o = V_A/I_D = \frac{V_A' L}{I_D}$	$r_o = V_A/I_C$
Intrinsic Gain $A_0 \equiv g_m r_o$	$A_0 = V_A/(V_{OV}/2)$ $A_0 = \frac{2V_A' L}{V_{OV}}$ $A_0 = \frac{V_A'\sqrt{2\mu_n C_{ox} WL}}{\sqrt{I_D}}$	$A_0 = V_A/V_T$
Input Resistance with Source (Emitter) Grounded	∞	$r_\pi = \beta/g_m$
High-Frequency Model		

(*continued*)

Table 7.A.3 *continued*

	NMOS	*npn*
Capacitances	$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$ $C_{gd} = WL_{ov}C_{ox}$	$C_\pi = C_{de} + C_{je}$ $C_{de} = \tau_F g_m$ $C_{je} \simeq 2C_{je0}$ $C_\mu = C_{\mu 0} \Big/ \left[1 + \frac{V_{CB}}{V_{C0}}\right]^m$
Transition Frequency f_T	$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$ For $C_{gs} \gg C_{gd}$ and $C_{gs} \simeq \frac{2}{3}WLC_{ox}$, $f_T \simeq \frac{1.5\mu_n V_{OV}}{2\pi L^2}$	$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$ For $C_\pi \gg C_\mu$ and $C_\pi \simeq C_{de}$, $f_T \simeq \frac{2\mu_n V_T}{2\pi W_B^2}$
Design Parameters	I_D, V_{OV}, L, $\frac{W}{L}$	I_C, V_{BE}, A_E(or I_S)
Good Analog Switch?	Yes, because the device is symmetrical and thus the i_D–v_{DS} characteristics pass directly through the origin.	No, because the device is asymmetrical with an offset voltage V_{CEoff}.

Operating Conditions At the outset, note that we shall use **active mode** or **active region** to denote both the active mode of operation of the BJT and the saturation mode of operation of the MOSFET.

The conditions for operating in the active mode are very similar for the two devices: The explicit threshold V_t of the MOSFET has $V_{BE\text{on}}$ as its implicit counterpart in the BJT. Furthermore, for modern processes, $V_{BE\text{on}}$ and V_t are almost equal.

Also, pinching off the channel of the MOSFET at the drain end is very similar to reverse biasing the CBJ of the BJT; the first makes i_D nearly independent of v_D, and the second makes I_C nearly independent of v_C. Note, however, that the asymmetry of the BJT results in $V_{BC\text{on}}$ and $V_{BE\text{on}}$ being unequal, while in the symmetrical MOSFET the operative threshold voltages at the source and the drain ends of the channel are identical (V_t). Finally, for both the MOSFET and the BJT to operate in the active mode, the voltage across the device $(v_{DS},\ v_{CE})$ must be at least 0.1 V to 0.3 V.

Current–Voltage Characteristics The square-law control characteristic, i_D–v_{GS}, in the MOSFET should be contrasted with the exponential control characteristic, i_C–v_{BE}, of the BJT. Obviously, the latter is a much more sensitive relationship, with the result that i_C can vary over a very wide range (five decades or more) within the same BJT. In the MOSFET, the range of i_D achieved in the same device is much more limited. To appreciate this point further, consider the parabolic relationship between i_D and v_{OV}, and recall from our discussion above that v_{OV} is usually kept in a narrow range (0.1 V to 0.3 V).

Next we consider the effect of the device dimensions on its current. For the bipolar transistor, the control parameter is the area of the emitter–base junction (EBJ), A_E, which determines the scale current I_S. It can be varied over a relatively narrow range, such as 10 to 1. Thus, while the emitter area can be used to achieve current scaling in an IC (as we can see in Section 7.4 in connection with the design of current mirrors), its narrow range of variation reduces its significance as a design parameter. This is particularly so if we compare A_E with its counterpart in the MOSFET, the aspect ratio *W/L*. MOSFET devices can be designed with *W/L* ratios in a wide range, such as 1.0 to 500. As a result, *W/L* is a very significant MOS

design parameter. Like A_E, it is also used in current scaling, as we can see in Section 7.4. Combining the possible range of variation of v_{OV} and W/L, one can design MOS transistors to operate over an i_D range of four decades or so.

The channel-length modulation in the MOSFET and the base-width modulation in the BJT are similarly modeled and give rise to the dependence of i_D (i_C) on v_{DS} (v_{CE}) and, hence, to the finite output resistance r_o in the active region. Two important differences, however, exist. In the BJT, V_A is solely a process-technology parameter and does not depend on the dimensions of the BJT. In the MOSFET, the situation is quite different: $V_A = V_A' L$, where V_A' is a process-technology parameter and L is the channel length used. Also, in modern deep submicron processes, V_A' is very low, resulting in V_A values that are lower than the corresponding values for the BJT.

The last, and perhaps most important, difference between the current–voltage characteristics of the two devices concerns the input current into the control terminal: While at low frequencies the gate current of the MOSFET is practically zero and the input resistance looking into the gate is practically infinite, the BJT draws base current i_B that is proportional to the collector current; that is, $i_B = i_C/\beta$. The finite base current and the corresponding finite input resistance looking into the base comprise a definite disadvantage of the BJT in comparison to the MOSFET. Indeed, it is the infinite input resistance of the MOSFET that has made possible analog and digital circuit applications that are not feasible with the BJT. Examples include dynamic digital memory (Chapter 15) and switched-capacitor filters (Chapter 16).

Example 7.A.1

(a) For an NMOS transistor with $W/L = 10$ fabricated in the 0.18-μm process whose data are given in Table 7.A.1, find the values of V_{OV} and V_{GS} required to operate the device at $I_D = 100$ μA. Ignore channel-length modulation.

(b) Find V_{BE} for an *npn* transistor fabricated in the low-voltage process specified in Table 7.A.2 and operated at $I_C = 100$ μA. Ignore base-width modulation.

Solution

(a) $$I_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}^2$$

Substituting $I_D = 100$ μA, $W/L = 10$, and, from Table 7.A.1, $\mu_n C_{ox} = 387$ μA/V^2 results in

$$100 = \frac{1}{2} \times 387 \times 10 \times V_{OV}^2$$
$$V_{OV} = 0.23 \text{ V}$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.23 = 0.73 \text{ V}$$

(b) $$I_C = I_S e^{V_{BE}/V_T}$$

Substituting $I_C = 100$ μA and, from Table7.A.2, $I_S = 6 \times 10^{-18}$ A gives,

$$V_{BE} = 0.025 \ln \frac{100 \times 10^{-6}}{6 \times 10^{-18}} = 0.76 \text{ V}$$

EXERCISE

7.A.1 (a) For NMOS transistors fabricated in the 0.18-μm technology specified in Table 7.A.1, find the range of I_D obtained for V_{OV} ranging from 0.2 V to 0.4 V and $W/L = 0.1$ to 100. Neglect channel-length modulation.
(b) If a similar range of current is required in an *npn* transistor fabricated in the low-voltage process specified in Table 7.A.2, find the corresponding change in its V_{BE}.
Ans. (a) $I_{D\text{min}} = 0.8$ μA and $I_{D\text{max}} = 3.1$ mA for a range of about 4000:1; (b) for I_C varying over a 4000:1 range, $\Delta V_{BE} = 207$ mV

Low-Frequency Small-Signal Models The low-frequency models for the two devices are very similar except, of course, for the finite base current (finite β) of the BJT, which gives rise to r_π in the hybrid-π model and to the unequal emitter and collector currents in the T models ($\alpha < 1$). Here it is interesting to note that the low-frequency, small-signal models become identical if one thinks of the MOSFET as a BJT with $\beta = \infty$ ($\alpha = 1$).

For both devices, the hybrid-π model indicates that the **open-circuit voltage gain** obtained from gate to drain (base to collector) with the source (emitter) grounded is $-g_m r_o$. It follows that $g_m r_o$ is the *maximum gain available from a single transistor* of either type. This important transistor parameter is given the name **intrinsic gain** and is denoted A_0. We will have more to say about the intrinsic gain shortly.

Although not included in the MOSFET low-frequency model shown in Table 7.A.3, the body effect can have some implications for the operation of the MOSFET as an amplifier. In simple terms, if the body (substrate) is not connected to the source, it can act as a second gate for the MOSFET. The voltage signal that develops between the body and the source, v_{bs}, gives rise to a drain current component $g_{mb}v_{bs}$, where the body transconductance g_{mb} is proportional to g_m; that is, $g_{mb} = \chi g_m$, where the factor χ is in the range of 0.1 to 0.2. The body effect has no counterpart in the BJT.

The Transconductance For the BJT, the transconductance g_m depends *only* on the dc collector current I_C. (Recall that V_T is a physical constant $\simeq 0.025$ V at room temperature.) It is interesting to observe that g_m does not depend on the geometry of the BJT, and its dependence on the EBJ area is only through the effect of the area on the total collector current I_C. Similarly, the dependence of g_m on V_{BE} is only through the fact that V_{BE} determines the total current in the collector. By contrast, g_m of the MOSFET depends on I_D, V_{OV}, and W/L. Therefore, we use three different (but equivalent) formulas to express g_m of the MOSFET.

The first formula given in Table 7.A.3 for the MOSFET's g_m is the most directly comparable with the formula for the BJT. It indicates that for the same operating current, g_m of the MOSFET is smaller than that of the BJT. This is because $V_{OV}/2$ is the range of 0.05 V to 0.15 V, which is two to six times the corresponding term in the BJT's formula, namely V_T.

The second formula for the MOSFET's g_m indicates that for a given device (i.e., given W/L), g_m is proportional to V_{OV}. Thus a higher g_m is obtained by operating the MOSFET at a higher overdrive voltage. However, we should recall the limitations imposed on the magnitude of V_{OV} by the limited value of V_{DD}. Put differently, the need to obtain a reasonably high g_m constrains the designer's interest in reducing V_{OV}.

The third g_m formula shows that for a given transistor (i.e., given W/L), g_m is proportional to $\sqrt{I_D}$. This should be contrasted with the bipolar case, where g_m is directly proportional to I_C.

Output Resistance The output resistance for both devices is determined by similar formulas, with r_o being the ratio of V_A to the bias current (I_D or I_C). Thus, for both transistors,

r_o is inversely proportional to the bias current. The difference in nature and magnitude of V_A between the two devices has already been discussed.

Intrinsic Gain The intrinsic gain A_0 of the BJT is the ratio of V_A, which is solely a process parameter (5 V to 100 V), and V_T, which is a physical parameter (0.025 V at room temperature). Thus A_0 of a BJT is independent of the device junction area and of the operating current, and its value ranges from 200 V/V to 5000 V/V. The situation in the MOSFET is very different: Table 7.A.3 provides three different (but equivalent) formulas for expressing the MOSFET's intrinsic gain. The first formula is the one most directly comparable to that of the BJT. Here, however, we note the following:

1. The quantity in the denominator is $V_{OV}/2$, which is a design parameter, and although it is becoming smaller in designs using short-channel technologies, it is still at least two to four times larger than V_T. Furthermore, as we have seen, there are reasons for selecting larger values for V_{OV}.
2. The numerator quantity V_A is both process- and device-dependent, and its value has been steadily decreasing.

As a result, the intrinsic gain realized in a single MOSFET amplifier stage fabricated in a modern short-channel technology is only 20 V/V to 40 V/V, at least an order of magnitude lower than that for a BJT.

The third formula given for A_0 in Table 7.A.3 points out a very interesting fact: For a given process technology (V_A' and $\mu_n C_{ox}$) and a given device (W/L), the intrinsic gain is inversely proportional to $\sqrt{I_D}$. This is illustrated in Fig. 7.A.1, which shows a typical plot of A_0 versus the bias current I_D. The plot confirms that the gain increases as the bias current is lowered. The gain, however, levels off at very low currents. This is because the MOSFET enters the subthreshold region of operation (Section 5.1.9), where it becomes very much like a BJT with an exponential current–voltage characteristic. The intrinsic gain then becomes constant, just like that of a BJT. Note, however, that although a higher gain is achieved at lower bias currents, the price paid is a lower g_m and less ability to drive capacitive loads and thus a decrease in bandwidth. This point will be further illustrated shortly.

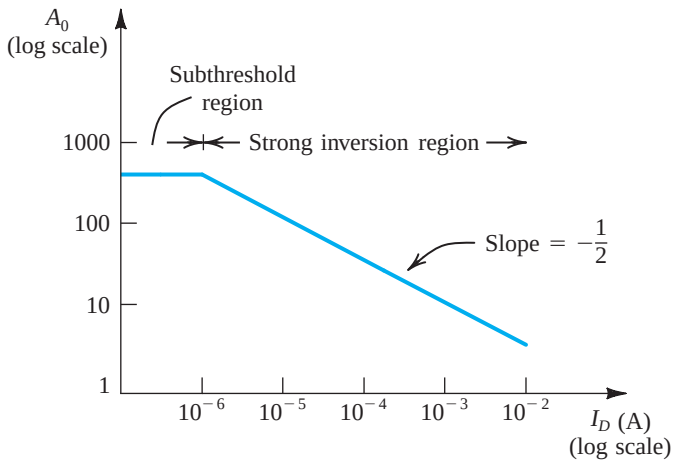


Figure 7.A.1 The intrinsic gain of the MOSFET versus bias current I_D. Outside the subthreshold region, this is a plot of $A_0 = V_A' \sqrt{2\mu_n C_{ox} WL/I_D}$ for the case: $\mu_n C_{ox} = 20$ μA/V², $V_A' = 20$ V/μm, $L = 2$ μm, and $W = 20$ μm.

Example 7.A.2

We wish to compare the values of g_m, input resistance at the gate (base), r_o, and A_0 for an NMOS transistor fabricated in the 0.25-μm technology specified in Table 7.A.1 and an *npn* transistor fabricated in the low-voltage technology specified in Table 7.A.2. Assume both devices are operating at a drain (collector) current of 100 μA. For the MOSFET, let $L = 0.4$ μm and $W = 4$ μm, and specify the required V_{OV}.

Solution

For the NMOS transistor,

$$I_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}^2$$

$$100 = \frac{1}{2} \times 267 \times \frac{4}{0.4} \times V_{OV}^2$$

Thus,

$$V_{OV} = 0.27 \text{ V}$$

$$g_m = \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right)I_D}$$

$$= \sqrt{2 \times 267 \times 10 \times 100} = 0.73 \text{ mA/V}$$

$$R_{\text{in}} = \infty$$

$$r_o = \frac{V_A' L}{I_D} = \frac{5 \times 0.4}{0.1} = 20 \text{ k}\Omega$$

$$A_0 = g_m r_o = 0.73 \times 20 = 14.6 \text{ V/V}$$

For the *npn* transistor,

$$g_m = \frac{I_C}{V_T} = \frac{0.1 \text{ mA}}{0.025 \text{ V}} = 4 \text{ mA/V}$$

$$R_{\text{in}} = r_\pi = \beta_0 / g_m = \frac{100}{4 \text{ mA/V}} = 25 \text{ k}\Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{35}{0.1 \text{ mA}} = 350 \text{ k}\Omega$$

$$A_0 = g_m r_o = 4 \times 350 = 1400 \text{ V/V}$$

EXERCISE

7.A.2 For an NMOS transistor fabricated in the 0.5-μm process specified in Table 7.A.1 with $L = 0.5$ μm, find the transconductance and the intrinsic gain obtained at $I_D = 10$ μA, 100 μA, and 1 mA.
Ans. 0.2 mA/V, 200 V/V; 0.6 mA/V, 62 V/V; 2 mA/V, 20 V/V

High-Frequency Operation The simplified high-frequency equivalent circuits for the MOSFET and the BJT are very similar, and so are the formulas for determining their unity-gain frequency (also called **transition frequency**) f_T. As we shall demonstrate in Chapter 9, f_T is a measure of the *intrinsic* bandwidth of the transistor itself and does *not* take into account the effects of capacitive loads. We address the issue of capacitive loads shortly. For the time being, note the striking similarity between the approximate formulas given in Table 7.A.3 for the value of f_T of the two devices. In both cases f_T is inversely proportional to the square of the critical dimension of the device: the channel length for the MOSFET and the base width for the BJT. These formulas also clearly indicate that shorter-channel MOSFETs[10] and narrower-base BJTs are inherently capable of a wider bandwidth of operation. It is also important to note that while for the BJT the approximate expression for f_T indicates that it is entirely process determined, the corresponding expression for the MOSFET shows that f_T is proportional to the overdrive voltage V_{OV}. Thus we have conflicting requirements on V_{OV}: While a higher low-frequency gain is achieved by operating at a low V_{OV}, wider bandwidth requires an increase in V_{OV}. Therefore the selection of a value for V_{OV} involves, among other considerations, a trade-off between gain and bandwidth.

For *npn* transistors fabricated in the modern low-voltage process, f_T is in the range of 10 GHz to 20 GHz as compared to the 400 MHz to 600 MHz obtained with the standard high-voltage process. In the MOS case, NMOS transistors fabricated in a modern submicron technology, such as the 0.18-μm process, achieve f_T values in the range of 5 GHz to 15 GHz.

Before leaving the subject of high-frequency operation, let's look into the effect of a capacitive load on the bandwidth of the common-source (common-emitter) amplifier. For this purpose we shall assume that the frequencies of interest are much lower than f_T of the transistor. Hence we shall not take the transistor capacitances into account. Figure 7.A.2(a) shows a common-source amplifier with a capacitive load C_L. The voltage gain from gate to drain can be found as follows:

$$V_o = -g_m V_{gs}(r_o \parallel C_L)$$

$$= -g_m V_{gs} \frac{r_o \frac{1}{sC_L}}{r_o + \frac{1}{sC_L}}$$

$$A_v = \frac{V_o}{V_{gs}} = -\frac{g_m r_o}{1 + sC_L r_o} \tag{7.A.1}$$

Thus the gain has, as expected, a low-frequency value of $g_m r_o = A_0$ and a frequency response of the single-time-constant (STC) low-pass type with a break (pole) frequency at

$$\omega_P = \frac{1}{C_L r_o} \tag{7.A.2}$$

Obviously this pole is formed by r_o and C_L. A sketch of the magnitude of gain versus frequency is shown in Fig. 7.A.2(b). We observe that the gain crosses the 0-dB line at frequency ω_t,

$$\omega_t = A_0 \omega_P = (g_m r_o)\frac{1}{C_L r_o}$$

[10] Although the reason is beyond our capabilities at this stage, f_T of MOSFETs that have very short channels varies inversely with L rather than with L^2.

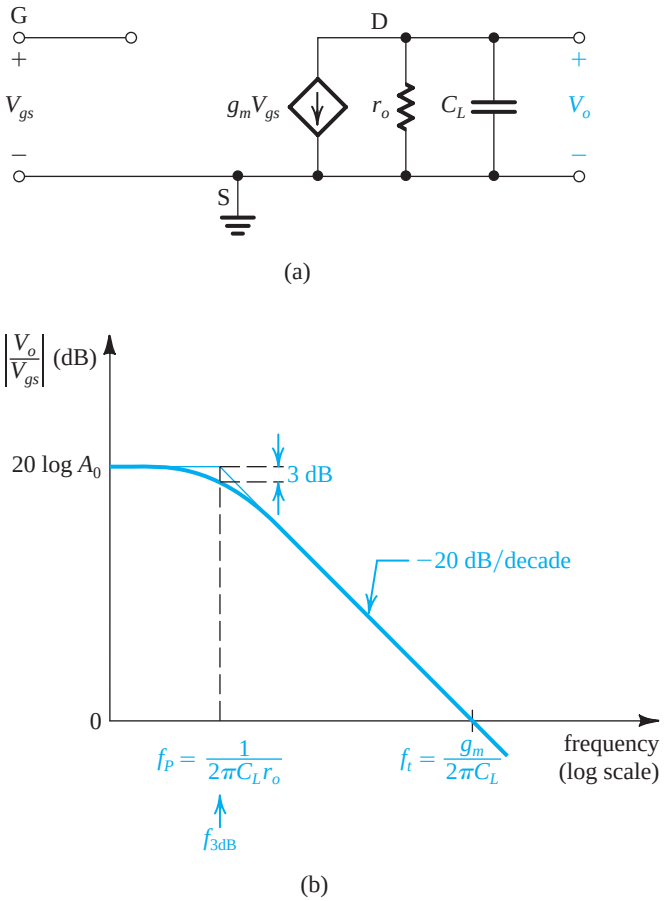


Figure 7.A.2 Frequency response of a CS amplifier loaded with a capacitance C_L and fed with an ideal voltage source. It is assumed that the transistor is operating at frequencies much lower than f_T, and thus the internal capacitances are not taken into account.

Thus,

$$\omega_t = \frac{g_m}{C_L} \tag{7.A.3}$$

That is, the **unity-gain frequency** or, equivalently, the **gain–bandwidth product**[11] ω_t is the ratio of g_m and C_L. We thus clearly see that for a given capacitive load C_L, a larger gain–bandwidth product is achieved by operating the MOSFET at a higher g_m. Identical analysis and conclusions apply to the case of the BJT. In each case, bandwidth increases as bias current is increased.

Design Parameters For the BJT there are three design parameters—I_C, V_{BE}, and I_S (or, equivalently, the area of the emitter–base junction)—and the designer can select any two. However, since I_C is exponentially related to V_{BE} and is very sensitive to the

[11]The unity-gain frequency and the gain–bandwidth product of an amplifier are the same when the frequency response is of the single-pole type; otherwise the two parameters may differ.

value of V_{BE} (V_{BE} changes by only 60 mV for a factor of 10 change in I_C), I_C is much more useful than V_{BE} as a design parameter. As mentioned earlier, the utility of the EBJ area as a design parameter is rather limited because of the narrow range over which A_E can vary. It follows that for the BJT there is only one effective design parameter: the collector current I_C. Finally, note that we have not considered V_{CE} to be a design parameter, since its effect on I_C is only secondary. Of course, as we learned in Chapter 6, V_{CE} affects the output-signal swing.

For the MOSFET there are four design parameters—I_D, V_{OV}, L, and W—and the designer can select any three. For analog circuit applications the trade-off in selecting a value for L is between the higher speed of operation (wider amplifier bandwidth) obtained at lower values of L and the higher intrinsic gain obtained at larger values of L. Usually one selects an L of about 25% to 50% greater than L_{min}.

The second design parameter is V_{OV}. We have already made numerous remarks about the effect of the value of V_{OV} on performance. Usually, for submicron technologies, V_{OV} is selected in the range of 0.1 V to 0.3 V.

Once values for L and V_{OV} have been selected, the designer is left with the selection of the value of I_D or W (or, equivalently, W/L). For a given process and for the selected values of L and V_{OV}, I_D is proportional to W/L. It is important to note that the choice of I_D or, equivalently, of W/L has no bearing on the value of intrinsic gain A_0 and the transition frequency f_T. However, it affects the value of g_m and hence the gain–bandwidth product. Figure 7.A.3 illustrates this point by showing how the gain of a common-source amplifier operated at a constant V_{OV} varies with I_D (or, equivalently, W/L). Note that while the dc gain remains unchanged, increasing W/L and, correspondingly, I_D, increases the bandwidth proportionally. This, however, assumes that the load capacitance C_L is not affected by the device size, an assumption that may not be entirely justified in some cases.

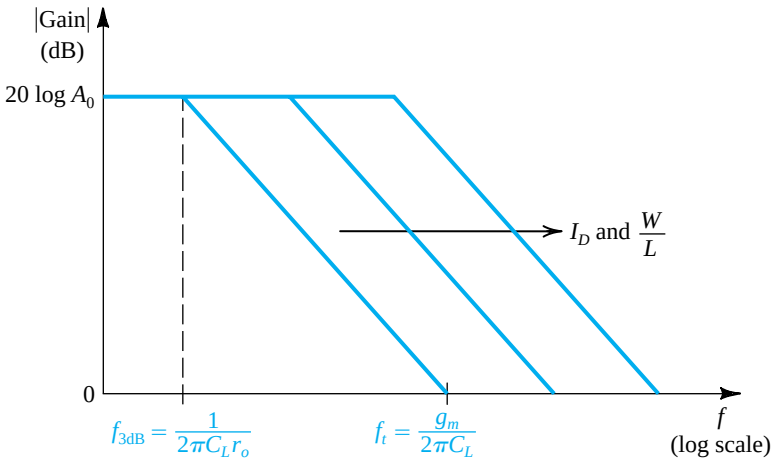


Figure 7.A.3 Increasing I_D or W/L increases the bandwidth of a MOSFET amplifier operated at a constant V_{OV} and loaded by a constant capacitance C_L.

Example 7.A.3

In this example we investigate the gain and the high-frequency response of an *npn* transistor and an NMOS transistor. For the *npn* transistor, assume that it is fabricated in the low-voltage process specified in Table 7.A.2, and assume that $C_\mu \simeq C_{\mu 0}$. For $I_C = 10$ μA, 100 μA, and 1 mA, find g_m, r_o, A_0, C_{de}, C_{je}, C_π, C_μ, and f_T. Also, for each value of I_C, find the gain–bandwidth product f_t of a common-emitter amplifier loaded by a 1-pF capacitance, neglecting the internal capacitances of the transistor. For the NMOS transistor, assume that it is fabricated in the 0.25-μm CMOS process with $L = 0.4$ μm. Let the transistor be operated at $V_{OV} = 0.25$ V. Find W/L that is required to obtain $I_D = 10$ μA, 100 μA, and 1 mA. At each value of I_D, find g_m, r_o, A_0, C_{gs}, C_{gd}, and f_T. Also, for each value of I_D, determine the gain–bandwidth product f_t of a common-source amplifier loaded by a 1-pF capacitance, neglecting the internal capacitances of the transistor.

Solution

For the *npn* transistor,

$$g_m = \frac{I_C}{V_T} = \frac{I_C}{0.025} = 40 I_C \text{ A/V}$$

$$r_o = \frac{V_A}{I_C} = \frac{35}{I_C} \ \Omega$$

$$A_0 = \frac{V_A}{V_T} = \frac{35}{0.025} = 1400 \text{ V/V}$$

$$C_{de} = \tau_F g_m = 10 \times 10^{-12} \times 40 I_C = 0.4 \times 10^{-9} I_C \text{ F}$$

$$C_{je} \simeq 2 C_{je0} = 10 \text{ fF}$$

$$C_\pi = C_{de} + C_{je}$$

$$C_\mu \simeq C_{\mu 0} = 5 \text{ fF}$$

$$f_T = \frac{g_m}{2\pi (C_\pi + C_\mu)}$$

$$f_t = \frac{g_m}{2\pi C_L} = \frac{g_m}{2\pi \times 1 \times 10^{-12}}$$

We thus obtain the following results:

I_C	g_m (mA/V)	r_o (kΩ)	A_0 (V/V)	C_{de} (f F)	C_{je} (f F)	C_π (f F)	C_μ (f F)	f_T (GHz)	f_t (MHz)
10 μA	0.4	3500	1400	4	10	14	5	3.4	64
100 μA	4	350	1400	40	10	50	5	11.6	640
1 mA	40	35	1400	400	10	410	5	15.3	6400

For the NMOS transistor,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

$$= \frac{1}{2} \times 267 \times \frac{W}{L} \times \frac{1}{16}$$

Example 7.A.3 *continued*

Thus,

$$\frac{W}{L} = 0.12 I_D$$

$$g_m = \frac{I_D}{V_{OV}/2} = \frac{I_D}{0.25/2} = 8 I_D \text{ A/V}$$

$$r_o = \frac{V_A' L}{I_D} = \frac{5 \times 0.4}{I_D} = \frac{2}{I_D}\ \Omega$$

$$A_0 = g_m r_o = 16 \text{ V/V}$$

$$C_{gs} = \tfrac{2}{3} W L C_{ox} + C_{ov} = \tfrac{2}{3} W \times 0.4 \times 5.8 + 0.6 W$$

$$C_{gd} = C_{ov} = 0.6 W$$

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

$$f_t = \frac{g_m}{2\pi C_L}$$

We thus obtain the following results:

I_D	W/L	g_m (mA/V)	r_o (kΩ)	A_0 (V/V)	C_{gs} (fF)	C_{gd} (fF)	f_T (GHz)	f_t (MHz)
10 μA	1.2	0.08	200	16	1.03	0.29	9.7	12.7
100 μA	12	0.8	20	16	10.3	2.9	9.7	127
1 mA	120	8	2	16	103	29	9.7	1270

EXERCISE

7.A.3 Find I_D, g_m, r_o, A_0, C_{gs}, C_{gd}, and f_T for an NMOS transistor fabricated in the 0.5-μm CMOS technology specified in Table 7.A.1. Let $L = 0.5$ μm, $W = 5$ μm, and $V_{OV} = 0.3$ V.
Ans. 85.5 μA; 0.57 mA/V; 66.7 kΩ; 38 V/V; 8.3 fF; 2 fF; 8.8 GHz

7.A.4 Combining MOS and Bipolar Transistors—BiCMOS Circuits

From the discussion above it should be evident that the BJT has the advantage over the MOSFET of a much higher transconductance (g_m) at the same value of dc bias current. Thus, in addition to realizing higher voltage gains per amplifier stage, bipolar transistor amplifiers have superior high-frequency performance compared to their MOS counterparts.

On the other hand, the practically infinite input resistance at the gate of a MOSFET makes it possible to design amplifiers with extremely high input resistances and an almost zero input bias current. Also, as mentioned earlier, the MOSFET provides an excellent

implementation of a switch, a fact that has made CMOS technology capable of realizing a host of analog circuit functions that are not possible with bipolar transistors.

It can thus be seen that each of the two transistor types has its own distinct and unique advantages: Bipolar technology has been extremely useful in the design of very-high-quality general-purpose circuit building blocks, such as op amps. On the other hand, CMOS, with its very high packing density and its suitability for both digital and analog circuits, has become the technology of choice for the implementation of very-large-scale integrated circuits. Nevertheless, the performance of CMOS circuits can be improved if the designer has available (on the same chip) bipolar transistors that can be employed in functions that require their high g_m and excellent current-driving capability. A technology that allows the fabrication of high-quality bipolar transistors on the same chip as CMOS circuits is aptly called **BiCMOS**. At appropriate locations throughout this book we present interesting and useful BiCMOS circuit blocks.

7.A.5 Validity of the Square-Law MOSFET Model

We conclude this appendix with a comment on the validity of the simple square-law model we have been using to describe the operation of the MOS transistor. While this simple model works well for devices with relatively long channels (>1 μm), it does *not* provide an accurate representation of the operation of short-channel devices. This is because a number of physical phenomena come into play in these submicron devices, resulting in what are called **short-channel effects**. Although a detailed study of short-channel effects is beyond the scope of this book, it should be mentioned that MOSFET models have been developed that take these effects into account. However, they are understandably quite complex and do not lend themselves to hand analysis of the type needed to develop insight into circuit operation. Rather, these models are suitable for computer simulation and are indeed used in SPICE (Appendix B). For quick, manual analysis, however, we will continue to use the square-law model, which is the basis for the comparison of Table 7.A.3.

PROBLEMS

Computer Simulation Problems

SIM Problems identified by this icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multism simulations for all the indicated problems can be found in the corresponding files on the disc. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

* difficult problem; ** more difficult; *** very challenging and/or time-consuming; D: design problem.

Section 7.2: The Basic Gain Cell

7.1 Find g_m, r_π, r_o, and A_0 for the CE amplifier of Fig. 7.1(b) when operated at $I = 10$ μA, 100 μA, and 1 mA. Assume $\beta = 100$ and remains constant as I is varied, and that $V_A = 10$ V. Present your results in a table.

7.2 Consider the CE amplifiers of Fig. 7.1(b) for the case of $I = 1$ mA, $\beta = 100$, and $V_A = 100$ V. Find R_{in}, A_{vo}, and R_o. If it is required to raise R_{in} by a factor of 4 by changing I, what value of I is required, assuming that β remains unchanged? What are the new values of A_{vo} and R_o? If the amplifier is fed with a signal source having $R_{sig} = 5$ kΩ and is connected to a load of 100-kΩ resistance, find the overall voltage gain, v_o/v_{sig}.

7.3 Find the intrinsic gain of an NMOS transistor fabricated in a process for which $k_n' = 200$ μA/V^2 and $V_A' = 20$ V μm. The transistor has a 0.5-μm channel length and is operated at $V_{OV} = 0.25$ V. If a 2-mA/V transconductance is required, what must I_D and W be?

7.4 An NMOS transistor fabricated in a certain process is found to have an intrinsic gain of 80 V/V when operated at an I_D of 100 μA. Find the intrinsic gain for I_D = 25 μA and I_D = 400 μA. For each of these currents, find the factor by which g_m changes from its value at I_D = 100 μA.

D 7.5 Consider an NMOS transistor fabricated in a 0.18-μm technology for which k'_n = 387 μA/V² and V'_A = 5 V/μm. It is required to obtain an intrinsic gain of 25 V/V and a g_m of 1 mA/V. Using V_{OV} = 0.2 V, find the required values of L, W/L, and the bias current I.

D 7.6 Sketch the circuit for a current-source-loaded CS amplifier that uses a PMOS transistor for the amplifying device. Assume the availability of a single +1.8 -V dc supply. If the transistor is operated with $|V_{OV}|$ = 0.3 V, what is the highest instantaneous voltage allowed at the drain?

D 7.7 An NMOS transistor is fabricated in the 0.18-μm process whose parameters are given in Table 7.A.1 on page 554. The device has a channel length twice the minimum and is operated at V_{OV} = 0.25 V and I_D = 10 μA.

(a) What values of g_m, r_o, and A_0 are obtained?
(b) If I_D is increased to 100 μA, what do V_{OV}, g_m, r_o, and A_0 become?
(c) If the device is redesigned with a new value of W so that it operates at V_{OV} = 0.25 V for I_D = 100 μA, what do g_m, r_o, and A_0 become?
(d) If the redesigned device in (c) is operated at 10 μA, find V_{OV}, g_m, r_o, and A_0.
(e) Which designs and operating conditions produce the lowest and highest values of A_0? What are these values? In each of these two cases, if W/L is held at the same value but L is made 10 times larger, what gains result?

D 7.8 Find A_0 for an NMOS transistor fabricated in a CMOS process for which k'_n = 200 μA/V² and V'_A = 20 V/μm. The transistor has a 0.4-μm channel length and is operated with an overdrive voltage of 0.25 V. What must W be for the NMOS transistor to operate at I_D = 100 μA? Also, find the values of g_m and r_o. Repeat for L = 0.8 μm.

D 7.9 Using a CMOS technology for which k'_n = 200 μA/V² and V'_A = 20 V/μm, design a current-source-loaded CS amplifier for operation at I = 50 μA with V_{OV} = 0.2 V. The amplifier is to have an open-circuit voltage gain of –100 V/V. Assume that the current-source load is ideal. Specify L and W/L.

D 7.10 The circuit in Fig. 7.3(a) is fabricated in a process for which $\mu_n C_{ox} = 2\mu_p C_{ox}$ = 200 μA/V², $V'_{An} = |V'_{Ap}|$ = 20 V/μm, $V_{tn} = -V_{tp}$ = 0.5 V, and V_{DD} = 2.5 V. The two transistors have L = 0.5 μm and are to be operated at I_D = 100 μA and $|V_{OV}|$ = 0.3 V. Find the required values of V_G, $(W/L)_1$, $(W/L)_2$, and A_v.

D 7.11 The circuit in Fig. 7.3(a) is fabricated in a 0.18-μm CMOS technology for which $\mu_n C_{ox}$ = 387 μA/V², $\mu_p C_{ox}$ = 86 μA/V², $V_{tn} = -V_{tp}$ = 0.5 V, V'_{An} = 5 V/μm, $|V'_{Ap}|$ = 6 V/μm, and V_{DD} = 1.8 V. It is required to design the circuit to obtain a voltage gain A_v = –40 V/V. Use devices of equal length L operating at I = 100 μA and $|V_{OV}|$ = 0.2 V. Determine the required values of V_G, L, $(W/L)_1$, and $(W/L)_2$.

7.12 Figure P7.12 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2, find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2.

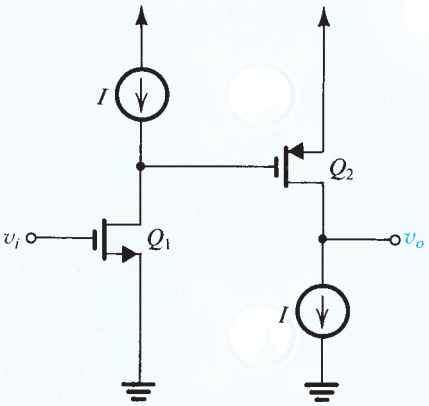


Figure P7.12

***7.13** The NMOS transistor in the circuit of Fig. P7.13 has V_t = 0.5 V, $k'_n W/L$ = 2 mA/V², and V_A = 20 V.

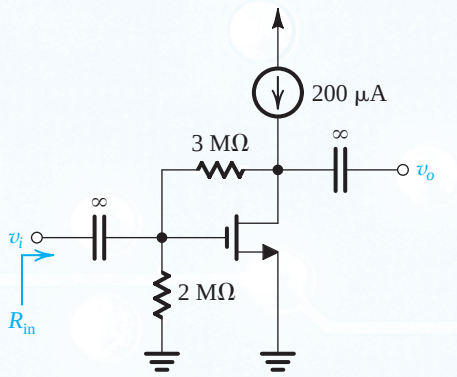


Figure P7.13

(a) Neglecting the dc current in the feedback network and the effect of r_o, find V_{GS}. Then find the dc current in the feedback network and V_{DS}. Verify that you were justified in neglecting the current in the feedback network when you found V_{GS}.

(b) Find the small-signal voltage gain, v_o/v_i. What is the peak of the largest output sinewave signal that is possible while the NMOS transistor remains in saturation? What is the corresponding input signal?
(c) Find the small-signal input resistance R_{in}.

D 7.14 Consider the CMOS amplifier of Fig. 7.4(a) when fabricated with a process for which $k_n' = 2.5k_p' = 250\ \mu A/V^2$, $|V_t| = 0.6$ V, and $|V_A| = 10$ V. Find I_{REF} and $(W/L)_1$ to obtain a voltage gain of –40 V/V and an output resistance of 100 kΩ. If Q_2 and Q_3 are to be operated at the same overdrive voltage as Q_1, what must their *W/L* ratios be?

7.15 Consider the CMOS amplifier analyzed in Example 7.3. If v_I consists of a dc bias component on which is superimposed a sinusoidal signal, find the value of the dc component that will result in the maximum possible signal swing at the output with almost-linear operation. What is the amplitude of the output sinusoid resulting? (*Note:* In practice, the amplifier would have a feedback circuit that causes it to operate at a point near the middle of its linear region.)

7.16 The power supply of the CMOS amplifier analyzed in Example 7.3 is increased to 5 V. What will the extent of the linear region at the output become?

***7.17** Consider the circuit shown in Fig. 7.4(a), using a 3.3-V supply and transistors for which $|V_t| = 0.8$ V and $L = 1\ \mu m$. For Q_1, $k_n' = 100\ \mu A/V^2$, $V_A = 100$ V, and $W = 20\ \mu m$. For Q_2 and Q_3, $k_p' = 50\ \mu A/V^2$ and $|V_A| = 50$ V. For Q_2, $W = 40\ \mu m$. For Q_3, $W = 10\ \mu m$.

(a) If Q_1 is to be biased at 100 μA, find I_{REF}. For simplicity, ignore the effect of V_A.
(b) What are the extreme values of v_O for which Q_1 and Q_2 just remain in saturation?
(c) What is the large-signal voltage gain?
(d) Find the slope of the transfer characteristic at $v_O = V_{DD}/2$.
(e) For operation as a small-signal amplifier around a bias point at $v_O = V_{DD}/2$, find the small-signal voltage gain and output resistance.

****7.18** The MOSFETs in the circuit of Fig. P7.18 are matched, having $k_n'(W/L)_1 = k_p'(W/L)_2 = 1\ mA/V^2$ and $|V_t| = 0.5$ V. The resistance $R = 1\ M\Omega$.

(a) For G and D open, what are the drain currents I_{D1} and I_{D2}?
(b) For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? [*Hint*: Replace the transistors with their small-signal models.]
(c) For finite $r_o(|V_A| = 20$ V), what is the voltage gain from G to D and the input resistance at G?
(d) If G is driven (through a large coupling capacitor) from a source v_{sig} having a resistance of 100 kΩ, find the voltage gain v_d/v_{sig}.
(e) For what range of output signals do Q_1 and Q_2 remain in the saturation region?

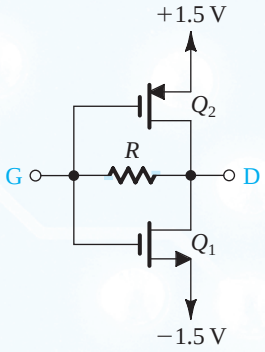


Figure P7.18

7.19 Transistor Q_1 in the circuit of Fig. P7.19 is operating as a CE amplifier with an active load provided by transistor Q_2, which is the output transistor in a current mirror formed by Q_2 and Q_3. (Note that the biasing arrangement for Q_1 is *not* shown.)

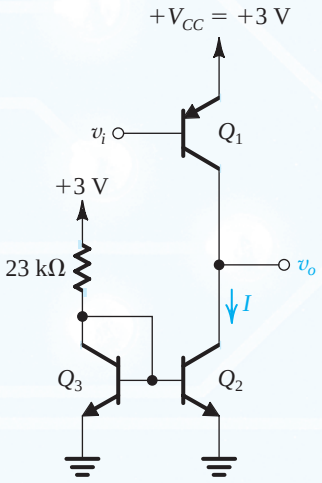


Figure P7.19

(a) Neglecting the finite base currents of Q_2 and Q_3 and assuming that their $V_{BE} \simeq 0.7$ V and that Q_2 has five times the area of Q_3, find the value of *I*.
(b) If Q_1 and Q_2 are specified to have $|V_A| = 50$ V, find r_{o1} and r_{o2} and hence the total resistance at the collector of Q_1.
(c) Find $r_{\pi 1}$ and g_{m1} assuming that $\beta_1 = 50$.
(d) Find R_{in}, A_v, and R_o.

D 7.20 It is required to design the CMOS amplifier of Fig. 7.4(a) utilizing a 0.18-μm process for which $k_n' = 387\ \mu A/V^2$, $k_p' = 86\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.5$ V, $V_{DD} = 1.8$ V, $V_{An}' = 5$ V/μm, and $V_{Ap}' = -6$ V/μm. The output voltage must be able to swing to within approximately 0.2 V of the power-supply rails (i.e., from 0.2 V to 1.6 V) and the voltage gain must be at least 10 V/V. Design for a dc bias current of 50 μA, and use devices with the same channel length. If the channel length is an integer multiple of the minimum 0.18 μm, what channel length is needed and what W/L ratios are required? If it is required to raise the gain by a factor of 2, what channel length would be required, and by what factor does the total gate area of the circuit increase?

Section 7.3: The Cascode Amplifier

D 7.21 In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 40. If the transistor is operated at $V_{OV} = 0.2$ V, what must its V_A be? If the process technology specifies V_A' as 5 V/μm, what channel length must the transistor have?

D 7.22 For a cascode current source such as that in Fig. 7.10, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by $IR_o = 2|V_A|^2/|V_{OV}|$. Now consider the case of transistors that have $|V_A| = 4$ V and are operated at $|V_{OV}|$ of 0.2 V. Also, let $\mu_p C_{ox} = 100\ \mu A/V^2$. Find the W/L ratios required and the output resistance realized for the two cases: (a) $I = 0.1$ mA and (b) $I = 0.5$ mA. Assume that V_{SD} for the two devices is the minimum required (i.e., $|V_{OV}|$).

D *7.23 For a cascode current source, such as that in Fig. 7.10, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by

$$IR_o = \frac{2|V_A'|^2}{|V_{OV}|}L^2$$

Now consider the case of a 0.18-μm technology for which $|V_A'| = 5$ V/μm and let the transistors be operated at $|V_{OV}| = 0.2$ V. Find the figure-of-merit IR_o for the three cases of L equal to the minimum channel length, twice the minimum, and three times the minimum. Complete the entries of the table at the bottom of the page. Give W/L and the area $2WL$ in terms of n. In the table, A_v denotes the gain obtained in a cascode amplifier such as that in Fig. 7.11 that utilizes our current source as load and which has the same values of g_m and R_o as the current-source transistors.

(a) For each current value, what is price paid for the increase in R_o and A_v obtained as L is increased?
(b) For each value of L, what advantage is obtained as I is increased, and what is the price paid?
(c) Contrast the performance obtained from the circuit with the largest area with that obtained from the circuit with the smallest area.

D 7.24 Design the cascode amplifier of Fig. 7.9(a) to obtain $g_{m1} = 1$ mA/V and $R_o = 400\ k\Omega$. Use a 0.18-μm technology for which $V_{tn} = 0.5$ V, $V_A' = 5$ V/μm and $k_n' = 400\ \mu A/V^2$. Determine L, W/L, V_{G2}, and I. Use identical transistors operated at $V_{OV} = 0.2$ V, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?

7.25 The cascode amplifier of Fig. 7.11 is operated at a current of 0.1 mA with all devices operating at $|V_{OV}| = 0.25$ V.

	$L = L_{min} = 0.18$ μm $IR_o =$ V				$L = 2L_{min} = 0.36$ μm $IR_o =$ V				$L = 3L_{min} = 0.54$ μm $IR_o =$ V			
	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm^2)	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm^2)	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm^2)
$I = 0.01$ mA $W/L = n$												
$I = 0.1$ mA $W/L =$												
$I = 1.0$ mA $W/L =$												

All devices have $|V_A| = 4$ V. Find g_{m1}, the output resistance of the amplifier, R_{on}, the output resistance of the current source, R_{op}, the overall output resistance, R_o, and the voltage gain, A_v.

D 7.26 Design the CMOS cascode amplifier in Fig. 7.11 for the following specifications: $g_{m1} = 2$ mA/V and $A_v = -200$ V/V. Assume that for the available fabrication process, $|V'_A| = 5$ V/μm for both NMOS and PMOS devices and that $\mu_n C_{ox} = 4\,\mu_p C_{ox} = 400$ μA/V^2. Use the same channel length L for all devices and operate all four devices at $|V_{OV}| = 0.2$ V. Determine the required channel length L, the bias current I, and the W/L ratio for each of four transistors. Assume that suitable bias voltages have been chosen, and neglect the Early effect in determining the W/L ratios.

D 7.27 Design the circuit of Fig. 7.10 to provide an output current of 100 μA. Use $V_{DD} = 3.3$ V, and assume the PMOS transistors to have $\mu_p C_{ox} = 60$ μA/V^2, $V_{tp} = -0.8$ V, and $|V_A| = 5$ V. The current source is to have the widest possible signal swing at its output. Design for $V_{OV} = 0.2$ V, and specify the values of the transistor W/L ratios and of V_{G3} and V_{G4}. What is the highest allowable voltage at the output? What is the value of R_o?

7.28 The cascode transistor can be thought of as providing a "shield" for the input transistor from the voltage variations at the output. To quantify this "shielding" property of the cascode, consider the situation in Fig. P7.28. Here we have grounded the input terminal (i.e., reduced v_i to zero), applied a small change v_x to the output node, and denoted the voltage change that results at the drain of Q_1 by v_y. By what factor is v_y smaller than v_x?

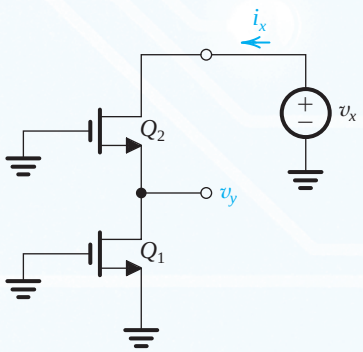


Figure P7.28

***7.29** In this problem we investigate whether, as an alternative to cascoding, we can simply increase the channel length L of the CS MOSFET. Specifically, we wish to compare the two circuits shown in Fig. P7.29(b) and (c). The circuit in Fig. P7.29(b) is a CS amplifier in which the channel length has been quadrupled relative to that of the original CS amplifier in Fig. P7.29(a) while the drain bias current has been kept constant.

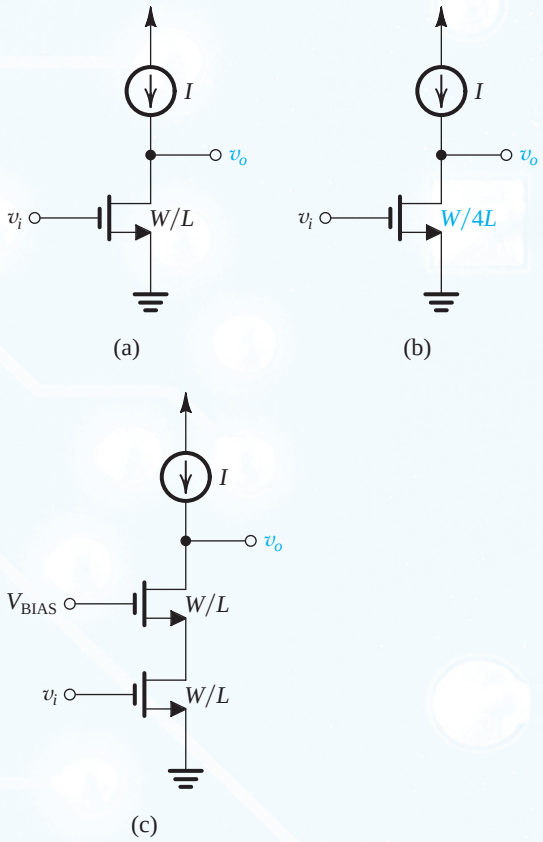


Figure P7.29

(a) Show that for this circuit V_{OV} is double that of the original circuit, g_m is half that of the original circuit, and A_0 is double that of the original circuit.
(b) Compare these values to those of the cascode circuit in Fig. P7.29(c), which is operating at the same bias current and has the same minimum voltage requirement at the drain as in the circuit of Fig. P7.29(b).

7.30 Consider the cascode amplifier of Fig. 7.11 with the dc component at the input $V_I = 0.8$ V, $V_{G2} = 1.2$ V, $V_{G3} = 1.3$ V, $V_{G4} = 1.7$ V, and $V_{DD} = 2.5$ V. If all devices are matched, that is $k_{n1} = k_{n2} = k_{p3} = k_{p4}$, and have equal $|V_t|$ of 0.5 V, what is the overdrive voltage at which the four transistors are operating? What is the allowable voltage range at the output?

7.31 Figure P7.31 shows a CG transistor fed with a signal source (v_{sig}, R_{sig}) and loaded with a resistance R_L.

(a) Find R_{in}.
(b) Noting that the current through R_L is equal to the input current i, find an expression for the overall voltage gain v_o / v_{sig}.
(c) Determine the values of R_{in} and v_o / v_{sig} for the case of $R_L = r_o = 10$ kΩ, $A_0 = 20$, and $R_{sig} = 1$ kΩ.

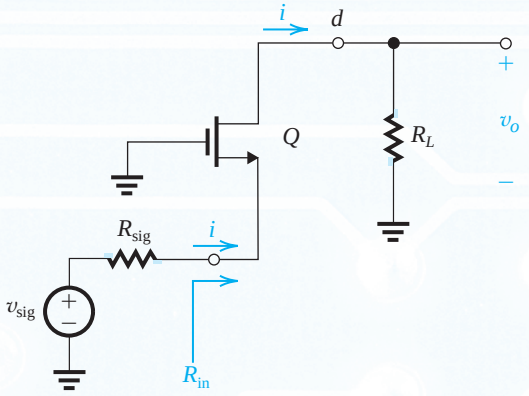


Figure P7.31

7.32 The CG transistor in Fig. P7.31 can be replaced by an equivalent circuit consisting of a controlled-source $G_m v_{sig}$ and an output resistance R_o, as shown in Fig. P7.32. Here G_m is the short-circuit transconductance. Its value can be determined by short-circuiting d to ground, finding the value of i, and dividing it by v_{sig}. The value of R_o is that of a CG transistor with a resistance R_{sig} in its source (Refer to Fig. 7.13).

(a) Find expressions for G_m and R_o.
(b) For the case $R_L = r_o = 10\ \text{k}\Omega$, $g_m r_o = 20$, and $R_{sig} = 1\,\text{k}\Omega$, find G_m, R_o, and v_o/v_{sig}.

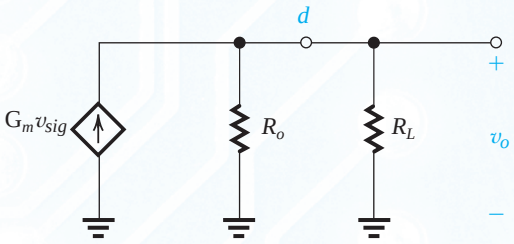


Figure P7.32

SIM 7.33 A CMOS cascode amplifier has identical CS and CG transistors that have $W/L = 5.4\ \mu\text{m}/0.36\ \mu\text{m}$ and biased at $I = 0.2$ mA. The fabrication process has $\mu_n C_{ox} = 4$, $\mu_p C_{ox} = 400\ \mu\text{A/V}^2$, and $V_A' = 5\ \text{V}/\mu\text{m}$. At what value of R_L does the gain become –100 V/V? What is the voltage gain of the common-source stage?

7.34 The purpose of this problem is to investigate the signal currents and voltages at various points throughout a cascode amplifier circuit. Knowledge of this signal distribution is very useful in designing the circuit so as to allow for the required signal swings. Figure P7.34 shows a CMOS cascode amplifier with all dc voltages replaced with signal grounds. As well, we have explicitly shown the resistance r_o of each of the four transistors. For simplicity, we are assuming that the four transistors have the same g_m and r_o. The amplifier is fed with a signal v_i.

(a) Determine R_1, R_2, and R_3.
(b) Determine i_1, i_2, i_3, i_4, i_5, i_6, and i_7, all in terms of v_i.
(c) Determine v_1, v_2, and v_3, all in terms of v_i.
(d) If v_i is a 5-mV peak sine wave and $g_m r_o = 20$, sketch and clearly label the waveforms of v_1, v_2, and v_3.

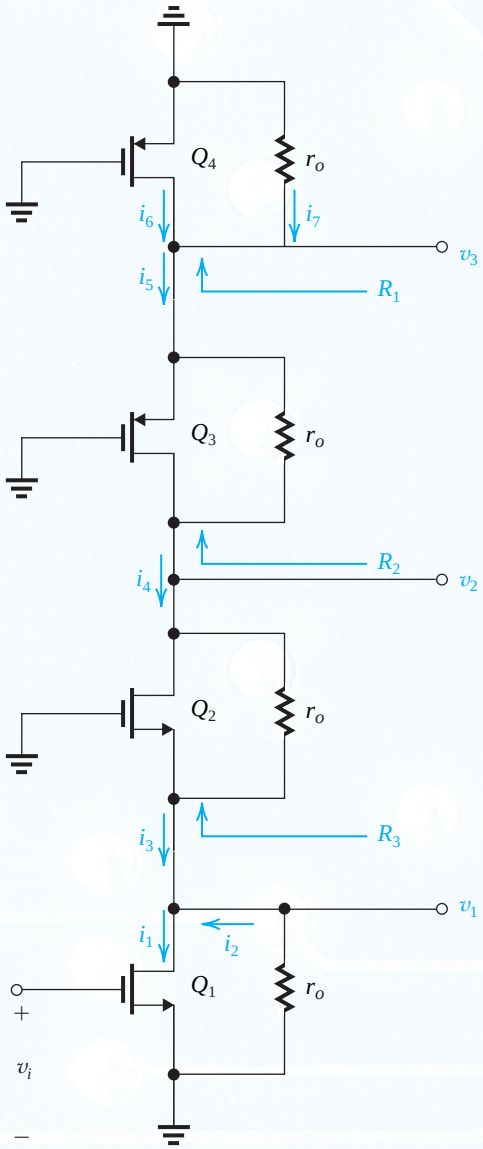


Figure P7.34

7.35 Figure P7.35 shows a CS amplifier with a resistance R_s in the source lead and with the drain short-circuited to ground. Determine the short-circuit transconductance G_m. Hence provide the output equivalent circuit of the source-degenerated CS amplifier, and show that the open-circuit voltage gain $A_{vo} = -A_0$.

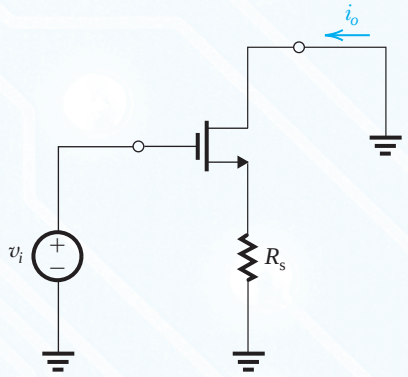


Figure P7.35

7.36 A CS amplifier operating with a g_m of 2 mA/V and having $r_o = 20$ kΩ has a 2-kΩ resistance R_s connected in its source lead. Find the output resistance R_o. Recalling that the open-circuit voltage gain remains unchanged at A_0, find the gain obtained with $R_L = 100$ kΩ.

D 7.37 Design the double-cascode current source shown in Fig. P7.37 to provide $I = 0.1$ mA and the largest possible signal swing at the output; that is, design for the minimum allowable voltage across each transistor. The 0.18-μm CMOS fabrication process available has $V_{tp} = -0.5$ V, $V'_A = -6$ V/μm, and $\mu_p C_{ox} = 100$ μA/V^2. Use devices with $L = 0.5$ μm, and operate at $|V_{OV}| = 0.2$ V. Specify V_{G1}, V_{G2}, V_{G3}, and the W/L ratios of the transistors. What is the value of R_o achieved?

7.38 Figure P7.38 shows a folded-cascode CMOS amplifier utilizing a simple current source Q_2, supplying a current $2I$, and a cascoded current-source (Q_4, Q_5) supplying a current I. Assume, for simplicity, that all transistors have equal parameters g_m and r_o.

(a) Give approximate expressions for all the resistances indicated.
(b) Find the amplifier output resistance R_o.
(c) Show that the short-circuit transconductance G_m is approximately equal to g_{m1}.
(d) Find the overall voltage gain v_o/v_i and evaluate its value for the case $g_{m1} = 2$ mA/V and $A_0 = 20$.

7.39 A cascode current source formed of two *pnp* transistors for which $\beta = 50$ and $V_A = 5$ V supplies a current of 0.5 mA. What is the output resistance?

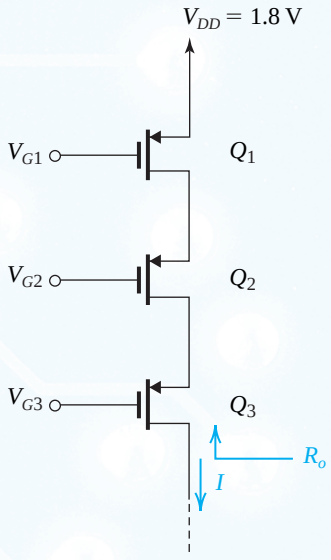


Figure P7.37

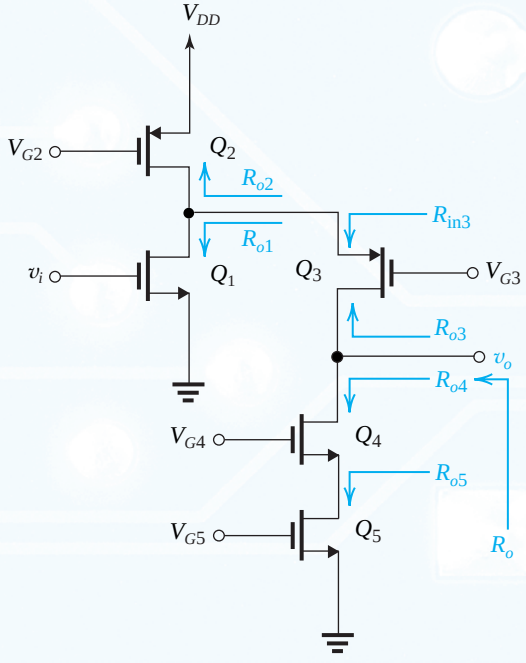


Figure P7.38

7.40 Use Eq. (7.45) to show that for a BJT cascode current source utilizing identical *pnp* transistors and supplying a current I,

$$IR_o = \frac{|V_A|}{(V_T/|V_A|) + (1/\beta)}$$

Evaluate the figure-of-merit IR_o for the case $|V_A| = 5$ V and $\beta = 50$. Now find R_o for the cases of $I = 0.1$, 0.5, and 1.0 mA.

7.41 Consider the BJT cascode amplifier of Fig. 7.19 for the case all transistors have equal β and r_o. Show that the voltage gain A_v can be expressed in the form

$$A_v = -\frac{1}{2}\frac{|V_A|/V_T}{(V_T/|V_A|)+(1/\beta)}$$

Evaluate A_v for the case $|V_A| = 5$ V and $\beta = 50$. Note that except for the fact that β depends on I as a second-order effect, the gain is independent of the bias current I!

7.42 A bipolar cascode amplifier has a current-source load with an output resistance βr_o. Let $\beta = 100$, $|V_A| = 100$ V, and $I = 0.1$ mA. Find the voltage gain A_v.

7.43 Find the value of the resistance R_e, which, when connected in the emitter lead of a CE BJT amplifier, raises the output resistance by a factor of (a) 5, (b) 10, and (c) 50. What is the maximum possible factor by which the output resistance can be raised, and at what value of R_e is it achieved? Assume the BJT has $\beta = 100$ and is biased at $I_C = 0.5$ mA.

***7.44** Consider the CE amplifier with an emitter-degeneration resistance R_e, shown in Fig. P7.44(a). It is required to represent the output circuit of the amplifier with the equivalent circuit shown in Fig. P7.44(b). Here A_{vo} is the open-circuit voltage gain $[v_o/v_i]_{R_L=\infty}$, and R_o is the output resistance (given by Eq. 7.50). Replace the BJT with its hybrid-π model, set $R_L = \infty$ (i.e., open-circuit the collector), and show that

$$A_{vo} = -g_m r_o \frac{1 - R_e/\beta r_o}{1 + R_e/r_\pi}$$

Now, use this result to find the overall short-circuit transconductance G_m (see Fig. P7.44c) and show that

$$G_m \simeq \frac{g_m}{1 + g_m R_e}$$

State clearly all the approximations you made to arrive at this expression for G_m.

For a BJT with $\beta = 100$ and $r_o = 100$ kΩ biased at $I_C = 0.2$ mA and having a resistance $R_e = 250$ Ω in its emitter, find R_o, A_{vo}, and G_m. Also calculate the voltage gain A_v obtained with $R_L = 10$ kΩ.

D *7.45 Figure P7.45 shows four possible realizations of the folded cascode amplifier. Assume that the BJTs have $\beta = 100$ and that both the BJTs and the MOSFETs have $|V_A| = 5$ V. Let $I = 100$ μA, and assume that the MOSFETs are operating at $|V_{OV}| = 0.2$ V. Assume the current sources

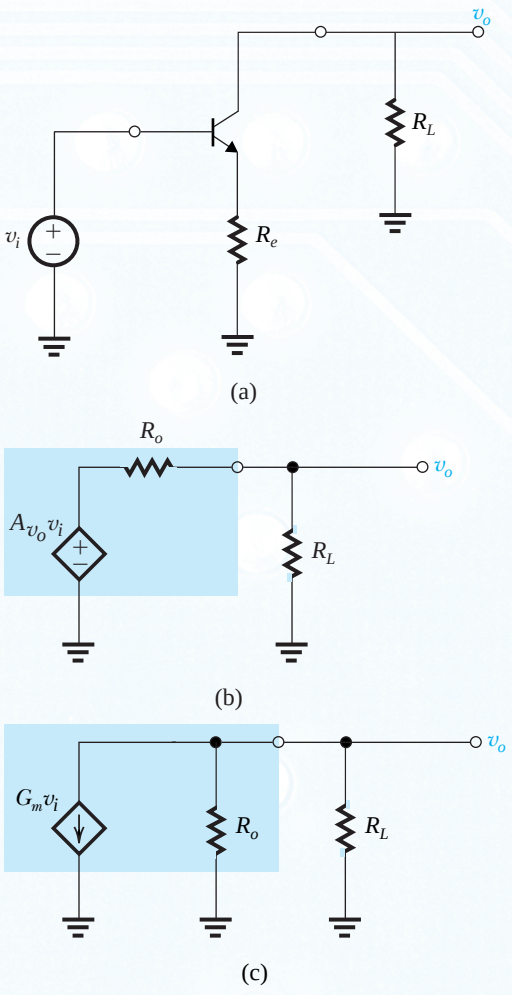


Figure P7.44

are ideal. For each circuit determine, R_{in}, R_o, and A_{vo}. Comment on your results.

Section 7.4: IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits

D 7.46 For $V_{DD} = 1.8$ V and using $I_{REF} = 100$ μA, it is required to design the circuit of Fig. 7.22 to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5 μm, channel widths of 4 μm, $V_t = 0.5$ V, and $k_n' = 400$ μA/V^2. What is the lowest possible value of V_O? Assuming that for this process technology the Early voltage $V_A' = 10$ V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a +0.5-V change in V_O.

D 7.47 Using $V_{DD} = 1.8$ V and a pair of matched MOSFETs, design the current-source circuit of Fig. 7.22 to provide

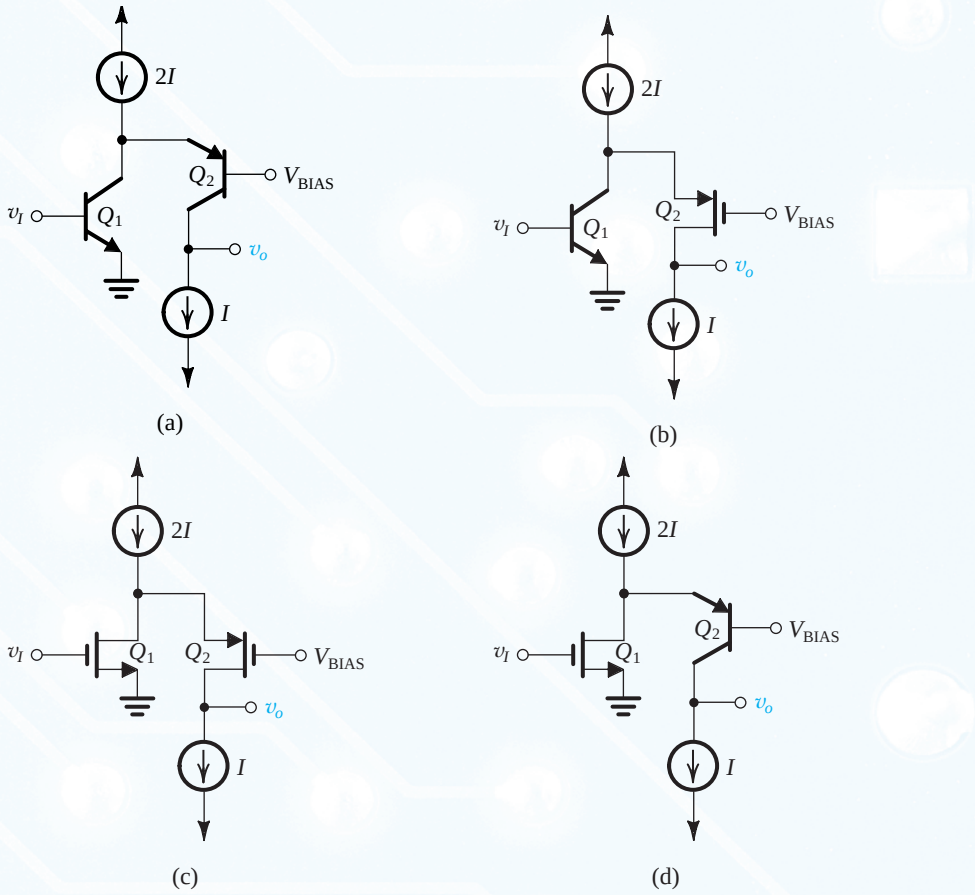


Figure P7.45

an output current of 200-μA nominal value. To simplify matters, assume that the nominal value of the output current is obtained at $V_O \simeq V_{GS}$. It is further required that the circuit operate for V_O in the range of 0.2 V to V_{DD} and that the change in I_O over this range be limited to 5% of the nominal value of I_O. Find the required value of R and the device dimensions. For the fabrication-process technology utilized, $\mu_n C_{ox} = 400\ \mu A/V^2$, $V_A' = 10\ V/\mu m$, and $V_t = 0.5\ V$.

7.48 Sketch the *p*-channel counterpart of the current-source circuit of Fig. 7.22. Note that while the circuit of Fig. 7.22 should more appropriately be called a current sink, the corresponding PMOS circuit is a current source. Let $V_{DD} = 1.8$ V, $|V_t| = 0.5$ V, Q_1 and Q_2 be matched, and $\mu_p C_{ox} = 100\ \mu A/V^2$. Find the device *W*/*L* ratios and the value of the resistor that sets the value of I_{REF} so that a nominally 80-μA output current is obtained. The current source is required to operate for V_O as high as 1.6 V. Neglect channel-length modulation.

SIM **7.49** Consider the current-mirror circuit of Fig. 7.23 with two transistors having equal channel lengths but with Q_2 having a width five times that of Q_1. If I_{REF} is 20 μA and the transistors are operating at an overdrive voltage of 0.2 V, what I_O results? What is the minimum allowable value of V_O for proper operation of the current source? If $V_t = 0.5$ V, at what value of V_O will the nominal value of I_O be obtained? If V_O increases by 1 V, what is the corresponding increase in I_O? Let $V_A = 20$ V.

7.50 For the current-steering circuit of Fig. P7.50, find I_O in terms of I_{REF} and device *W*/*L* ratios.

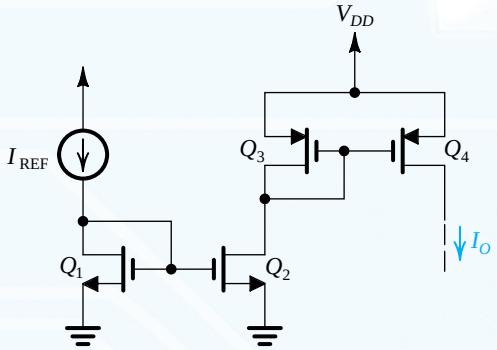


Figure P7.50

D 7.51 The current-steering circuit of Fig. P7.51 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 80\ \mu A/V^2$, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, $V'_{An} = 10$ V/µm, and $|V'_{Ap}| = 12$ V/µm. If all devices have $L = 0.8$ µm, design the circuit so that $I_{REF} = 20\ \mu A$, $I_2 = 100\ \mu A$, $I_3 = I_4 = 20\ \mu A$, and $I_5 = 50\ \mu A$. Use the minimum possible device widths needed to achieve proper operation of the current source Q_2 for voltages at its drain as high as +1.3 V and proper operation of the current sink Q_5 with voltages at its drain as low as –1.3 V. Specify the widths of all devices and the value of R. Find the output resistance of the current source Q_2 and the output resistance of the current sink Q_5.

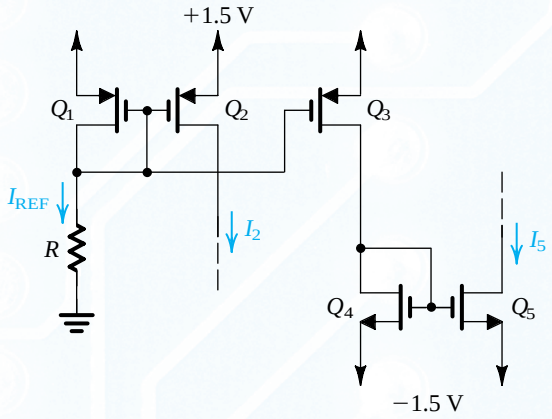


Figure P7.51

***7.52** A PMOS current mirror consists of three PMOS transistors, one diode connected and two used as current outputs. All transistors have $|V_t| = 0.6$ V, $k'_p = 100\ \mu A/V^2$, and $L = 1.0$ µm but three different widths, namely, 10 µm, 20 µm, and 40 µm. When the diode-connected transistor is supplied from a 100-µA source, how many different output currents are available? Repeat with two of the transistors diode connected and the third used to provide current output. For each possible input-diode combination, give the values of the output currents and of the V_{SG} that results.

7.53 Although thus far we have focused only on their application in dc biasing, current mirrors can also be used as signal-current amplifiers. One such application is illustrated in Fig. P7.53. Here Q_1 is a common-source amplifier fed with $v_I = V_{GS} + v_i$, where V_{GS} is the gate-to-source dc bias voltage of Q_1 and v_i is a small signal to be amplified. Find the signal component of the output voltage v_O and hence the small-signal voltage gain v_o/v_i. For this purpose, you may neglect all r_o's. Also, find the small-signal resistance of the diode-connected transistor Q_2 in terms of g_{m2} and r_{o2}, and hence the total resistance between the drain of Q_1 and ground. What is the voltage gain of the CS amplifier Q_1?

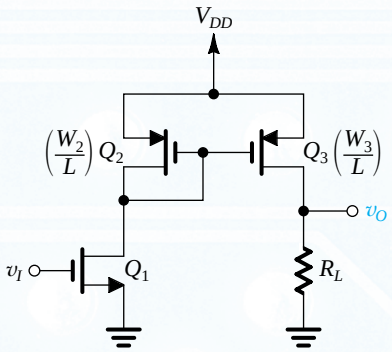


Figure P7.53

7.54 Consider the basic bipolar current mirror of Fig. 7.28 for the case in which Q_1 and Q_2 are identical devices having $I_S = 10^{-16}$ A.

(a) Assuming the transistor β is very high, find the range of V_{BE} and I_O corresponding to I_{REF} increasing from 10 µA to 10 mA. Assume that Q_2 remains in the active mode, and neglect the Early effect.

(b) Find the range of I_O corresponding to I_{REF} in the range of 10 µA to 10 mA, taking into account the finite β. Assume that β remains constant at 100 over the current range 0.1 mA to 5 mA but that at $\simeq 10$ µA and at $I_C \simeq 10$ mA, $\beta = 50$. Specify I_O corresponding to $I_{REF} = 10\ \mu A$, 0.1 mA, 1 mA, and 10 mA. Note that β variation with current causes the current transfer ratio to vary with current.

7.55 Consider the basic BJT current mirror of Fig. 7.28 for the case in which Q_2 has m times the area of Q_1. Show that the current transfer ratio is given by Eq. (7.69). If β is specified to be a minimum of 50, what is the largest current transfer ratio possible if the error introduced by the finite β is limited to 10%?

7.56 Give the circuit for the *pnp* version of the basic current mirror of Fig. 7.28. If β of the *pnp* transistor is 20, what is the current gain (or transfer ratio) I_O/I_{REF} for the case of identical transistors, neglecting the Early effect?

7.57 Consider the basic BJT current mirror of Fig. 7.28 when Q_1 and Q_2 are matched and $I_{REF} = 2$ mA. Neglecting the effect of finite β, find the change in I_O, both as an absolute value and as a percentage, corresponding to V_O changing from 1 V to 10 V. The Early voltage is 90 V.

D 7.58 The current-source circuit of Fig. P7.58 utilizes a pair of matched *pnp* transistors having $I_S = 10^{-15}$ A, $\beta = 50$, and $|V_A| = 50$ V. It is required to design the circuit to provide an output current $I_O = 1$ mA at $V_O = 2$ V. What values of I_{REF}

and R are needed? What is the maximum allowed value of V_O while the current source continues to operate properly? What change occurs in I_O corresponding to V_O changing from the maximum positive value to –5 V?

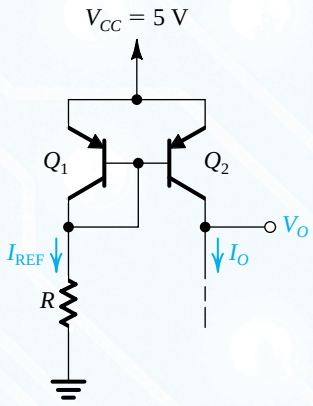


Figure P7.58

7.59 Find the voltages at all nodes and the currents through all branches in the circuit of Fig. P7.59. Assume $|V_{BE}|$ = 0.7 V and $\beta = \infty$.

7.60 For the circuit in Fig. P7.60, let $|V_{BE}|$ = 0.7 V and $\beta = \infty$. Find I, V_1, V_2, V_3, V_4, and V_5 for (a) R = 10 kΩ and (b) R = 100 kΩ.

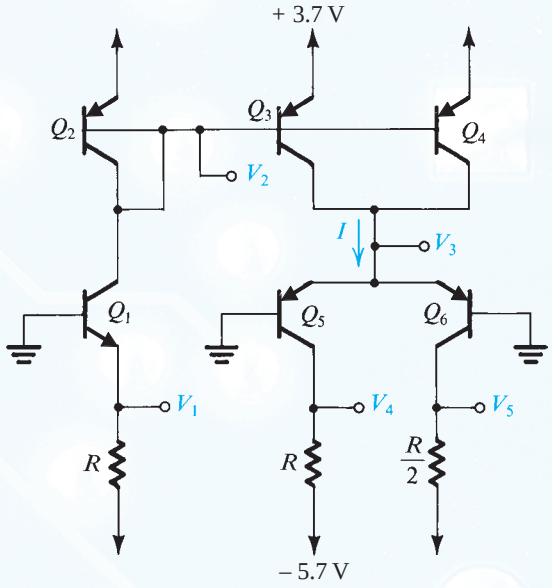


Figure P7.60

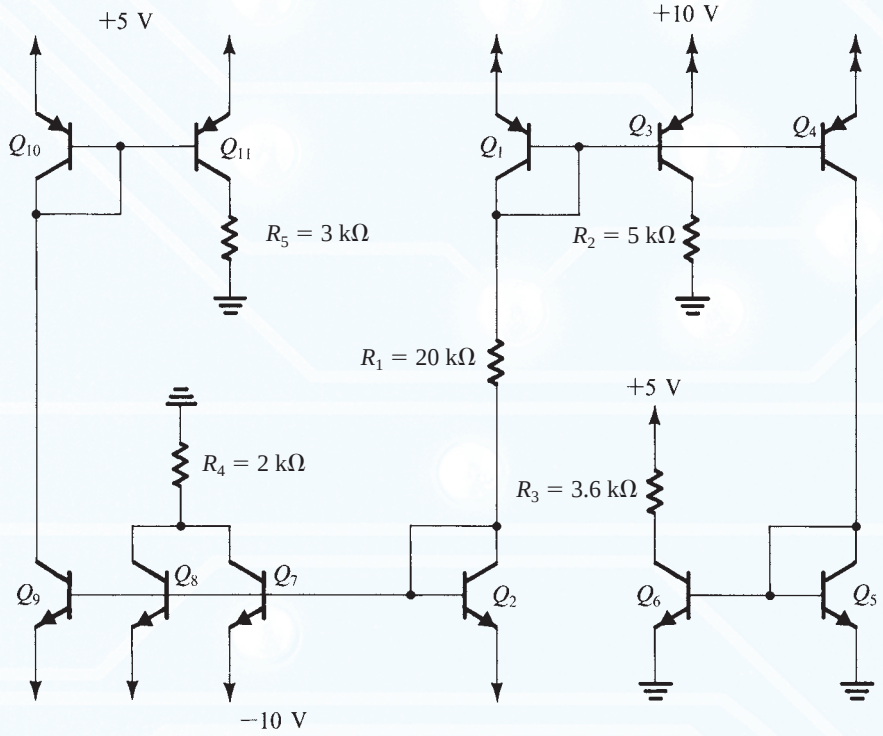


Figure P7.59

D 7.61 Using the ideas embodied in Fig. 7.31, design a multiple-mirror circuit using power supplies of ±5 V to create source currents of 0.2 mA, 0.4 mA, and 0.8 mA and sink currents of 0.5 mA, 1 mA, and 2 mA. Assume that the BJTs have $|V_{BE}| \simeq 0.7$ V and large β. What is the total power dissipated in your circuit?

***7.62** Figure P7.62 shows a current-mirror circuit prepared for small-signal analysis. Replace the BJTs with their hybrid-π models and find expressions for R_{in} and i_o/i_i, where i_o is the output short-circuit current. Assume $r_o \gg r_\pi$.

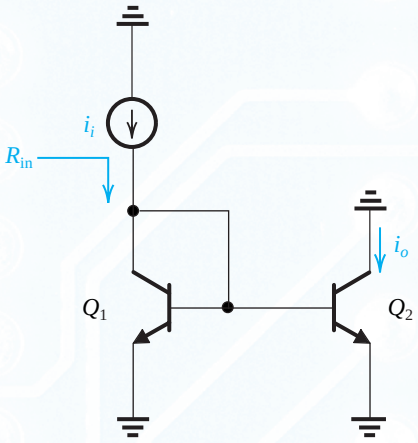


Figure P7.62

7.63 For the constant-current source circuit shown in Fig. P7.63, find the collector current I and the output resistance. The BJT is specified to have $\beta = 100$ and $V_A = 100$ V. If the collector voltage undergoes a change of 10 V while the BJT remains in the active mode, what is the corresponding change in collector current?

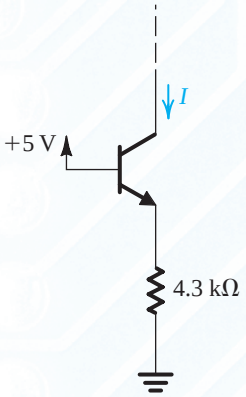


Figure P7.63

7.64 For the MOS cascode current mirror of Fig. 7.32 with $V_t = 0.5$ V, $k_n = 4$ mA/V^2, $V_A = 10$ V, and $I_{REF} = 100\,\mu$A, find R_o and the minimum allowable voltage at the output. At what value of V_O is I_O equal to I_{REF}? What does I_O become at $V_O = 5$ V?

Section 7.5: Current-Mirror Circuits with Improved Performance

SIM 7.65 In a particular cascoded current mirror, such as that shown in Fig. 7.32, all transistors have $V_t = 0.6$ V, $\mu_n C_{ox} = 160\ \mu$A/V^2, $L = 1\ \mu$m, and $V_A = 10$ V. Width $W_1 = W_4 = 4\ \mu$m, and $W_2 = W_3 = 40\ \mu$m. The reference current I_{REF} is 20 μA. What output current results? What are the voltages at the gates of Q_2 and Q_3? What is the lowest voltage at the output for which current-source operation is possible? What are the values of g_m and r_o of Q_2 and Q_3? What is the output resistance of the mirror?

7.66 Find the output resistance of the double-cascode current mirror of Fig. P7.66.

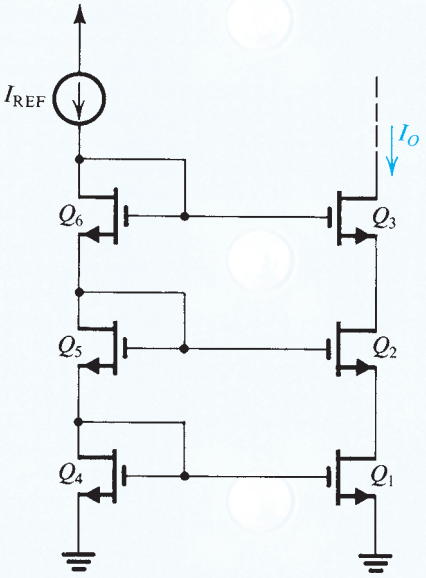


Figure P7.66

7.67 For the base-current-compensated mirror of Fig. 7.33, let the three transistors be matched and specified to have a collector current of 1 mA at $V_{BE} = 0.7$ V. For I_{REF} of 100 μA and assuming $\beta = 200$, what will the voltage at node x be? If I_{REF} is increased to 1 mA, what is the change in V_x? What is the value of I_O obtained with $V_O = V_x$ in both cases? Give the percentage difference between the actual and ideal value of I_O. What is the lowest voltage at the output for which proper current-source operation is maintained?

D 7.68 Extend the current-mirror circuit of Fig. 7.33 to n outputs. What is the resulting current transfer ratio from the input to each output, I_O/I_{REF}? If the deviation from unity is to be kept at 0.1% or less, what is the maximum possible number of outputs for BJTs with $\beta = 100$?

***7.69** For the base-current-compensated mirror of Fig. 7.33, show that the incremental input resistance (seen by the reference current source) is approximately $2\,V_T/I_{REF}$. Evaluate R_{in} for $I_{REF} = 100\ \mu A$. [*Hint*: Q_3 is operating at a current $I_{E3} = 2I_C/\beta$, where I_C is the operating current of each of Q_1 and Q_2. Replace each transistor with its T model and neglect r_o.]

7.70 Consider the Wilson current-mirror circuit of Fig. 7.34 when supplied with a reference current I_{REF} of 1 mA. What is the change in I_O corresponding to a change of +10 V in the voltage at the collector of Q_3? Give both the absolute value and the percentage change. Let $\beta = 100$ and $V_A = 100$ V.

D *7.71 (a) The circuit in Fig. P7.71 is a modified version of the Wilson current mirror. Here the output transistor is "split" into two matched transistors, Q_3 and Q_4. Find I_{O1} and I_{O2} in terms of I_{REF}. Assume all transistors to be matched with current gain β.
(b) Use this idea to design a circuit that generates currents of 0.1 mA, 0.2 mA, and 0.4 mA, using a reference current source of 0.7 mA. What are the actual values of the currents generated for $\beta = 50$?

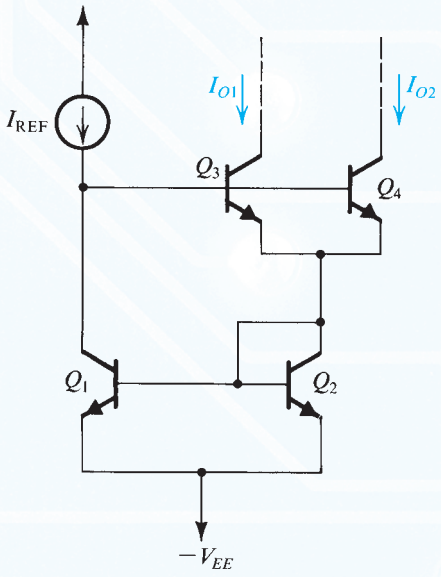


Figure P7.71

D 7.72 Use the *pnp* version of the Wilson current mirror to design a 0.2-mA current source. The current source is required to operate with the voltage at its output terminal as low as −2.5 V. If the power supplies available are ±2.5 V, what is the highest voltage possible at the output terminal?

***7.73** For the Wilson current mirror of Fig. 7.34, show that the incremental input resistance seen by I_{REF} is approximately $2\,V_T/I_{REF}$. (Neglect the Early effect in this derivation.) Evaluate R_{in} for $I_{REF} = 100\ \mu A$.

***7.74** Consider the Wilson MOS mirror of Fig. 7.35(a) for the case of all transistors identical, with $W/L = 12.5$, $\mu_n C_{ox} = 400\ \mu A/V^2$, and $V_A = 20$ V. The mirror is fed with $I_{REF} = 100\ \mu A$.

(a) Obtain an estimate of V_{OV} and V_{GS} at which the three transistors are operating, by neglecting the Early effect.
(b) Noting that Q_1 and Q_2 are operating at different V_{DS}, obtain an approximate value for the difference in their currents and hence determine I_O.
(c) To eliminate the systematic error between I_O and I_{REF} caused by the difference in V_{DS} between Q_1 and Q_2, a diode-connected transistor Q_4 can be added to the circuit as shown in Fig. 7.35(c). What do you estimate I_O now to be?
(d) What is the minimum allowable voltage at the output node of the mirror?
(e) Convince yourself that Q_4 will have no effect on the output resistance of the mirror. Find R_o.
(f) What is the change in I_O (both absolute value and percentage) that results from $\Delta V_O = 1$ V?

7.75 Show that the input resistance (seen by I_{REF}) for the Wilson MOS mirror of Fig. 7.35(a) is given by $2/g_m$. Assume that all three transistors are identical and neglect the Early effect. [*Hint*: Replace all transistors by their T model and remember that Q_1 is equivalent to a resistance $1/g_m$.]

D 7.76 (a) Utilizing a reference current of 100 μA, design a Widlar current source to provide an output current of 10 μA. Let the BJTs have $v_{BE} = 0.8$ V at 1-mA current, and assume β to be high.

(b) If $\beta = 200$ and $V_A = 50$ V, find the value of the output resistance, and find the change in output current corresponding to a 5-V change in output voltage.

D 7.77 Design three Widlar current sources, each having a 100-μA reference current: one with a current transfer ratio of 0.9, one with a ratio of 0.10, and one with a ratio of 0.01, all assuming high β. For each, find the output resistance, and contrast it with r_o of the basic unity-ratio source for which $R_E = 0$. Use $\beta = \infty$ and $V_A = 50$ V.

7.78 The BJT in the circuit of Fig. P7.78 has $V_{BE} = 0.7$ V, $\beta = 100$, and $V_A = 50$ V. Find R_o.

D 7.79 (a) For the circuit in Fig. P7.79, assume BJTs with high β and $v_{BE} = 0.8$ V at 1 mA. Find the value of R that will result in $I_O = 10\ \mu A$.

(b) For the design in (a), find R_o assuming $\beta = 100$ and $V_A = 50$ V.

D *7.80 If the *pnp* transistor in the circuit of Fig. P7.80 is characterized by its exponential relationship with a scale current

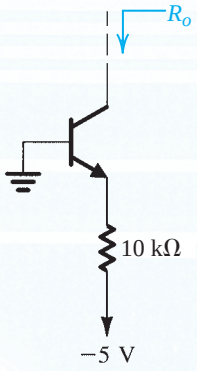


Figure P7.78

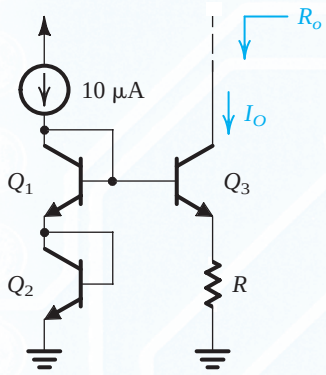


Figure P7.79

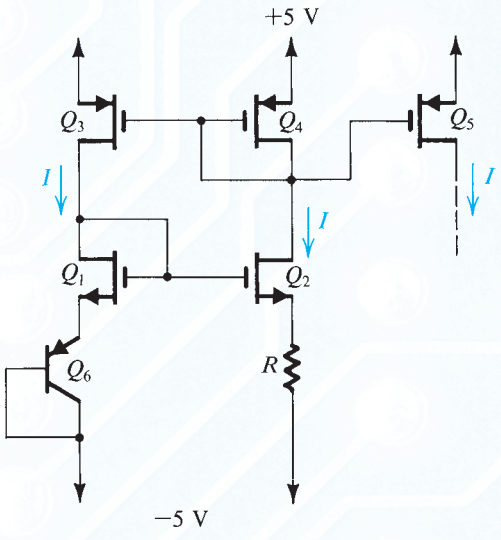


Figure P7.80

I_S, show that the dc current I is determined by $IR = V_T \ln(I/I_S)$. Assume Q_1 and Q_2 to be matched and Q_3, Q_4, and Q_5 to be matched. Find the value of R that yields a current $I = 100$ μA. For the BJT, $V_{EB} = 0.7$ V at $I_E = 1$ mA.

Section 7.6: Some Useful Transistor Pairings

7.81 The transistors in the circuit of Fig. P7.81 have $\beta = 100$ and $V_A = 100$ V.

(a) Find R_{in} and the overall voltage gain.
(b) What is the effect of increasing the bias currents by a factor of 10 on R_{in}, G_v, and the power dissipation?

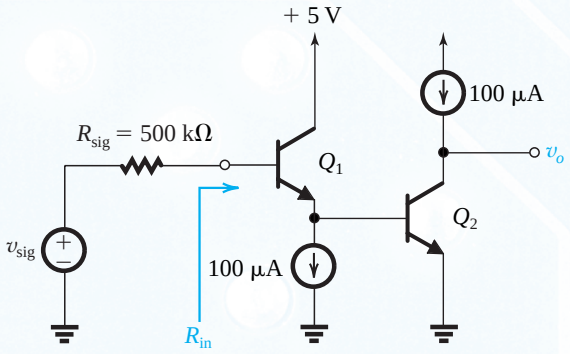


Figure P7.81

D *7.82 Consider the BiCMOS amplifier shown in Fig. P7.82. The BJT has $V_{BE} = 0.7$ V and $\beta = 200$. The MOSFET has $V_t = 1$ V and $k_n = 2$ mA/V^2. Neglect the Early effect in both devices.

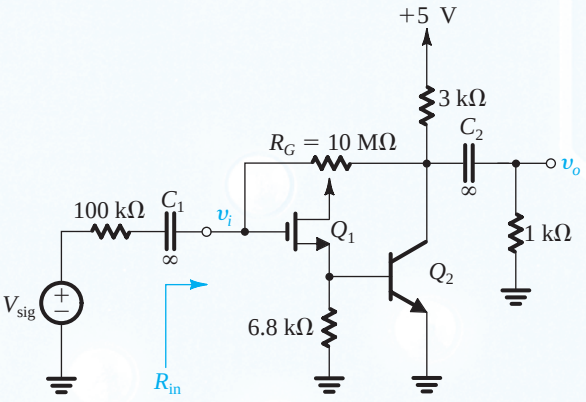


Figure P7.82

(a) Consider the dc bias circuit. Neglect the base current in Q_2 in determining the current in Q_1. Find the dc bias currents in Q_1 and Q_2 and show that they are approximately 100 μA and 1 mA, respectively.
(b) Evaluate the small-signal parameters of Q_1 and Q_2 at their bias points.
(c) Determine the voltage gain $A_v = v_o/v_i$. For this purpose you can neglect R_G.

(d) Noting that R_G is connected between the input node where the voltage is v_i and the output node where the voltage is $A_v v_i$, find R_{in} and hence the overall voltage gain v_o/v_{sig}.

(e) To considerably reduce the effect of R_G on R_{in} and hence on G_v, consider the effect of adding another 10-MΩ resistor in series with the existing one and placing a large bypass capacitor between their joint node and ground. What will R_{in} and G_v become?

7.83 The BJTs in the Darlington follower of Fig. P7.83 have $\beta = 100$. If the follower is fed with a source having a 100-kΩ resistance and is loaded with 1 kΩ, find the input resistance and the output resistance (excluding the load). Also find the overall voltage gain, both open-circuited and with load.

7.84 For the amplifier in Fig. 7.41(a), let $I = 1$ mA and $\beta = 120$, and neglect r_o. Assume that a load resistance of 10 kΩ is connected to the output terminal. If the amplifier is fed with a signal v_{sig} having a source resistance $R_{sig} = 20$ kΩ, find G_v.

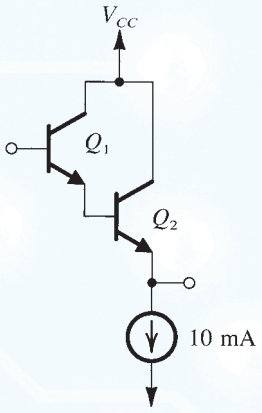


Figure P7.83

7.85 Consider the CD–CG amplifier of Fig. 7.41(c) for the case $g_m = 5$ mA/V, and $R_{sig} = R_L = 20$ kΩ. Neglecting r_o, find G_v.

****7.86** In each of the six circuits in Fig. P7.86, let $\beta = 100$, and neglect r_o. Calculate the overall voltage gain.

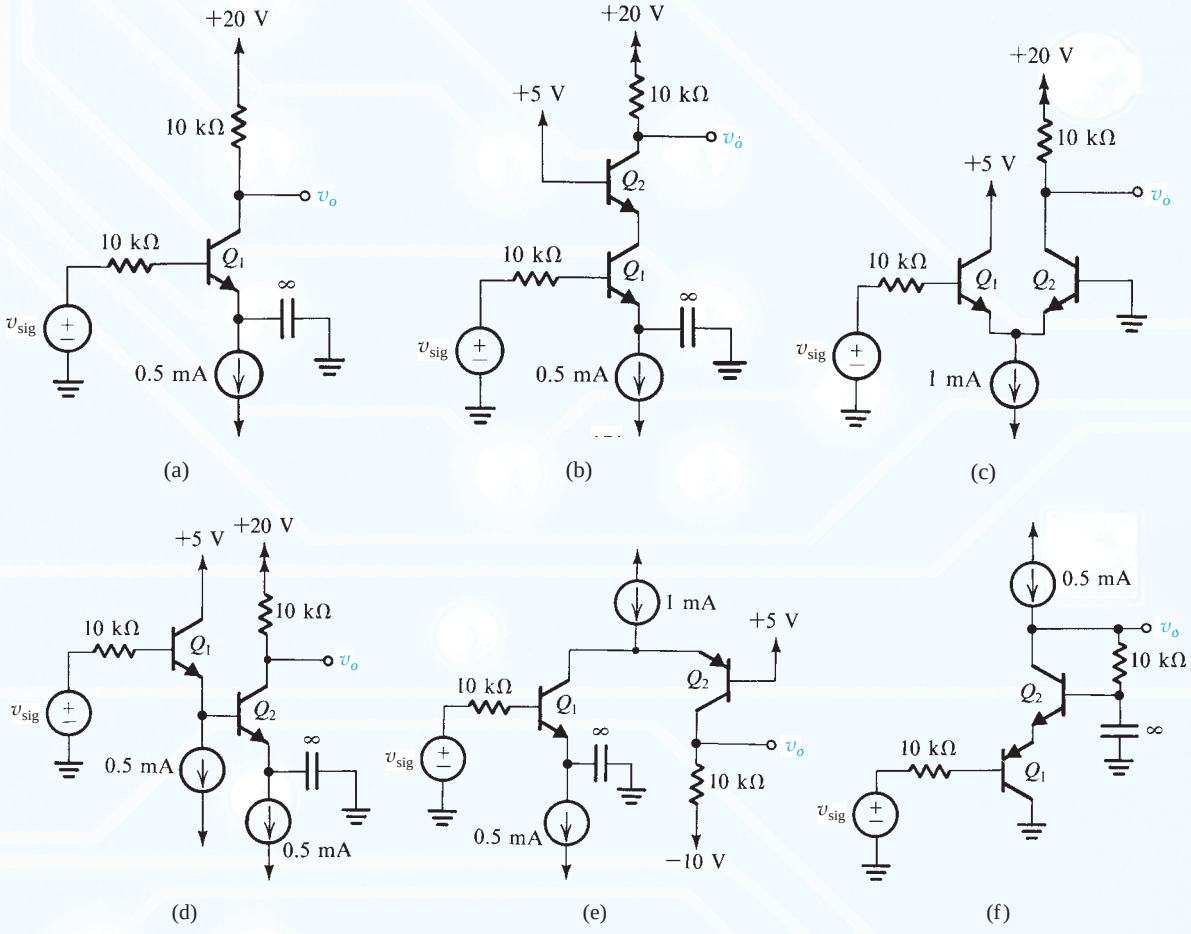


Figure P7.86

APPENDIX 7.A: Comparison of the MOSFET and the BJT

7.87 Find the range of I_D obtained in a particular NMOS transistor as its overdrive voltage is increased from 0.15 V to 0.4 V. If the same range is required in I_C of a BJT, what is the corresponding change in V_{BE}?

7.88 What range of I_C is obtained in an *npn* transistor as a result of changing the area of the emitter–base junction by a factor of 10 while keeping V_{BE} constant? If I_C is to be kept constant, by what amount must V_{BE} change?

7.89 For each of the CMOS technologies specified in Table 7.A.1, find the $|V_{OV}|$ and hence the $|V_{GS}|$ required to operate a device with a W/L of 10 at a drain current $I_D = 100$ µA. Ignore channel-length modulation.

7.90 Consider NMOS and PMOS devices fabricated in the 0.25-µm process specified in Table 7.A.1. If both devices are to operate at $|V_{OV}| = 0.25$ V and $I_D = 100$ µA, what must their W/L ratios be?

7.91 Consider NMOS and PMOS transistors fabricated in the 0.25-µm process specified in Table 7.A.1. If the two devices are to be operated at equal drain currents, what must the ratio of $(W/L)_p$ to $(W/L)_n$ be to achieve equal values of g_m?

7.92 An NMOS transistor fabricated in the 0.18-µm CMOS process specified in Table 7.A.1 is operated at $V_{OV} = 0.2$ V. Find the required W/L and I_D to obtain a g_m of 10 mA/V. At what value of I_C must an npn transistor be operated to achieve this value of g_m?

7.93 For each of the CMOS process technologies specified in Table 7.A.1, find the g_m of an NMOS and a PMOS transistor with $W/L = 10$ operated at $I_D = 100$ µA.

7.94 An NMOS transistor operated with an overdrive voltage of 0.25 V is required to have a g_m equal to that of an *npn* transistor operated at $I_C = 0.1$ mA. What must I_D be? What value of g_m is realized?

7.95 It is required to find the incremental (i.e., small-signal) resistance of each of the diode-connected transistors shown in Fig. P7.95. Assume that the dc bias current $I = 0.1$ mA. For the MOSFET, let $\mu_n C_{ox} = 200$ µA/V^2 and $W/L = 10$.

7.96 For an NMOS transistor with $L = 1$ µm fabricated in the 0.8-µm process specified in Table 7.A.1, find g_m, r_o, and A_0 if the device is operated with $V_{OV} = 0.5$ V and $I_D = 100$ µA. Also, find the required device width W.

7.97 For an NMOS transistor with $L = 0.3$ µm fabricated in the 0.18-µm process specified in Table 7.A.1, find g_m, r_o, and A_0 obtained when the device is operated at $I_D = 100$ µA with $V_{OV} = 0.2$ V. Also, find W.

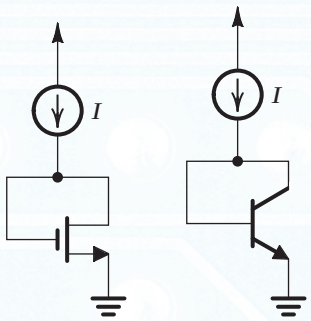


Figure P7.95

7.98 Fill in the table below. For the BJT, let $\beta = 100$ and $V_A = 100$ V. For the MOSFET, let $\mu_n C_{ox} = 200$ µA/V^2, $W/L = 40$, and $V_A = 10$ V. Note that R_{in} refers to the input resistance at the control input terminal (gate, base) with the (source, emitter) grounded.

	BJT		MOSFET	
Bias Current	$I_C = 0.1$ mA	$I_C = 1$ mA	$I_D = 0.1$ mA	$I_D = 1$ mA
g_m (mA/V)				
r_o (kΩ)				
A_0 (V/V)				
R_{in} (kΩ)				

7.99 For an NMOS transistor fabricated in the 0.18-µm process specified in Table 7.A.1 with $L = 0.3$ µm and $W = 6$ µm, find the value of f_T obtained when the transistor is operated at $V_{OV} = 0.2$ V. Use both the formula in terms of C_{gs} and C_{gd} and the approximate formula. Why does the approximate formula overestimate f_T?

7.100 An NMOS transistor fabricated in the 0.18-µm process specified in Table 7.A.1 and having $L = 0.3$ µm and $W = 6$ µm is operated at $V_{OV} = 0.2$ V and used to drive a capacitive load of 100 fF. Find A_0, f_P (or f_{3dB}), and f_t. At what I_D value is the transistor operating? If it is required to double f_t, what must I_D become? What happens to A_0 and f_P in this case?

7.101 For an *npn* transistor fabricated in the high-voltage process specified in Table 7.A.2, evaluate f_T at $I_C = 10$ µA, 100 µA, and 1 mA. Assume $C_\mu \simeq C_{\mu 0}$. Repeat for the low-voltage process.

7.102 Consider an NMOS transistor fabricated in the 0.8-μm process specified in Table 7.A.1. Let the transistor have L = 1 μm, and assume it is operated at I_D = 100 μA.

(a) For V_{OV} = 0.25 V, find W, g_m, r_o, A_0, C_{gs}, C_{gd}, and f_T.
(b) To what must V_{OV} be changed to double f_T? Find the new values of W, g_m, r_o, A_0, C_{gs}, and C_{gd}.

7.103 For a lateral *pnp* transistor fabricated in the high-voltage process specified in Table 7.A.2, find f_T if the device is operated at a collector bias current of 1 mA. Compare to the value obtained for a vertical *npn*.

7.104 Show that for a MOSFET the selection of L and V_{OV} determines A_0 and f_T. In other words, show that A_0 and f_T will not depend on I_D and W.

7.105 Consider an NMOS transistor fabricated in the 0.18-μm technology specified in Table 7.A.1. Let the transistor be operated at V_{OV} = 0.2 V. Find A_0 and f_T for L = 0.2 μm, 0.3 μm, and 0.4 μm.

D 7.106 Consider an NMOS transistor fabricated in the 0.5-μm process specified in Table 7.A.1. Let L = 0.5 μm and V_{OV} = 0.3 V. If the MOSFET is connected as a common-source amplifier with a load capacitance C_L = 1 pF (as in Fig. 7.A.2a), find the required transistor width W and bias current I_D to obtain a unity-gain bandwidth of 100 MHz. Also, find A_0 and f_{3dB}.

General Problem:

***7.107** The circuit shown in Fig. P7.107 is known as a **current conveyor**.

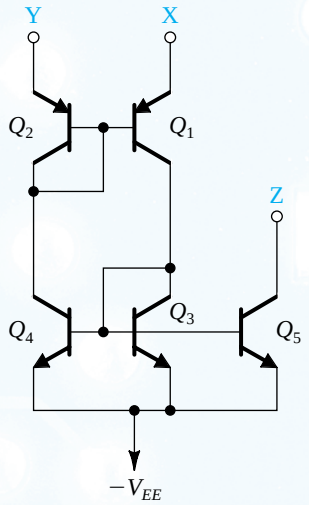


Figure P7.107

(a) Assuming that Y is connected to a voltage V, a current I is forced into X, and terminal Z is connected to a voltage that keeps Q_5 in the active region, show that a current equal to I flows through terminal Y, that a voltage equal to V appears at terminal X, and that a current equal to I flows through terminal Z. Assume β to be large. Corresponding transistors are matched, and all transistors are operating in the active region.
(b) With Y connected to ground, show that a virtual ground appears at X. Now, if X is connected to a +5-V supply through a 10-kΩ resistor, what current flows through Z?